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End-of-Fabrication CMOS Process Monitor

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ABSTRACT

A set of test "modules" for verifying the quality of a CMOS process at the end of the wafer fabrication is documented. By electrical testing of specific structures, over thirty parameters are collected characterizing interconnects, dielectrics, contacts, transistors, and inverters. Each test module contains a specification of its purpose, the layout of the test structure, the test procedures, the data reduction algorithms, and exemplary results obtained from 3-, 2-, or 1.6-micrometer CMOS/bulk processes. The document is intended to establish standard process qualification procedures for Application Specific Integrated Circuits (ASICs).

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PREFACE

The described procedures have evolved through their use in qualifying Application Specific Integrated Circuits (ASICs) fabricated through the USC/ISI MOSIS Project. Besides this Process Monitor, test chips for defect, parametric yield, and reliability analyses are under development at JPL.

The layout of the test structures of this Process Monitor is available from JPL on magnetic tape in CIF or Calma/GDSII format for selected CMOS/Bulk technologies. Presently 1.2-, 1.6-, 2.0-, and 3.0-μm processes are supported using MOSIS design rules. The authors invite critical comments and suggestions for improvement of this publication.

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Chapter 1

Introduction

This publication describes a CMOS Process Monitor for wafer level testing at the end of the wafer fabrication process. The test structures provide a "snapshot" of important process and device parameters and are key to the qualification of accompanying Application Specific Integrated Circuits (ASICs). The modular design of the structures allows for their placement in available space on ASIC wafers, including in saw kerfs. A Process Monitor Test Strip has been fabricated in 3.0-, 2.0-, 1.6-, and 1.2-μm CMOS/Bulk since 1982 through the USC/ISI MOSIS Project and used as a qualification tool for ASICs. The goal of this publication is to establish one part of a "workmanship" standard for ASIC qualification. It is aimed at design and test engineers with at least an undergraduate education. Publications specifying complementary test procedures for defect, parametric yield, and reliability analyses are in preparation.

The present publication contains a description of the procedures for designing, testing, and analyzing the following test structures:

1. Split-Cross-Bridge Resistor
2. Contact Resistor
3. MOSFET Capacitor
4. Field-oxide MOSFET
5. MOSFET: Gross parameters
6. MOSFET Quartet: Model parameters
7. Inverter
8. Ring Oscillator[1]
9. Timing Sampler[1]

The process and device parameters that are extracted from each structure are listed in Table 1.1. An overview of the test structure layout is given in Figs. 1.1 and 1.2 by a plot of the CMOS/Bulk Test Strip. All test structures are modular in design using 2 x N probe pad arrays. The details of the standard probe pad array (No. 1) and a compressed probe pad array (No. 2) are shown in Appendix A. For pad identification, a modular counting system is recommended which assigns odd numbers $(1, 3, ..., 2N-1)$ to the lower row of pads and even numbers $(2, 4, ..., 2N)$ to the upper row counting from left to right.

The description of each test structure is contained within a test module that includes the following elements:

1. Test module name and structure size
2. Purpose of the test structure
   List of extracted process/device parameters
3. Geometrical description/design principles
   List of critical design parameters
4. Test procedure
   - 4.1 Circuit diagram
   - 4.2 Test conditions
     List of test input/output parameters
   - 4.3 Data reduction algorithms
     List of auxiliary process/device parameters
5. Test results
   List of extracted parameter values
6. References and further reading

In this publication the test module name is given in the chapter heading. The size is given in terms of required terminals, i.e., number of probe pads. For structures which do not fit in the space between the pads, the additional external space requirement is roughly estimated in an equivalent number of pads.

The purpose of the test module is generally stated by a *list of process or device parameters* which we want to extract. (Intermediate parameters are listed in parentheses.)

The geometrical description is given in terms of layer/mask names used by

[1]These more complex test structures are somewhat beyond the scope of a process monitor. Furthermore, their design depends quite on the specific process and its rules. They are, therefore, treated here rather briefly, and the interested reader should refer to the cited literature.

Table 1.1: Parameters Extracted from the CMOS Process Monitor

Test Structure	Parameter	Parameter Name
Split-Cross-Bridge Resistor	R_s	Sheet resistance
	W_e, S_e	Minimum linewidth, spacing
	P_e	Pitch
	Q_P	Quality factor
Contact Resistor	R_I	Interfacial contact resistance
	ρ	Interfacial contact resistivity
MOSFET Capacitor	T_{ox}	Gate oxide thickness
	C'_{ox}	Gate-oxide capacitance/area
	C'_{go}	Gate-overlap capacitance/length
Field-Oxide MOSFET	V_{Tfield}	Field oxide threshold voltage
MOSFET:	I_{DSoff}	Channel leakage current
Gross Parameters	I_{DBleak}	Drain diode leakage current
	I_{GBleak}	Gate leakage current
	I_{DSon}	Transistor on current
	V_{DBbd}	Drain diode breakdown voltage
MOSFET Quartet:	K_P	Intrinsic conduction factor
Model Parameters	$\Delta L, \Delta W$	Decrease in channel length, width
(Main parameters,	δ	Secondary body coefficient
complete list	ϵ	Velocity saturation coeff.
in Table 7.1)	θ, θ_B, η	Gate-field, Body-voltage, Drain-field mobility degradation coeff.
	λ	Channel length modulation coeff.
	$\gamma, \gamma_z, \gamma_M$	Body effect, Body-current, M-factor body effect coeff.
	M_0	Intrinsic M-factor
	V_{it}	Interface trap voltage
	V_{FB0}	Flatband voltage less V_{it}
Inverter	V_{Tinv}	Inverter threshold voltage
	V_{OL}, V_{OH}	Inverter output voltages
	G	Inverter gain
	V_{nm}	Inverter noise margin
Ring Oscillator	–	Gate delay
Timing Sampler	–	Inverter propagation delay

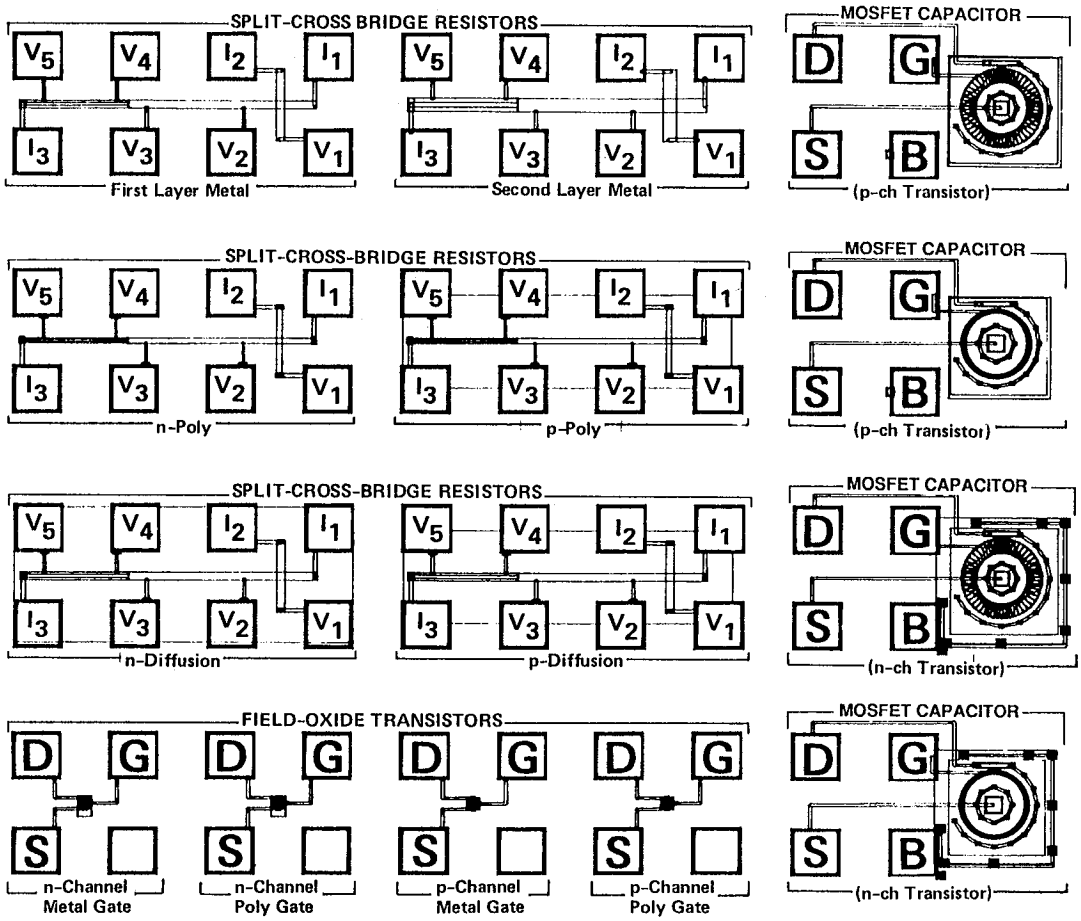

Figure 1.1: CMOS/bulk test strip based on probe pad array No. 1, Part 1

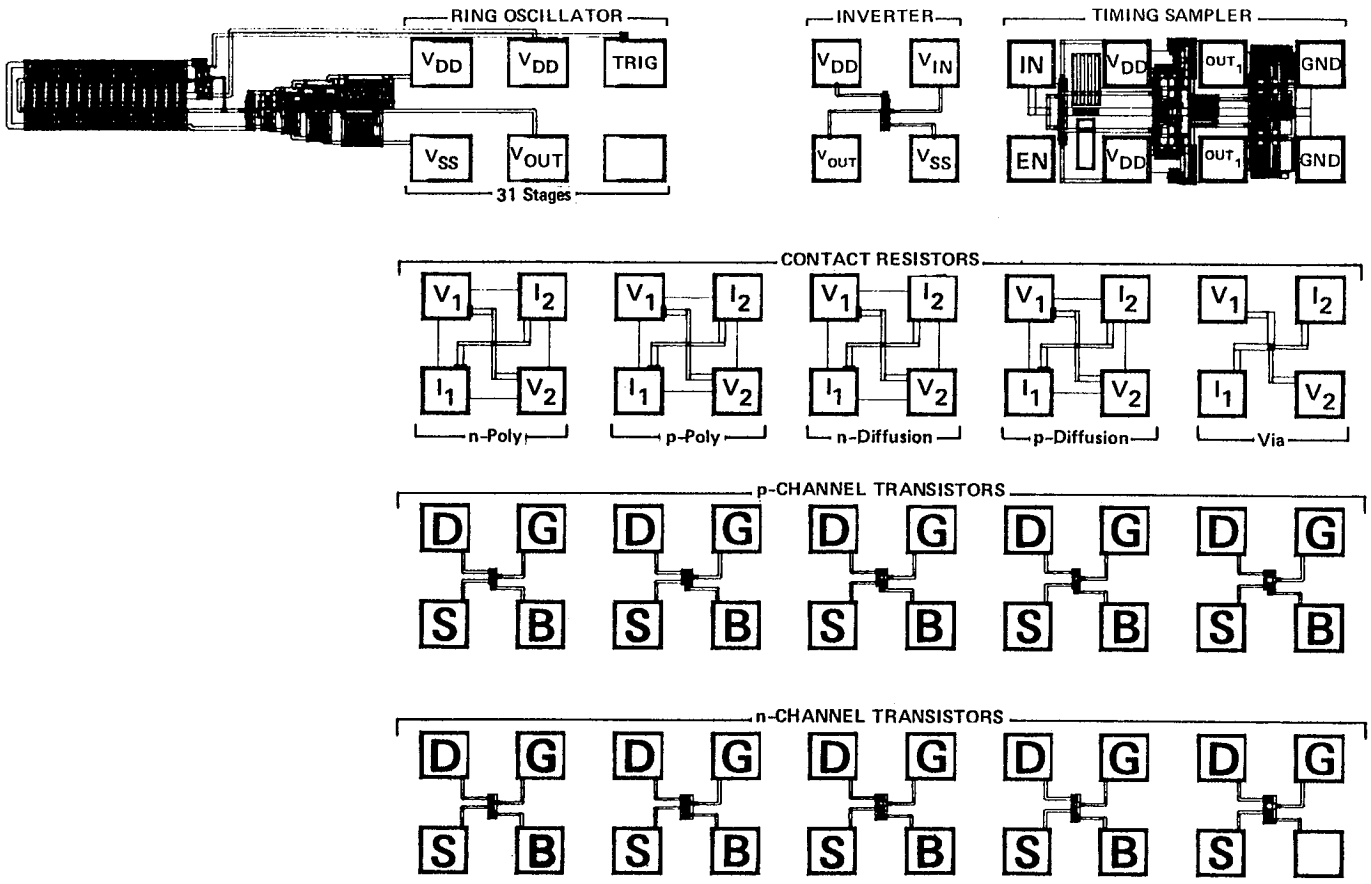

Figure 1.2: CMOS/bulk test strip based on probe pad array No. 1, Part 2

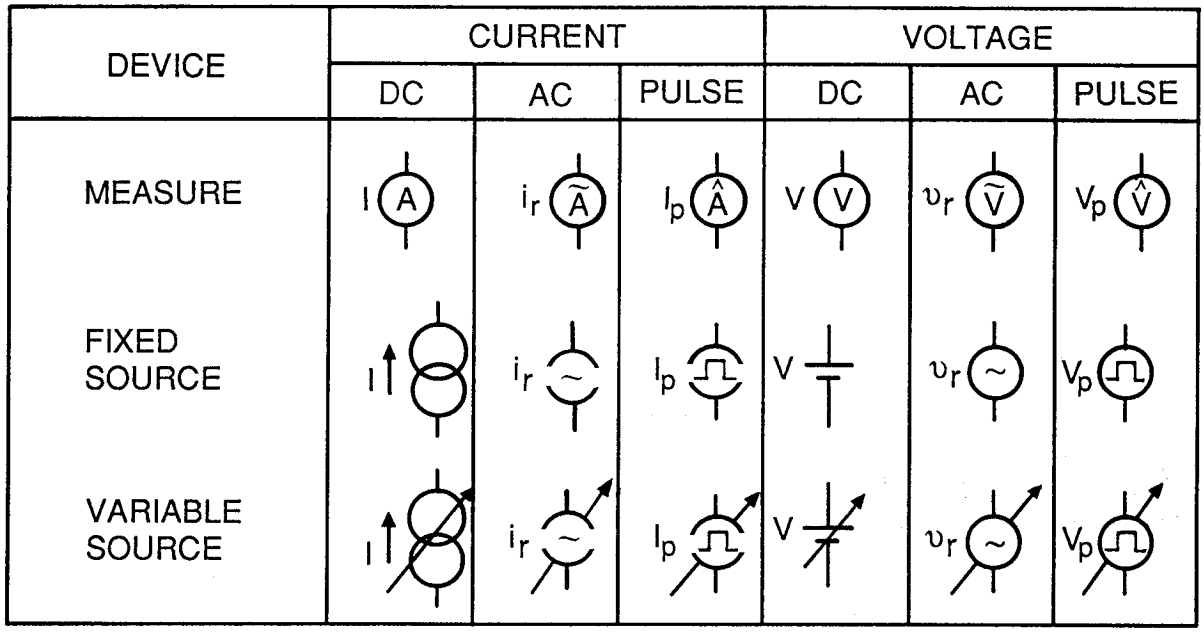

Figure 1.3: Electrical Symbols for Current, Voltage, Measure, and Source Devices.

MOSIS for the P-well process. Conversion to N-well or twin-well is left to the reader. MOSIS' layer definitions and design rules are given in Appendix B. Note specifically that ACTIVE means an area under thin oxide, which becomes N^+-doped (e.g., source/drain of a transistor) except under POLY (e.g., gate of transistor), where it has the doping of the N-bulk or P-well, and under SELECT, where it becomes P^+-doped. The geometrical description is accompanied by a *list of critical design parameters*. Some parameters are given in multiples of λ, where 2λ is the minimum gate length of the process, e.g., $\lambda = 0.6$ μm for a 1.2-μm process.

The circuit diagrams contain a symbolic or equivalent circuit representation of the device under test connected to symbolized measurement instruments. The symbols used in this publication are listed in Figs. 1.3 to 1.4. Where possible, the symbols were taken from an IEEE standard [1.1]. Where a symbol could not be found, a commonly used symbol is indicated.

The data reduction algorithms start with the listed *test output parameters* and the *auxiliary process/device parameters* as input and generate values for the *extracted process/device parameters* listed in the "purpose" section.

Finally, exemplary test results are given as an orientation to the test engineers in judging their own data.

CIRCUIT ELEMENT	SYMBOL
1. POWER TERMINATION	
2. GROUND TERMINATION	
3. WIRE INTERCONNECT	 OR 
4. WIRE CROSSING	

Figure 1.4: Electrical Symbols for Wire Crossing, Interconnect, and Terminations.

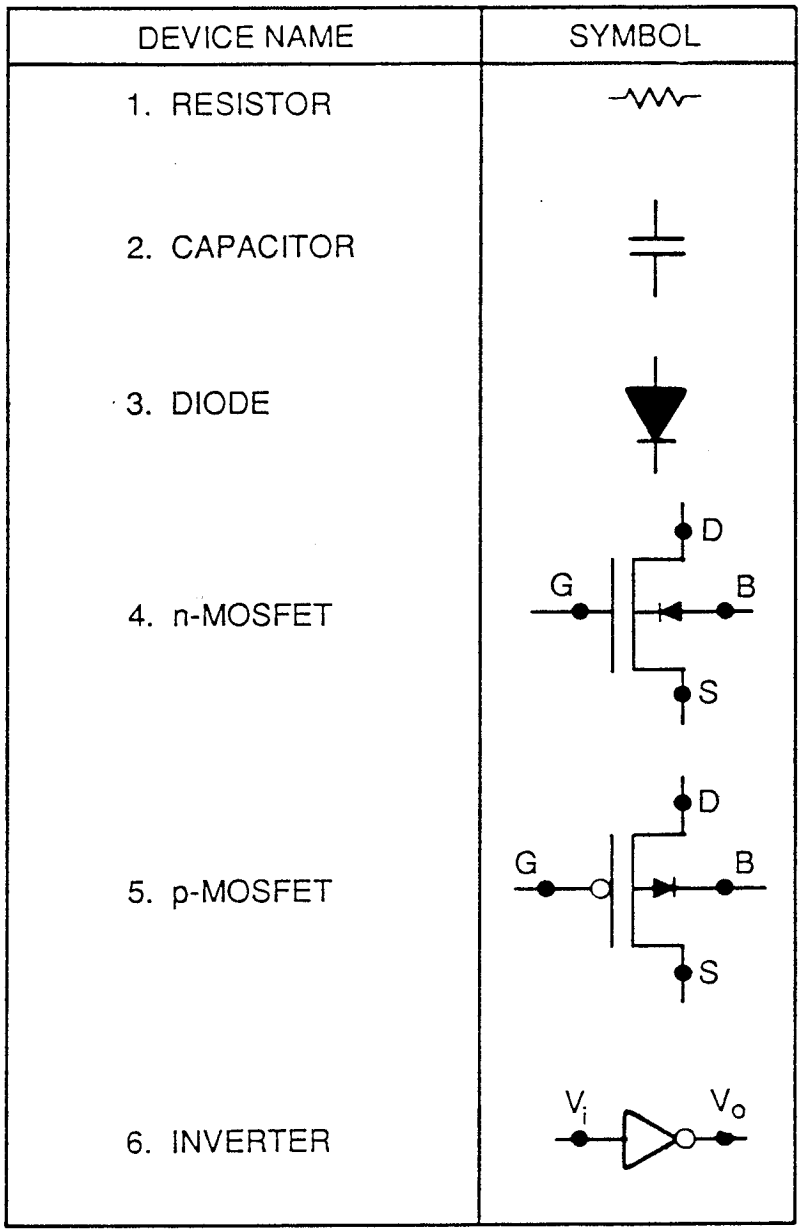

Figure 1.5: Electrical Symbols for Devices.

REFERENCE:

1.1 *Electrical and Electronics Graphic Symbols and Reference Designations*, IEEE, New York (1987)

Chapter 2

Split-Cross-Bridge Resistor

2.1. TEST MODULE: The Split-Cross-Bridge Resistor is an 8-terminal structure fitting completely within a 2 x 4 pad array.

2.2. PURPOSE: Split-Cross-Bridge Resistors are used to measure sheet resistance as well as width, spacing, and pitch of conducting lines designed to their minimum rule. One structure is needed for each conducting layer, i.e., the polysilicon layer, the (junction isolated) diffused layers, and the metal layers. The relative deviation of the extracted pitch from the designed one serves as a quality factor indicating geometry-dependent processing and/or other problems like a magnification error, lack of homogeneity in sheet resistance or linewidth, and probe/instrument errors. The extracted parameters are listed in Table 2.1. The extracted values of the geometrical quantities have been given the index e in order to distinguish them from the design values.

Table 2.1: Parameters extracted from Split-Cross-Bridge Resistor

Parameter	Parameter Name
R_s	Sheet resistance
(W_{be}	Bridge linewidth)
W_e	Minimum design rule linewidth
S_e	Minimum design rule line spacing
P_e	Line Pitch
Q_P	Quality Factor

2.3. GEOMETRICAL/DESIGN PRINCIPLES: The Split-Cross-Bridge Resistor

[2.1], shown in Figure 2.1, consists of a van-der-Pauw cross [2.2] (left), a bridge section (middle), and a split-bridge section (right). The split-bridge is layed out so that design linewidth W and spacing S have the minimum dimensions set by the design rules. The design line pitch is then $P = W + S$. The design linewidth of the (unsplit) bridge must be layed out as $W_b = 2W + S$. The width of the four arms of the cross is usually chosen as W_b, too. Four additional geometrical

Table 2.2: Critical design parameters for Split-Cross-Bridge Resistor

Parameter	Parameter Name	Value
W	Split-bridge linewidth	Minimum design rule
S	Split-bridge spacing	Minimum design rule
W_b	Bridge linewidth	$W + 2S$
P	Line Pitch	$W + S$

rules must be followed when designing the Split-Cross-Bridge Resistor so that the results are accurate to better than one percent [2.1]. Rule No. 1 requires that the length of each of the four arms of the cross be at least twice the width of the arm ($L_c \geq 2W_b$) [2.3]. This allows the use of the van-der-Pauw Equation (2.1) for the sheet resistance. Rule No. 2 requires that the voltage taps of the bridges (terminals 4 to 7) be of minimum width W and that the distances between the taps (L_b and L_s) be large enough so that the as-drawn distance between taps can be used directly in the calculations. Rule No. 3 requires that the length of the bridge voltage taps be at least twice the tap width. Rule No. 4 requires that the separation of a voltage tap from a discontinuity in the line be at least twice the linewidth. The critical design parameters are summarized in Table 2.2.

2.4. TEST PROCEDURE:

2.4.1. Sheet resistance, R_s:

2.4.1.1. Circuit diagrams: The circuit diagrams shown in Figures 2.2 and 2.3 indicate that a current source is applied to two adjacent terminals of the van-der-Pauw cross and a voltmeter is applied to the other two terminals. The remaining terminals are allowed to float electrically.

2.4.1.2. Test conditions: R_s is determined from the average of four resistance measurements. The first two resistances are determined by measuring V_{24}, i.e., voltage between terminals 2 and 4, for I_{13} , i.e., a current between terminals 1 and 3, forced in each direction (Figure 2.2). The second two resistances are determined analogously by measuring the voltage V_{34} for a current I_{12} forced in each direction (Figure 2.3). The magnitude of these "van-der-Pauw" currents is chosen the

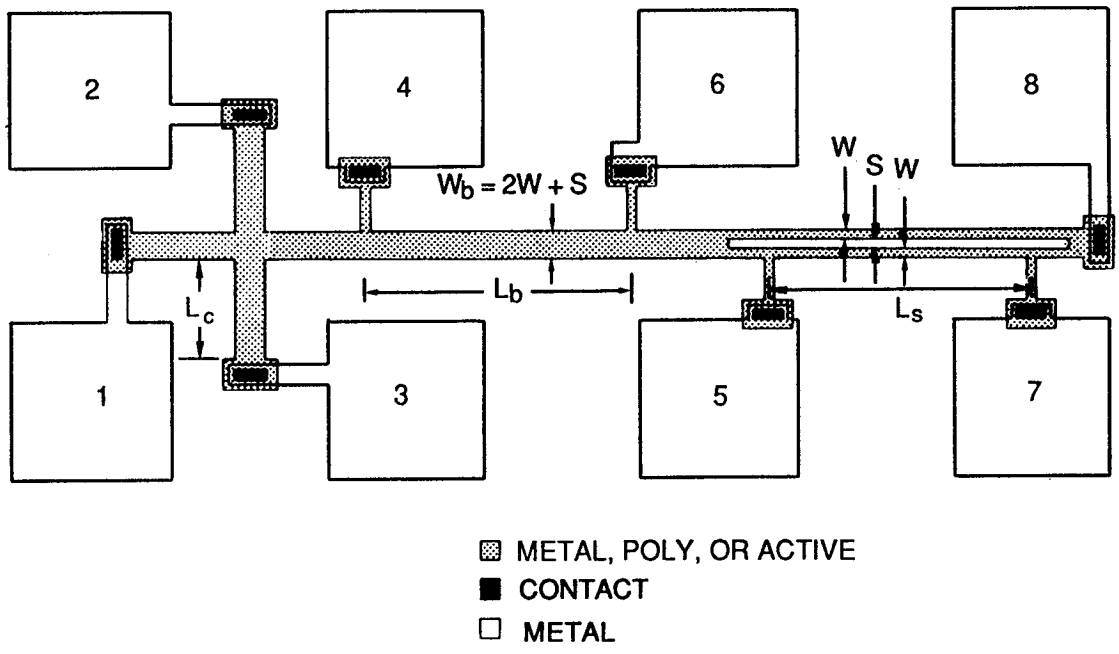

Figure 2.1: Layout of the Split-Cross-Bridge Resistor.

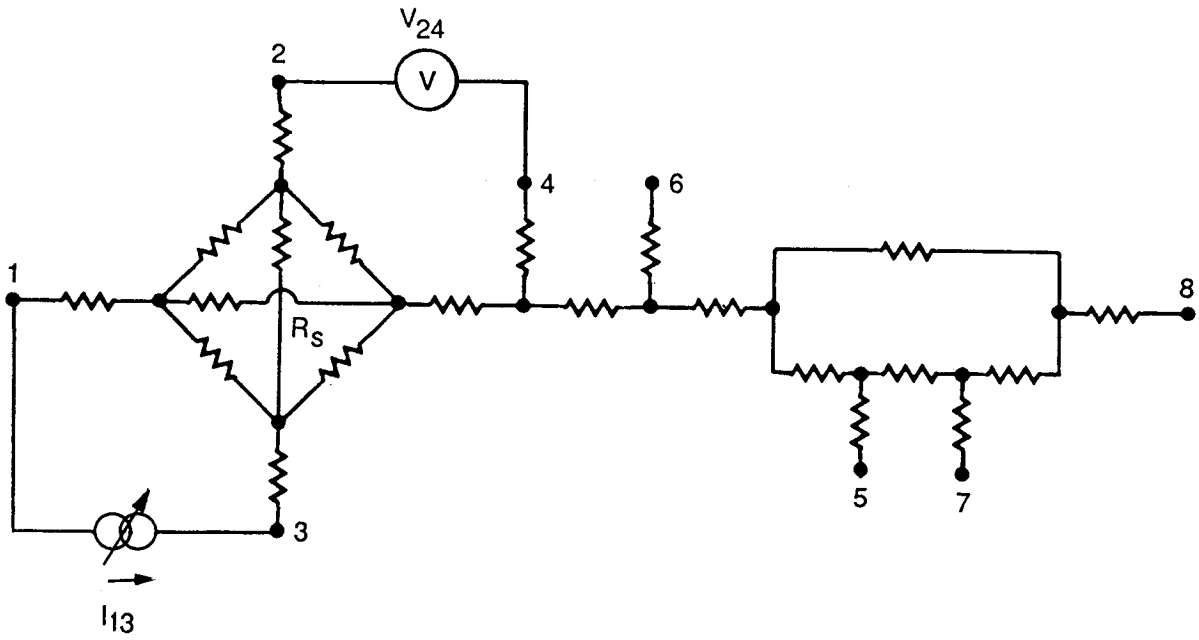

Figure 2.2: Split-Cross-Bridge Resistor sheet resistance, R_s, measurement circuit, configuration No. 1. (The van-der-Pauw structure has been represented by a 6-resistor network.)

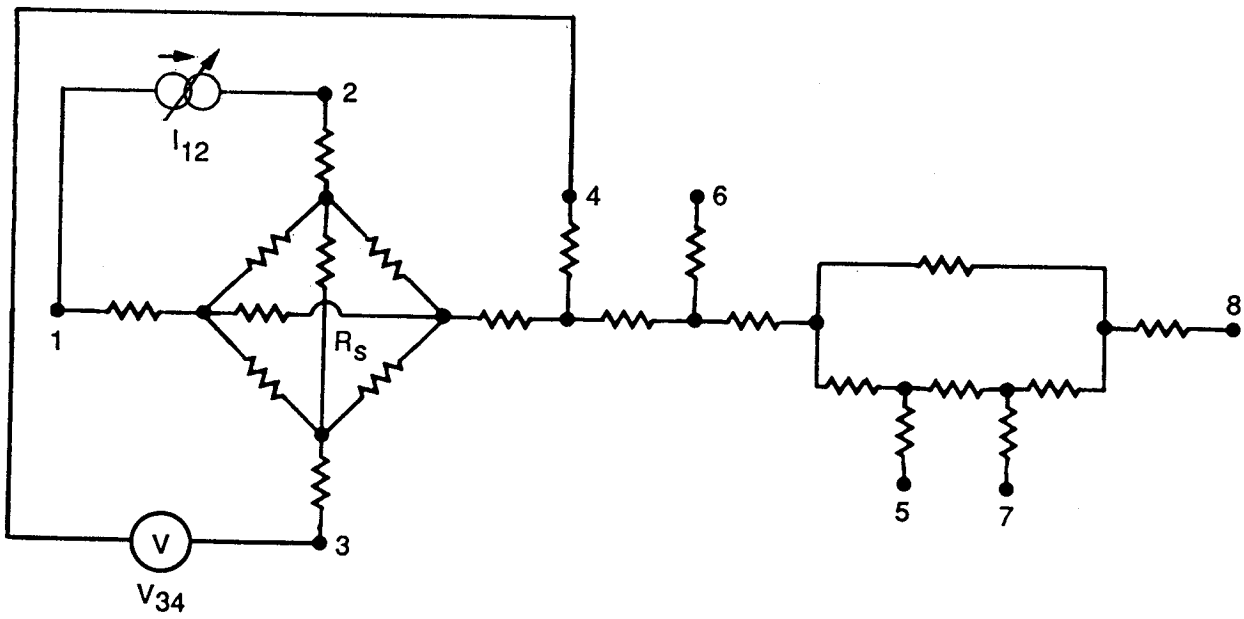

Figure 2.3: Split-Cross-Bridge Resistor van-der-Pauw sheet resistance, R_s, measurement circuit, configuration No. 2.

same for all four van-der-Pauw voltage measurements so that only the magnitudes of the four measured voltages need to be averaged. This current magnitude, called I_v, is adjusted so that the magnitude of the measured voltages is between 1 and 10 mV. This condition allows the voltage to be measured accurately with a floating voltmeter having 1 μV resolution and also prevents spurious current flow in junction-isolated layers due to junction forward biasing or junction breakdown. A list of test input/output parameters is given in Table 2.3.

Table 2.3: Test input/output parameters for Split-Cross-Bridge Resistor

Input parameter	Value	Output parameter
I_{13}	$\pm I_v$	$V_{24}(\pm I_v)$
I_{12}	$\pm I_v$	$V_{34}(\pm I_v)$
I_{18}	$\pm I_b$	$V_{46}(\pm I_b)$, $V_{57}(\pm I_b)$

2.4.1.3. Data reduction algorithm: R_s is derived from the van-der-Pauw Equation [2.2]:

$$R_s = \frac{\pi}{\ln 2}\frac{V_v}{I_v} = 4.53\frac{V_v}{I_v}. \tag{2.1}$$

In this equation $V_v = (|V_{24}(+I_v)| + |V_{24}(-I_v)| + |V_{34}(+I_v)| + |V_{34}(-I_v)|)/4$ is the average magnitude of the van-der-Pauw voltages with $I_v = |I_{13}| = |I_{12}|$, cf. Fig. 2.2 and Fig. 2.3.

2.4.2. Effective bridge linewidth, W_{be}: This is an intermediate parameter needed for the calculation of the effective line spacing and pitch, see below.

2.4.2.1. Circuit diagram: See Figure 2.4.

2.4.2.2. Test conditions: The bridge voltage V_{46} is measured between terminals 4 and 6 while a bridge current I_{18} is forced between terminals 1 and 8. The magnitude of that bridge current is called I_b and is set so the measured voltage is between 1 and 10 mV. The procedure is repeated with the current reversed and the voltage magnitudes averaged.

2.4.2.3. Data reduction algorithm: The effective bridge width W_{be} is derived from

$$W_{be} = \frac{R_s L_b I_b}{V_b}, \tag{2.2}$$

where $V_b = (|V_{46}(+I_b)| + |V_{46}(-I_b)|)/2$ is the average magnitude of the bridge voltages and $I_b = |I_{18}|$, cf. Figure 2.4, and L_b is the designed distance between the taps shown in Figure 2.1.

2.4.3. Effective (split-bridge) linewidth, W_e:

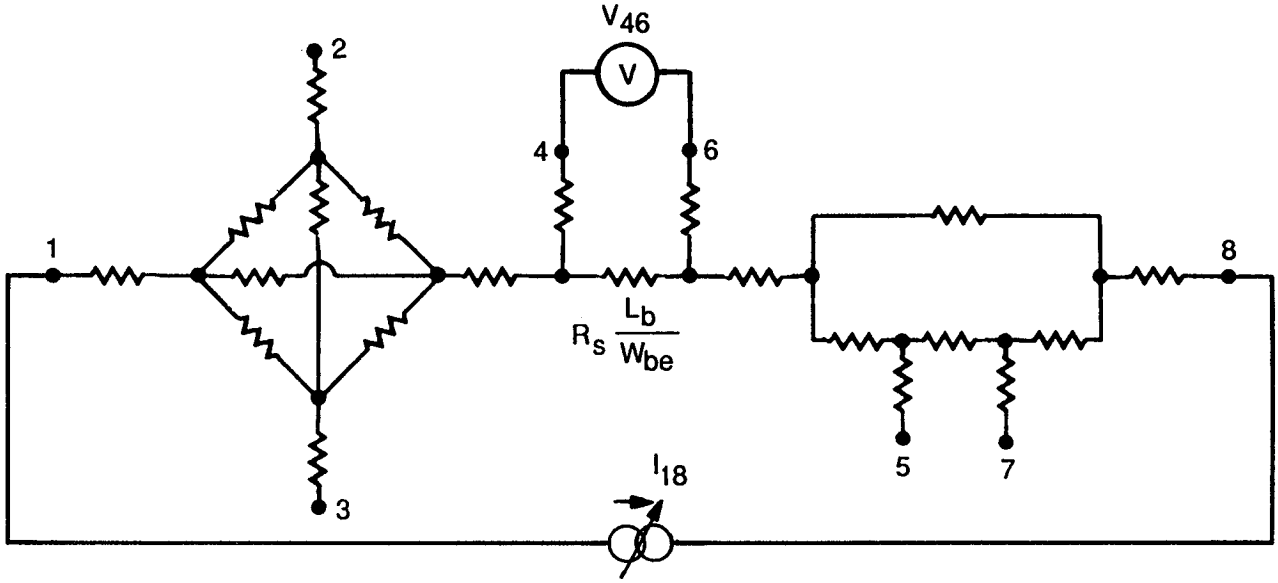

Figure 2.4: Split-Cross-Bridge Resistor bridge linewidth, W_{be}, measurement circuit.

2.4.3.1. Circuit diagram: See Figure 2.5.

2.4.3.2. Test conditions: The split-bridge voltage V_{57} is measured between terminals 5 and 7 while a split-bridge current I_{18} is forced between terminals 1 and 8 with its current magnitude, I_s, set so the measured voltage is between 1 and 10 mV. The procedure is repeated with the current reversed and the voltage magnitudes averaged.

2.4.3.3. Data reduction algorithm: The linewidth is

$$W_e = \frac{R_s L_s I_s}{2V_s}. \tag{2.3}$$

In this equation, $V_s = (|V_{57}(+I_s)| + |V_{57}(-I_s)|)/2$ is the average magnitude of the split-bridge voltage with $I_s = |I_{18}|$, and L_s is the distance between the voltage taps of the split bridge shown in Figure 2.1. Note the factor 2 in Eq. 2.3 indicating that only one half of the external current is flowing through the tapped section of the split-bridge.

2.4.4. Effective line spacing, S_e, effective pitch, P_e, and quality factor Q_P:

2.4.4.1. Data reduction algorithm: The effective line spacing is given by, cf. Fig. 2.1,

$$S_e = W_{be} - 2W_e, \tag{2.4}$$

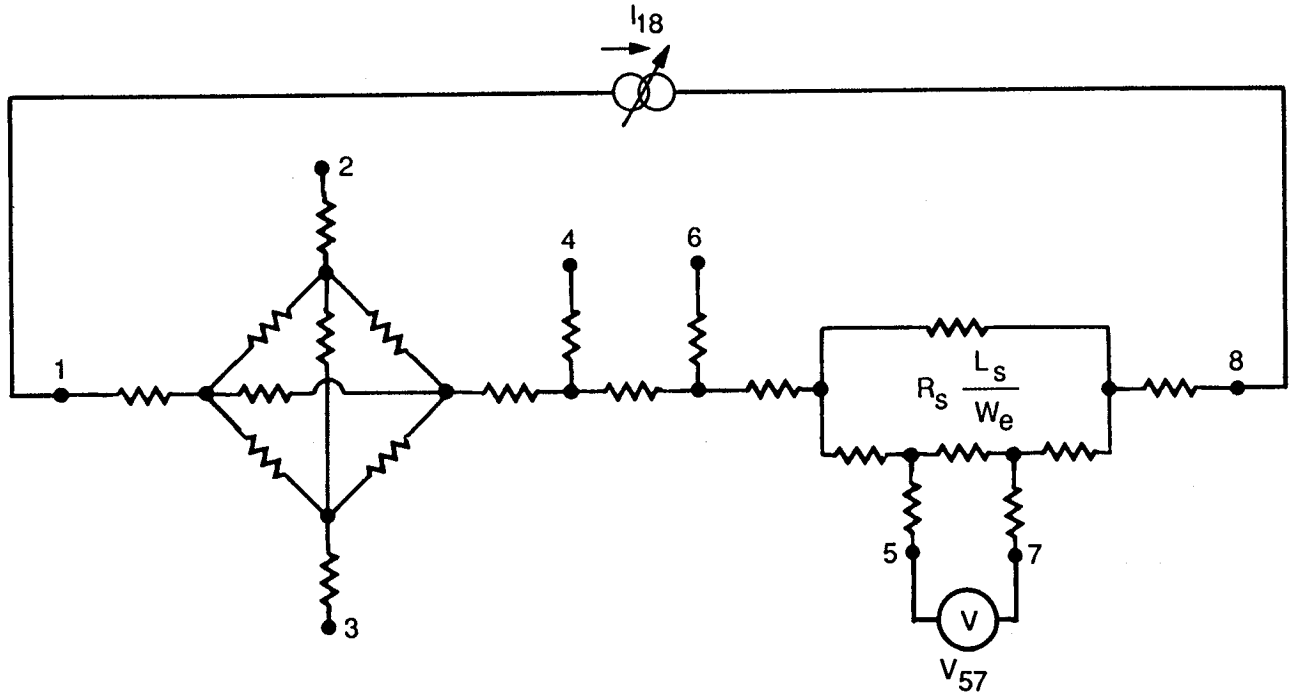

Figure 2.5: Split-Cross-Bridge Resistor split-bridge linewidth, W_e, measurement circuit.

where W_{be} and W_e are given by Eqs. 2.2 and 2.3, respectively. Similarly, the effective pitch is

$$P_e = W_{be} - W_e. \tag{2.5}$$

As a quality check, the extracted pitch, P_e, is compared to the design pitch, $P = W + S = W_b - W$. The quality factor for the Split-Cross Bridge Resistor expressed in percentage is

$$Q_P = \frac{P_e - P}{P} \times 100, \tag{2.6}$$

where P_e is given by Eq. 2.5.

2.5. TEST RESULTS: Exemplary test results are given in Table 2.4

Table 2.4: Results from Split-Cross-Bridge Resistors

Parameter	Poly	Metal	N^+-Diffusion
R_s [$\Omega/\square$]	16.8	39.3m	36.6
W_e (W) [μm]	2.08 (3.00)	4.36 (4.50)	5.45 (4.50)
S_e (S) [μm]	3.92 (3.00)	4.61 (4.50)	3.57 (4.50)
P_e (P) [μm]	6.01 (6.00)	8.97 (9.00)	9.02 (9.00)
Q_P [%]	+0.2	-0.3	-0.2

2.6. REFERENCES:

2.1. M. G. Buehler and C. W. Hershey, "The Split-Cross-Bridge Resistor for Measuring the Sheet Resistance, Linewidth, and Line Spacing of Conducting Layers," *IEEE Trans. Elec. Dev.*, **ED-33**, 1572 (1986)

2.2. L.J. van der Pauw, "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape," *Philips Res. Rept.*, **13**, 1 (1958)

2.3. M. G. Buehler, S. D. Grant, and W. R. Thurber, "Bridge and van der Pauw Sheet Resistors for Characterizing the Line Width of Conducting Layers," *J. Electrochem. Soc.*, **125**, 650 (1978)

Chapter 3

Contact Resistor

3.1. TEST MODULE: Two structures are offered in this module, the 4-Terminal D-Contact Resistor and the 6-Terminal L-Contact Resistor[1]. The 4- and 6-terminal structures fit completely within 2 x 2 and 2 x 3 pad arrays, respectively. A criterion will be given by which it can be judged whether the more economic 4-terminal structure is sufficient.

3.2. PURPOSE: To determine the interfacial resistance, R_I, of a contact between two conducting layers and calculate the interfacial resistivity, ρ, by multiplying R_I with the area of the contact. In order to establish that ρ is a true process parameter (i.e., independent of area), the resistances of at least two contacts with different areas must be measured. The presented methods have been applied to metal/poly, metal/diffusion, and metal/metal contacts. We found that, if properly measured, ρ is usually indeed independent of area, except in undersized contacts. However, mean and standard deviation of ρ, taken over a wafer, can vary widely from wafer to wafer. For that reason we chose a method which measures directly this critical parameter in contrast to the otherwise often used Transmission-Line Tap Resistor, see, e.g., [3.3]. The extracted parameters are listed in Table 3.1.

[1]In this publication the labels D and L characterize the shape of the current/voltage taps rather than their arrangement, cf. the following sections. The use of these labels in this sense is now common in the literature although not in accord with their origin, see, e.g., [3.3].

Table 3.1: Extracted Contact Resistor Parameters.

Parameter	Parameter Name
(R_{4D}	4-terminal D-contact resistance)
(R_{6L}	6-terminal L-contact resistance)
R_I	Interfacial contact resistance
ρ	Interfacial contact resistivity

3.3. 4-TERMINAL D-CONTACT RESISTOR:

3.3.1. *Geometrical Description/Design Principles:* The layout of the D-Contact Resistor is shown in Figure 3.1. The square contact of length d is probed with a voltage tap V_i and a current tap I_i in each of the two conducting layers ($i = 1, 2$). The taps have the same width as the contact except in the vicinity of the contact, where they widen to a "flange" allowing for misalignments between the conducting layers and the contact window in the isolating dielectric layer. This dogbone shape of the taps is the origin of the label D. With the current taps in line, as shown in the figure, and flange widths, δ_1 and δ_2, approaching zero, the horizontal current flow is approximately 1-dimensional, and the measured 4-terminal resistance, R_{4D} approaches the interfacial contact resistance, R_I.

For finite flange widths, R_{4D} is somewhat larger than R_I due to lateral current flow in the flanges around the contact. The dogbone design minimizes the flange effect; however, the complex geometry has so far prohibited an analytical treatment which would allow calculation of R_I from R_{4D}. The following criterion for the validity of the approximation $R_I \approx R_{4D}$ has been derived from simulations [3.1], [3.2], [3.3]: For the case where $\delta_1 = \delta_2 = \delta$, the measured contact resistance R_{4D} differs from R_I by less than 20 percent, or $0.8R_{4D} < R_I < R_{4D}$, provided

$$\Gamma \equiv \frac{R_{4D}}{R_{S1} + R_{S2}} \left(\frac{d}{\delta}\right)^{1.2} > \gamma, \tag{3.1}$$

where R_{S1} and R_{S2} are the sheet resistances of layers 1 and 2, respectively, and $\gamma = 0.65$. This relation is plotted in Fig. 3.2. The shaded area is the region in which R_D differs from R_I by less than 20 percent.

Noting in Eq. 3.1 that $R_{4D} \approx R_I = \rho/d^2$, we obtain the smallest interfacial resistivity which can be reasonably measured with this test structure as

$$\rho_{min} = \gamma(R_{S1} + R_{S2})\delta^{1.2}d^{0.8}. \tag{3.2}$$

This ρ_{min} should be minimized by designing d and δ to the minimum dimensions which are compatible with the process design rules and the structural requirements

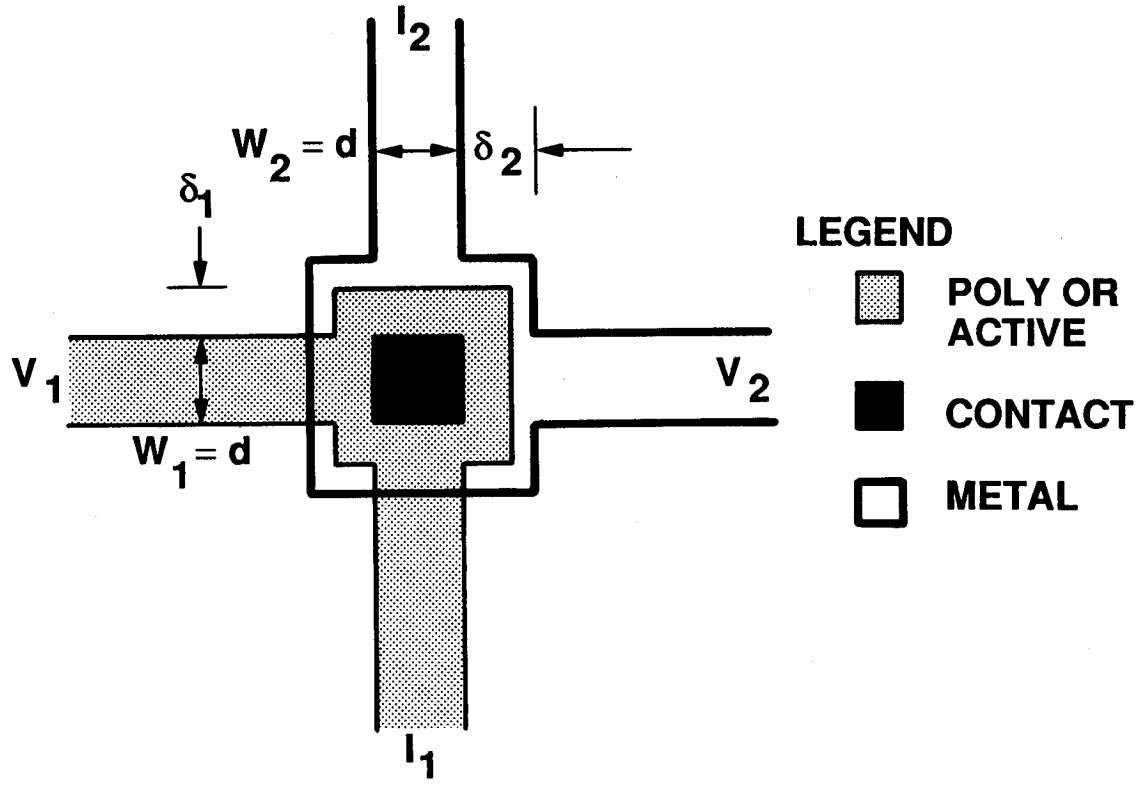

Figure 3.1: Layout of a metal-poly 4-Terminal D-Contact Resistor

of the D-Contact Resistor. We conclude the following set of design rules for the 4-Terminal D-Contact Resistor:

1. Design contact width $d = d_{min}$, where d_{min} is equal to the larger of the following minimum design rules: contact width, first layer linewidth, and second layer linewidth.
2. Design flange widths $\delta_1 = \delta_2 = \delta_{min}$, where δ_{min} is equal to the larger of the minimum design rules for contact overlap in the two layers.
3. Design the tap widths W_1 and W_2 equal to the contact width d.

If ρ_{min} is larger than the maximum value tolerable, e.g. in an ASIC, the D-Contact Resistor should not be used. For metal-semiconductor contacts use the 6-Terminal L-Contact Resistor instead. For metal-metal contacts, see [3.5]. If the area independence of ρ is to be established, a second contact resistor with twice the minimum contact width is recommended. Table 3.2 summarizes the critical design parameters.

The simulations which lead to formulas 3.1 and 3.2 were made for hypothetical perfectly aligned contacts. Fortunately, effects on R_{4D} of misalignments in opposite directions cancel each other to first order, so that the relations hold for averages from samples with random misalignments. For individual 4-Terminal D-Contact Resistors, the design flange width δ in those formulas should be replaced by an effective flange width of 2δ accounting approximately for the worst case of

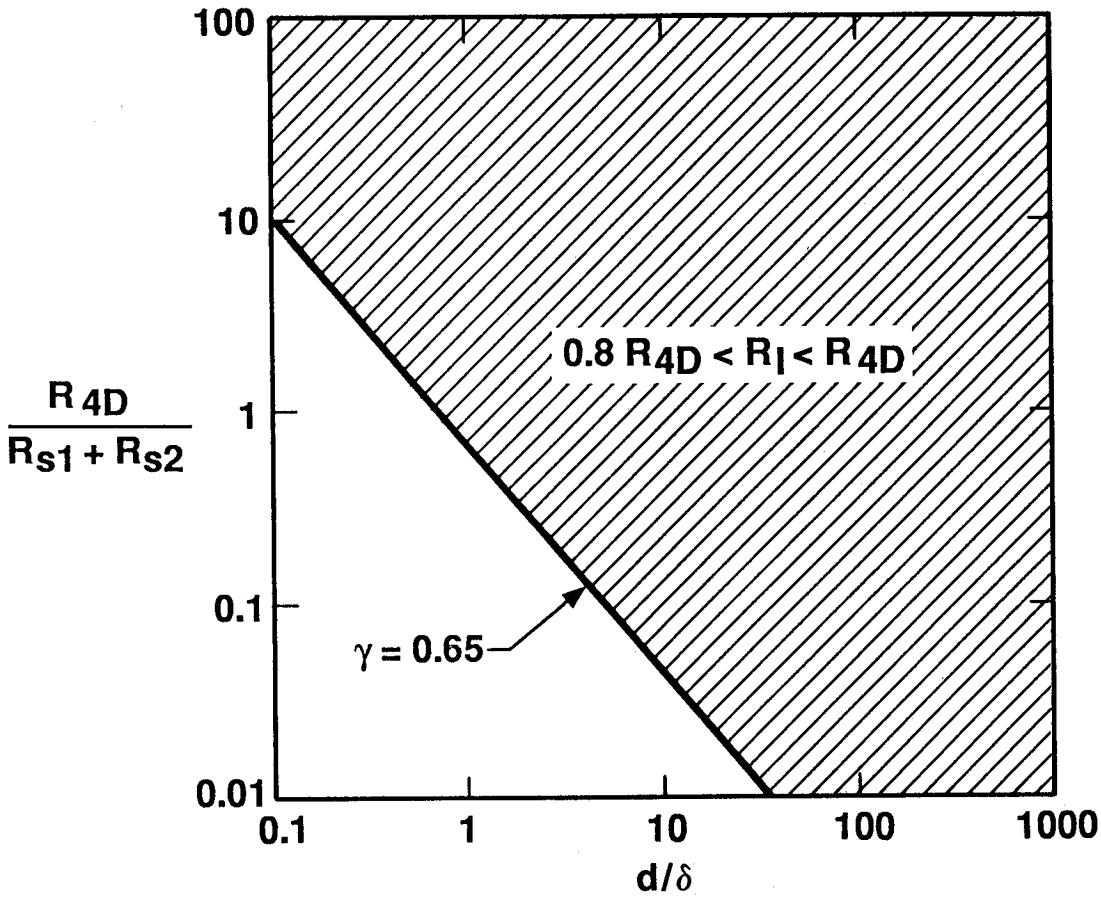

Figure 3.2: Useful parameter zone for 4-Terminal D-Contact Resistors. In the shaded area the measured and misalignment corrected 4-Terminal D-Contact Resistance, R_{4D}, equals the interfacial resistance, R_I, within 20 percent. For measured contact resistances from which misalignment effects have not been removed the value of δ should be replaced by 2δ.

Table 3.2: Critical design parameters for 4-Terminal D-Contact Resistor

Parameter	Parameter Name	Value
d	Contact length = contact width	$d_{min}[, 2d_{min}]$
δ_1, δ_2	Flange widths in layers 1,2	δ_{min}
W_1, W_2	Tap widths in layers 1,2	d

misalignment.

In general, if the validity criterion, Eq. 3.1, for the 4-Terminal D-Contact Resistor is not met, the results from that structure can be stated only in the form $R_I < R_{4D}$. This will usually be sufficient for metal-to-metal contacts.

3.3.2. *Test Procedure:*

3.3.2.1. Circuit diagram: See Figure 3.3.

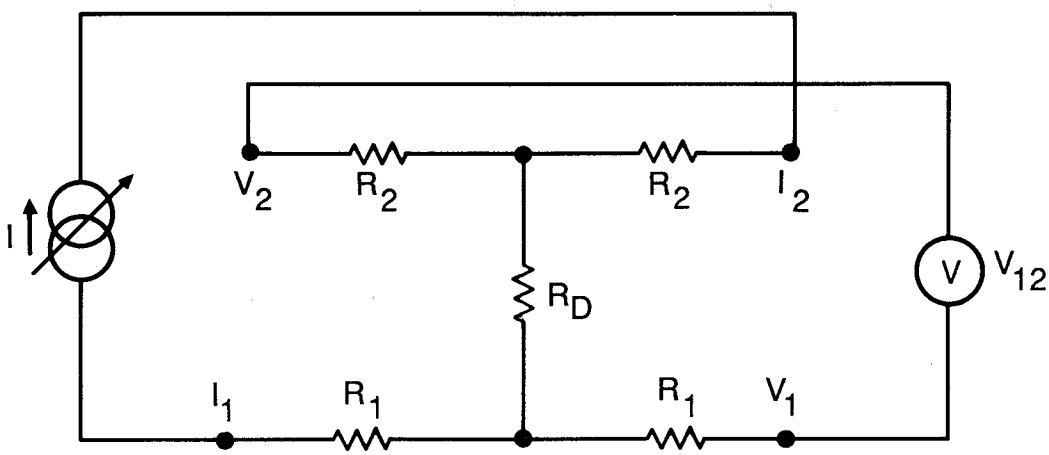

Figure 3.3: Measurement of 4-terminal D-contact resistance, R_{4D}

3.3.2.2. Test conditions: R_{4D} is determined from the average of two resistance measurements. The resistances are determined by measuring the voltage V_{12} between points V_1 and V_2 for current forced in both directions between points I_1 and I_2. If the current magnitude, I, is the same in both the forward and reverse directions, then the resistance can be determined from the average of the voltage measurements. The magnitude of the current is adjusted so that the measured voltage is between 1 and 10 mV. In the case of the metal-metal via, the higher current density needed to achieve this voltage may cause Joule heating which could affect the results. This possibility should be recognized in any test and an upper current bound be set for the test. Joule heating can be identified by taking resistance measurements at higher current levels and observing deviations in the resistance from values taken at lower currents.

3.3.2.3. Data reduction algorithm: R_{4D} is derived from the following equation:

$$R_{4D} = \frac{V_D}{I}, \tag{3.3}$$

where $V_D \equiv \langle |V_{12}| \rangle \equiv (|V_{12}(+I)| + |V_{12}(-I)|)/2$ and I is the current. The interfacial resistance is estimated as $R_I \approx R_{4D}$ for $\Gamma > 0.65$. In the case where R_{4D} has not been misalignment corrected, Γ must be calculated with an effective flange width of 2δ. For $\Gamma < 0.65$ the result should be stated as $R_I < R_{4D}$.
With the same restrictions for Γ the interfacial resistivity is estimated from

$$\rho = R_I d^2 \leq R_{4D} d^2. \tag{3.4}$$

Consideration should be given to the error which is introduced in the result by a deviation of the true d from the designed contact width. A visual measurement of d should be attempted.

3.4. 6-TERMINAL L-CONTACT RESISTOR:

3.4.1. *Geometrical Description/Design Principles:* The approach of the 6-Terminal L-Contact Resistor is different from that of the D-Resistor by simplifying the geometry to an analytically tractable form at the expense of a somewhat larger flange effect. However, the 6-Terminal L-Contact Resistor is restricted to metal/semiconductor contacts. The structure is shown in Figure 3.4. As the resistance in the metal layer is small compared to that in the semiconductor layer, $R_{S2} \ll R_{S1}$, voltage drops in the metal near the contact can be neglected. Consequently, only one voltage tap and one current tap is provided in the metal layer and the exact metal geometry is not critical although minimum rules are recommended. In the semiconductor layer the width of the voltage or current probing taps has been enlarged to $W_1 = d + \delta_1$, giving the taps the shape of straight legs, which we label L. Furthermore, there are now four taps in the semiconductor layer, which allow current injection from opposite sides. The effect of misalignment of the contact window with respect to the semiconductor layer, shown in the figure, can thus be eliminated to first order. The design should of course be made with $\delta_{11} = \delta_{12} = \delta_{13} = \delta_{14} = \delta_1$. Although the effect of the flange on the measured contact resistance will be removed analytically, the effect should be minimized by design in the first place. As for the L-Contact Resistor holds a relation similar to that of Eq. 3.1 (with γ=2.0), the flange effect is minimized by designing d and δ_1 to their minimum rules. Table 3.3 summarizes the critical design parameters for the 6-Terminal L-Contact Resistor. Again, for the establishment of an area independent ρ, a second contact resistor with d equaling twice the minimum rule is recommended.

3.4.2. *Test Procedure:*

3.4.2.1. Circuit diagrams: See Figs. 3.5 and 3.6.

3.4.2.2. Test conditions: First a current I_{16} of magnitude I is applied between terminals 1 and 6 in both directions, and the average magnitude of the voltages

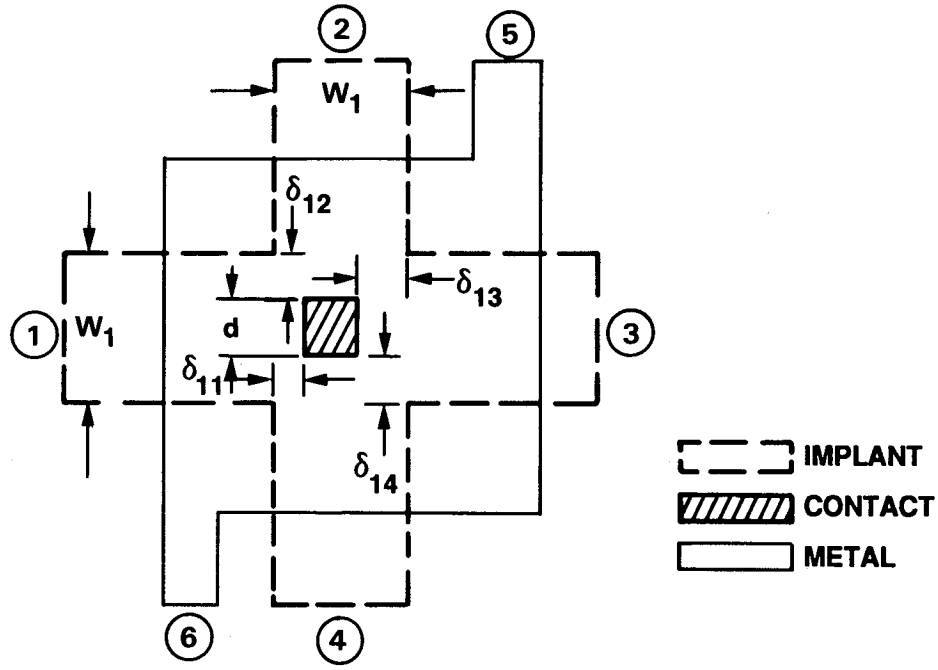

Figure 3.4: Structure of metal-semiconductor 6-Terminal L-Contact Resistor. Contact shown misaligned although designed with $\delta_{1j} = \delta_1$, $j = 1, ..., 4$. Size of metal flange exaggerated for clarity of drawing.

Table 3.3: Critical design parameters for 6-Terminal L-Contact Resistor

Parameter	Parameter Name	Value
d	Contact length = contact width	minimum design rule [,x2]
δ_1	Flange width in layer 1	minimum design rules
W_1	Tap width in layer 1	$d + 2\delta_1$

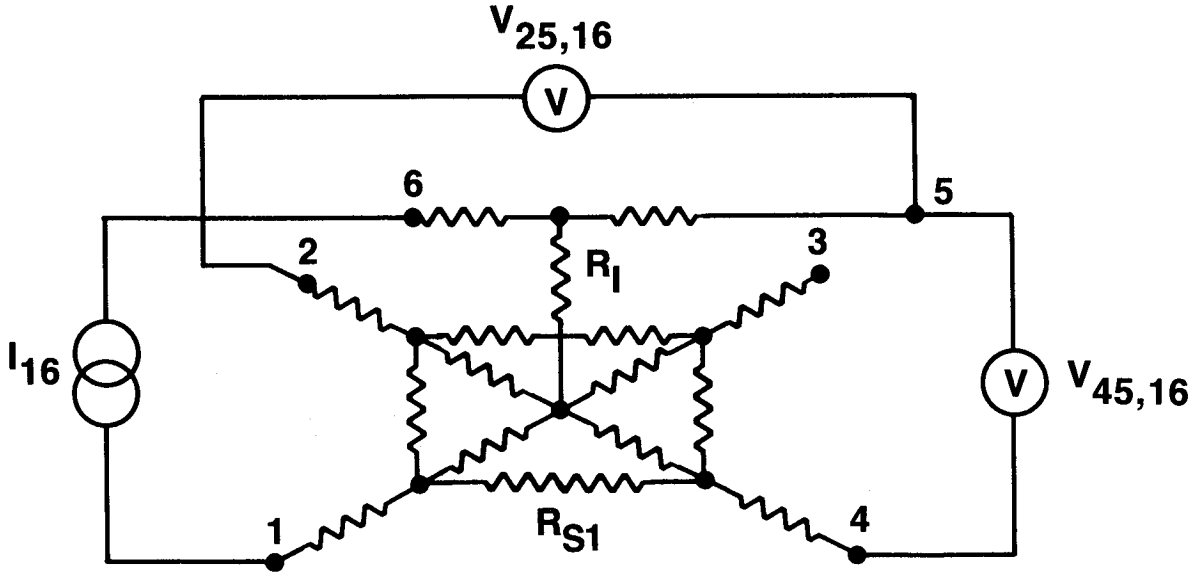

Figure 3.5: Measurement of 6-terminal L-contact resistance, R_{6L}, configuration No. 1. Semiconductor flange represented by 8-resistor network. Voltages $V_{25,16}$ and $V_{45,16}$ can be measured sequentially with one voltmeter.

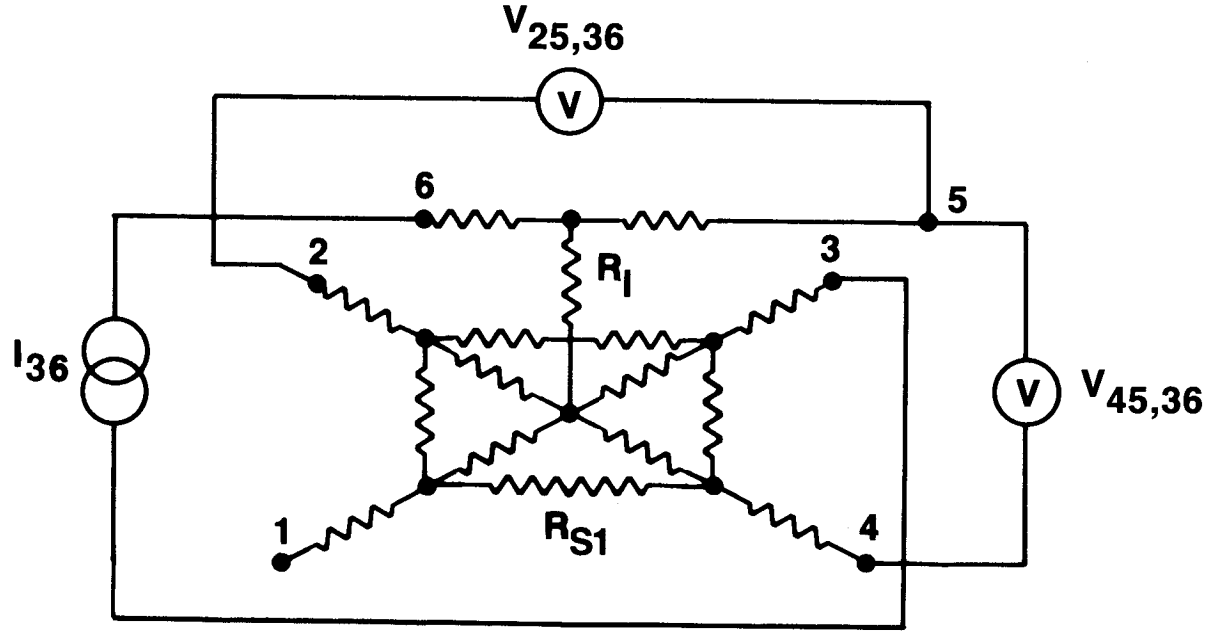

Figure 3.6: Measurement of 6-terminal L-contact resistance, R_{6L}, configuration No. 2

between terminals 2 and 5 as well as 4 and 5, $\langle|V_{25,16}|\rangle$ and $\langle|V_{45,16}|\rangle$, respectively recorded, cf. Fig. 3.5 and test procedure for the 4-terminal D-Resistor. Then the current $I_{36} = \pm I$ is applied between terminals 3 and 6, resulting in the voltages $\langle|V_{25,36}|\rangle$ and $\langle|V_{45,36}|\rangle$, cf. Fig. 3.6.

3.4.2.3. Data reduction algorithms: First the misalignment effect on the contact resistance is eliminated by calculating the average

$$R_{6L} = \frac{\langle|V_{25,16}|\rangle + \langle|V_{45,16}|\rangle + \langle|V_{25,36}|\rangle + \langle|V_{45,36}|\rangle}{4I}. \tag{3.5}$$

This is to first order the contact resistance which would be measured if the contact had a symmetrical flange of $\delta_1 = (\delta_{11} + \delta_{12} + \delta_{13} + \delta_{14})/4$.

In the next step, the parasitic effect of the symmetrized flange is removed from R_{6L} with the help of the Thin-Film Model (TFM). The TFM assumes a functional dependence as $R_{6L}(\rho, d, R_{S1}, \delta_1)$. This function is (iteratively) inverted to calculate ρ or $R_I = \rho/d^2$ as described in the appendix of this chapter.

3.5. TEST RESULTS: Results for some contacts are listed in Table 3.4. The *auxiliary parameters* R_{S1} and R_{S2} stem from Split-Cross Bridge Resistor (SXB) measurements. For d and δ the design values were used. The uncertainty in these dimensions introduces a relatively large potential error in the extracted interfacial parameters. A *probably* improved estimate of δ may be obtained by $\delta_e = \delta - \Delta W/2$, where $\Delta W = W - W_e$ is taken from a SXB measurement of the layer under consideration. The table lists results from 4-Terminal D-Contact Resistors and 6-Terminal L-Contact Resistors. The results in the table represent averages over several chips for which random misalignments were assumed. Of the two D-Contact Resistors only the one making contact to N-diffusion has a $\Gamma > 0.65$, i.e., large enough for sufficiently error free results. In the case of the contact to N-poly, the D-Contact Resistor allows only upper limits of the interfacial parameters to be extracted. The results from the 6-Terminal L-Contact Resistor, although from a smaller contact and from a different run, show an interfacial resistivity of the N-poly contact far below the upper limit extracted from the 4-Terminal D-Contact Resistor. It is highly recommended to calculate how uncertainties in the dimensions propagate into the results. For the case of the 6-Terminal L-Contact Resistor in the table, an error in δ of 0.2 μm results in an error of about 22% in the interfacial parameters. An error in d affects obviously ρ much more directly than R_I.

Table 3.4: Results from Contact Resistors

Run M-	Contact	d [μm]	δ [μm]	R_{4D} [Ω]	R_{6L} [Ω]	R_{S1} [$\Omega/\Box$]	R_{S2} [$\Omega/\Box$]	Γ	R_I [Ω]	ρ [$\Omega\mu m^2$]
770	MND	3.0	1.5	6.1		15.5	35m	0.90	≈ 6.1	≈ 55
770	MNP	3.0	1.5	2.5		15.5	35m	0.37	<2.5	<23
95F	MNP	1.6	0.8		4.9	24.1	50m	0.47	2.3	5.8
Contacts: MND = metal/N-poly, MND = metal/N-diffusion										

3.6. APPENDIX: The Thin-Film-Model (TFM):

The approach of the TFM is to replace the original contact area with: a) an equipotential core of dimension smaller than the contact and embedded in the semiconductor layer, with the semiconductor layer being treated as a two dimensional sheet; and b) a lumped resistor with a value equal to the interfacial contact resistance connected to the equipotential core region. After some simplifying assumptions, the potential in the two dimensional sheet is solved by conformal transformations. The upper layer is treated as an equipotential plane. The model was derived in [3.4] for a 4-Terminal L-Contact Resistor; but the derivation shows that it is valid for the 6-Terminal L-Contact Resistor without modification.

In the TFM, the measured contact resistance, R_{6L}, is the sum of two parts, the intrinsic contact resistance, R_I, and the parasitic resistance, R_{f1}, due to the flange in the semiconducting layer. Thus:

$$R_{6L} = R_I + R_{f1}, \tag{3.6}$$

where

$$R_I = \frac{\rho}{d^2} \tag{3.7}$$

and

$$R_{f1} = \frac{R_{S1}}{\pi} \text{arcosh}\left(\frac{1-t}{a}\right) \times \frac{\delta_1 + \lambda_s}{W_1}, \tag{3.8}$$

with λ_s given below. The parameters t and a are determined from

$$q = \text{arcosh}\left(\frac{b-2x}{b}\right) + \sqrt{b-1}\,\arccos\left(\frac{bx+b-2x}{b(1-x)}\right), \tag{3.9}$$

where

$$b = \frac{W_1}{\delta_1 + \lambda_s} + 1, \tag{3.10}$$

$$\lambda_s = \frac{\lambda \delta_1}{W_1 - \lambda}, \tag{3.11}$$

$$\lambda_f = \lambda - 2\lambda_s, \tag{3.12}$$

$$\lambda = L_T \left[\coth\left(\frac{d}{L_T}\right) - \frac{L_T}{d} \right], \tag{3.13}$$

and L_T is the transmission length given by

$$L_T = \sqrt{\rho / R_{S1}}, \tag{3.14}$$

by requiring:

$$q(x = t - a) = \frac{W_1 - \delta_1 - \lambda_f}{\pi(\delta_1 + \lambda_s)} \tag{3.15}$$

and

$$q(x = t + a) = \frac{\delta_1}{\pi(\delta_1 + \lambda_s)}. \tag{3.16}$$

The inversion of Eq. 3.9 for a given $q = q_0$ can be achieved iteratively by starting with $x_{old} = -1$ and calculating successive improved values

$$x_{new} = x_{old} \frac{q_0}{q(x_{old})}. \tag{3.17}$$

The procedure is terminated when $q(x_{new})$ approximates q_0 within 1%. The resulting values for t and a are then substituted into Eq. 3.8 to determine R_{f1}.

Combining Eqs. 3.6 and 3.7:

$$R_{6L} = \frac{\rho}{d^2} + R_{f1}. \tag{3.18}$$

As R_{f1} is a function of ρ, Eq. 3.18 must be solved iteratively for ρ. For a measured $R_{6L} = R_0$, use of the false position rule is recommended with initial values $\rho_{lo} = \epsilon$, where ϵ is less than the minimum expected ρ, and $\rho_{hi} = R_0 \times d^2$ and with updates

$$\rho_{new} = \rho_{lo} + \frac{\rho_{hi} - \rho_{lo}}{R_{6L}(\rho_{hi}) - R_{6L}(\rho_{lo})} [R_{c0} - R_{6L}(\rho_{lo})]. \tag{3.19}$$

If $R_{6L}(\rho_{new}) < R_0$, then set $\rho_{lo} = \rho_{new}$ else $\rho_{hi} = \rho_{new}$. This procedure is repeated until $|R_{6L}(\rho_{new}) - R_0| < \eta$, where η is of the order of the measurement error of the contact resistance.

3.7. REFERENCES AND FURTHER READING:

3.1. M. Finetti, A. Scorzoni, and G. Soncini, "Lateral Current Crowding Effects on Contact Resistance Measurements in Four Terminal Resistor Patterns," *IEEE Electron Dev. Lett.*, **EDL-5, 524** (1984)

3.2. W. J. C. Alexander and A. J. Walton, "Sources of Error in Extracting the Specific Contact Resistance from Kelvin Device Measurements," *Proc. IEEE 1988 Int. Conf. Microelectronic Test Structures*, **1**, 17 (1988)

3.3. A. Scorzoni and M. Finetti, "Metal/Semiconductor Contact Resistivity and its Determination from Contact Resistance Measurements," *Material Science Reports*, **3(2)** 79, (1988)

3.4. U. Lieneweg and D. J. Hannaman, "New Flange Correction Formula Applied to Interfacial Resistance Measurements of Ohmic Contacts to GaAs," *IEEE Electron Dev. Lett.*, **EDL-8**, 202 (1987)

3.5. U. Lieneweg and D. J. Hannaman,"Flange Correction to Four-Terminal Contact Resistance Measurements," *Proc. IEEE 1990 Int. Conf. Microelectronic Test Structures*, **3**, 27 (1990)

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Chapter 4

MOSFET Capacitor

4.1. TEST MODULE: The MOSFET Capacitor is a 4-terminal structure connected to a 2 x 2 pad array. As the Capacitor does not fit between the pads, a total area equivalent to a 2 x 3 standard pad array is required, cf. Fig. 1.1.

4.2. PURPOSE: To extract the gate-oxide capacitance per unit area, C'_{ox}, and the overlap capacitance between gate and source and drain per unit length, C'_{go} of MOS transistors. Further data reduction gives the gate-oxide thickness, T_{ox}. The two-sided reduction in gate length due to processing, ΔL, can be extracted from two Capacitors with different gate lengths. The list of extracted MOSFET Capacitor parameters is given in Table 4.1. The structure can also be used for extraction of DC MOS transistor parameters.

Table 4.1: Extracted MOSFET Capacitor Parameters.

Parameter	Parameter Name
C'_{ox}	Gate-oxide capacitance/unit area
C'_{go}	Gate-to-source and drain overlap capacitance/unit length
T_{ox}	Gate-oxide thickness
ΔL	Reduction in gate length

4.3. GEOMETRICAL DESCRIPTION/DESIGN PRINCIPLES: The MOSFET Capacitor, shown in Figure 4.1, is an MOS transistor with a gate in the shape of a large ring. The inner and outer radii of that ring are designed as $R - L/2$ and

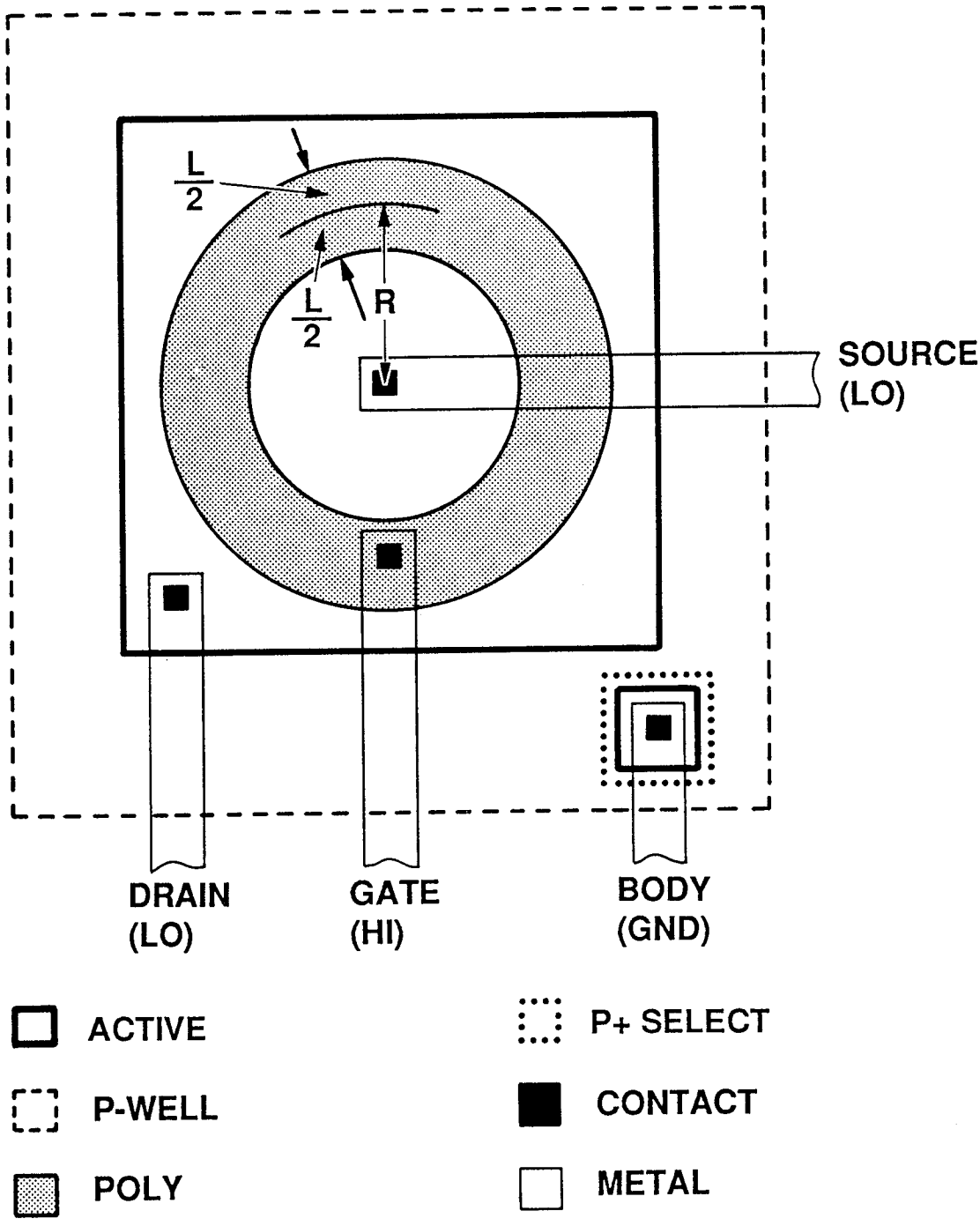

Figure 4.1: MOSFET Capacitor (closed geometry transistor)

$R + L/2$, respectively, where L is the design length of the gate. Metal connectors run from source, gate, drain, and body to the four terminal pads. In order to reduce parasitic series resistances, the single contacts to source and drain shown for simplicity in the figure should in reality be replaced by multiple minimum geometry contacts placed around the periphery of the gate in the source and drain regions. The total gate area of the MOSFET should be sufficiently large to provide at least 1.0 pF total gate-oxide capacitance. The critical design parameters are the radius of the gate, R, and the gate length, L. The MOSFET Capacitors shown in Figure 1.1 for the 3-μm CMOS process have the critical dimensions of $R = 54$ μm and $L = 6$ or 24 μm. The critical design parameters for MOSFET Capacitor are shown in Table 4.2

Table 4.2: Critical design parameters for MOSFET Capacitor

Parameter	Parameter Name	Recommended Value
R	Gate radius	$\approx 40\ \lambda$
$L(1)$, $L(2)$	Gate lengths	$\approx 5, 15\ \lambda$

4.4. TEST PROCEDURE:

4.4.1. Circuit diagram: In Figure 4.2 the MOSFET Capacitor is modeled by a network of capacitors, part of which are switched on and off according to different bias conditions, as explained below. The source and drain terminals are connected externally and treated from now on as one terminal, labeled SOURCE/DRAIN. The capacitances of interest are the gate-oxide capacitance, C_{ox}, and the gate-overlap capacitance, C_{go}. The body capacitance, C_b, the source/drain diode capacitance, C_d, the probe pad capacitance, C_{gb}, and the offset capacitance, C_{off}, are parasitic capacitances. A DC voltage source, V_{GDS}, and an AC voltage source, v_s, are connected in series to the GATE terminal; an AC ammeter, i_m, is connected to the SOURCE/DRAIN terminal; and an AC voltmeter, v_{sm}, is connected between the GATE and SOURCE/DRAIN terminals.

4.4.2. Test conditions: In the test set-up shown in Figure 4.2 it is assumed that the impedance of the AC voltmeter is high enough so that its measurement current may be neglected. In addition, the impedance of the AC ammeter is assumed to be very low so that the SOURCE/DRAIN terminal is a virtual ground. This means that the current through C_d may be neglected. By grounding the BODY and measuring the AC signal voltage, v_{sm}, the effects of C_b, C_d, and C_{gb} can be

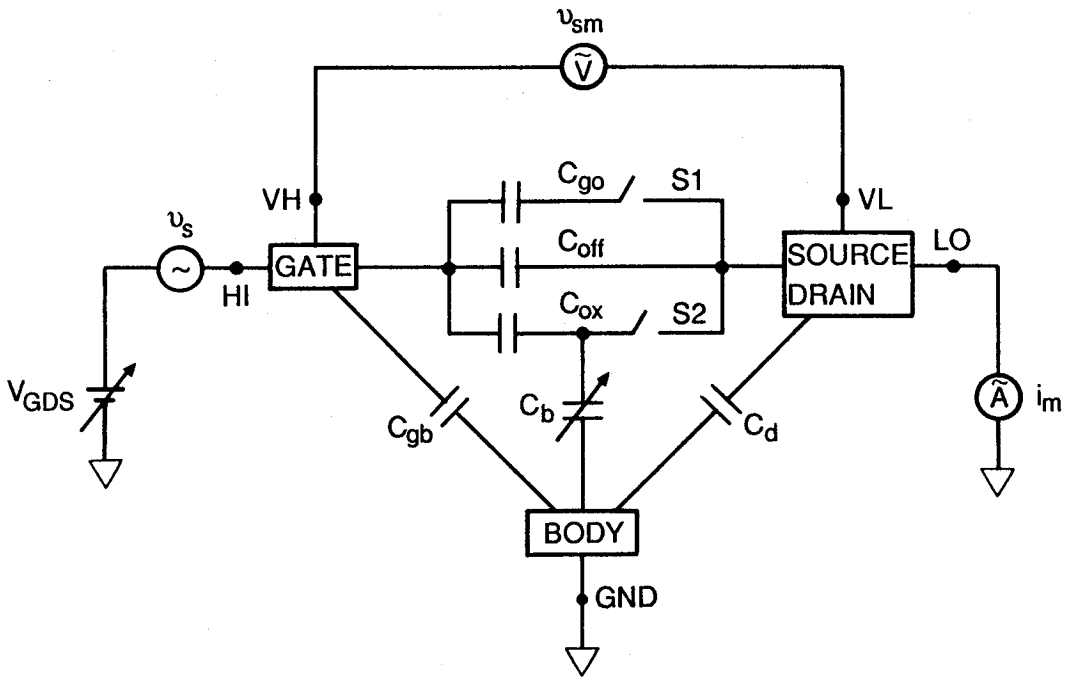

Figure 4.2: Measurement of the gate-oxide and gate-overlap capacitances using a MOSFET. When the body is inverted ($V_{GDS} = 5$ V) switches S1 and S2 are closed. When the body is depleted ($V_{GDS} = 0$), only switch S1 is closed. When the body is accumulated ($V_{GDS} = -5$ V), both switches are open.

neglected. The remaining parasitic capacitance, C_{off}, is independent of the device operating conditions and is measured as described below.

"Measured" capacitances are derived from

$$C_{meas} = i_m / 2\pi f_s v_{sm}, \tag{4.1}$$

where f_s is the frequency of the AC source. A typical value for the AC source voltage is v_s = 100 mV(rms) with a frequency between 100 kHz and 1.0 MHz. Commercial capacitance meters can be found which are based on the same principle and provide the necessary circuitry ending in terminals usually labeled HI and LO, cf. Fig. 4.2.

The capacitance between the gate and the source/drain is measured as a function of the DC bias gate voltage, V_{GDS}. In the three-point method described below one measures the capacitance at three values of V_{GDS}. The first capacitance, C_1, is measured at $V_{GDS} = +V_{DD}$, the second, C_2, at $V_{GDS} = 0$, and the third, C_3, at $V_{GDS} = -V_{DD}$, where, usually, V_{DD} = 5 V. Test input/output parameters for the MOSFET Capacitor are listed in Table 4.3.

Table 4.3: Test input/output parameters for MOSFET Capacitor

Input parameter	Value	Output parameter
f_s	$\in$ [0.1, 1] MHz	
v_s	$\in$ [10, 100] mV(rms)	i_m or C_{meas}
V_{GDS}	$+V_{DD}$, $\approx$0, $-V_{DD}$	C_1, C_2, C_3

4.4.3. Data reduction algorithm: The data reduction algorithms are based on the operating characteristics of the MOSFET as shown in Figure 4.3. Here, an n-MOSFET is shown operating in strong inversion, depletion, and strong accumulation.

The dependence of the measured capacitance on the gate bias is shown in Figure 4.4. Also indicated are the three key data points C_1, C_2, and C_3, which are used to extract the desired capacitances. Care must be taken that C_2 is measured for the MOSFET biased in the depletion mode. It is suggested that a capacitance versus voltage curve be plotted to verify the (weak) depletion at $V_{GDS} = 0$. (The bias voltage for C_2 should be 0.5 to 1.0 V below the onset of inversion, i.e., the threshold voltage.)

When the MOSFET is in strong inversion, the oxide capacitance, C_{ox}, is con-

nected to the source and drain terminals through the channel formed under the gate as seen in Figure 4.3a; thus, the measured capacitance is

$$C_1 \equiv C_{meas}(V_{GDS} = +V_{DD}) = C_{off} + C_{go} + C_{ox}. \tag{4.2}$$

When the MOSFET surface is depleted, the oxide capacitance is no longer connected to the gate but is connected instead to the ground through C_b as seen in Figure 4.3b; thus

$$C_2 \equiv C_{meas}(V_{GDS} = 0) = C_{off} + C_{go}. \tag{4.3}$$

Finally, when the MOSFET is strongly accumulated, the overlap capacitance is decoupled from the measurement terminals by depletion/inversion of the source/drain pn junctions as shown in Figure 4.3c, giving

$$C_3 \equiv C_{meas}(V_{GDS} = -V_{DD}) = C_{off}. \tag{4.4}$$

Then C_{ox} and C_{go} are given simply by:

$$C_{ox} = C_1 - C_2 \tag{4.5}$$

and

$$C_{go} = C_2 - C_3. \tag{4.6}$$

The gate-oxide capacitance/unit area is defined by $C'_{ox} = C_{ox}/\text{gate-area}$. For the annular geometry shown in Figure 4.1, the gate area is $\pi(R + L_e/2)^2 - \pi(R - L_e/2)^2 = 2\pi RL_e$, where L_e is the effective gate length and R is the designed mean radius of the gate; thus

$$C'_{ox} = \frac{C_{ox}}{2\pi RL_e}. \tag{4.7}$$

The effective gate length is $L_e = L - \Delta L$, where L is the as-drawn dimension and ΔL is the two-sided reduction in the gate length due to processing. ΔL can be determined by using two devices with the same radius but different L ($L(1)$ and $L(2)$), assuming ΔL and C'_{ox} are the same for both devices. Then from Eq. 4.6

$$\Delta L = \frac{L(1)C_{ox}(2) - L(2)C_{ox}(2)}{C_{ox}(2) - C_{ox}(1)}, \tag{4.8}$$

where $C_{ox}(1)$ and $C_{ox}(2)$ are the measured oxide capacitances of the first and second device, respectively. As a second choice, the Split-Cross-Bridge Resistor (see that chapter) can be used to determine ΔL; however, somewhat different results are expected when the cross section of the gate conductor is not rectangular. As

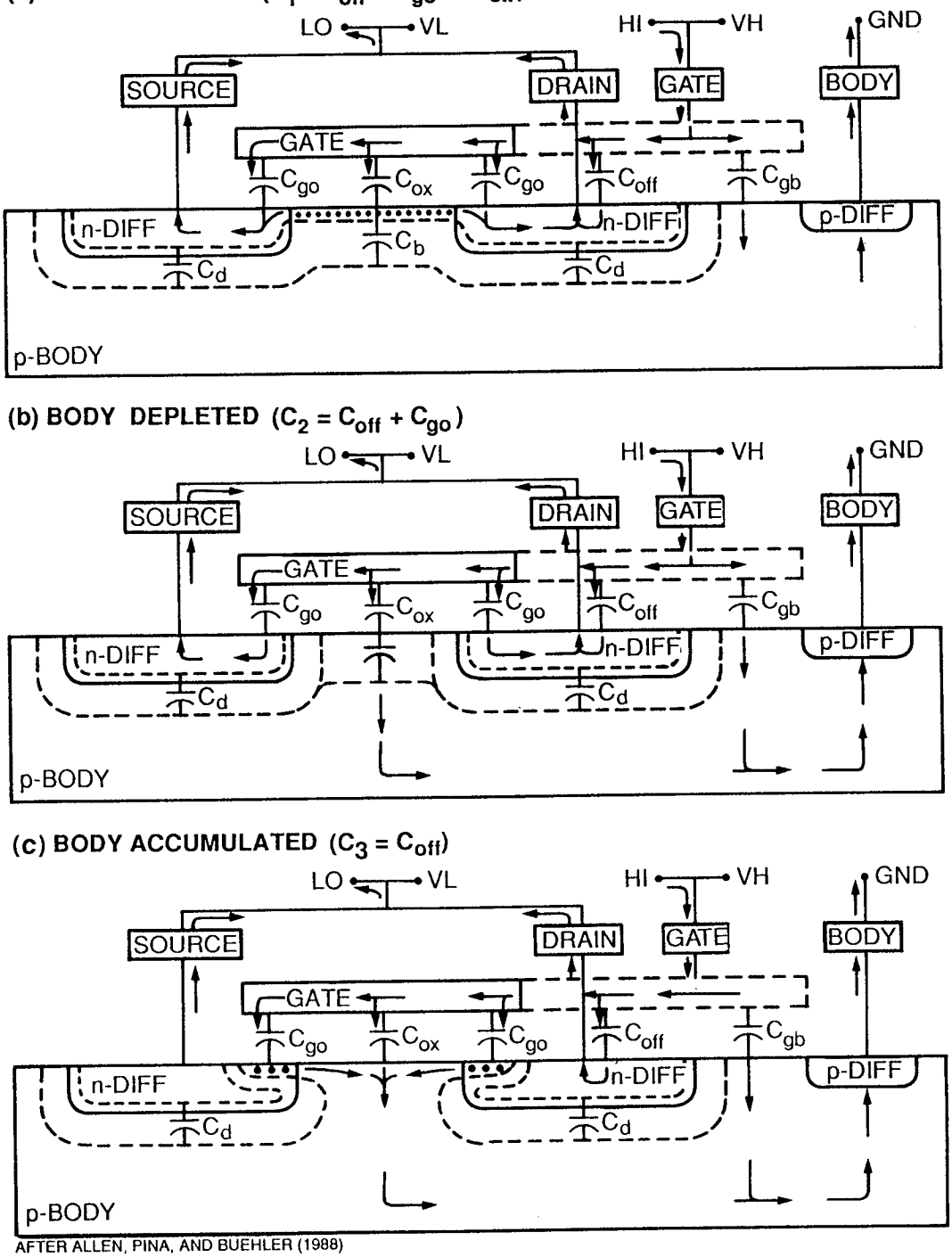

Figure 4.3: n-MOSFET cross section depicting the three regions of MOSFET operation used to extract the gate-oxide and gate-overlap capacitances.

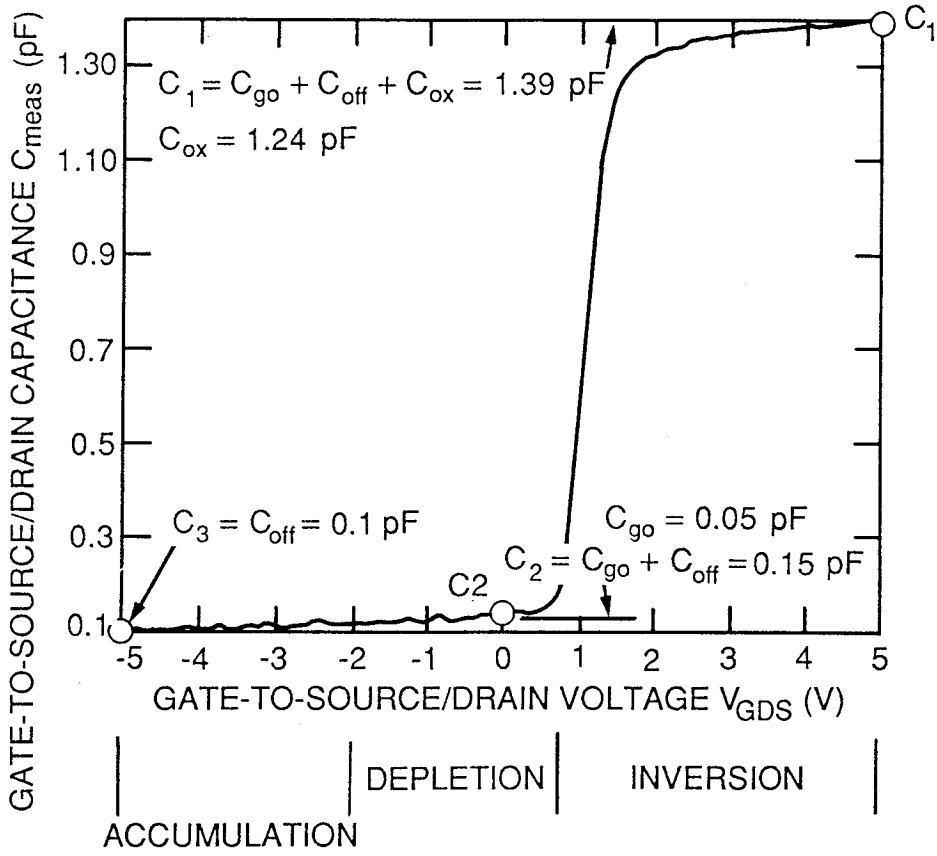

Figure 4.4: Three-point method for measuring the gate-oxide and gate-overlap capacitances from an n-MOSFET, where the threshold voltage is approximately 0.8 V.

Table 4.4: MOSFET Capacitor results

Parameter	Units	3μm CMOS p-well	1.6μm CMOS n-well
C'_{ox}	fF/μm^2	0.73	1.317
C'_{go}	fF/μm	0.074	0.090
T_{ox}	nm	47.0	26.2
R	μm	54	36
L	μm	6, 24	4, 8
ΔL	μm	1	0.44
Channel	type	n	n

a last choice, $\Delta L = 0$ is assumed.

The gate-overlap capacitance/unit length is given by $C'_{go} = C_{go}$/gate-perimeter, where the gate-perimeter is $2\pi(R + L_e/2) + 2\pi(R - L_e/2) = 4\pi R$, thus:

$$C'_{go} = \frac{C_{go}}{4\pi R}. \tag{4.9}$$

Notice that C'_{go} does not depend on ΔL.
The gate oxide thickness, T_{ox}, is calculated from $C'_{ox} = \epsilon_o/T_{ox}$, giving:

$$T_{ox} = \frac{\epsilon_o}{C'_{ox}} \tag{4.10}$$

where $\epsilon_o = \epsilon(SiO_2) = 34.515 \times 10^{-6}$pF/$\mu$m.

4.5. TEST RESULTS: Typical results for MOSFET Capacitors fabricated by a 3-μm CMOS p-well and a 1.6-μm CMOS n-well process are given in Table 4.4, where the 3-μm CMOS p-well results follow from the data shown in Figure 4.4. The above n-MOSFET discussion can be extended to a p-MOSFET by simply changing the sign of V_{GDS}.

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Chapter 5

Field-Oxide Transistor

5.1. TEST MODULE: The Field-Oxide Transistor is a 4-terminal structure fitting completely within a 2 x 2 pad array.

5.2. PURPOSE: To assure that the surface between MOSFETs is electrically isolated, i.e., that, under normal conditions, no inversion channels are formed under field oxide subjected to fields from crossing poly or metal lines. Onset of surface conduction is characterized by the field-oxide threshold voltage, V_{Tfield}. The Field-Oxide Transistor method is applied to regions with n-type and regions with p-type doping under the field oxide. The absolute value of V_{Tfield} should be larger than the supply voltage, i.e., usually 5 V, by a safe margin.

5.3. GEOMETRICAL DESCRIPTION/DESIGN PRINCIPLES: The layout is shown in Figure 5.1. The channel length, L, should be minimum feature size. However, the channel width, W, should be much greater than minimum feature size, say $W = 5L$. The gate metal is designed to overlap the active region by a distance L_{go} to allow for misalignment and overetching effects. A recommended value for L_{go} is the poly-gate overlap design rule, denoted O:PAn in Table B2 (Appendix). Note that this overlap region becomes N^+-doped when the gate is metal. In the case of a poly gate, the overlap regions have the channel doping, but will normally be inverted long before the surface under the field oxide inverts. This is because the gate oxide is much thinner than the field oxide. Design parameters for an n-channel Field-Oxide Transistor in 3-μm CMOS p-well technology are listed with test parameters and a typical result in Table 5.1.

5.4. TEST PROCEDURE:

5.4.1. Circuit diagram: The circuit diagram shown in Figure 5.2 indicates that the test set-up requires a current source for I_{DS} and a voltmeter for the measurement

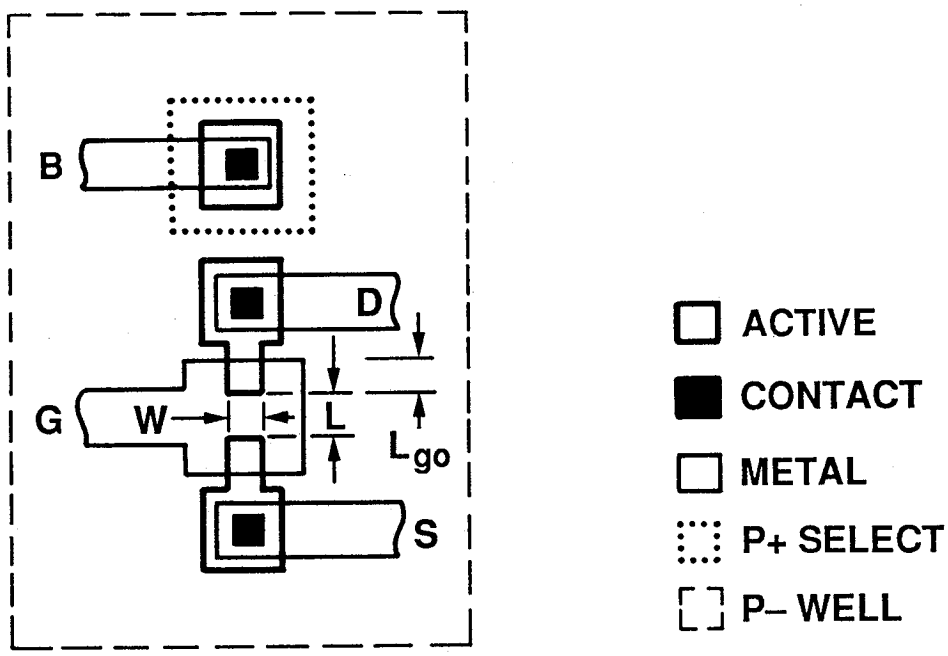

Figure 5.1: . Layout of a four-terminal, metal-gate, n-channel Field-Oxide Transistor.

Table 5.1: Field-Oxide MOSFET Parameters.

Extracted Parameter:		
Parameter	Name	
V_{Tfield}	Field-oxide threshold voltage	
Critical Design Parameters:		
Parameter	Name	Value
L	Channel length	Minimum feature
W	Channel width	$5L$
L_{go}	Gate overlap	Design rule O:PAn
Test Input/Output Parameters:		
Input Parameter	Value	Output Parameter
V_{BS}	0	
V_{DG}	0	
I_{DS}	1 μA	V_{GS}
Result:		
Parameter	Type or Value	
Gate material	Metal	
Channel	n-type	
V_{Tfield}	15 V	

of V_{Tfield}. The bulk terminal is externally connected to the source terminal and the gate terminal to the drain terminal.

5.4.2. Test conditions: For simplicity, we define the field-oxide threshold voltage, V_{Tfield}, as the gate voltage at which a current $I_{DS} = 1$ μA flows through the channel of a Field-Oxide Transistor with $W/L = 5$. Actually, V_{Tfield} is measured with the current source set to $I_{DS} = 1$ μA while $V_{BS} = 0$ and $V_{GS} = V_{DS}$. The last condition ensures that the Transistor is operating in the saturation region. It may happen that the gate oxide breaks down before the surface under the field oxide becomes inverted. In such a case, the measured voltage represents a lower bound for V_{Tfield}. If a distinction is needed, the current flowing into the gate should be monitored.

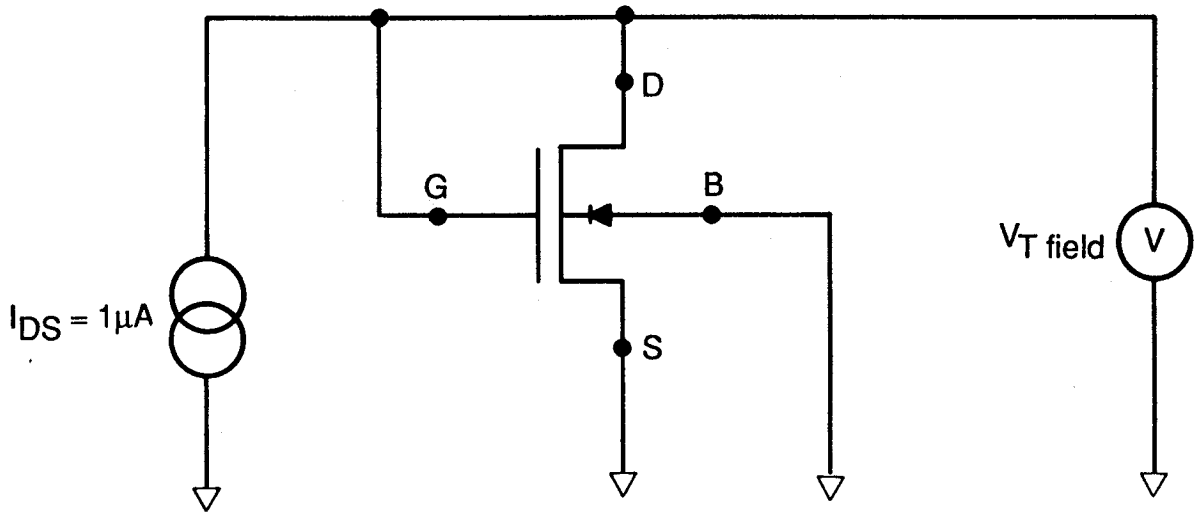

Figure 5.2: Field-oxide threshold voltage, $V_{T\,field}$, measurement circuit.

Chapter 6

MOSFET Gross Parameters

6.1. TEST MODULE: The MOSFET Gross Parameters module uses a four-terminal enhancement-mode MOSFET fitting completely within a 2 x 2 pad array. The test can be applied to any of the four transistors of the MOSFET Quartet described in the next chapter.

6.2. PURPOSE: To evaluate the gross parameters of the MOSFET which are listed in Table 6.1.

Table 6.1: MOSFET Gross Parameters

Parameter	Parameter Name
I_{DSoff}	Source-drain leakage current
I_{DBleak}	Source and drain diode leakage current
I_{GBleak}	Gate leakage current
I_{DSon}	Source-drain on current
V_{DBbd}	Source and drain diode breakdown voltage
V_{DBGbd}	Source and drain isolation voltage

6.3. GEOMETRICAL DESCRIPTION/DESIGN PRINCIPLES: The layout of a four-terminal n-MOSFET in a p-well is shown in Figure 6.1. The MOSFET elements are labeled as follows: S for source, D for drain, G for gate, and B for body. The source and drain series resistances are designed to have a minimum value by minimizing the distance between the contacts and the gate.

6.4. TEST PROCEDURE: All tests are described for n-MOSFETs. Measurements of p-MOSFETs are performed by reversing the voltages applied to the

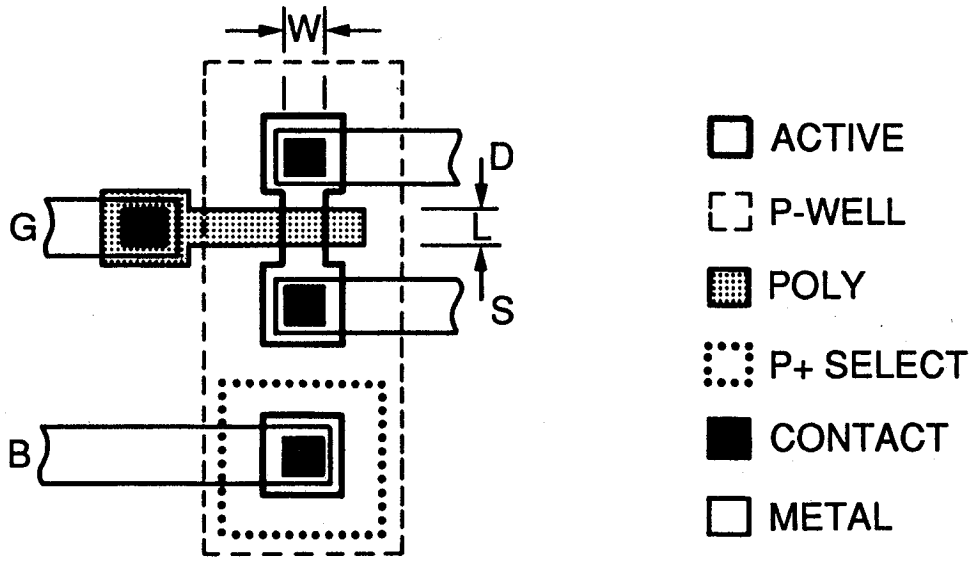

Figure 6.1: Layout of four-terminal n-MOSFET in p-well

devices and measuring the magnitude of the current.

6.4.1. Source-drain leakage current, I_{DSoff}:

Circuit diagram: See Figure 6.2.

Test conditions: I_{DSoff} is the current that flows in the reverse direction through the drain diode with the gate biased so that the channel is turned off. I_{DSoff} is measured with the body connected to the source, the gate connected to the ground, and $V_{DS} = 5$ V.

6.4.2. Source and drain diode leakage current, I_{DBleak}:

Circuit diagram: See Figure 6.3.

Test conditions: I_{DBleak} is the sum of the leakage currents that flow through the reverse-biased source and drain diodes to the body. I_{DBleak} will also include leakage currents that flow through the gate oxide that overlaps the source and drain junctions. I_{DBleak} is measured with the drain connected to the source, the gate connected to the body, and $V_{DB} = +5$ V.

6.4.3. Gate leakage current, I_{GBleak}:

Circuit diagram: See Figure 6.4.

Test conditions: I_{GBleak} is the sum of the currents that flow from the gate to

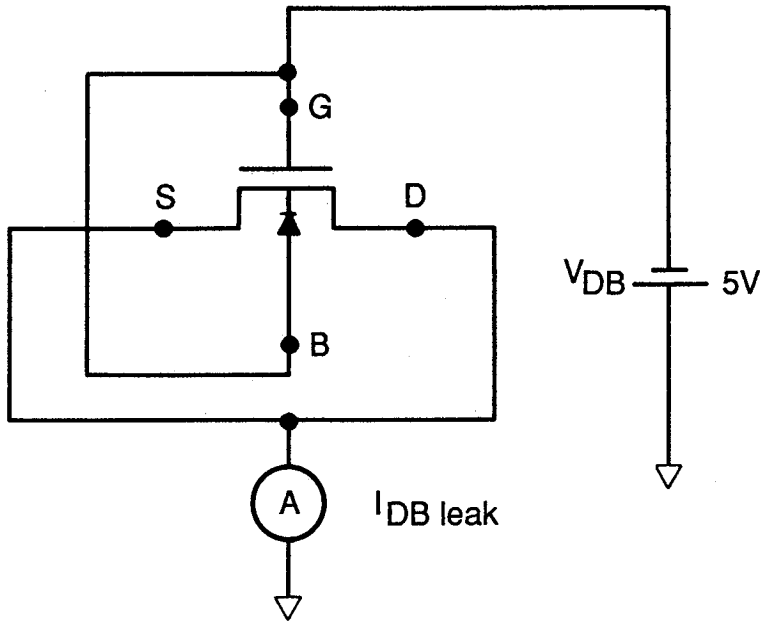

Figure 6.2: MOSFET source-drain leakage current, I_{DSoff}, measurement circuit.

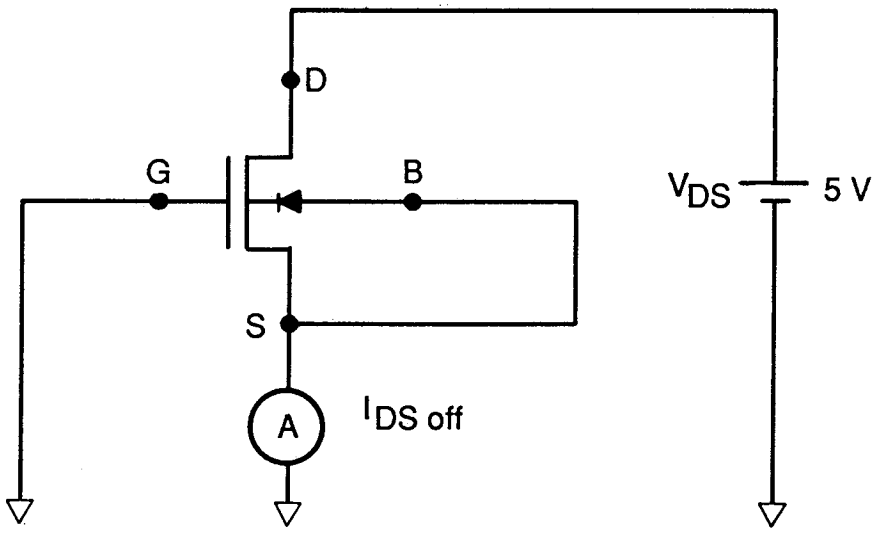

Figure 6.3: Source and drain diode leakage, I_{DBleak}, measurement circuit.

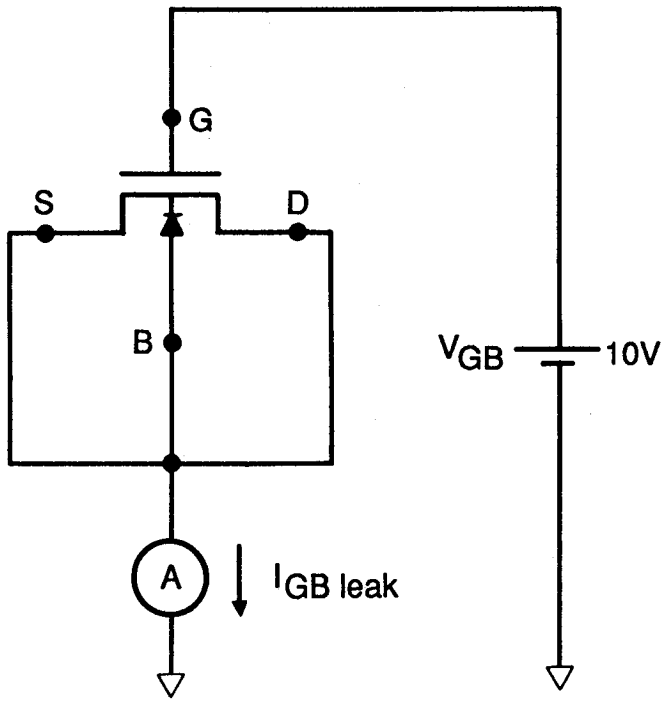

Figure 6.4: Gate leakage current, I_{GBleak}, measurement circuit

the body, source, and drain with the gate biased so the channel is on. I_{GBleak} is measured with the source and the drain connected to the body and $V_{GB} = 10$ V.

6.4.4. Source-drain on current, I_{DSon}.

Circuit diagram: See Figure 6.5.

Test conditions: I_{DSon} is the current which flows between the source and the drain with the channel turned on. I_{DSon} is measured with the gate connected to the drain, the source connected to the body, and $V_{DS} = 5$ V.

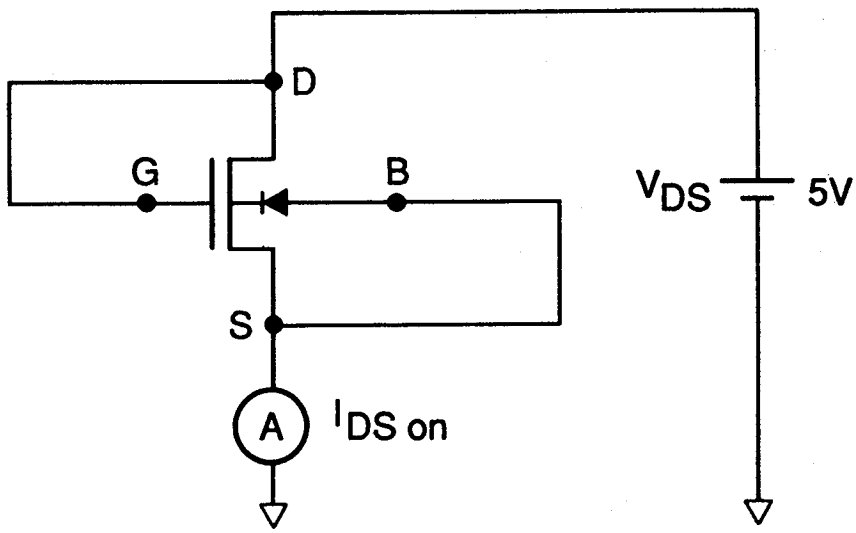

Figure 6.5: Circuit for measuring source-drain on current, I_{DSon}

6.4.5. Source and drain diode breakdown voltage, V_{DBbd}, and source and drain isolation voltage, V_{DBGbd}

Circuit diagram: See Figure 6.6.

Test conditions: V_{DBbd} is the breakdown voltage measured across both the source and drain diodes with 1 microampere forced in the reverse-bias direction through the diodes. V_{DBbd} is measured with the source and the gate connected to the drain and $I_{DB} = 1$ μA.

The source and drain isolation voltage, V_{DBGbd}, is measured the same way except that the gate is also grounded. V_{DBGbd} is somewhat lower than the source and drain diode breakdown voltage because of parallel current flow through the gate oxide induced by the fields at the edges of source and drain. If V_{DBGbd} is

substantially lower than V_{DBbd} a problem with the integrity of the oxide may be suspected. This simple, semiquantitative oxide test is intended to serve as a flag only.

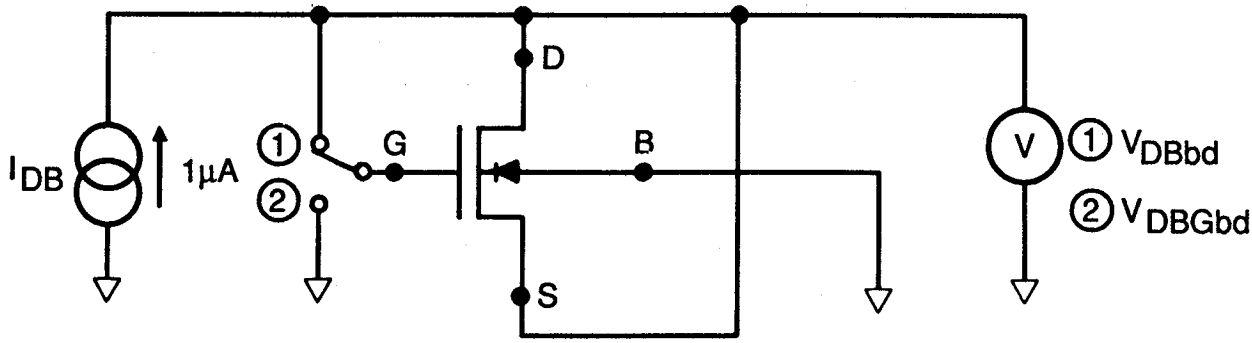

Figure 6.6: Source and drain diode breakdown voltage, V_{DBbd}, and source and drain isolation voltage, V_{DBGbd}, measurement circuit

6.5. TEST RESULTS: Tables 6.2 and 6.3 show results obtained from one chip with sets of four n- and p-MOSFETs with different gate widths, W, and lengths, L, cf. the chapter on MOSFET-Quartet Model Parameters. For ease of orientation, the data are arranged in the tables as they would appear in a W vs. L plane. The transistors were fabricated in 1.6-μm n-well technology. All transistors turn on and off satisfactorily. I_{DSon} is approximately proportional to W/L. The ratio I_{DSoff}/I_{DSon} is less than 10^{-6} for the n-channel and 10^{-7} for the p-channel devices. The leakage and breakdown of the source and drain diodes appear to be normal. The source and drain isolation voltages are 3 to 4 V lower than the diode breakdown voltages but still comfortably large in comparison to the supply voltage.

Table 6.2: Gross Parameters extracted from n-MOSFET Quartet

$W = 7.2\ \mu$m	$L = 1.6\ \mu$m	$L = 4.8\ \mu$m
I_{DSoff}	64 pA	74 pA
I_{DBleak}	5 pA	6 pA
I_{GBleak}	100 pA	192 pA
I_{DSon}	1.70 mA	0.70 mA
V_{DBbd}	19 V	18 V
V_{DBGbd}	16 V	15 V
$W = 2.4\ \mu$m	$L = 1.6\ \mu$m	$L = 4.8\ \mu$m
I_{DSoff}	1129 pA	114 pA
I_{DBleak}	188 pA	31 pA
I_{GBleak}	104 pA	69 pA
I_{DSon}	0.54 mA	0.21 mA
V_{DBbd}	18 V	19 V
V_{DBGbd}	15 V	15 V

Table 6.3: Gross Parameters extracted from p-MOSFET Quartet

$W = 7.2\ \mu$m	$L = 1.6\ \mu$m	$L = 4.8\ \mu$m
I_{DSoff}	14 pA	5 pA
I_{DBleak}	22 pA	20 pA
I_{GBleak}	22 pA	2 pA
I_{DSon}	0.72 mA	0.23 mA
V_{DBbd}	18 V	18 V
V_{DBGbd}	14 V	14 V
$W = 2.4\ \mu$m	$L = 1.6\ \mu$m	$L = 4.8\ \mu$m
I_{DSoff}	933 pA	10 pA
I_{DBleak}	63 pA	40 pA
I_{GBleak}	39 pA	107 pA
I_{DSon}	0.19 mA	0.06 mA
V_{DBbd}	18 V	18 V
V_{DBGbd}	14 V	14 V

Chapter 7

MOSFET Quartet: Model Parameters

7.1. TEST MODULE: The MOSFET Quartet consists of a set of four 4-terminal, enhancement-mode MOSFETs, each having a different gate geometry. For the CMOS process, separate Quartets are required for n-channel and p-channel transistors. Each transistor fits completely within a 2 x 2 pad array.

7.2. PURPOSE: To extract a set of geometry independent parameters which allow description of the behavior of 4-terminal MOSFETs by simple model equations. First, geometry dependent parameters are extracted for each of the four MOSFETs operating in either the subthreshold, linear, or saturation regions. From these "individual" parameters, "global" geometry independent parameters are derived. The approach is designed for easy parameter extraction from a minimal data set.

The MOSFET model used here is most like SPICE MOS3 [7.1] and is similar to CASMOS [7.2] and MOSAID [7.3] models. The MOSFET model equations are brought into a form which is linear in the unknown coefficients containing the model parameters. Fast linear least-squares methods can then be used for the parameter extraction [7.4]. Due to the simplicity of the model, the resulting parameters still depend somewhat on the extraction equation and the placement of points [7.5]. The following procedures are specified to ensure that the same parameter values are extracted independent of the test system or operator. The MOSFET model parameters are listed in Table 7.1.

The MOSFET model pertains to the circuit shown in Fig. 7.1, which shows an "intrinsic" 3-terminal transistor with added source and drain series resistances,

R, and source and drain to body diodes, making up the "extrinsic" 4-terminal transistor. Note that the intrinsic gate and drain voltages, $V_{G'}$ and $V_{D'}$, are referenced to the intrinsic source S', whereas the (extrinsic) gate, drain, and body voltages, V_G, V_D, and V_B are referenced to the (extrinsic) source S. From Fig. 7.1, the relationship between the intrinsic and extrinsic voltages is:

$$V_{G'} = V_G - I_C R \tag{7.1}$$

and

$$V_{D'} = V_D - 2I_C R. \tag{7.2}$$

Note further that the (extrinsic) drain current, I_D, is the sum of the channel current, I_C, which is the intrinsic drain current, and the body current, I_B:

$$I_D = I_C + I_B. \tag{7.3}$$

In the following, equations for the channel current will be given which hold separately in the linear and in the saturation region. In the subthreshold region, the channel current is zero. For the body current, a solution which holds in the subthreshold and in the active region will be used. The separation of the cited regions is governed by the relation of gate and drain voltages relative to the threshold voltage as indicated in Fig. 7.2. The threshold voltage, V_T, is, in turn, a function of the body voltage:

$$V_T = V_{bi} + \gamma\sqrt{2\phi_f - V_B} + V_{Tsn}, \tag{7.4}$$

where

$$V_{bi} = 2\phi_f + V_{FB0} + V_{it} \tag{7.5}$$

has been called built-in voltage, with ϕ_f being the Fermi potential in the body with reference to the intrinsic level; V_{FB0} the flatband voltage due to the workfunction difference between the gate material and the bulk silicon and due to oxide traps; and the flatband voltage shift V_{it} caused by interface traps [7.6]. The Fermi potential depends on the body dopant density, N, like

$$\phi_f = V_t \ln N/N_i, \tag{7.6}$$

where N_i is the intrinsic carrier density of silicon and $V_t = kT/q$ the thermal voltage with k being Boltzmann's constant, T the absolute temperature, and q the electronic charge. Again in Eq. 7.4, γ is the body effect coefficient given by

$$\gamma = \frac{\sqrt{2\epsilon_s q N}}{C'_{ox}}, \tag{7.7}$$

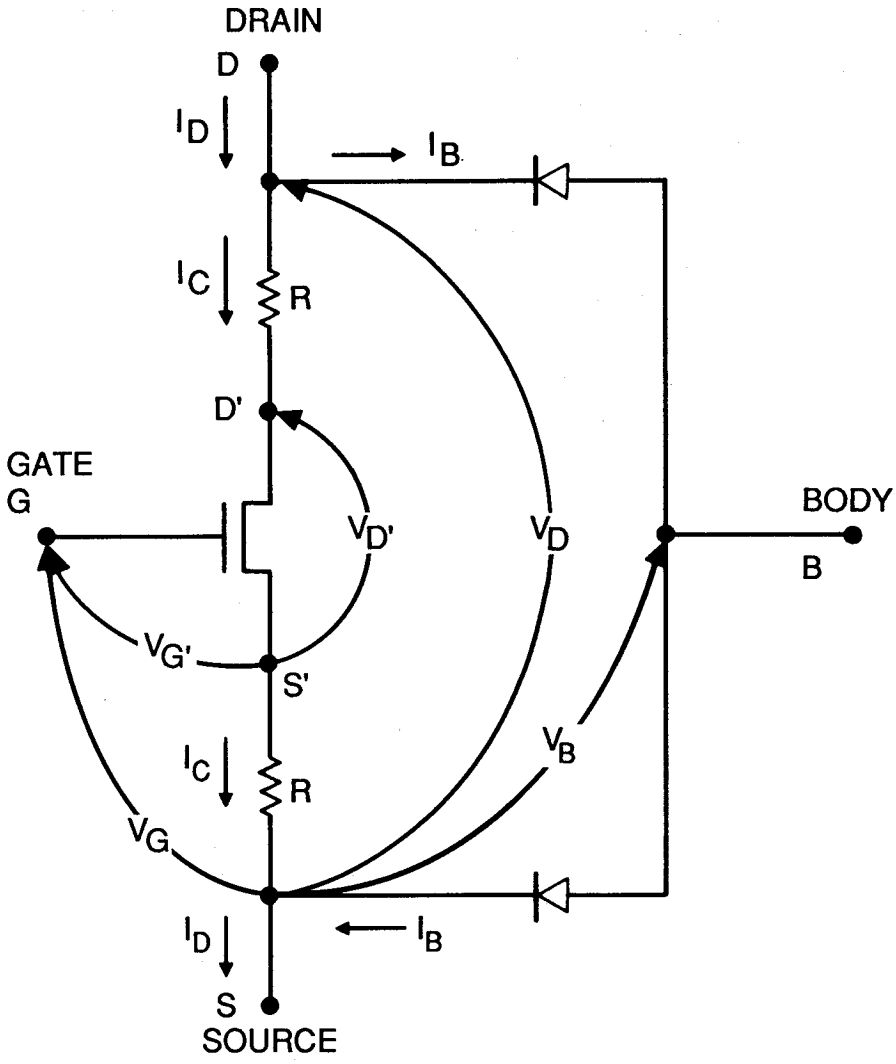

Figure 7.1: Four-terminal n-MOSFET circuit model with source and drain series resistances and source and drain diodes. Intrinsic voltages are denoted with primes and extrinsic (applied) voltages are unprimed.

Table 7.1: MOSFET Model Parameters.

Parameter	Parameter name
ϕ_f	Intrinsic Fermi potential
β	Conduction factor
$K_P = \mu_0 C_{ox}$	Intrinsic conduction factor
ΔW	Decrease in channel width
ΔL	Decrease in channel length
W_e	Effective channel width
L_e	Effective channel length
V_T	Threshold voltage
V_{T0}	Threshold voltage for $V_B = 0$
V_{bi}	Built-in voltage
γ	Body effect coefficient
δ	Secondary body effect coefficient
D_0	Delta coefficient
θ'	Intrinsic gate-field mobility degradation coefficient
$(\theta$	Extrinsic gate-field mobility degradation coefficient)
θ_B	Body-voltage mobility degradation coefficient
R	Series resistance
R_P	Series resistance per unit width
η'	Intrinsic drain-field mobility degradation coefficient
$(\eta$	Extrinsic drain-field mobility degradation coefficient)
ϵ	Carrier velocity saturation coefficient
λ	Channel length modulation coefficient
I_{Bo}	Active region body current
γ_z	Body-current body effect coefficient
M	Subthreshold slope (M-factor)
M_o	Intrinsic M-factor
γ_m	M-factor body effect coefficient
V_{it}	Interface-trap voltage
V_{FB0}	Flatband voltage less interface-trap voltage
ζ'	Intrinsic V_D-dependent fitting factor
$(\zeta$	Extrinsic V_D-dependent fitting factor)
I_{Bcut}	Cutoff current
V_{Bcut}	Cutoff voltage
p_0	Fat FET value of parameter p; $p = \delta, \epsilon, \eta, \theta, \theta_B, \lambda$
K_{WP}	Width coefficient of parameter p; $P = D, E, H, T, TB, L$
K_{LP}	Length coefficient of parameter p; $P = D, E, H, T, TB, L$

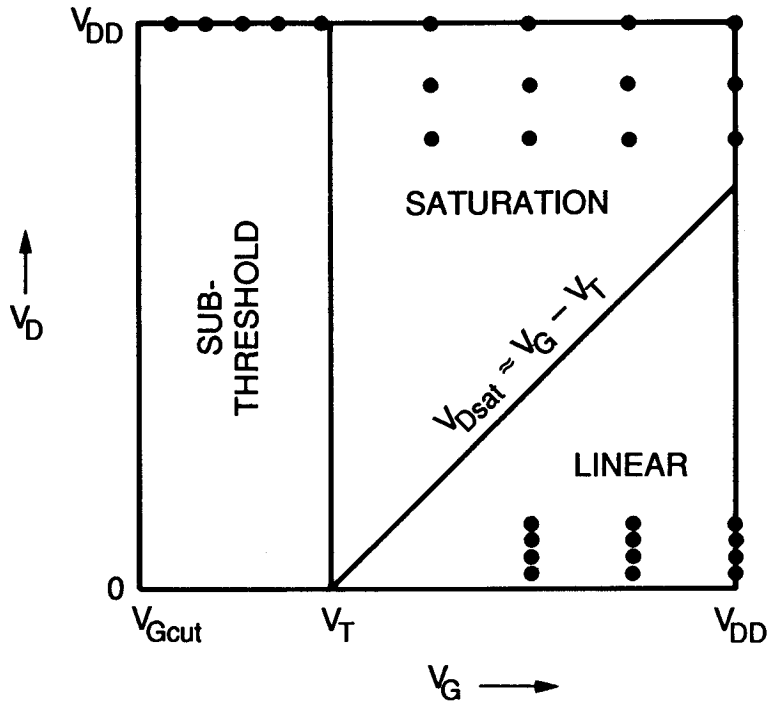

Figure 7.2: Map of operating regions of MOSFET model parameters

where ϵ_s is the dielectric constant of silicon and C'_{ox} is the gate-oxide capacitance per unit area. The term V_{Tsn} contains the short and narrow channel effects.

The threshold voltage of a "fat" transistor, i.e., one with dimensions so large that V_{Tsn} can be neglected, is denoted as

$$V_{Tf0} = V_{bi} + \gamma\sqrt{2\phi_f}. \tag{7.8}$$

The validity of Eq. 7.4 is restricted to not too large body voltages. We found reasonable fitting for $|V_B| \leq 2$ V. Measurements at $|V_B| = 0$, 0.75, and 1.5 V are recommended. Note that V_B values are negative for normal n-MOSFET operation. Although positive for normal p-MOSFET operation, they must be inserted negative into Eq. 7.4 as well.

The drain voltages $V_{D'sat}(V_{G'})$, which separate the linear region from the saturation region (cf. Fig. 7.2) are given by

$$V_{D'sat} = \frac{2(V_{G'} - V_T)/ac}{1 + \sqrt{1 + 2[(\epsilon - \theta')/abc^2](V_{G'} - V_T)}}, \tag{7.9}$$

where $a = 1+\delta$, $b = 1+\theta'(V_{G'} - V_T)$, and $c = 1+(\theta'/2ab)(V_{G'} - V_T)$. Here θ' is the gate-field mobility degradation coefficient, ϵ is the velocity saturation coefficient, and δ is the secondary body coefficient given by

$$\delta = \frac{D_0}{\sqrt{2\phi_f - V_B}} + \delta_{sn}, \tag{7.10}$$

where $D_0 \approx \gamma/4$ and where δ_{sn} contains the short and narrow channel terms.

In the *linear region*, i.e., $V_{D'} \leq V_{D'sat}$ and $V_{G'} \geq V_T$, the channel current is

$$I_C = \frac{\beta[V_{G'} - V_T - (1+\delta)V_{D'}/2]V_{D'}}{1 + \theta'(V_{G'} - V_T) + \zeta' V_{D'} + \theta_B V_B}. \tag{7.11}$$

Here β is the conduction factor and ζ_0 is the V_D-dependent fitting factor given by

$$\zeta' = \eta'(1 - 2V_{Z'} + V_{Z'}^2) + \epsilon(2 - V_{Z'})V_{Z'} + (\lambda - \frac{\theta'}{2})(1 - V_{Z'})V_{Z'} \tag{7.12}$$

with $V_{Z'} = V_{D'}/V_{D'sat}$; the intrinsic drain-field mobility degradation coefficient η'; the channel length modulation factor, λ; and the intrinsic gate-field mobility degradation coefficient, θ'. The θ_B accounts for the body voltage dependence of the mobility [7.7].

The expression of the channel current for the *saturation region*, i.e., $V_{D'} \geq V_{D'sat}$ and $V_{G'} \geq V_T$, is derived from the linear region by substituting $V_{D'sat}$ for $V_{D'}$ in Eq. 7.9 and reducing Eq. 7.12 to $\zeta' = \epsilon + \lambda(1 - V_{D'}/V_{D'sat})$, resulting in

$$I_C = \frac{\beta[V_{G'} - V_T - (1+\delta)V_{D'sat}/2]V_{D'sat}}{1 + \epsilon V_{D'sat} + \theta'(V_{G'} - V_T) - \lambda(V_{D'} - V_{D'sat}) + \theta_B V_B}. \tag{7.13}$$

An expression for the *body current*, I_B, which holds in the subthreshold region, where $V_G \leq V_T$ and $I_C = 0$, as well as in the active region, where $V_G \geq V_T$ and $I_C > 0$, was derived from Swanson's subthreshold model [7.8] and the Antognetti et al. subthreshold-active region model [7.9] by Blaes et al. [7.10] as

$$I_B = \frac{I_{Bo}(1 - \exp[-V_D/V_t])}{1 + \exp[-(V_G - V_T)/MV_t]}. \tag{7.14}$$

This equation contains two parameters which still depend on the body voltage, the first being

$$I_{Bo} = \frac{\beta\gamma_z V_t^2}{2\sqrt{2\phi_f - V_B}}, \tag{7.15}$$

where γ_z has the same physical interpretation as γ given in Eq. 7.5 but is treated as an independent fitting parameter, and the second being

$$M = \frac{M_o + \gamma_m/2\sqrt{2\phi_f - V_B}}{1 - V_t/2(2\phi_f - V_B)}, \tag{7.16}$$

where for γ_m holds what has been said about γ_z and

$$M_o = 1 + V_{it}/\phi_f \tag{7.17}$$

is related to the interface trap voltage.

The validity of Eq. 7.14 is restricted to body currents above some minimum value, I_{Bcut}, due to leakage currents and noise in the transistor and in the instrumentation. A procedure for determining I_{Bcut} will be given in the test procedure section.

The parameters β, δ, ϵ, η, θ, and λ, which describe the behavior of individual transistors, are dependent on the effective channel width and length, $W_e = W - \Delta W$ and $L_e = L - \Delta L$, which differ from the drawn quantities, W and L, by the the two-sided shrinkages ΔW and ΔL, respectively.

The conduction factor is given by

$$\beta = K_P \frac{W_e}{L_e}, \tag{7.18}$$

where $K_P = \mu_0 C'_{ox}$ is the intrinsic conduction factor with μ_0 being the zero-field channel mobility and C'_{ox} the gate oxide capacitance per unit area.

The dependence of the other individual parameters $p = \delta,\epsilon,\eta,\theta,\theta_B,\lambda$, is modeled by

$$p = p_0 + K_{WP}/W_e + K_{LP}/L_e, \tag{7.19}$$

where p_0 is the parameter value for a "fat" transistor and K_{LP} and K_{LW} are mainly empirical constants.

7.3. GEOMETRICAL DESCRIPTION/DESIGN PRINCIPLES: The layout and design principles of a single MOSFET have been briefly described in the previous chapter. In order to extract geometry-independent parameters, four MOSFETs [7.4] should be designed with the following dimensions. The minimum geometry MOSFET has a channel length-to-width ratio of L_m/W_m. The other three MOSFETs have ratios of NL_m/W_m, L_m/NW_m, and NL_m/NW_m with a recommended $N = 3$. The layout of this MOSFET Quartet is shown in Fig. 7.3. If not prohibited by design rules, the contacts should be elongated as shown and not created from a series of minimum geometry contacts. This allows a more accurate calculation of the source-drain series resistance. The contact length, d, should be kept constant as well as the distance between contact and gate, L_{CG}. Both lengths should be minimized.

7.4. TEST PROCEDURE:

7.4.1. Circuit diagram: See Fig. 7.4.

7.4.2. Test Conditions: First the threshold voltages are determined, from which the boundaries of the three regions of operation can be estimated, cf. Fig. 7.2. Then points (V_G, V_D) for the measurement of I_D are chosen in each region so that simplified equations can be used for easy parameter extraction.

7.4.2.1. Threshold Voltage: In the model equations presented in the preceding section the threshold voltage of a MOSFET has been implicitly defined as that voltage at which the potential at the surface of the silicon bulk equals $2\phi_f$. This condition is difficult to verify experimentally, especially when ϕ_f is not known a priori. Therefore a procedural approach is used here which is based on the maximum slope [7.11] of the $\sqrt{I_D}$ versus V_G curve measured in the saturation region with $V_D = V_{DD}$. For the extraction of the threshold voltage, the following approximations are made:
1. The body current is ignored by setting $I_B = 0$ so that $I_D = I_C$.
2. The expression for the channel current Eq. 7.13 is simplified by neglecting the

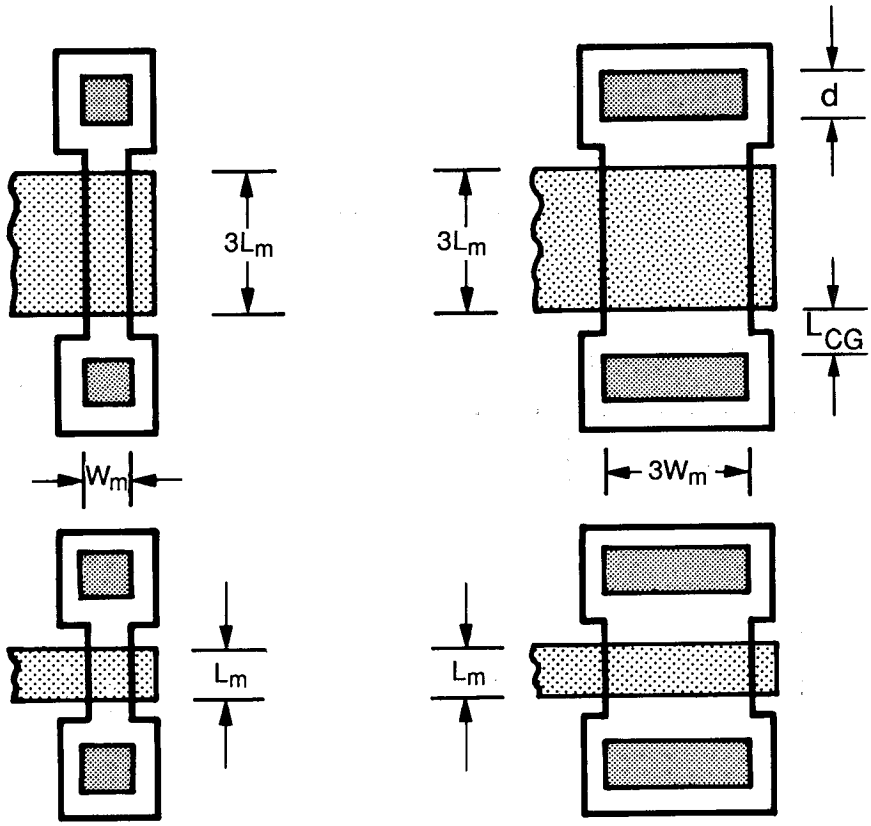

Figure 7.3: MOSFET Quartet for extracting geometry independent model parameters

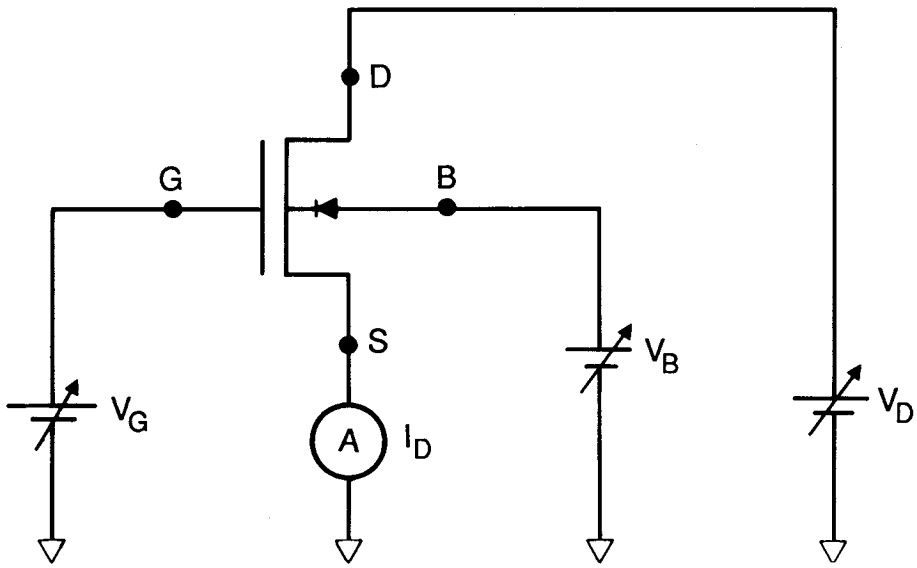

Figure 7.4: Measurement of MOSFET model parameters

terms with ϵ, θ, λ, and δ.
3. The difference between intrinsic and extrinsic voltages is neglected.
This leads to the simplified saturated drain current

$$\sqrt{I_D} = \sqrt{\frac{\beta}{2}}(V_G - V_T). \tag{7.20}$$

It is assumed now that the preceding relation holds at the maximum slope of the measured $\sqrt{I_D}$ versus V_G curve as illustrated in Fig. 7.5. Then the extracted conduction factor is

$$\beta_{max} = 2\left(\left.\frac{d\sqrt{I_D}}{dV_G}\right|_{max}\right)^2, \tag{7.21}$$

and the threshold voltage is

$$V_T = V_{Gmax} - \sqrt{\frac{2I_{Dmax}}{\beta_{max}}}, \tag{7.22}$$

where V_{Gmax} and I_{Dmax} are the coordinates of the maximum slope point on the $\sqrt{I_D}$ versus V_G curve. This threshold voltage is taken to be representative for the particular geometry and body voltage of the measured transistor. The conduction factor, however, has been given the index max to indicate that it depends largely on the used procedure. It will be determined more accurately later.

The point of maximum slope is determined by $F^{(2)} \equiv d^2F(I_D)/dV_G^2 = 0$, where $F(I_D) \equiv \sqrt{I_D}$. The following procedure is used to find that point and the value of the slope from a minimum set of data points: A set of $N = 5$ equidistant data points, centered at $V_{Gstart} \approx V_{Gmax}$ with increments of ΔV_G, is acquired and the 5-point smoothed second derivative of F in the center point evaluated, as explained below. If that derivative is greater (smaller) than zero, an additional equidistant data point at a larger (smaller) V_G is taken, the point at the smallest (largest) V_G is dropped, and the second derivative is calculated again. This is repeated until the second derivative changes sign. Then the point of maximum slope has been bracketed, and no further data are needed. Recommended gate voltages are: $V_{Gstart} = V_G(I_D = 1\mu\text{A})$ and $\Delta V_G = 50\text{mV}$. The method is illustrated in Figure 7.6. The first and second derivatives of the jth data set are denoted by $F_j^{(1)}$ and $F_j^{(2)}$, respectively. An algorithm for calculating $F_j^{(1)}$ and $F_j^{(2)}$ from $N \geq 5$ equidistant points by least-squares fitting to a cubic polynomial is described in Appendix C. The results for $N = 5$, with the ith drain current in the jth data set denoted by I_{Dj+i} and $i = -2, -1, 0, 1, 2$, are

$$F_j^{(1)} = \frac{dF(I_D)}{dV_G} = \frac{1}{12\Delta V_G}[F(I_{Dj-2}) - 8F(I_{Dj-1}) + 8F(I_{Dj+1}) - F(I_{Dj+2})] \tag{7.23}$$

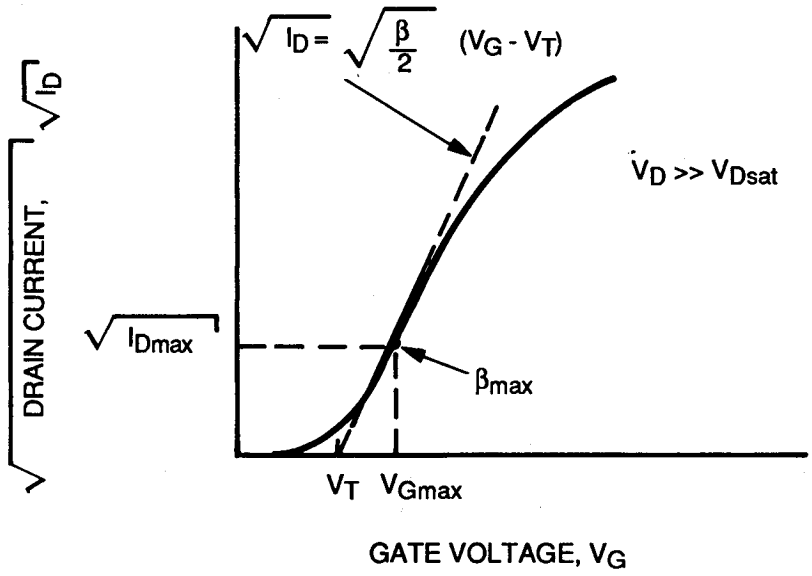

Figure 7.5: Threshold voltage derived from the maximum slope method applied to the MOSFET saturation region

and

$$F_j^{(2)} = \frac{d^2F(I_D)}{dV_G^2} \tag{7.24}$$
$$= \frac{1}{7\Delta V_G^2}[2F(I_{Dj-2}) - F(I_{Dj-1}) - 2F(I_{Dj}) - F(I_{Dj+1}) + 2F(I_{Dj+2})].$$

In the figure, the initial five-point data set, labeled Set 0, has a positive second derivative, $F_0^{(2)}$. Additional data sets, labeled Set 1, Set 2, and Set 3, have to be formed by measuring additional $I_D(V_G)$ values until the second derivative turns negative. The values of V_G and F at that inversion point, V_{Gmax} and F_{max}, respectively, are then calculated from two-point linear interpolation using the values measured on either side of the zero crossing of the second derivative. In Fig. 7.6, these two values of the second derivative are $F_2^{(2)}$ and $F_3^{(2)}$. Thus, V_{Gmax} is calculated from

$$V_{Gmax} = V_{Gk} + \frac{F_k^{(2)}}{F_k^{(2)} - F_{k+1}^{(2)}}\Delta V_G, \tag{7.25}$$

where the index k refers to the left bracketing data set (Set 2 in the figure) and k+1 to the right bracketing one (Set 3 in the figure). The term V_{Gk} denotes the center gate bias value of Set k. Likewise, F_{max} is calculated from

$$F_{max} = F_k + (F_{k+1} - F_k)\frac{(V_{Gmax} - V_{Gk})}{\Delta V_G}, \tag{7.26}$$

where F_k and F_{k+1} belong to the center values of the bracketing data sets.

Now, the value of the maximum slope of the $F(I_D)$ vs. V_G curve is determined from the first and second derivatives of the two bracketing data sets using cubic interpolation:

$$\begin{aligned} F_{max}^{(1)} = {} & F_k^{(1)} + F_k^{(2)}\delta V_G \\ & + [\frac{3}{\Delta V_G^2}(F_{k+1}^{(1)} - F_k^{(1)}) - \frac{1}{\Delta V_G}(F_{k+1}^{(2)} + 2F_k^{(2)})]\delta V_G^2 \\ & + [-\frac{2}{\Delta V_G^3}(F_{k+1}^{(1)} - F_k^{(1)}) + \frac{1}{\Delta V_G^2}(F_{k+1}^{(2)} + F_k^{(2)})]\delta V_G^3 \end{aligned} \tag{7.27}$$

where $\delta V_G = V_{Gmax} - V_{Gk}$. Implicit in this equation is the condition: $V_{Gk} < V_{Gmax} < V_{Gk+1}$.

Now the parameters β_{max} and V_T can be calculated from Eqs. 7.21 and 7.22, respectively, as

$$\beta_{max} = 2(F_{max}^{(1)})^2 \tag{7.28}$$

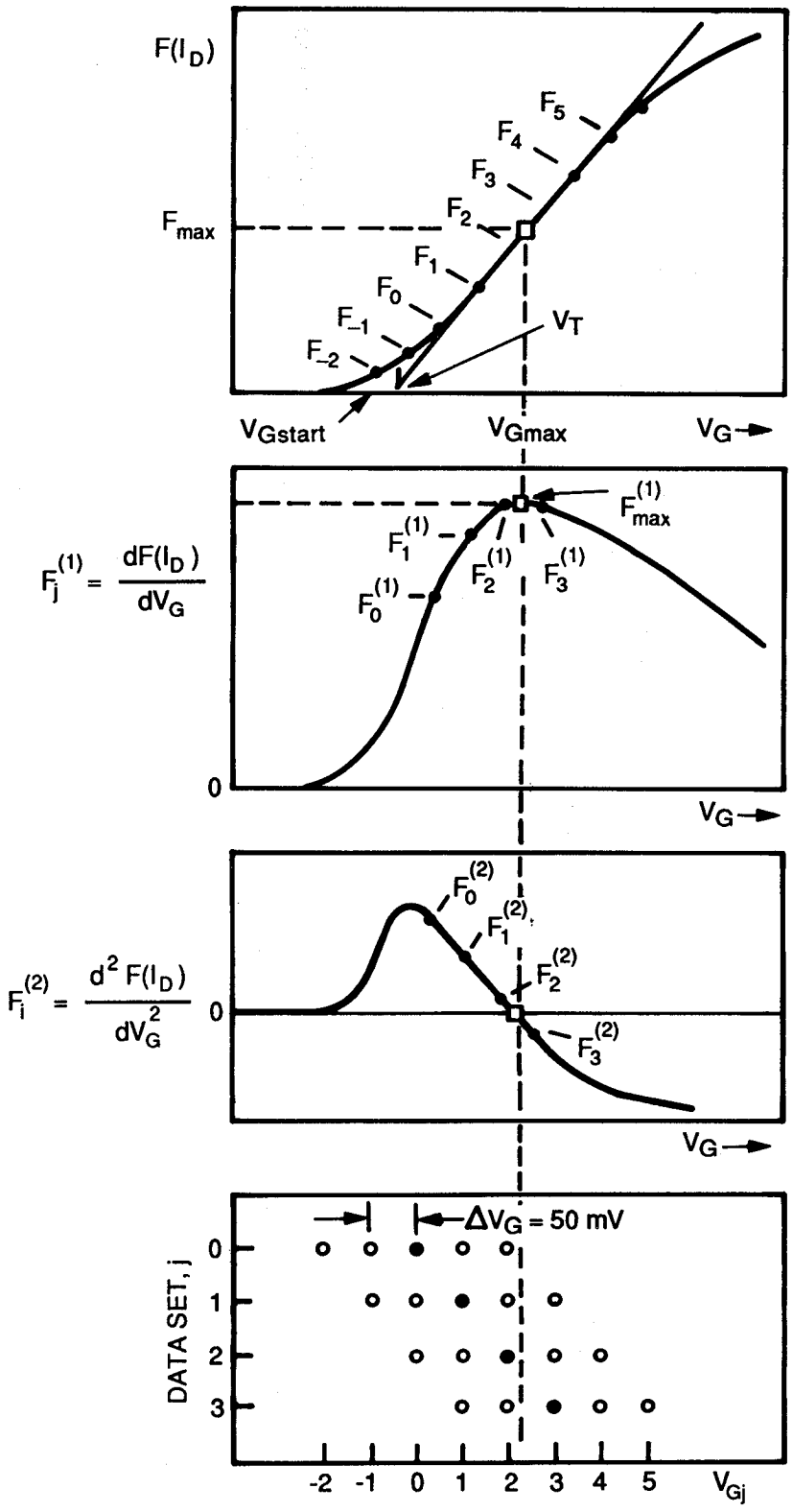

Figure 7.6: Five-point maximum slope method for determining the MOSFET threshold voltage

and

$$V_T = V_{Gmax} - \frac{F_{max}}{F_{max}^{(1)}}. \tag{7.29}$$

The procedure is carried out for $V_B = 0, -0.75, -1.5$ V.

7.4.2.2. Cutoff body current, I_{Bcut}: In the subthreshold region, $V_G \leq V_T$, the channel current is zero in our model; hence, the drain current, I_D, is given by the body current I_B. For $V_D \gg V_t$, Eq. 7.14 leads to the following simplified subthreshold region current expression:

$$\log I_B = \log(I_{Bo} - I_B) + \frac{V_G - V_T}{MV_t} \log e. \tag{7.30}$$

A plot of a measured $\log I_D$ vs. V_G curve is shown in Fig. 7.7. We define I_{Bcut} now as that current at which the first inversion point of that curve occurs when the current is lowered. The procedure, which searches for the second derivative going through zero, is identical to the one described in the previous section if one substitutes $\log I_D$ for F, V_{Gcut} for V_{Gmax}, and $\log I_{Bcut}$ for F_{max}, resulting in $I_{Bcut} = 10^{F_{max}}$. The procedure is carried out for $V_B = 0, -0.75, -1.5$ V.

7.4.2.3. Subthreshold Current: The drain current is measured in the subthreshold region, i.e., $V_{Gcut} < V_G < V_T$. For $V_B = 0, -0.75, -1.5$ V and a drain voltage of $V_D = V_{DD}$, the gate voltage is chosen as $V_G = V_T(V_B) - sV_t - (k/6)[V_T(V_B) - sV_t - V_{Gcut}(V_B)]$ with $k = 1, 2, 3, 4, 5$; $s = 1$ for n-channel; and $s = 0$ for p-channel transistors. This makes a total of 15 points in the subthreshold region, as shown in Figure 7.8.

7.4.2.4. Linear Current: The expression for the channel current, Eq. 7.11, can be transformed into a function of the extrinsic voltages, defined in Eqs. 7.1 and 7.2 as

$$I_c = \frac{\beta[V_G - V_T - (1+\delta)V_D/2]V_D}{1 + \theta(V_G - V_T) + \zeta V_D + \theta_B V_B}. \tag{7.31}$$

with

$$\theta = \theta' + 2\beta R \tag{7.32}$$

and

$$\zeta = \zeta' - \beta R - 2\delta\beta R. \tag{7.33}$$

In the derivation of these relations, terms $\propto I_C^2$ have been neglected. Furthermore, if we choose $V_D \ll V_{Dsat} \approx (V_G - V_T)$, we can set $\zeta_0 \approx \eta_0$, cf. Eq. 7.12. It is recommended that the drain current be measured for body voltages of $V_B = 0, -0.75, -1.5$ V with the drain voltage be set to $V_D = 0.05, 0.1, 0.2, 0.5$ V and the

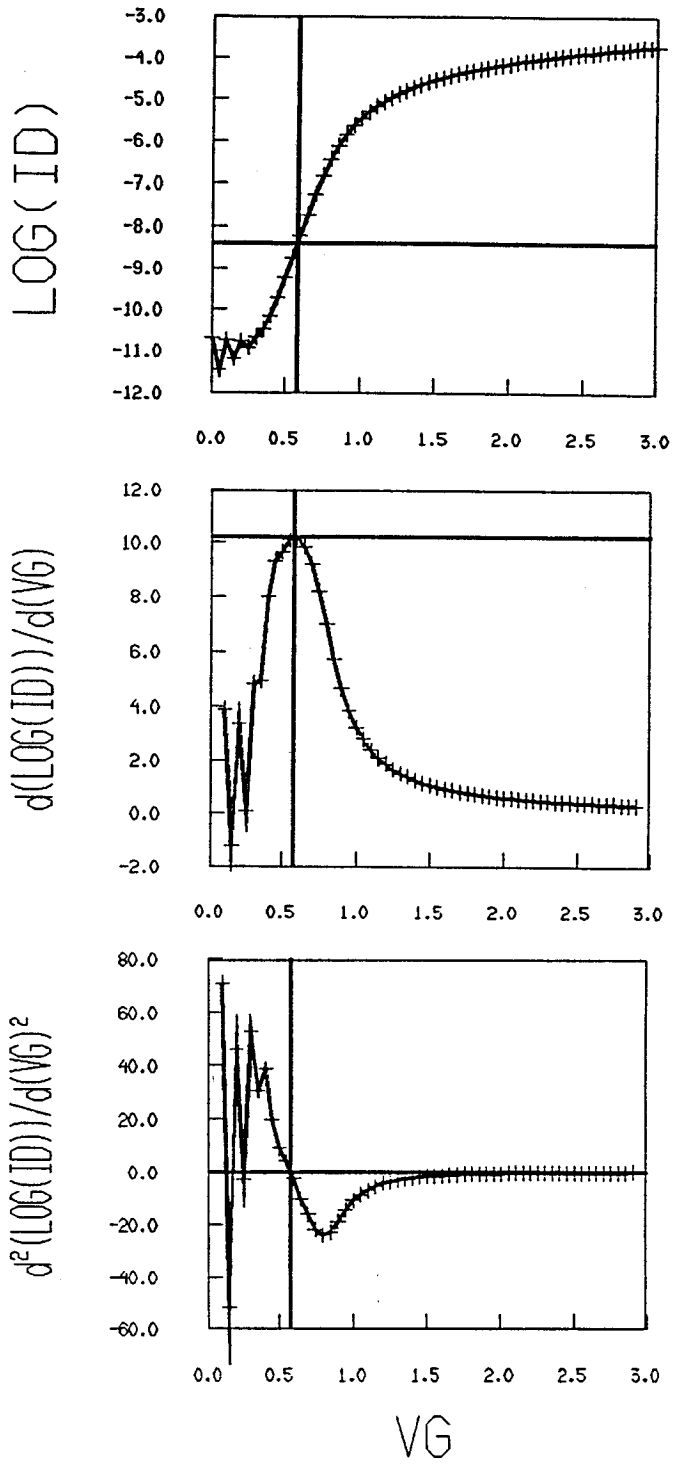

Figure 7.7: V_{Gcut} and I_{Bcut} derived from the maximum slope method applied to the subthreshold region. In this example $V_{Gcut} = 0.583$ V and $I_{Bcut} = 3.97$ nA.

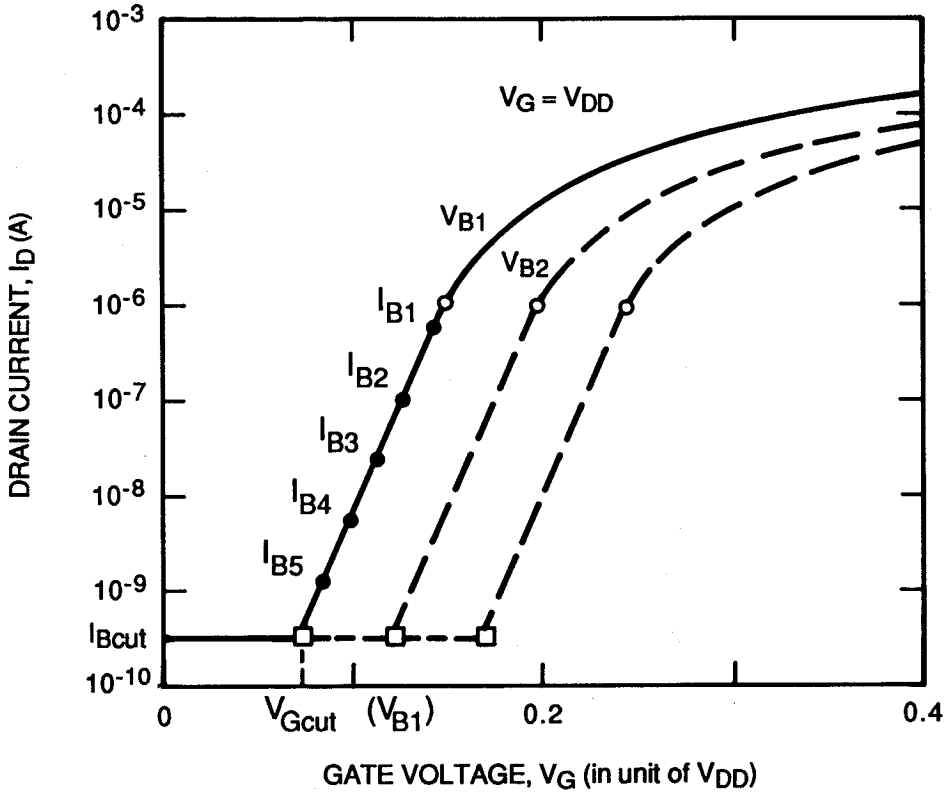

Figure 7.8: Subthreshold region extraction points (solid points) for body current parameters, cf. Eq. 7.31. Open points are threshold voltages determined from the maximum slope method.

gate voltage to $V_G = V_T(V_B) + (k/4)[V_{DD} - V_T(V_B)]$ with $k = 2, 3, 4$. This makes a total of 36 points in the linear region, as illustrated in Fig. 7.9.

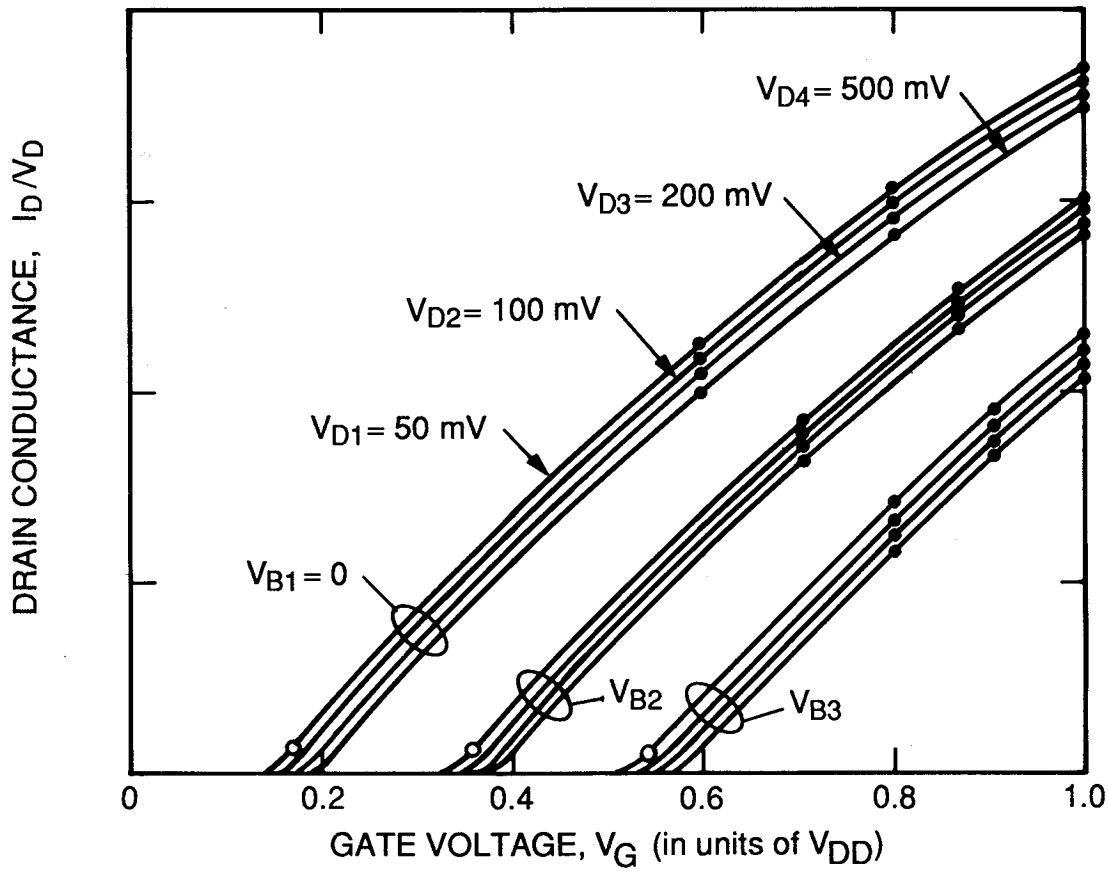

Figure 7.9: Linear region extraction points (solid points) for drain current parameters, cf. Eq. 7.32. Open points are threshold voltages determined from the maximum slope method.

7.4.2.5. Saturation Current: The drain current is measured in the saturation region, i.e. $V_G > V_T$ and $V_D > V_{Dsat} \approx (V_G - V_T)$, cf. Fig. 7.2. It is recommended that for body voltages of $V_B = 0, -0.75, -1.5$ V, the drain voltage be set to $V_D = 0.8V_{DD}, 0.9V_{DD}, 1.0V_{DD}$ and the gate voltage to $V_G = V_T(V_B) + (k/4)[V_{DD} - V_T(V_B)]$ with $k = 1, 2, 3, 4$. This makes a total of 36 points in the saturation region, illustrated in Fig. 7.10.

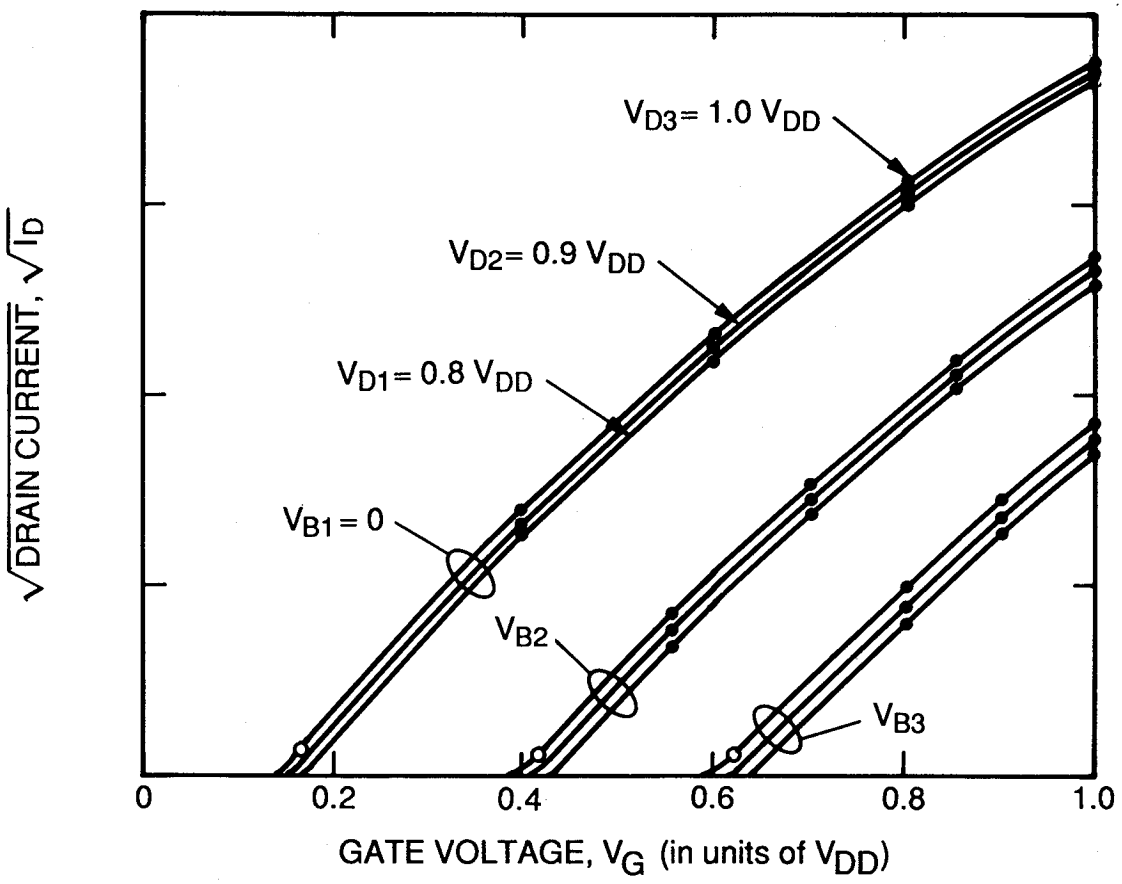

Figure 7.10: Saturation region extraction points (solid points) for drain current parameters, cf. Eq. 7.15. Open points are threshold voltages determined from the maximum slope method.

7.4.3. Data reduction algorithms: In the following reduction procedures, the known parameters are listed after the term "GIVEN", and the unknown parameters are listed after the term "FIND". Parameters are extracted using a least-squares fit [7.12] of the model equations to the data. Thus, the number of data points required is at least one more than the number of parameters to be extracted. Extracted parameters are enclosed in angle brackets in the equations shown below.

7.4.3.1. Subthreshold analysis: GIVEN $I_D(V_G, V_B)$ in the subthreshold region as specified by the test procedures, $V_T(V_B)$, V_t; FIND I_{Bo}, $M(V_B)$. The data reduction algorithm is obtained from Eq. 7.14. After linearizing this equation by taking logarithms and assuming that $V_D \gg V_t$, the subthreshold drain currrent $I_D \approx I_B$ is characterized by

$$\ln I_D = \langle \ln I_{Bo}(V_B) \rangle 1 + \langle \frac{1}{M(V_B)} \rangle \frac{V_G - V_T}{V_t}. \tag{7.34}$$

7.4.3.2. Linear analysis: GIVEN $I_D(V_G, V_D, V_B)$ as specified by the test procedures, $V_T(V_B)$; FIND β , θ, η, γ. The data reduction algorithm is obtained from the channel current expression, Eq. 7.31 with $\zeta \approx \eta$, and $I_C = I_D - I_B$. Furthermore, the δ term can be neglected in the extraction region, resulting in

$$\frac{I_D}{V_D} = \langle \beta \rangle (V_G - V_T - \frac{V_D}{2}) - \langle \theta \rangle \frac{I_D}{V_D}(V_G - V_T) - \langle \eta \rangle I_D - \langle \delta\beta \rangle \frac{V_D}{2} - \langle \theta_B \rangle \frac{I_D}{V_D} V_B, \tag{7.35}$$

which is first solved for sets of 12 data points $I_D(V_G, V_D, V_B)$ with $V_B = const$ in order to extract $\delta(V_B)$ and then solved for body voltage independent β, θ, η, and θ_B simultaneously for all 36 data points of each of the four transistors. The $\delta(V_B)$ of this routine will be replaced later by values extracted from the saturation region.

7.4.3.3. Conduction factor analysis: GIVEN $\beta(W, L)$; FIND K_P, ΔW, ΔL, W_e, L_e. The analysis follows from Eq. 7.18. This equation can be algebraically rearranged to yield the following system of 4 linear equations:

$$\beta L = \langle K_P \rangle W - \langle K_P \Delta W \rangle + \langle \Delta L \rangle \beta. \tag{7.36}$$

For the following equations the effective gate dimensions are now calculated as $W_e = W - \Delta W$ and $L_e = L - \Delta L$.

7.4.3.4. Gate field mobility and series resistance analysis: GIVEN K_P, θ, L_e, W_e, FIND θ_0, K_{WT}, K_{LT} or R_P, R. The source or drain series resistance is contained in the extrinsic θ, cf. Eq. 7.32. Assuming that the source and drain series resistors

have the same effective length L^* between the contact and the channel for all four transistors, the series resistance can be written as

$$R = R_P/W_e = R_s L^*/W_e, \tag{7.37}$$

where R_p is the source or drain resistance per unit width, and R_s the sheet resistance of the source drain regions.

The combination of this expression with the β expression, Eq. 7.18, and substitution into Eq. 7.32 leads to the extraction equation

$$\theta = \langle\theta_0\rangle + \langle K_{WT}\rangle/W_e + \langle 2R_P K_P + K_{LT}\rangle/L_e, \tag{7.38}$$

where W_e, L_e, and K_P come from the preceding conduction factor analysis. For $L \geq 1.6\mu$m we obtained good fits of the current in the linear region by assuming $K_{LT} \approx 0$ and extracting R_P from the last term in Eq. 7.38. For $L = 1.2\mu$m, however, this procedure did not result in good fits. The results improved substantially by calculating R_P from Split-Cross-Bridge and Contact Resistor data (see those chapters) and extracting K_{LT}. The effective source or drain resistor length is calculated as $L^* = L_{CG} + \Delta L/2 + L_t \coth(d/L_t)$ with the transfer length $L_t = \sqrt{\rho/R_s}$, where L_{CG} is the drawn distance from contact to gate and ρ and d are the resistivity and length of the contact, respectively. For consistency, we recommend the latter procedure in general. The series resistance is in any case calculated from Eq. 7.37.

7.4.3.5. Body-voltage mobility analysis: GIVEN θ_B; FIND θ_{B0}, K_{WTB}, K_{LTB}. The global parameters of the body voltage mobility degradation coefficient are extracted from

$$\theta_B = \langle\theta_{B0}\rangle + \langle K_{WTB}\rangle/W_e + \langle K_{LTB}\rangle/L_e. \tag{7.39}$$

7.4.3.6. Threshold analysis: GIVEN $V_T(V_B)$, W_e, L_e, $2\phi_f$ or C'_{ox}; FIND V_{bi}, γ, V_{T0}, $2\phi_f$, K_{WG}, K_{LG}. We extract V_{bi}, γ, K_{WG}, and K_{LG} by fitting Eq. 7.4:

$$V_T = \langle V_{bi}\rangle + \langle\gamma\rangle\sqrt{2\phi_f - V_B} + \langle K_{WG}\rangle/W_e - \langle K_{WL}\rangle/L_e \tag{7.40}$$

The goodness of the fit and even the value of γ is quite insensitive to the value of ϕ_f, so that a rough idea of the doping will lead with Eq. 7.6 to reasonable results. While 3-μm processes used doping densities of $N \approx 10^{15}/\text{cm}^3$ leading to $2\phi_f \approx 0.6$ V, the doping density in the channel of 1.6-μm gate transistors is an order of magnitude higher leading to $2\phi_f \approx 0.7$ V. In the context of the present publication, we recommend using the information about the gate-oxide capacitance per unit area, $C'_{ox} = \epsilon_{ox}/T_{ox}$, extracted with the MOSFET capacitor (see that chapter), together with Eq. 7.7 to calculate a second estimate of N. Because of the logarithmic dependence of ϕ_f on N, an iterative procedure including Eqs. 7.40, 7.7, and 7.6 converges very rapidly.

7.4.3.7. M-factor analysis: GIVEN $M(V_B)$, $2\phi_f$, V_t; FIND M_o, γ_m, V_{it}, V_{FB0}). The data reduction algorithm follows from Eq. 7.16:

$$M\left[1-\frac{1}{2}\left(\frac{V_t}{2\phi_f-V_B}\right)\right]=\langle M_o\rangle+\langle\gamma_m\rangle\frac{1}{2\sqrt{2\phi_f-V_B}}. \tag{7.41}$$

The interface trap voltage is calculated from Eq. 7.17 as

$$V_{it}=(M_o-1)\phi_f, \tag{7.42}$$

and the flatband voltage due to workfunction difference and oxide traps is calculated from Eq. 7.8 as

$$V_{FB0}=2\phi_f+V_{it}-V_{bi} \tag{7.43}$$

for an n-MOSFET, and as

$$V_{FB0}=V_{bi}-2\phi_f-V_{it} \tag{7.44}$$

for a p-MOSFET.

7.4.3.8. I_{Bo}-factor analysis: GIVEN $I_{Bo}(V_B)$, β, V_t, $2\phi_f$; FIND γ_z. The data reduction algorithm follows from Eq. 7.15:

$$I_{Bo}=\langle\gamma_z\rangle\frac{\beta V_t^2}{2\sqrt{2\phi_f-V_B}}. \tag{7.45}$$

The values for β come from the linear region analysis.

7.4.3.9. Saturation analysis: GIVEN $I_D(V_G,V_D,V_B)$ as specified by the test procedure, $I_{Bo}(V_B)$, $V_T(V_B)$, β, θ, θ_B; FIND $\delta(V_B)$, ϵ, λ. The data reduction algorithm follows from the channel saturation current expression, Eq. 7.13, which holds for $V_G<V_D+V_T(V_B)$. For $V_G>V_T(V_B)+3V_t$ we can replace I_C by I_D-I_{Bo}. The values for β and θ come from the linear region analysis. The extraction equation is

$$\begin{aligned}I_C[1+\theta'(V_{G'}-V_T)+\theta_BV_B]-\beta(V_{G'}-V_T-V_{D'sat}/2)V_{D'sat}\\ =\langle\delta(V_B)\rangle-\langle\epsilon\rangle V_{D'sat}I_C+\langle\lambda\rangle(V_{D'}-V_{D'sat})I_C,\end{aligned} \tag{7.46}$$

where $I_C\approx I_D-I_{Bo}$ with $I_{Bo}=\gamma_z\beta V_t^2/2\sqrt{2\phi_f-V_B}$ and $V_{D'sat}$ is given by Eq. 7.9. As $V_{D'sat}$ depends also on δ and ϵ, a few iterations between Eqs. 7.9 and 7.46 are necessary, starting with $\epsilon=\delta=0$ in Eq. 7.9. This system is first solved for the three groups of twelve data points with $V_B=const$ separately in order to extract $\delta(V_B)$. The parameters ϵ and λ, which appear to depend on V_B after this step, are now consolidated by solving the complete system Eq. 7.46 of 36 equations simultaneously with $\delta(V_B)$ as a known variable and only ϵ and λ as (body voltage independent) fitting parameters.

7.4.3.10. Secondary body effect analysis: GIVEN $\delta(V_B)$, $2\phi_f$, W_e, L_e; FIND D_0, K_{WD}, K_{LD}. The data reduction algorithm follows from Eq. 7.10 as

$$\delta = \langle D_0 \rangle \frac{1}{\sqrt{2\phi_f - V_B}} + \langle K_{WD} \rangle / W_e + \langle K_{LD} \rangle / L_e. \tag{7.47}$$

7.4.3.11. Drain-field mobility analysis: GIVEN η, β, R, δ, W_e, L_e; FIND η_0, K_{WH}, K_{LH}. The global parameters of the drain-field mobility degradation factor are obtained from

$$\eta' = \eta + \beta R = \langle \eta_0 \rangle + \langle K_{WH} \rangle / W_e + \langle K_{LH} \rangle / L_e. \tag{7.48}$$

This equation has been derived from Eqs. 7.33 and 7.12 with term $\delta\beta R$ neglected.

7.4.3.12. Velocity saturation analysis: GIVEN ϵ, W_e, L_e; FIND ϵ_0, K_{WE}, K_{LE}. The data reduction algorithm follows from Eq. 7.19 as

$$\epsilon = \langle \epsilon_0 \rangle + \langle K_{WE} \rangle / W_e + \langle K_{LE} \rangle / L_e. \tag{7.49}$$

7.4.3.13. Channel length modulation analysis: GIVEN λ, W_e, L_e; FIND λ_0, K_{WL}, K_{LL}. The data reduction algorithm follows from Eq. 7.19 as

$$\lambda = \langle \lambda_0 \rangle + \langle K_{WL} \rangle / W_e + \langle K_{LL} \rangle / L_e. \tag{7.50}$$

The the test and extraction procedures are summarized in Table 7.2.

7.5. RESULTS: The model presented above has been successfully applied to MOSFET Quartets fabricated in 2-, 1.6-, and 1.2-μm technologies. The extracted global, i.e., geometry independent, parameters are quite stable and the goodness of fit to the experimental data is only slightly deteriorated at 1.2 μm. We present, therefore, a typical 1.2-μm result as the worst case.

Tables 7.3 and 7.4 list the global parameters for n- and p-channel MOSFETs extracted from one Quartet each, located on the same chip. Also, the absolute and relative errors are given. Most of the parameters with negative values are essentially zero except θ_B, which must be negative in order to compensate for the negative sign of V_B. Large differences in ΔW and ΔL between n- and p-channel devices have been seen in all fabrication runs.

Tables 7.5 and 7.6 list the individual n- and p-MOSFET parameters which were calculated from the global parameters as a function of (W, L, V_B). The correlation between the drain currents calculated from these parameters and those measured over the *entire* linear and saturation regions (all data points in Figs. 7.12 and 7.13

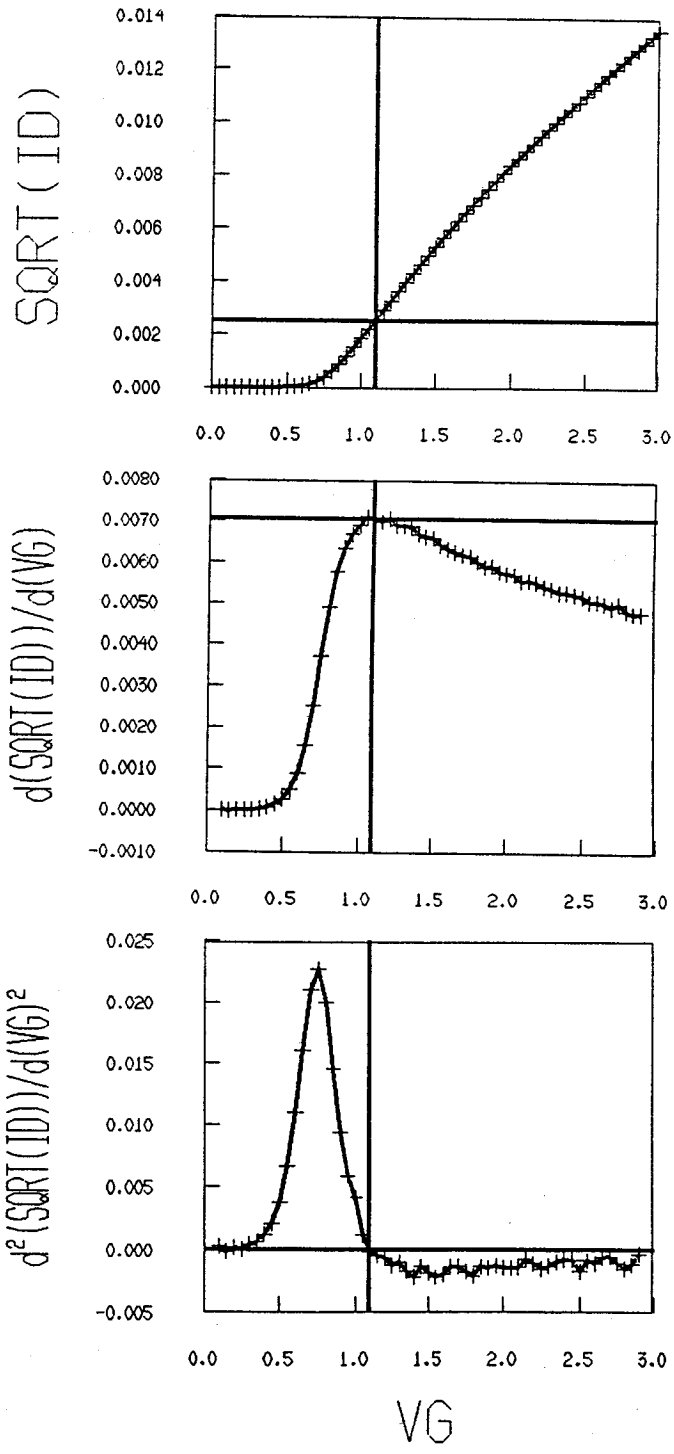

Figure 7.11: Maximum slope method for saturation region threshold voltage. In this example $V_{Gmax} = 1.094$ V, $I_{Dmax} = 6.30\mu$A, $\beta = 99.2\mu\text{A/V}^2$ resulting in $V_T = 0.711$ V

Table 7.2: MOSFET Parameter Extraction Procedures

Input variables	Output variables
Test procedures	
$V_{Gstart}, \Delta V_G = 50\text{mV}, V_B, V_D = V_{DD}$	$V_T(V_B), V_{Gcut}(V_B)$
$V_G = V_T(V_B) - sV_t - (k/6)[V_T(V_B) - sV_t$	⎤
$-V_{Gcut}(V_B)]$; $k = 1,2,3,4,5$	⟩ I_D(subthreshold)
$s = (1,0)$ for (n,p)-channel, $V_D = V_{DD}, V_B$	⎦
$V_G = V_T(V_B) + (k/4)[V_{DD} - V_T(V_B)]$	⎤
$k = 2,3,4$	⟩ I_D(linear)
$V_D = (0.05, 0.1, 0.2, 0.5)\text{V}$, V_B	⎦
$V_G = V_T(V_B) + (k/4)[V_{DD} - V_T(V_B)]$	⎤
$k = 1,2,3,4$	⟩ I_D(saturation)
$V_D = (0.8, 0.9, 1.0)\text{V}$, V_B	⎦
Data reduction procedures	
I_D(subthreshold), $V_T(V_B)$	$I_{B0}(V_B), M(V_B)$
I_D(linear), $V_T(V_B)$	$\beta, \theta, \eta, \theta_B$
β	$K_P, \Delta W, \Delta L, W_e, L_e$
$\theta, K_P, W_e, L_e, [R_s^*, \rho^*]$	$\theta_0, K_{WT}, [K_{LT}], R_P, R$
θ_B	$\theta_{B0}, K_{WTB}, K_{LTB}$
$V_T(V_B), W_e, L_e, 2\phi_f^*, [C_{ox}'^*]$	$V_{bi}, \gamma, V_{T0}, [2\phi_f], K_{WG}, K_{LG}$
$M(V_B), 2\phi_f$	$M_0, \gamma_m, V_{it}, V_{FB0}$
$I_{B0}(V_B), \beta, 2\phi_f$	γ_z
I_D(saturation), $I_{B0}(V_B), V_T(V_B), \beta, \theta, \theta_B$	$\delta(V_B), \epsilon, \lambda$
$\delta(V_B), 2\phi_f, W_e, L_e$	D_0, K_{WD}, K_{LD}
η, β, R, W_e, L_e	η_0, K_{WH}, K_{LH}
ϵ, W_e, L_e	$\epsilon_0, K_{WE}, K_{LE}$
λ, W_e, L_e	$\lambda_0, K_{WL}, K_{LL}$

Throughout $V_B = (0, -0.75, -1.5)\text{V}$; [] optional; * auxiliary parameters

top or bottom plots) is for each (W, L, V_B) expressed in the correlation coefficient CC. The average correlation coefficients for the n- and p-channel transistors are 0.9990 and 0.9994, respectively.

Figs. 7.12 and 7.13 show, as typical examples, measured data points and calculated curves for n- and p-channel transistors the correlation coefficient of which happened to coincide with the just mentioned averages. The I_D vs. V_D plots emphasize the saturation region, the I_D/V_D vs. V_G plots the linear region, and the $\log I_D$ vs. V_G the subthreshold region. The data points used in the parameter extraction procedures are filled by a cross. Both figures show good fits in all regions; however, the n-channel transistor curves show the larger deviations, as expected from the smaller correlation coefficient. No systematic dependence of CC on (W, L, V_B) has been seen. Correlation coefficients for transistors with $L_m \geq 1.6\mu$m were consistently greater than 0.9990.

Table 7.3: Global Model Parameters for n-Channel Transistors of $1.2-\mu$m CMOS N-Well Process

GIVEN:	Rs(Ω/sq)	=	80.70				
	ρ(Ω μm^2)	=	77.59				
	Tox(nm)	=	21.40				
SUBSTRATE:	NSUB(cm^{-3})	=	2.83E+16				
	2ϕf(V)	=	0.749				
BETA:	KP($\mu A/V^2$)=μoCo	=	87.609	±	1.869	(	2.13%)
	ΔW(μm)	=	0.383	±	0.038	(	10.02%)
	ΔL(μm)	=	0.362	±	0.037	(	10.30%)
THRESHOLD:	VTfØ(V)	=	0.779	±	0.059	(	7.59%)
	VFB(V)	=	0.537	±	0.050	(	9.33%)
	Γ($\sqrt{V}$)	=	0.606	±	0.036	(	5.99%)
	KLG(V*μm)	=	0.133	±	0.021	(	16.06%)
	KWG(V*μm)	=	-0.005	±	0.037	(	-817.91%)
DELTA:	DØ($\sqrt{V}$)	=	0.187	±	0.035	(	18.76%)
	KLD(μm)	=	0.365	±	0.029	(	7.95%)
	KWD(μm)	=	0.185	±	0.050	(	27.22%)
THETA:	ΘØ(1/V)	=	0.071	±	0.007	(	9.79%)
	KLT(μm/V)	=	0.061	±	0.006	(	9.70%)
	KWT(μm/V)	=	0.067	±	0.010	(	15.41%)
THETAB:	ΘbØ(1/V)	=	-0.0230	±	0.0041	(	-18.00%)
	KLTB(μm/V)	=	-0.0061	±	0.0035	(	-58.05%)
	KWTB(μm/V)	=	-0.0456	±	0.0061	(	-13.47%)
ETA:	HØ(1/V)	=	-0.048	±	0.001	(	-1.91%)
	KLH(μm/V)	=	0.039	±	0.001	(	1.96%)
	KWH(μm/V)	=	0.005	±	0.001	(	25.86%)
EPSILON:	EØ(1/V)	=	0.068	±	0.039	(	57.18%)
	KLE(μm/V)	=	0.478	±	0.033	(	6.96%)
	KWE(μm/V)	=	-0.045	±	0.058	(	-130.05%)
LAMBDA:	LØ(1/V)	=	0.000	±	0.002	(	816.06%)
	KLL(μm/V)	=	0.038	±	0.002	(	6.43%)
M:	MØ(unitless)	=	1.117	±	0.079	(	7.11%)
	Vit(V)	=	0.044	±	0.030	(	68.06%)
	Γm($\sqrt{V}$)	=	0.810	±	0.176	(	21.69%)
IBØ:	Γz($\sqrt{V}$)	=	3.384	±	0.317	(	9.38%)

Table 7.4: Global Model Parameters for p-Channel Transistors of $1.2-\mu$m CMOS N-Well Process

GIVEN:	Rs(Ω/sq)	=	130.00				
	ρ(Ω μm^2)	=	70.72				
	Tox(nm)	=	21.40				
SUBSTRATE:	NSUB(cm^{-3})	=	1.64E+16				
	$2\phi f$(V)	=	0.720				
BETA:	KP($\mu A/V^2$)=μoCo	=	29.058	±	0.010	(	0.04%)
	ΔW(μm)	=	0.471	±	0.001	(	0.12%)
	ΔL(μm)	=	-0.030	±	0.001	(	-2.49%)
THRESHOLD:	VTfØ(V)	=	0.967	±	0.025	(	2.58%)
	VFB(V)	=	-0.253	±	0.021	(	-8.42%)
	Γ($\sqrt{V}$)	=	0.461	±	0.015	(	3.30%)
	KLG(V*μm)	=	0.148	±	0.015	(	10.07%)
	KWG(V*μm)	=	0.001	±	0.015	(	1027.45%)
DELTA:	DØ($\sqrt{V}$)	=	0.183	±	0.021	(	11.61%)
	KLD(μm)	=	0.304	±	0.027	(	9.02%)
	KWD(μm)	=	0.096	±	0.027	(	28.53%)
THETA:	ΘØ(1/V)	=	0.135	±	0.008	(	5.79%)
	KLT(μm/V)	=	0.023	±	0.010	(	43.91%)
	KWT(μm/V)	=	0.080	±	0.010	(	12.50%)
THETAB:	ΘbØ(1/V)	=	-0.0760	±	0.0025	(	-3.25%)
	KLTB(μm/V)	=	0.0016	±	0.0032	(	204.36%)
	KWTB(μm/V)	=	-0.0137	±	0.0032	(	-23.04%)
ETA:	HØ(1/V)	=	0.020	±	0.001	(	3.45%)
	KLH(μm/V)	=	0.012	±	0.001	(	7.85%)
	KWH(μm/V)	=	-0.019	±	0.001	(	-4.66%)
EPSILON:	EØ(1/V)	=	0.058	±	0.014	(	23.70%)
	KLE(μm/V)	=	0.154	±	0.018	(	11.74%)
	KWE(μm/V)	=	0.008	±	0.018	(	223.91%)
LAMBDA:	LØ(1/V)	=	0.001	±	0.002	(	232.22%)
	KLL(μm/V)	=	0.091	±	0.003	(	3.33%)
M:	MØ(unitless)	=	1.300	±	0.105	(	8.09%)
	Vit(V)	=	0.108	±	0.038	(	35.03%)
	Γm($\sqrt{V}$)	=	0.434	±	0.230	(	52.88%)
IBØ:	Γz($\sqrt{V}$)	=	3.434	±	0.215	(	6.26%)

Table 7.5: Individual Model Parameters for n-Channel Transistors of 1.2 – μm CMOS N-Well Process

L	W	VB	β	VT	δ	θ′	η	ε	λ	R	CC
1.20	5.40	0.00	5.24E-04	0.620	-0.183	0.131	0.000	0.493	0.045	42.1	0.9981
3.60	5.40	0.00	1.36E-04	0.737	0.140	0.077	-0.034	0.070	0.012	42.1	0.9995
3.60	1.80	0.00	3.83E-05	0.735	0.234	0.043	-0.032	0.048	0.012	149.0	0.9997
1.20	1.80	0.00	1.48E-04	0.618	-0.089	0.097	0.003	0.471	0.045	149.0	0.9981
1.20	5.40	-0.75	5.24E-04	0.837	-0.246	0.131	0.000	0.493	0.045	42.1	0.9979
3.60	5.40	-0.75	1.36E-04	0.955	0.077	0.077	-0.034	0.070	0.012	42.1	0.9999
3.60	1.80	-0.75	3.83E-05	0.952	0.170	0.043	-0.032	0.048	0.012	149.0	0.9993
1.20	1.80	-0.75	1.48E-04	0.835	-0.152	0.097	0.003	0.471	0.045	149.0	0.9986
1.20	5.40	-1.50	5.24E-04	1.004	-0.274	0.131	0.000	0.493	0.045	42.1	0.9989
3.60	5.40	-1.50	1.36E-04	1.121	0.049	0.077	-0.034	0.070	0.012	42.1	0.9999
3.60	1.80	-1.50	3.83E-05	1.119	0.142	0.043	-0.032	0.048	0.012	149.0	0.9995
1.20	1.80	-1.50	1.48E-04	1.002	-0.180	0.097	0.003	0.471	0.045	149.0	0.9982

L	W	VB	IBØ	M	Temp	IDØ	θb
1.20	5.40	0.00	6.85E-07	1.609	300.0	1.31E-11	-0.0378
3.60	5.40	0.00	1.77E-07	1.609	300.0	7.86E-12	-0.0356
3.60	1.80	0.00	5.01E-08	1.609	300.0	3.54E-11	-0.0556
1.20	1.80	0.00	1.93E-07	1.609	300.0	9.84E-12	-0.0640
1.20	5.40	-0.75	4.84E-07	1.463	300.0	3.36E-11	-0.0378
3.60	5.40	-0.75	1.25E-07	1.463	300.0	1.43E-11	-0.0356
3.60	1.80	-0.75	3.54E-08	1.463	300.0	1.52E-11	-0.0556
1.20	1.80	-0.75	1.37E-07	1.463	300.0	2.05E-11	-0.0640
1.20	5.40	-1.50	3.95E-07	1.399	300.0	2.60E-11	-0.0378
3.60	5.40	-1.50	1.02E-07	1.399	300.0	3.35E-11	-0.0356
3.60	1.80	-1.50	2.89E-08	1.399	300.0	3.43E-11	-0.0556
1.20	1.80	-1.50	1.12E-07	1.399	300.0	1.79E-11	-0.0640

Table 7.6: Individual Model Parameters for p-Channel Transistors of $1.2 - \mu$m CMOS N-Well Process

L	W	VB	β	VT	δ	θ′	η	ε	λ	R	CC
1.20	5.40	0.00	1.16E-04	0.847	-0.012	0.138	0.026	0.068	0.075	81.7	0.9998
3.60	5.40	0.00	3.95E-05	0.927	0.152	0.125	0.019	-0.014	0.026	81.7	0.9998
3.60	1.80	0.00	1.06E-05	0.927	0.205	0.081	0.009	-0.010	0.026	302.9	0.9998
1.20	1.80	0.00	3.14E-05	0.848	0.041	0.094	0.015	0.073	0.075	302.9	0.9994
1.20	5.40	-0.75	1.16E-04	1.015	-0.077	0.138	0.026	0.068	0.075	81.7	0.9993
3.60	5.40	-0.75	3.95E-05	1.094	0.087	0.125	0.019	-0.014	0.026	81.7	0.9997
3.60	1.80	-0.75	1.06E-05	1.095	0.140	0.081	0.009	-0.010	0.026	302.9	0.9991
1.20	1.80	-0.75	3.14E-05	1.016	-0.024	0.094	0.015	0.073	0.075	302.9	0.9998
1.20	5.40	-1.50	1.16E-04	1.143	-0.105	0.138	0.026	0.068	0.075	81.7	0.9995
3.60	5.40	-1.50	3.95E-05	1.222	0.059	0.125	0.019	-0.014	0.026	81.7	0.9996
3.60	1.80	-1.50	1.06E-05	1.223	0.112	0.081	0.009	-0.010	0.026	302.9	0.9989
1.20	1.80	-1.50	3.14E-05	1.144	-0.052	0.094	0.015	0.073	0.075	302.9	0.9998

L	W	VB	IBØ	M	Temp	IDØ	θb
1.20	5.40	0.00	1.57E-07	1.580	300.0	3.41E-11	-0.0767
3.60	5.40	0.00	5.33E-08	1.580	300.0	3.94E-11	-0.0792
3.60	1.80	0.00	1.44E-08	1.580	300.0	1.66E-12	-0.0850
1.20	1.80	0.00	4.24E-08	1.580	300.0	4.94E-11	-0.0859
1.20	5.40	-0.75	1.10E-07	1.495	300.0	5.48E-11	-0.0767
3.60	5.40	-0.75	3.73E-08	1.495	300.0	5.42E-11	-0.0792
3.60	1.80	-0.75	1.01E-08	1.495	300.0	3.22E-11	-0.0850
1.20	1.80	-0.75	2.97E-08	1.495	300.0	5.88E-11	-0.0859
1.20	5.40	-1.50	8.97E-08	1.459	300.0	2.72E-11	-0.0767
3.60	5.40	-1.50	3.04E-08	1.459	300.0	4.35E-11	-0.0792
3.60	1.80	-1.50	8.19E-09	1.459	300.0	2.62E-11	-0.0850
1.20	1.80	-1.50	2.42E-08	1.459	300.0	1.11E-11	-0.0859

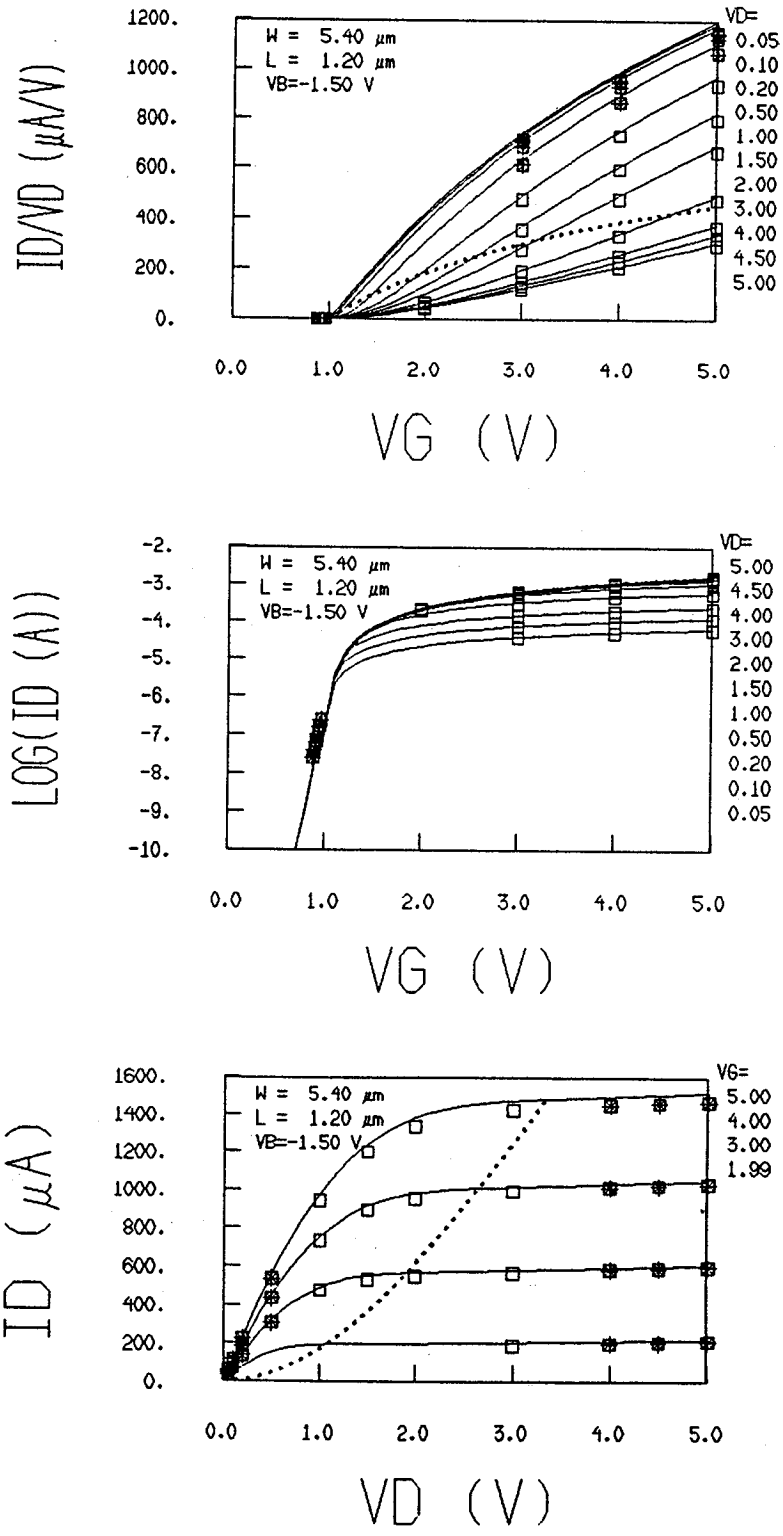

Figure 7.12: Characteristics of n-channel MOSFET with correlation $CC = 0.9990$ between model (curves) and data (points). Filled points used for parameter extraction. Emphasis on linear (top), subthreshold (middle) and saturation region (bottom).

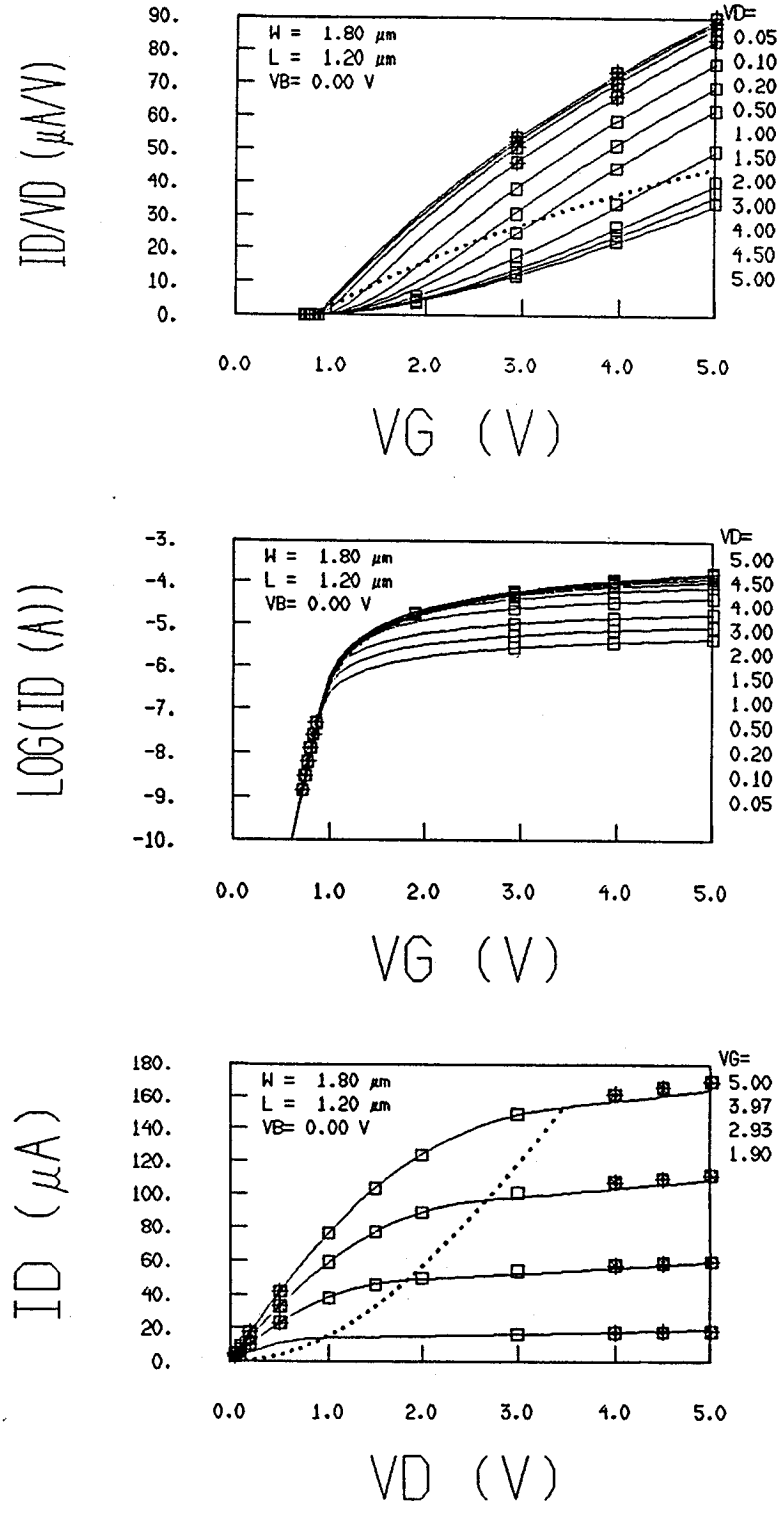

Figure 7.13: Characteristics of p-channel MOSFET with correlation $CC = 0.9994$ between model (curves) and data (points). Filled points used for parameter extraction. Emphasis on linear (top), subthreshold (middle) and saturation region (bottom).

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Chapter 8

Inverter

8.1. TEST MODULE: The CMOS/Bulk inverter is a 4-terminal structure fitting completely within a 2 x 2 pad array.

8.2. PURPOSE: To measure the first four parameters listed in Table 8.1 characterizing a three-piece linear approximation of an inverter transfer curve and to calculate a noise margin. As Fig. 8.1 shows, V_{OH} is the inverter output voltage V_O for nominal low input voltage, $V_I = 0$, and V_{OL} is the output voltage for a nominal high input voltage, $V_I = V_{DD}$. The point where output equals input voltage is called the inverter threshold voltage, V_{Tin}, and the magnitude of the slope of the transfer curve in that point is called the inverter gain G. The parameters extracted from the CMOS/Bulk Inverter are listed in Table 8.1.

Table 8.1: Parameters extracted from CMOS/Bulk Inverter

Parameter	Parameter Name
V_{OH}	Output voltage high
V_{OL}	Output voltage low
V_{Tinv}	Threshold voltage
G	Gain
V_{nm}	Noise margin

8.3. GEOMETRICAL DESCRIPTION/DESIGN PRINCIPLES: The layout of a p-well CMOS inverter is shown in Figure 8.2. It is recommended that the channel length of the n-MOSFET, L_n, equal the length of the p-MOSFET, L_p, and that the channel lengths be designed at the minimum rule. In addition, the channel

width of the p-MOSFET, W_p, should be 3/2 times the width of the n-MOSFET and that W_n be designed using the minimum rule. Thus, the conductance of the p- and n-MOSFETs will be approximately equal since the electron mobility is approximately 3/2 times larger than the hole mobility. The critical design parameters for the CMOS/Bulk Inverter are summarized in Table 8.2.

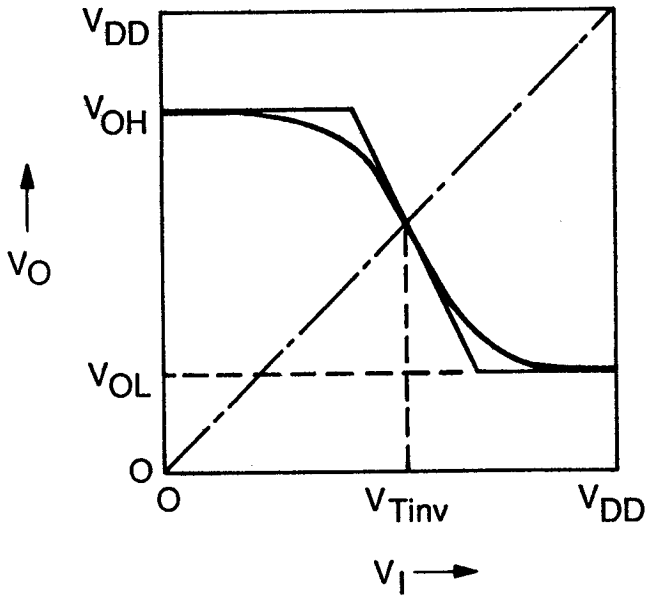

Figure 8.1: Inverter transfer curve and three-piece linear approximation.

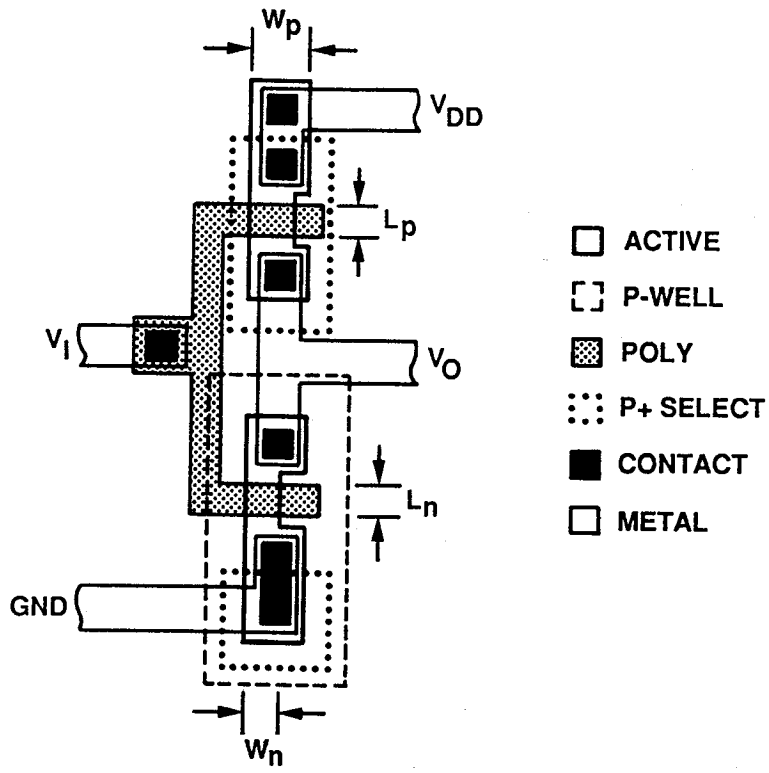

Figure 8.2: Layout of a p-well CMOS inverter.

Table 8.2: Critical design parameters for CMOS/Bulk Inverter

Parameter	Parameter Name	Value
L_n	n-channel length	Minimum
L_p	p-channel length	L_n
W_n	n-channel width	Minimum
W_p	p-channel width	$1.5W_n$

8.4. TEST PROCEDURE:

8.4.1. Output voltage high, V_{OH}, and output voltage low, V_{OL}:

8.4.1.1. Circuit diagram: See Figure 8.4. A supply voltage of $V_{DD} = 5$ V is connected to the VDD terminal. A voltage source is connected to the inverter input and set to V_I, and the inverter output voltage, V_O is measured with a voltmeter.

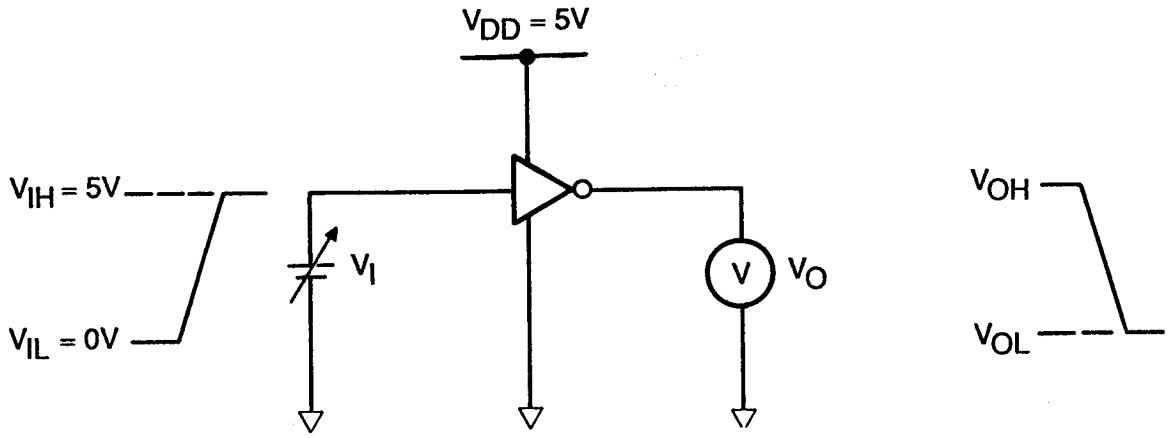

Figure 8.3: Inverter, V_{OH} and V_{OL}, measurement circuit.

8.4.1.1. Test conditions: The parameters V_{OH} and V_{OL} are the measured output voltages for $V_I = 0$ V and $V_I = V_{DD} = 5$ V, respectively.

8.4.2. Inverter threshold voltage, V_{Tinv}:

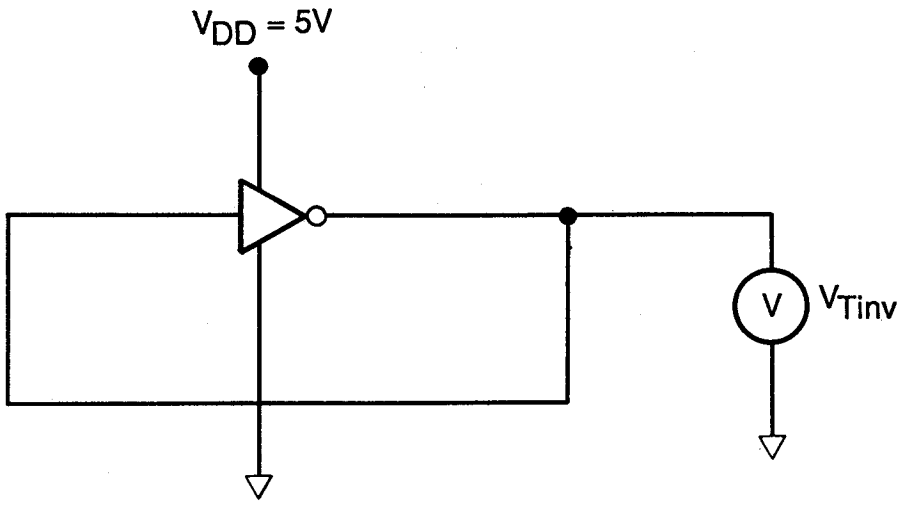

Figure 8.4: Inverter threshold voltage, V_{Tinv}, measurement circuit.

8.4.2.1. Circuit diagram: See Figure 8.4. The inverter input is connected externally to the inverter output and the output voltage measured.

8.4.2.2. Test conditions: The test is set up so that $V_O = V_{Tinv}$.

8.4.3. Inverter gain, G:

8.4.3.1. Circuit diagram: See Figure 8.5. Same circuit as for inverter output level measurement.

8.4.3.2. Test conditions: The inverter gain G is determined from a two-point method in which the inverter output voltage is measured at the inverter input voltages $V_{Tinv} + \Delta V$ and $V_{Tinv} - \Delta V$, where $\Delta V = 25$ mV.

Table 8.3: Test input/output parameters for CMOS/Bulk Inverter

Input Parameter	Output parameter
Output logic levels:	
$V_I = 0, V_{DD}$	$V_O = V_{OH}, V_{OL}$
Inverter threshold voltage:	
$V_I = V_O$	$V_O = V_{Tinv}$
Inverter gain:	
$V_I = V_{Tinv} \pm 25$ mV	$V_O = V_{Tinv} \pm G \times 25$ mV

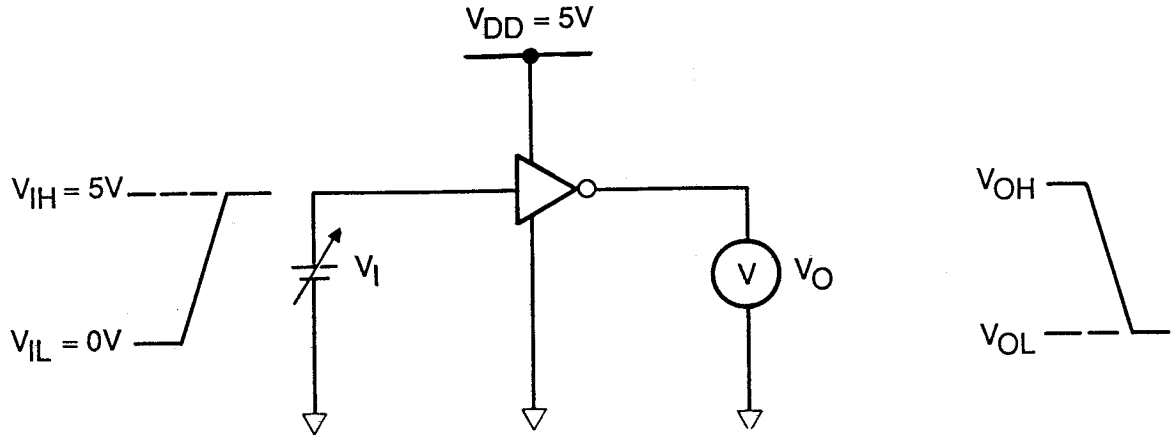

Figure 8.5: Inverter gain, G, measurement circuit.

8.4.3.3. Data reduction algorithm: The inverter gain is determined from:

$$G = \frac{V_O(V_I = V_{Tinv} - \Delta V) - V_O(V_I = V_{Tinv} + \Delta V)}{2\Delta V}. \tag{8.1}$$

8.4.4. Inverter noise margin V_{nm}:

8.4.4.1. Data reduction algorithm: The inverter noise margin is calculated from the inverter parameters described above using the so-called maximum square method [8.1]. This method implies that the noise margin V_{nm} is defined by that DC voltage increment which changes the output state of a long chain of inverters or that of a bistable latch when applied in an adverse sense to all inputs simultaneously. The method is illustrated in Figure 8.6 using the three-piece linear approximations of transfer curves. Two cases must be distinguished depending on the size of V_{Tinv}. Assuming $V_{OL} \approx 0$ and $V_{OH} \approx V_{DD}$, we obtain for the case when $V_{Tinv} \geq V_{DD}/2$,

$$V_{nm} \approx (1 - \frac{1}{G})(V_{DD} - V_{Tinv}), \tag{8.2}$$

and when $V_{Tinv} \leq V_{DD}/2$,

$$V_{nm} \approx (1 - \frac{1}{G})V_{Tinv}. \tag{8.3}$$

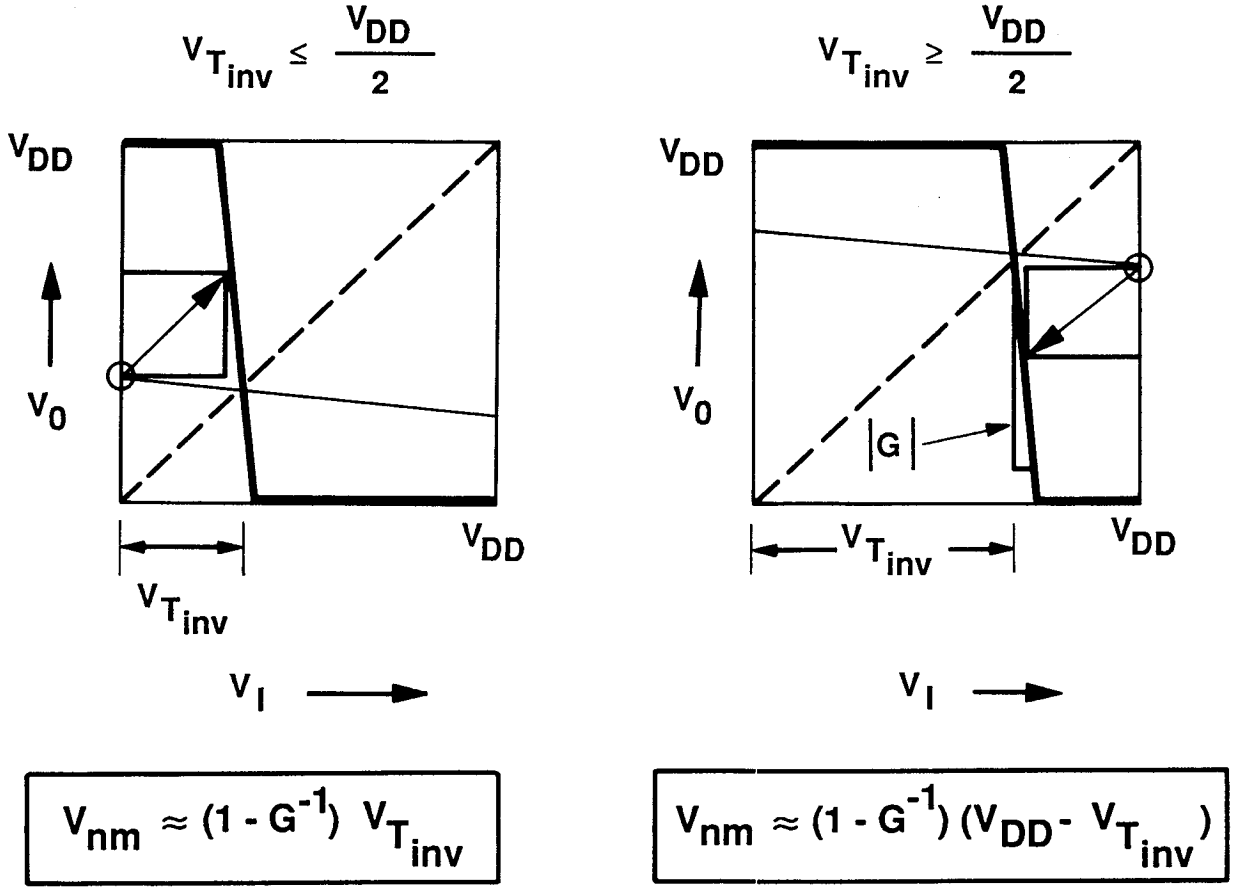

Figure 8.6: Inverter noise margin as derived from the maximum square method for two ranges of V_{Tinv}. The sides of the squares give the noise margins, V_{nm}.

8.5. TEST RESULTS: The logic levels V_{OL} and V_{OH} should be very close to 0 and $V_{DD} = 5$V. Deviations can be caused by bad contacts. For the designed transistor width ratio the threshold voltage, V_{Tinv}, should be close to $V_{DD}/2$. For the inverter gain, G, we have measured values between 10 and 20.

8.6. REFERENCES AND FURTHER READING:

8.1 C. F. Hill, "Noise margin and noise immunity in logic circuits," *Microelectronics (London)*, **1 (5)**, 16 (1968)

8.2 M. G. Buehler, and T. W. Griswold, "The Statistical Characterization of CMOS Inverters Using Noise Margins," *Electrochem. Soc. Extended Abs.*, **257**, 391-392 (1983)

8.3 M. G. Buehler and H. R. Sayah, "Addressable Inverter Matrix for Process and Device Characterization," *Solid State Technology*, **28, No. 5**, pp. 185-191 (1985)

Chapter 9

Ring Oscillator

9.1. TEST MODULE: Ring oscillator or other AC test structure.

9.2. PURPOSE: To evaluate inverter gate delay.

9.3. GEOMETRICAL DESCRIPTION/DESIGN PRINCIPLES: The specific geometrical description of this device is dependent upon the specific design rules and devices used. In Figure 9.1, the logic design of a typical ring oscillator is shown. However, to achieve accurate results, several design rules must be followed:

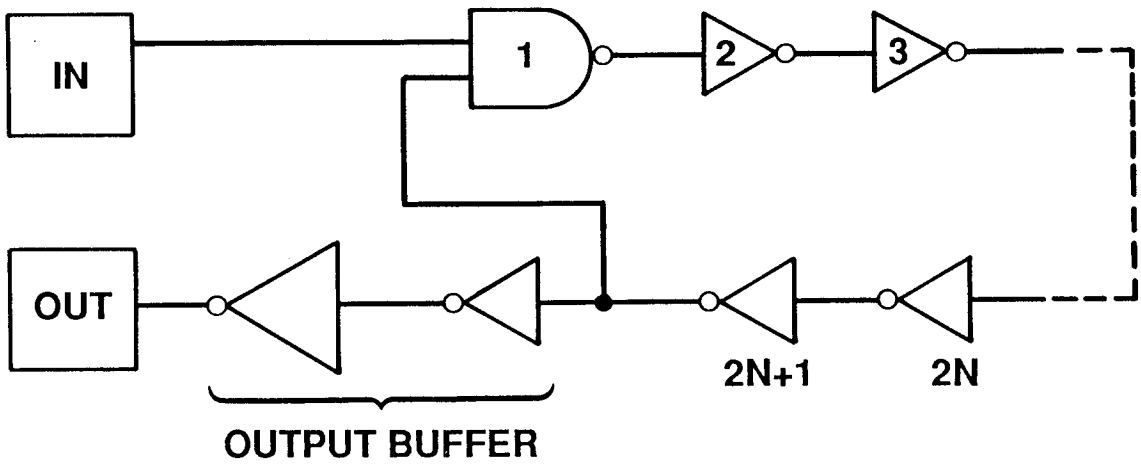

Figure 9.1: The ring oscillator, where N is an integer.

1. The number of stages in the oscillator must be an odd number (usually a prime number) that is large enough to allow each inverter to fully reach the high or low state after switching. If the output is not allowed to reach its final value before the input begins to change again, the ring oscillator will oscillate at abnormally high frequencies.
2. The output buffer inverter should be designed using minimum geometry transistors to add minimum capacitive load to the oscillator.
3. The output buffer should be provided with separate power and ground so the power drawn by the oscillator can be accurately measured.
4. The circuit should include a NAND gate trigger to allow control of the onset of oscillation, preventing the propagation of multiple pulses.

9.4. TEST PROCEDURE: The actual test procedure for this device is to be left to the discretion of the manufacturer.

9.5. FURTHER READING:

9.1 M. G. Buehler, "Microelectronic Test Chips for VLSI Electronics," in *VLSI Electronics: Microstructure Science*, **6**, Academic Press, 554-556 (1983)

9.2 C. Mead and L. Conway, *Introduction to VLSI Systems*, Addison-Wesley, Reading, Massachusetts, 235-236 (1980)

9.3 N. Sasaki, "Higher Harmonic Generation in CMOS/SOS Ring Oscillators," *IEEE Trans. Electron Devices*, **ED-29**, 280-283 (1982)

9.4 T. W. Houston, "Comments on Higher Harmonic Generation in CMOS/ SOS Ring Oscillators," *IEEE Trans. Electron Devices*, **ED-30**, 958-959 (1983)

Chapter 10

Timing Sampler

10.1. TEST MODULE: CMOS/Bulk timing sampler.

10.2. PURPOSE: To evaluate inverter pair propagation delay.

10.3. GEOMETRICAL DESCRIPTION/DESIGN PRINCIPLES: The timing sampler structure allows the direct measurement of the on-chip inverter propagation delay. The circuit schematic diagram of this structure is shown in Figure 10.1. This circuit consists of an inverter chain and two Muller C-element latches. The latches are connected to the inverter chain at the input and output of an inverter-pair (nodes b and b′). The critical design dimensions are the width and length of the MOSFETs in the inverters.

10.4. TEST PROCEDURE: Delays are measured for rising and falling step inputs. The latch connected to node b will trip when the step input signal, IN, reaches node b. The time of arrival of the signal at node b is determined by adjusting the step enable signal, EN, to coincide with the time of arrival of the IN signal at node b. The inverter-pair delay is determined by subtracting the signal arrival times measured at node b from that measured at node b′.

10.5. FURTHER READING:

10.1 B. R. Blaes, M. G. Buehler, and Y-S Lin, "Propagation Delay Measurements from a Timing Sampler Intended for use in Space", *IEEE Trans. Nucl. Sci.*, **NS-34**, 1470-1473 (1987)

10.2 B.R. Blaes and M.G. Buehler, "Inverter Propagation Delay Measurements Using Timing Sampler Circuits", *Proc. IEEE 1989 Int. Conf. Microelectronic Test Structures*, **2**, 227 (1989)

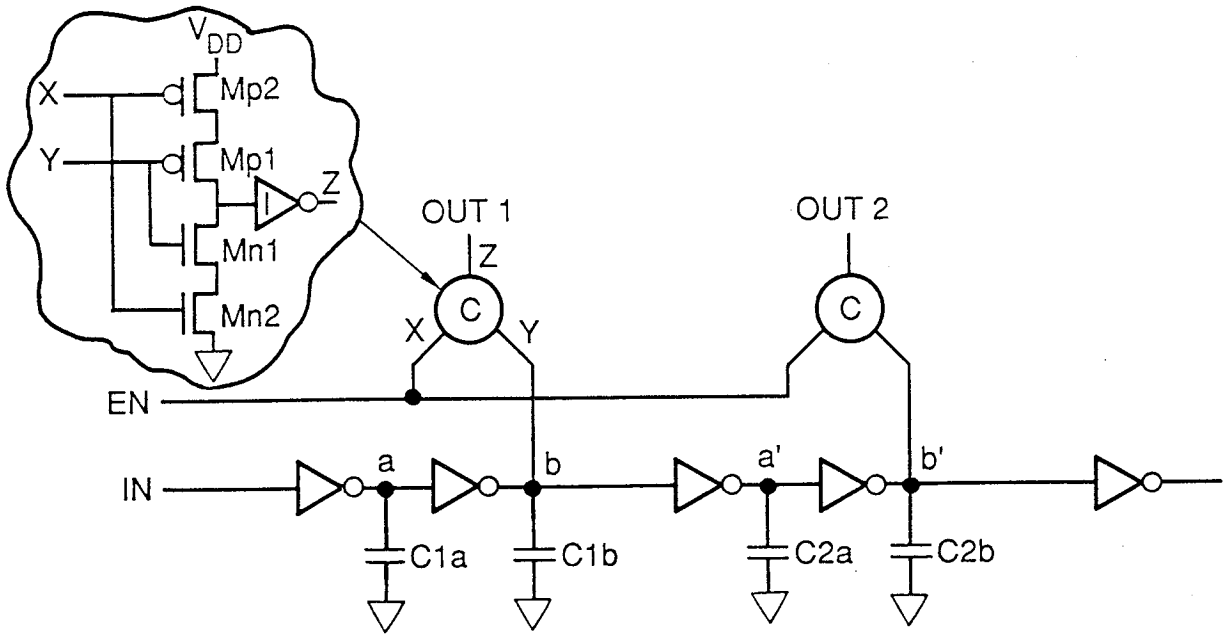

Figure 10.1: Circuit diagram of the timing sampler for measurement of inverter propagation delay.

Appendix A

Currently Used $2 \times N$ Probe Pad Arrays

Two probe-pad configurations used in the semiconductor industry are shown in this appendix. Probe Pad Arrays No. 1 and No. 2 are shown in Figures A1 and A2, respectively. Array 1 is bondable, array 2 is not; however, there is a significant space savings when this layout is used. The layout of the test strip using Probe Pad Array No. 1 is illustrated in Figure 1.1. The stacking box (indicated by the dashed lines) is used when butting multiple probe-pad-array blocks together to assure uniform pad spacing and test strip probe-ability. The bounding box, which defines the boundary of usable and unusable space, is indicated by the dotted lines. Features cannot be located outside the bounding box unless they extend beyond the end of the probe-pad contact area such as in the case of the area MOSFET and ring oscillator test structures illustrated in Figure 1.1.

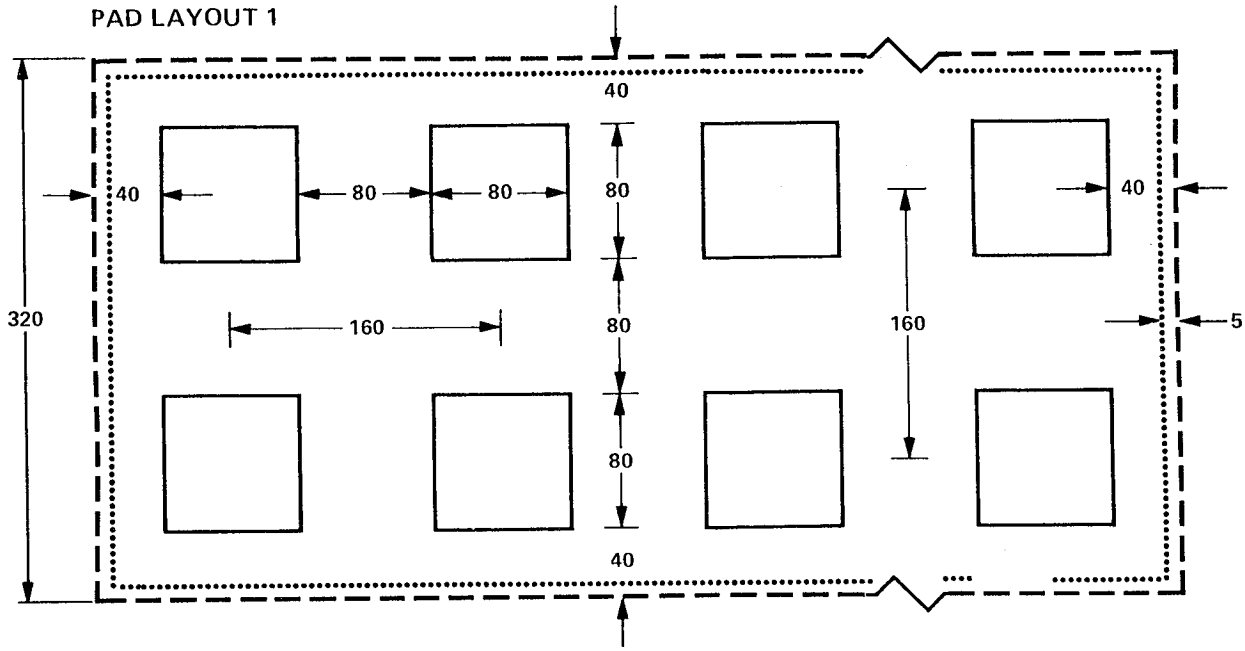

Figure A1: Probe-pad array No. 1.

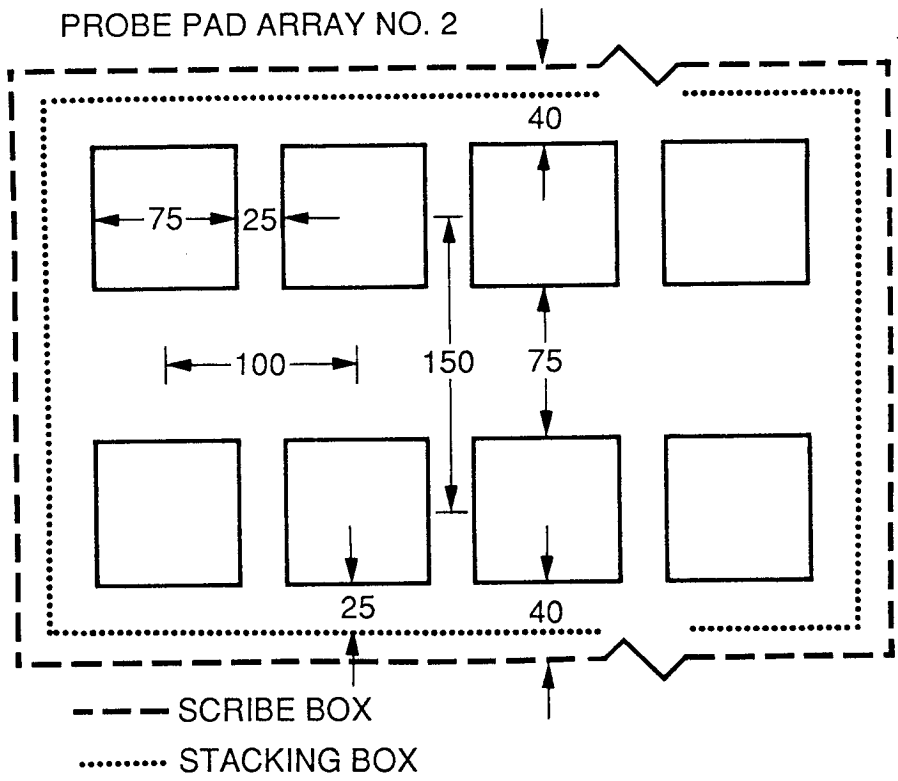

Figure A2: Probe-pad array No. 2.

Appendix B

Geometrical Design Rules

The notation for the rule set used to design the CMOS Process Monitor is listed in Table B1. The design rules are listed in Table B2. It is a modification of revision six of the MOSIS CMOS scalable rule set which is taken from the MOSIS CMOS-Bulk design rules, dated February, 1988. This is a double-metal single-poly enhancement MOSFET process which does not use split butting or buried contacts. The complete design rule set is available from MOSIS/ISI. The design rule set given here is for a 2μm process. All dimensions used in Table B2 are in micrometers. Table B3 is provided to define the process and CIF or CALMA GDS-2 layer names.

A personalized CMOS Process Monitor can be obtained by entering the data requested in Tables B2 and B3. A column has been left for the fabricator to insert the dimensions of his rules in Tables B2 and B3. The submission of your rule set dimensions and layer names to JPL will allow preparation of a personalized tape containing the CMOS Process Monitor. When providing your rule set, please give any additional information that is relevant to making a successful transition of the CMOS Process Monitor to you. That is, if there are additional rules that should be known, please list them.

Table B1: Geometrical Design Rule Notation.

Dimensions	Layer Names	Layer Modifiers
S = Space	W = Well	n = n-type
O = Overlap	A = Active	p = p-type
W = Width	P = Polysilicon	
L = Length	I = Select	
	C = Contact Cuts	
	M = Metal # 1	
	M2 = Metal # 2	
	V = Via	
	G = Glass	
	XT = MOSFET	

Table B2: Geometrical Design Rule Specification.

Layer Symbols	JPL Dimensions (μm)	Fabricator Dimensions (μm)	Symbol Description
L:nXT	= 2.0	_____	n-MOSFET minimum drawn channel length
W:nXT	= 3.0	_____	n-MOSFET minimum drawn channel width
L:pXT	= 2.0	_____	p-MOSFET minimum drawn channel length
W:pXT	= 3.0	_____	p-MOSFET minimum drawn channel width
S:WW	= 6.0	_____	Spacing Well to Well (same potential)
W:W	= 10.0	_____	Linewidth of Well
S:AA	= 3.0	_____	Spacing Active to Active
S:AW	= 5.0	_____	Spacing Active to Well Boundry
W:A	= 3.0	_____	Linewidth of Active
W:P	= 2.0	_____	Linewidth of Poly
S:PP	= 2.0	_____	Spacing Poly to Poly
S:PA	= 1.0	_____	Spacing Field Poly to Active
O:PA	= 2.0	_____	Overlap Poly over Active
O:IA	= 2.0	_____	Overlap Select beyond Active
W:I	= 2.0	_____	Linewidth of Select
S:II	= 2.0	_____	Spacing Select to Select
S:IA	= 2.0	_____	Spacing Select to Active
O:IA	= 2.0	_____	Overlap Select to Active
O:IXT	= 2.0	_____	Overlap Select to MOSFET Gate
W:C	= 2.0	_____	Width of Contact
S:CXT	= 2.0	_____	Spacing Contact to MOSFET Gate
O:M1C	= 1.0	_____	Overlap of Metal 1 to Contact
O:PC	= 1.0	_____	Overlap of Poly to Contact

continued

Table B2: Geometrical Design Rule Specification - continued.

Layer Symbols	JPL Dimensions (μm)	Fabricator Dimensions (μm)	Symbol Description
O:AC	= 1.0	_____	Overlap of Active to Contact
S:CC	= 2.0	_____	Spacing Contact to Contact
S:CA	= 3.0	_____	Spacing Contact to p-Active
W:V	= 2.0	_____	Width of Via
O:M1V	= 1.0	_____	Overlap 1st Metal beyond Via
O:M2V	= 1.0	_____	Overlap 2nd Metal beyond Via
W:M	= 3.0	_____	Width of 1st Metal
S:MM	= 3.0	_____	Spacing of Metal to Metal
W:M2	= 3.0	_____	Width of 2nd Metal
S:M2M2	= 4.0	_____	Spacing of 2nd Metal to 2nd Metal

* = p-Well or twin-well process only
** = n-Well or twin-well process only

Table B3: Process Definition and Layer Naming Conventions (MOSIS)

Process (check one):

___ p-Well ___ n-Well ___ twin Well

Contacts currently used in the Process Monitor:

The Process Monitor uses only three types of contacts. The Cuts layers specify contacts to Active and Poly from First Level Metal. Contacts from First to Second-Level Metal are called out by the Via layer. Direct contact from the Second-Level Metal to Active or Poly is assumed to be unsupported unless otherwise specified.

Layer Name	CIF	CALMA	Fabricator
P-Well	CWP	53	_____
N-Well	CWN	42	_____
Active	CAA	43	_____
Poly	CPG	46	_____
P-Select (P^+Implant)	CSP	44	_____
N-Select (N^+Implant)	CSN	45	_____
Contact Cut: Metal to Active	CCA	48	_____
Contact Cut: Metal to Poly	CCP	47	_____
Metal 1	CMF	49	_____
Metal 2	CMS	51	_____
Via	CVA	50	_____
Glass/Passivation	COG	52	_____
Other (_____)			_____
Other (_____)			_____
Other (_____)			_____

Note that each of these layers translates directly to the corresponding mask layer. No Boolean or sizing functions are used. If your software requires layers to be defined differently, please explain on a separate page.

Appendix C

Smoothed First and Second Derivatives

If we have a set of $N = 2m+1$ data points $(x_i, y_i), i = -m, ..., m$, with equidistant x_i, then the first and second derivatives about the center value, x_0, denoted $F^{(1)}$ and $F^{(2)}$, respectively, can be calculated by

$$F^{(1)} = \left.\frac{dy}{dx}\right|_{x_o} = \sum_{i=-m}^{m} \frac{C_{i1m} y_i}{M_{1m} \Delta x}$$

and

$$F^{(2)} = \left.\frac{d^2y}{dx^2}\right|_{x_o} = \sum_{i=-m}^{m} \frac{C_{i2m} y_i}{M_{2m} \Delta x^2},$$

where Δx is the increment between successive x_i values, C_{i1m} and C_{i2m} are the first and second derivative smoothing coefficients, and M_{1m} and M_{2m} are normalization factors. The smoothing coefficients and normalization factors for the first and second derivatives are listed in Tables C1 and C2, respectively. These coefficients were derived from least-squares fitting of a cubic polynomial to the data sets [C1], [C2].

REFERENCES

C1 A. Savitzky and H. J. E. Golay, "Smoothing and Differentiation of Data by Simplified Least Squares Procedures," *Analytical Chemistry*, **36**, 1627 (1964)

C2 J. Steinier, Y. Termonia, and J. Deltour, "Comments on Smoothing and Differentiation of Data by Simplified Least Square Procedure," *Analytical Chemistry*, **44**, 1906 (1972)

Table C1: Smoothing coefficients for calculating the first derivative at the central point of a set of data least-squares-fitted to a cubic polynomial.

N	13	11	9	7	5
m	6	5	4	3	2
M_{1m}	24024	5148	1188	252	12
C_{-61m}	1133				
C_{-51m}	-660	300			
C_{-41m}	-1578	-294	86		
C_{-31m}	-1796	-532	-142	22	
C_{-21m}	-1489	-503	-193	-67	1
C_{-11m}	-832	-296	-126	-58	-8
C_{-01m}	0	0	0	0	0
C_{11m}	832	296	126	58	8
C_{21m}	1489	503	193	67	-1
C_{31m}	1796	532	142	-22	
C_{41m}	1578	294	-86		
C_{51m}	660	-300			
C_{61m}	-1133				

Table C2: Smoothing coefficients for calculating the second derivative at the at the central point of a set of data least-squares-fitted to a cubic polynomial.

N	13	11	9	7	5
m	6	5	4	3	2
M_{2m}	1001	429	462	42	7
C_{-62m}	22				
C_{-52m}	11	15			
C_{-42m}	2	6	28		
C_{-32m}	-5	-1	7	5	
C_{-22m}	-10	-6	-8	0	2
C_{-12m}	-13	-9	-17	-3	-1
C_{02m}	-14	-10	-20	-4	-2
C_{12m}	-13	-9	-17	-3	-1
C_{22m}	-10	-6	-8	0	2
C_{32m}	-5	-1	7	5	
C_{42m}	2	6	28		
C_{52m}	11	15			
C_{61m}	22				