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NASA Technical Memorandum

NASA TM- 103569

BUGS SYSTEM CLOCK DISTRIBUTOR

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Science and Engineering Directorate

November 1991

National Aeronautics and
Space Administration

George C. Marshall Space Flight Center

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	November 1991	Technical Memorandum

4. TITLE AND SUBTITLE

BUGS System Clock Distributor

5. FUNDING NUMBERS

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

George C. Marshall Space Flight Center
Marshall Space Flight Center, AL 35812

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

National Aeronautics and Space Administration
Washington, D.C. 20546

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

NASA TM-103569

11. SUPPLEMENTARY NOTES

Prepared for Space Science Laboratory, Science & Engineering Directorate.
*Work performed while author was on Professional Intern Program.

12a. DISTRIBUTION / AVAILABILITY STATEMENT

Unclassified--Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

A printed circuit board which will provide external clocks and precisely measure the time at which events take place has been designed for the Bristol University Gas Spectrometer (BUGS). The board, which has been designed to interface both mechanically and electrically to the CAMAC system, has been named the BUGS system clock board. This document describes the board's design and how to use it.

14. SUBJECT TERMS

BUGS System Clock Distributor, Fiber Optic Transmitter, CAMAC System Interface, CAMAC, Cosmic Ray

15. NUMBER OF PAGES
15

16. PRICE CODE
NTIS

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	

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I. INTRODUCTION TO GENERAL OPERATION

The system clock board has been developed for the Bristol University Gas Spectrometer (BUGS). The board provides three services to the BUGS data system. First, it provides a clock to each of the eight inner PMT detectors. The inner detectors use the clocks to shift data into the sample FIFO. Second, the board measures the position within the 2 μs sample window where an event trigger occurs. To simplify terminology, this measurement will hereafter be referred to as the time-of-event. And finally, the board measures the elapsed time between events. Refer to Figure 1 for block diagram level description of the BUGS clock distributor.

II. DISTRIBUTION OF SYSTEM CLOCK

A. External Clocks

As mentioned previously, the BUGS system clock board provides eight external clock signals. The signals are generated by allowing an internal clock to drive fiber optic transmitters. The internal clock is generated by dividing the output of a 32-MHz TTL clock oscillator by 8, 4, and 2 which creates 4-, 8-, and 16-MHz clock signals, respectively. The system user has the option of selecting any of the three frequencies via the straps JP1 and JP2 (see Table 1). The system processor may determine the state of straps JP1 and JP2 by reading status register three (see section V.F). These clocks are then routed to a data selector. The output of the data selector is used as the input to a gating circuit which allows the BUGS system to start and stop the clock signals on command. The RUN command starts the clock on a rising edge. The external clocks will be stopped on the next falling edge immediately following the /STOP command. Both of these commands are simply low going pulses at least 50 ns wide. The BUGS system will transmit command pulses to the system clock board via coax connectors provided on its front panel. Finally, the outputs of the gating circuit are sent to eight

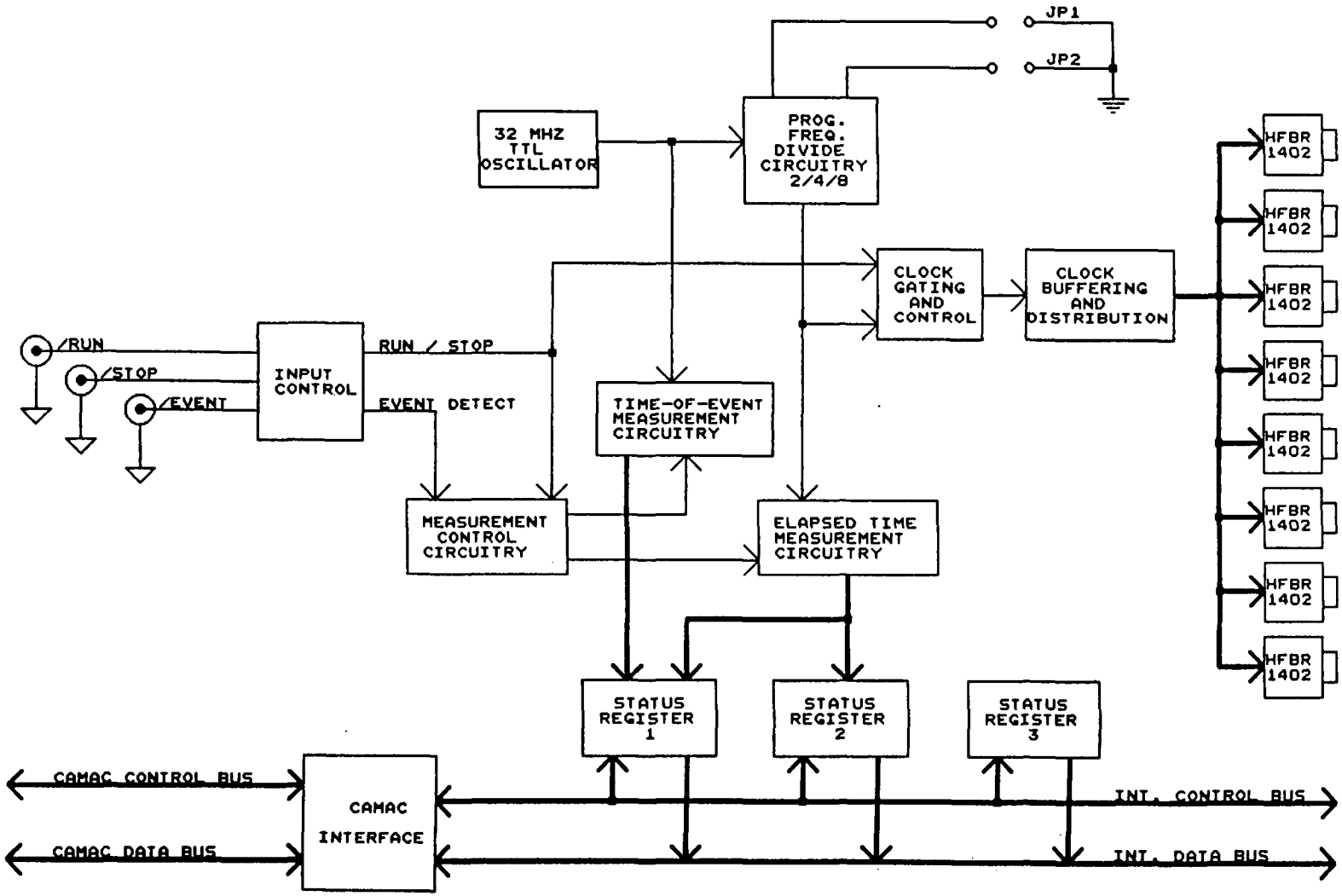

Figure 1. BUGS Clock Distributor Block Diagram.

distinct fiber optic driver circuits. The drivers have been designed for Hewlett Packard HFBR-1402 fiber optic transmitters. The transmitters have built-in SMA type connectors and are located on the front panel of the board.

Table 1. Clock Frequency Straps

JP2	JP1	EXT./INT. CLOCK (MHz)
0	0	4
0	1	8
1	0	16
1	1	0

Note: As described in the above table, the presence of a strap is equivalent to a "0," and the absence of a strap is equivalent to a "1."

B. Internal Clocks

There are two internal clocks on the system clock board which synchronize its functions. One of the clocks, INTCLK1, is fixed at 32 MegaHertz, and the other, INTCLK2, is variable. The rising edges of INTCLK1 and INTCLK2 coincide. Both INTCLK2 and the eight external clocks are derived from the same output of the data selector mentioned in the previous section. Therefore, the external clocks and INTCLK2 operate at the same frequency. Also, the rising edges of the external clocks are synchronized with the rising edge of INTCLK2. The internal clocks will not stop when the /STOP command has been received. As is the case for the external clocks, straps JP1 and JP2 determine the frequency of INTCLK2 (see Table 1). It should be noted that as INTCLK2 changes, the sample window changes as shown in Table 2.

Table 2. Sample Window Versus Clock Frequency

INTCLK2 (MHz)	Sample Window (μs)
4	4
8	2
16	1

III. TIME-OF-EVENT MEASUREMENT

The time-of-event circuitry measures the time at which an event takes place with respect to the beginning of a sample window.

The circuit is designed around two, 4-bit counters. The counters add up the number of periods of the two internal clocks, INTCLK1 and INTCLK2, that have elapsed since the beginning of the sample window. At the beginning of each new sample window (every 2 μs, if an 8 MHz internal clock is chosen), the count rolls over to zero (refer to Figure 2).

When an event trigger has taken place, the counters are commanded to stop. (This does not stop the external clocks.) The BUGS system must send this command signal which will be called /EVENT for convenience. Like the /RUN and /STOP commands, the /EVENT command should be a low going pulse at least 50 ns wide. There is a coax connector provided on the front of the clock board for its physical connection.

Approximately 1 μs after each /EVENT command is received, the outputs of the two counters are latched into status register one. The upper byte of this register holds the measurement. Within this byte, the upper nibble represents the number of INTCLK2 periods that have elapsed, and the lower nibble represents the number of INCLK1 or 32-MHz periods that have elapsed (see section V.D for a further description of status register one). When the data in register one are ready, the clock board will issue a signal to the BUGS system. (This signal will be discussed further in section V.B.) This information will be lost if not read before the next /RUN command is received.

Three separate equations, each based on the possible frequencies of INTCLK2, are required to convert this binary number to the time-of-event. The calculation is made using equation one, two, or three when INTCLK2 is 16, 8, or 4 MHz, respectively.

$$t = [\ MSN * 62.5\ ] + [\ LSN * 31.25\ ]\ ns \qquad (1)$$

MSN is the number represented by bits 12 through 15 of status register one, and LSN is the number represented by bit 8. Bits 11, 10, and 9 may be ignored in this calculation.

$$t = [\ MSN * 125\ ] + [\ LSN * 31.25\ ]\ ns \qquad (2)$$

MSN is the same in equation (2) as it is in equation (1). LSN is the number represented by bits 8 and 9. Bits 11 and 10 may be ignored.

$$t = [\ MSN * 250\ ] + [\ LSN * 31.25\ ]\ ns \qquad (3)$$

MSN is the same as it was in equations (1) and (2). LSN is the number represented by bits 8, 9, and 10. Bit 11 may be ignored.

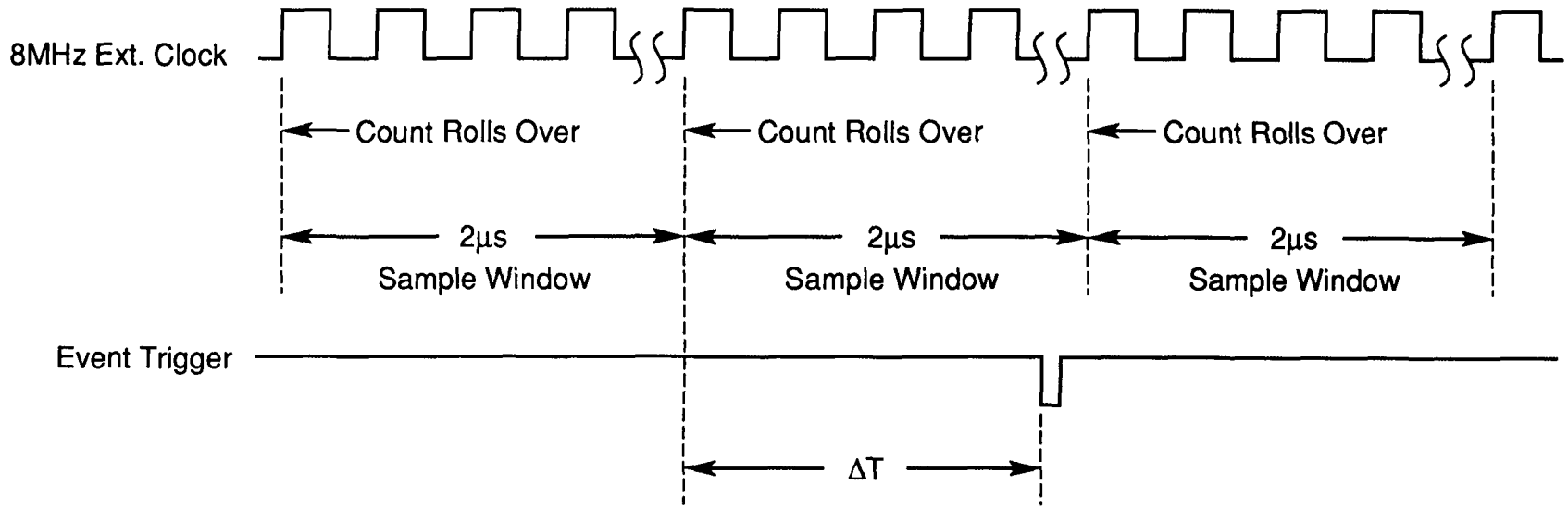

Figure 2. Timing Diagram for Time-of-Event Measurement

A typical sequence of events, shown in Figure 3, would be as follows:

1. The clock board receives a /RUN command.
2. On the falling edge of /RUN, the counters are cleared.
3. One INTCLK2 period after being cleared, the counters are enabled and begin counting.
4. The counters continue counting, rolling over each new sample window, until an /EVENT command is received.
5. One microsecond after /EVENT, the time-of-event data ready in status register one.
6. To start the sequence over, the clock board MUST receive the /STOP command before the next /RUN command has been received.

IV. TIME BETWEEN EVENT MEASUREMENT

The time between event circuitry measures the elapsed time between two consecutive events (see Figure 4). The circuit has been designed by combining six, 4-bit counters into a 24-bit counter. The counters are driven by the INTCLK2 internal clock and will roll over every 1, 2, or 4 seconds if the frequency of INTCLK2 is 16, 8, or 4 MHz, respectively. After reset, the counters are not enabled until the first event has been detected. The system processor may read status register three to determine whether the first event has been detected (see section V.B).

On the falling edge of the /EVENT command, the counters are disabled for 1 µs. During this time, the 24-bit word created by the counters is latched into status registers one and two. The most significant byte of this word is contained in the lower byte of status register one. The two least significant bytes of the 24-bit word are in status register two. (For further details on status register one and two, refer to sections V.D and V.E.) After the data have been latched, the counters are cleared and then re-enabled. Again, the system clock board issues a signal which indicates that this information is ready. The data will be lost if it has not been read before the next event takes place.

Conversion of the 24-bit word to the time between events depends on the frequency of INTCLK2. The number (base 10) should be multiplied by 62.5, 125, or 250 ns if INTCLK2 is selected to be 16, 8, or 4 MHz, respectively. Also, 1 µs should be added to this number to account for the time during which the counters have been disabled.

V. SYSTEM INTERFACE

The system clock board has been designed to interface both mechanically and electrically with the CAMAC system. Its major features are described in the following sections.

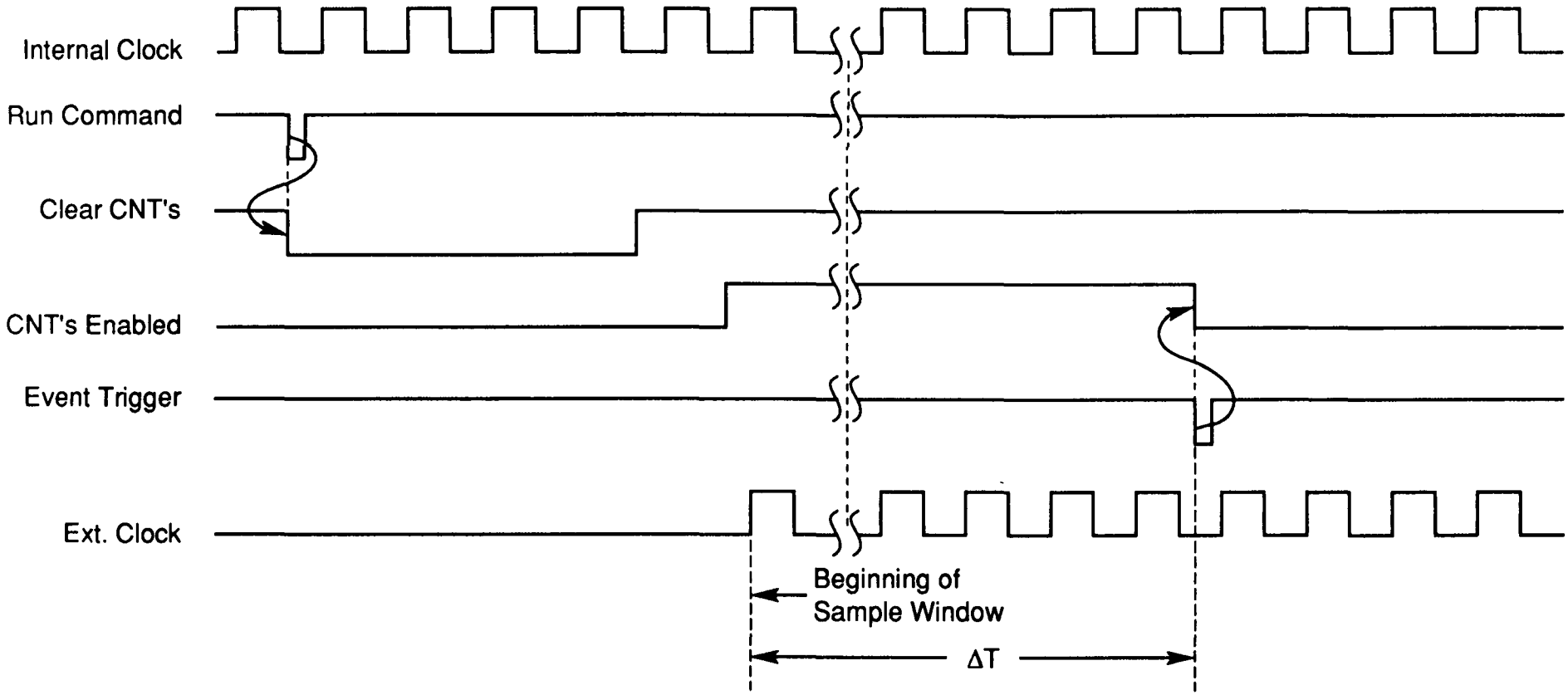

Figure 3. Timing Diagram for Typical Sequence of Operation

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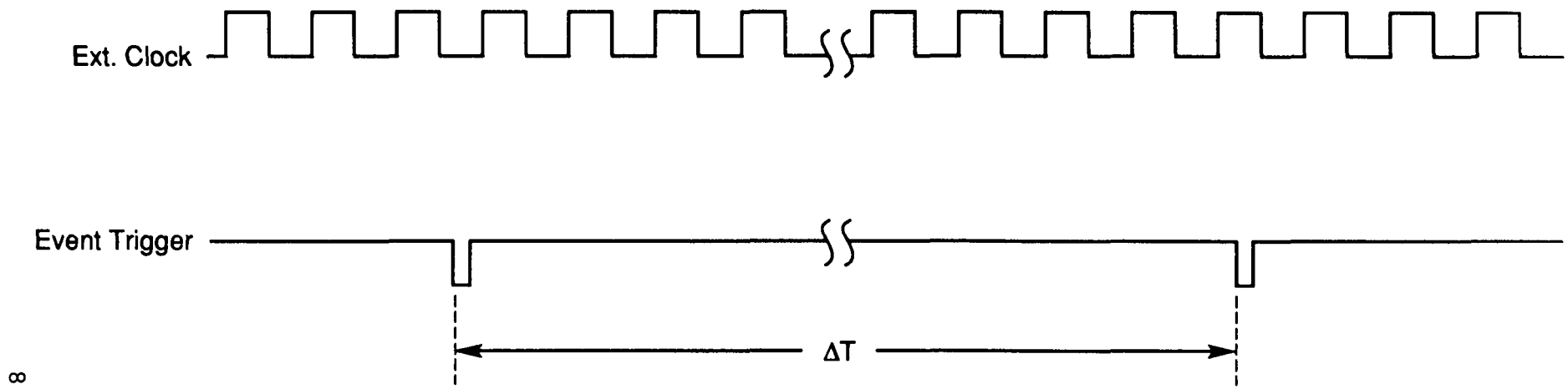

ΔT = Time Between Events Measurement

Figure 4. Timing Diagram for Time Between Events Measurement

A. CAMAC Command Decoding

The system clock board supports eight CAMAC commands. The commands are decoded based on the combination of their function code and subaddress. Table 3 lists the commands and gives a brief description of them.

Table 3. CAMAC Commands

Command	Function
F0A0	Read Status Register One
F0A1	Read Status Register Two
F0A2	Read Status Register Three
F8A15	Test Look-At-Me
F9A15	Board Reset
F10A0	Clear Look-At-Me
F24A0	Disable Look-At-Me
F26A0	Enable Look-At-Me

B. Look-At-Me Status Signal

One microsecond after every event, the system clock board generates a "look-at-me" signal. The "look-at-me" or LAM indicates that the measurements stored in status registers one and two can be read. Once the system clock board asserts the LAM, the LAM will remain active until the system processor clears it, and there are three ways to clear the LAM. First, any time status register one or two is read, the LAM is automatically cleared. Second, the clear look-at-me command can be used. Third, the system clock board can be reset.

The LAM signal may be prevented from leaving the system clock board via a programmable mask. In other words, the system clock board may generate a LAM, but the mask may prevent the system clock board from asserting the signal onto the control bus. The reset or the disable look-at-me command, F24A0, will turn the mask on. The enable look-at-me command, F26A0, will turn the mask off or enable the LAM signal.

The state of both the LAM and the LAM mask may be determined at any time by reading status register three. Bit zero contains the LAM and bit 1 contains the LAM mask. Therefore, even if the LAM signal has been masked, the system processor is still capable of determining its state.

Also, the logical AND combination of the LAM and the LAM mask may be tested using the test look-at-me command.

C. Status Registers

The status registers may be read via the CAMAC interface by using the function code F0. The individual registers are distinguished by their subaddress. The subaddress for status registers one, two, and three are A0, A1, and A2, respectively.

D. Status Register 1

READ COMMAND = F0A0

BITS		BITS	
15	INTCLK2(3)	7	EVTCNT(23)
14	INTCLK2(2)	6	EVTCNT(22)
13	INTCLK2(1)	5	EVTCNT(21)
12	INTCLK2(0)	4	EVTCNT(20)
11	NOT USED	3	EVTCNT(19)
10	INTCLK1(2)	2	EVTCNT(18)
9	INTCLK1(1)	1	EVTCNT(17)
8	INTCLK1(0)	0	EVTCNT(16)

The most significant byte of status register one holds the time-of-event measurement. Bits 12 through 15 represent the number of INTCLK2 periods that have elapsed. Bit 11 is not used. Its value will always be zero. Bits 8 through 10 represent the number of INTCLK1, 32 MHz, periods that have elapsed.

The lower byte of status register one holds the most significant byte of the 24-bit word that represents the elapsed time between events.

E. Status Register 2

READ COMMAND = F0A1

BITS		BITS	
15	EVTCNT(15)	7	EVTCNT(7)
14	EVTCNT(14)	6	EVTCNT(6)
13	EVTCNT(13)	5	EVTCNT(5)
12	EVTCNT(12)	4	EVTCNT(4)
11	EVTCNT(11)	3	EVTCNT(3)
10	EVTCNT(10)	2	EVTCNT(2)
9	EVTCNT(9)	1	EVTCNT(1)
8	EVTCNT(8)	0	EVTCNT(0)

Status register two holds the least two significant bytes of the 24-bit word that represents the elapsed time between events.

F. Status Register 3

READ COMMAND = F0A2

BITS

7	Not Used
6	Not Used
5	Not Used
4	1 = First Event Detected; 0 = No Events Detected
3	STRAP JP2 (see Table 1)
2	STRAP JP1 (see Table 1)
1	1 = LAM Enabled; 0 = LAM Disabled ("Masked")
0	LOOK-AT-ME

G. Reset

There are two ways to reset the system clock board through the CAMAC interface. The system processor may either use the reset command, F9A15, or the initialize signal, Z, may be asserted.

H. Response and Command Accepted

In response to each command that it recognizes, the system clock board generates the response, Q, and the command accepted, x, signals.

VI. TECHNOLOGY

The system clock board has been designed using TTL technology integrated circuits. However, if the need arises, all components on this board may be replaced with CMOS equivalents.

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APPROVAL

BUGS SYSTEM CLOCK DISTRIBUTOR

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The information in this report has been reviewed for technical content. Review of any information concerning Department of Defense or nuclear energy activities or programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

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