RECOMMENDATIONS

Degradation Implementation

The ACI spectra, as documented in the previous section, clearly show third order intermodulation between the two adjacent channels. The intermodulation is low enough in level that measurement of the adjacent channel power is still accurate, but the internal spectral spreading of each seems to be significant and the use of amplifiers with higher third order intercept points is recommended.

Another difficulty is the requirement of an HPA Output Filter to compensate for regrowth of the sidelobes. The system design showed good results but was unrealistic because ideal equalization of the filter's group delay was assumed. Reasonable filters of this bandwidth can be built at 3 GHz, but become much more difficult in real world systems which would likely run at 20/30 GHz.

Decoder Implementation

Although the actual power consumption of the decoder is about 60% of the originally predicted worst case, it still is 3/4 of the total power consumption. It could be reduced in the engineering model phase of development by using gate arrays or custom ICs for some portions of the decoder. The add/compare/select function of the state metric calculator has already been hybridized to reduce interconnect delays. Future refinement of the processing algorithms for hardware simplification could also be investigated.

Coarse AGC Design

An improvement to the design of the coarse AGC may be obtained by implementing it entirely after the downconversion instead of at the higher IF. One advantage is that it would use all low frequency components which are more readily available. The phase margin of the closed loop would also be increased because the logamp in the feedback loop would be tied directly to the AGC output instead of after a path delay. The logamp is used to linearize the control loop response of the pin diode attenuator and is much easier to obtain at the lower frequency. Finally, the input bandpass filter could be eliminated, although high level adjacent channels may cause third order intermodulation in the input amplifier and downconverting mixer.

The coarse AGC is presently implemented as an analog, closed-loop control system which impacts the system acquisition time with a settling speed of approximately 360ns (=72 information bit times). The carrier acquisition time is twice the specified preamble length of 100 bit times and the carrier recovery circuitry is somewhat level sensitive, so in the worst case the total acquisition time is 192 + 72 = 264 information bit times. This could only be marginally improved with state of the art components in the AGC, so alternate topologies are recommended for future design efforts. The carrier recovery circuitry could be designed for insensitivity to the 20dB dynamic range of the QAM signal. The AGC could also be significantly sped up by implementing it as an open loop compensator which could use a fast detector and digitizer to drive a digitally controlled attenuator.

Nyquist Filters

The Nyquist filters significantly degrade BER performance due to ISI. The performance section shows the amount of ISI from the filters in the eye pattern figures, and that a major source of the problem is group delay ripple. The BER degradation of the entire system will be limited by the filters, so the BER degradation specification of 2 dB cannot be met with the present filters. Bandwidth efficiency restrictions on this system require the use of Nyquist filters, so specification and implementation of them will be an important part of any future work.

Ringing Filters

The spurious response of the present crystal filters can be expected to affect the phase error of the recovered carrier and clock. The frequency plan of the Demodulator could be redone to change the percent bandwidth of the carrier recovery filter, which might allow operation of the crystals without forcing a response which results in spurs. This cannot be done for the clock recovery where the frequency is determined by the symbol rate, so alternate filter implementations should be investigated for both cases.

Signal Path Filters

Several narrowband filters exist in the QAM signal path which are expected to affect the BER performance of the system by introducing intersymbol interference (ISI) distortion through group delay ripple. The BER simulations in the initial system study include the effects of an HPA output filter, but the implemented Demodulator has two additional filters. One is at the input to minimize the effect of the adjacent channels on the coarse AGC and its high-gain RF amplifier. The second is after the downconversion to eliminate the mixing spurs. With the use of "better" Nyquist filters, it may be necessary to more tightly specify these filters. The possibility of removing the second filter from the signal path and only inserting it directly before level detecting circuits should also be investigated.

Component Selection

Wideband track/hold (T/H) amplifiers are presently used three times in the Demodulator. The purpose is to "lock in" various control voltages at UW detection to avoid fluctuations due to envelope variations of the QAM signal during the data portion of the burst. The problem with using T/H Amps is their inherent pedestal offset and droop rate. The sensitivity of the system's BER performance to these parameters has not yet been determined, but is expected to be a minor problem. Future designs may need to use improved T/H amps or use feedforward digital control.

Wideband opamps are used at thirteen spots in the Demodulator. Seven of them dissipate a lot of power (900mW) but were used because of their performance characteristics. New opamps are now available which would improve performance in five locations, require fewer external components, and dissipate less than 150 mW each.

The Gating Processor and the UW Detector in the Demodulator are presently implemented using 100K ECL and dissipate about 6.6 Watts. The power consumption of the system as well as size could be reduced by using ECL (or possibly high speed TTL or CMOS) programmable logic for these two functions.

MIMIC/Commercial Components

Several companies, including TRW, are presently developing millimeter-wave microwave integrated circuit (MIMIC) technology which will provide attractive opportunities to reduce the size of the RF portions of the modem/codec system. As one example, TRW is developing HBT technology which has definite size and unit cost advantages because the transistor structure supports high yields and high integration density. Switches, amplifiers, mixers, and logamps are under current development, and more advanced functions such as digital attenuators, I/Q detectors, and linear mixers could be expected in the future.

RECOMMENDATIONS (continued)

Summary

Object	Change	Improvement
Degradation Implementation	Amplifier IP3, HPA filter	Measurement accuracy
Decoder Implementation	Use more gate array technology	Power dissipation
Coarse AGC Design	Settling time	Acquisition speed (preamble Length)
	Topology	Material cost, complexity
Nyquist Filters	Tighter specifications	BER performance
Ringing Filters	Spur-free	Acquisition speed, BER performance
Signal Path Filters	Specs and system topology	BER performance
Component Selection	New components	Performance, space and power
	Use programmable logic	Size and power
	Use MIMIC where possible	Size and cost

CONCLUSION

In order to achieve 2 bit/s/Hz bandwidth efficiency along with implementation simplicity and power efficiency for the Uplink, a modulation/coding format of 4x4 QAM with rate 3/4 FEC coding was chosen. The special test equipment is very near completion with only a few performance discrepancies that need to be resolved. The demodulator portion is at the beginning of the integration phase so complete performance results are not yet available. The 8-state Viterbi decoder portion of the POC system is completed and performs very well with a worst case BER degradation of 0.2 dB from theory. It is known, however, that several major sources of degradation in BER performance and acquisition time exist and that power consumption for the POC system is high. The actual performance of the system and the individual impact of each portion of the system will be available at the conclusion of the program.

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TRW, Redondo Beach, California
Russell Kam - Breadboard Development
Keith K. Yamashiro - Quenching Analysis

REFERENCES

Feher, K. Digital Communications: Satellite/Earth Station Engineering. Prentice-Hall, Englewood Cliffs, New Jersey, 1983. p. 155.

Gardner, Floyd M., Carrier and Clock Synchronization for TDMA Digital Communications. European Space Agency, Paris, France. December 1976. pp. 19-28.

Nyquist, H. "Certain Topics in Telegraph Transmission Theory," Trans. AIEE, Volume 47, 1928.

Rhodes, S. A. "Effects of Hardlimiting of Bandlimited Transmissions with Conventional and Offset QPSK Modulation," IEEE Telecommunications Conference Record. Houston, Texas, 1972. pp. 20-F-1 to 20-F-7.

AN 8-PSK TDMA UPLINK MODULATION AND CODING SYSTEM

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ABBREVIATIONS USED IN BRIEFING

• ACI	adjacent channel interference
• ADC	analog to digital converter
• AMTD	Advanced Modulation Technology Development
• ASIC	application specific integrated circuit
• AWGN	additive white Gaussian noise
• BER	bit error rate
• CCI	co-channel interference
• codec	coder/decoder
• DAC also D/A	digital to analog converter
• DBT	detected baud transitions
• ECL	emitter coupled logic
• LUT	lookup table
• MCD	multi-channel demultiplexer and demodulator
• MMIC	monolithic microwave integrated circuit
• modem	modulator/demodulator
• PCB	printed circuit board
• POC	proof-of-concept
• SAW	surface acoustic wave
• SBW	sub-burst window
• TDMA	time division multiple access
• UW	unique word

OVERVIEW

- OBJECTIVES
- PHASES
- REQUIREMENTS
- PROOF-OF-CONCEPT MODEL BLOCK DIAGRAM
- PROOF-OF-CONCEPT MODEL PHYSICAL CONFIG.
- PERFORMANCE OF POC MODEL
- CONCLUSIONS OF PROGRAM
- RECOMMENDATIONS FOR FUTURE

OBJECTIVES AND PHASES

OBJECTIVES:

- Develop a proof-of-concept uplink modulation system which will significantly increase the bandwidth efficiency of a TDMA uplink system
- Maintain present performance levels (i.e., QPSK power and bandwidth efficiencies)
- POC model should exhibit potential for low weight and power consumption

PHASES:

- Refine preliminary design
- Develop preliminary design
- Build and test breadboard
- Plan, specify, and fab POC model
- Test POC model and establish POC
- Product assurance

REQUIREMENTS

SALIENT REQUIREMENTS FROM RFP:

- **Bandwidth Efficiency > 2 bits/ sec/ Hz**
- **Implementation loss < 2 dB**
- **1 dB degradation in 20 db ACI or CCI**
- **TDMA burst mode with preamble < 100 bit periods**
- **Throughput > 200 Mbps**

DERIVED REQUIREMENTS:

- **8PSK modulation**
- **Nyquist filter with rolloff factor of 0.2**
- **CCI spec requires forward error correction coding**
- **Mostly digital mechanization for eventual ASIC design**

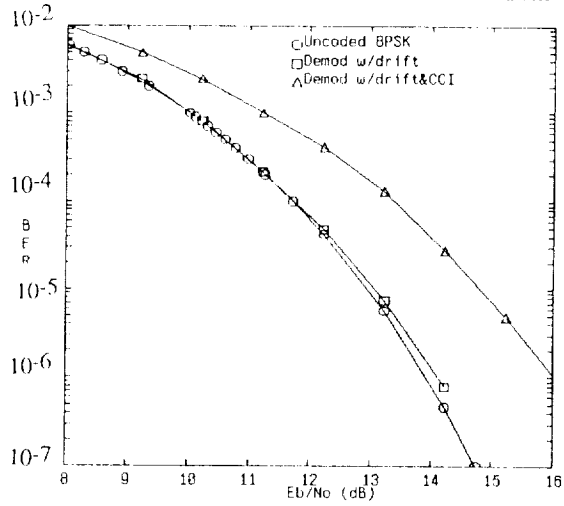
The combination of 8PSK modulation and >2 bits/sec/Hz drove the design of the Nyquist filter to one specified to have a rolloff factor of 0.2. This filter when built and tested was found to produce too much intersymbol interference and was abandoned for a design with rolloff factor of 0.4.

Preamble is limited to 100 bit periods of the uncoded bit period of 5 ns for a maximum preamble length of 500 ns or 40 8PSK symbol times at 12.5 ns per symbol.

For 8PSK modulation, the required maximum degradation of 1 dB in -20 dB CCI drove the requirement for forward error correction coding. In this contract, the funding was not sufficient to develop the proposed codec so the codec was limited to a paper design during the preliminary design phase.

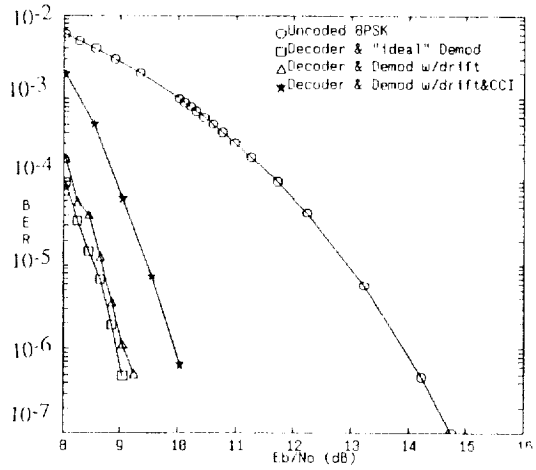
The mechanization of the demodulator is digital starting from the output of the ADCs which quantize the outputs of the quadrature phase detectors. This approach is amenable to an ASIC replacement in the next phase of development.

SIMULATIONS OF DEMOD PERFORMANCE WITH DRIFT AND CCI



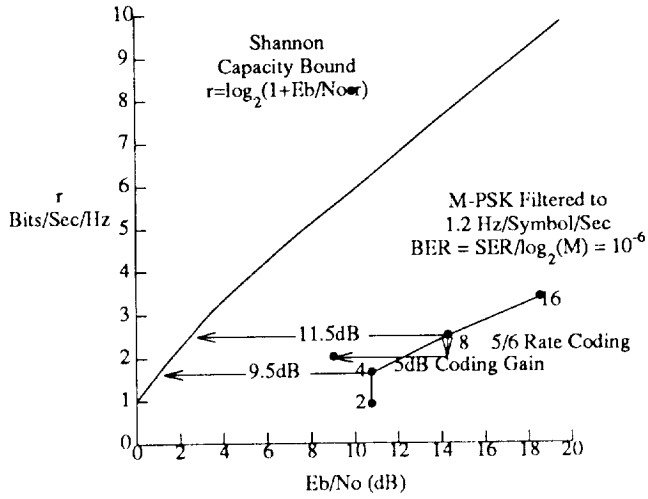
At BER equal to 5 E-7, degradation from theoretical for -20 dB CCI is seen to be about 2 dB. This drove the requirement for forward error correction coding.

SIMULATIONS OF DEMOD AND DECODER PERFORMANCE WITH DRIFT AND CCI



The simulated codec (to be shown in some detail below) produces 5 dB improvement in AWGN and, in the presence of CCI, the degradation is only 1 dB.

BANDWIDTH AND POWER EFFICIENCIES OF MODULATION SYSTEMS



Note that with coding, 8PSK system is both more power and bandwidth efficient than uncoded QPSK which satisfies the requirement for both bandwidth efficiency and to "maintain present performance levels".

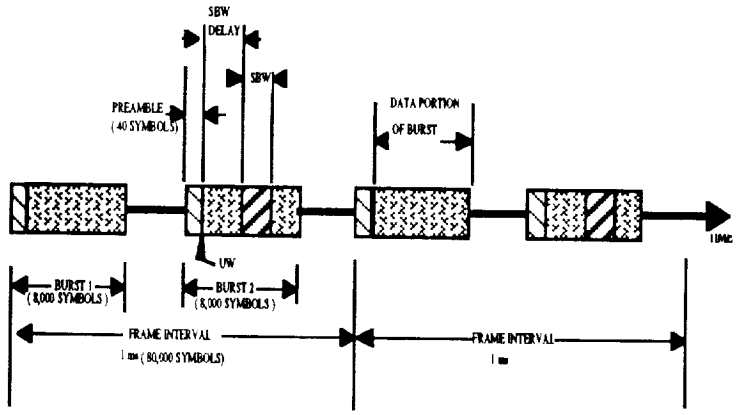
r=capacity/occupied bandwidth

16 QAM and 16PSK were both considered but were rejected as requiring a more complex modem.

SPECIFICATIONS OF POC MODEL

PARAMETER	VALUE	TEST SPEC NO OR METHOD OF DETERMINING COMPLIANCE
Bandwidth Efficiency	> 2 bits/sec/Hz	T
Bit Rate	240 Mbps	by design
Channel Spacing	96 MHz	by design
Transmission Mode	TDMA	by design
Frame Length	1 ms	by design
Preamble (CW portion) (UW portion)	32 symbols 8 symbols	by design
Receive Frequency	3.323656 GHz±1.5KHz	by design
Input level at receiver filter	-80 dBm±10 dB	by design
BER at Eb/No=21 dB	< 5×10^{-7}	T
Degradation Due to +20 dB ACI	< 1dB	S
Degradation Due to -20 dB CCI	< 1dB	S
Probability of bit error due to missing unique word	< 1×10^{-3} at Eb/No = 6 dB	by computation & T
Probability of Carrier Cycle Slip	< 1E6D at Eb/No= 10.6 dB	S
Bit-timing Jitter	< 125 ps RMS	S
Probability of Clock Cycle Slip	< 1E6 at Eb/No =10.6 dB	T
Minimum Guard Time Between Bursts		25 ns by design of STE

PREAMBLE AND BURST STRUCTURE

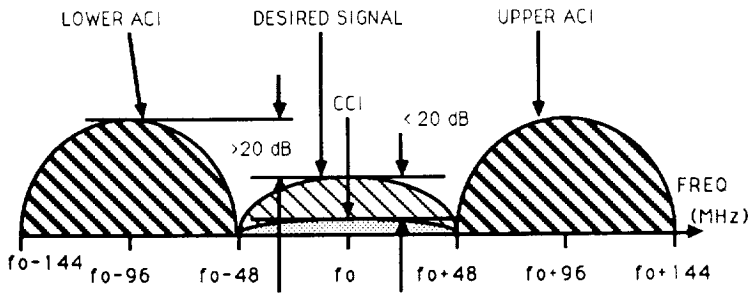


The sub-burst window (SBW) is used to measure the BER in only a selected portion of the burst. Its position within the burst and length are adjustable.

8,000 symbol bursts shown only for example; test equipment can generate any length bursts up to 80,000 symbols

The unique word is eight BPSK symbols for high noise immunity.

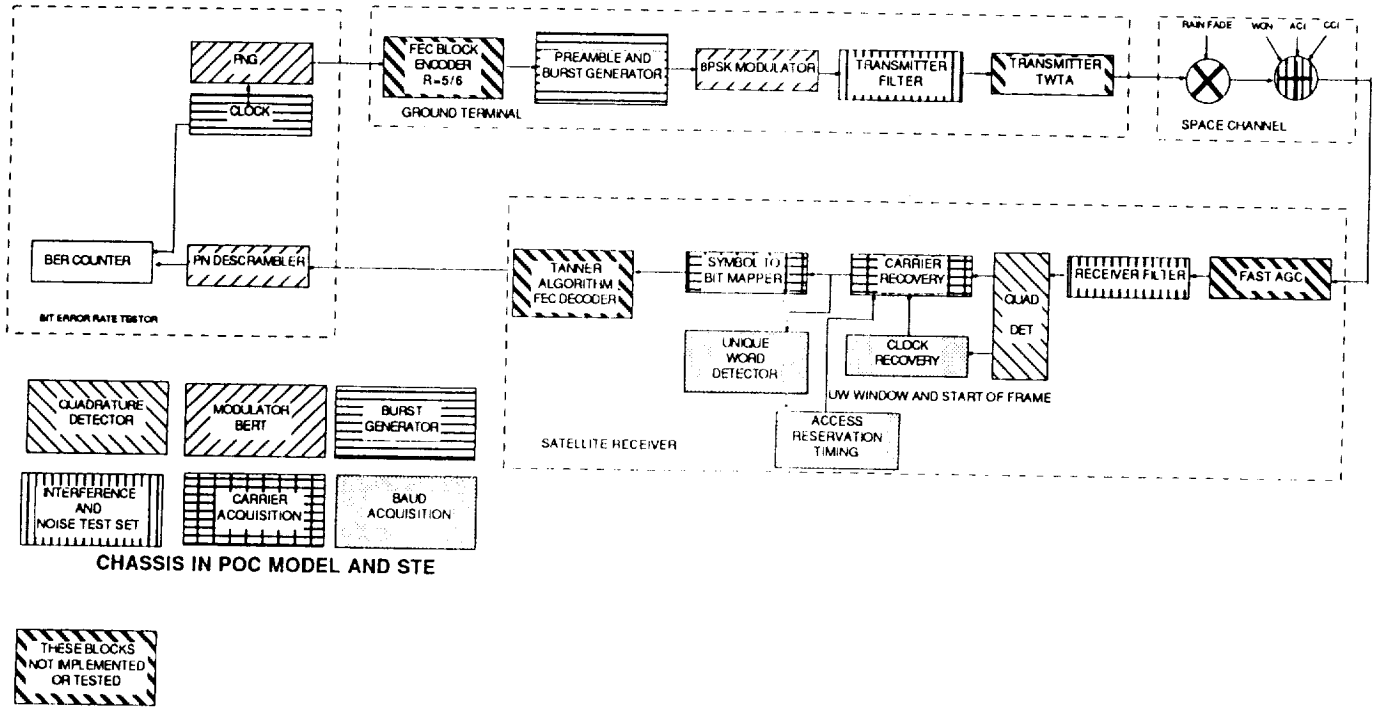
SIGNAL SPECTRA SHOWING CO-CHANNEL AND ADJACENT-CHANNEL INTERFERENCES



Center frequency, fo, specified as 3.373056 GHz ± 1.5 KHz

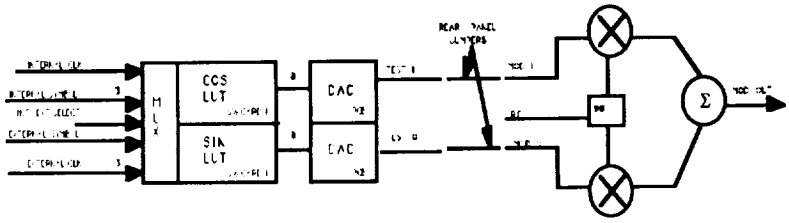
ACI spacing shown to achieve the design goal of 2 bits/sec/Hz with a rolloff factor of 0.2

A block diagram of the ground and satellite system is shown on the following page. The seven different shadings are shown to signify the physical chassis in which the functional unit is located within the POC model and STE. The heavy diagonal hatching (plus the rain fade) illustrates those elements which would be in a full system but were not implemented in the POC model stage because of time and/or budget limitations.



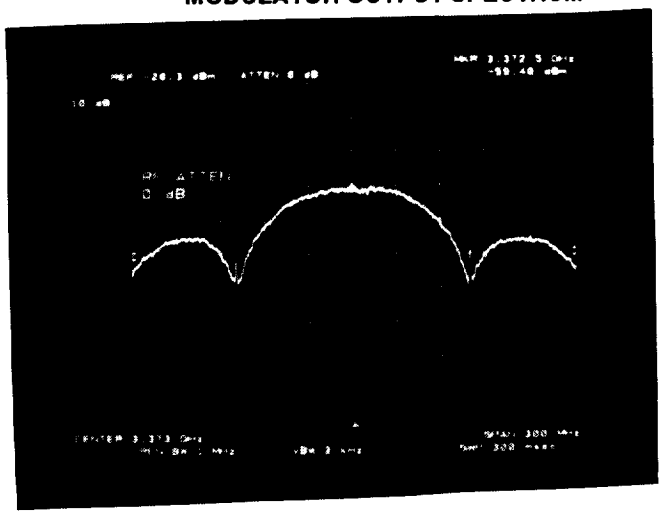
BLOCK DIAGRAM OF GROUND AND SATELLITE TDMA TEST SYSTEM

QUADRATURE MODULATOR

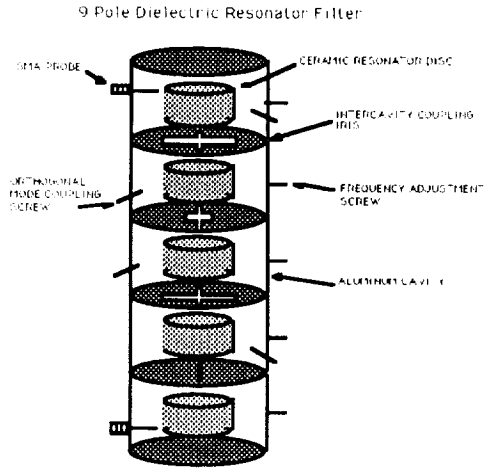


Three bits of Gray coded data are applied as addresses to the sine and cosine LUTs. The LUT contents, which are the projections of the modulation symbol in the I and Q axes, are applied to a pair of DACs and then to the quadrature balanced mixer to produce the spectrum shown on the following page. A highly accurate modulator can be produced since compensation for non-ideal behavior of the balanced mixers can be included in the LUT.

MODULATOR OUTPUT SPECTRUM



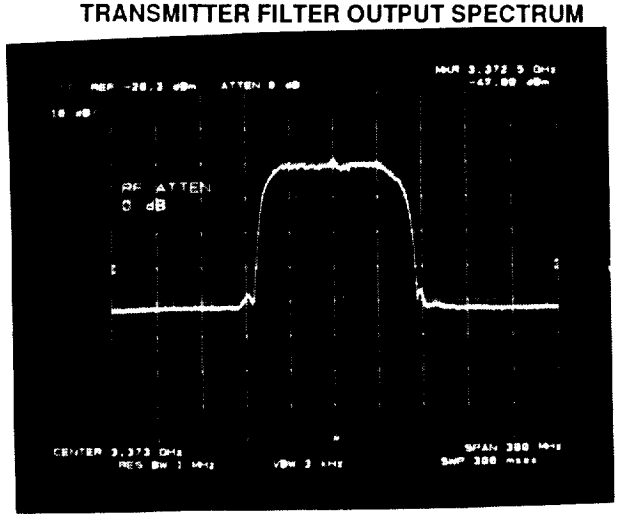
MECHANICAL CONFIGURATION OF NYQUIST FILTERS



The original Nyquist filter design was to produce a rolloff factor of 0.2 (excess bandwidth of 20%) but when tested, too much intersymbol interference resulted. The rolloff factor was increased to 0.4 where a satisfactory eye-pattern was obtained.

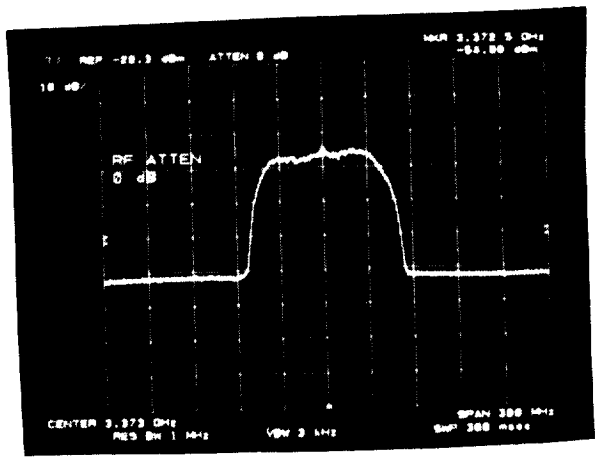
The nine pole filter shown above was comprised of four dual mode and one single mode dielectric resonators to produce the square-root Nyquist response. Identical filters were used in both the modulator and demodulator. In addition, an inverse sinc function equalizer in the transmitter and amplitude and group delay equalizers in both transmitter and receiver utilizing similar resonators were used.

TRANSMITTER FILTER OUTPUT SPECTRUM



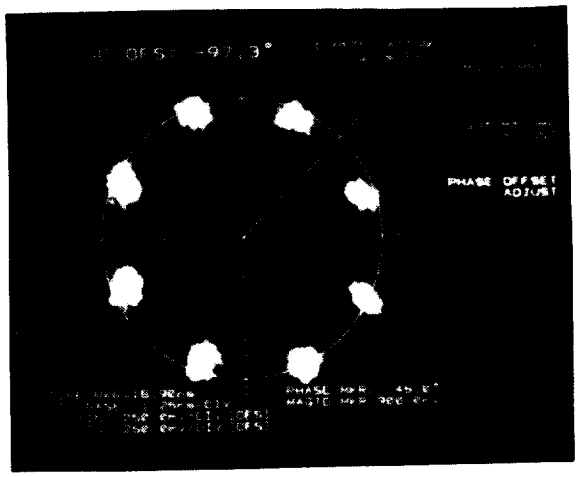
The transmitter spectrum is shown above where the previously displayed modulator spectrum has been equalized by the inverse sinc and then passed through the transmitter square-root Nyquist filter with a 0.4 rolloff factor.

RECEIVER FILTER OUTPUT SPECTRUM

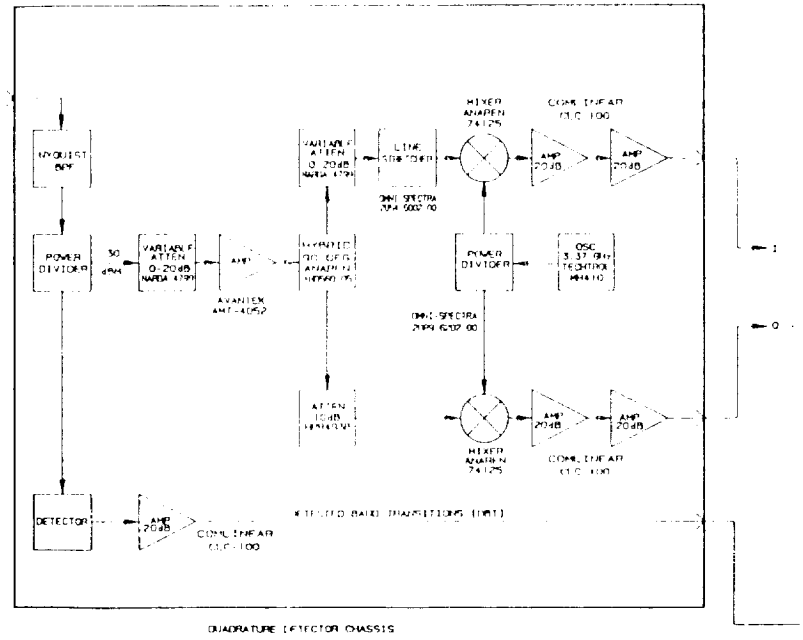


The output of the receiver filter shown above displays the full Nyquist response with 0.4 rolloff factor.

CONSTELLATION OUTPUT AT RECEIVER QUADRATURE DETECTOR

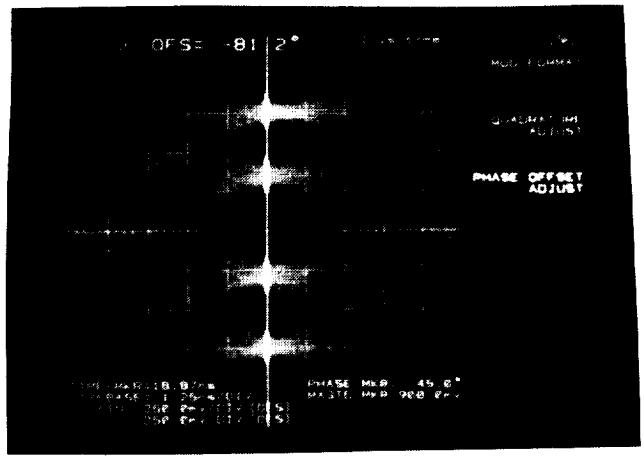


The 8PSK constellation at the output of the receiver quadrature detector as displayed on the HP 8980A vector analyzer. It is at this point that the I and Q signals are digitized and applied to the digital PLL. Note that the constellation at this point is normally still spinning at a rate equal to the difference frequency between the received carrier and the LO. However, for the purposes of producing this constellation display, it has been despun by using a coherent LO.



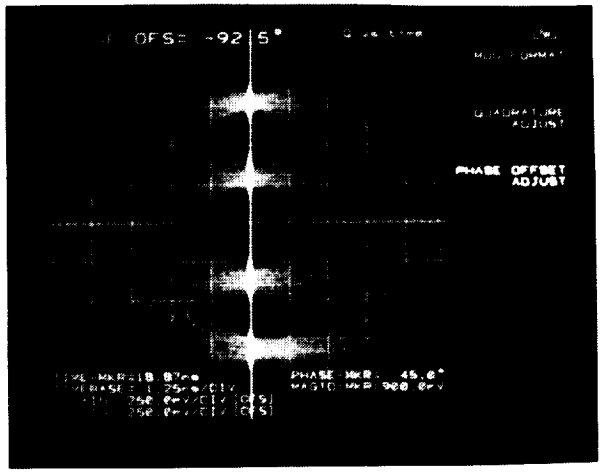
QUADRATURE DETECTOR CHASSIS

EYE PATTERN AT "I" SIDE OF QUADRATURE DETECTOR



The eye patterns using the rolloff factor of 0.4 are open at the point of sampling.

EYE PATTERN AT "Q" SIDE OF QUADRATURE DETECTOR



FEATURES OF THE DIGITAL DEMODULATOR

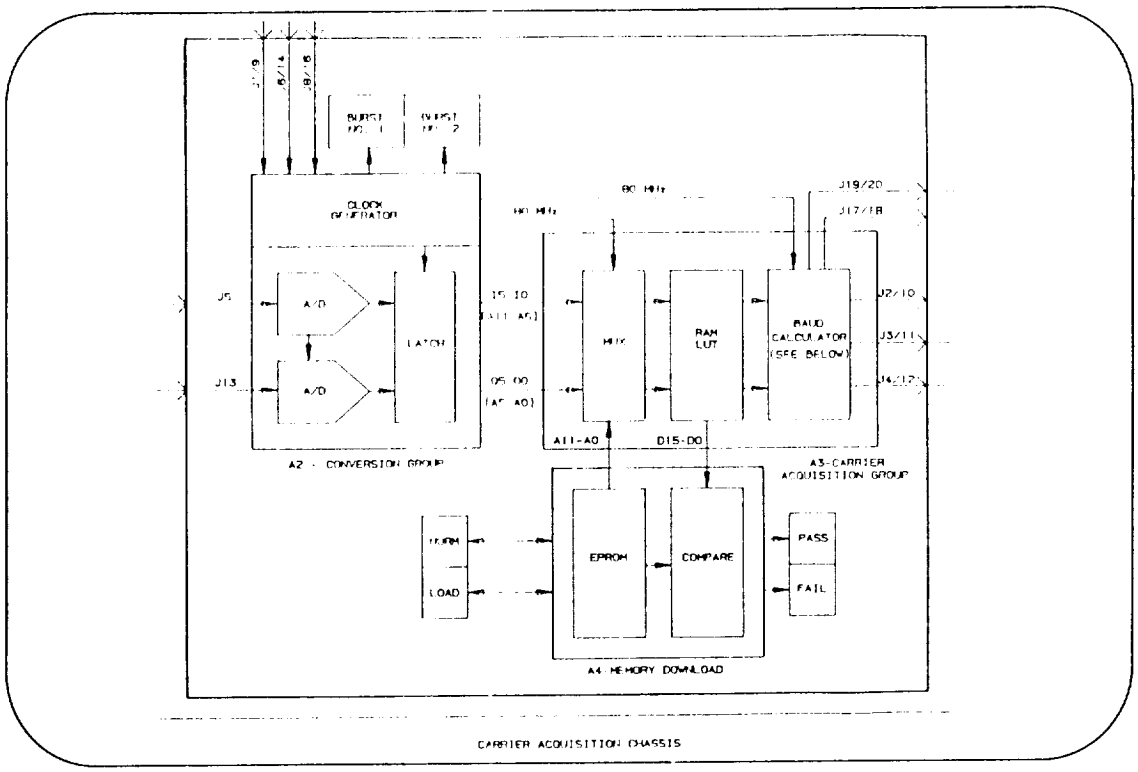
CARRIER ACQUISITION CHASSIS

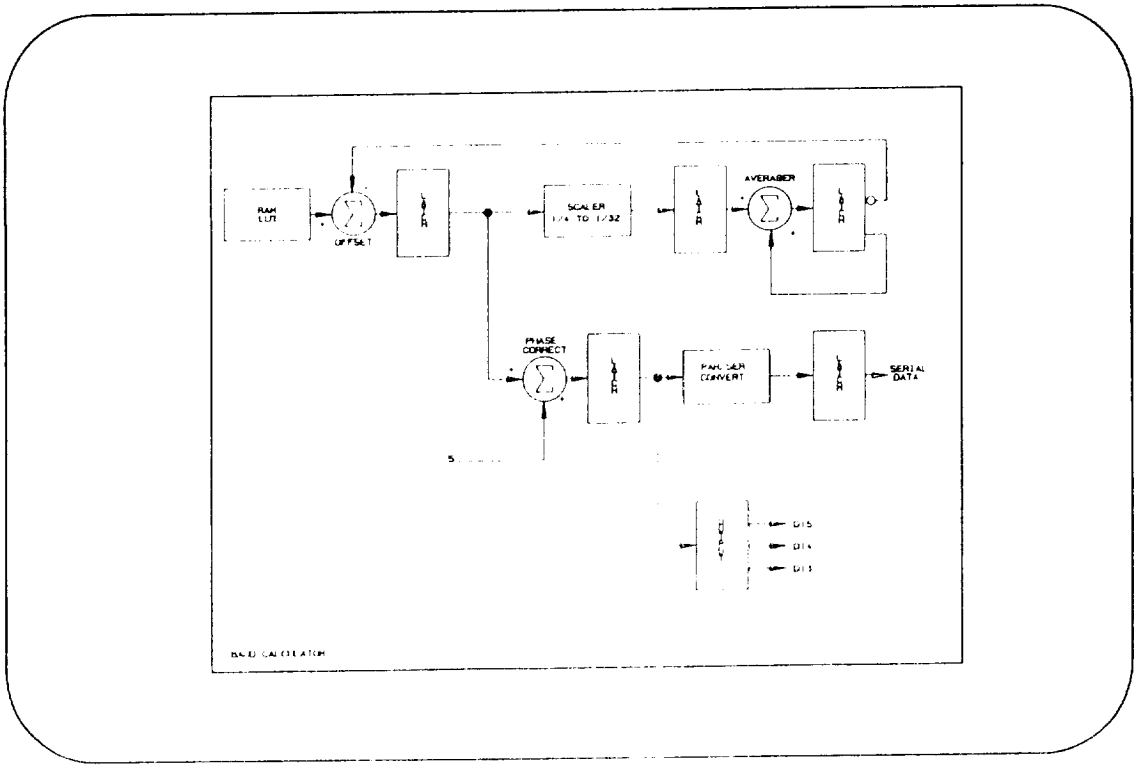
Clock generator is locked to the recovered symbol clock and drives the sampling of the I and Q ADCs once per symbol.

A RAM LUT was used instead of a ROM since a ROM with the necessary access time (less than 5 ns) was not available when the design was started. The RAM is downloaded from the ROM when the system is started. Its contents are the arctangents of the addresses formed by the I and Q data words.

BAUD CALCULATOR

The first order carrier PLL despins the constellation. The PLL gain is 1/8 during the carrier acquisition portion of the preamble and decreases to 1/32 during modulation when it tracks the incoming carrier modulo 45 degrees. The value 0.5 is added to the phase error at the phase correction summer to rotate the phase error samples by 22.5 degrees. This numerically adjusts the decision boundries so that the symbol decision can be made by simply truncating the phase error samples to its three most significant bits.

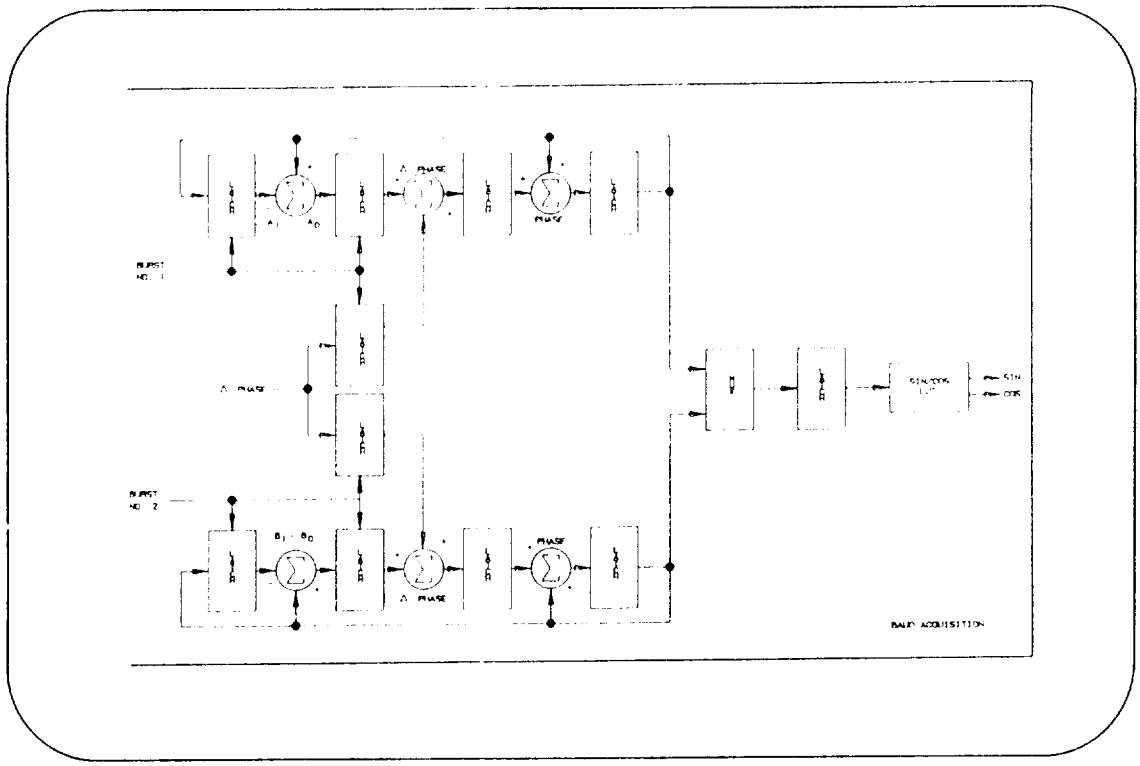

CLOCK GENERATOR
A/D
A/D
LATCH
MUX
RAM LUT
BAUD CALCULATOR (SEE BELOW)
A11-A0
D15-D0
A2 - CONVERSION GROUP
A3-CARRIER ACQUISITION GROUP
EPROM
COMPARE
PASS
FAIL
LOAD
A4 MEMORY DOWNLOAD
CARRIER ACQUISITION CHASSIS

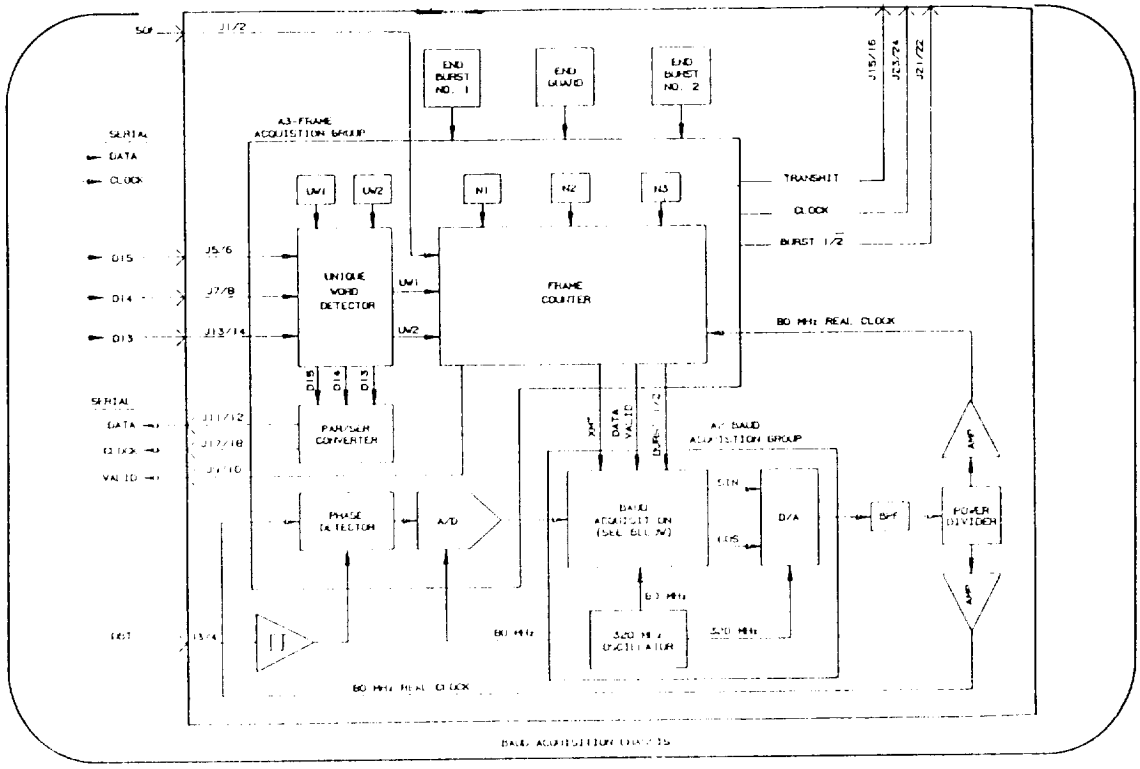

RAM LUT
OFFSET
SCALER 1/4 TO 1/32
AVERAGER
PHASE CORRECT
SERIAL DATA

FEATURES OF THE DIGITAL DEMODULATOR (CONT.)

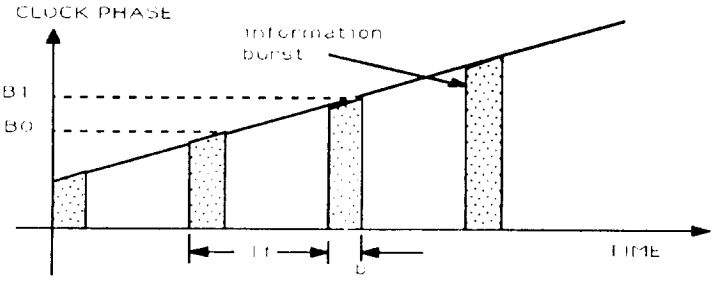
BAUD ACQUISITION CHASSIS

Detected baud transitions are applied to a threshold and phase compared with the output of a numerically controlled oscillator running at a nominal four samples per cycle. A detail of the baud acquisition is shown in the following diagram. It has two independent first order PLLs which track the two test bursts. The baud acquisition exploits the phase continuity of the symbol clock between bursts of the same access to predict the phase change between bursts from the same access. In principle, such a scheme can improve the burst efficiency by eliminating the need for clock transitions to appear in the preamble of each burst. In practice, this scheme needs a "training burst" for each access (probably on a super-frame basis) to correctly initialize the phase predictor. The training burst was not implemented during the POC model phase which probably explains the degraded performance as the bursts were shortened.


BURST NO. 1
Δ PHASE
BURST NO. 2
Σ PHASE
BAUD ACQUISITION

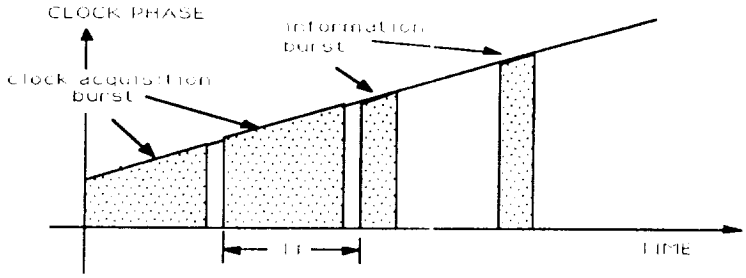

SOF
END BURST NO. 1
END BURST NO. 2
A3-FRAME ACQUISITION GROUP
SERIAL DATA
CLOCK
UW1
UW2
N1
N2
N3
TRANSMIT
CLOCK
BURST 1/2
UNIQUE WORD DETECTOR
FRAME COUNTER
80 MHz REAL CLOCK
PAR/SER CONVERTER
PHASE DETECTOR
A/D
BAUD ACQUISITION (SEE BELOW)
D/A
POWER DIVIDER
A/C BAUD ACQUISITION GROUP
80 MHz
80 MHz REAL CLOCK

SYMBOL CLOCK ACQUISITION

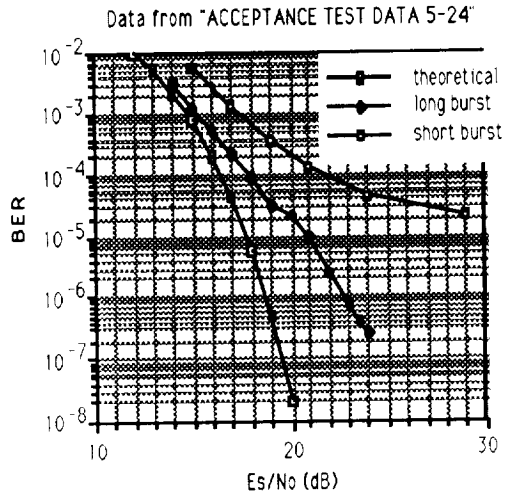


Phase slope = (B1-B0)/Tf

Phase correction=phase slope•(Tf-Tb)-(B1-B0)•(Tf-Tb)/Tf

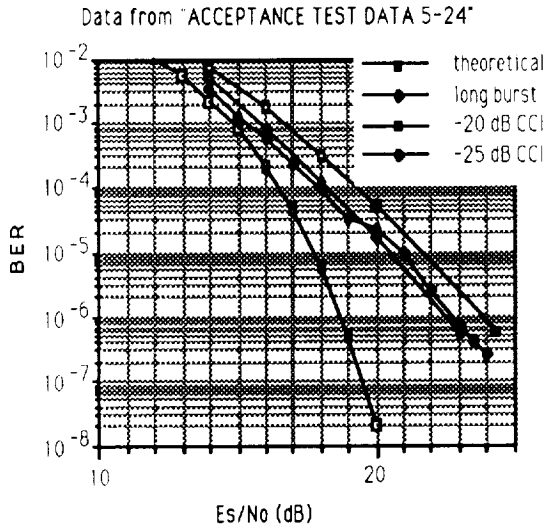


BIT ERROR RATE VERSUS Es/No IN AWGN FOR LONG AND SHORT BURSTS



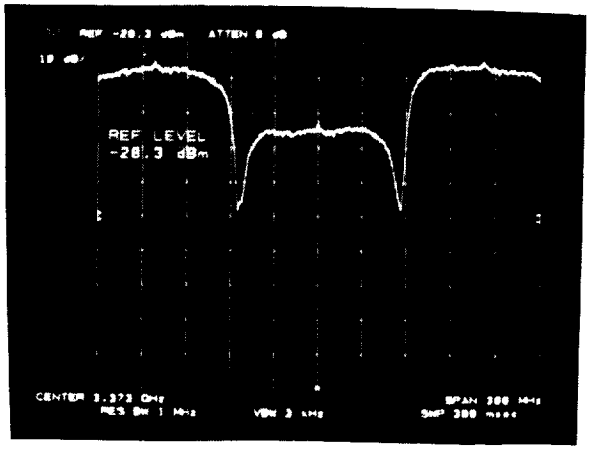
Displayed above is the BER versus the Es/No. The leftmost curve is the theoretical curve for Gray coded 8PSK. The next curve to the right is the measured curve of the POC model when using long bursts (about 90% of the frame). The rightmost curve is the BER for a burst length of about 46% of the frame. The degradation during shorter bursts is probably due to the poor performance of the phase predictor.

BER VERSUS ES/NO IN CCI



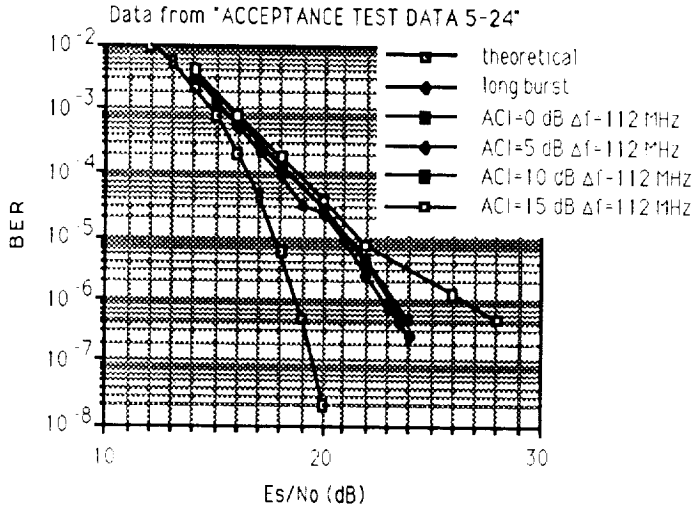
The relatively insensitive behavior of the BER in CCI is probably due to the implementation loss being high enough to mask the effect of CCI. Recall that the CCI degradation predicted from computer simulations at -20 dB CCI was 2 dB at BER equal to 5E-7 while the measured degradation is only about 1 dB.

INPUT SPECTRUM TO RECEIVER WITH +20 dB ACI AT ±112 MHz



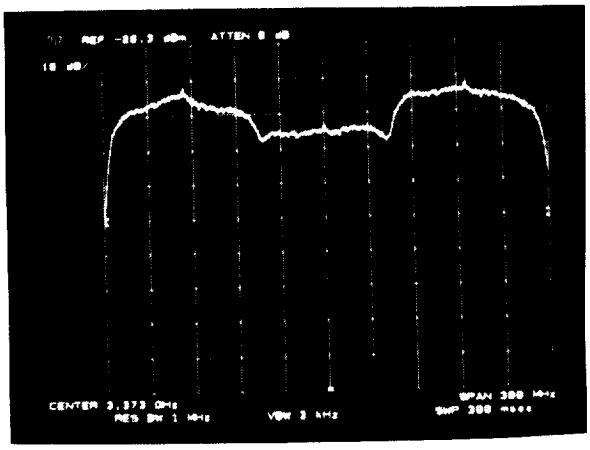
The original spacing between adjacent channels was to be 96 MHz based on the rolloff factor of 0.2. However, since satisfactory filters could not be built with this steepness in the transition band, the correct spacing for the filters with a rolloff factor of 0.4 is 112 MHz. The above spectral display shows two 20 dB ACI signals spaced by 112 MHz. The deep cusps between the spectra indicate little leakage of the ACI power into the desired signal.

BER VERSUS Es/No IN ACI FOR 112 MHz SPACING



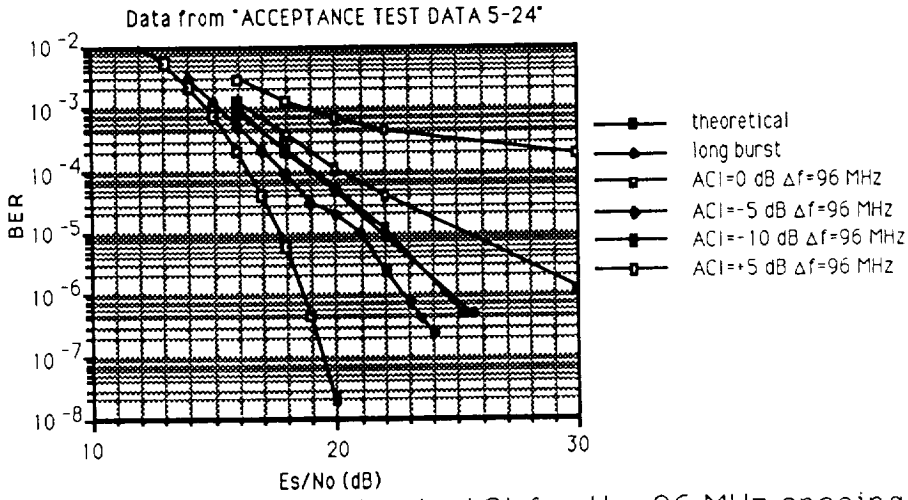
As predicted from the spectral display, until the ACI exceeds 15 dB, small degradation is experienced.

INPUT SPECTRUM TO RECEIVER WITH +10 dB ACI AT ±96 MHz



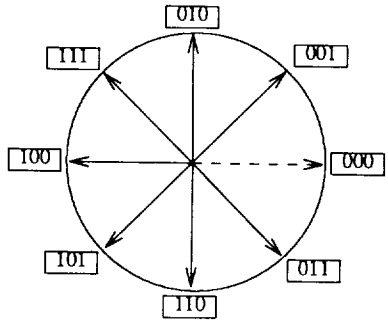
Shown here is the spectral display with the ACI at ± 96 MHz but still using the Nyquist filter with rolloff factor of 0.4. As expected, since the transition band skirts are much less steep, the ACI power leaks into the desired signal to such an extent that the cusps between the spectra are completely filled in even with the ACI at only 10 dB.

BER VERSUS Es/No FOR ACI SPACING OF 96 MHz



As expected, the degradation in ACI for the 96 MHz spacing is very large. The obvious conclusion is that to realize the target bandwidth efficiency with the coded 8PSK, it is necessary to use a Nyquist filter with a 0.2 rolloff factor. We believe that such a filter can indeed be realized using a properly equalized SAW device at a center frequency of about 280 MHz. Several iterations of the filter mask may be required to achieve the desired response and this contingency should be planned for.

SIGNIFICANT BIT 8PSK TO 3-TUPLE MAPPING

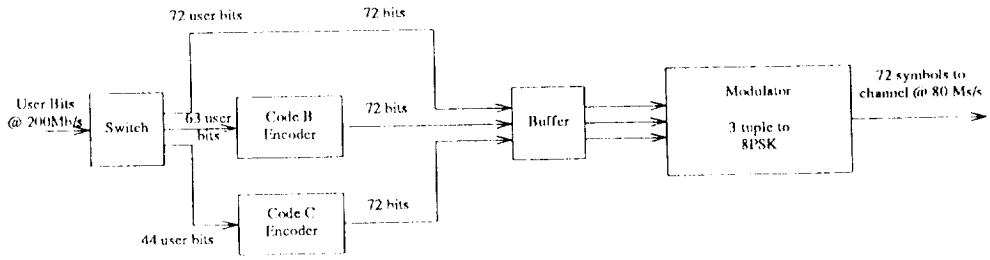


Due to budgetary limitations, the coding portion of the AMTD POC model was only produced as a "paper design". Its features will be outlined in the next few panels.

While the POC model used Gray coding of the symbol constellation for improved noise immunity, the constellation coding shown above would be used with our FEC system. The coding shown is called significant bit 8PSK to 3-tuple mapping and results in a combined modulation and FEC system which can be set partitioned as follows:

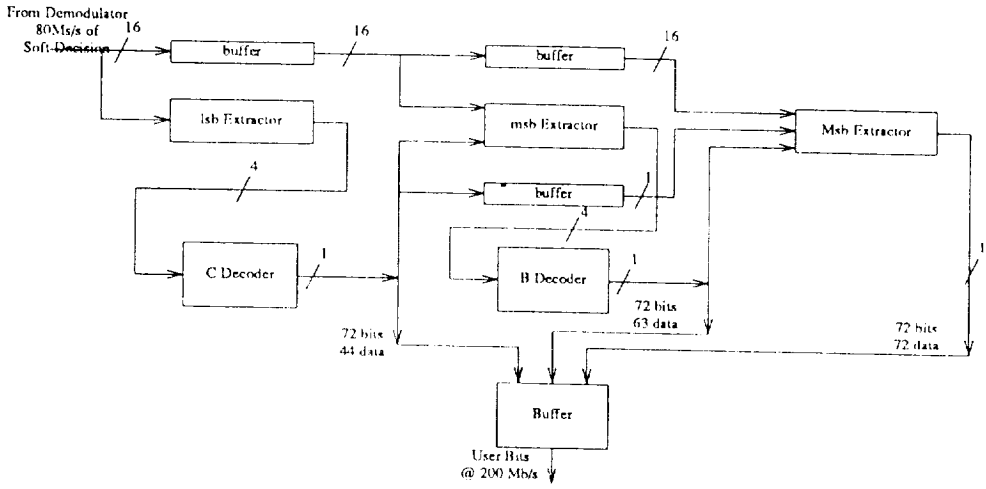
The lsb (the rightmost bit) if it is a 0 signifies one QPSK constellation while if it is a 1, signifies the other QPSK set rotated 45 degrees to the first. Similarly, within each QPSK set, the msb (middle significant bit) signifies one of two BPSK sets. The Msb (Most significant bit) signifies which of the BPSK states is sent. The decoder uses this knowledge of the set partitioning to decode the symbol starting with the lsb and using that information to decode the msb and, finally, uses the lsb and msb information to decode the Msb.

ENCODER SYSTEM



The encoder system shown above takes into account the minimum Euclidean distances (E.D.) between the transmitted phase states. Since the lsbs select between adjacent QPSK constellations which have the smallest E.D., they are encoded with the most powerful code, a shortened 73 bit BCH code of rate 44/72; indicated above as the Code C encoder. The msbs select between alternative BPSK sets within the QPSK sets. Since the BPSK sets have a larger E.D., Code B, which encodes the msb is a lower power Hamming code of rate 63/72. The Msb, since it selects between antipodal states, is uncoded. The overall coding rate is aproximately 5/6. The bandwidth expansion is 6/5 which when combined with the 200 MHz uncoded data rate yields 240 Mbps (coded). Using 8PSK with 3 coded bits per symbol and the targeted adjacent channel spacing (using the 0.2 rolloff filter) of 96 MHz, obtains the target bandwidth efficiency of 200/96=2.08 bits/sec/Hz.

DECODER SYSTEM



A block of 72 8PSK symbols are input from the demodulator to a cascade of buffers each 72 symbols long and 16 bits wide. The input rate is 80 Msps or 240 Mbps (coded). The lsb extractor estimates the lsb sign and soft decision weight from the channel data and passes this infomation to the C Decoder. The C Decoder performs a soft decision block decoding on the lsb data according to the Tanner Algorithm B (reference 1). The Tanner algorithm has the advantage of a lower computational complexity and is amenable to a highly parallel decoder circuit architecture compared to the traditional BCH hard decision decoders such as those using the Berlekamp-Massey algorithm. The C Decoder will "almost always" correct four errors in a block and can correct up to eight errors.

The channel data along with the lsb decisions are passed to the msb extractor. The lsb decisions are also buffered for use by the Msb extractor. The msb extractor estimates the signs of the block of msbs and passes them for decoding in the hard decision B Decoder which is a modified Hamming decoder correcting one error per block. The lsb and msb decisions along with the channel data is passed to the Msb extractor for hard decisions on the block of Msbs. The lsb, msb, and Msb data is serialized and output from the output buffer at 200 Mbps (uncoded). The performance of this decoding system was shown on a previous page. It produces about 5 dB coding gain in AWGN at an output BER of 5e-7.

Reference 1: R. M. Tanner, "A Recursive Approach to Low Complexity Codes", IEEE Transactions on Information Theory, VOL. IT-27, No. 5, Sept. 1981

C.2

SUMMARY

- CONCEPT OF THE POWER AND BANDWIDTH EFFICIENT SATELLITE DEMODULATOR HAS BEEN PROVEN WITHIN THE BUDGETARY CONSTRAINTS OF THE PROGRAM
- BANDWIDTH EFFICIENCY COULD BE DEMONSTRATED (I.E., ACI SPEC MET) THROUGH FILTER IMPROVEMENTS
- POWER EFFICIENCY COULD BE DEMONSTRATED (I.E., BER SPEC MET IN AWGN) THROUGH IMPROVEMENTS IN CLOCK RECOVERY LOOP AND FILTERS
- DIGITAL PORTION OF THE SATELLITE DEMODULATOR COULD BE REALIZED IN TWO GATE ARRAYS PLUS SOME MEMORY CHIPS, ANALOG PORTION COULD BE GREATLY REDUCED IN SIZE AND WEIGHT BY UTILIZING SAW FILTERS AND AN MMIC QUADRATURE DETECTOR
- CODEC PERFORMANCE WITH DEMOD IN CCI PROVEN BY SIMULATION