RATE 8/9 CODED 8-PSK SYSTEM FOR DOWNLINK APPLICATIONS

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ABSTRACT

An advanced Coded Trellis Modulation (CTM) System which achieves a 2 bits/s/Hz bandwidth efficiency at an information rate of 200 Mbit/s while minimizing satellite power requirements, has been developed for downlink earth station applications. This CTM system employs a high-speed rate 8/9 convolutional code with Viterbi decoding and an 8-PSK modem. The minimum Euclidean distance between the modulated waveforms corresponding to the information sequences are maximized in order to maximize the noise immunity of the system. Nyquist filters with square-root 40 percent roll-off are used at the transmit and receive sides of the modem in order to minimize intersymbol interference, adjacent channel interference, and distortion at the nonlinear satellite power amplifier. The use of coded system here also minimizes the effects of co-channel interference. The developed performance of the hardware system has been measured to achieve within 1.5 dB from theory at a bit error rate of 5×10^{-7} over an additive white Gaussian noise channel.

The Viterbi codec subsystem operates at an information rate of 200 Mbit/s and a channel rate of 225 Mbit/s without using parallel processing and is believed to be the highest speed, high code rate Viterbi codec ever built in the world. This codec required the development of 16 special hybrid circuits to realize the 16 add-compare-select (ACS) operations necessary for decoding the 16 state convolutional code with the Viterbi algorithm. These ACS hybrids can operate at a speed as high as 110 MHz. Due to excessive power dissipation, forced air is required for cooling. To minimize power dissipation and the cooling requirements, these ACS hybrid circuits are now being replaced by ECL gate-arrays with lower power dissipation. Each gate-array chip contains two ACS circuits, and hence a total of 8 is needed rather than 16. No forced air will be necessary. These ECL gate-arrays have achieved a clock speed ranging from 120 MHz to 150 MHz. The gate-array upgrade version of the coded 8-PSK system will be completed in the Summer of 1989.

PROGRAM OBJECTIVES

- To develop an advanced coded trellis modulation system which achieves a 2 Bit/s/Hz bandwidth efficiency at an information rate of 200 Mbit/s while minimizes satellite power requirements for downlink applications.

- Specifically, to develop a rate 8/9 high speed Viterbi FEC codec, a burst-mode 75 MBaud 8-PSK modem, and the associated special test equipment (STE).

The key performance goals of the coded 8-PSK system are summarized into the table below.

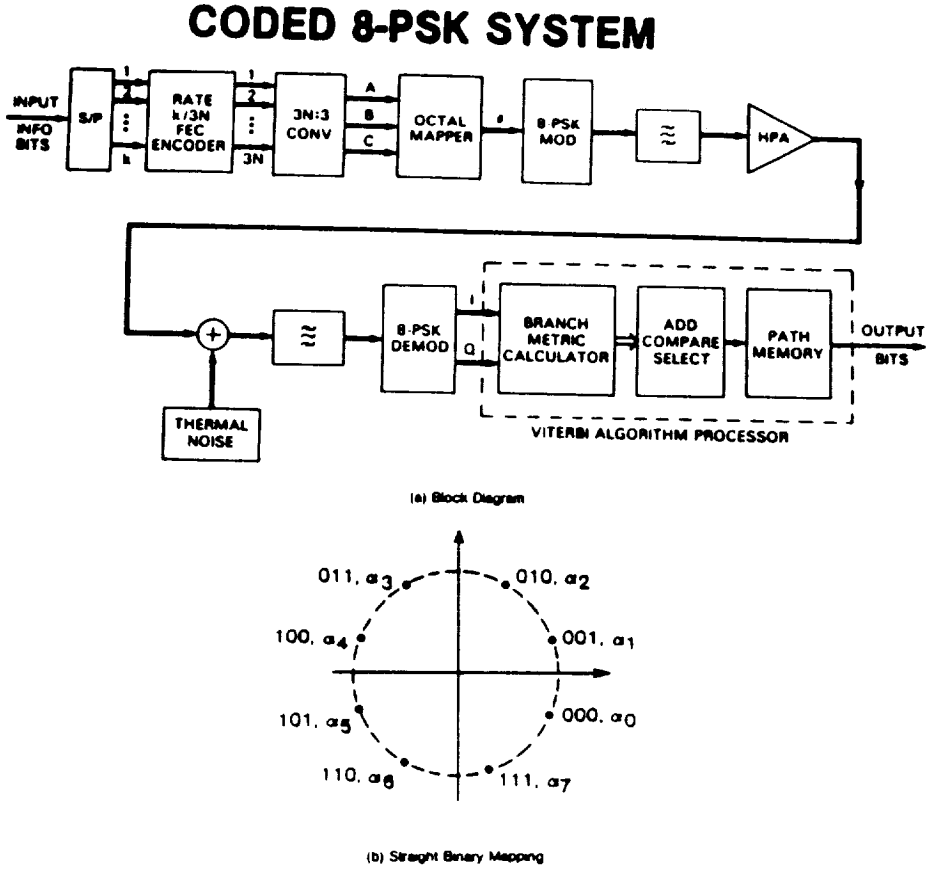
PERFORMANCE GOALS

PARAMETER	GOAL
INFORMATION RATE	200 MBPS
8-PSK SYMBOL RATE	75 MSPS
BANDWIDTH EFFICIENCY	2 BIT/S/Hz
CHANNEL BANDWIDTH	100 MHz
FEC CODE RATE & TYPE	8/9, CONVOLUTIONAL
DECODER TYPE	VITERBI @ 75 MHz
GUARD TIME BETWEEN BURSTS	10 usec
PROB. OF MISS AND FALSE UW DETECTION	$<1 \times 10^{-8}$
BURST TO BURST VARIATION	10 dB
BACK-TO-BACK MODEM/CODEC PERFORMANCE	2 dB FROM THEORY @ 5×10^{-7} OVER AWGN CHANNEL
DEGRADATION DUE TO CCI @ C/I=20 dB	<1 dB @ 5×10^{-7}
DEGRADATION DUE TO ACI @ ACI = 20-dB	<1 dB @ 5×10^{-7}

SYSTEM OVERVIEW

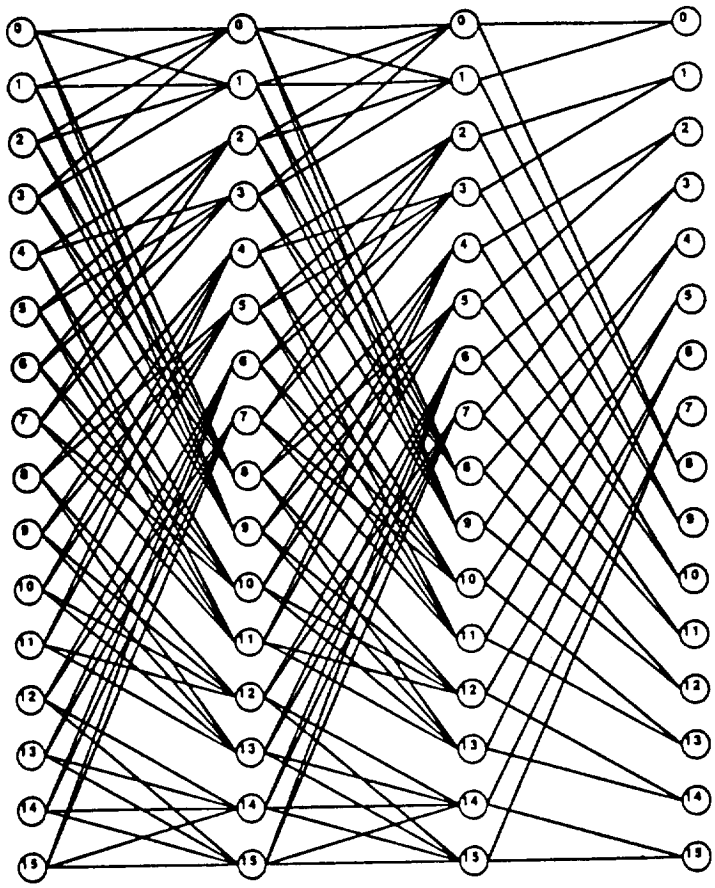
CODED 8-PSK SYSTEM SYSTEM DESCRIPTION

Input information bits at 200 Mbit/s are converted by the serial-to-parallel converter into 8-bit words at 25 MHz. These 8-bit words are encoded by a rate 8/9 convolutional encoder followed by a 3 to 1 parallel-to-serial converter. Thus, these output 3-bit words are at a speed of 25 x 9÷3 = 75 MHz. Each of these 3-bit word is mapped by an octal mapper into one of the 8 phases for transmission by an 8-PSK modulator at 75 Msps.



TRELLIS REPRESENTATION

The output of the modulator can be represented by a trellis. To maximize the system noise immunity, the convolutional encoder and the octal mapping function are optimized to maximize the minimum Euclidean distance between the code word sequences at the output of the modulator rather than merely the minimum Hamming distance between the algebraic code words at the input of the octal mapper. To further simplify the codec implementation a time varying code is selected, which is composed of three subcodes of rate 3/3, 3/3, and 2/3 each.

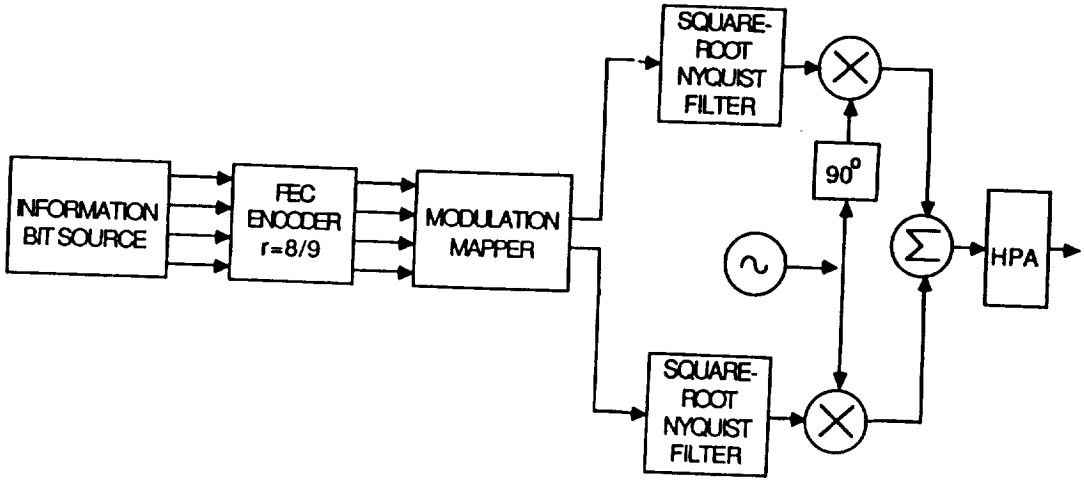


TRELLIS OF RATE 8/9 CODE

8-PSK MODULATOR

The 8-PSK modulator employs a quadrature modulation structure. The shaping filters are realized in the baseband. To minimize intersymbol interference and adjacent channel interference, 40 percent square root Nyquist filters are employed.

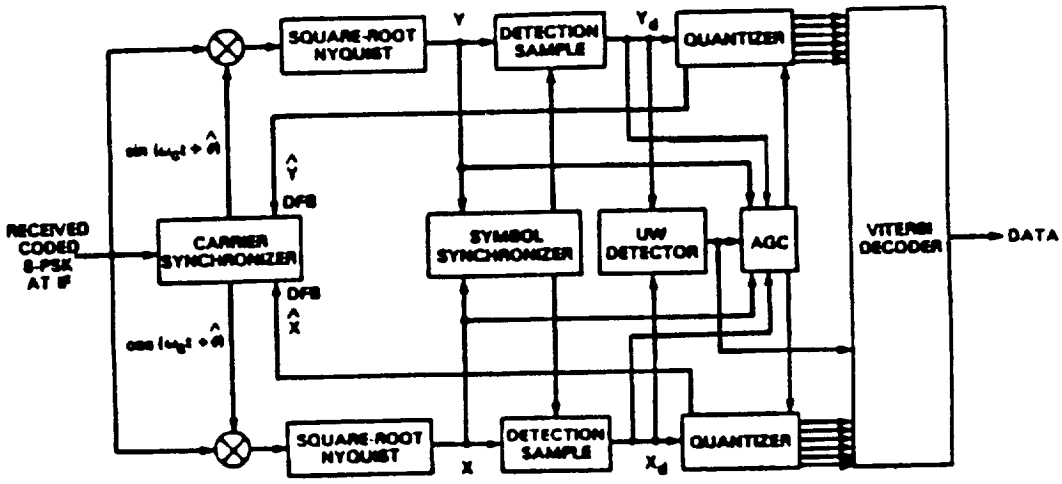
GENERATION OF CODED OPSK BY THE USE OF A QUADRATURE MODULATOR



8-PSK DEMODULATION

The received coded 8-PSK signals are coherently detected into in phase and quadrature components by first recovering the carrier. Nyquist filters with 40 percent roll off are then employed to match filter these two components. After symbol timing, UW and AGC are obtained, these two quadrature components are sampled and quantized into 5-bit words for Viterbi decoding.

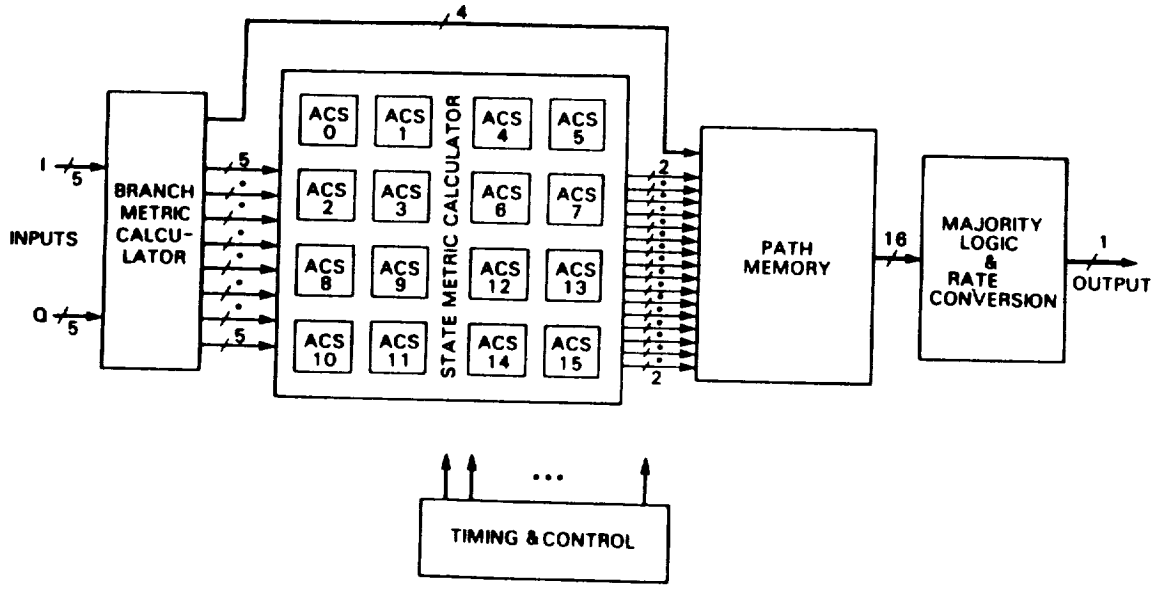
DEMODULATOR



VITERBI DECODER

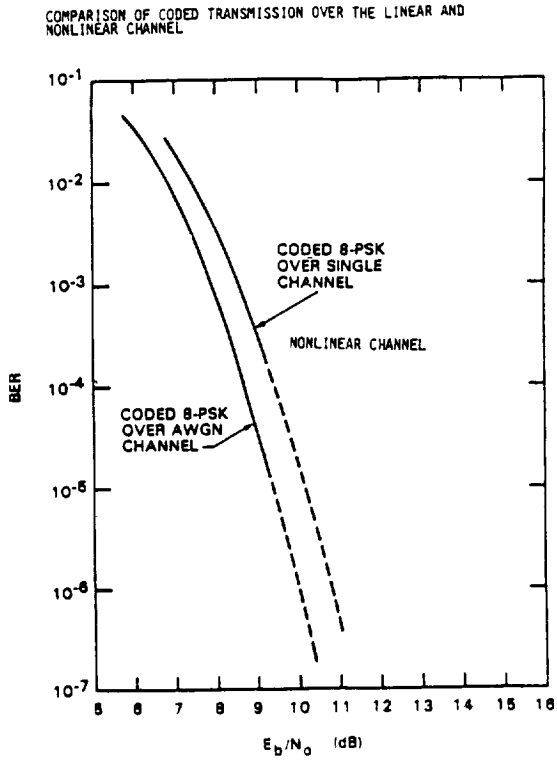
The Viterbi decoder takes the 5-bit I and Q components from the 8-PSK demodulator and performs the following functions: (i) branch metric calculation for each branch leading into each code state, (ii) adding branch metric to the path metric leading into each code state, comparing them, and selecting the largest cumulative path metric as the new state metric, and (iii) path memory traceback for recovering the corresponding information sequence.

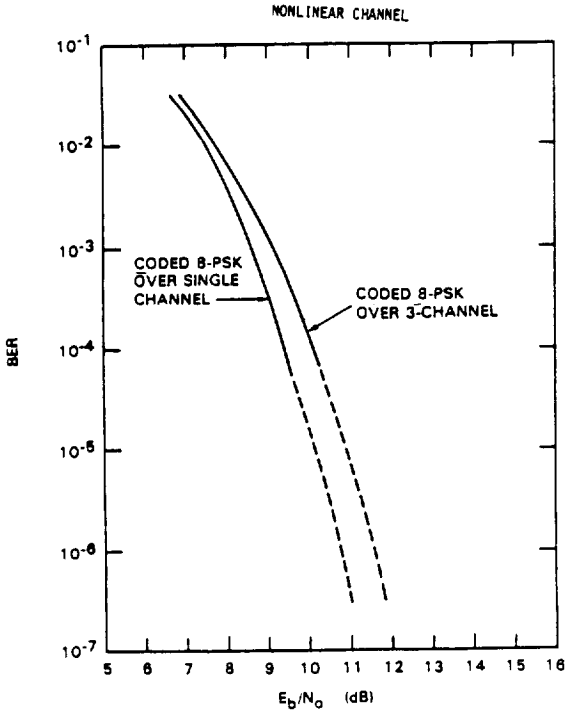
MAXIMUM-LIKELIHOOD VITERBI DECODER

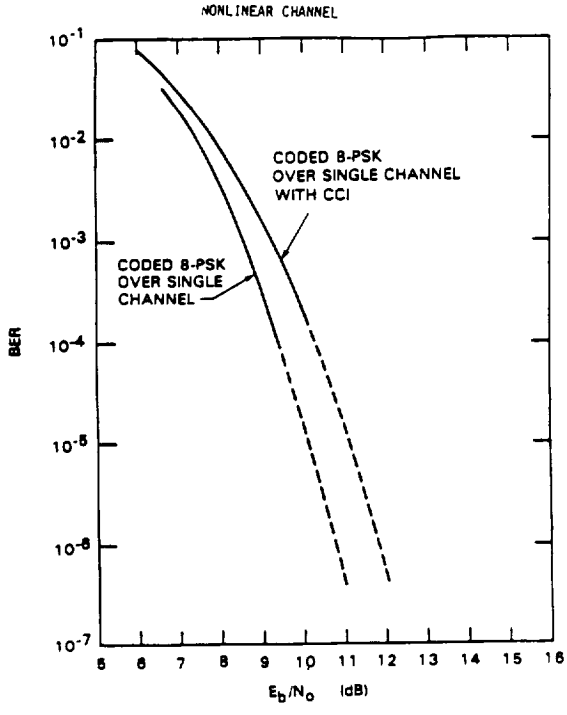


PERFORMANCE SIMULATION

Performance of the rate 8/9 coded 8-PSK system has been simulated for various channel conditions including: (i) AWGN channel, (ii) a single nonlinear satellite channel, (iii) three contiguous nonlinear satellite channels, and (iv) a single nonlinear satellite channel with co-channel interference. In all cases, 40 percent roll off square root Nuquist filters are employed.







Viterbi decoding is an implementation of maximum likelihood decoding for convolutional codes. The output of a maximum likelihood decoding of any sequence of received symbols, **y**, is that sequence of transmitted symbols, **x'**, which maximizes the conditional probability:

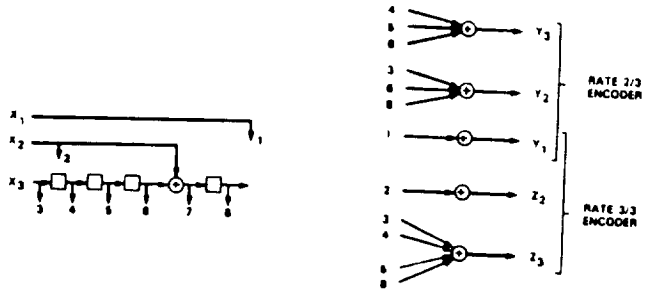
$$\mathbf{x}' = \mathbf{x}_m \text{ if } \Pr(\mathbf{x}_m|\mathbf{y}) > \Pr(\mathbf{x}_{m'}|\mathbf{y}) \text{ for all } m' \neq m \qquad (1)$$

This rule will result in minimum probability of error. Equivalently, the logarithm of the probability can be maximized, since the logarithm is a monotonically increasing function. If the symbols are independent, the logarithm of this joint probability can be decomposed into the sum of the logarithms:

$$\ln \Pr(\mathbf{x}|\mathbf{y}) = \sum \ln \Pr(x_i|y_i) \qquad (2)$$

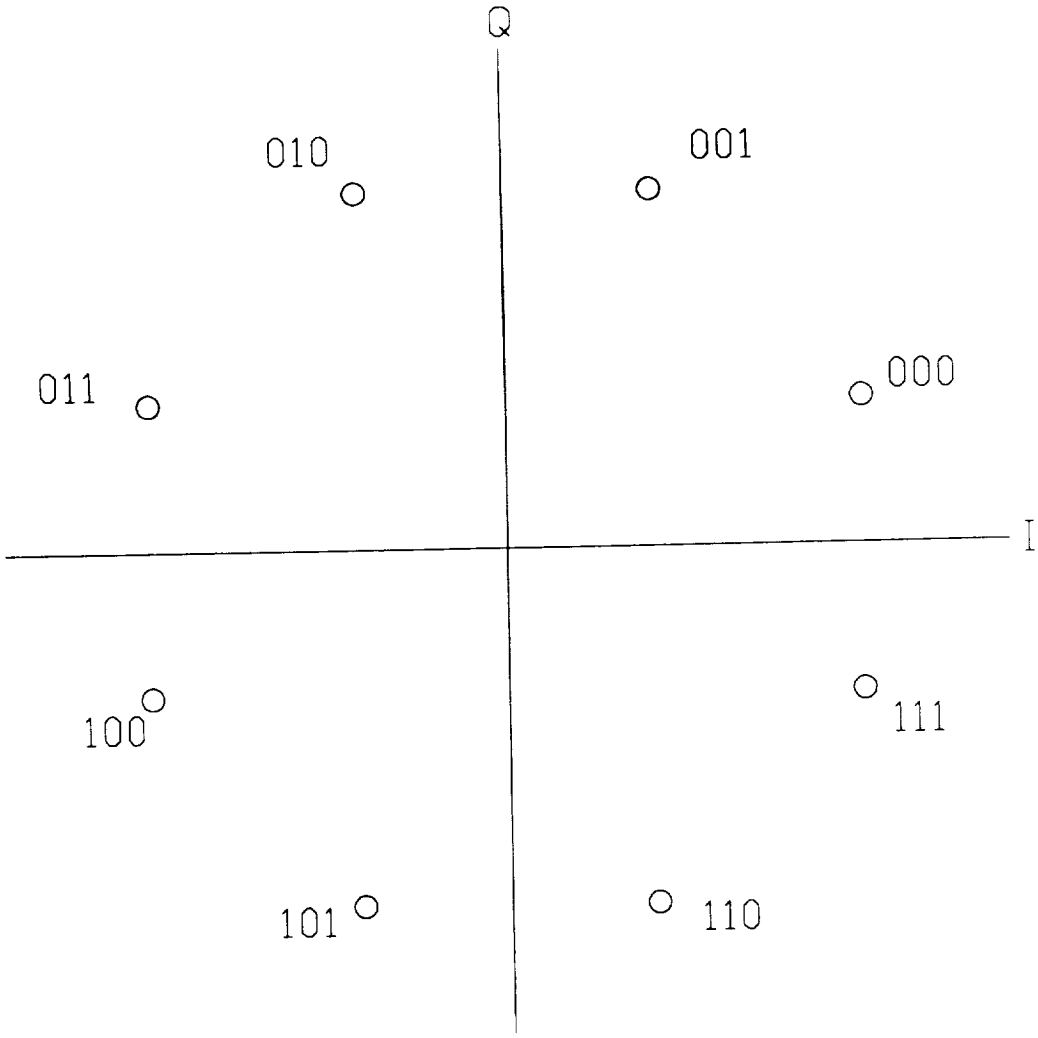
Thus, maximum likelihood decoding of independent symbols is performed by finding the set of symbols, x_i, which maximizes this sum of conditional probabilities. The convolutional coding system used here is based on a finite state machine and can therefore be represented by a trellis diagram. Because the encoder has finite memory, the summations in (2) do not have to be taken over a set of sequences that increases exponentially without bounds over increasing sequence length. Instead, each sequence can be considered as one path through the trellis diagram. Whenever two or more paths merge in the same state, only the best path needs to be followed. Thus, rather than forming an unlimited number of summations over all possible sequences, there need be only a finite number of summations, one for each state.

The convolutional encoder used in this application implements a periodically time-varying code, with a period of three symbols. The first symbol is formed from two information bits, while the second and third symbols are formed from three information bits. This gives a total of 8 information bits forming three octal symbols, for an overall rate of 8/9. The four bit memory of the encoder implies 16 possible code states. Notice, too, that the MSB of each output symbol is identical to one of the information bits; this bit is referred to as uncoded. The introduction of the uncoded bits through the encoder is one of the factors that allows the decoder design to depart from that of a conventional Viterbi decoder.



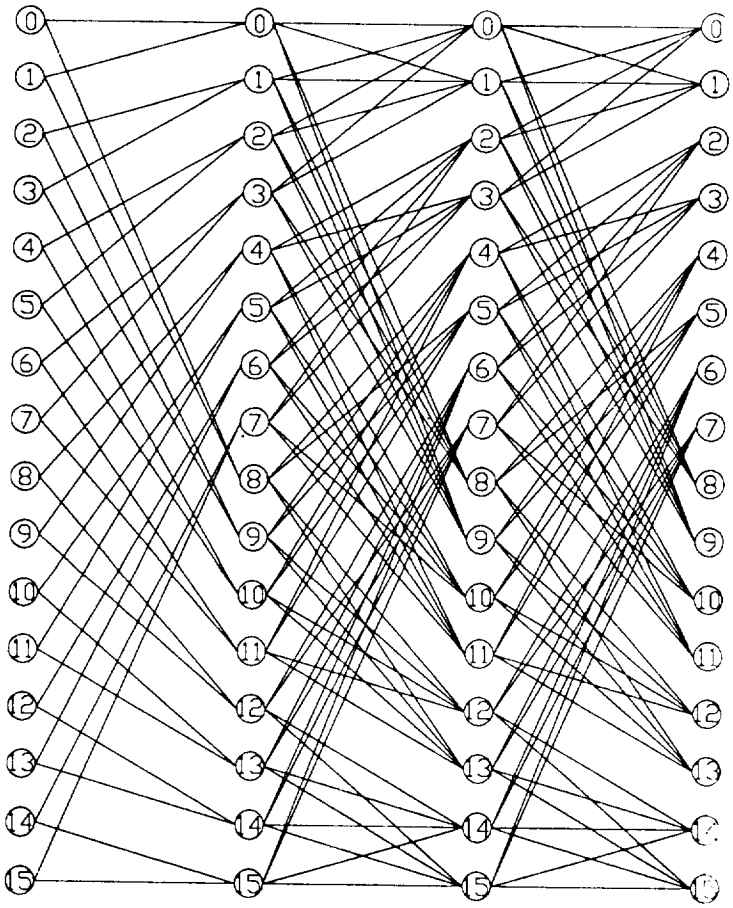
Rate 8/9 Time-varying Convolutional Encoder Block Diagram.

The encoder output symbols are mapped into 8-PSK modulator input symbols in such a way as to maximize the Euclidean distance between them. As mentioned previously, one bit of each symbol is uncoded, in the sense that it does not affect the state of the encoder. Under mapping, this bit selects between antipodal symbols. The large Euclidean distance between the uncoded bits is sufficient to decode the points without additional error protection. However, decoding of the uncoded bits leads to a new design complexity. While these bits are simply decoded by a binary hard decision as in BPSK, the axis on which the decision is made is not known by the decoder a priori. There are four possible decision axes corresponding to the two lower bits of each symbol. The BPSK hard decision must be made after the Viterbi processor determines the two lower bits of each symbol.



8-PSK Mapping of Encoded Symbols.

Considering the four bit convolutional encoder finite state machine operation, the rate 8/9 code can be represented by this 16-state trellis diagram. Any sequence of symbols can be represented as a path through this trellis diagram. One full period of the periodically time-varying code is shown. On two of the code steps, there are four possible paths into each state, while on the third step there are two possible paths into each state. Actually, each of the branches on the trellis is a double branch, since two different information sequences, differing in the uncoded bit, can lead to the same state transition. The maximum likelihood decoding procedure for this code selects the best of the four inputs into each state as each symbol is received and resolves the double branch issue as a BPSK decision using the path information selected from the trellis decoding. During the time-varying steps of the trellis decoding process, the hardware control multiplexes different inputs into the state processors that correspond to the branch metrics for the related encoder transitions.



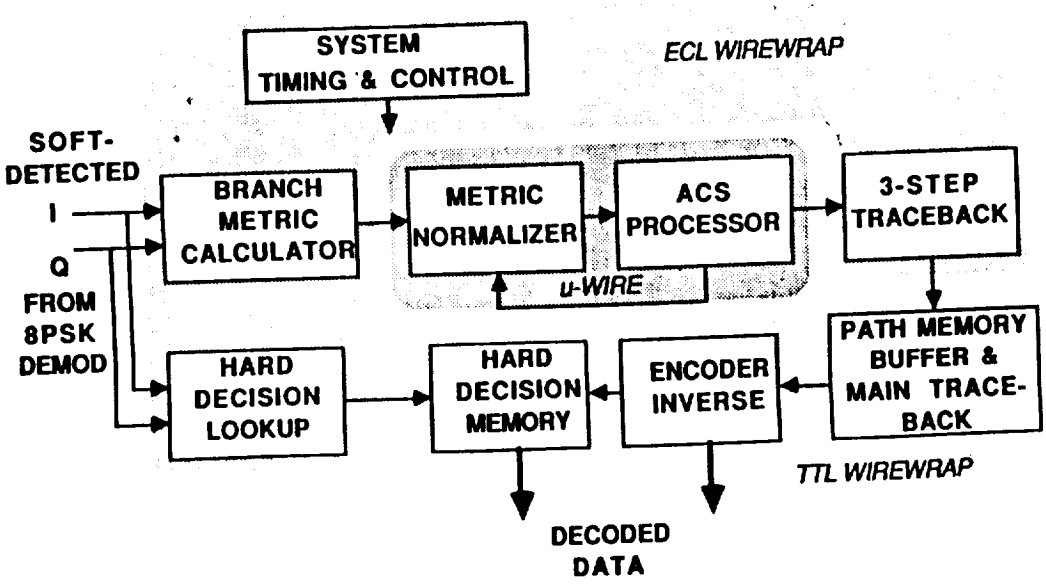
Trellis of Rate 8/9 Code.

The hardware implementation of the Viterbi decoder is divided into 8 major functions. These are:

- branch metric calculator
- hard decision lookup
- metric normalizer
- ACS processor
- 3-step traceback
- main traceback
- hard decision memory
- encoder inverse

The functions are grouped into circuit boards according to the board packaging technology used. The different technologies are :

- ECL wirewrap
- Microwire
- TTL wirewrap



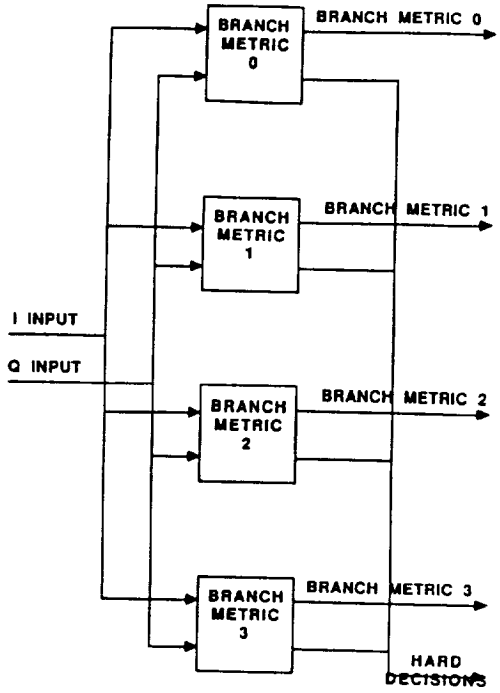
Viterbi Decoder Block Diagram.

For independent symbols over an AWGN channel, the branch metrics are linearly related to the log of the conditional probability :

$$BM(\underline{x},\underline{y}) \sim \ln[Pr(\underline{x}|\underline{y})] \sim (\underline{y} - \underline{x})^2$$

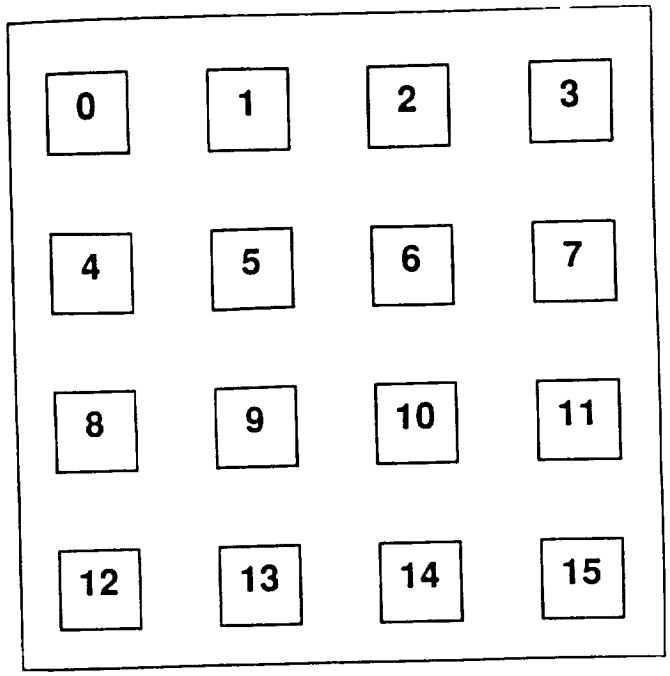
where $\underline{y}$ is the received symbol vector and $\underline{x}$ is the transmitted symbol vector. These branch metrics are the inputs to the ACS processor. The uncoded bits are decoded by a simple binary antipodal decision, called a hard decision, since the uncoded bit is used to select antipodal symbols. The correct axis to use for the binary decision is not known until the other two bits in the symbol are decoded, so all four possible decisions are made on the input vector and these decisions are stored for later use.

The branch metric calculation and hard decision operations are both performed in parallel by a simple table lookup in the decoder. The table is formatted so that it automatically selects the closest of the pairs of symbols. There are four six bit branch metrics and four sets of 1 bit hard decisions for each (I,Q) input vector from the demodulator.



Branch Metric and Hard Decision Lookup Block Diagram.

The state metric calculator is the heart of the Viterbi decoder, and must operate at the received symbol rate. It consists of 16 Add-Compare-Select (ACS) units, one for each code state. Each ACS unit has four branch metric inputs and four corresponding state metric inputs. The state metric output of each ACS unit connects to the state metric inputs of four ACS units, in the same interconnection pattern as shown in the trellis diagram. Because the code is time-varying, during the rate 2/3 code step only two sets of inputs are used, while on the rate 3/3 code steps all four inputs are used. The ACS units have additional inputs which are used to disable the unused branch and state metric inputs during the rate 2/3 step. These ACS units compute the accumulated path metrics (state metrics) by adding the branch metric inputs to the corresponding state metric, and selecting the minimum (most likely) as the new state metric for that state. The ACS units also output a binary code at each symbol interval, indicating which of the input branches was selected. This branch select information is used by the traceback circuits.

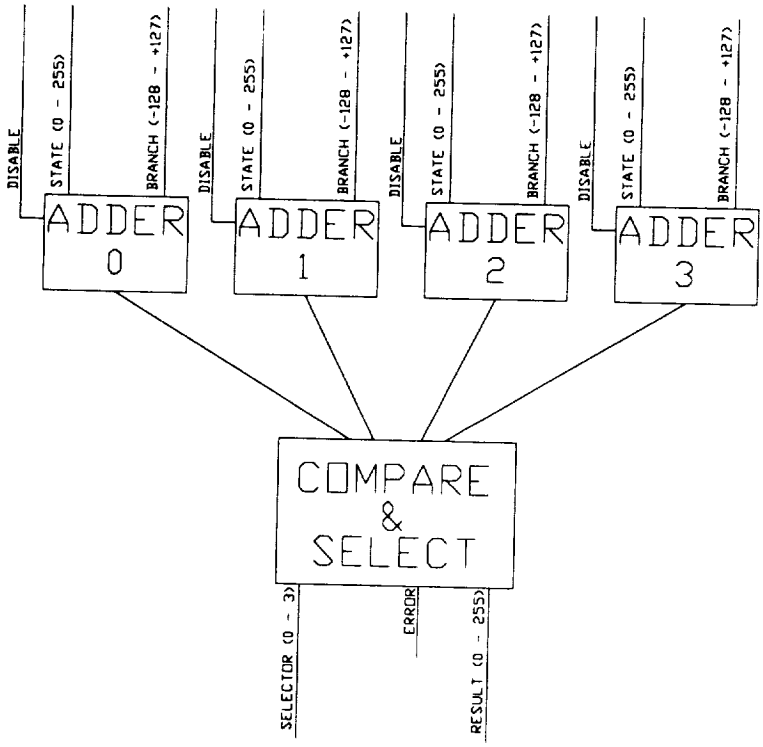


State Metric Calculator Block Diagram.

Each ACS unit has four high speed adders operating in parallel which add the state metric input values to the corresponding branch metric input values. These four path metrics are then compared and the minimum is chosen and sent to the output of the device as the new state metric. The comparison is performed by six comparators, which perform all pairwise comparisons of the four path metrics in parallel. The selection is performed by two levels of basic gates which operate directly from the comparator outputs. The ACS unit also provides a binary output indicating which of the four input branches was chosen. The ACS unit operates at the symbol rate.

The AMTD Rate 8/9 decoder was originally designed with an ACS unit that was fabricated as a high speed ECL hybrid circuit containing 22 100K ECL devices with two-level metal interconnect, controlled impedance lines, and thin film terminations.

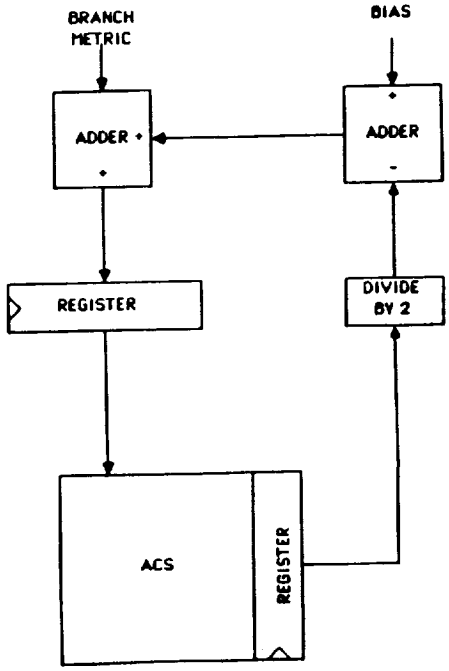
A recent modification to the AMTD Rate 8/9 decoder included the conversion of the ACS unit design into a monolithic high speed ECL gate array. This new ACS unit will be incorporated into the state metric calculator and will improve the overall power consumption of the system, as well as provide greater timing margin to this time critical portion of the system.



ACS Unit Block Diagram.

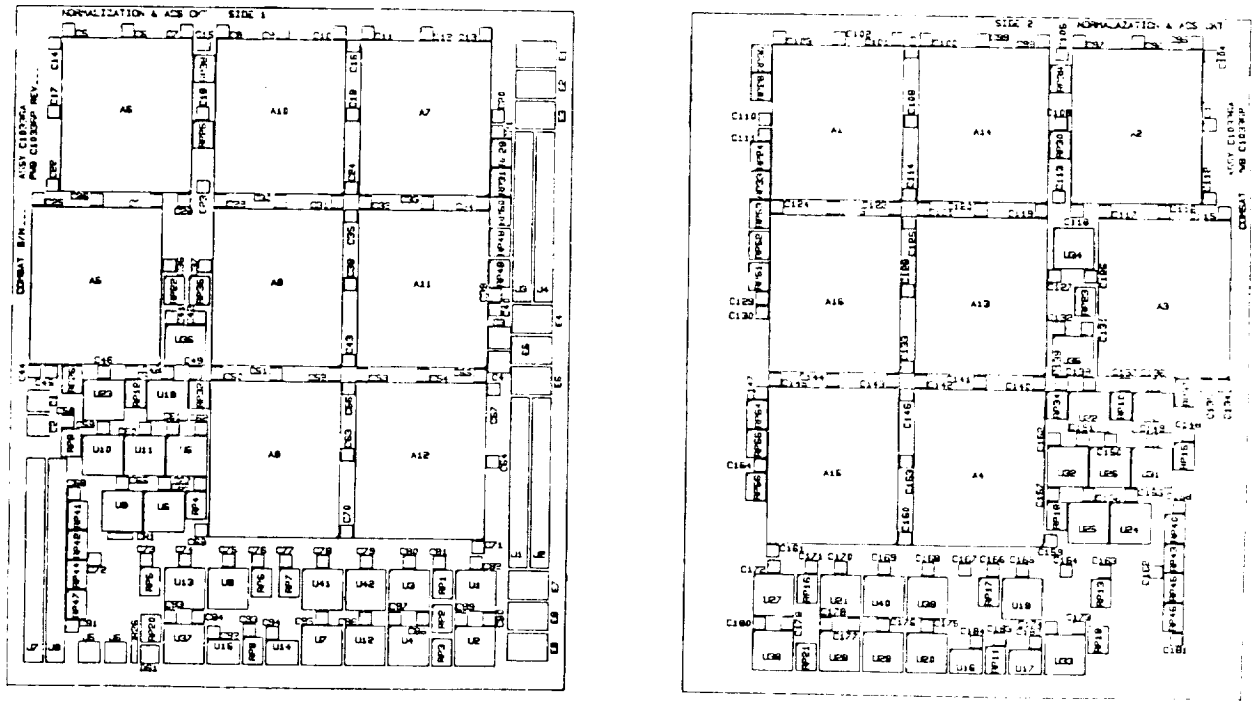
The state metrics accumulated by the ACS units would naturally tend to grow larger in value over time, eventually overflowing the finite arithmetic capacity of these units if some precautions were not taken to prevent it. A commonly used technique to prevent overflow subtracts some value from all of the state metrics periodically. This procedure is called normalization. Ideally, the minimum state metric value is found and subtracted from the others, so that the minimum becomes zero, but this is impractical for high speed implementation since the task of finding the minimum from 16 state metrics is quite difficult at high speeds.

In this design, an arbitrarily selected metric is subtracted from the others, a procedure more suited to high speed implementation. This technique is not optimum, since the dynamic range of the state metrics is doubled, but it involves far less hardware complexity than the traditional method. The subtraction is done to the branch metric inputs, rather than in the ACS operation, thus removing the subtraction from the time critical paths, and reducing the number of subtraction circuits required.



Normalization Block Diagram.

The ACS Processor board is a high speed (75 MHz) design that implements the normalization and state metric calculation functions. It incorporates 16 large ACS ECL units in a highly interconnected network. The circuit requires a large surface area while the high speed operation requirement places severe limitations on the length of the interconnecting signal wires. To overcome this problem, half of the parts were placed on each side of a Microwire board so that the surface area that the wires need to traverse is effectively cut in half, thus reducing the length of the wires to a distance which supports the critical operating speed requirement. Microwire technology supports surface mount technology, and provides a controlled impedance environment and reduced signal crosstalk.

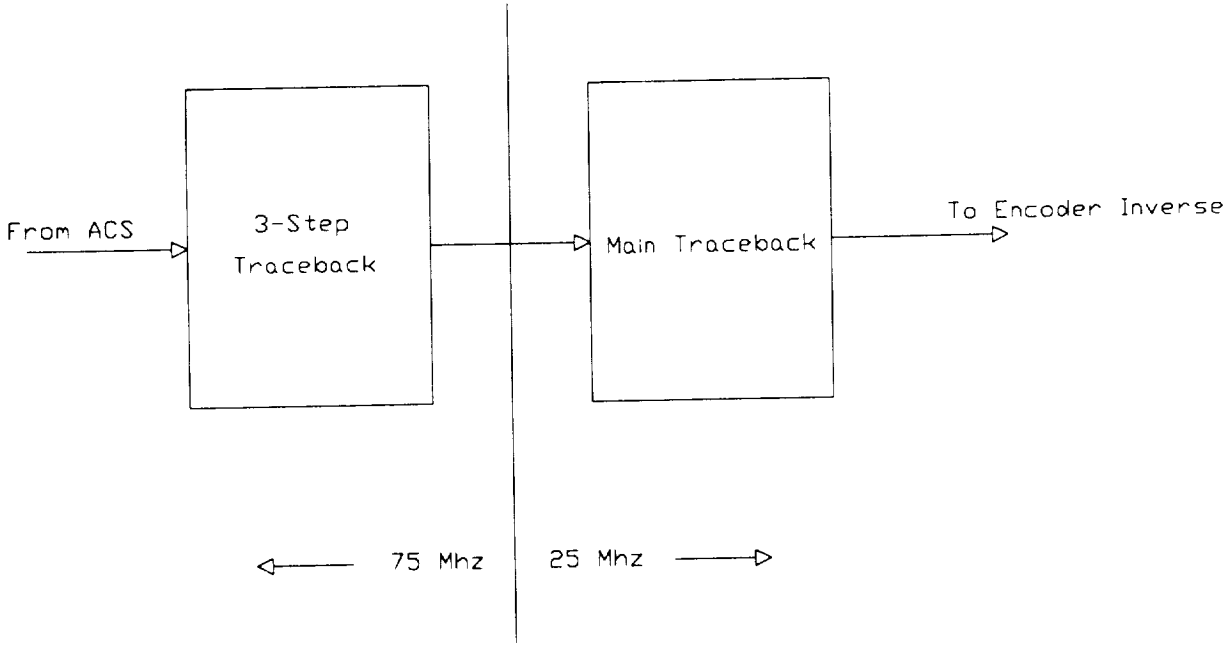


Two-sided ACS Processor Board Layout.

The traceback, or the path memory, is the final step in the decoding process. Starting at an arbitrary state, the most likely path is traced backward in time a finite number of symbols. This gives an estimate of the most likely state sequence, from which the information bits can be derived.

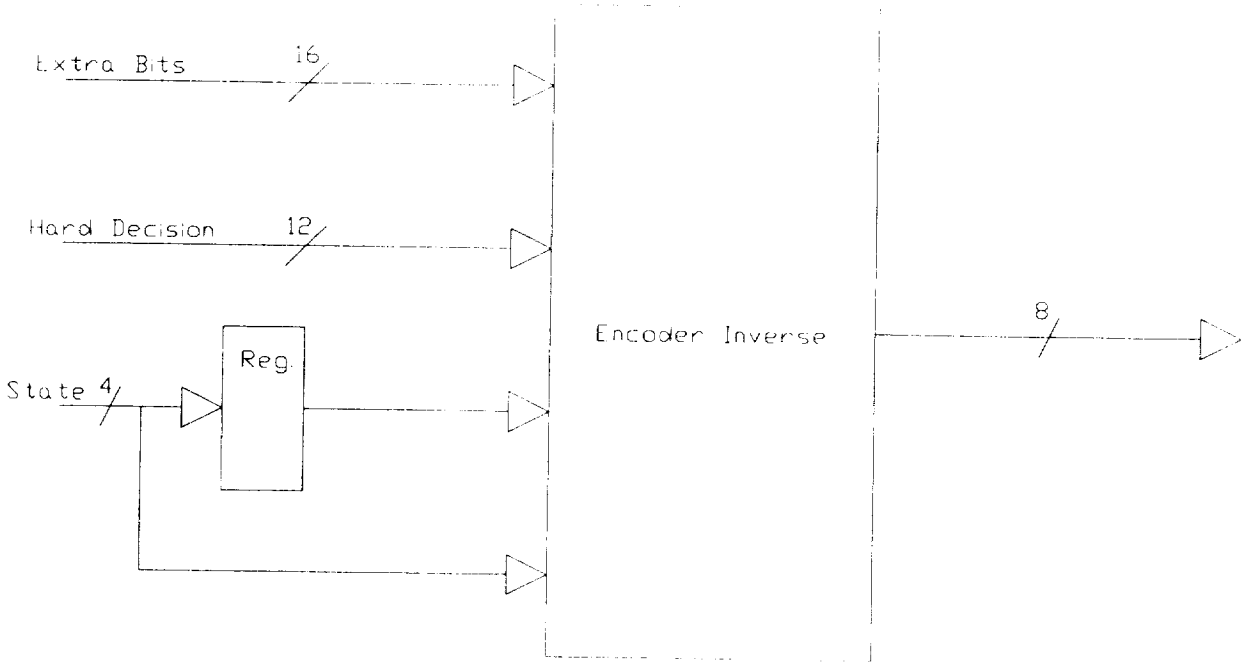
The unique design employed here divides the traceback operation into two stages. The first stage, performed at the symbol rate uses the branch selection outputs from the ACS units. For this process the ACS branch select outputs are transformed into a best predecessor state and processed by the three-step traceback circuits. There are 16 three-step traceback circuits, one for each code state. They have low complexity, and operate easily at the symbol rate. The output of these 16 circuits is the best predecessor to each state over 3 steps. These best predecessor state results are fed to the main traceback, which operates at 1/3 of the symbol rate, allowing the use of TTL and CMOS circuitry.

The main traceback circuit completes the traceback function by finding the best estimate of the sequence of encoder states for some finite path history. This circuit processes three code steps at a time. The unique design not only allows the main traceback to operate at 1/3 of the symbol rate, but it also reduces the number of processing stages by a factor of three. Each stage of the traceback finds the best predecessor state to the state number input to that stage. The main traceback circuit uses a pipelined architecture to perform the traceback in real time.



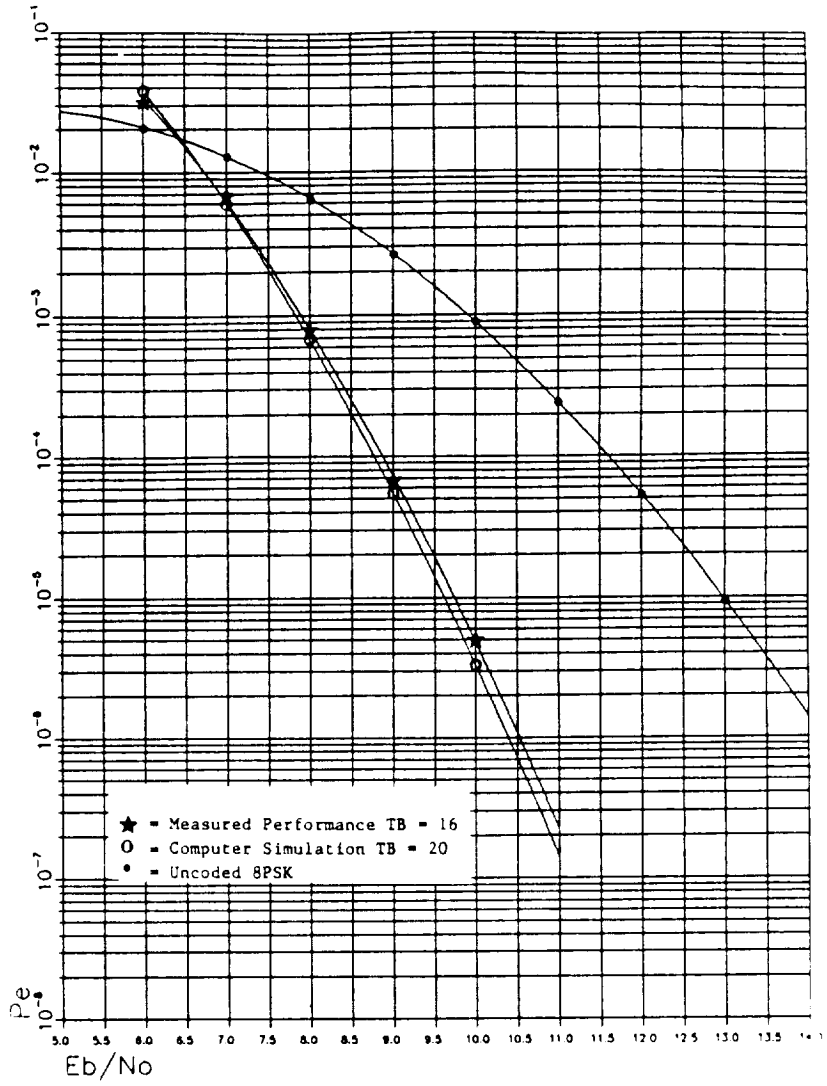
Traceback Partitioning.

The encoder inverse uses the information from the main traceback and the hard decision memory to derive the best estimate of the information bits. The coded bits are obtained from the estimate of the encoder state sequence by combinatorial algebraic processing. The encoder inverse uses the state sequence to select the appropriate bits from the hard decision memory, which gives the estimate of the uncoded information bits.



Encoder Inverse Block Diagram.

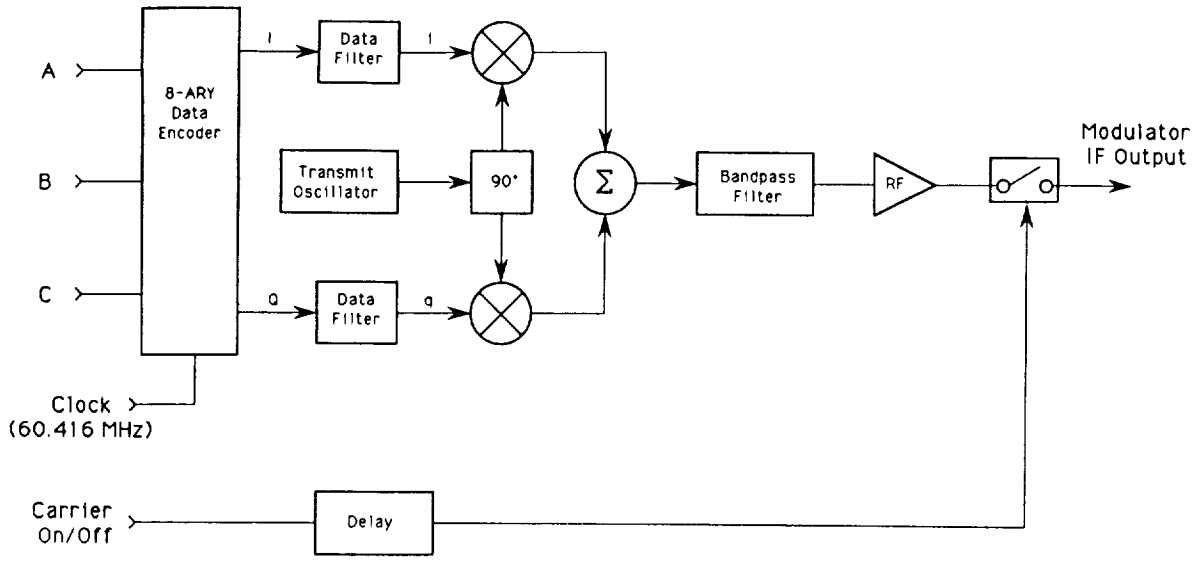
Performance of the rate 8/9 Viterbi decoder was measured at an operating frequency of 75 MSPS using a specially developed digital noise test set which simulated an AWGN channel with an ideal modem. As shown in the performance curve, the rate 8/9 time-varying convolutional decoder is capable of providing a BER of 10^{-6} at an Eb/No of 10.6 dB, assuming a perfect modem. This compares favorably with uncoded 8PSK which requires approximately 14 dB to give the same error rate performance.



BER for Rate 8/9 Codec Over AWGN Channel.

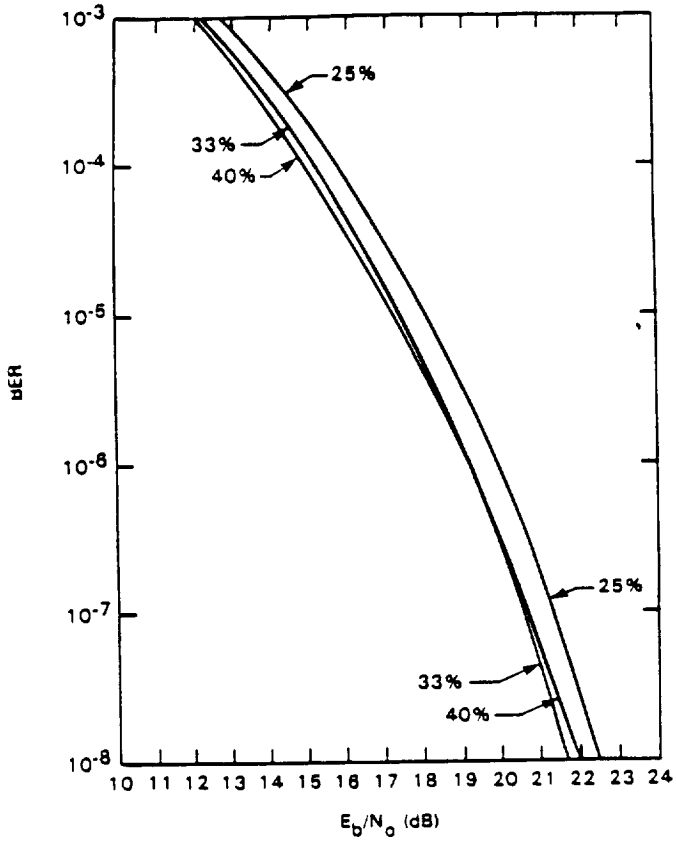
8-PSK MODULATOR

The 8-PSK modulator receives the three bits from the encoder and maps these bits into the proper level to obtain the correct carrier phase. This results in one of four levels which appear at the I and Q channel data filter inputs. These four level signals are filtered with a square root 40% raised cosine filter which also employs x/sinx equalization. These signals then modulate quadrature components of the IF carrier. The signals are then combined, filtered, amplified and passed through an IF switch used for burst mode operation.



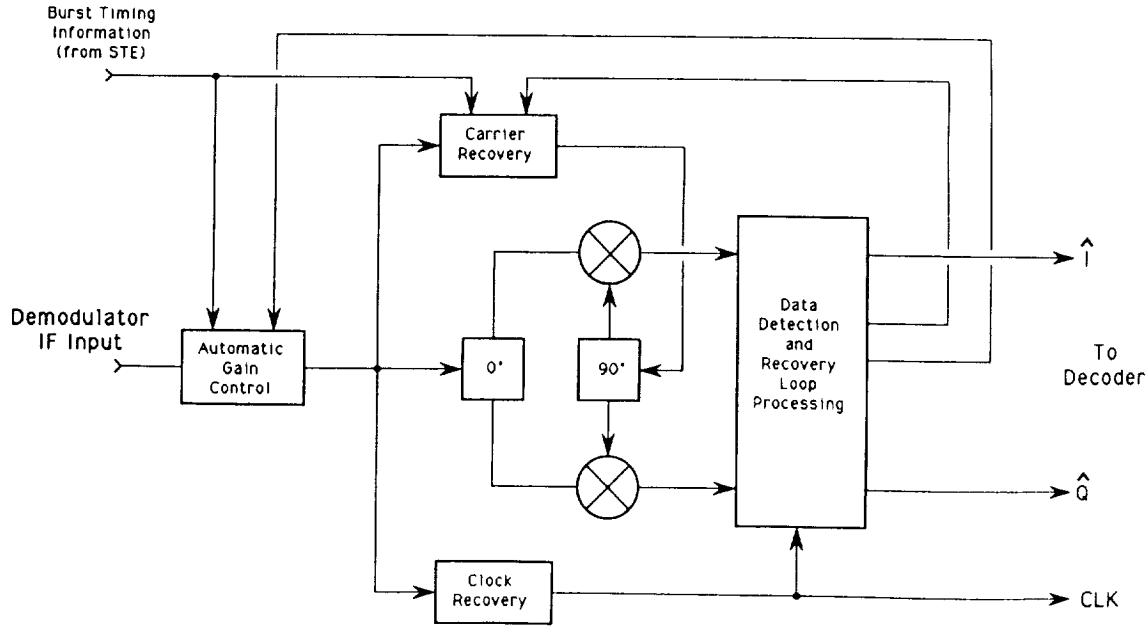
DATA FILTER ROLLOFF SELECTION

Selection of the data filter rolloff characteristics for the coded 8-PSK system was based on computer simulations through a nonlinear channel with adjacent channel interference. Assuming a code rate of 8/9 and an information rate of 200 Mbit/s, the resulting 8-PSK symbol rate is 75 Msymbols/s. The adjacent channels are assumed to be at 100 MHz spacing to give the required 2 bits/s/Hz bandwidth efficiency. Results of BER vs Eb/No performance simulations of the 8-PSK modem under these conditions with raised cosine filters of varying rolloffs is shown below. The choice is between 33% and 40% rolloff, since each performs better in one segment of the Eb/No range. The 40% rolloff filter was selected due to ease of implementation and its slightly better performance in the range of Eb/No where actual operation is anticipated.



OVERALL DEMODULATOR BLOCK DIAGRAM

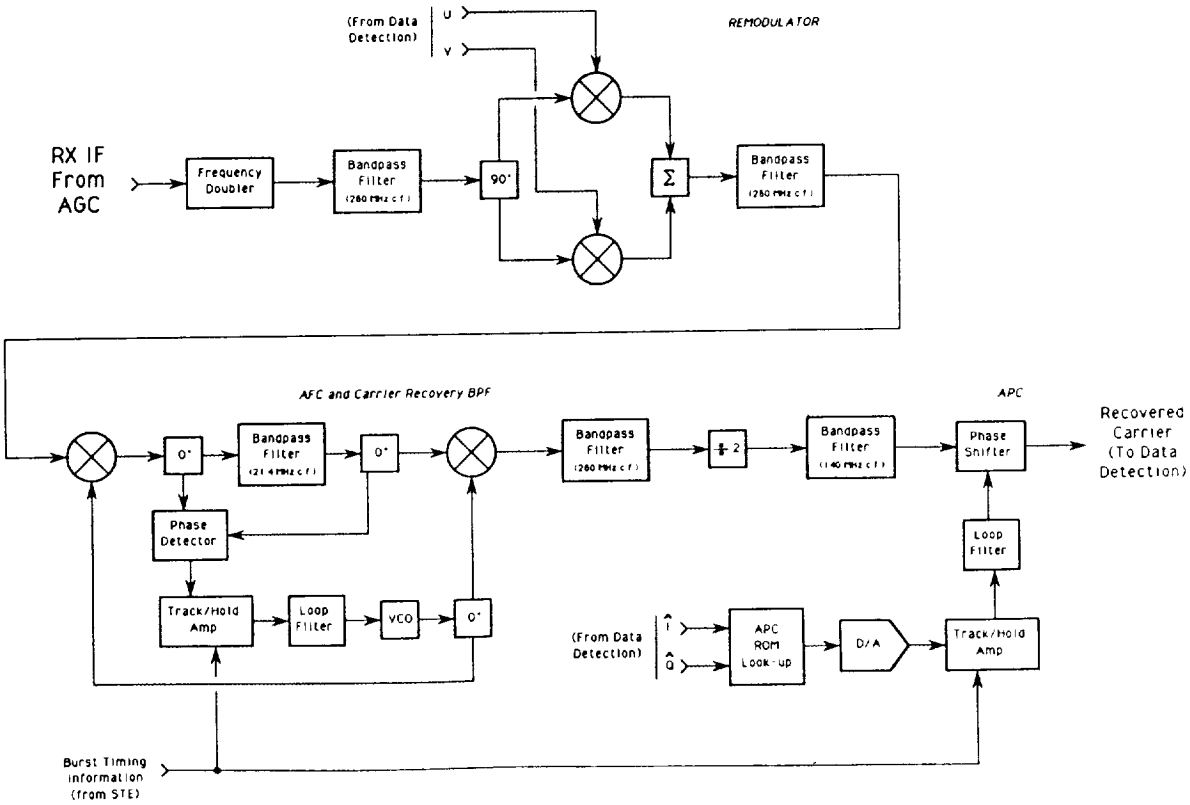
The demodulator receives the incoming IF signal at 140 MHz, removes level variations through the use of automatic gain control (AGC), recovers the carrier and clock references, demodulates the 8-PSK signal into quadrature paths, and provides 5 bit soft detected data to the decoder. Burst timing information for the various demodulator functions is received from the special test equipment. The major components of the demodulator are shown in the block diagram below and will be detailed further in the following charts.



CARRIER RECOVERY FOR 8-PSK

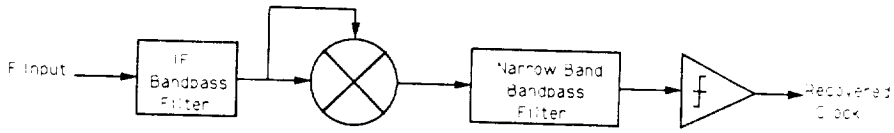
The carrier recovery circuit shown in block diagram form below, must recover a replica of the transmitted unmodulated carrier from the 8-PSK spectrum with low phase jitter. The circuit must be capable of operation in burst mode and handle IF frequency offsets of ±25 KHz. Additionally, the stability of the absolute phase reference must be maintained to a high degree due to the sensitivity of 8-PSK to phase offsets.

The basic principle of operation for the carrier recovery is a modified decision feedback structure. The incoming IF is first doubled, which maps the eight phase states of the signal into only four phase states. This greatly simplifies the decision feedback implementation, since the multipliers are now ±1 rather than the 8-PSK values of ±0.383 and ±0.924. Once the modulation is removed, the signal is passed through a narrow band filter embedded in an automatic frequency control (AFC) loop. The AFC is used to keep the recovered carrier signal in the center of the filter passband thereby reducing phase offsets due to frequency variations. The AFC loop functions in a track and hold mode for burst operation. After division by two, the phase of the carrier reference is adjusted by an automatic phase control (APC) circuit which monitors the receive eye patterns and maintains the phase at the correct value. The APC also operates in burst mode via a track and hold circuit.



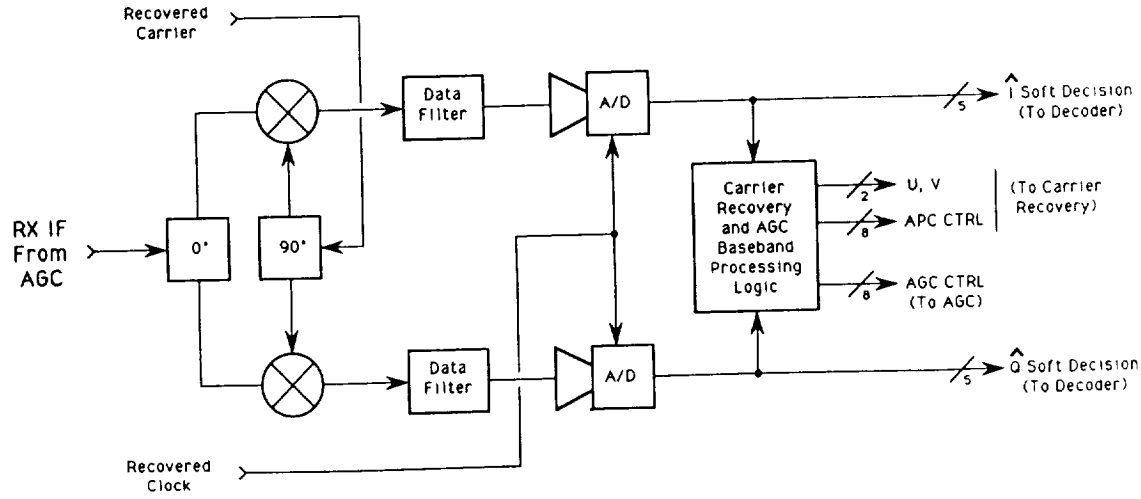
SYMBOL TIMING RECOVERY

Symbol timing recovery is accomplished by taking advantage of the envelope fluctuations introduced by bandlimiting of the 8-PSK signal. After bandpass filtering, the IF is frequency multiplied by two and the clock component extracted by the narrow band filter. An ECL comparator then converts the signal to the proper ECL level for distribution to the data detection circuits.



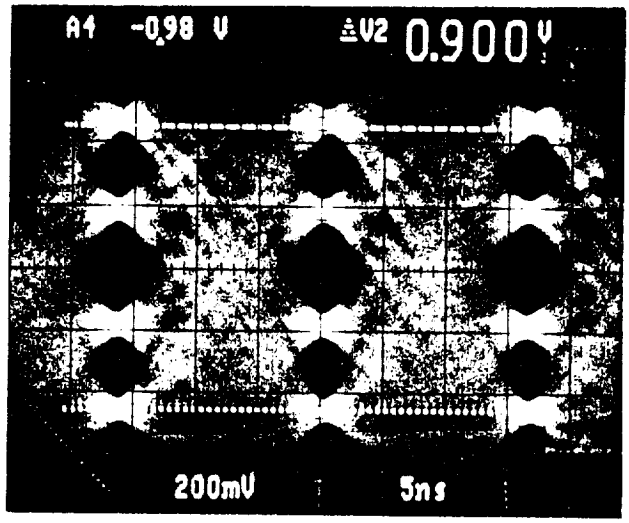
DEMODULATION AND DATA DETECTION

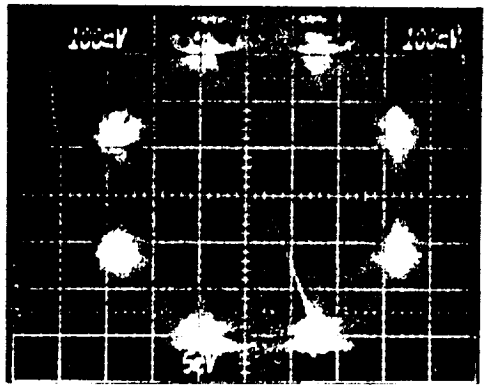
The demodulator shown in the block diagram below first separates the data into two quadrature paths using the recovered carrier. The resulting baseband signals are filtered by square root 40% raised cosine filters to obtain the multilevel eye patterns and then sampled by a 6 bit flash A/D converter. These digitized waveforms are then processed to obtain the U and V decision feedback values as well as the AGC and APC control values. The five most significant bits are passed to the unique word detector for unique word detection and phase ambiguity removal before entering the decoder



RECEIVE EYE PATTERNS AND PHASE STATE SCATTER DIAGRAM

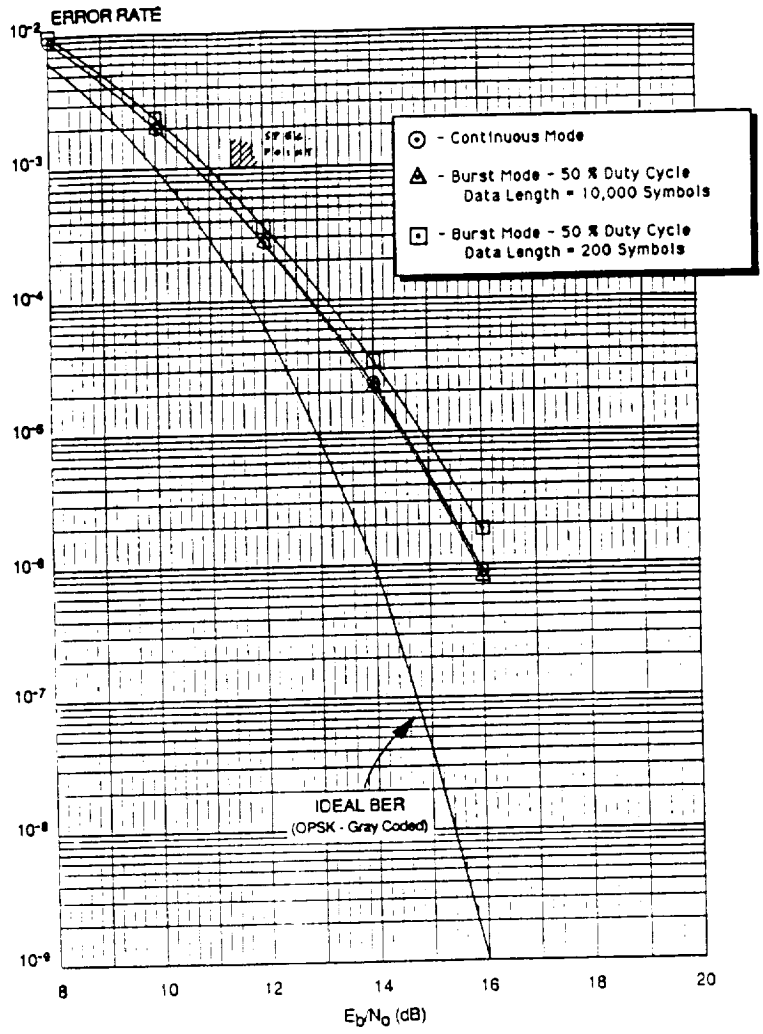
The top photo below shows one of the two receive eye patterns from the 8-PSK modem. Also shown is the phase state scatter diagram which was obtained using the receive eye pattern test points to drive the horizontal and vertical inputs of a high speed oscilloscope.





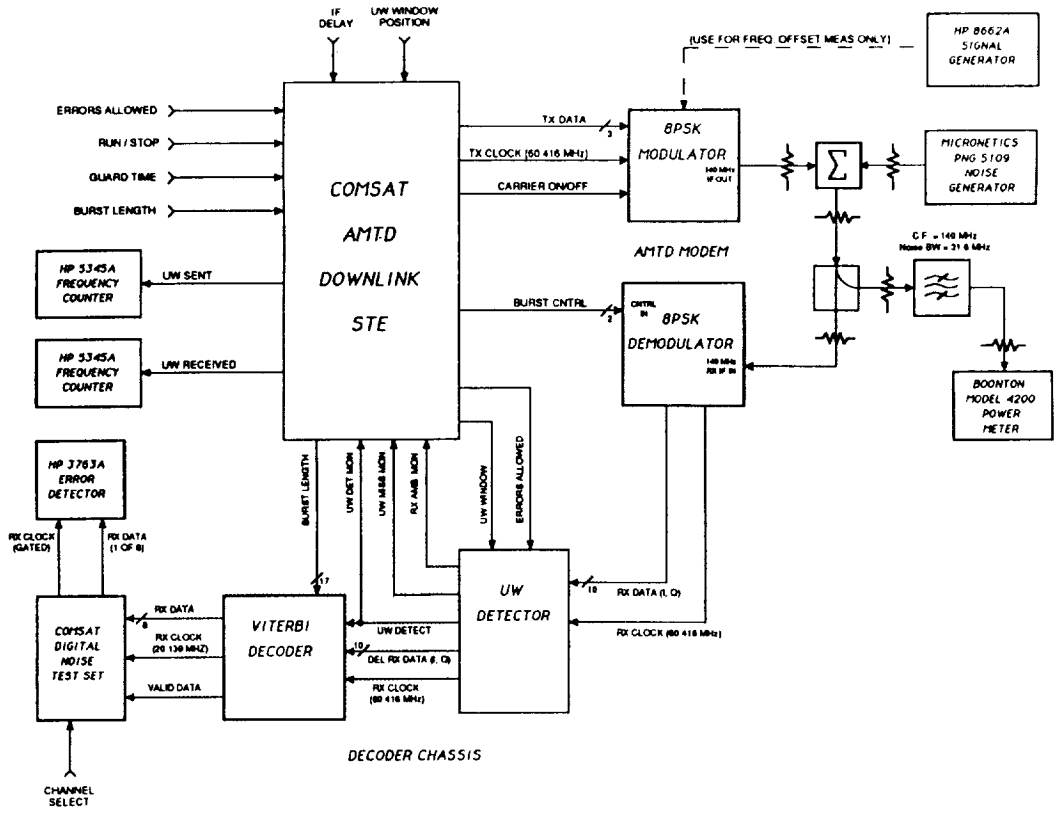
MODEM SELF TEST BER PERFORMANCE

Performance of the modem hard decision BER is shown in the curves plotted below. Data was taken for continuous mode, and burst mode with long and short bursts. Also shown for reference is the 8-PSK ideal performance curve.



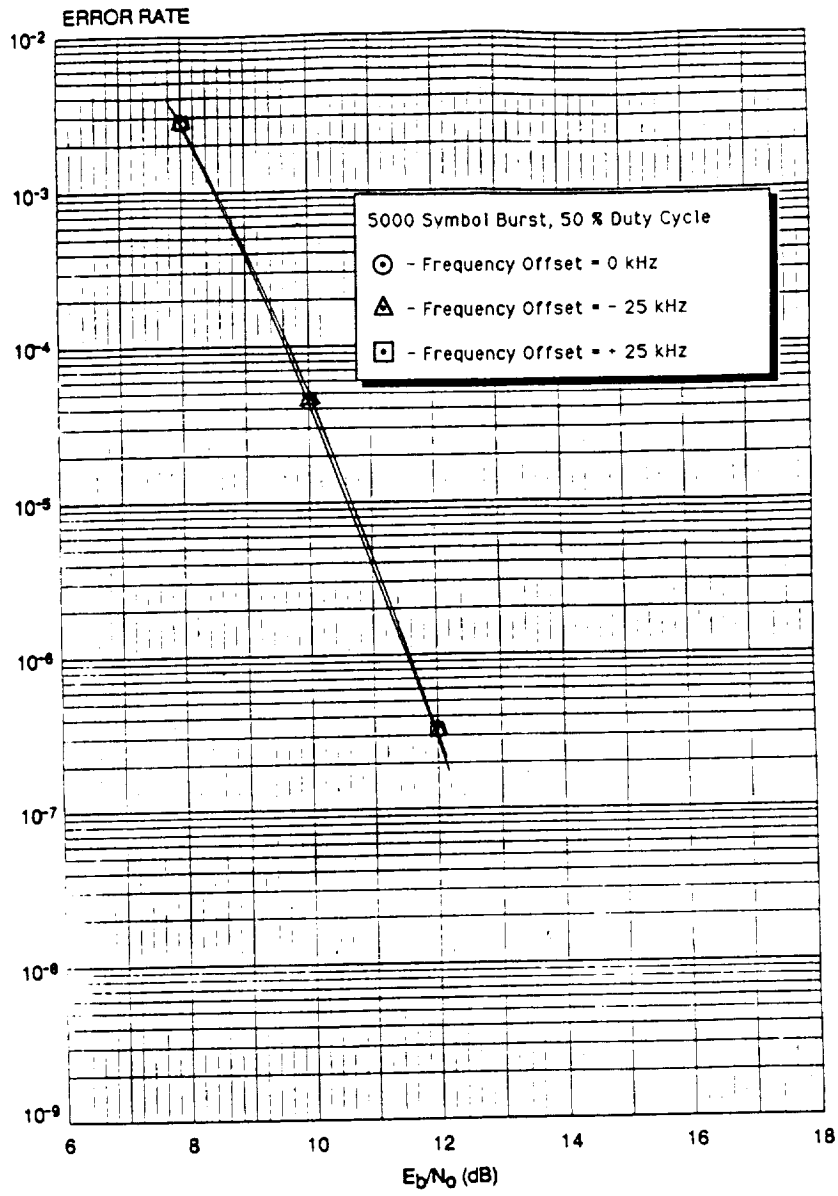
CODED SYSTEM BER AND UW MISS TEST SETUP

Performance of the coded 8-PSK system was measured using the test setup shown below. Data for the eight parallel 20 Mbit/s channels were generated in the STE which also encoded the data. Noise was added at the IF and the C/N was then measured using a separate calibrated filter. BER was measured at the decoder output on one of the eight received channels by the HP BER receiver. The digital noise test set was used for convenience to select which of the channels was to be measured. Unique word misses and bursts transmitted were measured using standard frequency counters for determination of unique word miss rate.



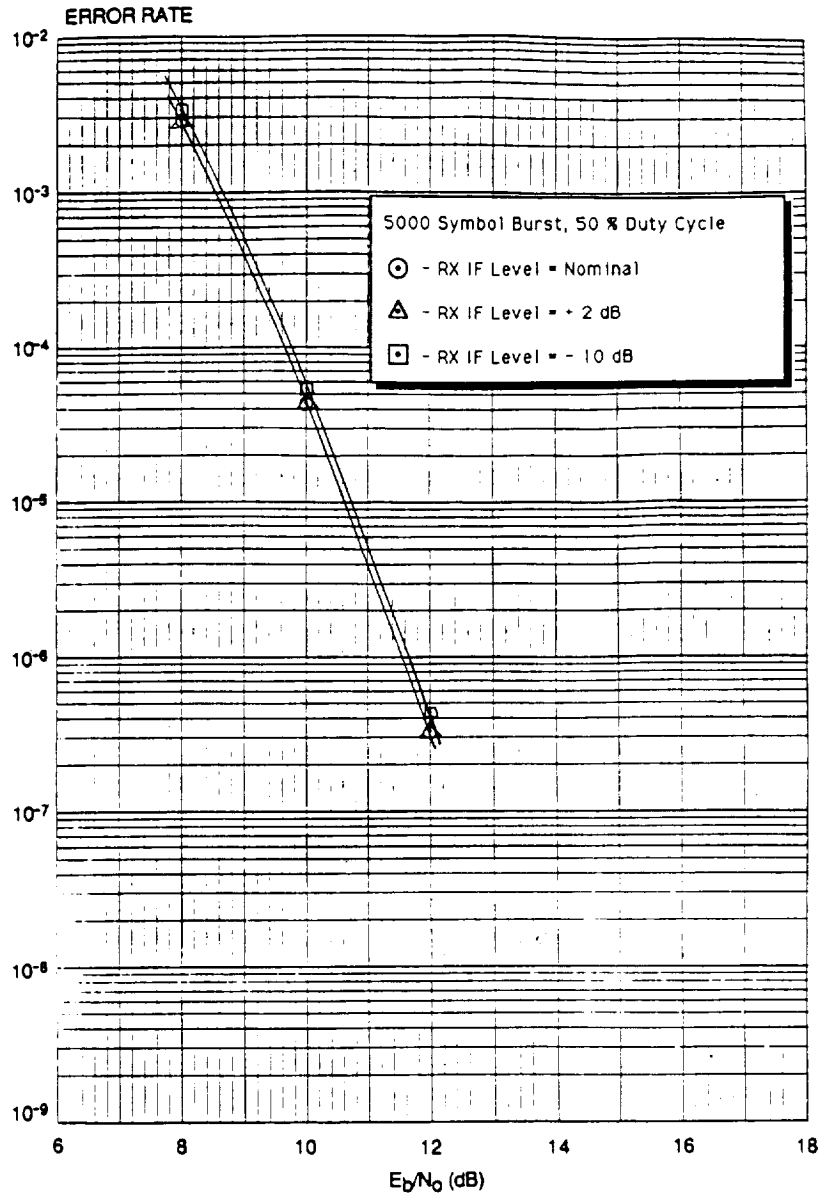
BER vs. E_b/N_o WITH FREQUENCY OFFSET

BER vs Eb/No Performance of the coded system is shown below for frequency offsets of zero and ±25 KHz. Frequency offset of the IF signal can result in phase offsets in the carrier recovery loop if left uncorrected.



BER vs. E_b/N_o WITH IF INPUT LEVEL VARIATION

BER vs Eb/No performance of the coded system with input IF level variation over the specification range is shown in the figure below. In general, 8PSK will be more sensitive than QPSK to level variations due to the multilevel nature of the quadrature eye patterns.



CODED SYSTEM BER PERFORMANCE

The curves below illustrate the overall coded system BER vs Eb/No performance in an AWGN channel for nominal and worst case operating conditions. Also shown for comparison is the codec performance data taken using the codec digital noise self test setup. As can be seen from the figure, the modem introduces approximately 1 dB of implementation loss.