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CODED 16-CPFSK FOR DOWNLINK APPLICATIONS

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ABSTRACT

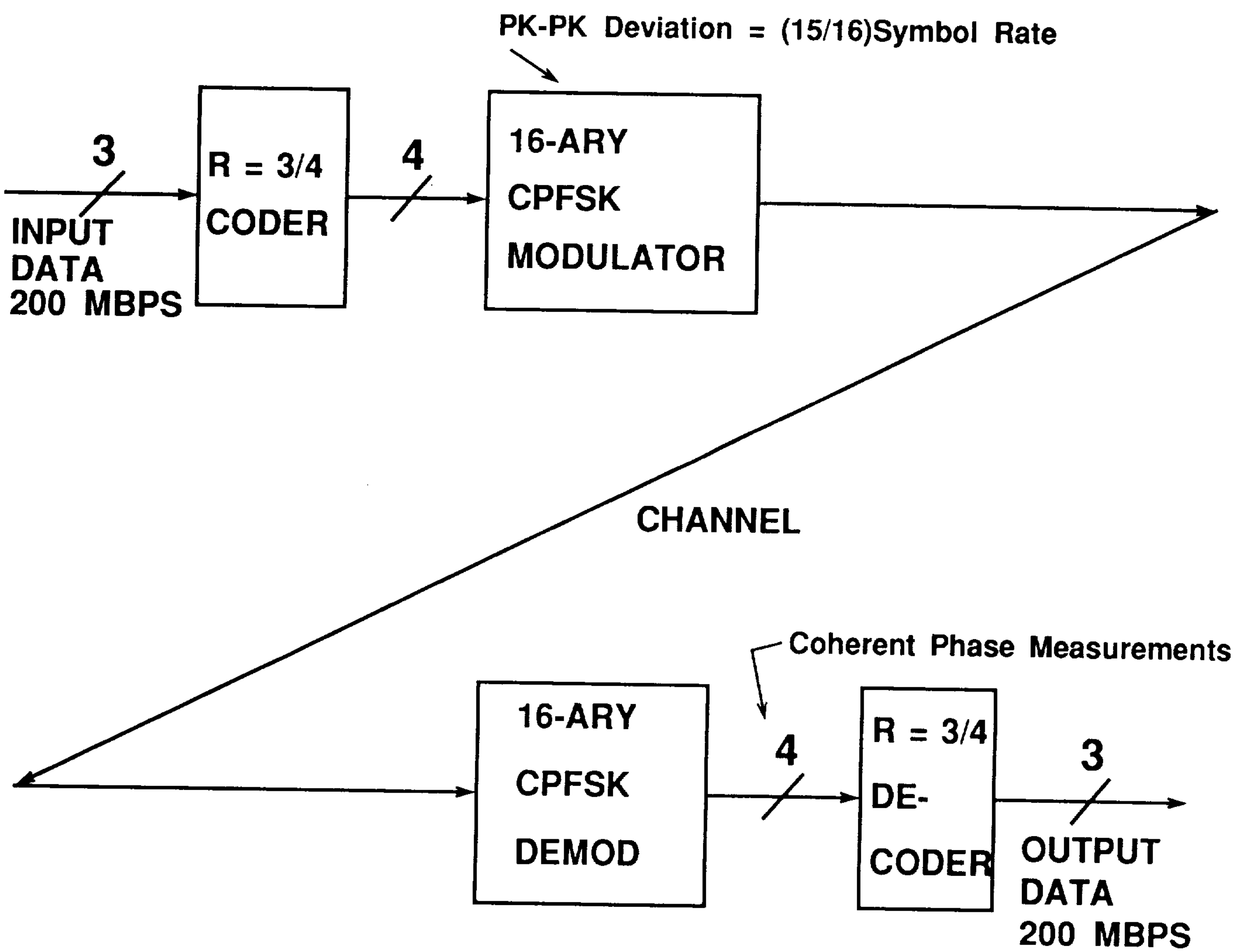
We describe a bandwidth-efficient constant-envelope Proof-of-Concept (POC) modem developed on an Advanced Modulation Techniques Development contract for NASA/Lewis Research Center. The POC modem employs 16-ary Continuous Phase Frequency Shift Keying (16-CPFSK) modulation. The 16 frequencies are spaced every 1/16th baud rate which produces a compact spectrum allowing 2 bits/sec/Hz operation. The modem is designed for 200 mb/s TDMA application with 100 mHz adjacent channel spacing. Overall rate 3/4 convolutional coding is incorporated. The demodulator differs significantly from typical quadrature phase detector approaches in that phase is coherently measured by processing the baseband output of a frequency discriminator. Baud rate phase samples from the baseband processor are subsequently decoded to yield the original data stream. The method of encoding onto the 16-ary symbol-ending phase nodes, together with convolutional coding gain, results in near QPSK theoretical performance. The modulated signal is of constant envelope; thus the power amplifier can be saturated for peak performance. The spectrum is inherently bandlimited and requires no RF filter for sidelobe containment. Two novel theoretical techniques are used in this 16-CPFSK modem: I) Coherent phase measurements are obtained by processing an FM discriminator baseband output; II) Modulation is accomplished via a closed-loop-linearized VCO.

*Work performed for NASA/Lewis Research Center on Contract NAS3-24681

BASIC BLOCK DIAGRAM OF MODEM

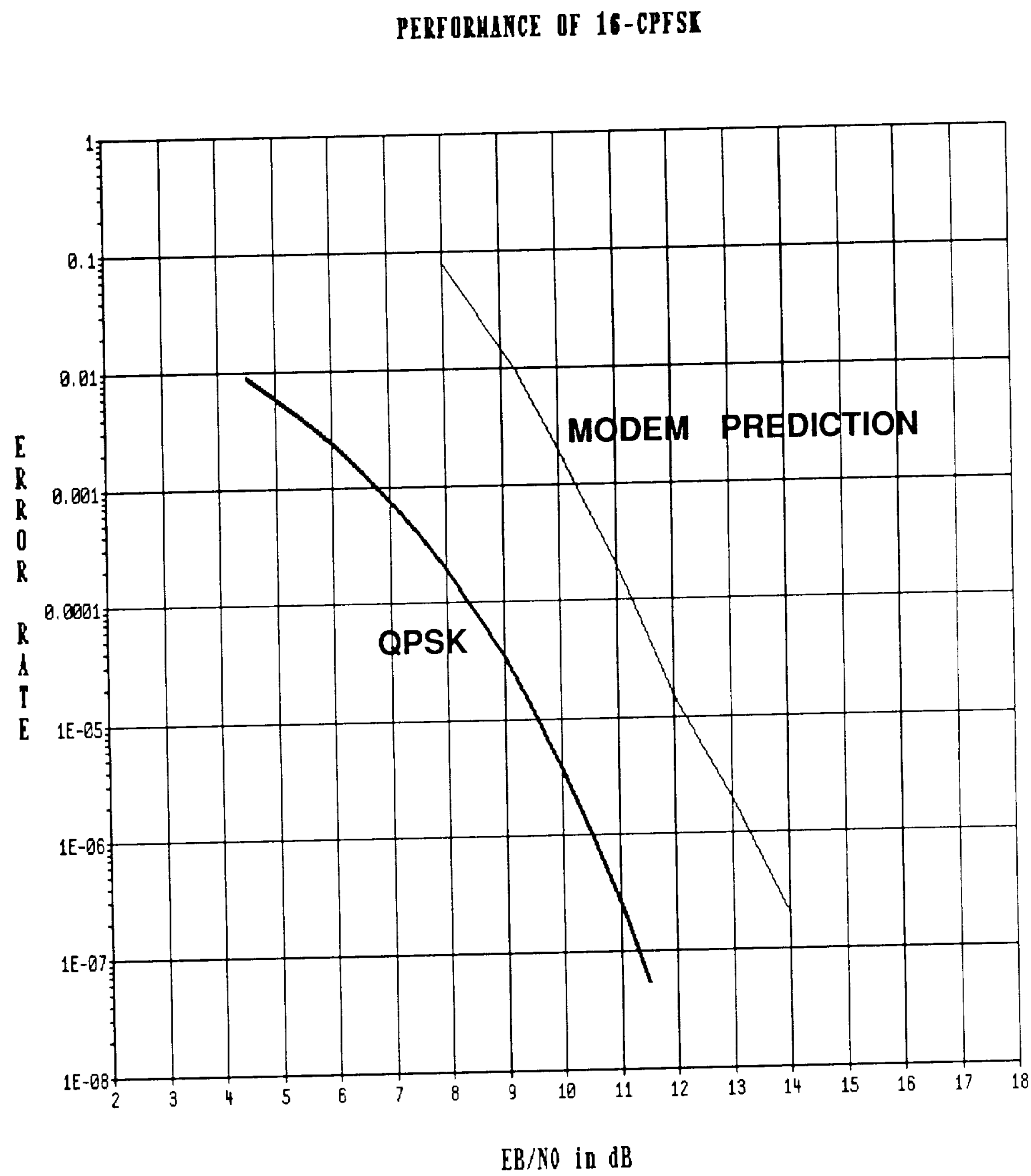
This figure shows a very basic level block diagram for the 200 Mbps TDMA modem Proof-of-Concept modem investigated by Harris Corporation on the Advanced Modulation Technology Development contract with NASA/Lewis Research Center.

BASIC MODEM BLOCK DIAGRAM



MODEM ERROR RATE PERFORMANCE

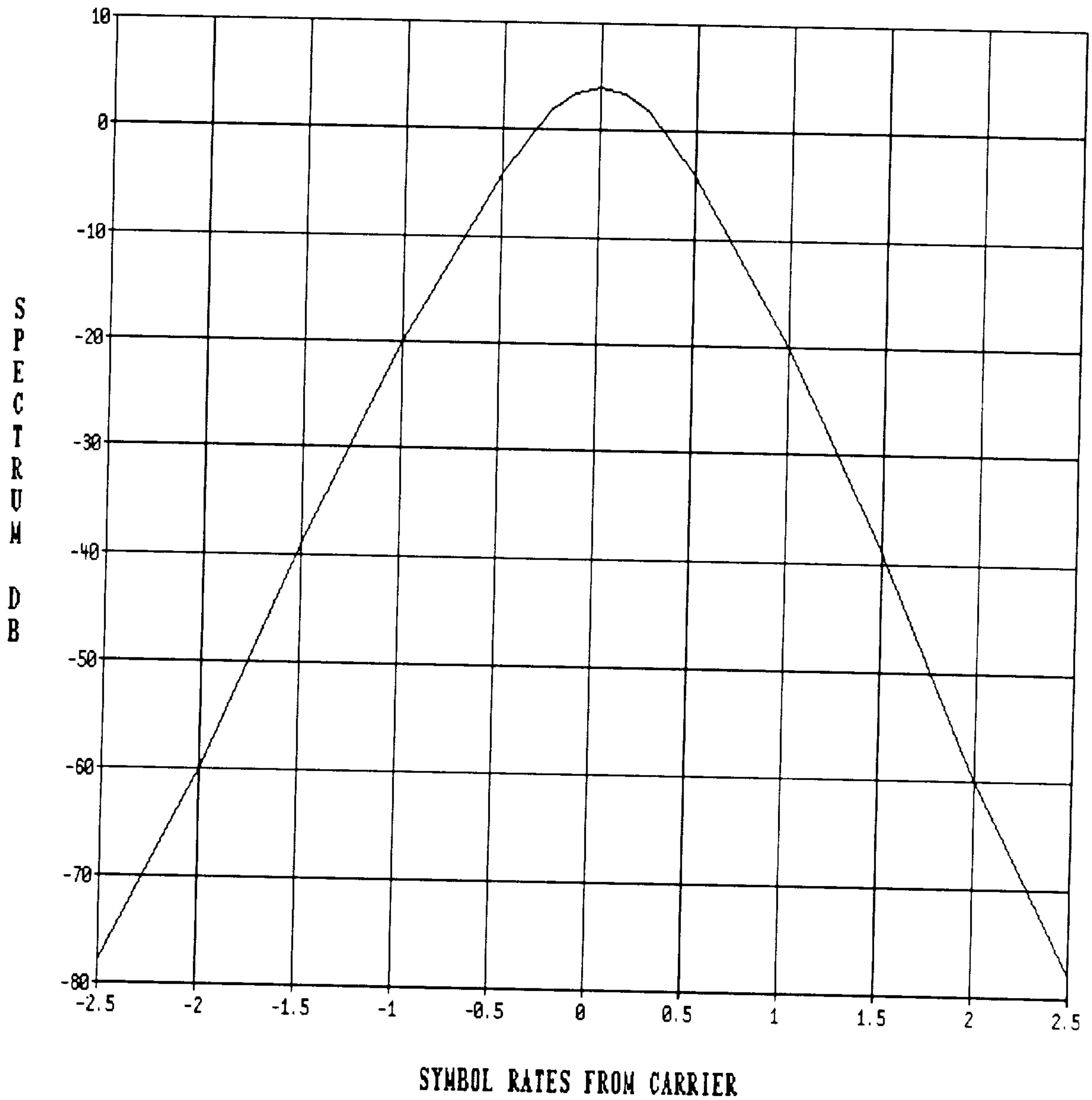
The figure shows the Bit Error Rate Performance predicted for the Harris TDMA Modem compared to QPSK performance.



MODEM SPECTRUM

Here is the spectrum for the Harris 200 Mbps TDMA Modem. The symbol rate is 72.73 MHz.

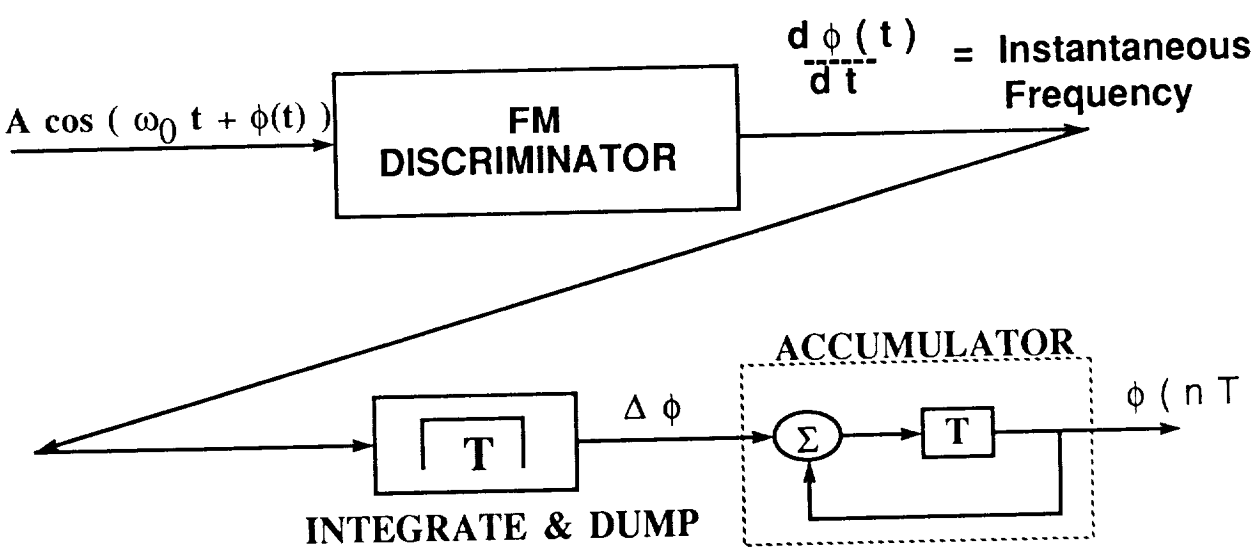
SPECTRUM OF BASEBAND FILTERED 16-CPFSK



OBTAINING COHERENT PHASE FROM A DISCRIMINATOR.

A discriminator outputs ϕ't) where $\phi(t)$ is the signal's phase modulation. Integration of ϕ't) recovers the desired signal, $\phi(t)$. Implementation of the integration has several practical problems: 1) Integrator output can grow without bound; 2) Initial phase, $\phi(0)$, must be determined; 3) AGC is needed on the baseband signal. Regarding problem 1), fortunately, we need only know phase Mod-2π. Thus the growth problem is avoided by integrating Mod-2π. How can such an integrator be implemented? It is essential only that we obtain $\phi(nT)$, phase at baud time intervals. An integrator yielding $\phi(nT)$ can be implemented as a T-interval Integrate-and-Dump (I&D) sampled by an A/D which feeds a digital accumulator that rolls over Mod-2π. The I&D is actually a lowpass Half-Nyquist filter in this modem, but the conceptual picture remains useful.

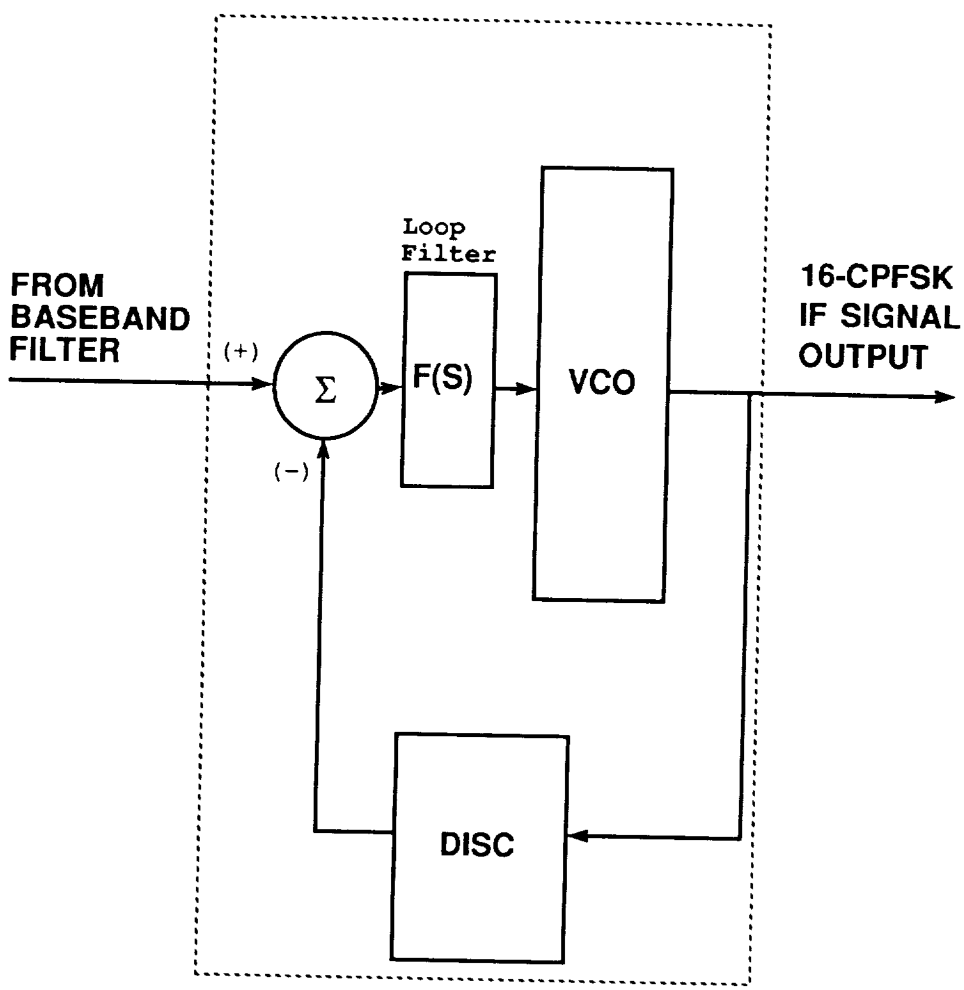
Problem 2)--acquiring initial unknown phase, $\phi(0)$, is handled by first observing for each baud time, the phase error to the closest one of the 16-CPFSK phase nodes (Mod-2π) equally spaced in the accumulator. This phase error is filtered by a lowpass loop filter whose output is subtracted from the accumulator input. The initial phase error, $\phi(0)$, appears as a DC component of the error and is eliminated by the baseband loop. Frequency offset (DC offset from the discriminator) also is eliminated by this baseband loop, the equations for which are identical to those for a PLL.



LINEARIZED VCO MODULATOR

The figure below shows the closed-loop-linearized VCO modulator. The baseband filter output is applied through a feedback summer to the VCO. F(s) is a wideband loop filter. The output of the VCO is immediately converted back to baseband by the discriminator (DISC) and subtracted from the baseband input modulating signal to generate a correction signal in the closed loop. The VCO is thus modulated with small error between the baseband modulating signal and the output of the DISC. If the modulator DISC is identical to the demod DISC, this modulator linearizes the baseband signal path through the modem's VCO/DISC combination.

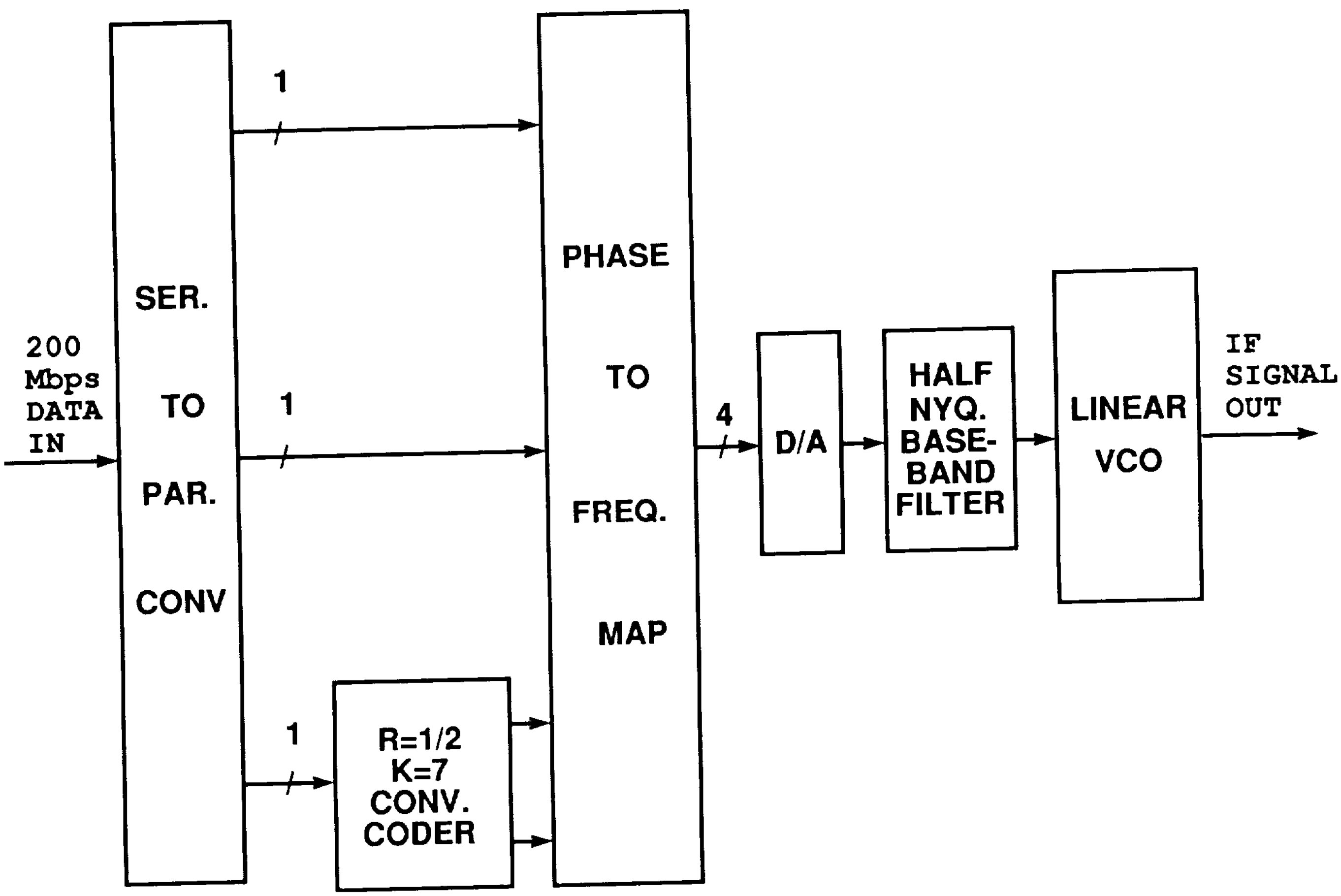
LINEARIZED VCO



BRIEF DESCRIPTION OF MODULATOR OPERATION

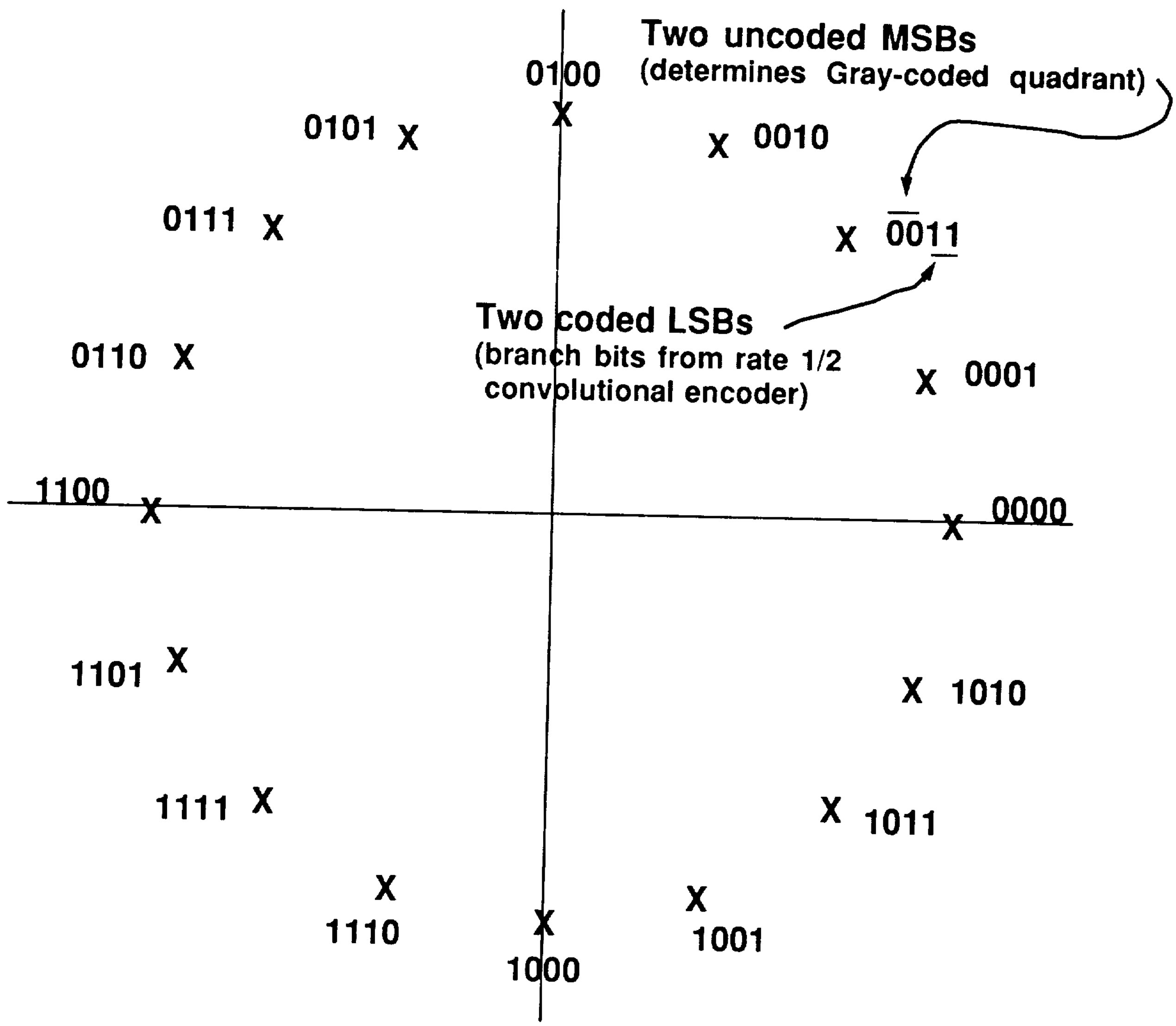
As shown in the figure below, incoming data is split into 3 parallel bit streams. The 2 MSBs are passed unaltered to modulator MSB positions. The LSB bit stream is coded by a rate 1/2, K=7 convolutional encoder. The 2 resulting coded branch bits go to the 2 LSB positions of the modulator. The 4 bits produced by this encoding process specify one of 16 symbol-ending phases (Mod-2π) from the 16-CPFSK modulator. Half-Nyquist filtering is employed at the VCO baseband on 16-ary impulses to produce the IF signal at the modulator.

BASIC MODULATOR BLOCK DIAGRAM



16-CPFSK PHASE NODES AND CODING STRATEGY

The figure below shows the 16-CPFSK symbol-ending phase nodes, along with the mapping of coded 4-bit groups onto them. Any set of 4 adjacent phases contains all 4 rate 1/2 code branches and has good distance structure. This fact forms the basis for our decoding strategy, which is: (1) Retain only the 4 phase nodes nearest the received coherent phase measurement; (2) then let the Viterbi decoder determine which of these 4 phases is most likely to have been transmitted; (3) The 2 modulator MSBs (which we call "tagalong bits") associated with the decoder's decision are output as 2 of the decoded bits; (4) The third bit decision is the data bit decision made by the decoder. These 3 bits form the total output data bit stream.

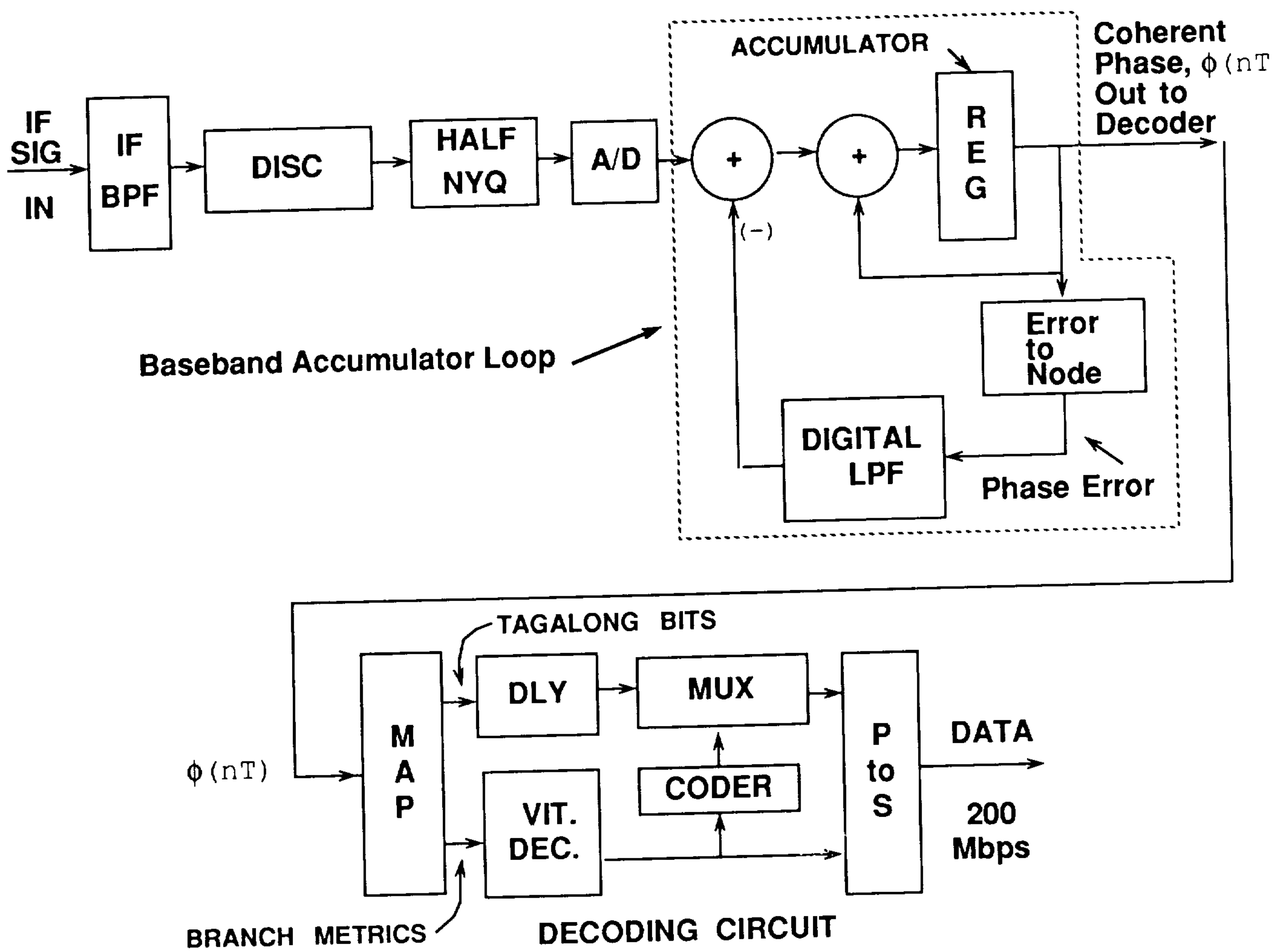


16-CPFSK ENDING PHASES

BRIEF DESCRIPTION OF DEMODULATOR OPERATION

At the demod the IF signal is filtered and passed to the discriminator (DISC). The DISC baseband signal is Half-Nyquist filtered and sampled at symbol rate by an 8-bit A/D. The Half-Nyquist filter completes shaping begun at the VCO, producing an overall Nyquist response to 16-ary impulses from VCO baseband to discriminator baseband. The A/D samples feed the accumulator, whose output is $\phi(nT)$. These coherent measured phase samples feed a Viterbi decoder for demodulation of the original 3 data streams.

BASIC DEMODULATOR BLOCK DIAGRAM



IMPLEMENTATION PROBLEMS

BASEBAND NOISE SOURCES:

Baseband noise sources must be carefully controlled. The A/D Converter's quantizing noise is 42 dB below signal power. To keep other sources of broadband noise small relative to this irreducible quantizing noise, the baseband SNR needs to be 50 dB or greater. At present, our Signal Combiner chassis is a source of unacceptably high levels of broadband noise. We currently are bypassing the Signal Combiner to isolate other problems.

BASEBAND NONLINEAR DISTORTION:

The nonlinearity from VCO baseband input to Discriminator baseband output needs to be 1% or less. For a cubic nonlinearity, this translates to a requirement that Third Order Intermod Distortion (IMD), as measured by a two-tone test, be at least 45 dB down relative to the desired tones.This is difficult to achieve. At one time we had achieved these levels of IMD. After buttoning up some of the equipment into the chassis, the IMD levels rose to 30 to 35 dB down. At this writing we believe we have discovered the source of this problem and we are working to remove it. We believe that this totally unacceptable level of IMD is a major source of our 5x10-3 irreducible error rate.

BASEBAND LINEAR DISTORTION:

With the 16-ary modulation used on this modem, the linear amplitude and group delay distortions must be carefully controlled. By careful adjustments of the baseband filters, we believe this source of difficulty has been largely controlled. The amplitude response is flat to within 0.1 to 0.2 dB and group delay distortion is less than 1 nsec out to the Nyquist band edge.

SUMMARY:

We believe that the major problem we currently are fighting in removing our 5x10-3 error floor is the baseband nonlinearity problem. At one time we had this parameter under control -- having produced -45 dB IMD. Our currently observed -30 to -35 dB IMD is totally unacceptable and we believe we will reduce this again to acceptable levels shortly.

SESSION III

OTHER LEWIS MODULATION AND CODING WORK
CHAIR: J.M. BUDINGER

HIGH SPEED HARDWARE DEVELOPMENT FOR FDMA/TDM SYSTEM
S.C. KWATRA, M.M. JAMALI
UNIVERSITY OF TOLEDO

A CO-DESIGNED EQUALIZATION, MODULATION AND CODING SCHEME
R.E. PEILE
UNIVERSITY OF SOUTHERN CALIFORNIA

MODULATION TECHNIQUES FOR POWER AND SPECTRALLY EFFICIENT SATCOM SYSTEMS
K. FEHER
UNIVERSITY OF CALIFORNIA

PROGRAMMABLE RATE MODEM UTILIZING DIGITAL SIGNAL PROCESSING TECHNIQUES
A. NAVEH
TIW SYSTEMS, INCORPORATED

SESSION III CONTINUED

MULTI-USER SATELLITE COMMUNICATIONS SYSTEM USING AN INNOVATIVE COMPRESSIVE RECEIVER

E.J. STAPLES
AMERASIA TECHNOLOGY, INCORPORATED

FLEXIBLE HIGH SPEED CODEC

R.W. BOYD AND W.F. HARTMAN
HARRIS CORPORATION

PROGRAMMABLE DIGITAL MODEM

M. KAPPES
COMSAT LABORATORIES