N92-22011

PROGRAMMABLE RATE MODEM UTILIZING DIGITAL SIGNAL PROCESSING TECHNIQUES
(SBIR-PHASE 1 CONTRACT #NAS3-25336)

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PROJECT SUMMARY

The engineering development study to follow was written to address the need for a Programmable Rate Digital Satellite Modem capable of supporting both burst and continuous transmission modes with either BPSK or QPSK modulation. The preferred implementation technique is an all digital one which utilizes as much digital signal processing (DSP) as possible. The majority of this report consists of outlining design trade-offs in each portion of the modulator and demodulator subsystem and of identifying viable circuit approaches which are easily repeatable, have low implementation losses and have low production costs.

TECHNICAL AREAS THAT WERE INVESTIGATED UNDER THIS CONTRACT:

- TRANSMIT DSP DATA FILTERS
- TRANSMIT CLOCK SYNTHESIS
- CARRIER SYNTHESIZER
- DEMODULATOR'S AUTOMATIC GAIN CONTROL
- RECEIVE DSP DATA FILTERS
- SATELLITE LINK RF OSCILLATOR PHASE NOISE IMPACT ON CARRIER RECOVERY OF PROGRAMMABLE RATE DIGITAL SATELLITE MODEMS
- MODEM FREQUENCY CONVERSION AND RECEIVE SIDE CARRIER SELECTION
- CARRIER RECOVERY
- TIMING RECOVERY AND DATA SAMPLING

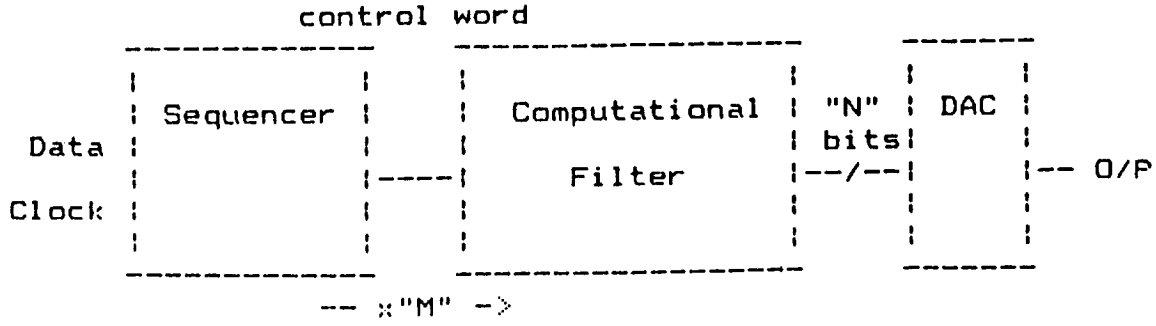


Figure 1. Transmit Data Filter Block Diagram

Table 1. Number of FIR Coefficients Verses Alpha Factor

Classical Alpha Factor	Normalized Transition Width	Number of Coefficients	Coefficients Phase Linear Requirement
1.0	.5	7.0	7
.9	.45	7.8	9
.8	.4	8.8	9
.7	.35	10.0	11
.6	.3	11.7	13
.5	.25	14.0	15
.4	.2	17.5	19
.3	.15	23.3	25
.2	.1	35.0	35
.1	.05	70.0	71

It is apparent by the data tabulated in Table 1 that as more restrictions are placed on the amount of excess bandwidth the DSP filter design must be capable of many more coefficients. It should be noted that Table 1 above is only an estimation and that depending on the values of the coefficients selected and the quantization level of the design that these estimates may need to be increased.

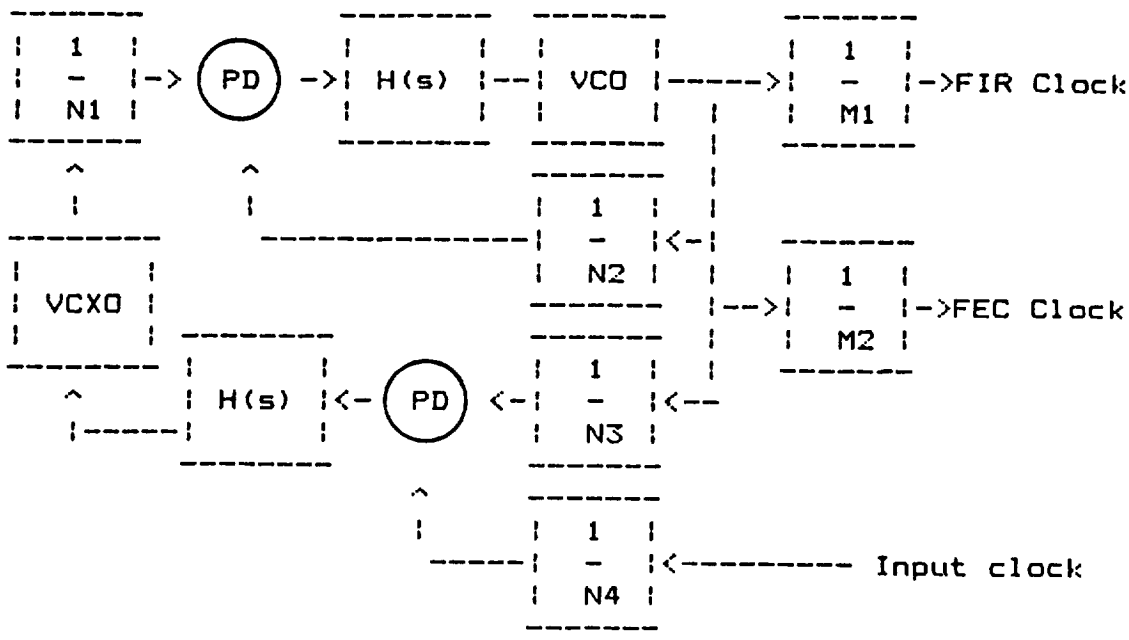


Figure 2. Multiloop Synthesizer for Clock Generation

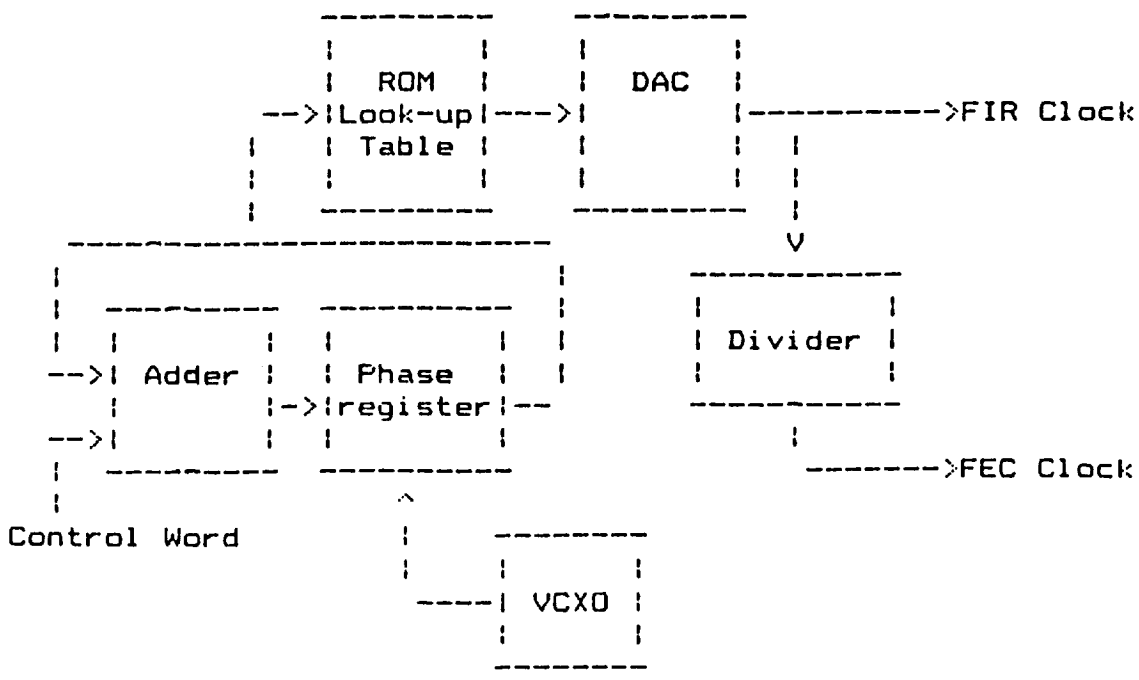


Figure 3. Direct Numerical Synthesis for Clock Generation

DUAL CONVERSION

Another consideration is the method of modulating the carrier frequency. The simplest method is to directly modulate the desired IF carrier. In this method the filtered baseband signal is mixed directly onto the desired carrier and the modulation is complete. A second method, known as dual conversion, uses a two step approach. In the first step the filtered baseband signal is modulated onto a fixed carrier, then in a second step an IF synthesizer is used to frequency translate the modulated spectrum to a particular carrier frequency. Figure __ reveals the modulation process known as dual conversion. Notice that this method requires an additional mixer and oscillator, however it does have advantages over the direct modulation method. One quadrature LO need only to operate at one frequency, therefore the quadrature can be ideal.

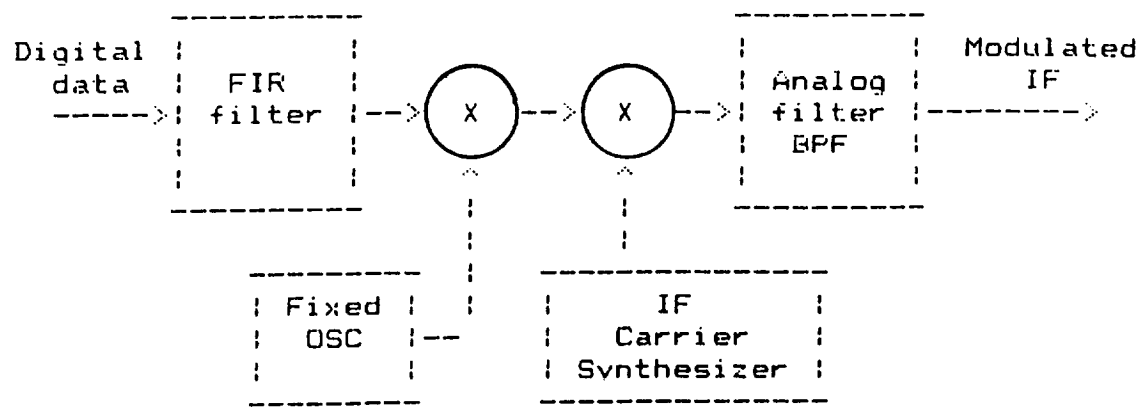
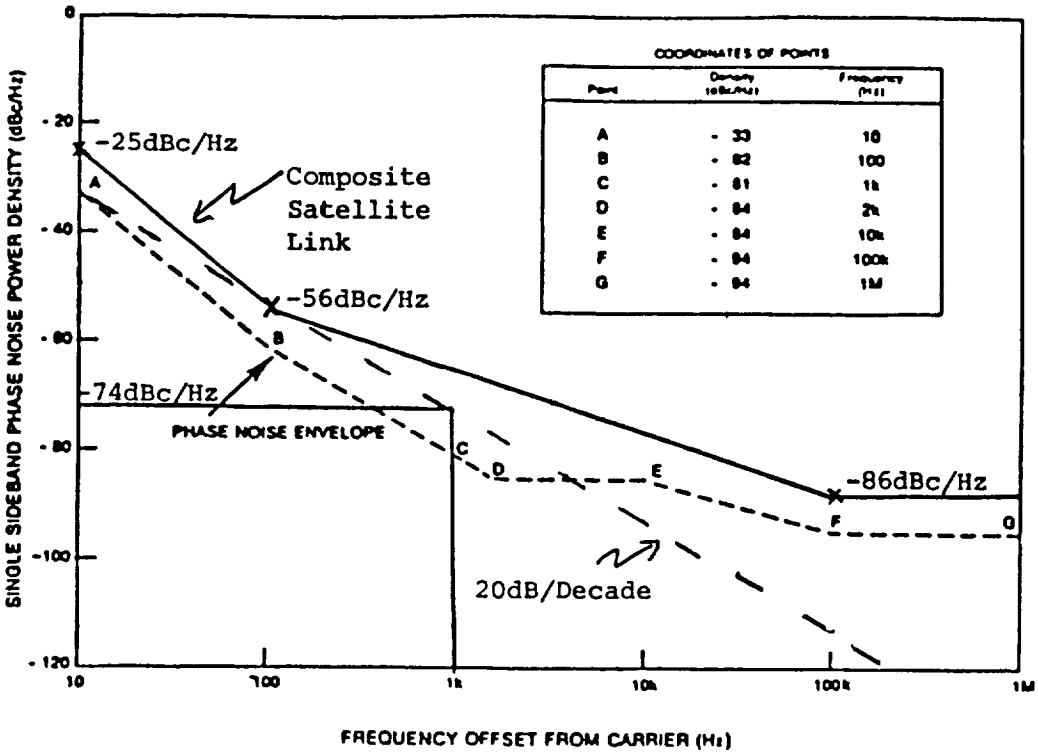


Figure 4. Dual Conversion Frequency Modulation

SATELLITE LINK RF OSCILLATOR PHASE NOISE IMPACT ON CARRIER
RECOVERY OF PROGRAMMABLE RATE DIGITAL SATELLITE MODEM

The carrier recovery network used in coherent demodulation of BPSK/QPSK signals must have sufficient bandwidth to track the phase noise of the down link translated carrier to minimize performance degradations caused by RMS phase error jitter. On the other hand, the larger this bandwidth the less signal to noise improvement, i.e., the higher the thermal noise performance degradations at low Eb/No's. Based upon these conflicting requirements a minimum carrier recovery bandwidth can be identified which is dependent on the RF frequency band used and the specific carrier recovery implementation. Once this bandwidth is identified, the respective lower data rate limit can be identified.

For Ku-Band (14/12 GHz) transmission INTELSAT documents IESS-308 and IESS-405 define worst case phase noise density masks for earth stations processing digital carriers with data rates up to 2048 KBS. Figures 5 and 6 depict these masks for the spacecraft and earth station frequency converters respectively. Also shown in Figure 5 is a plot of the composite satellite link. For K_A band operation (30/20 GHz) the composite phase noise density will be shifted higher by about 6-8 dB.



INTELSAT VA
Continuous Component of Phase Noise

Figure 5

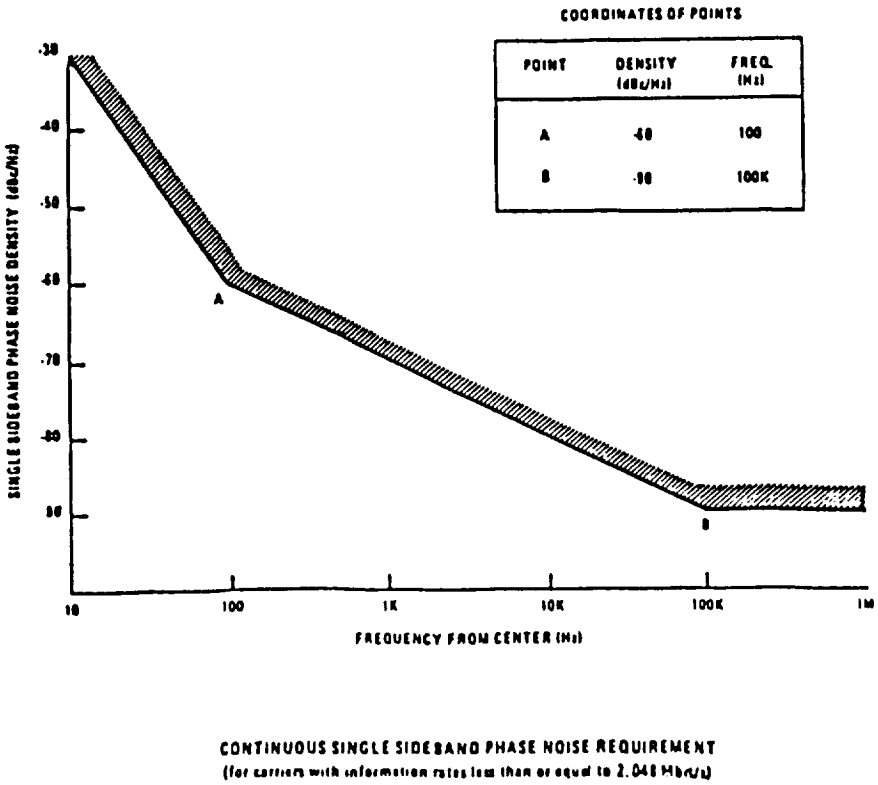


Figure 6

Table 2 from reference [1] depicts the magnitude of tracking errors for a second order loop with 0.707 damping factor.

Table 2

PHASE-LOCKED TRACKING OF PHASE NOISE FOR A PHASE-LOCKED LOOP WITH DAMPING $\zeta = 0.707$, AND NOISE BANDWIDTH $B_n = 0.53\omega_n$

Type of Phase Noise	*Phase-Noise Spectral Density*	*Phase Error — Second-Order Phase-Locked Loop, $\zeta = 0.707$* $\sigma_\phi^2 = \int_0^\infty \frac{\omega^4/\omega_n^4}{1+(\omega/\omega_n)^4} G_\phi(f)\,df$
Frequency flicker noise	$\frac{k_a}{f^3}$	$\frac{k_a\pi^3}{\omega_n^2} = \frac{k_a\pi^3}{(1/0.53)^2 B_n^2} = \frac{8.71k_a}{B_n^2}$
White frequency noise	$\frac{k_b}{f^2}$	$\frac{3.70k_b}{B_n}$
White phase noise	$k_c, f < f_b$	$k_c f_b$

(1) "Digital Communications By Satellite" by James J. Spilker, Jr., 1977 Prentice Hall, Inc., (Pages 336 through 357).

Inspection of the composite satellite link phase noise spectral density shown in Figure 5 identifies K_A and K_C as follows:

$$K_A = \left(\text{Log}_{10}^{-1} \quad \frac{-25dB}{10}\right) \quad (10\ \text{Hz})^3$$

$$K_A = 3.16$$

and

$$K_C = \left(\text{Log}_{10}^{-1} \quad \frac{-86dB}{10}\right)$$

$$K_C = 2.51 \times 10^{-9}$$

Since the plot shows a 10dB/decade not 20dB/decade rolloff between 100 Hz to 100 KHz, a worst case value of -74dBc/Hz at 1 KHz will be used to determine K_B since this value intersects the composite curve at the 100 Hz specification point.

TABLE 3

BN (Hz)	$\sigma_{\epsilon C}$			$\sigma_{\epsilon A}$	$\sigma_{\epsilon B}$	σ_ϵ TOTAL = RMS PHASE JITTER		
	f_H = 25 KHz	f_H = 50 KHz	f_H = 100 KHz			f_H = 25 KHz	f_H = 50 KHz	f_H = 100 KHz
10Hz	7.9×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	5.2×10^{-1}RAD	1.2×10^{-1}RAD	5.3×10^{-1}RAD (30.6°)	5.3×10^{-1}RAD (30.6°)	5.3×10^{-1}RAD (30.6°)
100Hz	7.9×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	5.2×10^{-2}RAD	3.8×10^{-2}RAD	6.5×10^{-2}RAD (3.7°)	6.5×10^{-2}RAD (3.7°)	6.63×10^{-2}RAI (3.8°)
200Hz	7.9×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	2.6×10^{-2}RAD	2.7×10^{-2}RAD	3.83×10^{-2}RAD (2.2°)	3.9×10^{-2}RAD (2.2°)	4.0×10^{-2}RAD (2.3°)
500Hz	7.9×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	1.0×10^{-2}RAD	1.7×10^{-2}RAD	2.1×10^{-2}RAD (1.2°)	2.27×10^{-2}RAD (1.3°)	2.53×10^{-2}RAI (1.45°)
1000Hz	7.8×10^{-3}RAD	1.12×10^{-2}RAD	1.58×10^{-2}RAD	5.2×10^{-3}RAD	1.2×10^{-2}RAD	1.5×10^{-2}RAD (0.87°)	1.72×10^{-2}RAD (0.99°)	2.05×10^{-2}RAI (1.2°)
2000Hz	7.6×10^{-3}RAD	1.09×10^{-2}RAD	1.58×10^{-2}RAD	2.6×10^{-3}RAD	8.6×10^{-3}RAD	1.18×10^{-2}RAD (0.67°)	1.4×10^{-2}RAD (0.81°)	1.82×10^{-2}RAI (1.04°)
5000Hz	7.1×10^{-3}RAD	1.06×10^{-2}RAD	1.54×10^{-2}RAD	1.0×10^{-3}RAD	5.4×10^{-3}RAD	9.0×10^{-3}RAD (0.51°)	1.2×10^{-2}RAD (0.68°)	1.6×10^{-2}RAD (0.94°)
10000Hz	6.1×10^{-3}RAD	1.00×10^{-2}RAD	1.50×10^{-2}RAD	5.2×10^{-4}RAD	3.8×10^{-3}RAD	7.2×10^{-3}RAD (0.41°)	1.07×10^{-2}RAD (0.61°)	1.55×10^{-2}RAI (0.89°)

TABLE 3

RMS TRACKING PHASE JITTER BETWEEN
RECOVERED CARRIER AND PSK SIGNAL
VERSUS BN (PLL NOISE BANDWIDTH)

MODULATOR IMPLEMENTATION

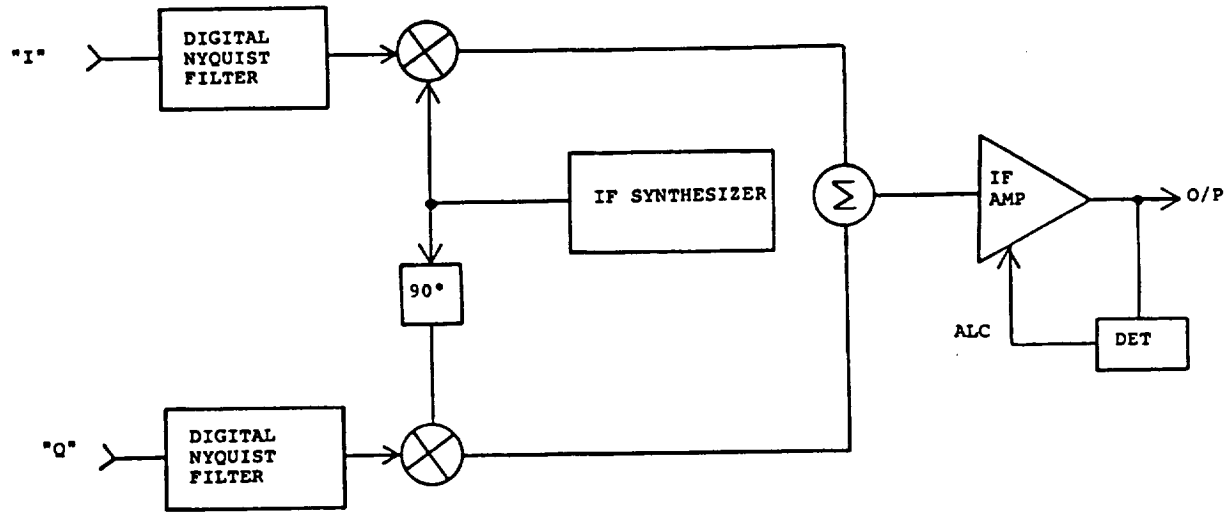


Figure 7a. Functional Block Diagram of Direct QPSK Modulator

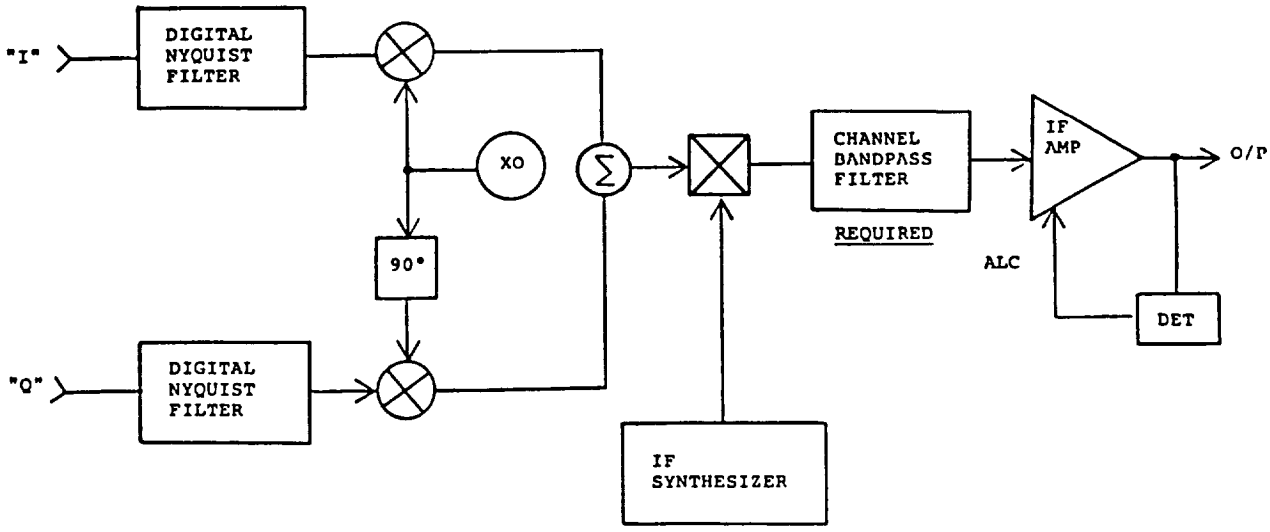


Figure 7. Functional Block Diagram of Frequency Translated QPSK Modulator

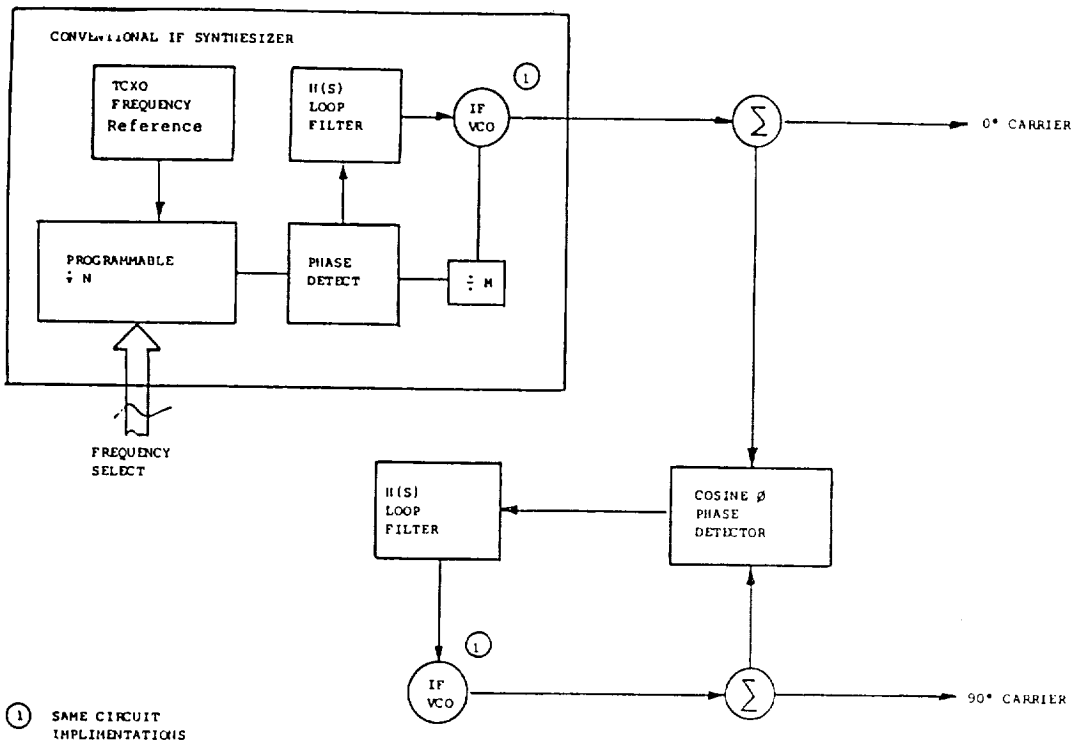


FIGURE 8
BROADBAND QUADRATURE
LOCAL OSCILLATOR GENERATOR

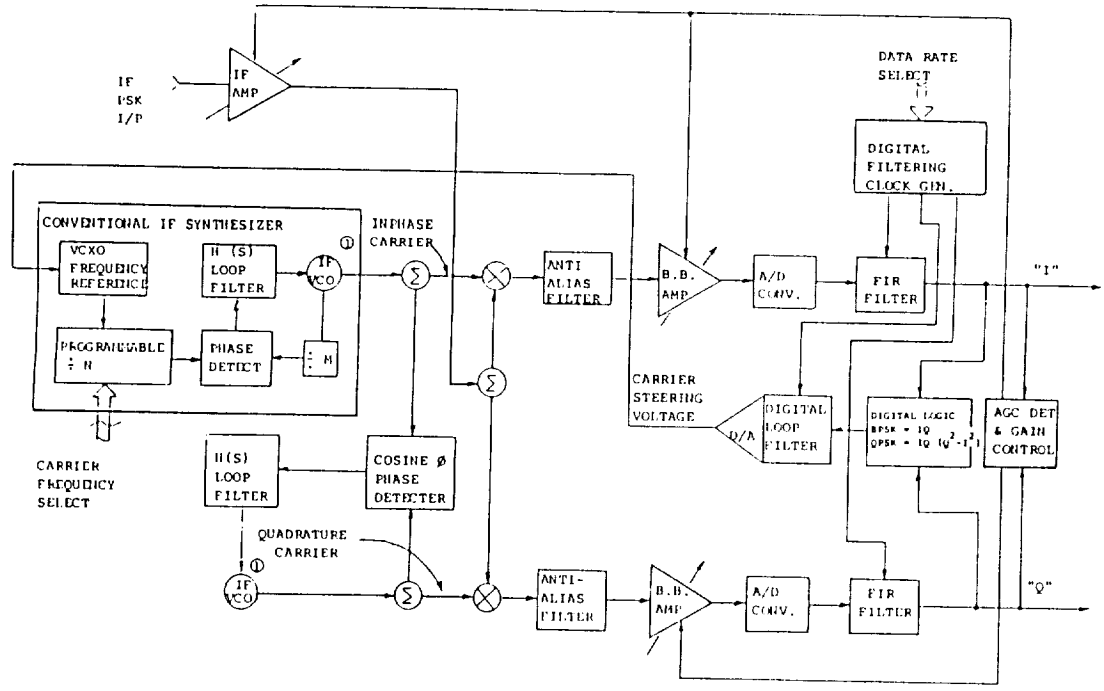


FIGURE 9
PROPOSED SIMPLIFIED BLOCK DIAGRAM
OF DIRECT DEMODULATION TECHNIQUE

CARRIER RECOVERY

INTRODUCTION

In general, Digital Satellite Modems are characterized by providing the lowest possible Bit Error Rate (BER) for a given Bit Energy per Noise Density (Eb/No). Typically these modems are implemented with robust BPSK or QPSK Modulation and high overhead Forward Error Correction such that error-less performance can be realized over the satellite link which is characterized with high noise.

In order to support this objective, these digital modems utilize Coherent Demodulation and optimum detection with low implementation losses. Coherent Demodulation is accommodated by multiplying the received PSK signal with a locally generated recovered carrier replica. This recovered carrier replica must have sufficient noise improvement quality and precise phase alignment with the specific PSK modulated signal being processed in order to support low implementation loss BER degradation. Since PSK is a suppressed carrier type of modulation, some type of non-linear signal processing is necessary to regenerate a coherent carrier reference. This process is the topic of this memo and is referred to as "Carrier Recovery".

We initiate our effort in this study area by assessing current and proposed Carrier Recovery schemes which are viable candidates for BPSK and QPSK Modulation. Next, we turn our attention towards the specific requirements of the work study, i.e., a Carrier Recovery implementation which:

1) Supports Programmable Data Rates;
2) Operates with BPSK or QPSK Modulation;
3) Supports both Burst and Continuous Modes of Operation;
4) Minimizes the constraints on Clock Recovery/Bit Synchronization;
5) Allows for digital filtering techniques prior to data detection;
6) Can be implemented with Digital Signal Processing Techniques as compared to Analog Signal Processing; and
7) Is viable in satellite communications.

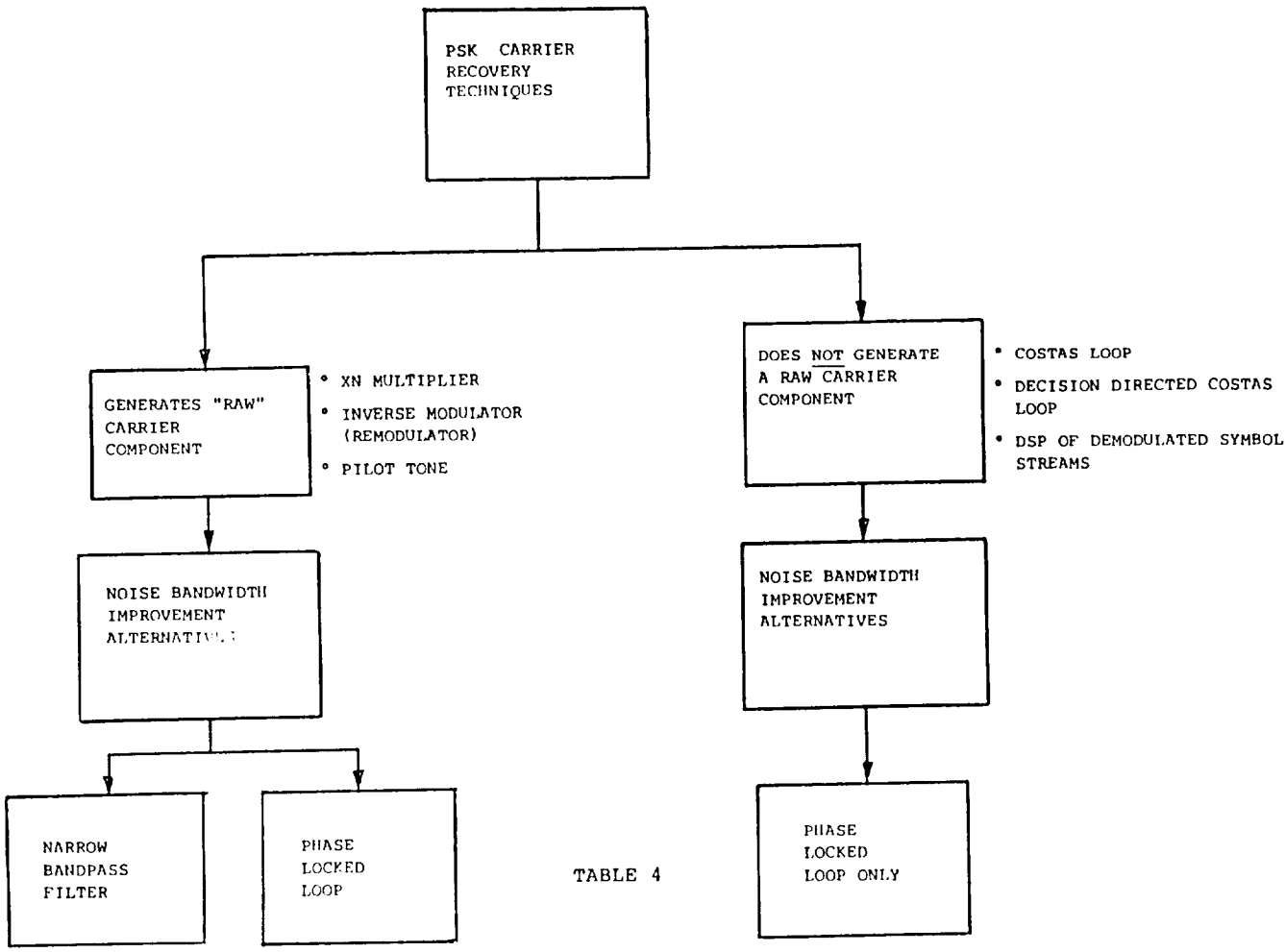


TABLE 4

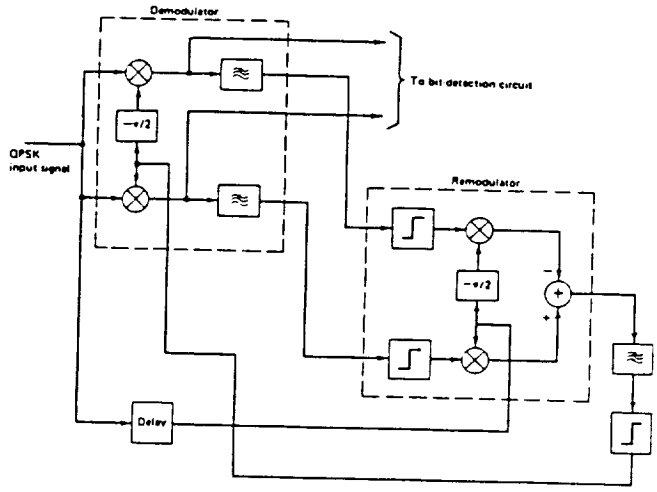


Figure 10a. Demodulator/Remodulator

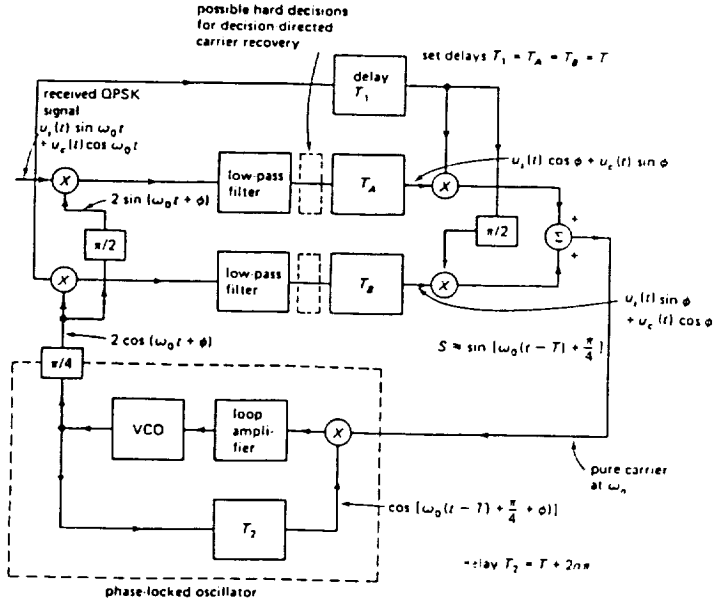


Figure 10b. QPSK carrier recovery using reverse modulation and a phase-locked oscillator. Decision-directed carrier recovery can be performed by making hard decisions as shown in the dashed boxes in the diagram.

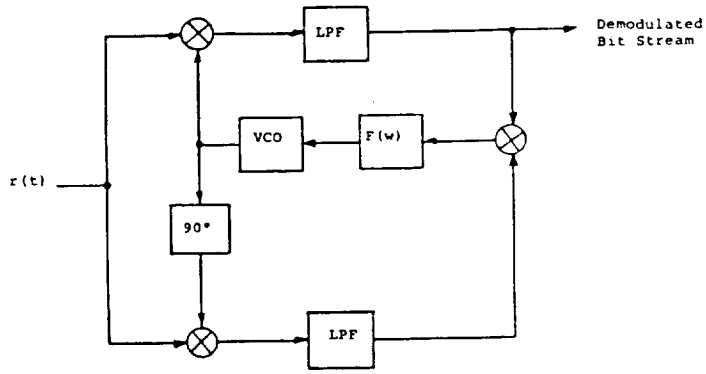


Figure 11a. BPSK Costas Loop

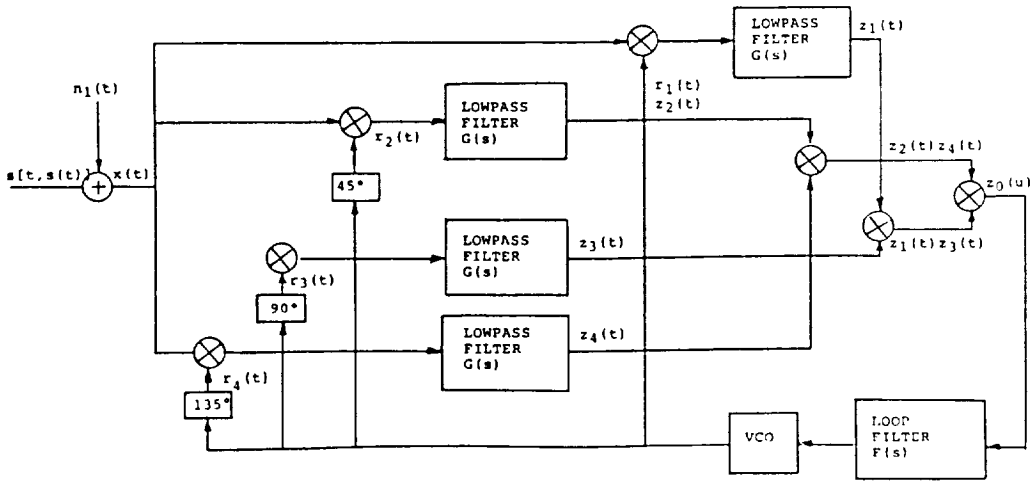
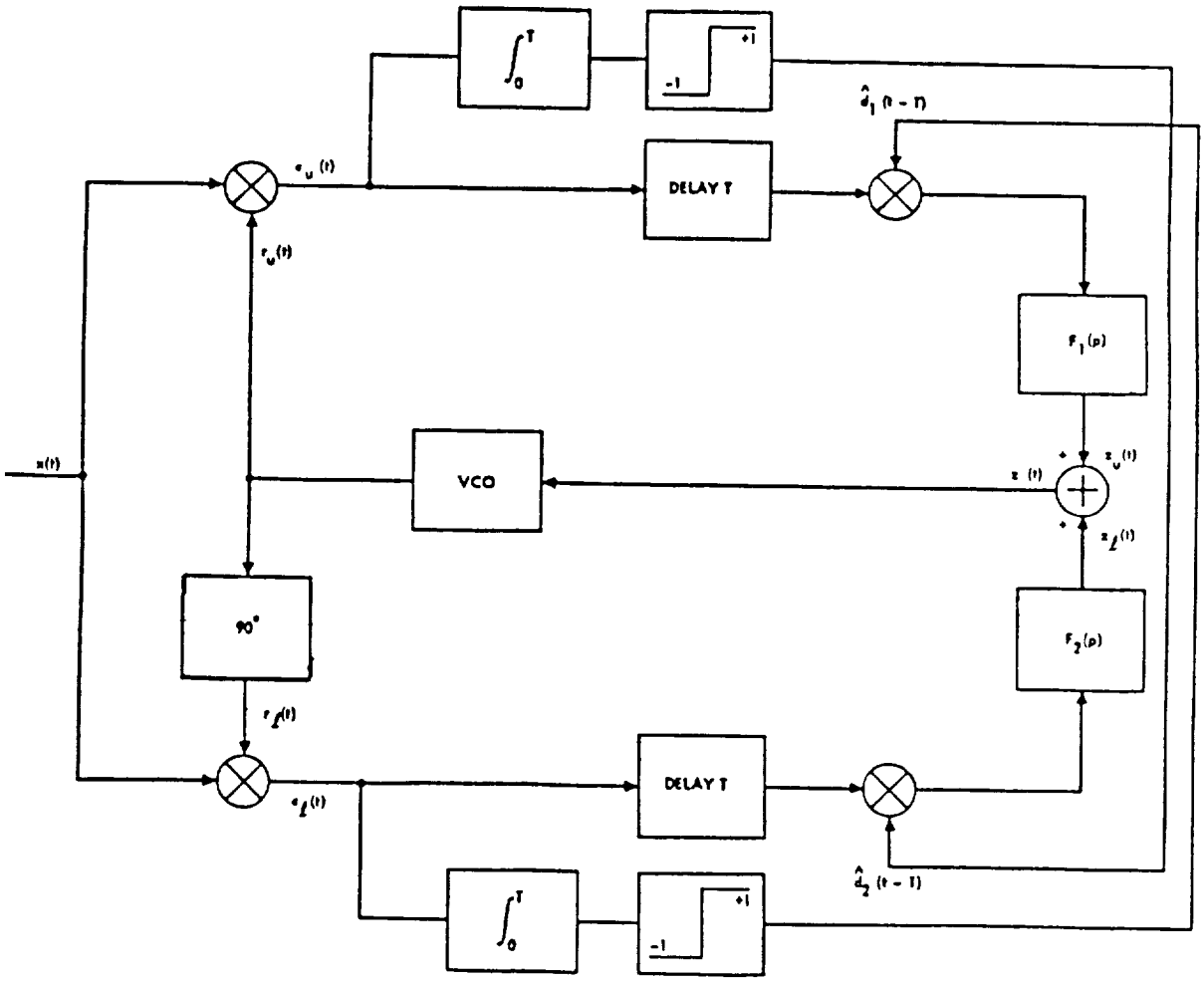


Figure 11b. A Conventional Quadriphase Costas Loop



Decision-Directed 4th Order Costas Loop with Integrate and Dump Filtering

Figure 12

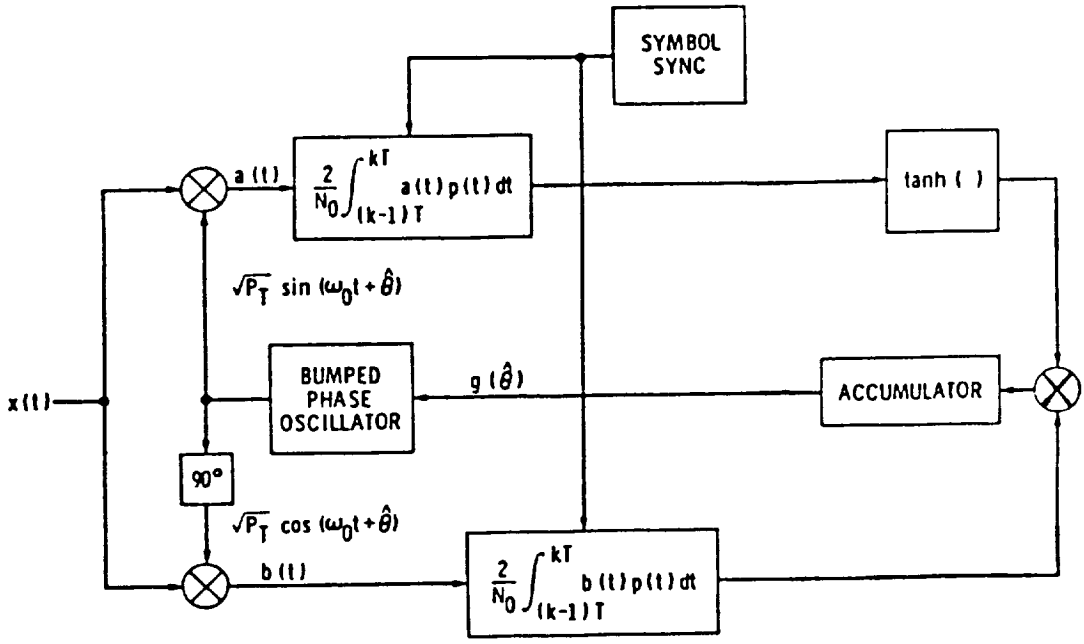


Figure 13a. The MAP Estimation Loop for Carrier Phase (BPSK)

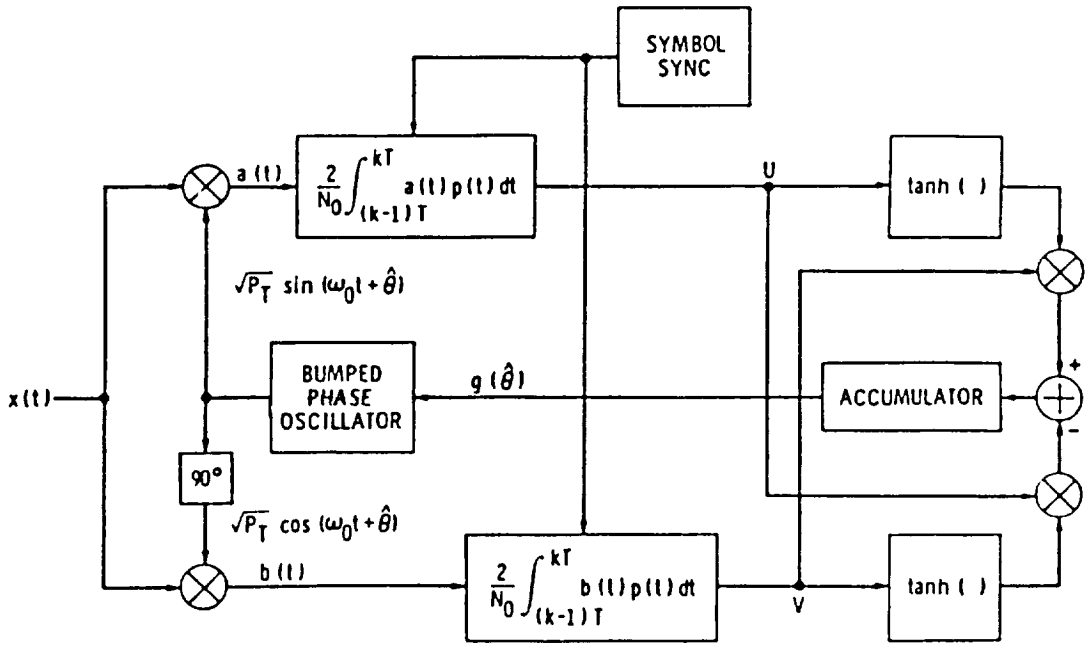


Figure 13b. The MAP Estimation Loop for Carrier Phase (QPSK)

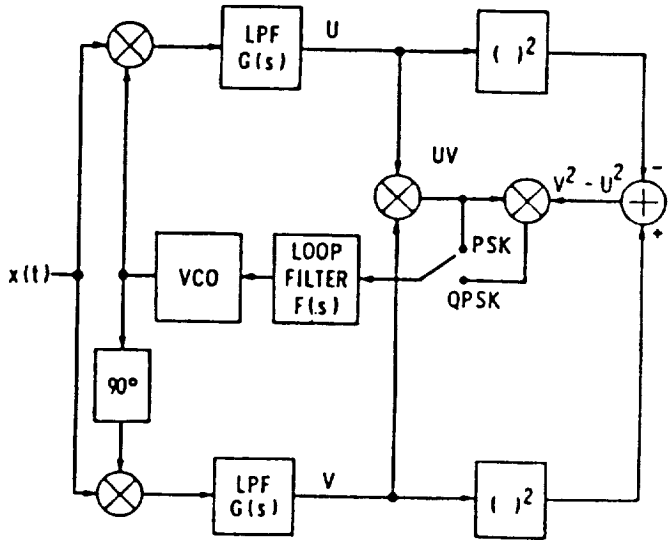


Figure 14. A Practical Realization of the MAP Estimation Loop, Passive Arm Filters, Small SNR

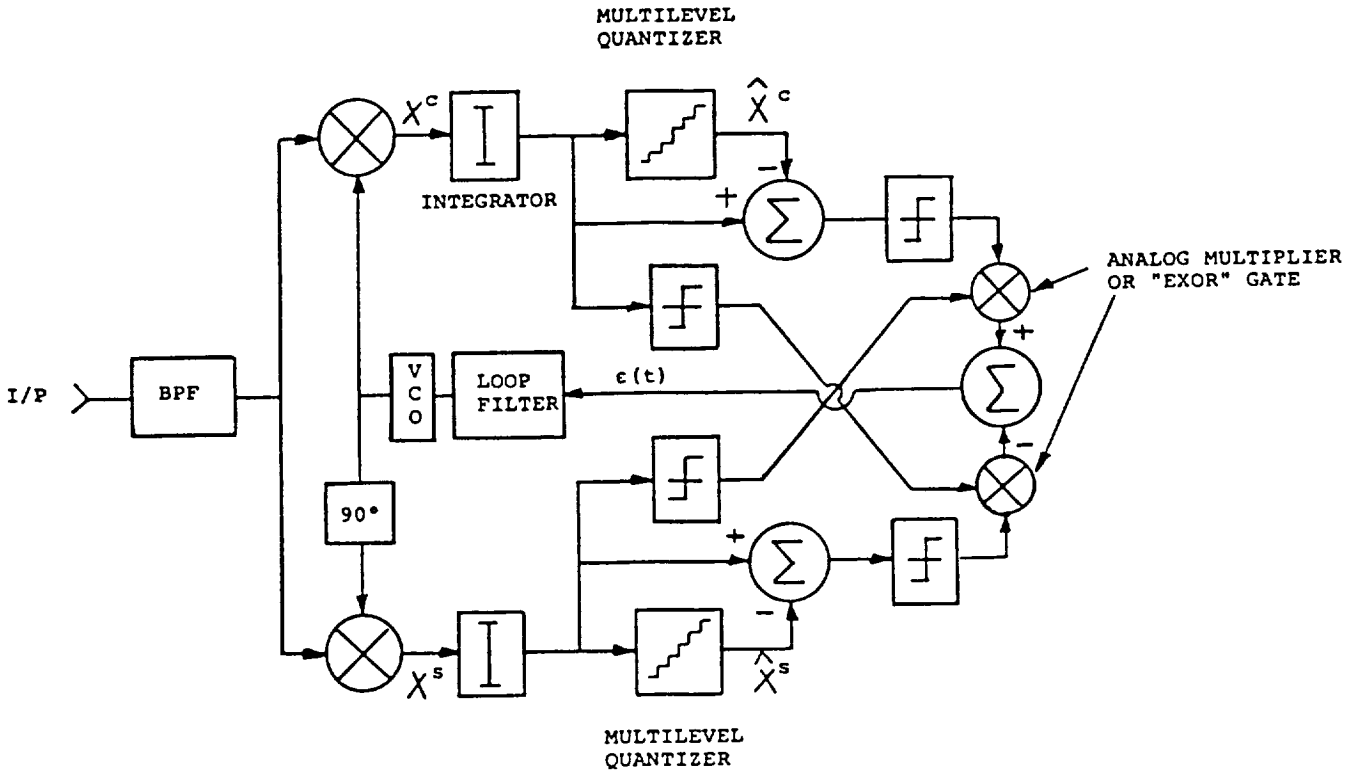


Figure 15. Block Diagram of the Carrier Recovery with Selective Gated PLL

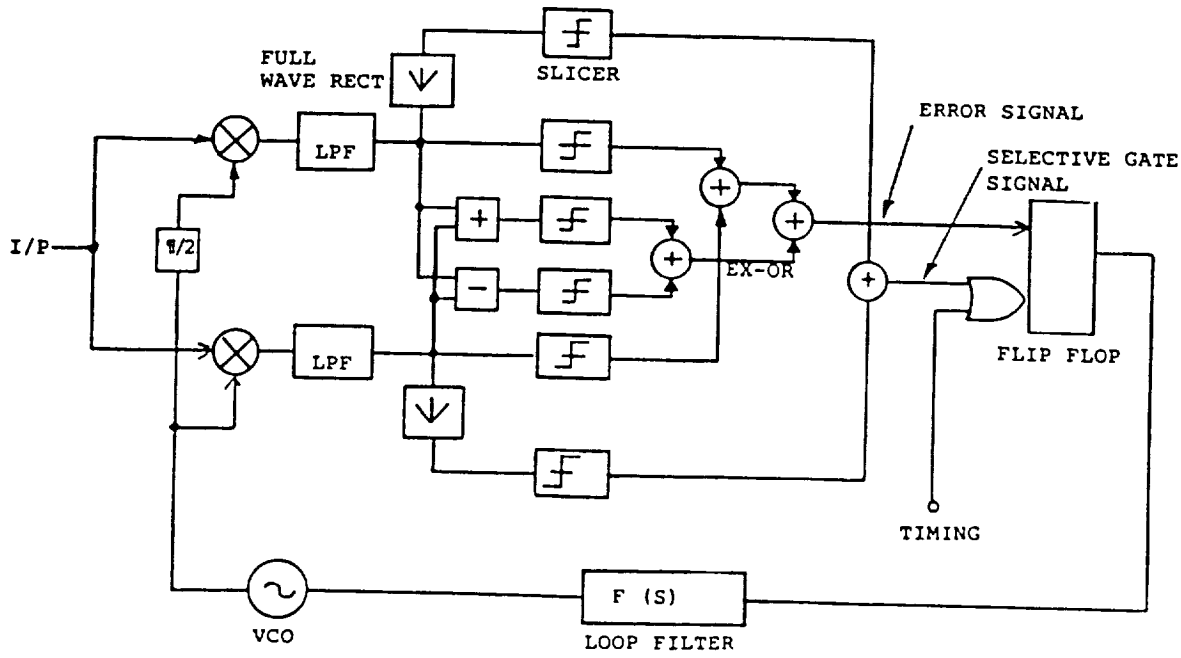


Figure 16. Proposed Carrier Recovery Loop Diagram

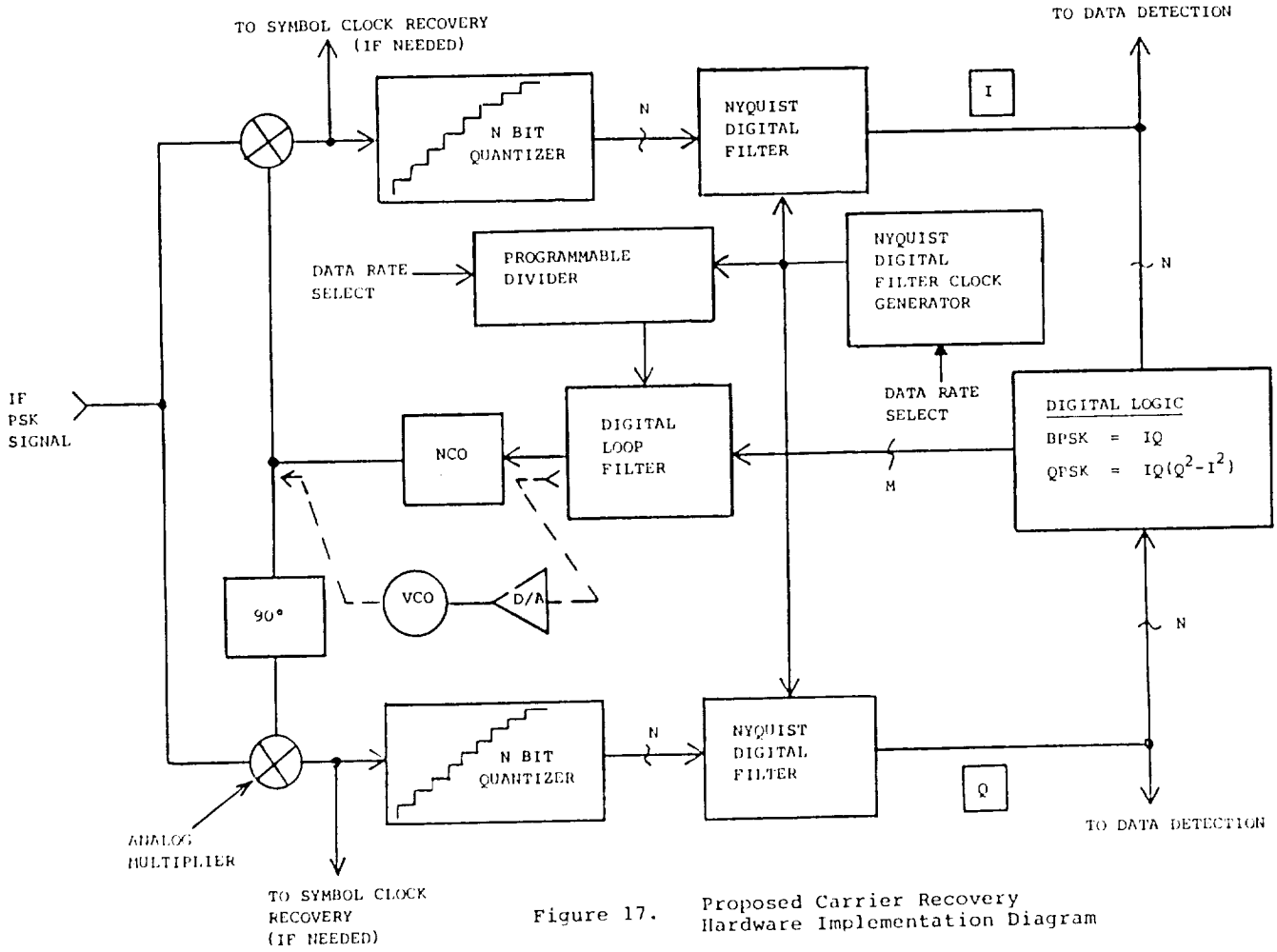


Figure 17. Proposed Carrier Recovery Hardware Implementation Diagram

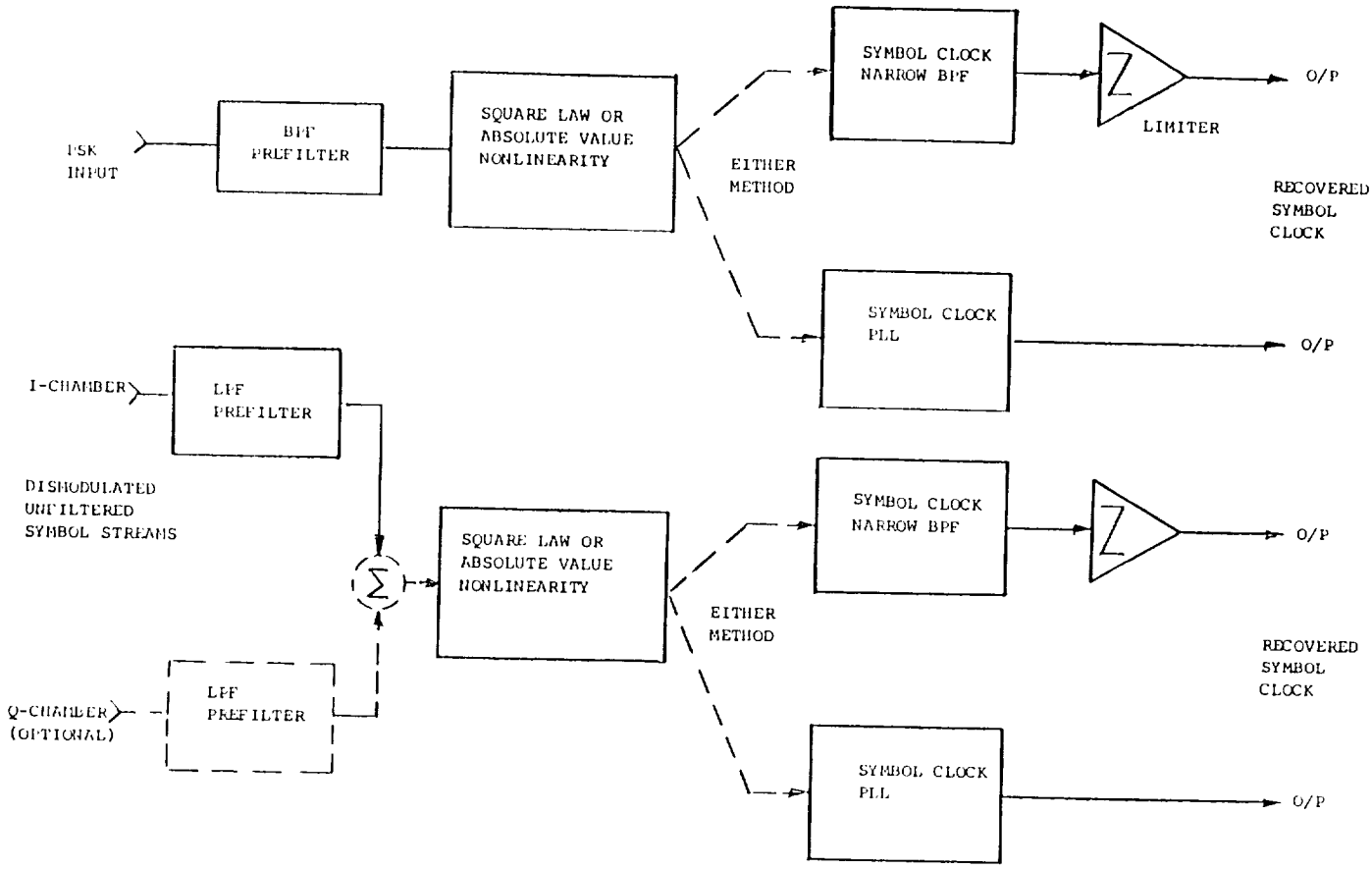
TIMING RECOVERY AND DATA SAMPLING

INTRODUCTION

The objective of this section is to identify the most favorable Timing Recovery Technique and its performance attributes which can be utilized by a Programmable Data Rate Digital Satellite Modem operating in a Multi-Carrier Transponder environment. We initiate our discussion by identifying the various types of Timing Recovery Techniques which are described in technical literature and used in digital communications. The operational characteristics and features of each Timing Recovery Scheme will be presented and a comparison to the study requirements will be made.

A candidate scheme will then be chosen based upon the one which offers the most favorable attributes. The performance impact of the candidate Timing Recovery Scheme on Soft Decision Data Sampling (detection) will also be assessed.

Lastly, viable hardware design techniques which utilize DSP Technology will be described for the various functions required in the implementation of the technique. This is concluded with an overall implementation diagram of the proposed Hardware Timing Recovery approach.



LPF - LOW PASS FILTER
BPF - BANDPASS FILTER
PLL - PHASE LOCKED LOOP

Figure 18

"SQUARE LAW"/"ABSOLUTE VALUE"
NONLINEARITY
TIMING RECOVERY SCHEMES

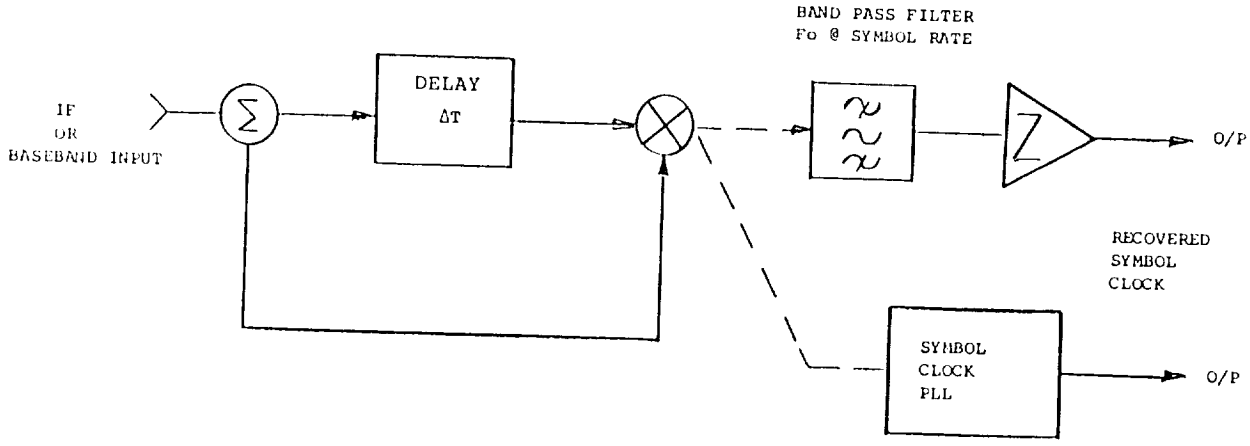


Figure 19

DELAY-LINE DETECTOR
FUNCTIONAL BLOCK DIAGRAM

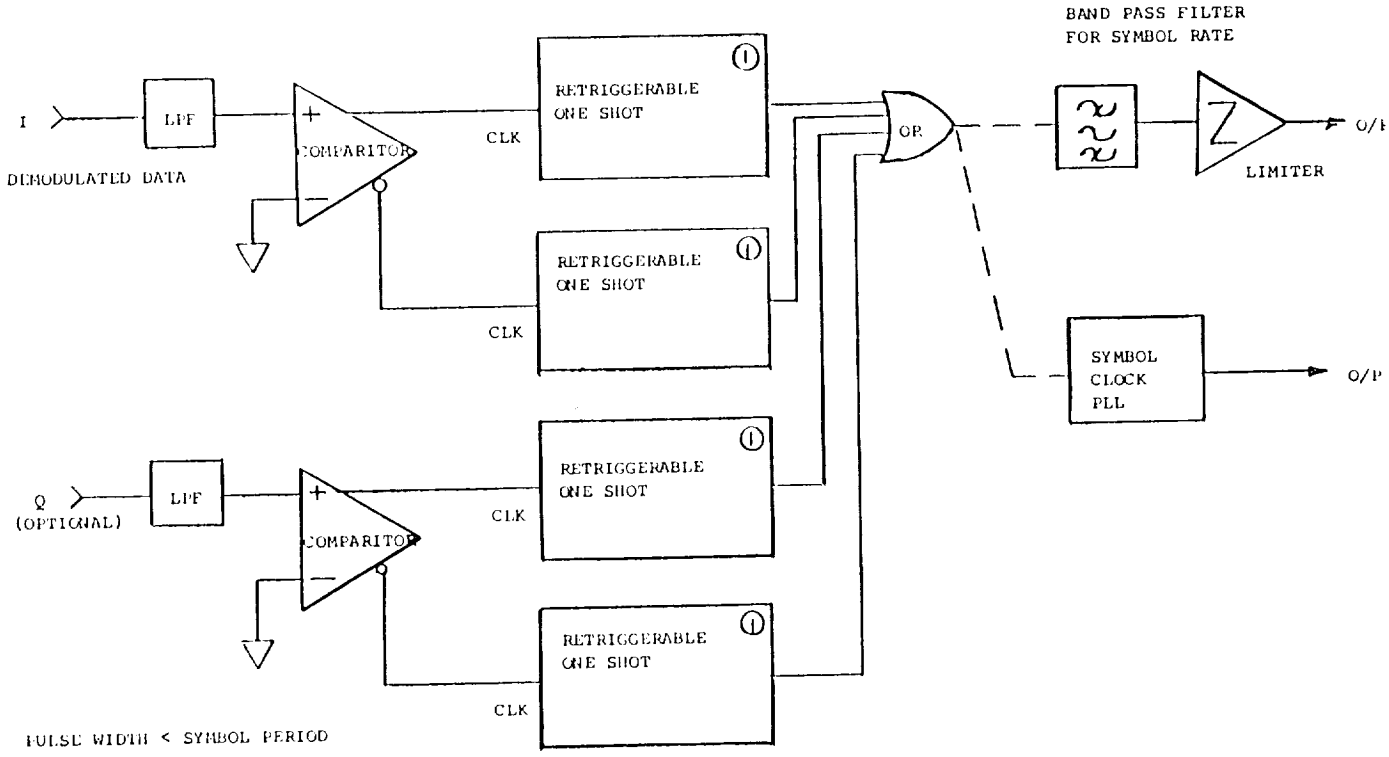


Figure 20

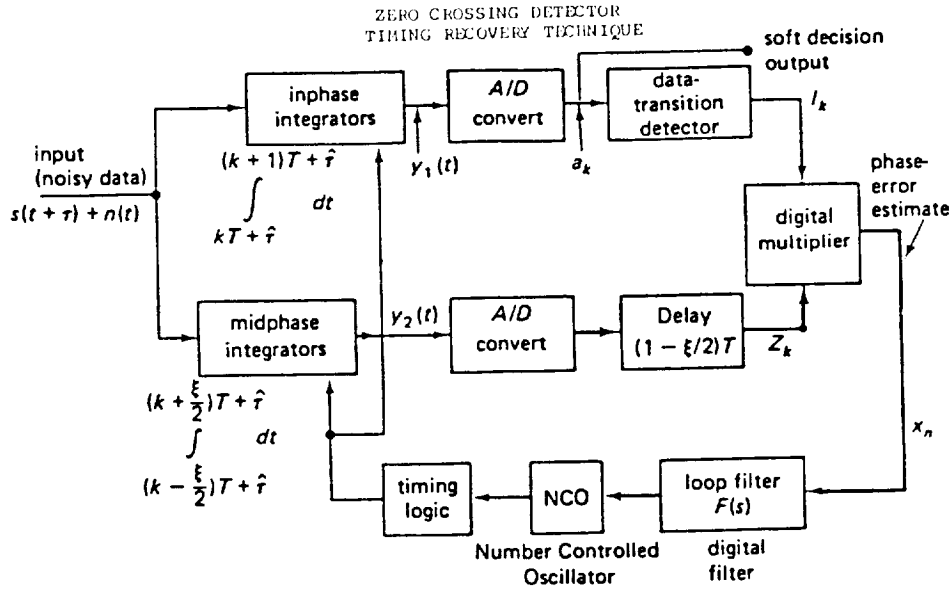
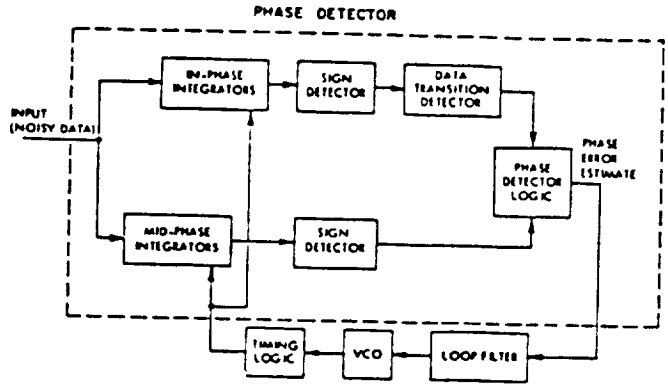
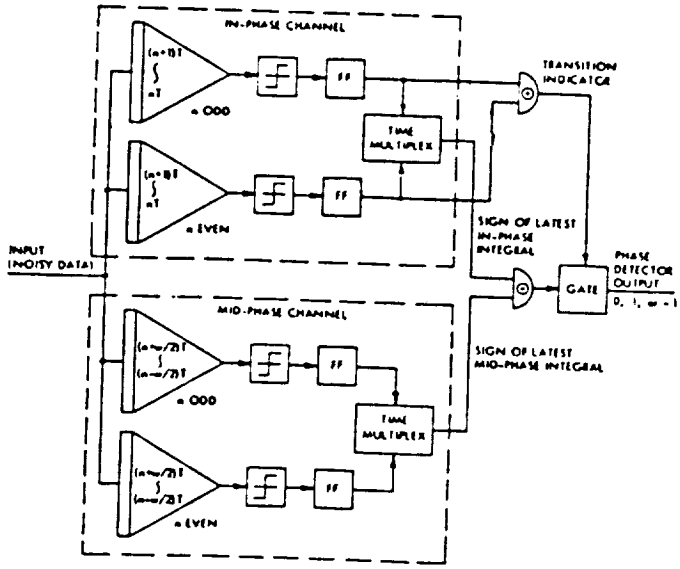


Fig. 8 In-phase/Mid-phase bit synchronizer with inphase and midphase channels. The input clock offset is τ, and the clock phase estimate is $\hat{\tau}$. The midphase integrator window width is ξT sec. The timing error is $\epsilon \triangleq \tau - \hat{\tau}$.

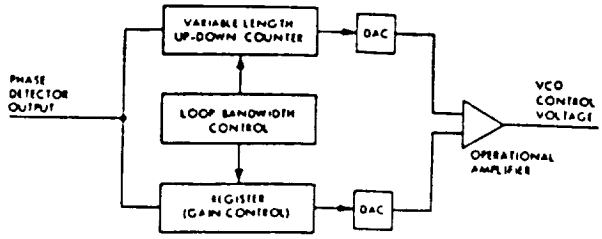
Figure 21



Symbol synchronizer.



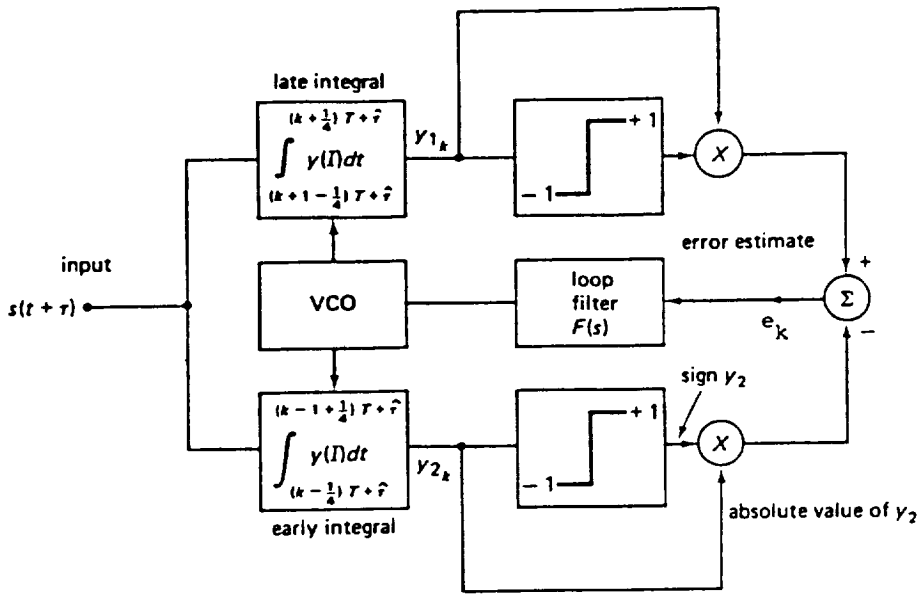
Phase detector.



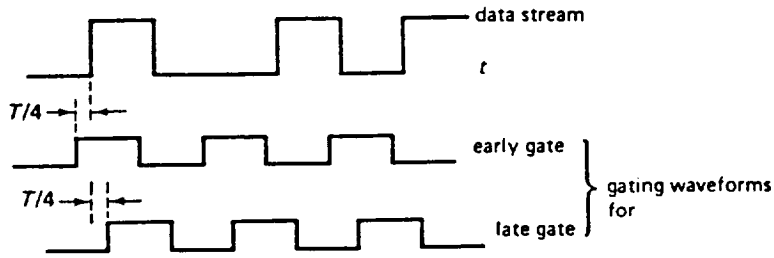
Loop filter.

Figure 22

PRACTICAL IMPLEMENTATION OF DIGITAL TRANSITION TRACKING SYMBOL SYNCHRONIZER FROM REFERENCE 9



(a)



(b)

NOTE

$\Delta_o T = \frac{T}{4}$ Shown

Block diagram and waveforms for an absolute-value early- late-gate bit synchronizer. (a) Block diagram; the $T/4$ overlap used can be shown to be optimum. (b) Waveforms for $\hat{\tau} = \tau$

Figure 23

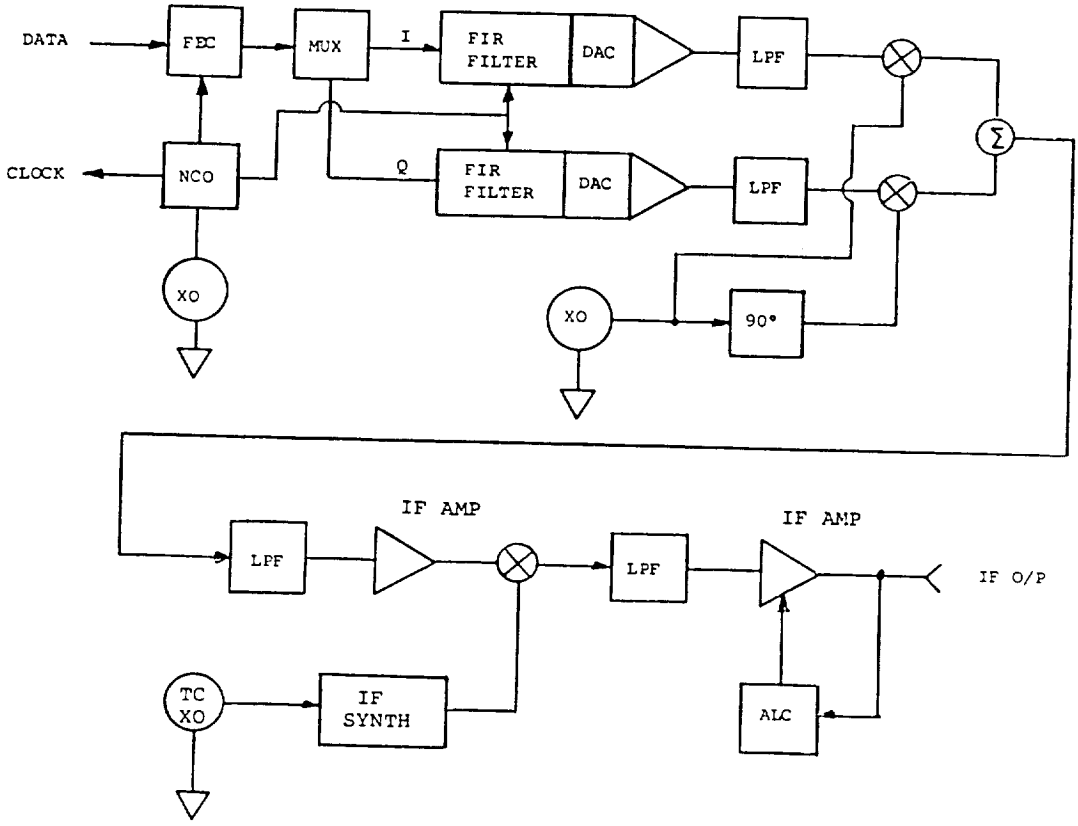


Figure 24

PROPOSED VARIABLE RATE MODULATOR BLOCK DIAGRAM

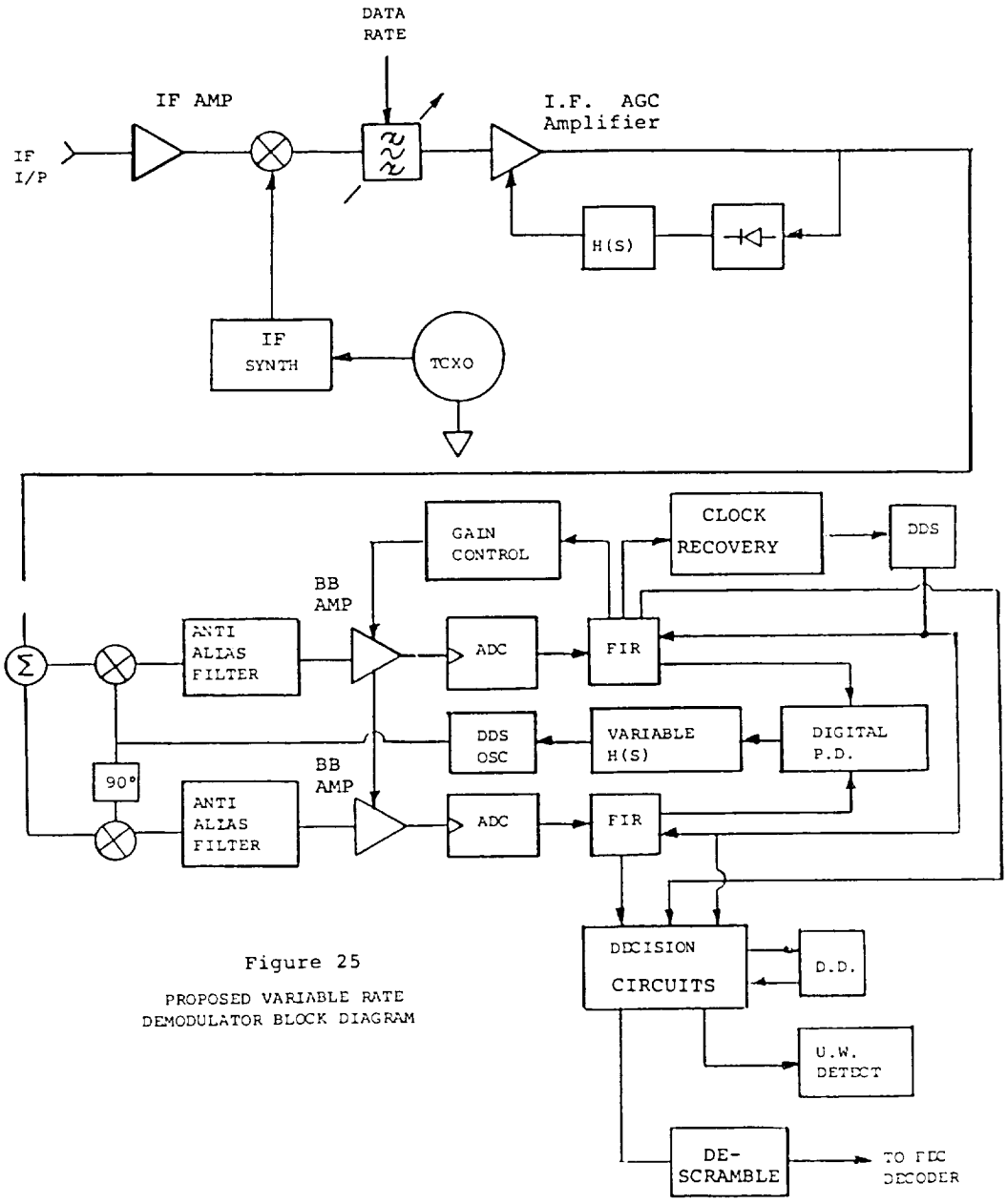


Figure 25

PROPOSED VARIABLE RATE
DEMODULATOR BLOCK DIAGRAM

The overall Block Diagrams of the modulator and demodulator suggested are:

Figure 24: PROPOSED MODULATOR

Figure 25: PROPOSED DEMODULATOR