

IV - HIGH-TEMPERATURE ELECTRONICS

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In recent years, the aerospace propulsion and space power communities have acknowledged the growing need for electronic devices that are capable of sustained high-temperature operation. Applications for high-temperature electronic devices include engine ground test instrumentation such as multiplexers, analog-to-digital converters, and telemetry systems capable of withstanding hot section engine temperatures in excess of 600 °C. Similarly, engine-mounted integrated sensors could reach temperatures which exceed 500 °C, while uncooled operation of control and condition monitoring systems in advanced supersonic aircraft would subject electronic devices to temperatures in excess of 300 °C (ref. IV-1). Hypersonic vehicles will ultimately pose even more severe demands on electronic devices and sensors.

In addition to aeronautics, there are many other areas that would benefit from the existence of high-temperature electronic devices. Space applications include power electronic devices for the Freedom space station, space platforms, and satellites. Since power electronics require radiators to shed waste energy, electronic devices that operate at higher temperatures would allow a reduction in radiator size. Other applications on earth include deep-well drilling instrumentation, power electronics, and nuclear reactor instrumentation and control.

To meet the needs of the applications mentioned previously, the high-temperature electronics program at the Lewis Research Center is developing silicon carbide (SiC) as a high-temperature semiconductor material. This program supports a major element of the Center's mission: to perform basic and developmental research aimed at improving aerospace propulsion systems. Research is focused on developing the crystal growth, characterization, and device fabrication technologies necessary to produce a family of SiC devices.

BENEFITS OF SILICON CARBIDE AS A SEMICONDUCTOR MATERIAL

Since the desired operating temperature for some of the applications mentioned approaches 600 °C, it is clear that a new semiconductor material will need to be developed. On the basis of the inherent solid-state properties of silicon, the maximum temperature at which a silicon device could theoretically operate is about 300 °C. Gallium arsenide could theoretically operate at 460 °C, but has not proven operationally stable at this temperature. In comparing potential candidate materials for high-temperature semiconductor devices, SiC stands out not only because of its excellent high-temperature electronic properties but also because it is a very stable ceramic material up to temperatures of 1800 °C. The maximum operating temperature for a semiconductor is determined by the forbidden bandgap energy. The temperature limit is reached when

the number of intrinsic carriers, thermally excited across the energy gap, approaches the number of extrinsic carriers. This temperature (when expressed as the absolute temperature) is roughly proportional to the energy bandgap.

By using the same criteria as applied to silicon, SiC could theoretically be employed at temperatures as high as 1200 °C. A more reasonable, shorter term goal is to produce electronic devices capable of 600 °C operation. SiC is characterized by excellent physical and chemical stability making it suitable for long-term use in high temperature, corrosive environments. The combination of the material's high thermal conductivity and high breakdown field provides the potential for improved power system electronics and for increasing the number of devices per unit area. Those properties which determine the high-frequency characteristics of semiconductor devices also appear to be excellent for SiC and superior to those of silicon or gallium arsenide. The properties and benefits of SiC are summarized in table IV-I.

SILICON CARBIDE CRYSTAL GROWTH

Until recently, there was no process whereby single crystals of SiC with sufficient size, purity, and perfection could be grown reproducibly. SiC does not melt at any reasonable temperature and pressure, so this rules out the growth-from-melt technique commonly used to obtain other semiconductor single crystals such as silicon and gallium arsenide. Historically, vapor phase growth processes have proven to be the most successful method for producing SiC crystals. Early research was done on SiC crystals that were a by-product of the industrial process for making abrasives. In the industrial process, SiC is formed at 2500 °C by the reaction of silica and coke. At this temperature, gas pockets form within the SiC reaction product. The SiC sublimates and then condenses on the walls of pockets located at cooler parts of the reaction product. Occasionally, isolated SiC crystals are produced within these pockets during the production process. The larger and better crystals were selected for research purposes.

In 1955, Lely developed a laboratory version of the industrial sublimation process and was able to produce rather pure SiC crystals. Encouraged by the Lely process, NASA Lewis and other laboratories pursued the development of SiC semiconductor devices during the 1960's and early 1970's (refs. IV-2 to IV-6). Though SiC devices were demonstrated above 400 °C, by the early 1970's the Lely process and other processes had not matured to the point where high-quality large-area crystals could be grown reproducibly. Since crystal substrates are crucial to device fabrication, interest in SiC waned. From 1973 to 1980, there was very little effort in the U.S. on SiC. However, research did continue in Japan and in Europe during this period.

In 1980, because of the increased need for high-temperature electronics in advanced turbine engines, NASA Lewis again embarked on a high-temperature electronics program. The emphasis again has been on developing SiC. The problem regarding the crystal growth of SiC is rooted in the fact that SiC crystals can take on many different structural forms called polytypes. In most cases, SiC crystals grown by sublimation techniques are a mixture of different polytypes. Since each SiC polytype has its own electronic properties, sublimation-grown SiC crystals usually contain heterojunctions and possess unpredictable electronic properties. To favor growth of a single polytype of SiC, epitaxial growth on a host crystalline substrate from gases containing silicon and carbon was hypothesized. The host crystal imparts its crystalline regularity to the

thin growing layer. Since silicon is available in perfect, large, and low-cost crystals, many attempts at the heteroepitaxial growth of SiC on Si were made. These efforts were largely unsuccessful because of the large lattice mismatch that exists between Si and SiC. (The SiC lattice is 20 percent smaller than the Si lattice.)

Large-area heteroepitaxial growth of cubic SiC on Si was finally achieved at the NASA Lewis Research Center in 1983 by using a chemical vapor deposition (CVD) process (ref. IV-7). In recognition of this achievement, an IR-100 award was presented to NASA Lewis. Recently, a research program utilizing the NASA Lewis SiC crystal growth process has been established at Howard University (ref. IV-8).

Crystal growth takes place at atmospheric pressure in a fairly conventional horizontal CVD system. A complete system description is given in reference IV-9. The chemical vapor deposition reaction system is illustrated schematically in figure IV-1. To grow single-crystal cubic SiC, first an electronic-grade silicon substrate is placed on an rf-heated graphite susceptor. The essential step in the growth process is a rapid temperature ramp from near room temperature to a growth temperature of 1360 °C in the presence of a hydrocarbon gas. The NASA Lewis process uses propane as the carbon-containing gas. During the first 2 min of growth, a single-crystal cubic SiC film about 20 nm thick is produced on the Si substrate. After this initial SiC growth, silane gas is added to provide a silicon source and to initiate the final step, the bulk growth of cubic SiC to the desired thickness. During this time, the cubic SiC layer grows at a rate of 3 to 4 $\mu\text{m/hr}$.

A photograph of the chemical vapor deposition system is shown in figure IV-2. The reaction tube and associated plumbing are in the hood (center). The control valves and flow controllers reside in the vented area directly to the right. In the right foreground are the manual and computer control systems, while in the left foreground is a mass spectrometer used to monitor system gases. The rf generator is not shown.

Cubic SiC is a transparent, yellow crystal which fractures into regular rectangular pieces. In the photograph of figure IV-3, the silicon substrate has been chemically removed from a 16- μm -thick crystal. Although visually, the material appears to be of relatively good quality, in actuality a high density of defects exists in the crystal. Certain defects can adversely affect the electrical properties of SiC devices. During the past five years, much progress has been made in understanding problems associated with crystal growth, but much research remains to be done in this area.

CHARACTERIZATION OF SiC FILMS

Initially, the transition from the Si substrate to the SiC epitaxial layer was thought to occur by means of a thin buffer layer or transition layer of the order of 20 nm thick (ref. IV-7). However, high-resolution transmission electron microscopy (TEM) has demonstrated that the SiC/Si interface is abrupt with no transition region (ref. IV-10). The cubic SiC films do contain a large

density of defects that include interfacial twins, stacking faults, and anti-phase disorder (ref. IV-11). The defect density in the films is greatest near the SiC/Si interface and decreases with distance away from the interface.

A particular type of lattice defect, called antiphase boundaries (APB's), was reported to be present in all SiC films grown on Si at NASA Lewis (ref. IV-12). The APB's can be decorated by chemical etching, sputter etching, wet oxidation, or cubic SiC growth in the presence of diborane (ref. IV-13) and have the appearance of irregular-shaped boundaries as shown in figure IV-4(a). APB's form in the initial stages of growth on the Si substrate when SiC islands of opposite phase nucleate and grow together. Across the APB, the chemical bonding is between like atoms (i.e., Si-Si or C-C), instead of the normal Si-C bond between neighboring atoms.

Normally, in epitaxial growth on Si, the surface of the Si substrate is oriented precisely parallel to an atomic plane, for example, the (001) plane. It has been found in the growth of gallium arsenide on Si that APB's are eliminated by orienting the substrate slightly off-axis from the (001) plane. This technique was applied to SiC growth at NASA Lewis with the following results: for Si substrates that were tilted 1° to 4° from the (001) plane, all APB's were eliminated from the subsequent films grown. In addition, the resultant SiC films were smoother by a factor of 2 to 3 than the films grown on on-axis substrates (ref. IV-13). The micrograph in figure IV-4(b) shows the results of using an off-axis Si substrate for SiC growth. Further work is needed to determine the effect on electrical properties and the performance of devices fabricated from these films. Also, the optimum tilt angle and the direction of optimum tilt have yet to be determined.

Additional SiC material characterization is provided by photoluminescence, Raman, Rutherford backscattering, cathodoluminescence, and DLTS techniques (refs. IV-14 to IV-17).

Electrical characterization to determine electrical properties of the cubic SiC films is an important and necessary evaluation step if high-quality SiC films are to be achieved. Room-temperature Hall measurements were made on cubic SiC films grown at NASA Lewis using the van der Pauw configuration (ref. IV-18). Ohmic electrical contacts consisted of sputtered tantalum followed by sputtered gold. Detailed analysis of the Hall measurements indicated that unintentionally doped films were always n-type and that the films were heavily compensated. It is believed that all present-day cubic SiC films grown at NASA Lewis and elsewhere are compensated. The significance of compensation is the degradation of device quality. Compensated semiconductors have many ionized impurities (positive for donors and negative for acceptors) embedded in the crystal lattice, and these ions serve as scattering centers for the moving charge carrier. This increases the impurity scattering and reduces the total mobility of the charge carrier compared to uncompensated material with the same density of free carriers. Identification and eventual elimination of the compensating impurities remains a research goal.

SiC DEVICE FABRICATION TECHNOLOGY

Devices fabricated from NASA Lewis-grown SiC have been characterized and compared to conventional silicon devices. Shown in figure IV-5 are the current-voltage curves for ion-implanted SiC and Si diodes. Note that at 300 °C the Si diode is rendered useless (shorted) while the SiC retains its rectification

properties. The poorer quality of the SiC diode characteristics at room temperature is due to the unoptimized design of the device, the fabrication process, and the crystal quality (ref. IV-19).

The availability of SiC substrates now allows NASA Lewis to place increasing emphasis on device fabrication. In-house research is pursuing the fabrication of an in situ grown junction diode. Device technology is also being developed through outside activities at two separate research laboratories.

North Carolina State University (NASA grant NAG3-782) is concentrating on fundamental SiC device fabrication utilizing, when possible, technology compatible with the silicon industry. Three device structures are being pursued at NCSU: Schottky barrier diodes, ion implanted diodes, and a metal-insulator-semiconductor field effect transistor (MISFET). The National Bureau of Standards (Contract C-30007-K) is developing a device quality insulating layer, oxide or nitride, for SiC. A quality insulating layer is of paramount importance for integrated circuit technology. Earlier research had examined the quality of an oxide insulating layer deposited onto the SiC surface (refs. IV-20 and IV-21).

Although SiC can easily survive the 600 °C temperature requirement for the NASA Lewis program, an electrical contact material must be developed which also can survive. Successful metallization (i.e., electrical contact) requires a metal that adheres well to the SiC surface and possesses a chemically stable metal/SiC interface. Additionally, low contact resistance and chemical stability of the metallization scheme at high temperatures are also necessary. In the study of SiC metallization, extensive information concerning the SiC surface properties has been learned (refs. IV-22 and IV-23). Methods to create a carbon-rich or silicon-rich SiC surface prior to metallization have been developed (refs. IV-24 and IV-25). Metals that are refractory carbide-formers or silicide-formers are currently being tested at 600 °C for long periods of time (refs. IV-26 and IV-27).

FOCUS OF CURRENT AND FUTURE SiC RESEARCH

Current and future program plans are outlined in figure IV-6. Near-term studies will be performed primarily through in-house and grant research efforts. Computer modeling of the chemical vapor deposition process for SiC crystal growth has been initiated as an in-house project based on a recently completed SBIR contract, NAS3-23891 (ref. IV-28). The goal is to improve the SiC crystal growth through the identification and understanding of the important chemical reactions involved in the growth process.

Ultimately, to achieve our goals of integrated circuits and sensors, the scope of the high-temperature electronics program must be expanded into the area of device packaging. At the same time, however, the basic crystal growth and characterization research must continue to receive appropriate attention.

CONCLUDING REMARKS

The development of semiconductor materials does not occur overnight. First germanium, then silicon and then gallium arsenide, for example, have come to the marketplace after years in the laboratory and countless dollars spent for development costs. The history of SiC as a high-temperature semiconductor has been one of high expectations followed by disappointment. Recent advances in the crystal growth of SiC and the increased knowledge of the bulk material properties of the grown SiC are cause for renewed enthusiasm. It should be noted that foreign research programs are more aggressively pursuing the development of SiC technology than are those in the U.S., and although the development of SiC falls into the category of high-risk research, the future looks promising and the potential payoffs are tremendous. SiC now appears ready to emerge as a useful semiconductor material.

TABLE IV-I. - BENEFITS OF SILICON CARBIDE AS SEMICONDUCTOR MATERIAL

Property	Benefit
High operating temperature	600 °C electronics
Excellent stability	Sustained use in hostile environment
High thermal conductivity and high breakdown field	Improved power electronics and increased device packing density
Excellent high-frequency properties	Superior high-frequency devices

CHEMICAL VAPOR DEPOSITION REACTION SYSTEM

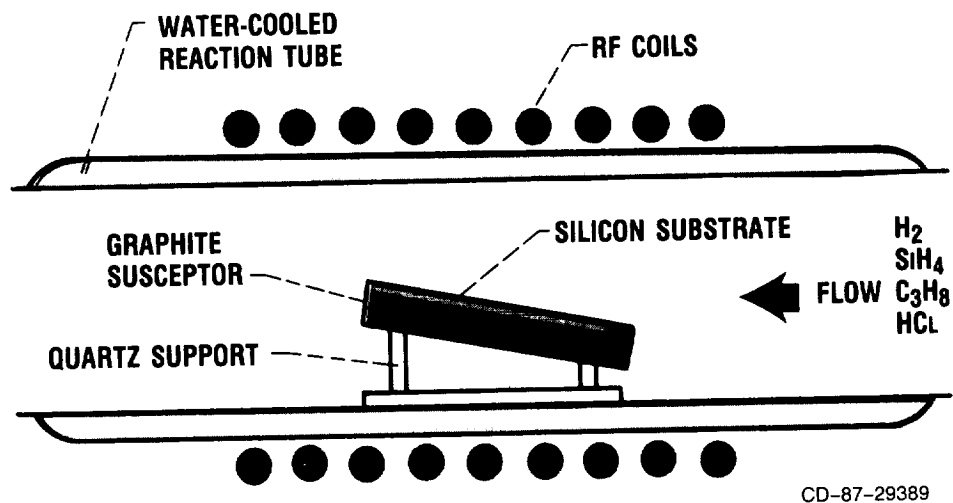
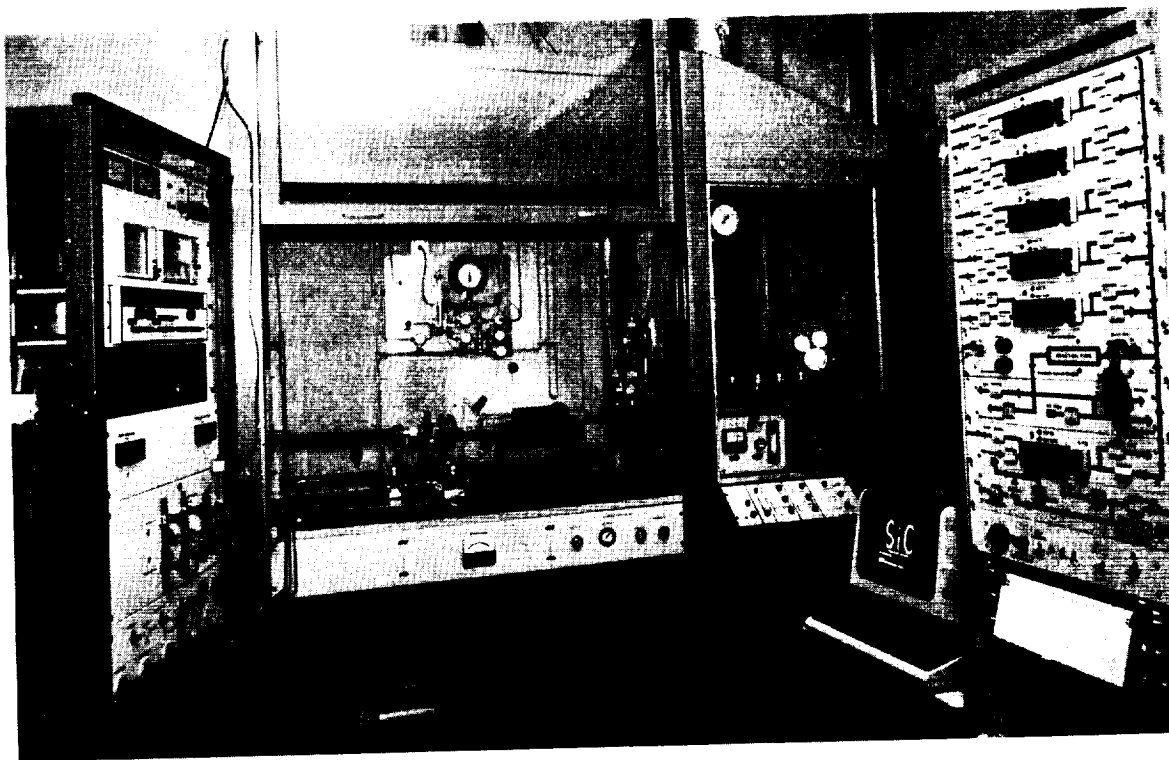
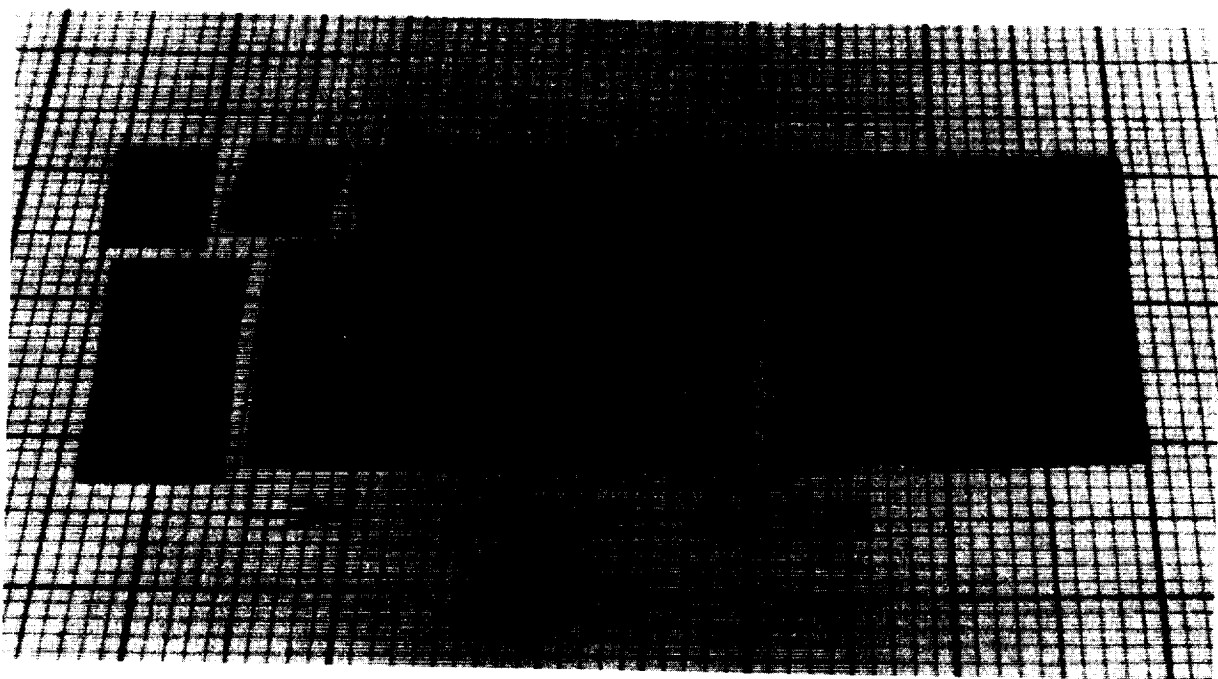


Figure IV-1. - Chemical vapor deposition reaction system.



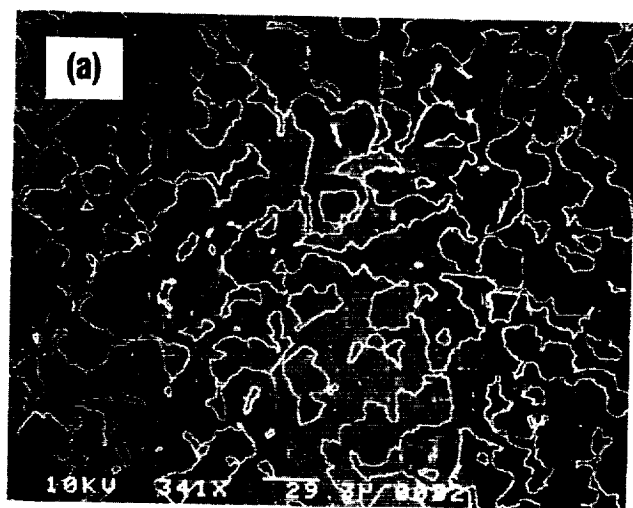
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Figure IV-2. - Chemical vapor deposition system.

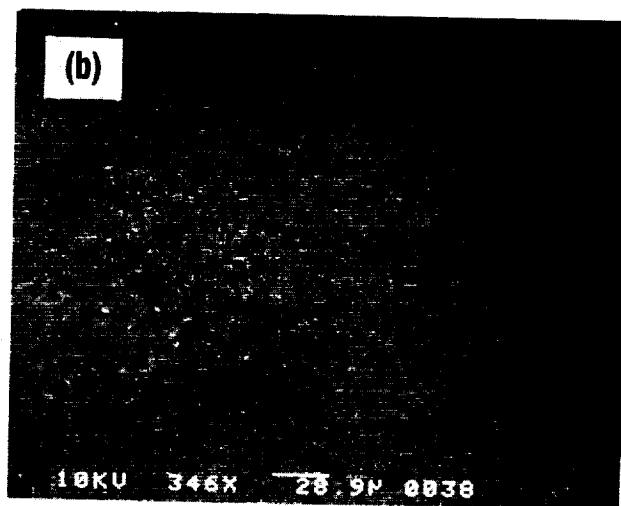


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Figure IV-3. - Silicon carbide crystal.



ON-AXIS (001) Si SHOWING
DEFECT (ANTIPHASE BOUNDARIES)



OFF-AXIS (001) Si SHOWING
ELIMINATION OF DEFECT

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Figure IV-4. - Scanning electron micrographs of SiC grown on silicon (Si).

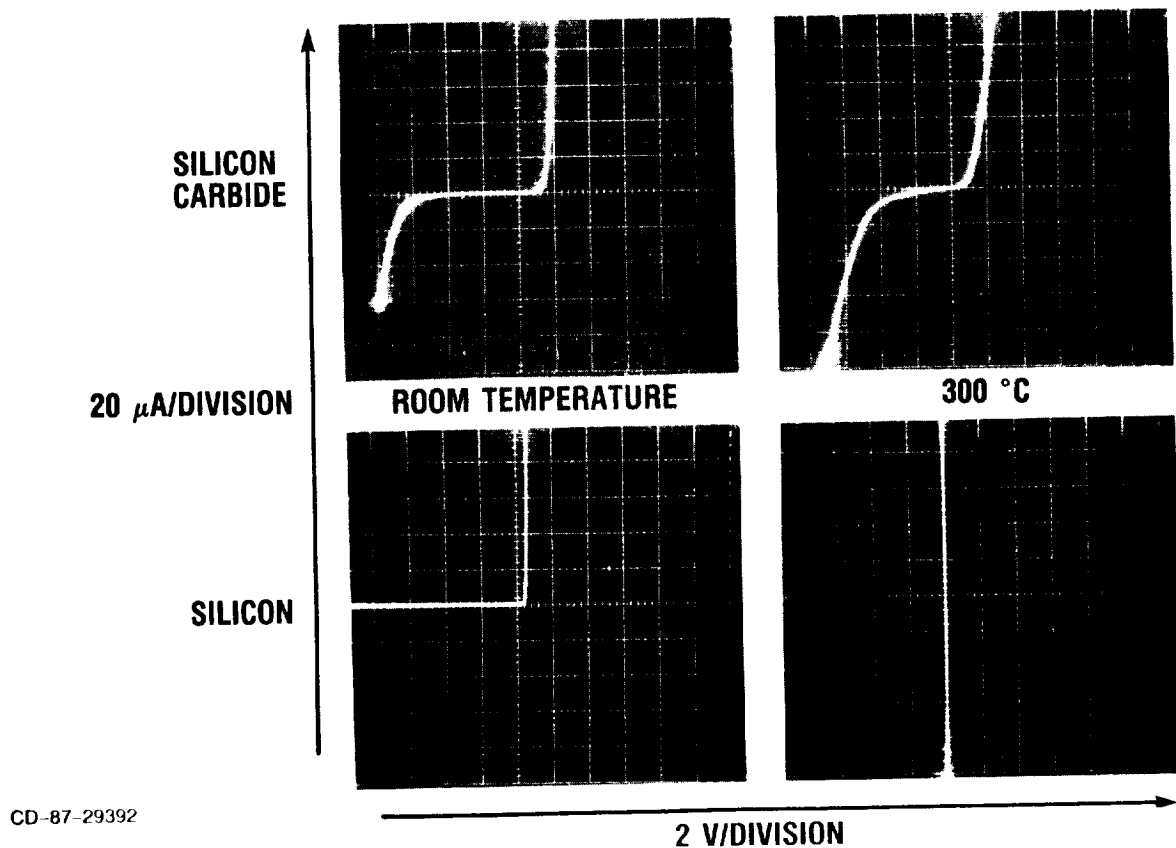


Figure IV-5. - Temperature characteristics of SiC and Si diodes.

CURRENT:

- CONTINUE PRESENT CVD STUDIES TO IMPROVE CRYSTAL QUALITY
- STUDY ALTERNATE CRYSTAL GROWTH METHODS
- CONTINUE DETAILED CHARACTERIZATION STUDIES
- CONTINUE DISCRETE DEVICE FABRICATION TECHNOLOGY RESEARCH
- CONTINUE CVD MODELING STUDIES

FUTURE:

- STUDY ALTERNATE CRYSTAL GROWTH METHODS
- CONTINUE DETAILED CHARACTERIZATION STUDIES
- DEMONSTRATE SIMPLE INTEGRATED-CIRCUIT TECHNOLOGY
- DEVELOP DEVICE METALIZATION AND PACKAGING TECHNIQUES
- DEMONSTRATE INTEGRATED-SENSOR TECHNOLOGY

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Figure IV-6. - Focus of current and future Lewis SiC research.

