National Aeronautics and Space Administration
Goddard Space Flight Center
Maryland

Modifications for a Communication Interface Board

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Acknowledgements

Through these lines, I would like to thank Dr. Clinton Lee for giving me the opportunity to be part of this Summer Goddard Graduate Intern Program. Also, I would like to thank the people at code 515 for their confidence, professionalism and friendship.

Jesus, my lord, my God ... thanks.

CDJ

Preface

This report is presented as a partial requirement for the completion of the Goddard Graduate Intern program. A description of the work developed as well as goals, procedures, and realizations are here summarized.

As a Goddard graduate intern, I had the opportunity to work in the Simulations and Compatibility Test branch (code 515) specifically in the Simulations Operations Section (code 515.2). This branch is responsible for developing and conducting simulations and compatibility test to stress and validate mission operations and data systems. Their resources are used in the initial check out of a flight mission interface with the space network (SN) and the ground network (GN). Among other responsibilities, they determine spacecraft compatibility with network tracking, telemetry, timing and command systems. They also verify compliance with Aerospace Data Systems Standards (ADSS) and conduct simulations for the purpose of training, development and interface verification.

My work at code 515.2 was related to the modification of a Communication Interface Board (CIB) using Erasable Programmable Logic Devices (EPLD). The interface will provide to Data General and Rolm computers (fig. # 1) a serial input/output link with the exterior world. The I/O board will enable the computer to simulate a spacecraft (fig. # 2) and allows the Simulation and Compatibility Test branch to test the Ground Network tracking, telemetry and

command parameters.

Objective

The objectives of the assignment are summarized next. First, it is to modify a Communication interface board by using Erasable Programmable Logic devices to replace standard SSI and MSI logic. Second, it is to simulate selected portions of the schematics using Altera Maxplus 1990 and Maxplus 2 1991 CAD programs. Finally, to replace a First Input First Output (FIFO) device as well as a serial to parallel an parallel to serial converters with new FIFO's that have internal converters.

Procedure

The Communication Interface Board is an input-output device designed to provide a serial path between Data General and Rolm computers and the outside world. Its operation mode is described as the following: a block of data or a frame of telemetry (fig. # 3) is received in series,

Block Transmission

Serial Transmission

Fig. # 3 Blocked and Serial Transmission.

the incoming data is compare to a synchronization pattern previously loaded in parallel by the computer to the CIB (fig # 4), a serial to parallel conversion is performed and the data is transferred directly into the computers memory. Two load pattern (loadpatt) and load mask (loadmask) signals are required since the sync pattern is 32 bits wide; the computer bus is only 16 bits. After comparing the data, one of three possibilities can arise: first, that the incoming data was not a sync pattern, second, that the incoming data matches the defined pattern (data true becomes asserted) and finally, that the received data be the inverse of the

predefined sync pattern, in which case, the data is said to be inverted. If the second possibility happens, the clock enable output signal in the correlator becomes asserted low and the data is received. If the third possibility occurs, the clock enable output signal becomes asserted low and the incoming data is first inverted and then received by the CIB. Otherwise, the incoming data is ignored. A copy of the simulation of the correlator circuit is included (fig. # 5).

Going back to fig. # 4, each box is nothing but a symbolic representation of a digital circuit created by a Computer Aided Design (CAD) program named Altera. This program allows engineers to accommodate exact equivalents of Small Scale Integrated (SSI) and Medium Scale Integrated (MSI) circuits into one single chip (fig # 6). The heart of an Altera Multiple Array Matrix (Max) EPLD is the Logic Array Block (LAB) (fig. # 7). It is composed of a macrocell array, an expander product term array and an I/O control block. A macrocell is a group of product terms (p-terms) (fig. # 8) feeding a sequential logic element while an expander is a group of uncommitted single product terms. A Max device consists of multiple LAB's linked together to through a Programmable Interconnect Array (PIA) (fig. # 9).

By using this technology, a Direct Memory Access (DMA) controller was redesigned (fig # 10). As in figure # 4 each box is nothing but a symbolic representation of an Altera device or that is to say, a digital logic circuit realizing a specific function. The architecture of Data General computers is described below to

and in the understanding of the CIB's operation.

The communication channel through which information passes between the computer and the CIB is called the I/O bus. Since it is shared by all the controllers as well as by the CPU, it is a half duplex bus so, only one operation occurs at a time. The information transferred between the computer and the CIB is classified into three groups: Status information, that tells the computer the state of the CIB; Control information, that tells the CIB what to do and Data information that can be read by the computer or written to the CIB. The information is transferred using one of the following controllers: the Programmed I/O (PIO) controller, in which a word (16 bits) or part of a word is transferred between an accumulator in the CPU and the CIB: the Data Channel (DCH) controller, through which a block of words is transferred (one word at a time) between the computers memory and the CIB: and the Burst Multiplexer Channel control, through which a block of words is transferred synchronously. The DCH transfer procedure is summarized as follows: a request for DCH bus is issued by the interface, bus access is granted, the address of a word is put in the computer bus, (16 bits bus) and the word is transferred. Each time a word is to be transferred, the procedure is repeated. Under the Burst Multiplexer Channel control, a burst of words is transferred once access is granted. The memory address (21 bits wide) and the number of words inside the burst needs to be specified in order to start the transmission.

The previous discussion presented a brief summary of the Data

General Computers structure. Now, the DMA controller can be discuss. The DMA controller is divided into four stages: word counter # 1 and word counter # 2, the burst counter, the address register, and a 4 to 1 16-bit multiplexer. The first stage receives the two's complement of the number of words to be transferred. Word counter # 1 is incremented by one each time a word goes into the FIFO. When an overflow occurs, or when all the words are in the FIFO, the word counter reloads itself and instruct the correlator to begin looking for new data again. Word counter # 2 (PR3CNTR) (fig. # 11) is incremented each time a word is transferred out of the FIFO. When an overflow occurs, a DONE flag becomes asserted and interrupts the computer. The computer then has the option of restarting the CIB, halting the CIB, or modifying control information. The word counter # 1 is read using the rising edge of the DIB control signal while the word counter 2 is read using the falling edge. It is done through a toggle flip flop and a multiplexer (see seqckt in fig. # 10). The PR4CNTR box in figure # 10 (see also fig. # 12) includes the address register (21 bits wide for the BMC and 16 bits for a DCH transmission) and the BMC burst counter which indicate the number of words per burst to be transferred. Finally, the 16 bits 4 to 1 multiplexer (16BCMUX) (fig. # 13) selects which register will be read by the computer. The following commands are used by the computer to control the CIB:

DOA - Load address

DIA - Read Address

DOB - Load word counter

DIB - Read word counter

DOC - Load BMC word

DIC - Read BMC word

Each stage was individually tested and its simulations are here included as well as the digital circuit logic inside each symbolic representation.

To avoid a lack in systems performance due to different transfer rates between the computer and the CIB, First Input First Output (FIFO) memory buffers are required. FIFOs allow data to be stored and read sequentially. Serial to parallel / parallel to serial conversions can also be performed by using IDT 72103 CMOS parallel-serial FIFOs. For instance, in the modified CIB, this single chip replaces the old FIFOs and the serial to parallel / parallel to serial circuit associated to it. Figure # 14 shows how the IDT 72103 CMOS are connected. The SI/PI pins are grounded telling the chip that the incoming data will be transferred in series. The input pins Di (i from 0 to 8) are used to indicate the size of the word. For instance, the word wide is 7 bits while in the first chip, it is 9 bits wide. Pin D8 in chip # 1 is connected to SIX of chip # 2 to create an expansion (9 bits from chip #1 plus 7 bits of chip # 2 equal to a 16 bits word). Each time a 16 bits word is read, a WRITE pulse is sent through the D6 pin. To transfer the data to the computer bus, a read pulse must be sent.

Illustrations

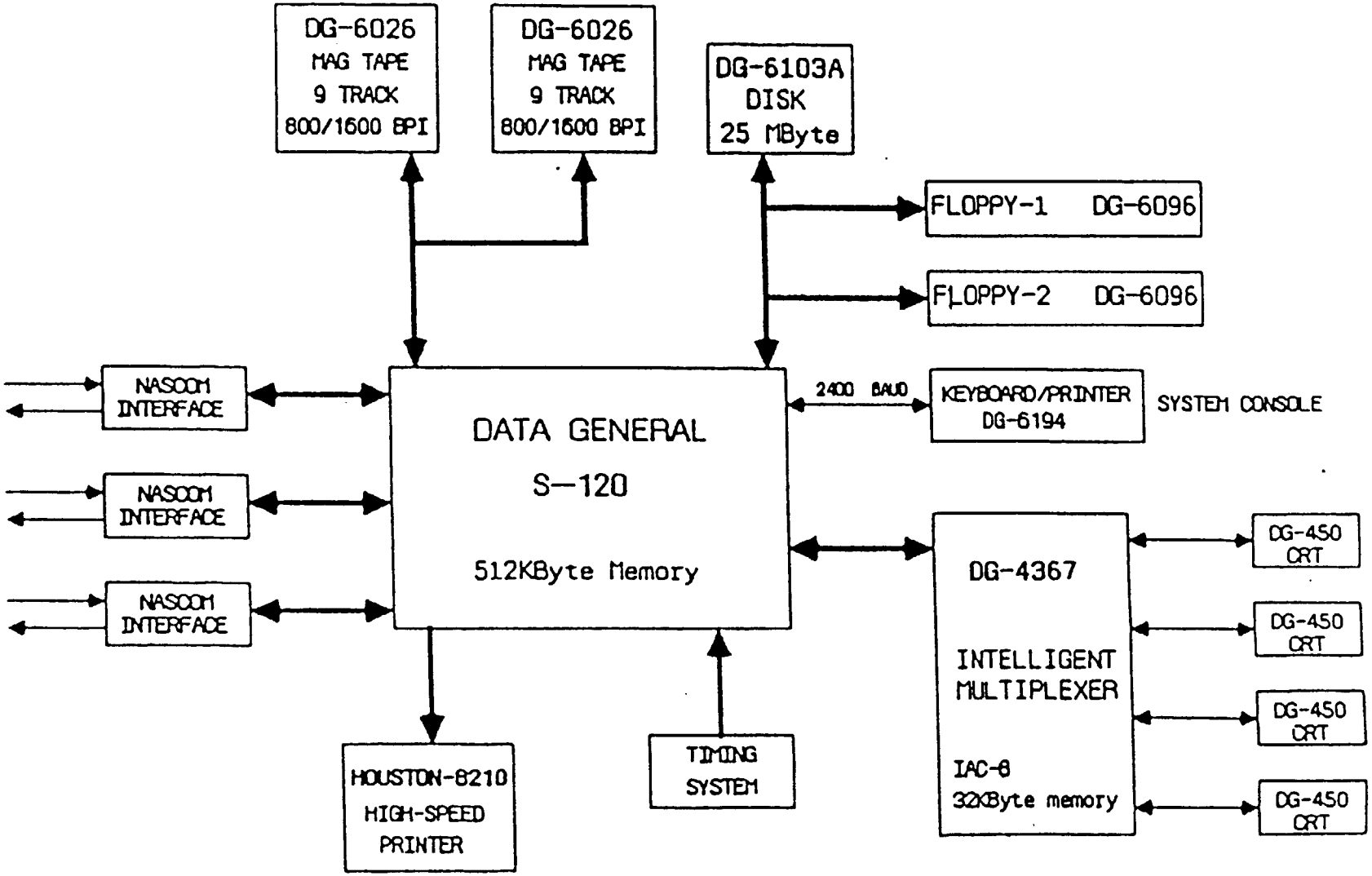


Fig. # 1 Data General S-120 System

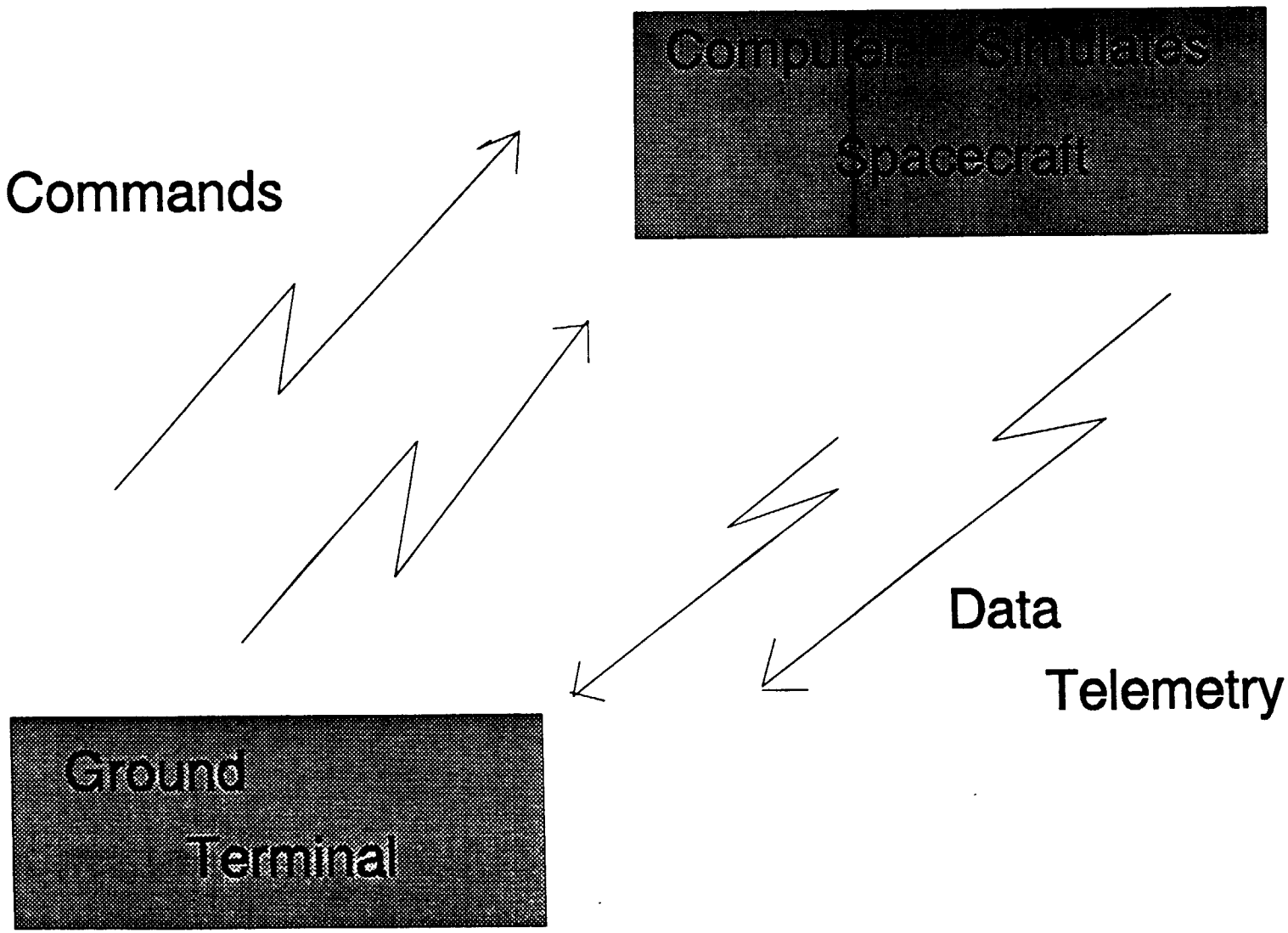


Fig. # 2 An application for the CIB.

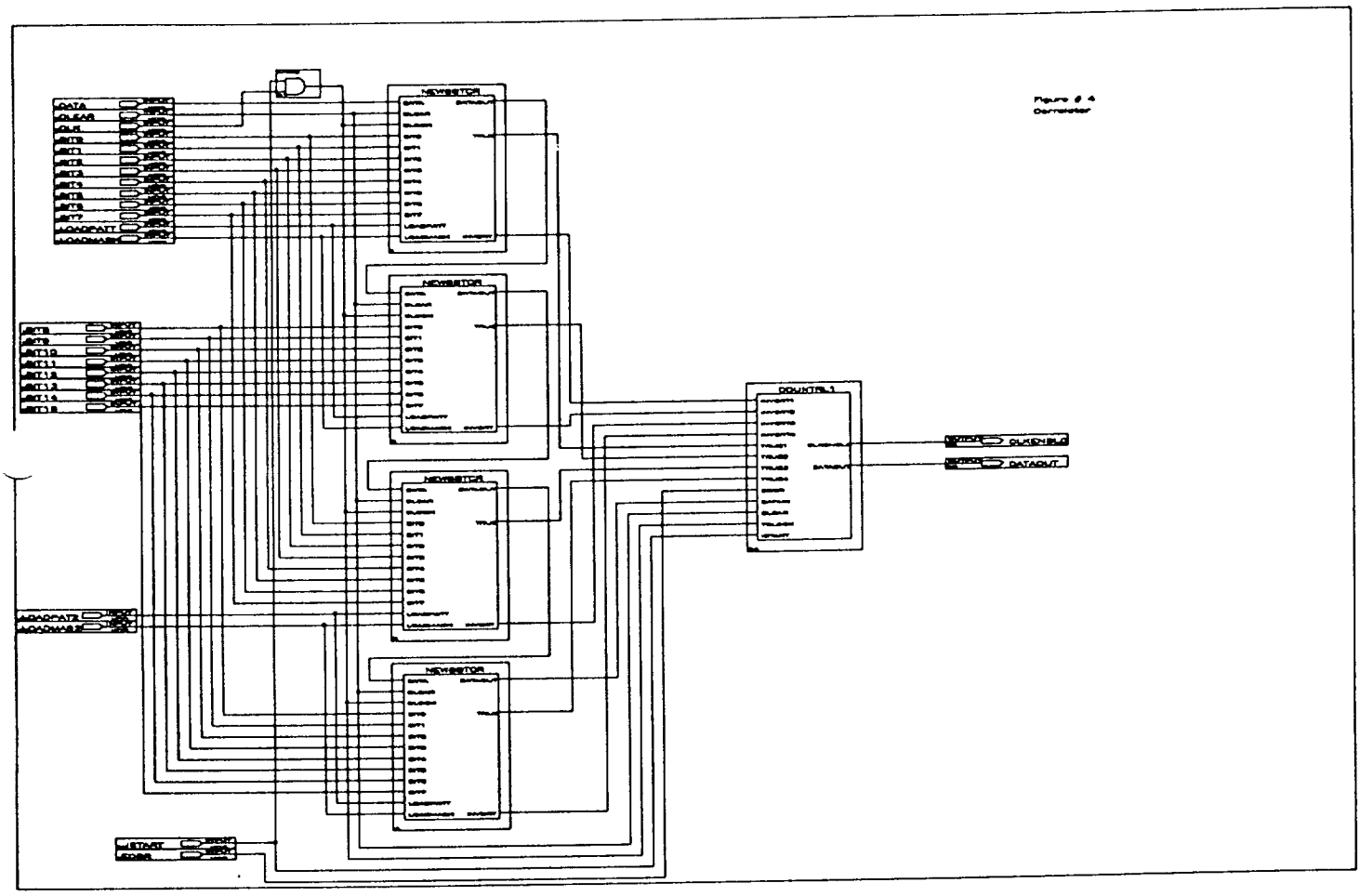


Fig. # 4 Correlator

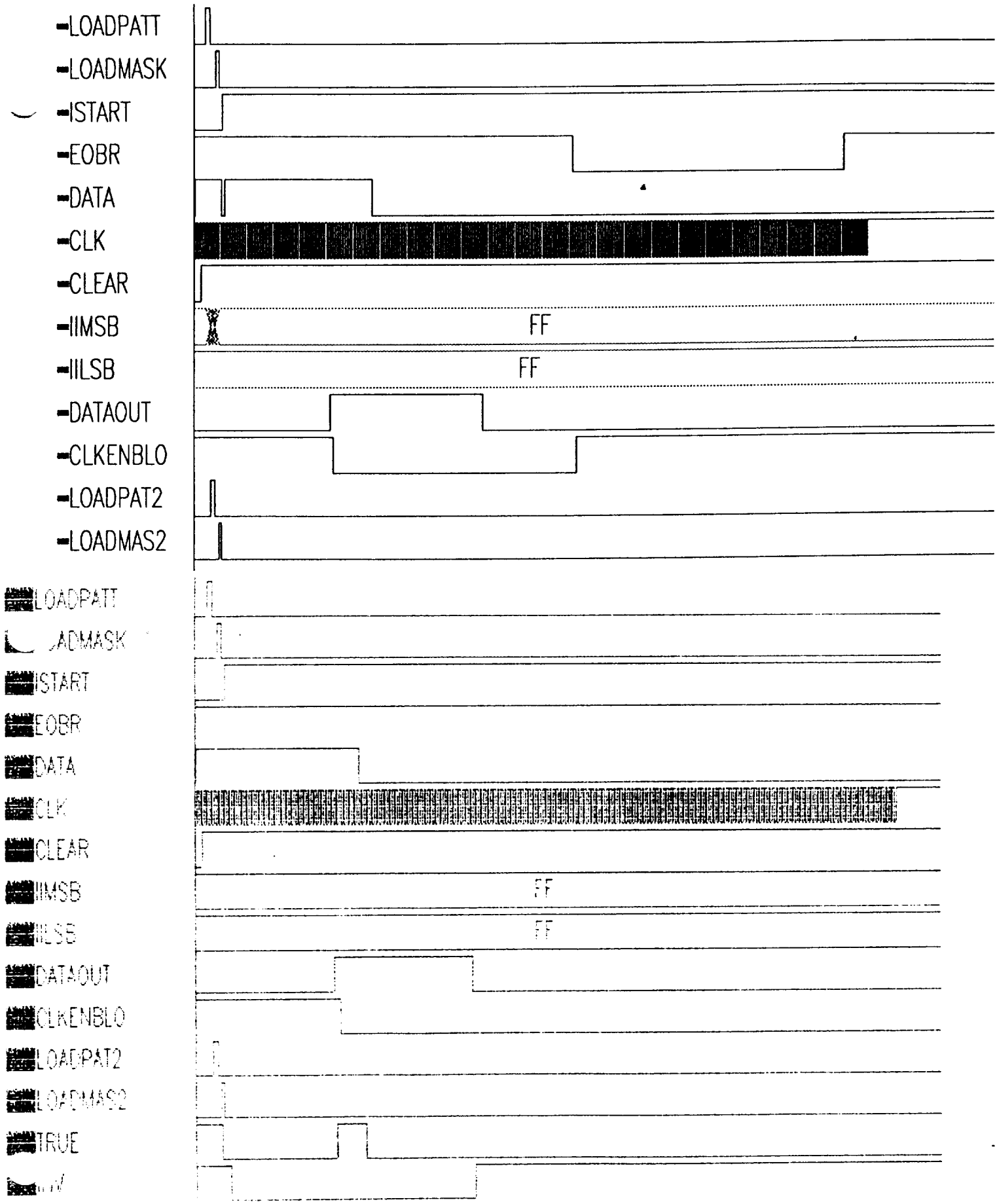


Fig. # 5 Correlators Simulation

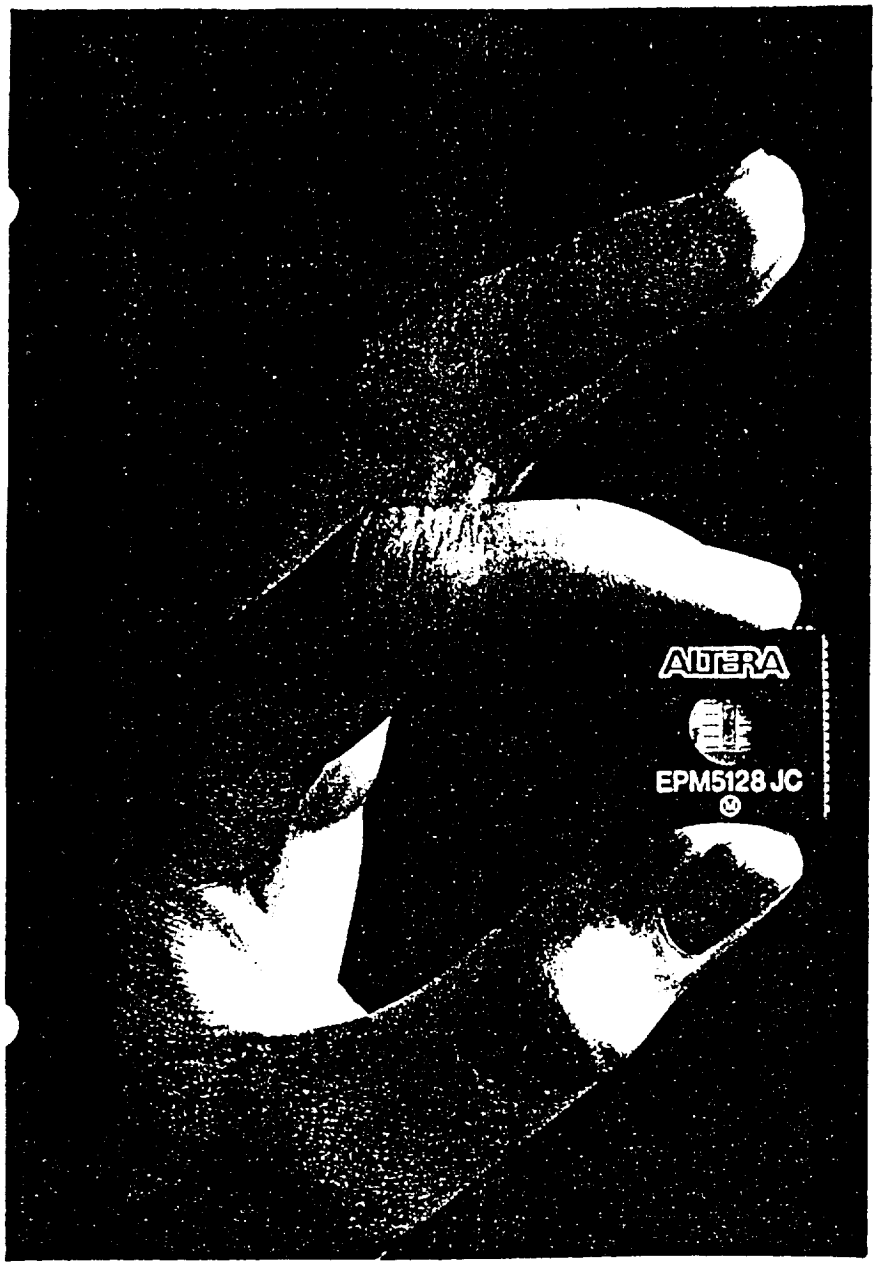


Fig. # 6 Altera EPM128 Chip

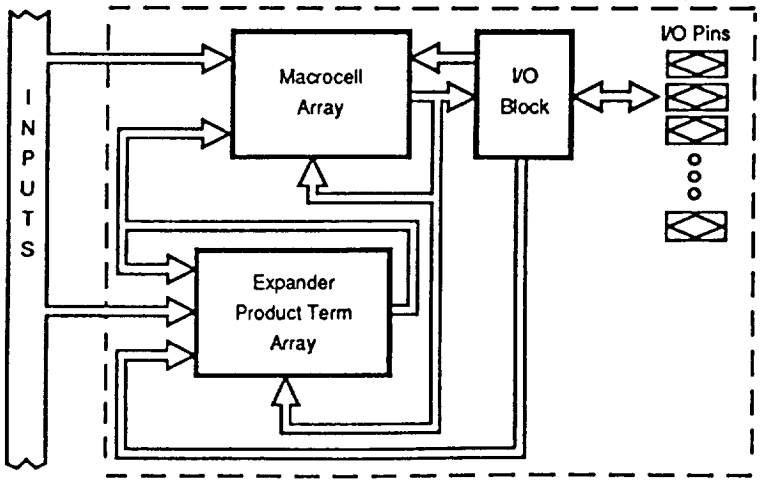


Fig. # 7 Logic Array Block

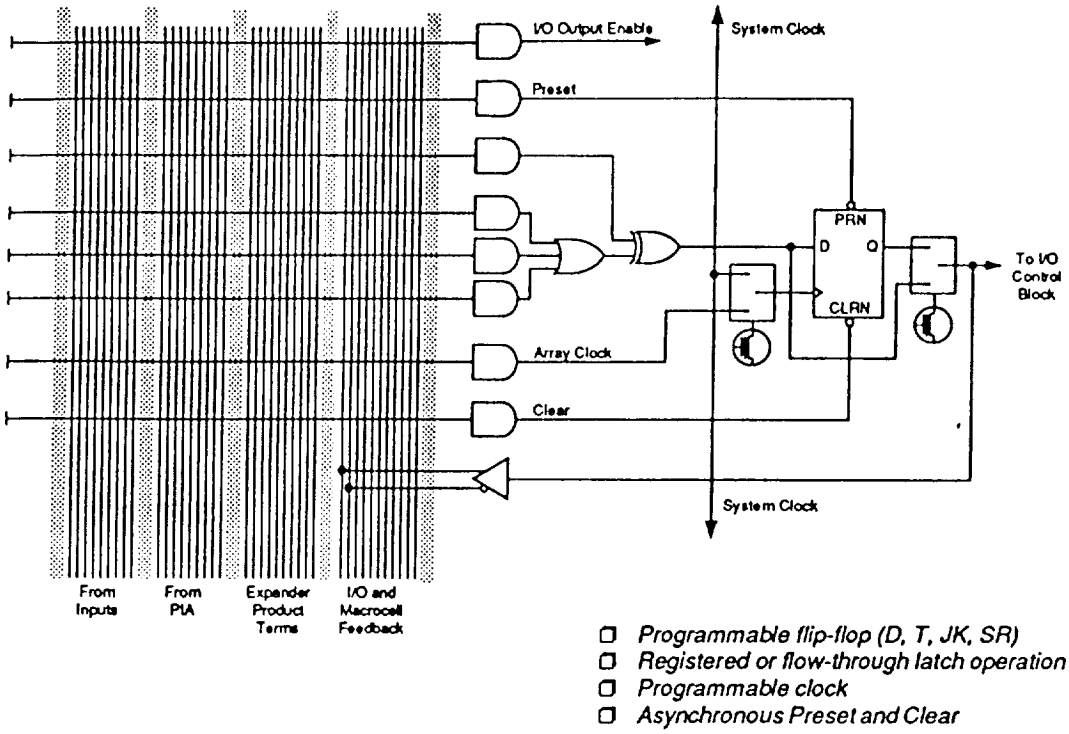


Fig. # 8 Macrocell Block Diagram

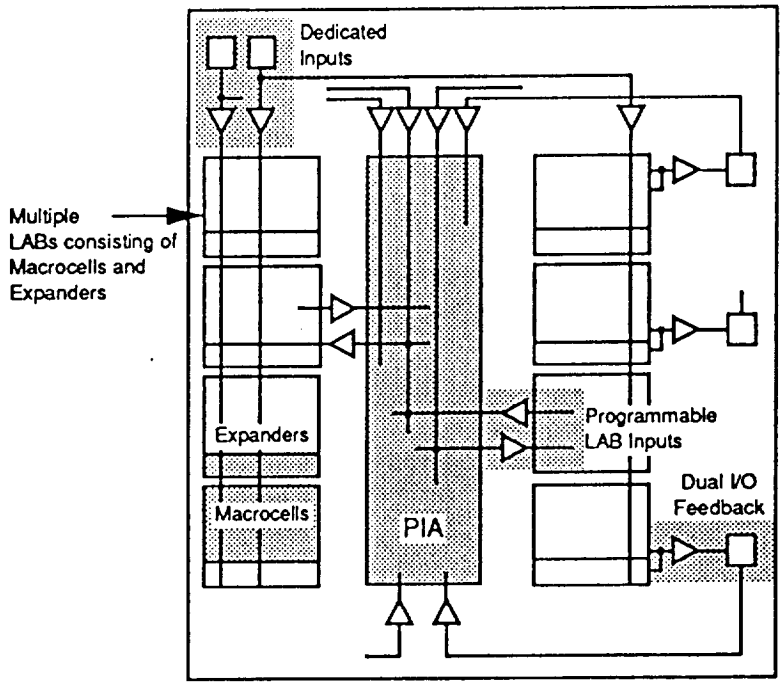


Fig. # 9 Programmable Interconnect Array Diagram

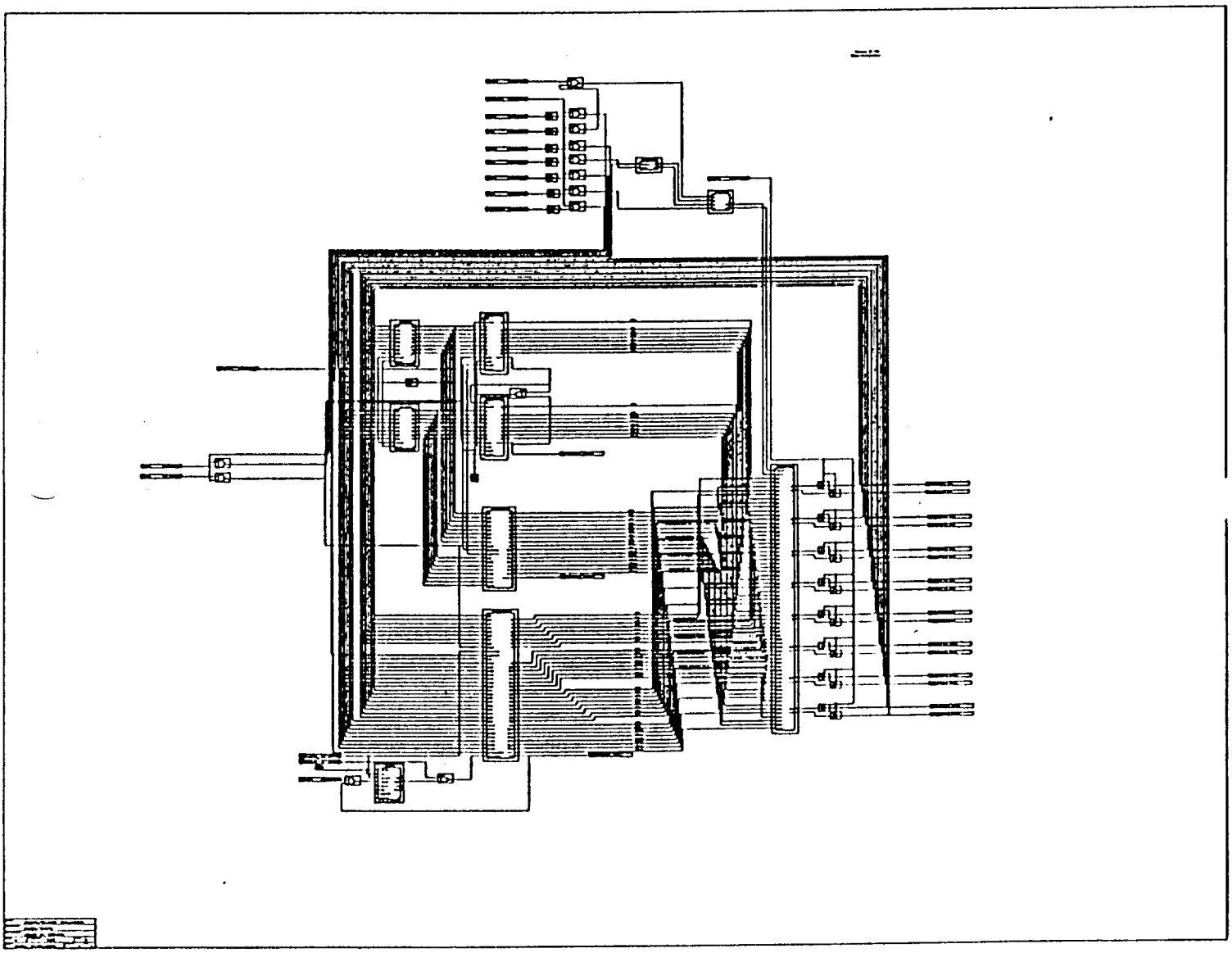


Fig. # 10 DMA Controller

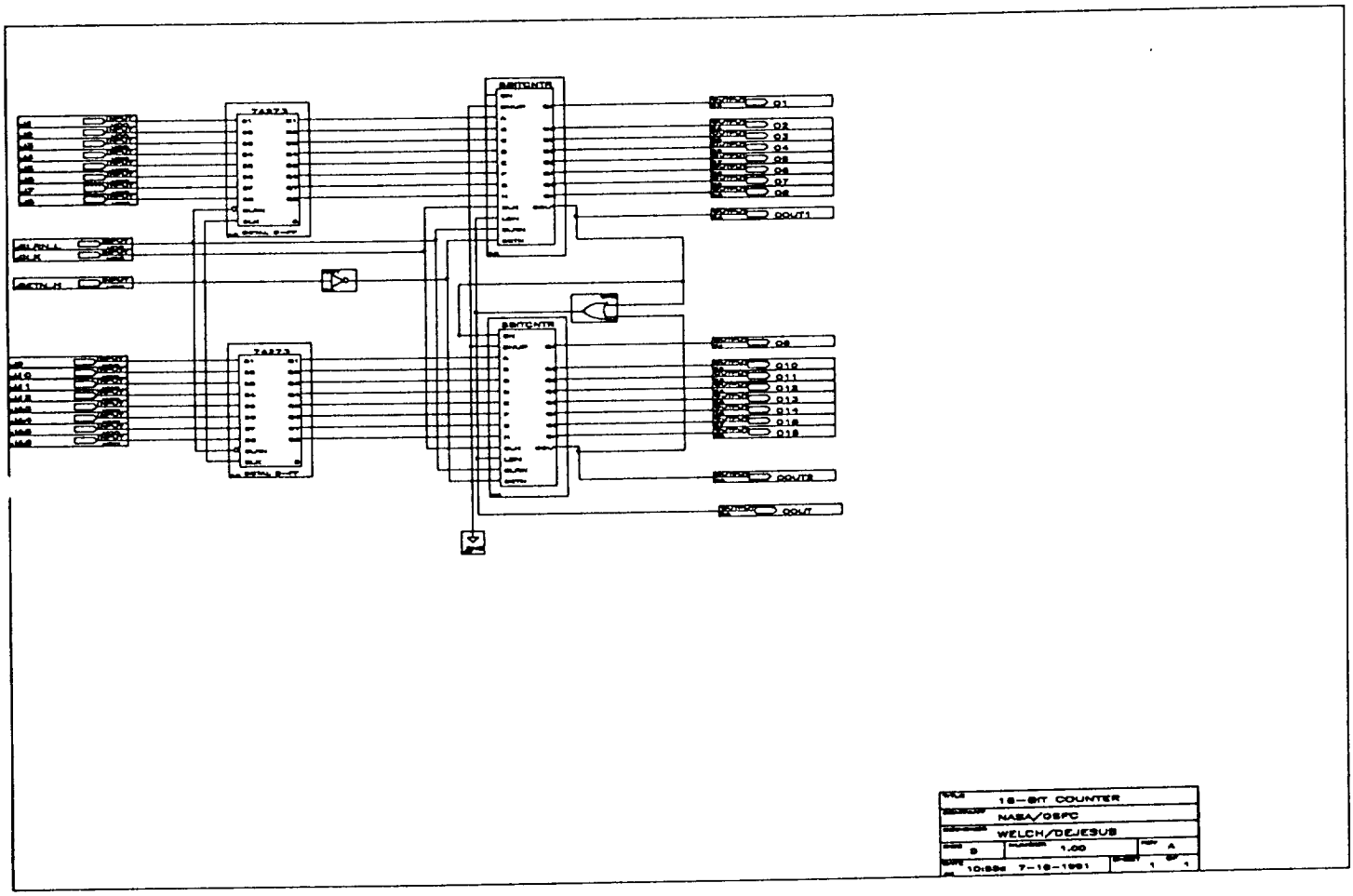


Fig. # 11.1 Word Counter # 1

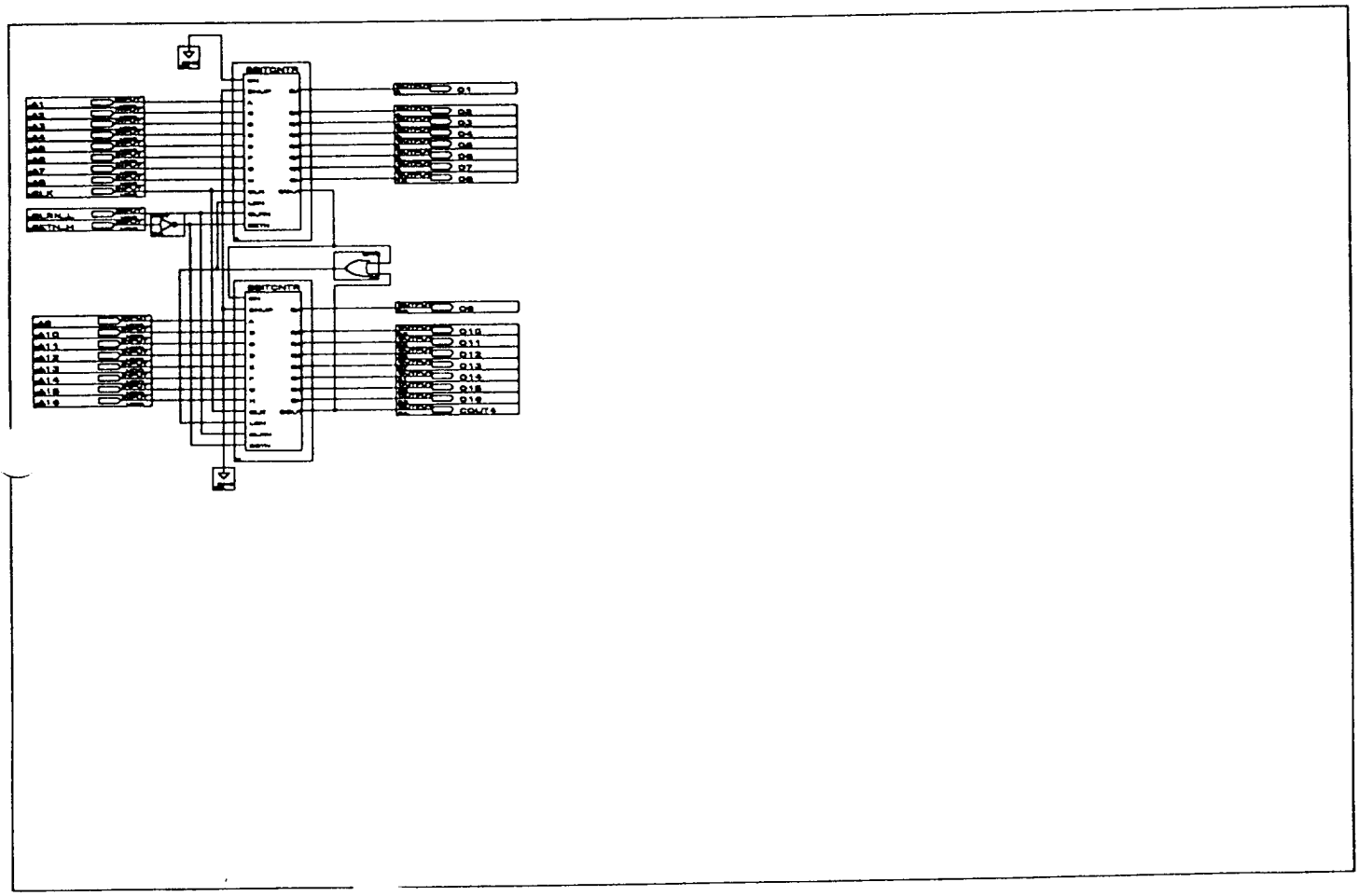
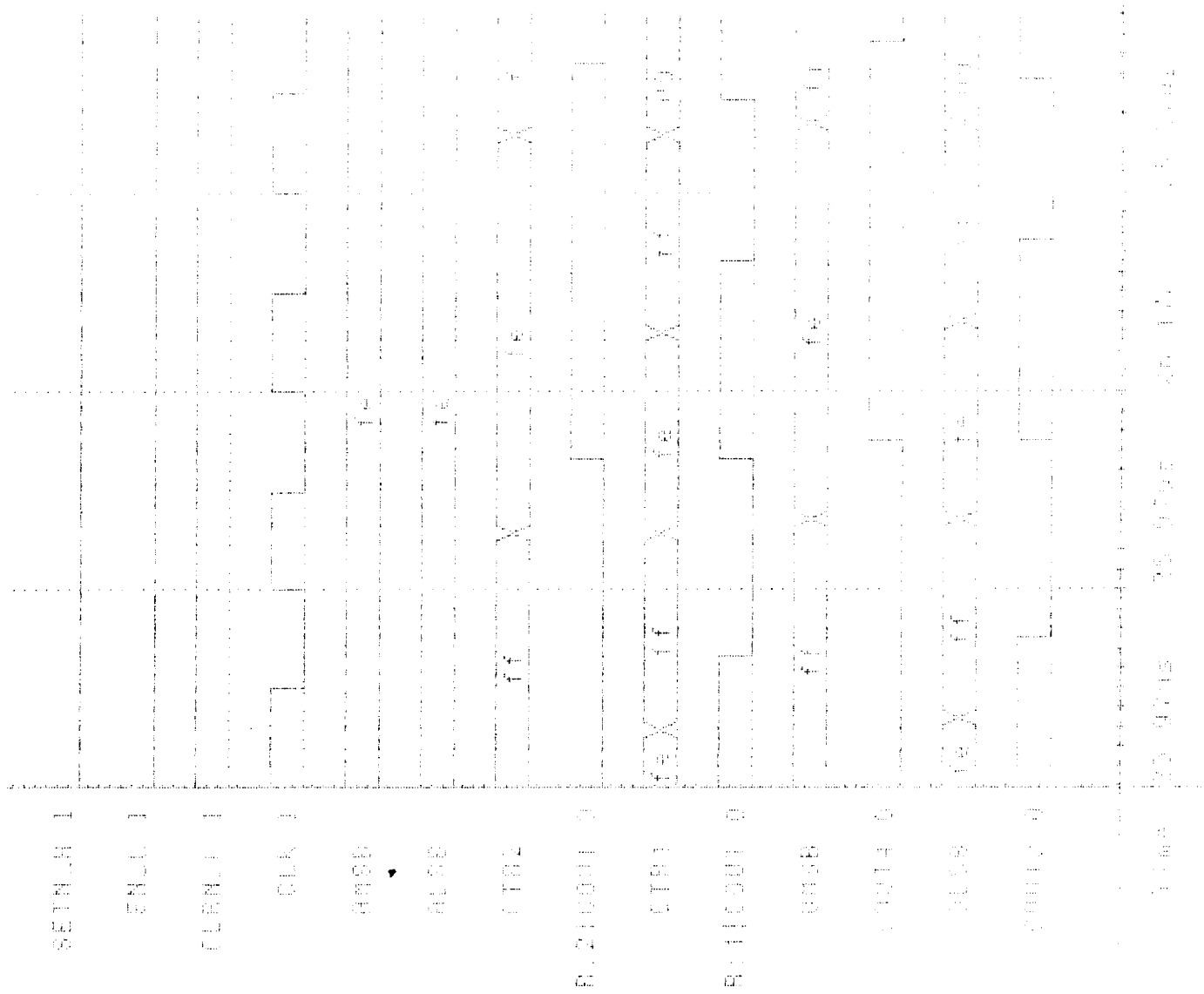


Fig. # 11.2 Word Counter # 2



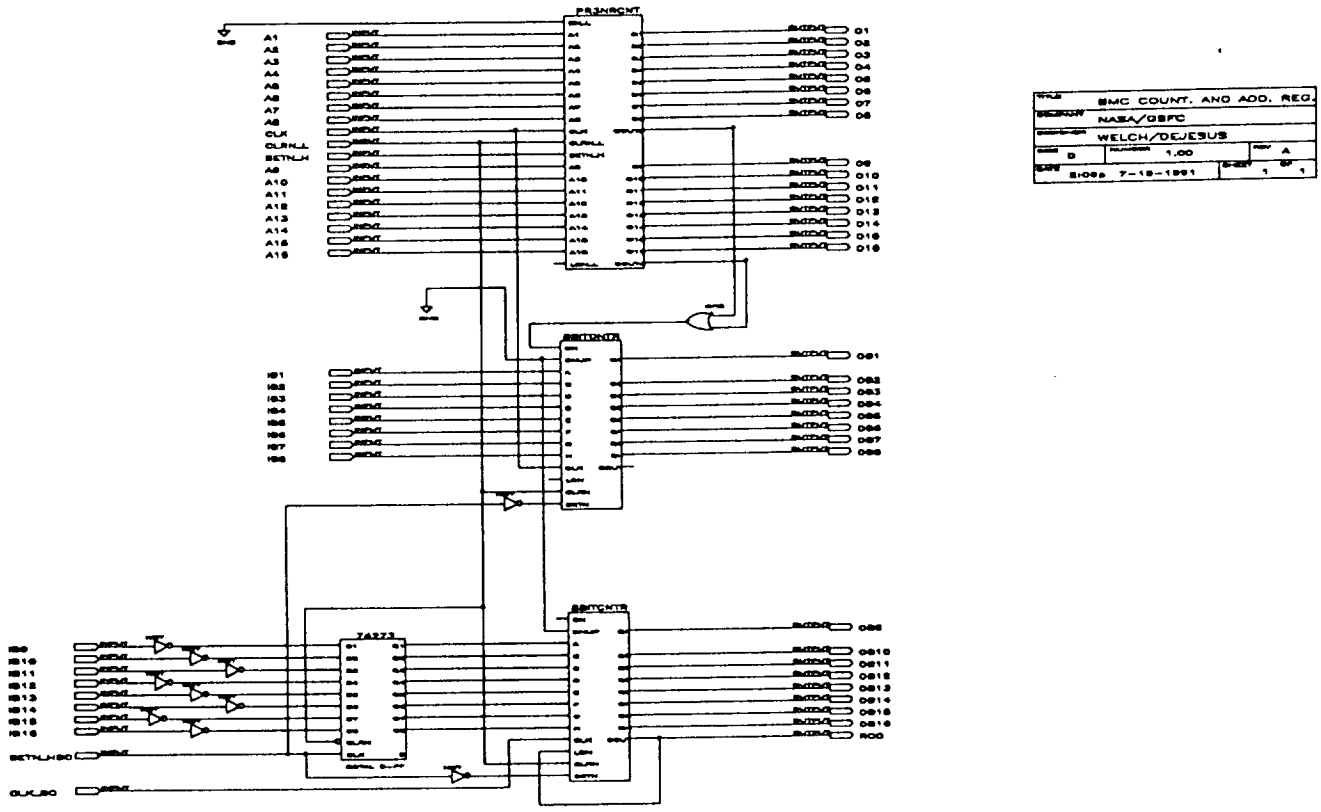


Fig. # 12 Address Register and BMC Counter

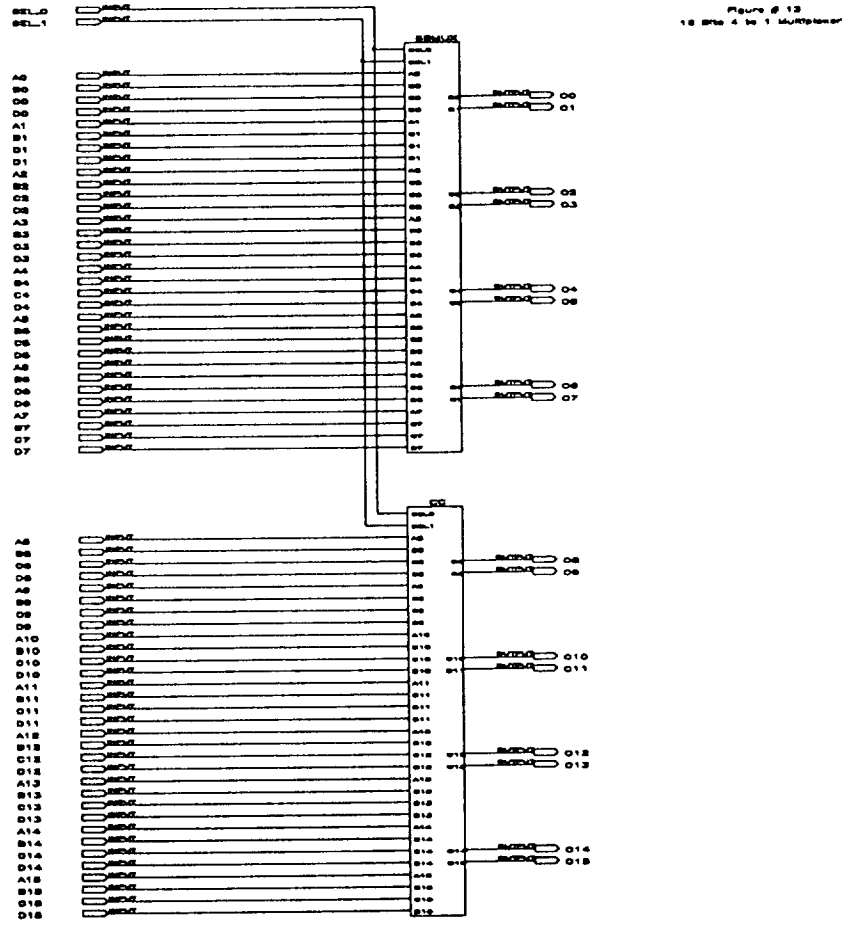
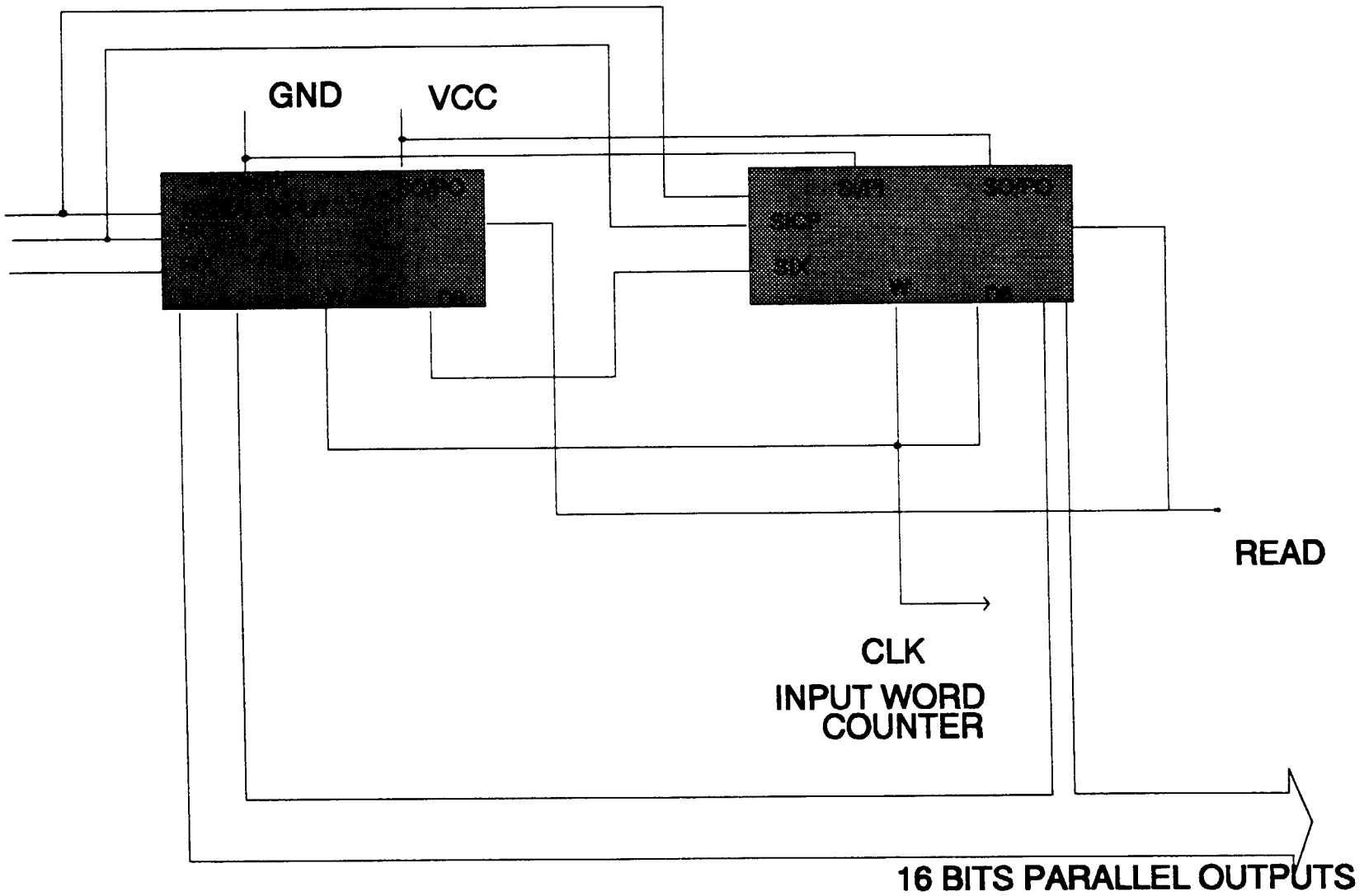


Fig. # 13 16 Bits 4 to 1 Multiplexer

FIG. # 14 SERIAL-PARALLEL FIFO BUFFER



Results

The results of the assignment are summarized as follow:

- Modifications for a communication interface board had been performed. Its DMA controller as well as its Correlator had been reduced to two single chip.

- Each part in the Correlator as well as in the DMA was individually tested to ratify its behavior.

- The Correlator was also simulated as a whole that is to say, with all its parts linked together. With respect to the DMA , it could not be simulated due to unrecoverable application errors in Microsoft Windows. Nevertheless, a copy of all the schematics was sent to Altera's bulletin board system in order to determine the nature of the problem and how to solve it.

Bibliography

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Altera Maxplus 2 Manuals, The Altera Corporation, San Jose CA., 1991

Eclipse MV/2000 Series Interface Designer Guide, Data General Corporation, USA, 1986

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Appendix

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Modifications for a Communication Interface Board

Carlos E. De Jesus Lafuente
University of Puerto Rico
Mayaguez Campus

Goddard Graduate Intern Program
Summer 1991

Objectives

- TO MODIFY A COMMUNICATION INTERFACE BOARD USING EPLD

-TO SIMULATE SELECTED PORTIONS OF THE SCHEMATICS USING ALTERA 1990 AND ALTERA 1991

-TO USE NEW FIFO'S WITH INTERNAL SERIAL-PARALLEL CONVERTERS IN THE MODIFIED CIB

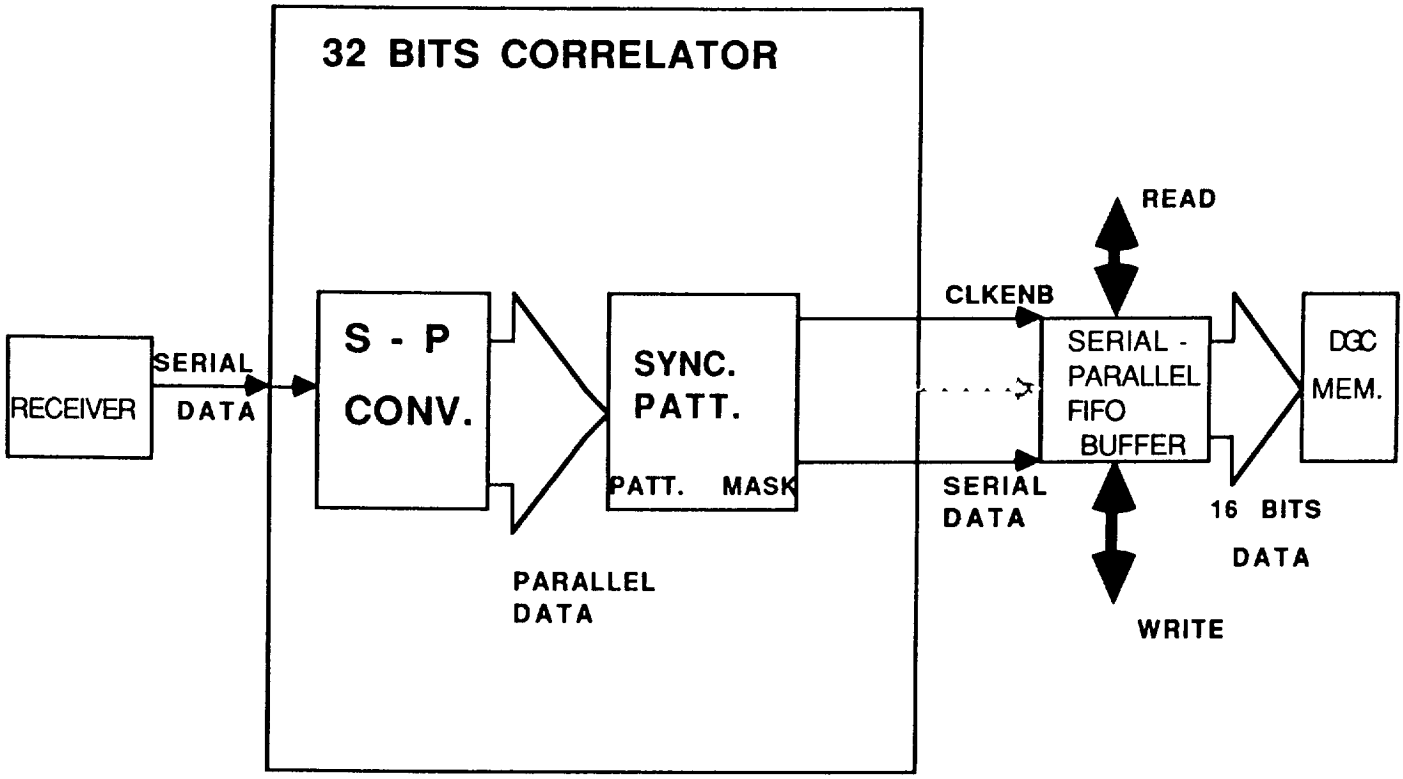
SIGNIFICANCE

- THE CIB WILL ALLOW OUR BRANCH TO USE DATA GENERAL AND ROLM COMPUTER TO SIMULATE SPACECRAFT.

- TO VALIDATE SPACE CRAFT COMPATIBILITY WITH NETWORK TRACKING AND COMMAND PROCEDURES.

- TO REDUCE THE SIZE OF THE CIB LOGIC CIRCUIT AND MINIMIZE THE SIZE OF THE BUS.

- TO MINIMIZE ERROR SOURCES SUCH AS NOISE AND TO AVOID WASTE OF TIME IN TROUBLE SHOOTING.


32 BITS CORRELATOR
RECEIVER
SERIAL
DATA
S - P
CONV.
SYNC.
PATT.
PATT.
MASK
PARALLEL
DATA
CLKENB
READ
SERIAL -
PARALLEL
FIFO
BUFFER
SERIAL
DATA
16 BITS
DATA
WRITE
DGC
MEM.

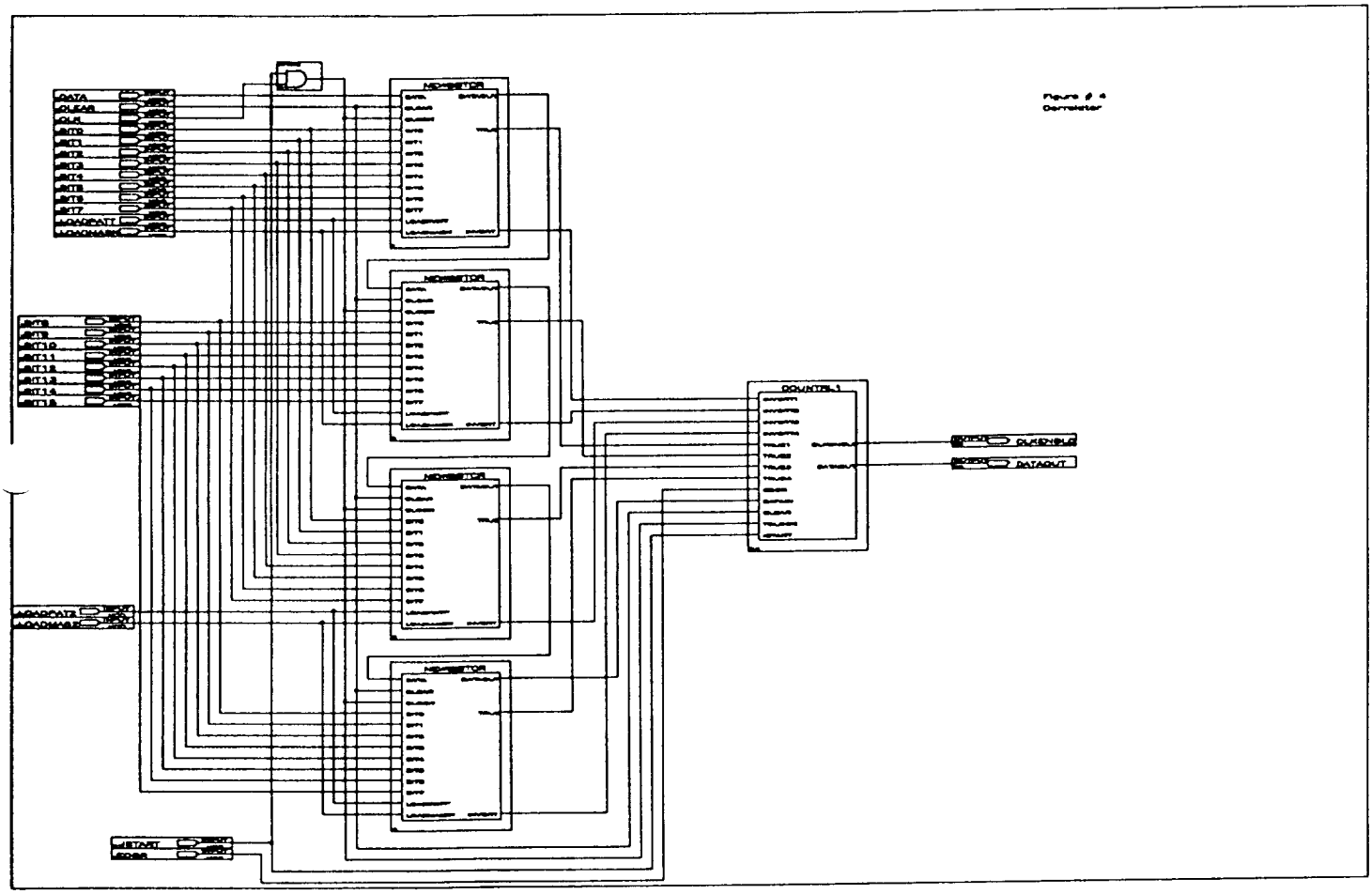


Fig. # 4 Correlator

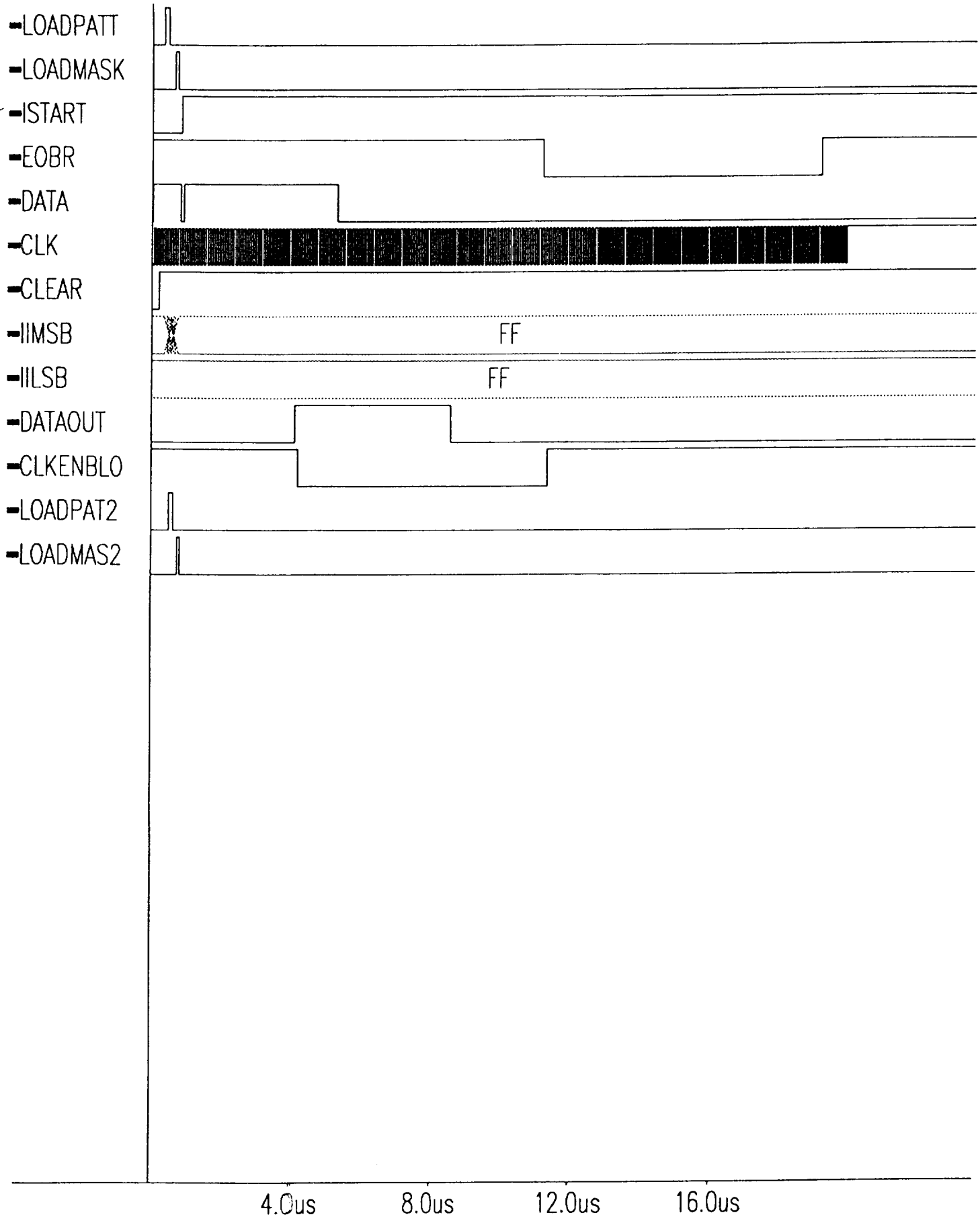
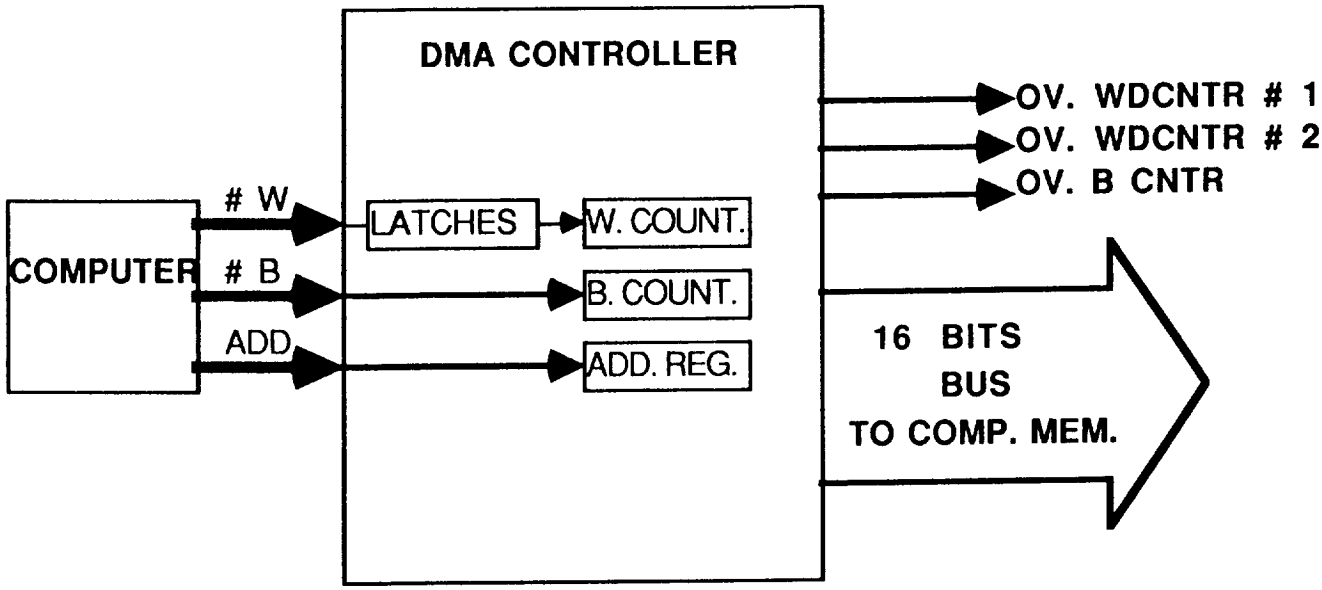


Fig. # 5 Correlators Simulation


DMA CONTROLLER
COMPUTER
W
B
ADD
LATCHES
W. COUNT.
B. COUNT.
ADD. REG.
OV. WDCNTR # 1
OV. WDCNTR # 2
OV. B CNTR
16 BITS
BUS
TO COMP. MEM.

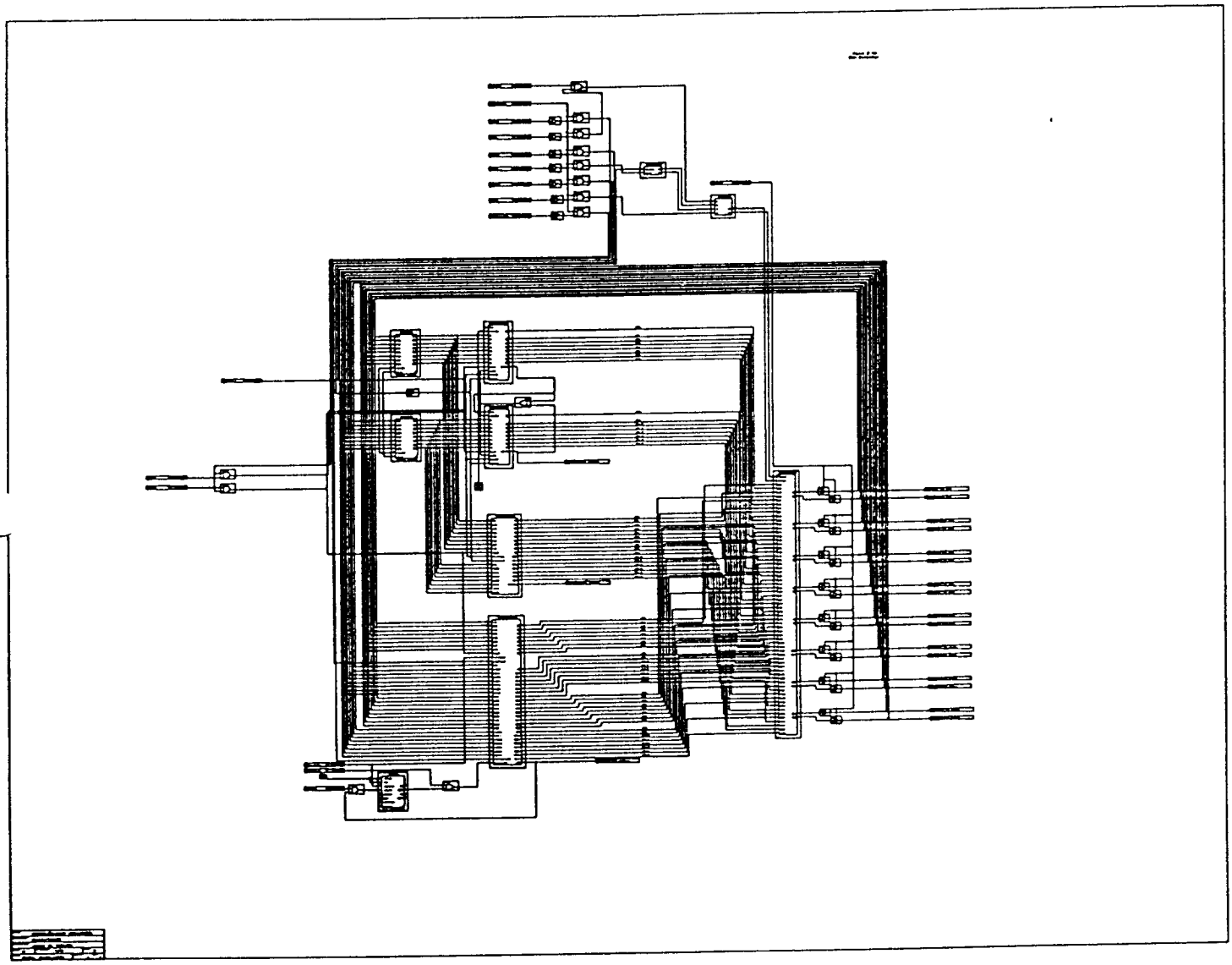


Fig. # 10 DMA Controller