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An Implementation of a Reference Symbol Approach to Generic Modulation in Fading Channels

R.J. Young, J.H. Lodge and L.C. Pacola

Communications Research Centre, Ottawa, Canada

ABSTRACT

As mobile satellite communications systems evolve over the next decade, they will have to adapt to a changing tradeoff between bandwidth and power. This paper presents a flexible approach to digital modulation and coding that will accomodate both wideband and narrowband schemes. This architecture could be the basis for a family of modems - each satisfying a specific power and bandwidth constraint yet all having a large number of common signal processing blocks. The implementation of this generic approach, with general purpose digital signal processors for transmission of 4.8 kbps digitally encoded speech, is described.

I. INTRODUCTION

As mobile satellite communications systems evolve over the next decade, they will have to adapt to a changing tradeoff between bandwidth and power. Initial systems using existing satellites are power limited and thus power efficient modulations such as rate 1/2 coded BPSK are appropriate. Future higher power satellites are expected to be bandlimited. When these spacecraft are in service bandwidth efficient modulations such as trellis coded modulation will be more appropriate.

This evolution provides the impetus for the definition of a flexible and easily adapted modem architecture that achieves robust digital communications over fading channels. In this paper we define such an architecture that maintains a large number of common signal processing blocks while accomodating various coding rates and signal constellations. This approach to modem design will allow a modular DSP software implementation to rapidly evolve from a power efficient modulation to a bandwidth efficient modulation.

II. THE REFERENCE SYMBOL APPROACH

Robust communication in the presence of fading can be achieved by performing some form of channel estimation and compensation at the receiver. A proven method for obtaining channel estimation is achieved by transmitting a known signal along with the information bearing signal. The receiver uses this known signal to estimate the multiplicative distortions introduced by the channel and subsequently to remove them from the received information bearing signal. This technique is often referred to as feed-forward signal regeneration (FFSR). The frequency domain approach to providing a reference signal is to allocate a portion of the transmit spectrum to a pilot tone [1,2]. The disadvantages of this approach are that the position of the pilot tone can constrain the choice of modulation and/or affect the performance of the FFSR. Also, the pilot tone will disturb the envelope properties of those modulations that have been designed with approximately constant envelope for use over nonlinear channels.

Recent papers [3,4] introduced a time domain analogue of the pilot tone which has similar power and bandwidth requirements but not the disadvantages described above. In the time domain scheme a sequence of symbols that is known to the receiver is multiplexed with the coded information symbols before transmission. When synchronized the receiver demultiplexes the reference samples and uses them to obtain channel estimation and compensation. The multiplex ratio of the reference sequence is M to 1, that is, M code symbols are transmitted between each reference symbol. The reference symbol rate ($1/M$ times the code symbol rate) must be at least twice the fading rate in order that Nyquist sampling of the channel is achieved. The reference symbols use $1/(M+1)$ of the transmit power and bandwidth. This allocation is recovered when one considers that receiver can use a form of coherent detection in channels that normally require differential detection.

The reference symbols are the foundation of our generic approach to modulation and coding in fading channels. As well as providing a form of coherent detection through channel tracking they can also provide the receiver with a means of achieving its

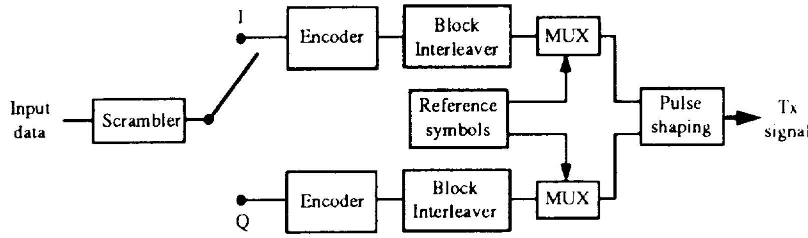

Fig.1. A block diagram of the signal processing in the transmitter.

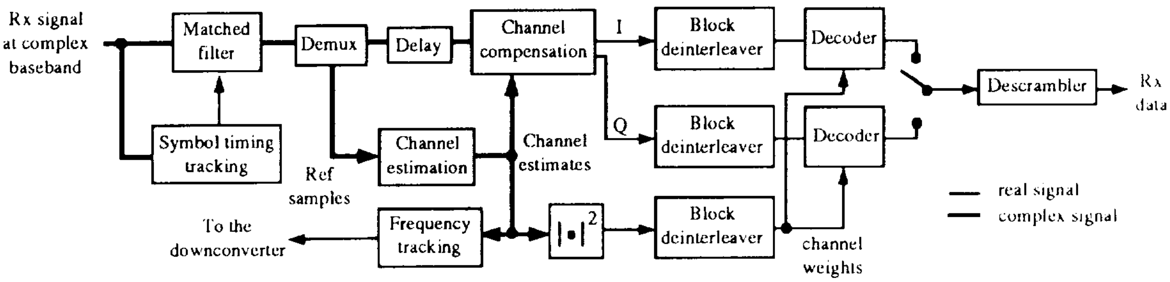

Fig. 2. A block diagram of the signal processing in the receiver.

other tracking functions (symbol timing tracking, frequency tracking and signal health tracking) independent of the signal constellation chosen. Therefore, a family of modems each with different coding rates (power efficiencies) and signal constellations (bandwidth efficiences) can be built from a common set of signal processing blocks.

A. Transmitter

The structure of the transmitter is shown in Fig. 1. The information bits are first scrambled to ensure that they have suitable randomness and then they are alternately sent to the I and Q channels. The I and Q bits are independently encoded and interleaved. Interleaving distributes the burst errors caused by the fading channels thereby improving decoder performance. The interleaver output is time division multiplexed with the reference sequence and the resulting composite symbol sequence is filtered to achieve the desired transmit spectrum.

B. Receiver

The signal processing section of the generic receiver, as shown in Fig. 2, assumes a complex baseband input signal sampled at twice the symbol rate, $f_s = 2f_r$. To recover the transmitted symbols the received signal is filtered by a filter matched to the transmitter's pulse shaping filter. The demultiplexor separates the reference samples from the code samples. The reference samples are used to estimate the channel gain and phase at the code symbol times. This channel state information is used to compensate the code samples thereby producing a "pseudocoherent" estimate of the received code sequence and to provide side information to the decoder. The I and Q code samples and the channel samples are deinterleaved and passed to the I and Q decoders. The decoded bits in the I and Q channels are recombined and descrambled to recover the transmitted data.

The signal processing to obtain the channel estimates from the reference symbols is shown in Fig. 3. The received reference samples are multiplied by the conjugate of the known transmitted sequence to produce samples of the channel at the reference symbol rate. The channel samples are lowpass filtered and then interpolated to produce estimates of the channel at each of the code sample times between the reference samples.

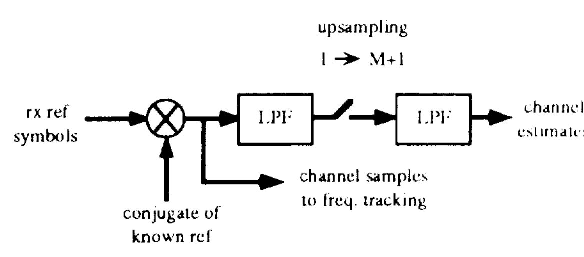

Fig. 3 Signal processing for channel estimation

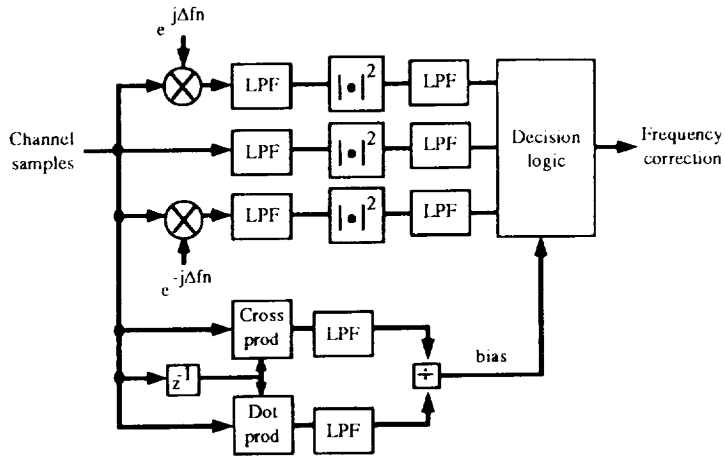

Fig. 4. A block diagram of the frequency tracking processing.

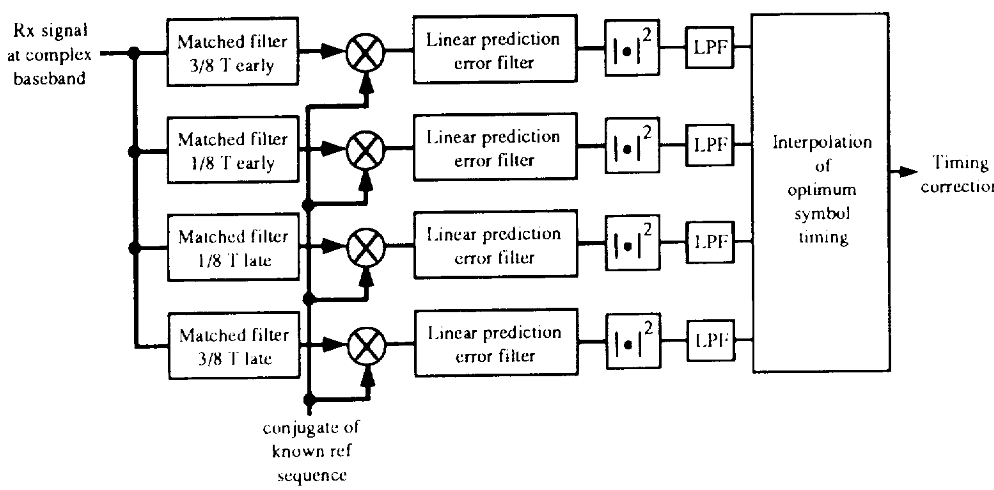

Fig. 5. A block diagram of the symbol timing tracking processing.

The receiver's frequency tracking function uses the channel samples from Fig. 3 before the noise rejection filter. The objective of the algorithm shown in Fig. 4 is to maximize the energy in the channel samples at the output of the noise rejection filter. This is done because the channel estimation and compensation process is able to make use of the multipath energy in the received signal. The channel samples are filtered in three parallel paths by frequency shifted versions of the noise rejection filter. One path contains the filter shifted by $-\Delta f$ Hz, another path contains the filter shifted by $+\Delta f$ Hz, and the final path contains the centered filter. Δf defines the resolution of the frequency tracking. The power at the output of each filter is computed and filtered. Decision logic attempts to make frequency corrections in order to maximize the power at the output of the centered filter. An additional bias signal is computed which tracks the direct path component of the channel. In static or slow fading channels the bias signal will pull the direct path towards the center of the noise rejection filter instead of allowing the received signal to wander back and forth over the maximum expected fading bandwidth.

The symbol timing tracking algorithm shown in Fig. 5 also makes use of the reference symbols. This algorithm uses an early/late detection approach to find the timing that minimizes the intersymbol interference (ISI) at the output of the matched filter. Outputs from each of a parallel bank of 4 matched filters with detection time offsets of +3/8, +1/8, -1/8, -3/8 of a symbol period respectively are obtained only during reference symbol detection periods. These outputs are multiplied by the conjugate of the known transmitted reference

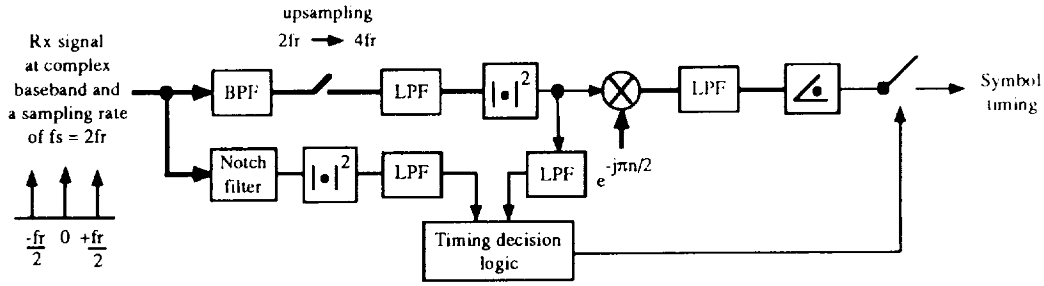

Fig. 6. A block diagram of the symbol timing acquisition processing.

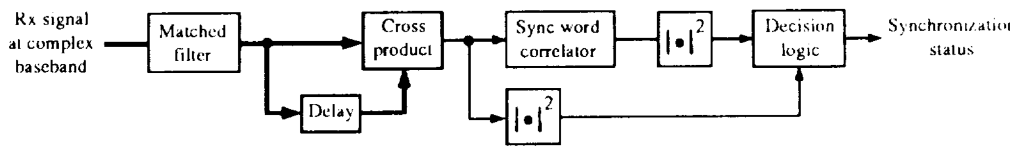

Fig. 7. A block diagram of the synchronization detection processing.

sequence. For a branch which corresponds to exact symbol timing the matched filter will detect the reference symbol without ISI and the multiplication with the known symbol will produce a signal with a bandwidth equal to the fading bandwidth. For a branch with some timing offset the matched filter output will include ISI and the following multiplication will produce a signal with a bandwidth larger than the fading bandwidth. Processing continues through a linear prediction error filter designed assuming a nominal fading spectrum. This filter acts like a highpass filter where the bandwidth of the stopband equals the fading bandwidth. The error filter output for correct timing will be small compared to the error filter output for incorrect timing. The error filter outputs are squared and filtered to produce power signals for each of the detection offsets. These power values define a detection performance versus timing offset surface where the optimum sampling time is found at the minimum. The performance surface samples are interpolated at points between $\pm 1/8$ of a symbol period timing offset to find the position of the minimum and hence the optimum timing.

C. Synchronization

The receiver requires that synchronization with the incoming sample sequence be obtained so that the demultiplexor can properly extract the reference samples and so that the block deinterleaver, decoder and descrambler can be properly initialized. Therefore, each data burst must be preceeded by a preamble that will allow synchronization to be found. Our strategy is to transmit a known timing pattern followed by a synchronization word. The timing pattern allows the receiver to obtain symbol timing before searching for the synchronization word. The signalling during the preamble was chosen to be symmetric BPSK [5] because it is well suited to transmission through non-linear channels. This choice of signalling is universally suited to preceed constant or non-constant envelope modulations and therefore fits the concept of the generic architecture.

To acquire symbol timing from the timing pattern the processing shown in Fig. 6 is used. The symbol sequence comprising the timing pattern is {1, j, 1, j, ...} and has spectral lines at $\pm f_r/2$ and 0 Hz. The received signal sampled at $f_s = 2f_r$ is first bandpass filtered to extract the spectral components at $\pm f_r/2$ Hz. This filter's passband must accomodate the maximum fading bandwidth. The output of this filter is interpolated to a sampling rate of $f_s = 4f_r$ and then squared. The squaring process generates spectral components at 0 and $\pm f_r$ Hz. The component at $+f_r$ Hz is down converted to complex baseband and narrowband filtered. Then if the down conversion oscillator is referenced to the assumed symbol clock the angle of the phasor at the narrowband filter output provides the symbol timing information. A timing signal presence indicator is obtained by notch filtering the discrete signal components at the input, squaring and lowpass filtering. This produces a signal proportional to the additive noise power at the receiver input. The power in the timing signal component can be obtained by lowpass filtering the timing signal prior to the down conversion. Timing signal presence is declared when the power in the timing signal exceeds a threshold relative to the input noise power.

The synchronization detection processing, shown in Fig. 7, is engaged after symbol timing has been declared. With symbol timing already established the transmitted symbols are filtered by a matched filter and differentially detected because the channel samples are not available yet. The resulting soft decisions are passed to the synchronization word correlator. The power at the output of the correlator is compared to the total signal power in the correlator delay line and when this ratio exceeds the detection threshold, synchronization is declared. At this point the reference sample demultiplexor, the decoder, the deinterleaver and the descrambler can be initialized.

III. IMPLEMENTATION

The modem for a 4.8 kbps digital voice terminal is being implemented on TMS320C25 digital signal processors (DSPs) using the reference symbol approach. Two versions of the terminal are currently planned. The first version is bandwidth efficient and intended for operation in 5 kHz channels. The second version will be power efficient and intended for operation in 20 kHz channels. Our approach to the software implementation on the DSPs is to follow a modular structure that will allow easy migration from the narrowband to the wideband version. The only modules that will need major modification are the coding/decoding modules. The acquisition and tracking modules are independent of the signal constellation, but, minor modifications will be required for optimization at different channel rates and signal-to-noise ratios.

The modem's block structure is matched in size and synchronized to the frame structure of the voice codec. This has several advantages. In the transmitter the preamble incurs no additional delay because it can be transmitted while the block interleaver is begin filled. In the receiver, techniques can be used to smooth or mask the undesireable effects of signal blockages or deep fades. The increase in bit errors during these periods often causes the codec to output objectionable audio and sometimes to lose frame synchronization. However, the channel state information can be used by the codec interface software to substitute repeated or known silence frames during poor channel periods. As well as reducing the potential for unwanted audio output, this approach allows faster recovery from blockages because the codec's frame synchronization is maintained throughout by the modem. Of course, this scheme requires knowledge of the codec's frame format.

The digital voice terminal is capable of operating in a voice activated fashion. Each burst of voice data is preceeded by one frame of preamble. When the receiver is not currently receiving a transmission it searches continuously for the preamble. To prevent the loss of an entire transmission if the preamble is missed, the reference pattern is used as a secondary means of synchronization since it has been designed to repeat every block. A search for the reference pattern is done in parallel with the preamble search and either process can synchronize the receiver.

The narrowband version is almost complete. The transmitter is implemented using a single C25 processor although it takes less than half of the available processing power. The transmitter's encoder is a 32 state, rate 1/2 Calderbank and Mazo (C&M) trellis code [6]. Each of the input bits in the I and Q paths at 2400 bps produce a 4 level code symbol at the encoder output. The reference symbol multiplex ratio is $M=4$ which results in a reference symbol rate of 600 reference symbols per seconds. At this rate the receiver can track fading channels with bandwidths up to 200 Hz. After multiplexing, a symbol rate of 3000 symbols per second is achieved. These complex symbols which are contained in a 16 QAM constellation are filtered with 50 % square root raised cosine pulse shaping filters before transmission. The transmitted spectrum is shown in Fig. 8.

The receiver is implemented using two C25 processors. The first processor is responsible for down conversion of the received signal to complex baseband and decimation to 2 samples per symbol, matched filtering, reference symbol demultiplexing, channel compensation and estimation, symbol timing tracking, frequency tracking, symbol timing acquisition and synchronization word detection. The second processor is responsible for deinterleaving, decoding, descrambling and the codec interfacing. The simulated performance of the receiver is shown in Fig. 9 for static and $k=-5$ dB, 60 Hz Rician channels. Three different trellis codes were simulated: the 32 state C&M trellis code, an 8 state C&M trellis code and a 64 state pragmatic trellis code [7]. These results show that, in the severely fading channel, an $E_b/N_o=7.3$ dB $(C/N_o=$ 44 dBHz) is required to achieve a bit error rate of 10^{-3} using the 32 state code. A bit error rate of 10^{-3} is the threshold where most voice codecs begin to suffer performance degradation from bit errors. While these are ideal results they do include the channel estimation and compensation processing which is equivalent to carrier recovery in conventional coherent systems. Therefore, any comparison to a other coherent techniques must include their assumed carrier recovery loss.

IV. CONCLUSIONS

A flexible modem architecture has been presented which provides robust performance in fading channels through the use of reference symbols. By using the reference symbols for the receiver's tracking functions, quick migration from one modulation and coding strategy to another is possible. This architecture could be the basis for a family of modems - each satisfying a specific power and bandwidth constraint yet all having a large number of common signal processing blocks.

V. REFERENCES

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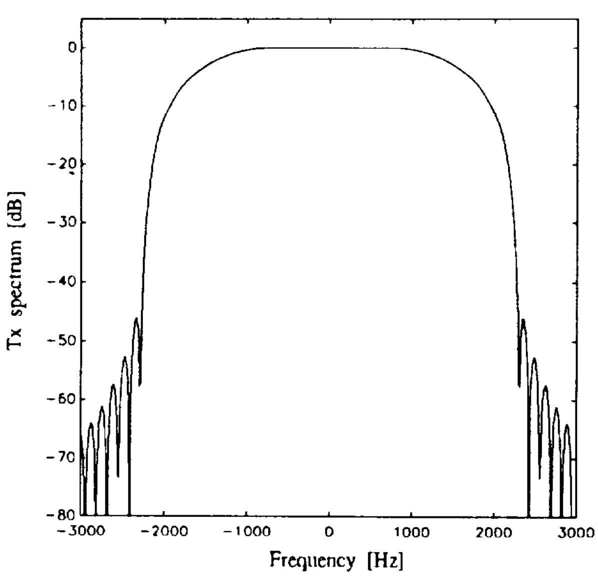

Fig. 8. The transmit spectrum of the narrowband modem.

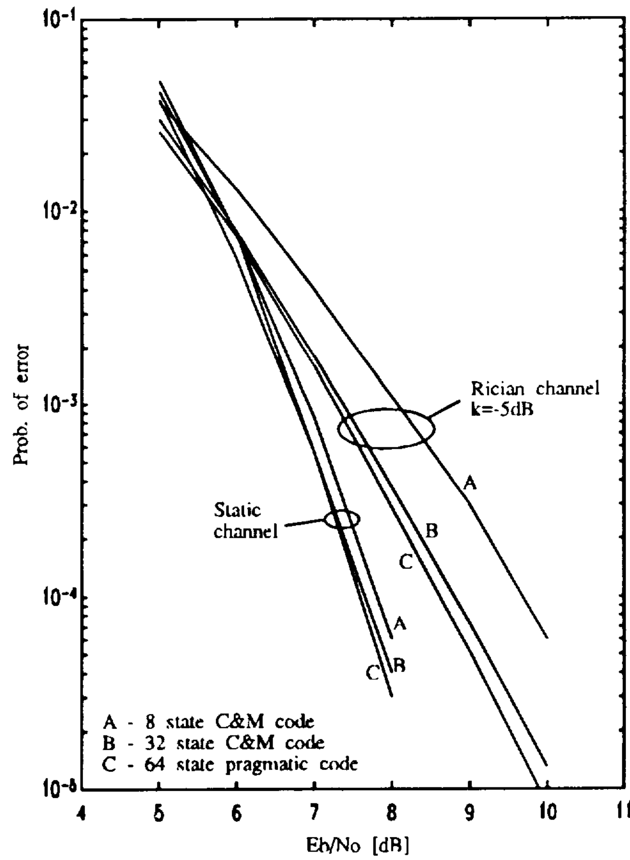

Fig. 9. The simulated BER performance of the reference symbol receiver.