Modem Design for a MOBILESAT Terminal

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ABSTRACT

This paper describes the implementation of a programmable digital signal processor based system, designed for use as a test bed in the development of a digital modem, codec and channel simulator. Code has been written to configure the system as a 5600bps or 6600bps QPSK modem. The test bed is currently being used in an experiment to evaluate the performance of digital speech over shadowed channels in the Australian mobile satellite (MOBILESAT) project.

1 INTRODUCTION

The availability of increasingly powerful digital signal processors (DSPs) has made possible the implementation of what were considered computationally complex tasks, at a reasonable cost and with relatively simple circuitry. Two examples of applications for DSPs are digital modems and codecs for digital speech. In the case of modems, traditionally analogue techniques have been used for the signal processing operations such as mixing, filtering, synchronisation etc. Digital signal processing allows better repeatability and a wider range of possible operations. In addition, DSPs provide a programmable development tool. This greatly facilitates the iterative process of algorithm implementation and development. (Alternatives include lengthy computer simulations and hardware modifications).

This paper describes the development of a programmable modem test bed based on DSP techniques. It has been designed for use in development of terminals for the Australian MOBILESAT system[1]. The intention is to provide a system which can be configured in various modes to provide a powerful DSP facility for the testing and development of modem and speech coding algorithms. This test bed allows generation of analogue signals at or near baseband, up-conversion to some intermediate frequency, and conversely in the receiver section, down conversion, sampling and discrete time processing. By provision of an IF interface, connection to existing RF transmitters and receivers for transmission over real channels is possible. An IF channel simulator can be used to recreate channel imperfections such as noise, multipath fading, shadowing, frequency offsets and interference. (Alternatively, some of these effects can be simulated at baseband by discrete time processes within the DSP. This provides a more controllable and programmable approach to testing, although less of a test for the entire system.) The main intended use for the modem test bed system is to provide a real time test facility for fairly low rate digital modem algorithms. It also allows a fast simulation tool for higher speed modems, and by the pipelining of extra DSPs and suitable break down of algorithms, testing of extra system components (eg digital speech codecs, forward error correction).

The immediate goal has been to provide a test modem for the MOBILESAT speech channel[2]. Current specifications allow for two channel data rates of 5600bps and 6600bps, each with a frame format corresponding to a frame length of 120ms. With the aim of using 5kHz or 7.5kHz bandwidth per speech channel, QPSK was initially chosen as the modulation scheme, with transmit root-Nyquist filtering and 40% excess bandwidth. Coherent detection was the chosen demodulation type (rather than differentially coherent), because of its superior performance with a direct path signal. Both frame formats allows for the insertion of a unique word at the start of each 120ms frame, and this is used to resolve the 4 state phase ambiguity.

The proposed MOBILESAT speech channel has an unfaded C/N_0 of 48 dB-Hz providing E_b/N_0 figures of 10.5 dB and 9.8 dB at 5600bps and 6600bps respectively. The high elevation angle for Australian geo-stationary satellites implies that the main problem associated with this channel at L-band will be shadowing caused by trees and buildings rather than multipath effects. This, together with channel measurements indicate that the propagation can be approximately modelled in terms of an 'on-off channel'. It is therefore desirable for the demodulator to have the ability to acquire signal synchronisation rapidly and 'free wheel' during periods of severe signal attenuation. A channel simulator has been developed that can be driven by amplitude and phase data to simulate shadowing effects at IF. This has successfully been used to replay recorded channel measurements during modem tests.

Section 2 gives a brief description of the hardware contained in the test bed at the time of the AUSSAT speech codec tests. Section 3 discusses the signal processing algorithms performed by the DSP. These include filtering, timing recovery, phase recovery and frame processing. Some results for the modem performance are given in section 4, and finally, in section 5, current work and future proposals for the modem test bed are outlined.

2 MODEM IMPLEMENTATION

The basic structure of the modem test bed is shown in figure 1. On the modulator (transmit) side of the system, the source supplies data via a serial bit stream, at 5600bps or 6600bps. Data is read by the modulator processor as pairs of bits (di-bits), which are formatted into frames and modulated to form a set of discrete baseband complex samples. The samples are converted to inphase and quadrature continuous analogue signal components using 14 bit D/As and analogue reconstruction filters. The signal is then mixed up to an IF of 71.15MHz using a quadrature mixer. The signal at IF can then be passed on to an RF transmitter, or passed through a channel simulator.

On the demodulator side, the converse functions take place. The received IF signal is mixed down to nominal baseband using a quadrature mixer, and then the inphase and quadrature components are low-pass filtered to eliminate aliasing effects, sampled, and the discrete quantised samples are passed on to the DSP. The DSP performs the receive filtering, all the synchronisation tasks (described in the next section) and reconstructs the data stream by unscrambling and differentially decoding, if necessary. The decoded data is sent to interface circuitry which converts it to a serial bit stream compatible with the AUSSAT specification.

Another important module in the system is the microcontroller. This provides a boot facility for the DSPs, control of DSP processes, and allows communication between the modem and a monitoring/controlling PC. This latter function allows downloading of programs to the DSPs, plus real-time monitoring and modification of DSP memory. With the aid of some graphical display software written for the PC, modem parameters can be observed in a convenient form, and recorded if required. For example, scatter diagrams, eye diagrams, frequency and timing tracking, etc can be shown in near real-time. This provides an excellent tool for the assessment of algorithm performance. Test programs have been written for the modem to measure bit error and frame error rates which can be monitored by a PC. Algorithm parameters can be modified during processing and subsequent improvements in performance (or otherwise) noted.

3 DIGITAL SIGNAL PROCESSING ALGORITHMS

The signal processing taking place in the modem test bed is illustrated in figure 2. Brief descriptions of the most important discrete time processes handled by the DSP are given below. The DSP32C was chosen as the most suitable DSP device because of its computational power (12.5MFlops), floating point processing capability, low cost, and the availability of a C compiler. These last two factors help considerably with software development, although careful optimisation of code is necessary to achieve the performance limits of the processor.

3.1 Filtering

Ideally, both the transmit and receive filters have identical root-Nyquist responses with an excess bandwidth of 40% for the purposes of limiting bandwidth, rejecting out of band noise and interference, and minimising inter-symbol interference. A finite impulse response filter is used to approximate the required filter response. This is achieved by a direct software

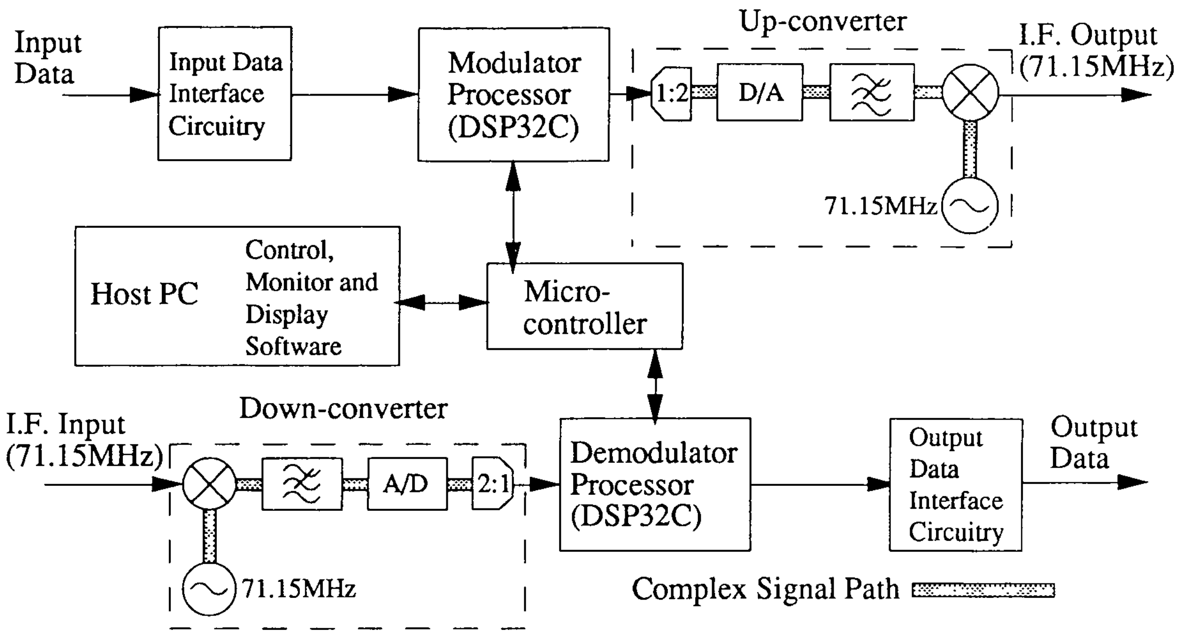

Figure 1: MOBILESAT Modem Test Bed

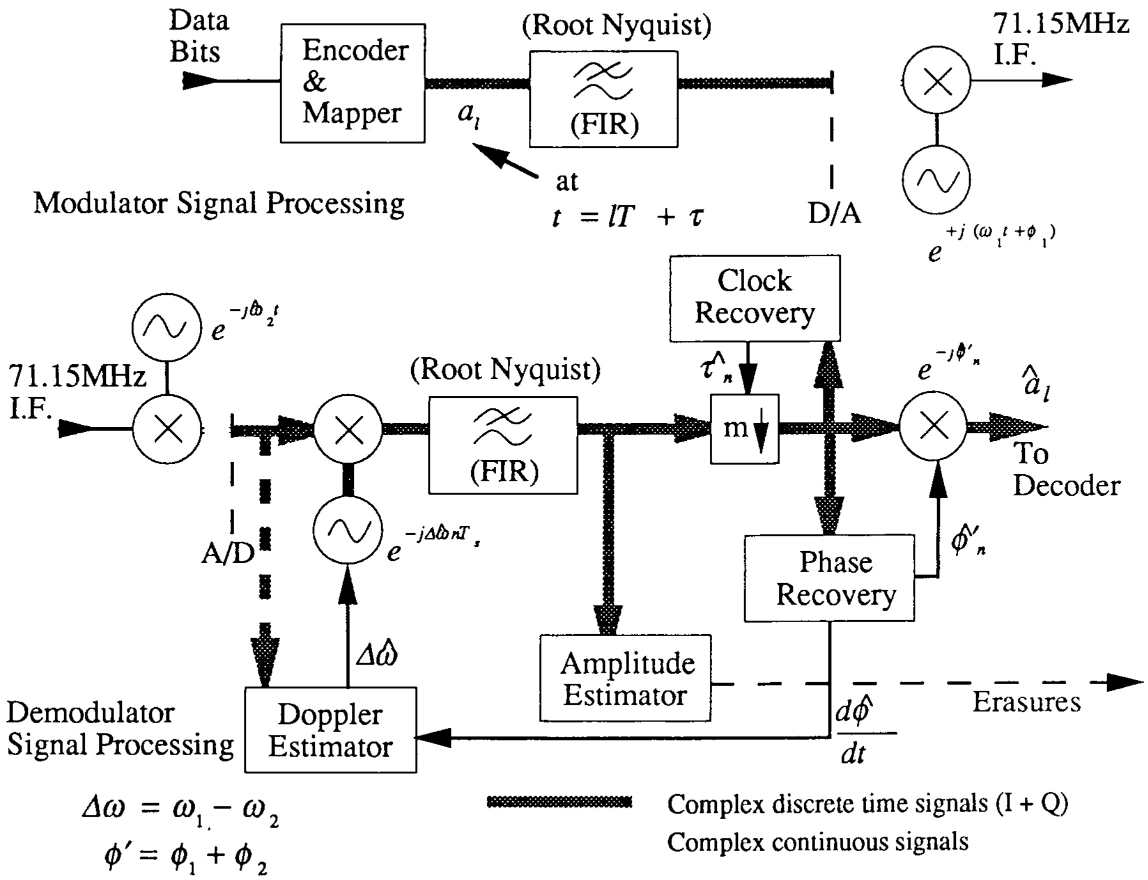

Figure 2: Modem Signal Processing

implementation of the filter equation

$$\overline{r_k} = \sum_{i=0}^{N-1} r_{k-i}\, h_i \qquad (1)$$

where h_i is a sample from the desired impulse response, r_k a received signal sample, and $\overline{r_k}$ the filtered signal. In the present design 4 complex-valued signal samples are taken per symbol period. After digital receive filtering, the symbol midpoint sample (y_n) can be interpolated and then used to update symbol timing and phase offset estimation. The number of taps was chosen to be 36 with a sampling rate of 4 per symbol.

3.2 Symbol Timing Recovery

The current symbol timing recovery algorithm is a one-sample-per-symbol decision-directed method that has been previously described by Cowley[3]. The technique represents a gradient solution to the maximum likelihood estimate of the timing offset between the sampling instant and the true symbol mid-point. The gradient solution leads to an iterative equation for estimating the timing offset, τ_n, associated with the nth received symbol:

$$\tau_n = \tau_{n-1} + \beta \operatorname{Re}\{ y'_n \bar{a}_{n-1} - y'_{n-1} \bar{a}_n \} \qquad (2)$$

where overbar indicates complex conjugation, a_i are the estimated symbol values, and β is a small positive adaption constant which controls the size of the symbol timing updates. The values y'_n are the complex signal samples after phase correction. To make the symbol timing independent of phase recovery, an estimate of the phase offset can be made from just the two samples y_n and y_{n-1}. A simple way of doing this is described in reference 4, in which the phase estimate is quantised by $\pi/4$. Although the technique is suboptimum, the degradation is small at the unfaded E_b/N_o ratio in use.

3.3 Phase Recovery

The phase recovery algorithm used in the current modem was described by Viterbi[4] and provides rapid and robust non-decision-directed feed forward phase recovery. If y_n is represented in polar form by r_n and θ_n then $z_n = r_n e^{j4\theta_n}$, an unbiased estimate of the phase offset, ϕ, associated with that symbol can be made by estimating the mean values of $\operatorname{Re}\{z_n\}$ and $\operatorname{Im}\{z_n\}$ over $2N+1$ symbols and calculating the corresponding phase angle. The nth estimate of ϕ is given by:

$$\phi_n = \frac{1}{4}\arctan\left(\frac{\sum_{i=-N}^{N} \operatorname{Im}\{ z_{n+i} \}}{\sum_{i=-N}^{N} \operatorname{Re}\{ z_{n+i} \}} \right) \qquad (3)$$

The mean phase offset is used to rotate the nth symbol sample y_n, thus achieving coherent demodulation.

Due to the phase quadrupling, a 4 phase ambiguity is left which can be resolved by observing the phase of the unique word (transmitted at the beginning of every frame).

3.4 Frequency Tracking

The frequency tracking is based on forming an estimate of the frequency offset of the signal mixed down to nominal baseband, and using this to frequency shift the signal closer to true baseband. The frequency offset estimate is updated periodically by calculating the mean phase estimate change per symbol. The maximum rate of change of frequency offset would be caused by the Doppler frequency shift due to mobile movement relative to the satellite. For an automobile this would usually be considerably less than 15Hz/s. Frequency offset updates rates of one per 120ms frame have proved to be more than adequate with the current phase recovery scheme.

3.5 Initial Frequency Estimation

The initial frequency estimation is based on a method involving the differerential power measurement from two passband filters located at either end of the required signal spectrum. Should the received signal have a spectrum that is offset in frequency, the power from the output of each of the filters is unbalanced and an error term can be derived to modify the frequency offset estimate. Simulation has indicated that a frequency offset of ±200Hz can be tracked within 50 symbols at an E_b/N_o of 0dB using this method.

3.6 Demodulator Frame Processing

The frame processing has two states of operation depending on whether frame synchronisation has occurred. If the modem does not have frame synchronisation, the initial frequency estimation is used, and on each received symbol a check is made to see if the unique word has been received. This continues until a UW is detected, at which time the modem switches to 'in frame sync' mode. The initial frequency estimation is deactivated, and the frequency tracking algorithm is used exclusively. The phase of the received UW is used to set the phase reference to demodulate future symbols. The proceeding data bits in the frame are then unscrambled and differentially decoded, if that option is set. After receiving an entire frame, the next UW is expected. If this is received successfully then the process continues as before. Otherwise, a counter is incremented to record the number of consecutive UW failures. If this counter reaches a given threshold, the demodulator reverts to its 'out of frame sync' mode. In fact there are two counters and thresholds which are used. One corresponds to a normal signal power level and the other to a shadowed power level. Should the average signal power drop below a predetermined level, then the signal is considered to be shadowed, and a larger number of UW failures are tolerated. The counters are reset as soon as a UW is detected again.

4 MODEM PERFORMANCE

Modem performance is measured in several ways including implementation loss compared to an ideal modem and acquisition time. The bit error rate performance of the 5600bps and 6600bps modems were found to be virtually identical. At E_b/N_o of 5dB and above the implementation loss is nearly 0.5dB, and the performance drops away considerably from the ideal case below 3dB.

Parameters of the modem synchronisation may be adjusted to give the best performance for the specific channel concerned. For example, if N is reduced in (3) the implementation loss increases but the recovery time after a signal outage is reduced. Symbol timing is not affected significantly by fades as the clock accuracy is sufficient to allow timing updates to be inhibited during fades so that symbol timing can 'free wheel'.

Some tests have been performed using a channel simulator allowing the replay of measured signal levels from a real mobile satellite channel. This demonstrated the modem's ability to retain synchronisation despite severe shadowing.

5 FUTURE ACTIVITIES

Several future developments are planned for the modem both in terms of hardware and software. It appears that part of the implementation loss evident in the modem tests could be due to some imperfections in the IF stages. To eliminate some of these, conversion to a low IF signal within the DSP is planned with a double stage conversion up to 71.15MHz. This will make the quadrature mixer redundant, thus getting rid of problems associated with errors in the quadrature arm phase shift and reducing carrier feed through. Similarly, IF sampling is planned for the receiver. Software configurable modem parameters such as sampling clock rates, filter cut-offs, and local oscillator frequency control are also under consideration.

The following modifications are also being made at the moment:

- Development of $\pi/4$ QPSK modem for the MOBILESAT speech channel
- More optimum synchronisation algorithms
- Conversion to low IF signal construction and sampling
- Alternative initial frequency estimation schemes.

The programmable nature of the DSP allows many modulation, coding and synchronisation algorithms to be developed and tested. It is hoped to produce a suite of algorithms that can be called upon to provide implementation of a range of modems and processing capabilities.

6 REFERENCES

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