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Stability Testing and Analysis of a PMAD DC Test Bed for the Space Station Freedom

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ABSTRACT

The Power Management and Distribution (PMAD) DC Test Bed at the NASA Lewis Research Center is introduced. Its usefulness to the Space Station Freedom Electrical Power System (EPS) development and design are discussed in context of verifying system stability. Stability criteria developed by Middlebrook and Cuk are discussed as they apply to constant power DC to DC converters exhibiting negative input impedance at low frequencies. The utility-type Secondary Subsystem is presented and each component is described. The instrumentation used to measure input and output impedance under load is defined. Test results obtained from input and output impedance measurements of test bed components are presented. It is shown that the PMAD DC Test Bed Secondary Subsystem meets the Middlebrook stability criterion for certain loading conditions.

INTRODUCTION

The Space Station *Freedom* (SSF) Electrical Power System (EPS) is a multi-kilowatt DC power system. The eventual goal is to provide 56kW (75kW peak) of power through six (6) 9.3kW (12.5kW peak) channels. Each channel is comprised of a source subsystem, a 160Vdc (nominal) primary distribution system, and a 120Vdc secondary distribution system. The source subsystem generates and regulates the 160Vdc primary power. The primary distribution power is converted to 120Vdc by DC to DC Converters (DDCUs). The secondary distribution system then distributes the 120Vdc power to the SSF users.

A Power Management and Distribution (PMAD) DC Test Bed has been developed at the NASA Lewis Research Center to provide early component and systems level data to support the development of flight hardware and EPS design. The PMAD DC Test Bed consists of breadboard hardware, configured as a single EPS channel, from power sources to user loads[1].

The Space Station *Freedom* Electrical Power System is unique in many ways. It will be the first space-based power system that will not have clearly defined loading conditions. Over the life of the power system hundreds

of loads will be attached to the power system, the majority of which are still undefined. This poses a system verification problem, the most severe being the possibility of a certain load mix causing system instability. Obviously, it is impossible to verify by test that the power system operates within specifications and is stable for all loading conditions. Therefore, it is imperative that constraints be placed in the design of the loads so that a combination of loads will not cause system instability.

Currently, a simple application of the Middlebrook stability criterion is being used as a guide by load converter designers. Although the Middlebrook criterion is normally applied to designing DC-to-DC converter input filters, the concept of instability caused by a negative impedance oscillation is also applicable at the systems level. The tests described below evaluate various input and output impedances of the PMAD DC Test Bed Secondary Subsystem to verify compliance with the Middlebrook stability criterion.

MIDDLEBROOK STABILITY CRITERION

At low frequencies, DC-to-DC converters exhibit a closed loop, negative incremental input impedance, $-R_i$, due to their constant power characteristics. That is, as the input voltage falls, the input current must rise to keep the input power constant. Since a DC-to-DC converter exhibits a negative impedance at low frequencies, the addition of an input filter could cause an instability. An ideal input filter has a low (positive) output impedance, Z_s , at low frequencies (Figure 1). However, the impedance rises to a resonant maximum value and the net circuit resistance (filter + converter) could become negative causing oscillations [3, p.91].

Stability criteria developed by R. D. Middlebrook and S. Cuk for the design of input filters for switching-mode DC-to-DC converters is discussed at great length in [2,3]. They describe an optimal method for designing input filters that are both stable and effect little change in the output impedance and regulation of the switch-mode converter. However, the criteria require knowledge of the internal components of the converter to meet an optimal filter design. Realizing that it is also common to design

filters for "black box" converters in which internal components are unknown, Middlebrook investigated another widely used criterion for stability based solely on the negative input impedance, $-R_i$, of a switch-mode converter.

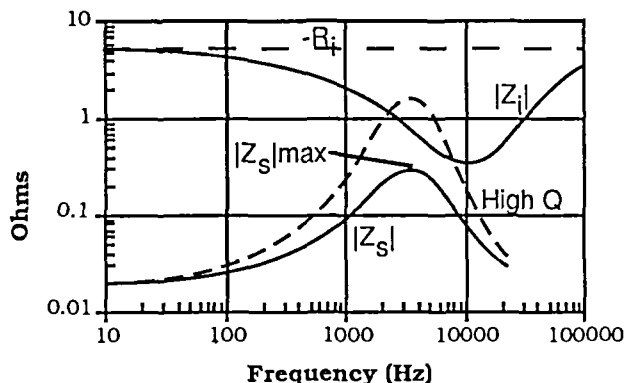


Figure 1 - Definition of Impedance Terms

As discussed in [3], a conventional rule for stability between an input filter and a DC to DC converter is:

$$|Z_s|_{\max} < -R_i. \quad (1)$$

where $|Z_s|_{\max}$ is the resonant peak output impedance of the filter (Figure 1). This rule implies that the input filter be designed with low Q to prevent the filter impedance from reaching a high resonant value. This could only be accomplished by increasing the ohmic resistance of the filter, thereby losing valuable efficiency points [3]. Middlebrook goes on to show that (1) will not guarantee stability and is not sufficiently general. Two cases are presented in which (1) is not satisfied yet the converter is stable, and another in which (1) is satisfied yet the converter is unstable (see High Q plot in Figure 1) [3].

A more general criterion to guarantee stability is

$$|Z_s| < |Z_i|. \quad (2)$$

where $|Z_i|$ is the magnitude of the closed-loop input impedance of the converter for all frequencies. Middlebrook stresses that this criterion is "more-than-necessary" to ensure stability, but does not guarantee that the converter performance will be unaffected by addition of the input filter.

The results of (2) guarantee stability between an input filter with a known output impedance, and a DC to DC converter with a known closed-loop input impedance. Currently, an application of (2) is being used as a guide for designers of load converters for the Space Station EPS. In a systems context, stability at an interface of a source and a constant power converter is similar to the input filter and DC to DC converter interface discussed previously. The source has an output impedance, Z_s , and the constant power converter has a closed loop input impedance (filter included) of Z_i . The current specification for load converters on the Space Station state that their input impedance must be 6dB above the output impedance of their secondary power interface for all frequencies. The specification is currently being

evaluated to ensure that it is not overly cautious and that it does not impose unrealistic constraints on the design of load converters.

SECONDARY SUBSYSTEM DESCRIPTION

The secondary subsystem of the PMAD DC Test Bed is shown in Figure 2. Its topology is similar to a single power channel of the Space Station EPS. The subsystem converts the widely-varying primary distribution voltage to a utility-type 120Vdc. The DC-to-DC Converter Units (DDCUs) receive primary distribution voltage (120Vdc-180Vdc) and step it down to 120Vdc. The DDCUs provide isolated, well regulated, utility-type power to the 23 load converters and facility loads in the test bed. Controlling the distribution of the power and providing fault protection are the Remote Power Controllers (RPCs). Finally, the secondary is populated with many different types of Load Converter Units (LCUs) all of which are DC-to-DC converters loaded by resistive loads. The hardware is described in detail below.

TRW DC to DC Converter Units (DDCUs)

The DDCUs were developed and built under an Advanced Development contract with TRW Space Systems of Redondo Beach, CA [4]. The TRW DDCUs are 6.25 kW converters utilizing a transformer isolated, series resonant topology. The DDCUs were originally designed as 12.5kW units comprised of two 6.25 kW power converters in parallel with a common controller. Recent changes to the Space Station program forced the TRW DDCU to be split into two separately controlled 6.25kW DDCUs with paralleling capability.

Two paralleling methods were employed in the re-designed DDCUs. The "droop" control method allows for paralleling and programmable power sharing between two DDCUs with no intra-controller connection. In droop mode, the DDCU's voltage regulator permits some voltage droop as the output power is increased. The amount of droop is controlled by setting the gain of the regulator to one of three settings. Power sharing is controlled by either changing the output voltage setpoint for each DDCU, or by setting different gains on the regulators. By changing these two values, each converter settles to a different output power level, thus controlling power sharing.

The second method employs a Master/Slave configuration. In this mode, the DDCU controllers are connected by an umbilical cable. The output voltage error bus is shared by both DDCUs. The controller developing the lowest error signal becomes the master and controls the shared error bus. The error bus signal, in each DDCU, is then analog multiplied by a fraction of 1.0. This signal is used in the current-mode control of the DDCU power stage and is proportional to the power output. By setting the multiplier through the DDCU data interface, power sharing between the two DDCUs can be controlled.

Remote Power Controllers (RPCs)

The Remote Power Controllers (RPCs) were developed and built by Westinghouse, Electrical Systems Division of Lima, OH. They are solid state switchgear which provide on/off control, overcurrent trip, current limiting, and power telemetry functions [7]. Three types of RPC's are used in the secondary; 65A, 12A, and 3.5 Amp RPCs.

Load Converter Units (LCUs)

Loading of the TRW DDCUs is accomplished through Load Converter Units (LCUs). These units are all DC to DC converters and represent the anticipated load converters necessary to convert the 120Vdc to useable voltage levels of 28, 15, and 5 Vdc. Loading is provided by programmable facility load banks. The various load converters used are described below.

TRW Load Converters

TRW Space Systems Division of Redondo Beach, CA developed three load converter topologies for use in the PMAD DC Test Bed. The three topologies: Series Resonant, Series Inductor, and Zero Voltage Switching (ZVS) all have the same specifications: output voltage (28Vdc), output power (1kW), good voltage regulation, short circuit current limiting, and input over/under voltage turn-off [6,7]. Eight (8) TRW LCUs are available for loads, six of which are ZVS units.

Westinghouse Load Converters

Westinghouse Electrical Systems Division of Lima, OH developed a 1kW, switching, full bridge DC to DC converter [6]. Specifications are the same as the TRW units: output voltage (28Vdc), output power (1kW), good voltage regulation, short circuit current limiting, and input over/under voltage turn-off. Three load converters

are available as 1kW constant power loads in the Secondary Subsystem.

Commercial Load Converters

Low power commercial DC to DC load converters were purchased from Vicor and Abbott [7]. These units range in power from 20W to 200W, range in output voltage from 5Vdc to 48Vdc, and are generally single switch, high frequency (+100kHz) converters. The Abbott and Vicor LCUs are connected to fixed resistive loads which provide full power loading.

SECONDARY IMPEDANCE TESTS

The PMAD DC Test Bed components were tested using an impedance measurement system described below. The DDCU's closed loop input impedance, Z_i , (input filter included) and output impedance, Z_o , were measured for a wide range of operating modes and conditions. Initial measurements of load converter input impedances are also taken to compare with the DDCU output impedance. Objectives of the impedance tests include the following:

- 1) Develop an impedance measurement system which could accurately measure the input or output impedance of any interface in the PMAD DC Test Bed.
- 2) Characterize the TRW DDCU input and output impedance verses power level and paralleling mode. Compare test results with current program stability requirements and Middlebrook stability criterion.
- 3) Provide actual test data to validate current computer models of the PMAD DC Test Bed so that further stability testing can be done using computer models.

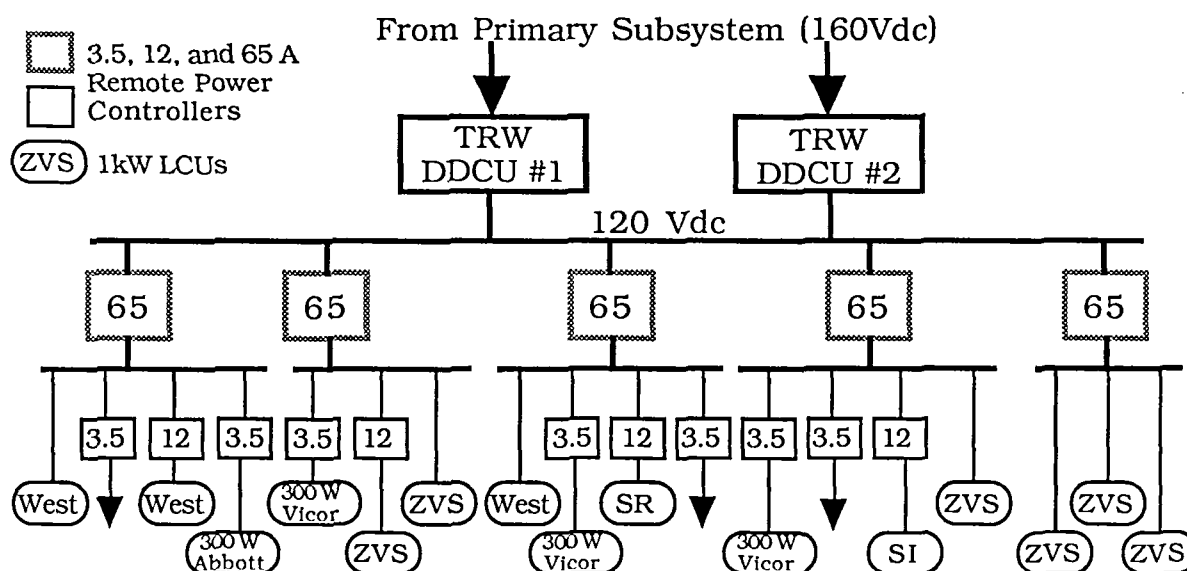


Figure 2 — PMAD DC Test Bed Secondary Distribution Block Diagram

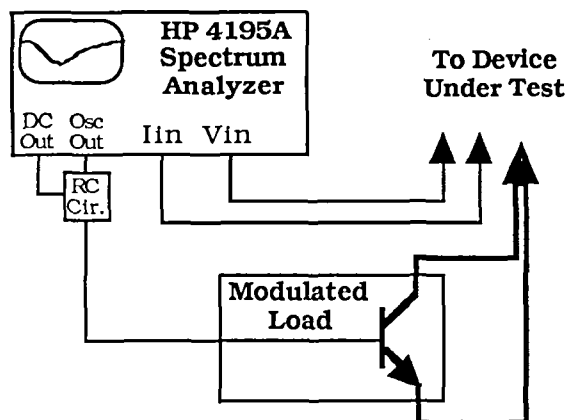


Figure 3 - Impedance Measurement System (IMS)

Impedance Measurement System (IMS)

The instrumentation used to measure the active impedance is shown in Figure 3. The system consists of: a digital spectrum analyzer with external drive signal, a programmable 6kW load, and standard DC current and voltage probes. The HP 4195 Spectrum Analyzer has both a DC bias and AC oscillator output. Using an external RC circuit, the two voltages are added producing a DC voltage with an AC ripple component. This signal is used to drive a programmable load which is programmed to vary its current draw with respect to the input signal. The result is a large current ripple (5 Ap-p) at the connection of the modulated load. As the Spectrum Analyzer sweeps up the frequency range, it measures the resultant current and voltage ripple components at the specific frequency and calculates $Z(s) = V(s)/I(s)$. The system is limited to impedance measurements from 10Hz to 20kHz since the programmable load can only produce low distortion sine waves up to 20kHz.

The placement and direction of the current probe determines whether input or output impedance is being measured (Figure 4). To measure output impedance, an output current ripple is created using the IMS and the resulting voltage ripple is measured. In this case, the

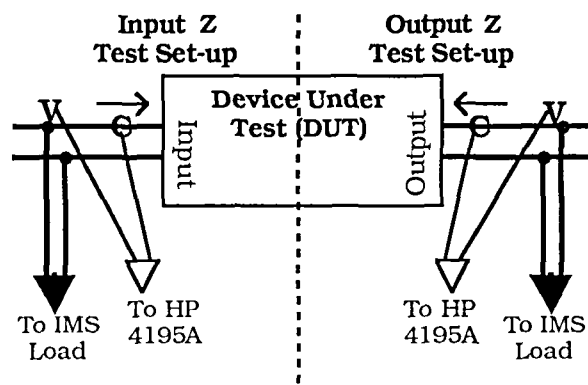


Figure 4 - Input / Output Impedance Measurement Configuration

current ripple measured is simply the current ripple created by the IMS. To measure input impedance, the IMS current ripple creates an input voltage ripple. The voltage ripple causes an input current ripple. In this case, the IMS current ripple is not measured, only the current ripple which results from the created voltage ripple.

TRW DDCU Impedance Test

Using the impedance measurement system, the input and output impedance of the TRW DDCU is measured from 100Hz to 20kHz. Results of the TRW input impedance tests are shown in Figures 5 and 6. For this test, three power levels were tested (1, 3, and 6 kW) on a single DDCU operating in droop mode regulation and an input voltage of 165Vdc. The test results shown are identical for paralleled DDCUs operating at various power levels and paralleling modes (droop and master/slave). The plot in Figure 5 shows a minimum impedance value of 0.45Ω at about 1.3 kHz. However, when the DDCU input voltage was changed from 165Vdc to 133Vdc, the impedance magnitude minimum dropped to 0.13Ω (11dB down) at about 1 kHz. Obviously, the DDCU input impedance magnitude is sensitive to variations in the input voltage. This is most likely due to the fact that incremental input impedance varies with input voltage.

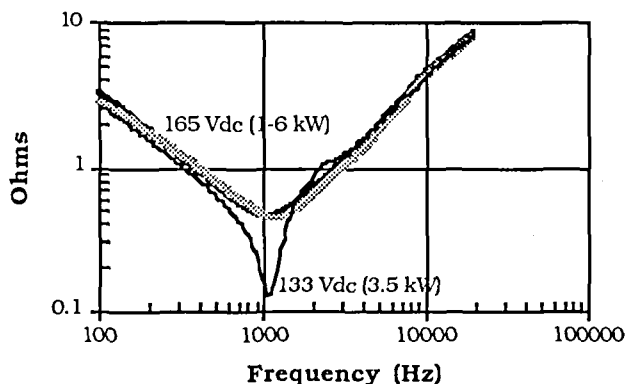


Figure 5 - TRW DDCU Input Impedance (Magnitude)

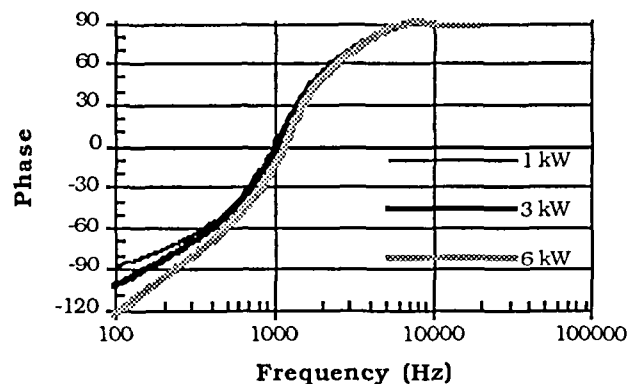


Figure 6 - TRW DDCU Input Impedance (Phase)

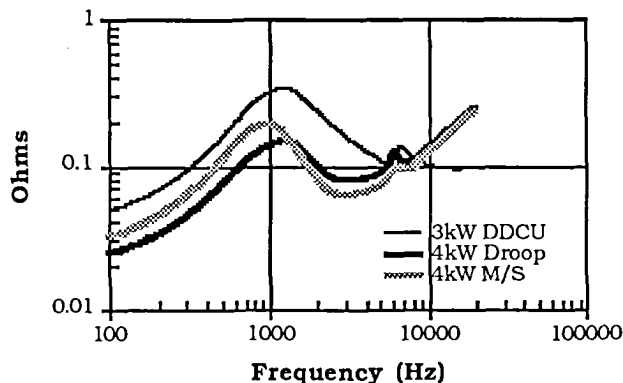


Figure 7 – DDCU Output Impedance Magnitude

Also, a lower input voltage will increase switch conduction time, thereby decreasing effective ohmic resistance and increasing effective circuit inductance. This results in a higher Q filter and a lower resonant input impedance.

The input impedance of an active converter has a negative real value when the phase is $-90^\circ > \theta > 90^\circ$.

$$\text{Re}[Z(s)] = |Z(s)| \cdot \cos(\theta)$$

The phase plot in Figure 6 displays the concept of the DC to DC converter having negative impedance. The single DDCU operating at 6kW has negative impedance characteristics from DC to 250 Hz. Middlebrook states that the negative impedance characteristic vanishes well below the loop gain crossover frequency (frequency at which the control loop gain is less than unity)[3]. Tests have shown the TRW DDCU loop gain crossover to be about 1kHz. Figure 6 also shows that the negative impedance characteristic of the DDCU varies with power level, the higher power levels having the highest negative impedance frequency band.

The output impedance of the TRW DDCU was measured for various power levels, parallel modes, and input voltages. Typical output impedance results are shown in

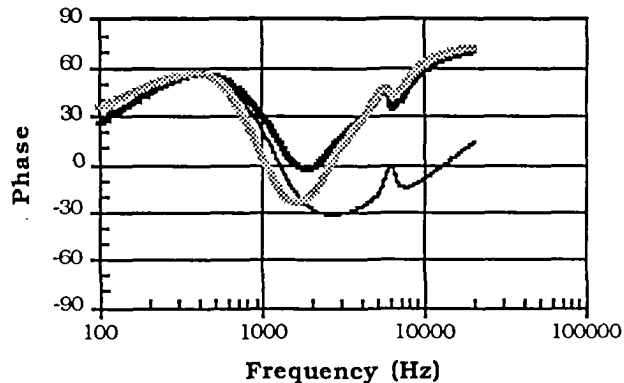


Figure 8 – DDCU Output Impedance Phase

Figures 7 and 8. The output impedance for a single DDCU operating at 3kW (in droop mode and input voltage of 165Vdc) has a peak impedance of 0.4Ω at 1.3kHz. The paralleled combination of two DDCUs lowers the output impedance peak to only 0.2Ω (3dB down) at 1kHz for the 4kW Master/Slave mode, and 0.14Ω (9 dB down) at 1.3kHz for the 4kW droop mode. Clearly, the output impedance of the two paralleled DDCUs is more favorable to system stability (lower Z_o) than the single DDCU. Also, variations in input voltage had no effect on the output impedance. The output impedance phase shown in Figure 8 shows a predominant inductive output for most frequencies.

DDCU-Load Converter Interface

Figures 9 and 10 show the results of impedance measurements taken at the DDCU interface with the load converters in the secondary subsystem. At this single interface, both a paralleled DDCU output impedance measurement and a load converter input impedance measurement was taken for a 4kW load. The DDCUs were in a Master/Slave mode with an input voltage of 165Vdc. The loads used were two TRW ZVS and one series resonant load converter (3kW) plus about 700 W from the IMS modulated load. Results show that at this

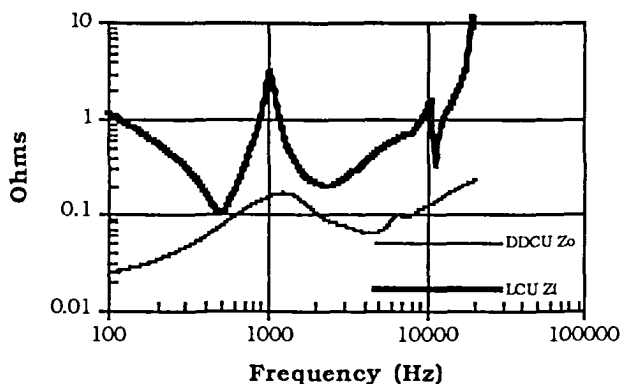


Figure 9 – DDCU / Load Converter Impedance Magnitude

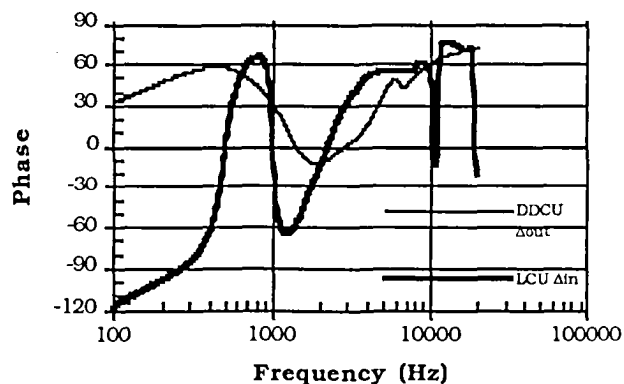


Figure 10 – DDCU / Load Converter Impedance Phase

interface, under the specific conditions outlined above, the sufficient condition for stability of (2) is met for all frequencies from 100Hz to 20kHz.

Computer Modelling

Test results of input and output impedance measurements were used to refine computer models being developed at the NASA Lewis Research Center [8]. The models being developed in EMTP are a combination of functional models of test bed components (DDCUs, LCUs) and circuit level models of cables and filters. Comparison of the computer generated impedance plots and actual test results is very good.

CONCLUSIONS

A utility-type secondary power distribution subsystem was introduced and its importance to the Space Station program was discussed. The problem of ensuring system stability for an undefined load mix was presented. Stability criteria developed by R.D. Middlebrook and S. Cuk for the design of input filters for DC to DC converters are applied to a general system interface to ensure stability.

An impedance measurement system was described which is used to measure the active input and output impedance of any DC power component. Impedance tests of paralleled TRW DC to DC converter units (DDCUs) showed that input impedance varies only with input voltage. Conversely, DDCU output impedance varies with parallel mode but not with input voltage. Comparison of the output impedance of paralleled DDCUs and the input impedance of several load converters showed that the Middlebrook stability criterion presented was met.

FUTURE TESTING

Component and systems level impedance testing will continue as new components are added and system configurations change. Using the computer models developed in EMTP, the limits of the Middlebrook stability criterion (2) will be investigated. The hope is to be able to relax the very restrictive criterion (based on (2)) currently being used in the Space Station specifications. By showing that this criterion can be relaxed, designers of load converters should be able to reduce filter weight and improve efficiency.

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