On the Performance of Trellis Coded Modulation with Octal Phase Shift Keying Over the TDRSS Channel

by

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Telemetering and Telecommunications Research

Executive Summary

As the National Aeronautics and Space Administration moves into the 21st century with programs like Space Station Freedom, a manned mission to Mars and the new Landsat mission, transmission demands on the Tracking and Data Relay Satellite System (TDRSS) will very likely exceed the available bandwidth. Under NASA grant NAG 5-1491 the Manual Lujan, Jr Center for Space Telemetering and Telecommunications Systems at New Mexico State University is studying techniques for increasing the data rate capabilities of TDRSS. These techniques include the use of advanced bandwidth efficient modulation formats to increase the data rate that can be sustained in a TDRSS transponder and the use of lossless bandwidth compression of the data to be transmitted to lower the data rate required from the user spacecraft.

Based upon current technology the most promising bandwidth efficient modulation technique is Trellis Coded Modulation (TCM) operating with Octal Phase Shift Keying (8PSK). TCM coding with 8PSK carrier modulation has the capability to increase the data rate which can be transmitted through the TDRSS spacecraft by a factor of 2 to 2.5 times that available with todays coded QPSK systems with only a small penalty in link performance relative to the existing systems. This increase in the maximum data rate applies to both the KSA and SSA services and can be used to carry more data from one user or to reduce contact times to allow more users.

However, before NASA can safely employ TCM coding it is necessary to prove that this complex format can perform on the real TDRSS link as it does in labs and simulation studies. This proof-of-concept test over a live satellite channel was the objective of the construction and testing performed under this task of the NMSU NASA grant referenced above. In conjunction with NASA, New Mexico State University's Center for Space Telemetering and Telecommunications Systems has constructed a system to test a new candidate TDRSS modulation scheme, TCM 8PSK, that can enhance the information throughput of the TDRSS spacecraft.

The test system for this project which was constructed over a period of 18 months by New Mexico State University consisted of two racks of commercial and university-designed and -built equipment. This system is illustrated in Figure ES-1. This project has included modifications of an

existing White Sands Ground Terminal (WSGT) High Rate QPSK Demodulator to demodulate 8PSK as well as the construction of other support hardware. Also, two TCM codecs (coder/decoders) have been constructed to implement two levels of bandwidth efficiency. One was designed and built by the research team at NMSU while the other was created by the University of Notre Dame with the University of South Australia. The NMSU codec achieves a 2-to-1 increase in data rate per unit bandwidth with a coding gain relative to QPSK of about 3dB. The Notre Dame/South Australia codec achieves a 2.5-to-1 increase in data rate per unit of occupied bandwidth and a coding gain of about 2dB.

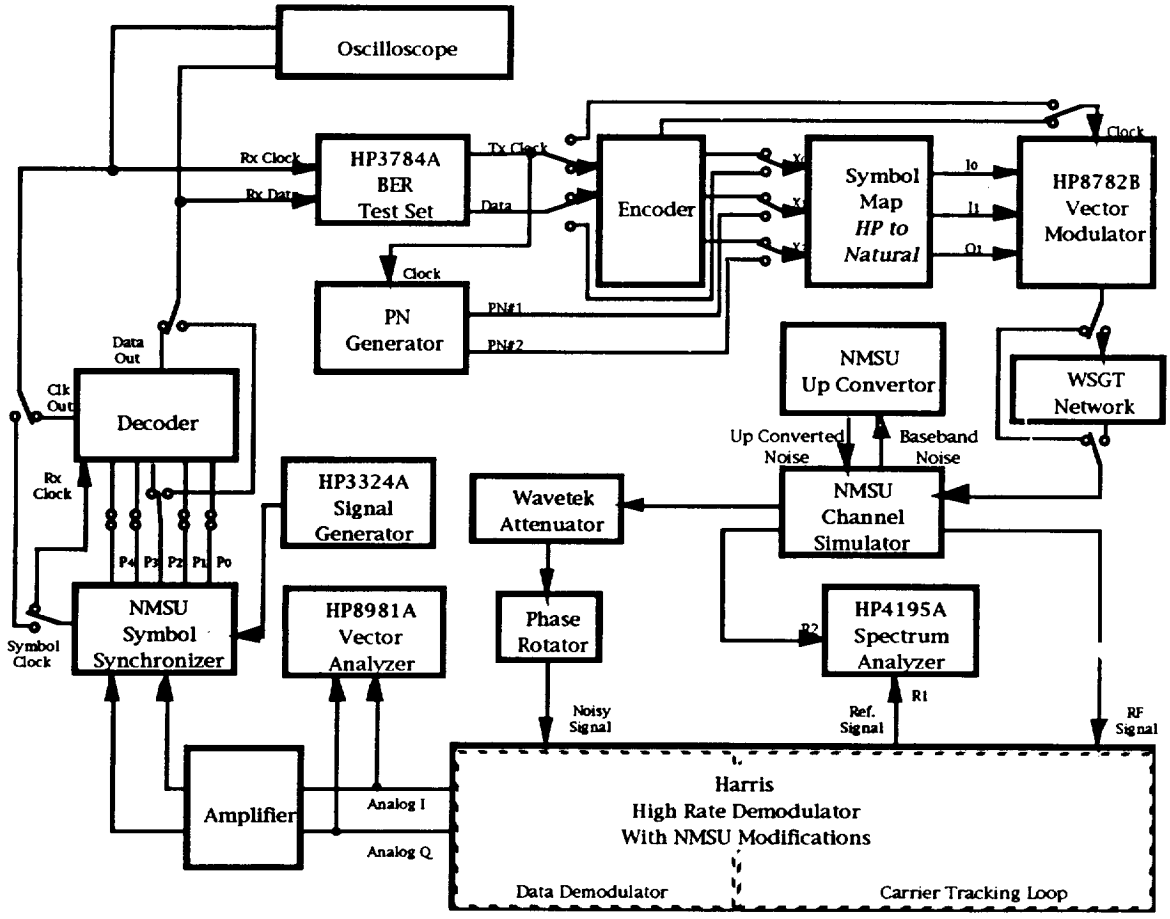

Figure ES-1 / System Diagram

The tests through TDRSS were very successful — demonstrating that 8PSK Trellis Coded modulation can achieve the same coding gains in the live satellite channel as those achieved in the laboratory and in the simulations. The entire test program consisted of tests in the university laboratory, testing in a loopback configuration at WSGT, testing through the Inter Facility Loopback simulator at WSGT and finally through the TDRSS spacecraft itself using both KSA and SSA modes. The results of all phases of this testing are presented in this report. The most telling results are reproduced as Figures ES-2 and ES-3. Figure ES-2 shows the results of testing the NMSU pragamatic coding system in the laboratory and through TDRSS. As can be seen in the figure the results are almost identical proving that the TDRSS channel can support this code. The measured coding gain with this codec was very near the 3dB predicted by theory and by simulations. Figure ES-3 presents the same data for the codec designed at Notre Dame and build by the University of South Australia. Again the results are the same — the codec performed the same in the lab and on the live satellite channel. This codec also displayed coding gain near it's theoretical 2dB while providing a factor of 2.5 in bandwidth compaction as compared to a factor of 2 obtained by the NMSU codec. This successful test program and the results shown in these figures clearly demonstrate the usefulness of TCM/8PSK in the TDRSS environment.

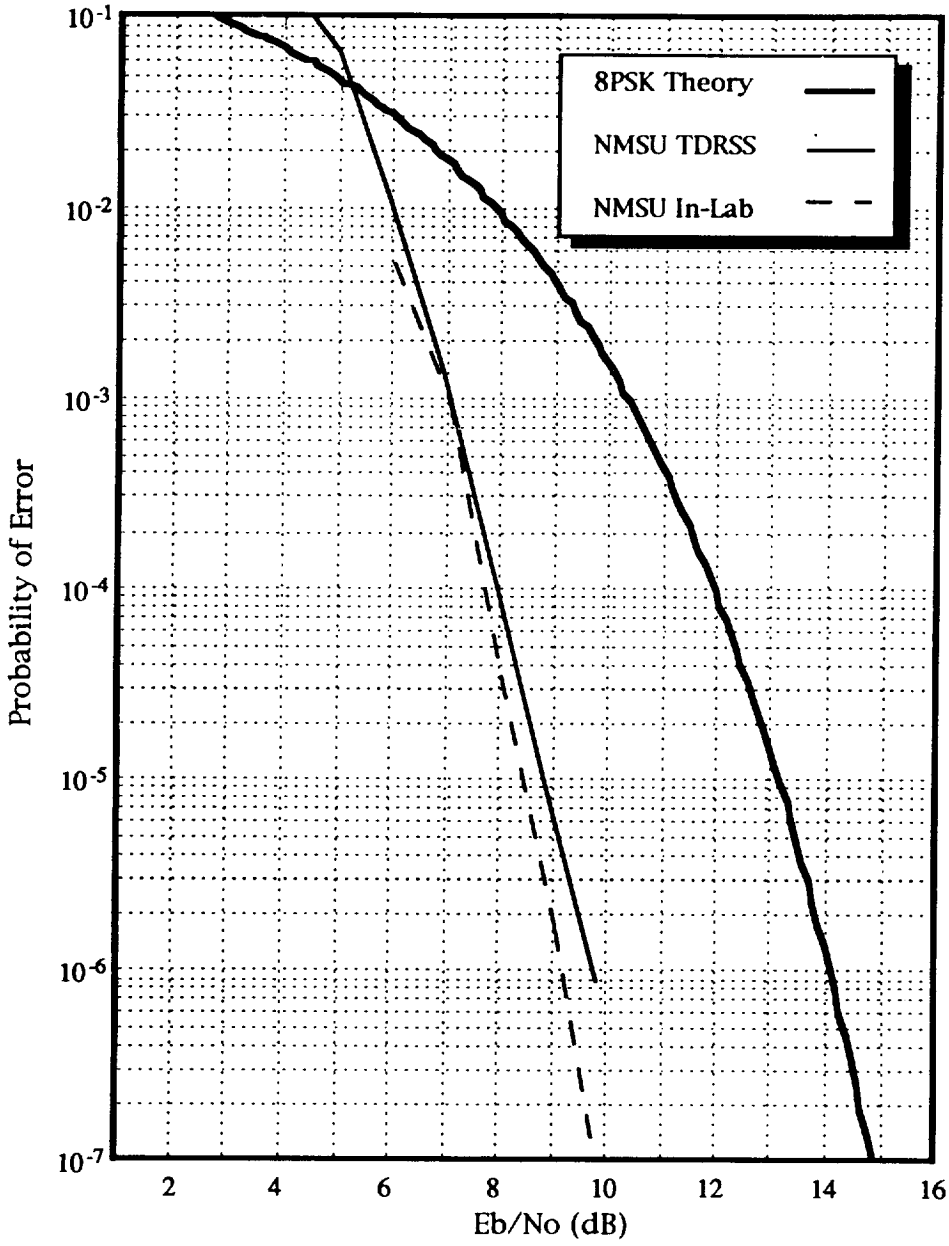

Figure ES-2 / NMSU Codec Performance

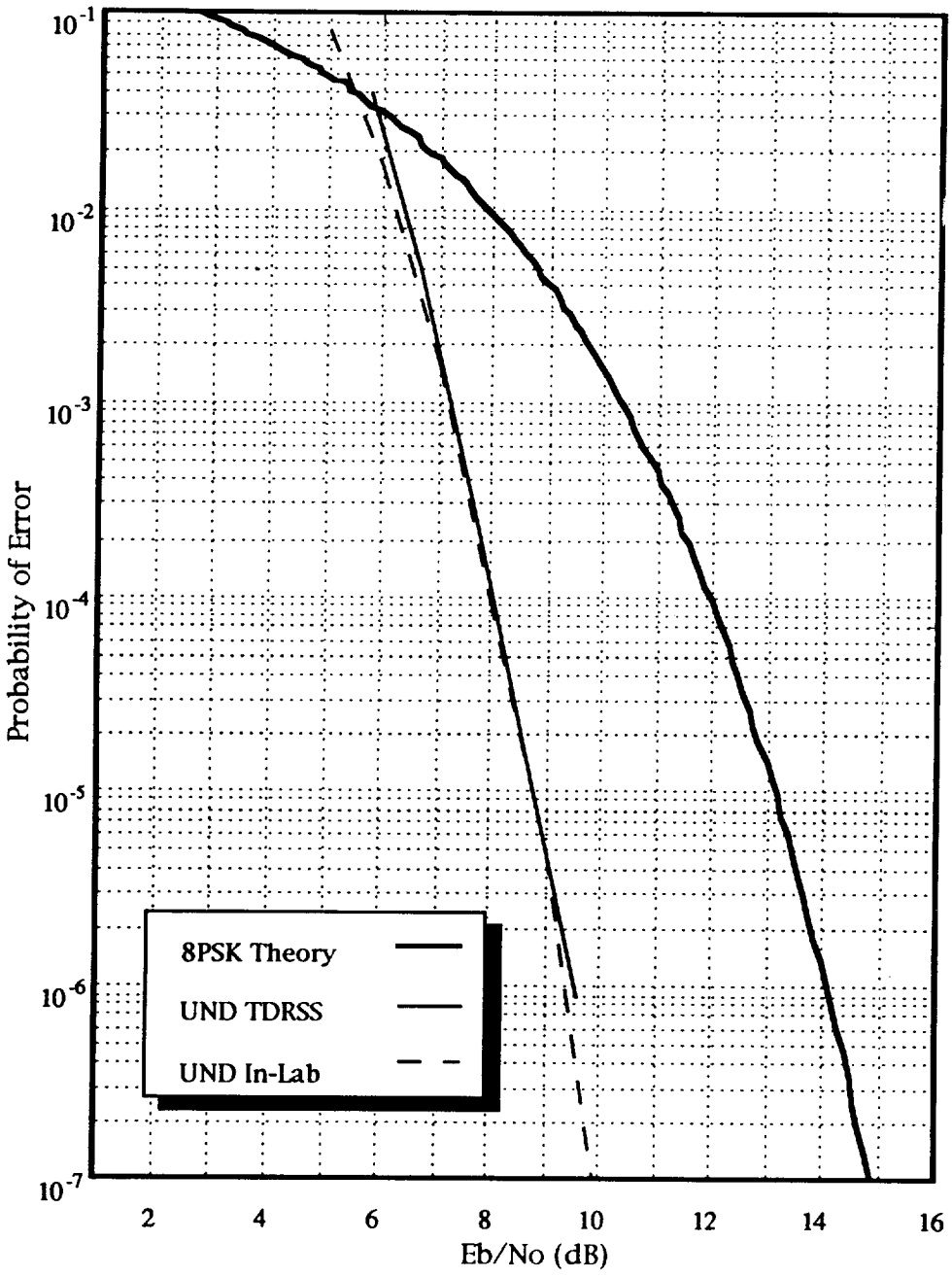

Figure ES-3 / UND/USA Codec Performance

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1. Introduction

As the National Aeronautics and Space Administration moves into the 21st century with programs like Space Station Freedom, a manned mission to Mars and the new Landsat mission, transmission demands on the Tracking and Data Relay Satellite System (TDRSS) will very likely exceed the available bandwidth. Under NASA grant NAG 5-1491, the Manual Lujan, Jr. Center for Space Telemetering and Telecommunications Systems at New Mexico State University is studying techniques for increasing the data rate capabilities of TDRSS. These techniques include the use of advanced bandwidth efficient modulation formats to increase the data rate that can be sustained in a TDRSS transponder and the use of lossless bandwidth compression of the data to be transmitted to lower the data rate required from the user spacecraft.

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However, before NASA can safely employ TCM coding, it is necessary to prove that this complex format can perform on the real TDRSS link as it does in labs and simulation studies. This proof-of-concept test over a live satellite channel was the objective of the construction and testing performed by NMSU under the NASA grant referenced above. In conjunction with NASA, NMSU's Center for Space Telemetering and Telecommunications Systems has constructed a system to test this new candidate modulation scheme, 8PSK TCM, that can enhance the information throughput of the TDRSS spacecraft. This project has included modifications of existing White Sands Ground Terminal (WSGT) equipment to demodulate 8PSK as well as the construction of other support hardware. Also, two TCM codecs (coder/decoders) have been constructed to implement two levels of bandwidth efficiency. One was designed and built by the research team at NMSU while the other was created by the University of Notre Dame with the University of South Australia. The NMSU codec achieves a 2-to-1 increase in

data rate per unit bandwidth with a coding gain relative to QPSK of about 3dB. The UND/USA codec achieves a 2.5-to-1 increase in data rate per unit of occupied bandwidth and a coding gain of about 2dB. This paper will discuss the design of the units used in this testing of TCM via TDRSS, the testing itself and the results of these successful tests.

The test system constructed for this project by NMSU consisted of two racks of commercial and university-designed and -built equipment. Section 2 provides an overview of this system and its operation during the testing phase. The individual units of equipment used to construct the overall test system are described in Section 3. Standard commercial equipment is treated lightly where as the description of the university-built equipment is given in sufficient detail to allow the reader to determine the techniques used in the construction of the custom test equipment. There were a number of theoretical problems — such as how to measure the carrier-to-noise ratio (C/kT) to plus or minus .1dB in a consistent manner, encountered in the testing and in the analysis of the results. These problems and their solutions are discussed in Section 4. Section 5 contains the test results and analysis. The results show that TCM can perform as well in the actual TDRSS environment as it does in the lab and that the theoretical coding gain of each of these codecs was achieved over the satellite channel. Section 6 provides a summary of the project and discusses ideas for future analysis and testing.

2. Test System Configuration & Operation

A block diagram of the test system constructed by NMSU along with its interaction with the WSGT network is shown in Figure 2.0-1. The test system was designed to be connected directly to the network. This required only two connections between the test system and the WSGT network. A 370MHz 8PSK data signal was supplied by the test system to the transmission side of the network. That data signal was then converted to S or K band and routed through either the Inter Facility Loopback (IFL) network, for channel simulation purposes, or the actual TDRSS channel. After the signal was processed by the WSGT network — either the IFL network or the satellite — it was returned to the test system at 370MHz. This section will describe the general test system operation and interaction with the WSGT equipment.

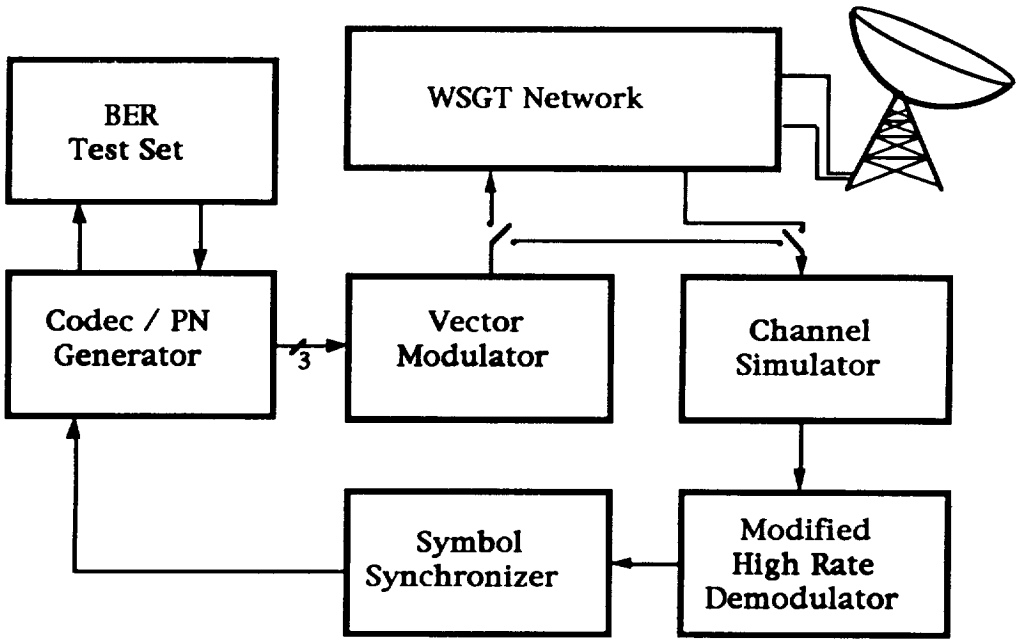


Figure 2.0-1 / NMSU Test System

As shown in Figure 2.0-1, the system starts and ends with the Bit Error Rate (BER) test set. The pseudo-random bit sequence to be transmitted is created here, as described in Section 3.5.1. This data sequence is supplied to the codec in operation (see Section 3.4) and the PN Generator (see Section

3.6.2). Here, the data is converted into three parallel bits for coded or uncoded 8PSK modulation. The Vector Modulator, described in Section 3.5.2, then takes this data and modulates it on a 370MHz carrier for transmission over the channel. This signal is either supplied to the WSGT network or routed directly to the system's receive side for loopback testing. The WSGT network performs the proper data manipulations and then feeds the signal through the IFL or to the antenna. It then returns the signal to 370MHz and supplies it to the receive side of the test system.

The receive side of the test system starts with a channel simulator, which is used to manipulate the received signal. This manipulation includes the addition of noise to the data signal, rotation of the data's phase for elimination of any phase ambiguity, and signal conditioning for interface with the demodulator. The signal is then demodulated by the modified High Rate Demodulator (HRD). The modifications to the HRD as well as the interface between it and the Channel Simulator are described in detail in Sections 3.3 and 3.4.

The clock is recovered from the demodulated signal by the Symbol Synchronizer, described in Section 3.2, which also converts the received analog data signal into 5 bits of digital phase information – the format required by the decoder side of the codecs. This data is then decoded and returned to the BER test set for measurement.

There were four distinct test phases — in-lab testing, to establish the baseline performance of each system; on-site testing, to assure that the equipment was undamaged on the move from NMSU to WSGT; IFL testing, to measure the performance through WSGT's simulator; and finally the TDRSS testing. During each phase, three tests were performed — a test to measure the performance of each of the two codecs and an uncoded test to facilitate the measurement of coding gain (see Section 4.2). Each test consisted of measuring the BER of the system over a range of signal-to-noise ratios (Es/No), set by the channel simulator system. This data was then plotted versus the energy per data bit, producing a uniform graphical format. Once the data was plotted on common scales, the results of each stage of the test could be evaluated and compared to those of other stages. The theoretical

basis of the testing, including noise calibration and test comparison, is explained fully in Section 4, while the results can be found in Section 5.

3. Test Equipment

The system as described in Section 2 includes a great deal of equipment, much of it used to support the main components in the test system. The block diagram shown in Figure 2.0-1 has been expanded in Figure 3.0-1 to include all the units in the system. The system, as shown, contains a number of commercial devices, as well as those designed and constructed by the universities involved. This section will describe each element in the system, discussing the commercial equipment briefly while fully explaining the units built specifically for this test.

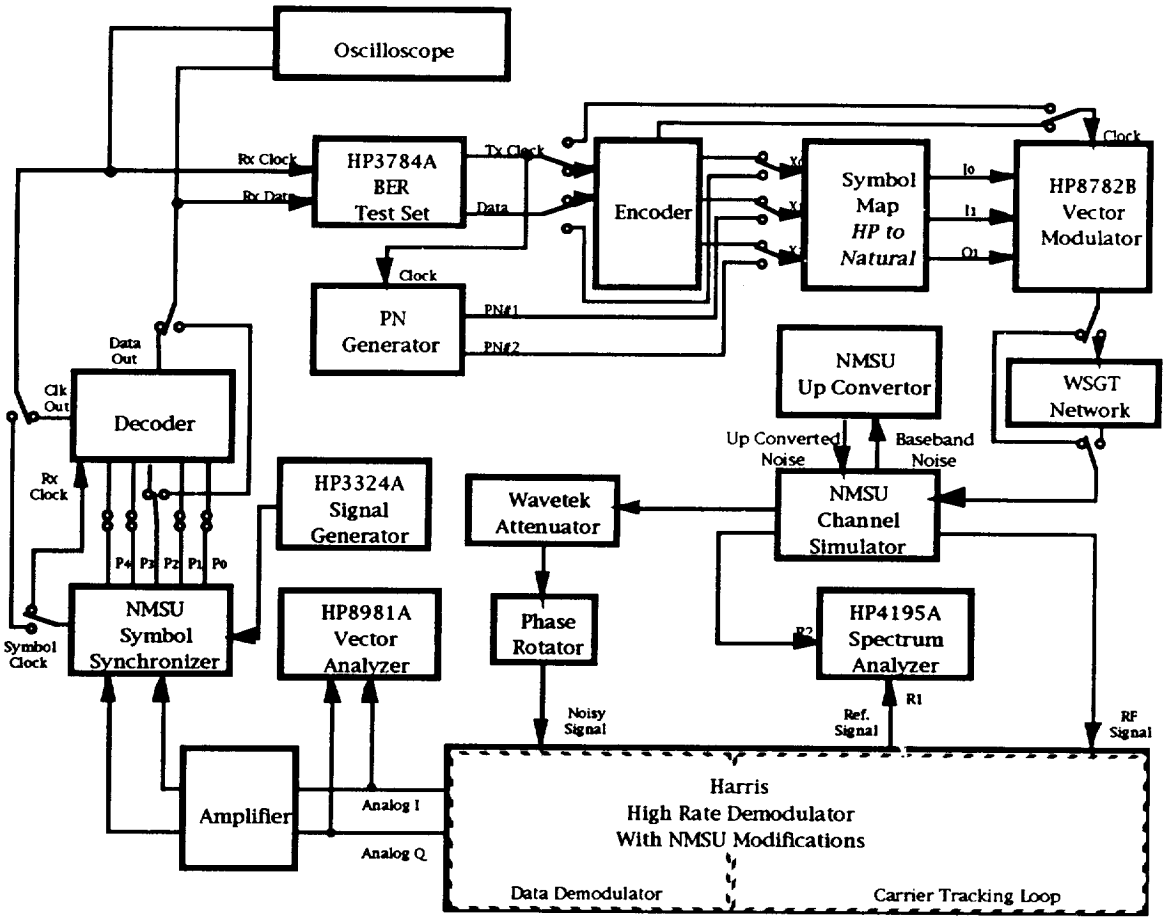


Figure 3.0-1 / System Diagram

3.1 Encoder/ Decoders

The trellis coding of the 8PSK signal was performed by two codecs (coder/decoders), each of which was designed to implement a different level of bandwidth efficiency. One, designed and built by the NMSU research team, increases the data rate per unit bandwidth by a factor of 2 as well as providing a coding gain — relative to QPSK — of about 3dB. The other employs a code that produces a 2dB coding gain, compared to QPSK, while increasing the data rate per unit of bandwidth by a factor of 2.5. This codec was designed and built by UND/USA. This section will discuss each of the codecs.

3.1.1 NMSU Pragmatic Codec

The NMSU Pragmatic Codec uses the pragmatic TCM standard invented by Viterbi [6] to implement TCM using a currently available binary Viterbi decoder. In the case of rate 2/3 8PSK, Viterbi has used the analytical technique of Zehavi and Wolf [8] to show that only 0.6 dB of coding gain is sacrificed by using pragmatic TCM, rather than the 64-state Ungerboeck code [4,5]. The decoder, shown in Figure 3.1-1, receives 5-bit phase information from the symbol synchronizer.

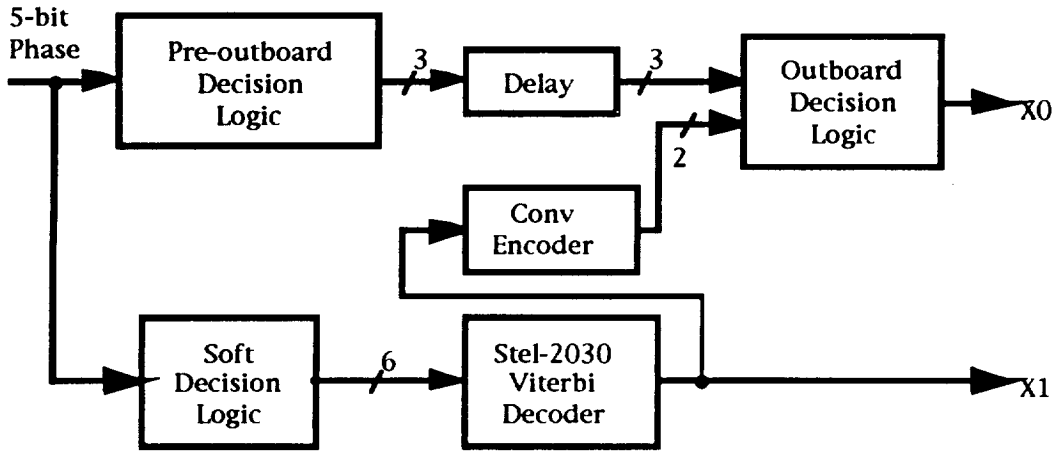


Figure 3.1-1 / NMSU Pragmatic Decoder

The soft decision logic converts phase information to a pair of soft decision inputs for the Stel-2030 Viterbi decoder. The soft decision is a 3-bit number that indicates, on a scale of 0 to 7, the relative likelihood that the code bit was a 0 or a 1. In QPSK operation, for which the Viterbi decoder was designed, the soft decision inputs are obtained from Digital-to-Analog conversion of the received I and Q components. To make the binary Viterbi decoder work for TCM, soft decision logic is used to convert the phase of the received vector into soft decisions that are meaningful to the decoder.

In generating pragmatic 8PSK, two data bits are modulated onto each symbol by the encoder, as shown in Figure 3.1-2. One of the two data bits is fed into a convolutional encoder, generating two codebits. The two codebits and the remaining data bit are mapped onto the 8PSK signal constellation. The data bit that is mapped directly onto the signal constellation is referred to as the outboard bit. When the TCM sequence is decoded, the Viterbi decoder returns the convolutionally encoded bit. The outboard bit is returned by the outboard decision logic, which requires phase information, as well as the re-encoded sequence. The phase information must be delayed to match the data delay introduced by the Viterbi decoder. The pre-outboard decision logic reduces the phase information that must pass through the delay from five bits to three. The decoded bits, X0 and X1, are clocked out of the decoder at the same rate that 5-bit phase codes are clocked into the decoder. The decoded bits are clocked to the BER test set, where error rates for the convolutionally encoded bit and the outboard bit are measured independently.

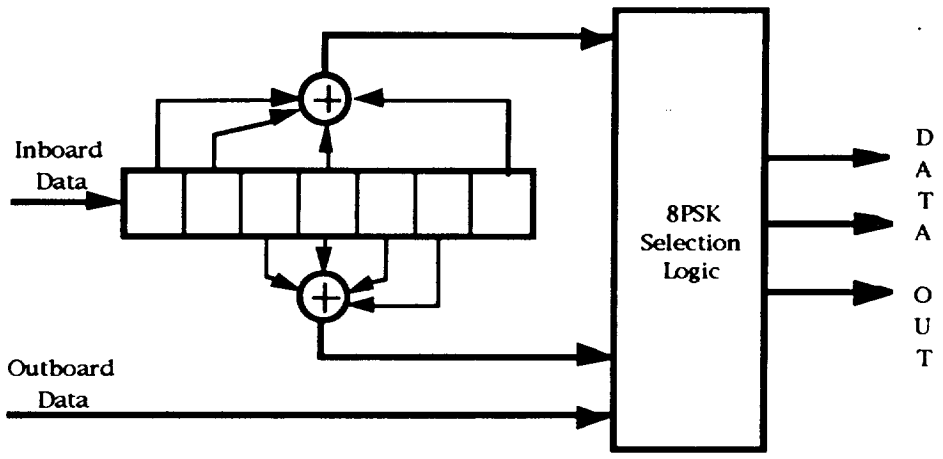


Figure 3.1-2 / NMSU Pragmatic Encoder

3.1.2 UND/USA Rate 5/6 8PSK Codec

The UND/USA codec uses a 4-dimensional signal set, each symbol consisting of a pair of 2-dimensional 8PSK signals. Five data bits are encoded onto the 4-dimensional symbol, thereby achieving a code rate of 5/6, — 6 codebits per 5 data bits — as compared to conventional 8PSK trellis codes, which have a code rate of 2/3. This gives the code a slightly higher spectral efficiency. Also, this code is designed for phase invariance, which means that the code will be decoded correctly even if the demodulator locks onto the wrong phase. Phase invariance is achieved using differential encoding, among other techniques. The decoder offers a selection of formats for the received signal vector, such as 7-bit phase, or 5-bit I and 5-bit Q. The advantages of the higher code rate and phase invariance are achieved at a slight compromise in bit error correcting performance.

For a complete description of the theory behind the codec, the reader should refer to "Trellis Coding with Multidimensional Signal Sets and Rotationally Invariant Trellis Codes," Ph.D. dissertation by Steven Silvio Pietrobon, University of Notre Dame [3].

3.2 NMSU Symbol Synchronizer

Before the codecs described in the previous section could perform the decoding, the received baseband data produced by the HRD had to be

modified. The phase information and a receive clock had to be derived from the analog I and Q signals. This task was accomplished through the use of the NMSU Symbol Synchronizer, which consisted of an Analog Signal Conditioner and a Digital Processing Unit. This section will discuss the design and operation of this system.

3.2.1 Analog Signal Conditioner

The levels of the HRD output signals had to be boosted before they could be processed by the Digital Processing Unit. This was accomplished by the Analog Signal Conditioner, using separate channels for the I and Q data. Figure 3.2-1 shows the circuitry used.

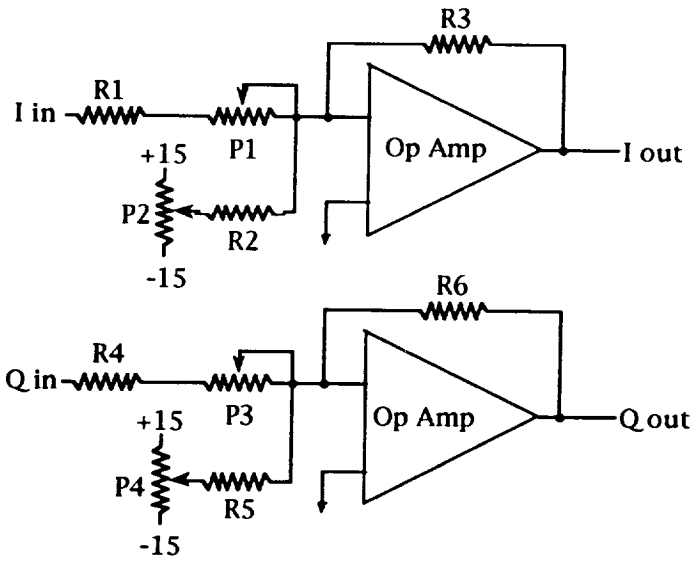


Figure 3.2-1 / Analog Signal Conditioner

The conditioner employed two separate high-gain inverting op-amps, one for each channel. Adjustments to a signal's dc offset and gain were made with the variable potentiometers shown in the figure above. P1 and P3 control the gain of the I and Q channel, respectively, while P2 and P4 control the dc offset, which was required to interface with the unipolar A/D converter in the Digital Processing Unit.

3.2.2 Digital Processing Unit

The NMSU Symbol Synchronizer was constructed to provide a clock, synchronized to the data, for the receive side of the racks. It is also used to convert the analog data produced by the HRD into digital data. All the digital steps in this process were performed by the Digital Processing Unit. The Stanford Telecomm model 2110A symbol synchronizer chip was employed to provide the synchronization and is the main component of this unit. Figure 3.2-2 shows the operational block diagram for this system.

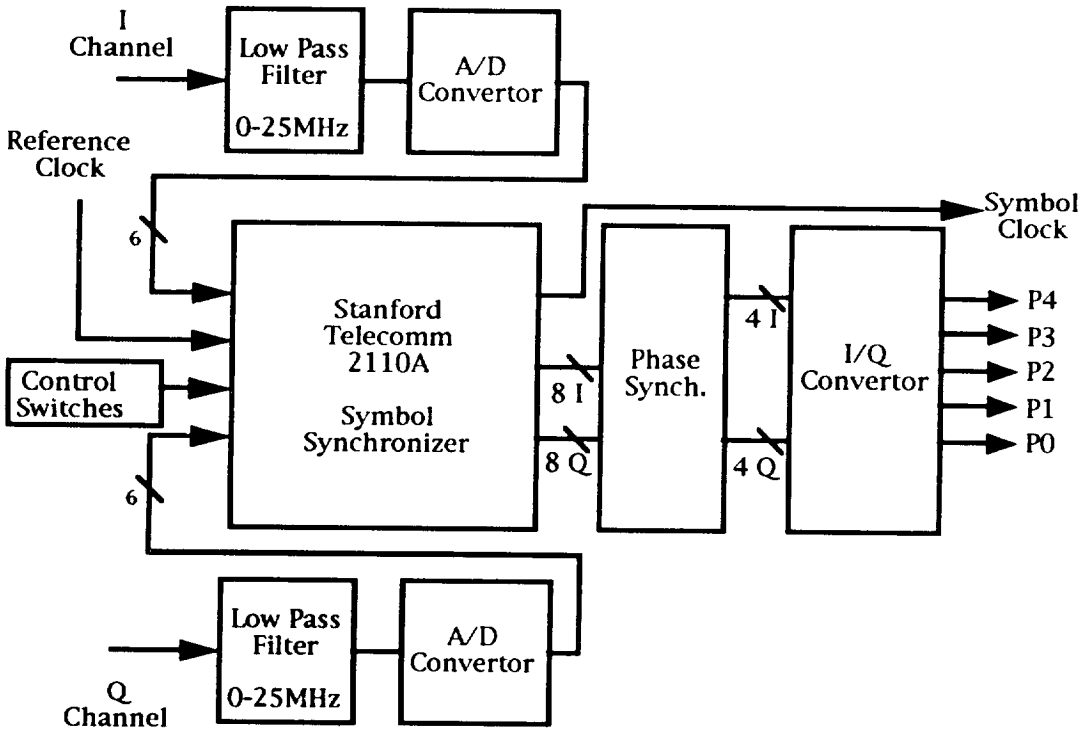


Figure 3.2-2 / Digital Processing Unit

The analog I and Q information is received by the system along with a reference clock, while the system produces five bits of phase and a synchronized clock. The I and Q channels are initially filtered before being processed by the Analog-to-Digital Convertors, which output six bits of information. The six bits of I and six bits of Q data, along with a reference clock, are then processed by the Stel 2110A, producing the synchronized symbol clock and eight bits each of I and Q data. The phase synchronization

circuitry then uses the sixteen data bits created by the Stel chip to create 4 bits of I data and 4 bits of Q data at the correct phase for the symbol received. This information is then converted to five bits of phase and sent on the decoder.

The chip must be initialized through the control switches on the front panel for the different system configurations. The control switches are used to write to specified memory locations on the chip to set the loop bandwidth, operating frequency, etc. The chip addresses used are as follows:

Address 11h: Loop Bandwidth Control Register

This register affects loop gain control factors K_1 and K_2.

Addresses 12h, 13h and 14h: Bit Rate Control Register

The 27-bit NCO is programmed with these three bytes, which are loaded into the 24MSBs of the 27-bit D-Phase Register. The formula for N_r, the number programmed in the NCO, is as follows:

$$N_r = R_s \times S_s \times A_i \times 2^{24}/f_c$$

where:

N_r = 24-bit number that establishes the nominal A/D sample rate
f_c = NCO input clock frequency
A_r = A/D convertor clock rate
R_s = symbol rate of PSK signal to be demodulated
S_s = number of accumulated samples per symbol

Address 17h: Loop Control Register

This register is used to open and close the loop and reset the chip.

For example, the following setup must be completed for the NMSU Codec:

Load 03h into address 17h.

This will reset the chip and open the loop.

Load 83h into address 17h.

This will put the chip in operational mode, with the loop open.

Load 2Ah into address 12h, AAh into address 13h and AAh into address 14h.

This combination will set the rate to 1Msps, as calculated using the equation described above as follows:

$$f_c = 48 \times 10^{-6}$$

$$A_r = 1$$

$$R_s = 10^6$$

$$S_s = 8$$

So,

$$N_r = 10^6 \times 8 \times 1 \times 2^{24}/(48 \times 10^{-6})$$

$$N_r = 2AAAAAh$$

3.3 HRD Modifications

The objective of this project was to test various TCM codecs using 8PSK modulation. In order to accomplish the desired testing, it was necessary to construct several additional pieces of equipment as discussed throughout Section 3. One of the major efforts required was to obtain carrier synchronization for the 8PSK modulated carrier and to be able to interface this carrier synchronization unit with the 370MHz IF at the WSGT. The most straightforward solution to this problem was to modify an existing WSGT demodulator to process the 8PSK format. The only unit available to be lent to NMSU for modification was the Harris-built High Rate Demodulator (HRD). This unit was designed in 1975 to process BPSK and QPSK signals. It employed a hard limited Costas crossover loop for carrier tracking and a separate I and Q mixing system for data demodulation. It was designed to operate at symbol rates from 10 to 75Msps. As the testing was conducted at

1Msps, the unit was not ideal for the project but, as stated, was the only one available. Any other approach would have involved considerable effort in just solving the interface and control problems associated with operation at WSGT.

The first of what turned out to be many modifications to the Harris HRD was the modification of the hard limited Costas crossover loop phase detector to a configuration that was capable of processing the 4-level I and Q signals associated with 8PSK. After considerable study, simulation and bread boarding, a phase detector employing 4-level quantizers in both the I and Q legs of the loop while retaining the basic Costas crossover configuration was selected. A full description of this modification was provided in a previous report, "Modification of the TDRSS High Rate Demodulator for 8-PSK Operation," by William P. Osborne and Gerald L. Stolarczyk [2]. This paper develops the background needed to understand the changes required and describes in detail the modifications made. These modifications included those required to run the device at 1Msps as well as the changes that will allow operation at 8PSK with the introduction of multi-level signals as opposed to the bi-level signals used in QPSK.

Initial testing of the modified HRD was encouraging in that the modified loop would lock up to and track 8PSK modulation. However, they were discouraging in that they unmasked several other problems associated with using the HRD in an 8PSK environment. The multi-level characteristic of the 8PSK signal presented most of the problems. First, the original lock detection circuitry was designed for bi-level signals. It employed full-wave rectifiers (FWR) and an unfiltered difference signal between the I and Q channel to estimate the noise level and compare it with the signal level. This information was used to determine the lock condition and to set the automatic gain control (AGC) levels. The process used did not allow modification for signals with four levels in I and Q. Hence, the lock detector in the HRD would not function with 8PSK. And without the lock detector the sweep and acquisition circuitry was not functional. Also, if the lock detector circuitry is not operating, the AGC circuitry will not work.

Further testing of the modified HRD in the presence of noise revealed another problem — the noise threshold of the modified loop was measured to

be between 76 and 78 dB C/KT. This was considerably higher than required for the testing of TCM as it was expected that the TCM codecs would operate at an Es/No of 7 to 9 dB or a C/kT of 67 to 69 dB for 1Msps symbol rate. A typical set of test results for the HRD threshold is shown in Figure 3.3-1.

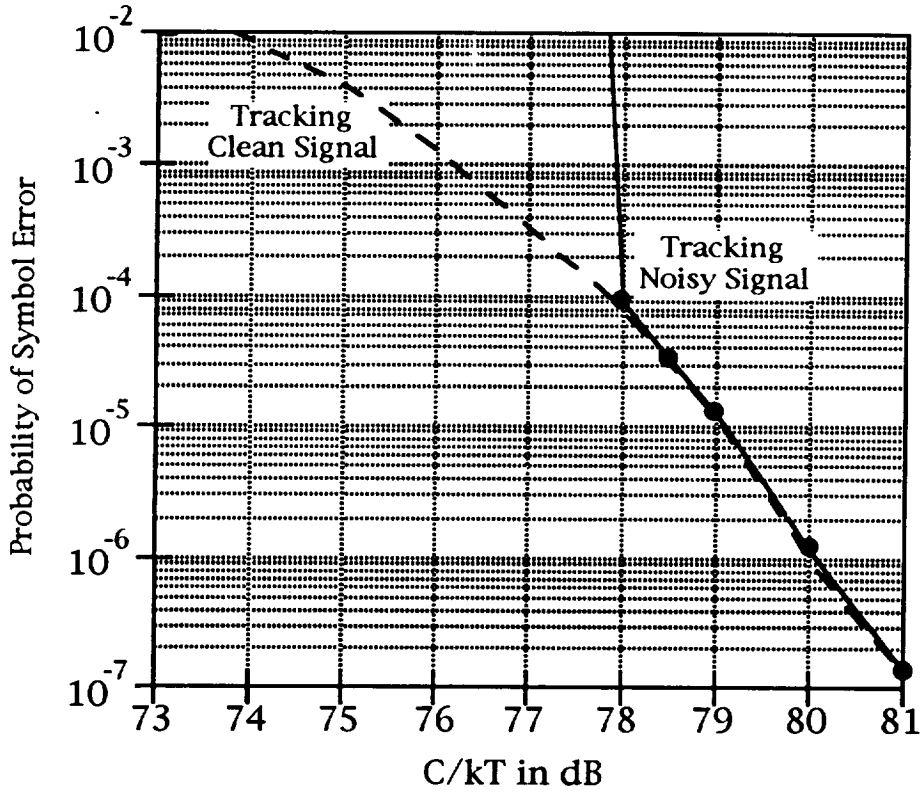


Figure 3.3-1 / HRD Performance Curve

These results were obtained by comparing the performance of the HRD and symbol synchronizer in an uncoded BER test using the internal HRD derived carrier for a reference in one case and using the Vector Modulator's coherent reference carrier as a recovered carrier in the baseline case. As can be seen from the figure, the basic system operates over a wide range of Es/Nos. But the modified HRD loop does indeed threshold at a Es/No that is unacceptably high for the intended coded experiment. It is expected that any 8PSK carrier loop will have a threshold and that the

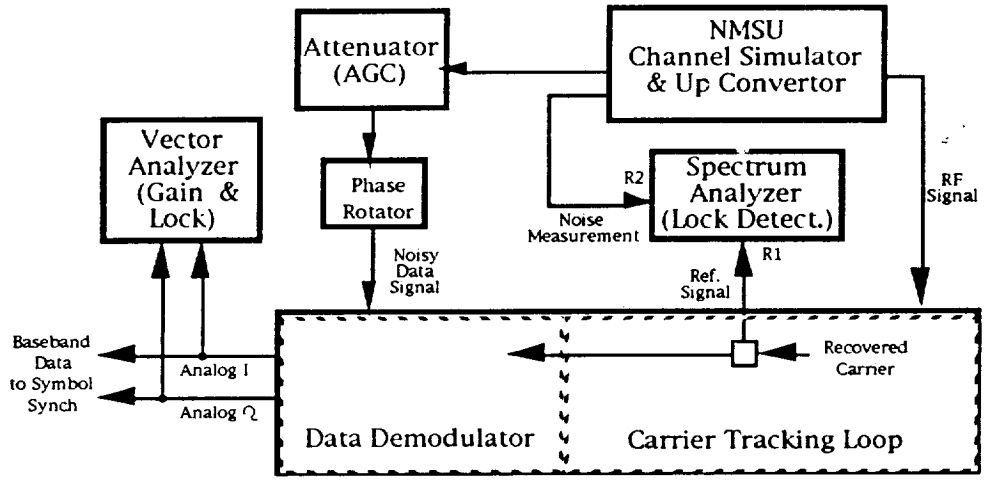
threshold will occur at a Es/No higher than one would expect based upon QPSK loops — due to the higher squaring loss associated with 8PSK loops. This effect was investigated in a companion grant [1]. Based upon both simulation and theoretical results, the modified HRD should have performed about 10 dB better than the results in Figure 3.3-1 indicate. There were several possible reasons for this degradation. First, the loop bandwidth of the modified HRD was calculated based upon the original HRD documentation. However, it was not measurable with the equipment at hand and the loop may have been wider than the Harris documentation indicated. Next, there was residual noise at the phase detector output due to the inter-symbol interference introduced by the filters added to the HRD, as well as by imbalances between the I and Q channels in the 15-year-old analog HRD. This noise affected the loop performance.

There were several design choices for fixing the HRD noise problem and lock detector problems. The choices were:

1. Scrap the approach of using the HRD and build a new 8PSK demodulator.
2. Continue to design modifications into the HRD to accommodate its weakness with respect to 8PSK.
3. Find techniques for compensating for the HRD problems using external devices.

Due to the time involved in approach one and two above and the need to keep the project near its promised schedule, the third approach was selected. The key step in implementing this approach was to take advantage of the fact that the HRD uses separate mixers for the phase detector in the carrier loop and the actual data detection process. The HRD was modified to allow separate signals to be used to drive the carrier tracking loop and the data demodulator. The test setup was then designed to allow a signal with a high C/kT to be used as an input to the carrier tracking loop at all times. A signal of varying Es/No was then applied to the data demodulator for the purpose of measuring BER versus Es/No (see Section 3.4 and Figure 3.3-2 below). In the satellite test the C/kT level available for driving the carrier

high C/kT to be used as an input to the carrier tracking loop at all times. A signal of varying Es/No was then applied to the data demodulator for the purpose of measuring BER versus Es/No (see Section 3.4 and Figure 3.3-2 below). In the satellite test the C/kT level available for driving the carrier loop varied between 85 and 90dB. As can be seen from Figure 3.3-1 this was well above the threshold of the loop and, hence, provided a recovered carrier from the satellite signal that could be used to demodulate the return signal and achieve the objective of testing TCM.



Harris High Rate Demodulator with NMSU Modifications

Figure 3.3-2 / HRD and Support Equipment

The other shortcomings of the HRD were readily solved with other external equipment once the basic configuration was made to work as described above. The lack of lock detector/AGC functionality was solved by two modifications. These were:

a) The AGC was disabled, the gain set to mid-range with a dc voltage and the functionality restored with an external variable attenuator under manual control.
b) The lock detector functionality was replaced by an external control unit that used manual switching to enable

sweep/lock track. External instrumentation was used to determine lock as well as the amplitude of the signal. These external units were the Vector Analyzer and the Spectrum Analyzer described elsewhere in Section 3.4.

When using the Pragmatic TCM decoder and uncoded testing, one additional problem required a solution — namely the phase ambiguity problem. The phase ambiguity problem is much more complex with eight symbols than it is with four. The phase cannot simply be rotated 90° when the demodulator locks on the wrong symbol, as with QPSK. With 8PSK, the phase must be rotated until the "000" symbol is in the correct absolute phase state, i.e., 22.5 degrees from the unmodulated carrier. This is also taken care of independent of the HRD. This led to the last of the additional modifications — disabling the HRD's internal ability to rotate the phase by 90 degrees. A phase adjustment device, consisting of a variable length cable, was then introduced to the system. By lengthening or shortening the path the IF data takes, the phase can be rotated through a range of more than 180°. This ability to rotate the phase of the data signal independent of the carrier reference allows the resolution of phase ambiguity when coupled with the ability of the Vector Analyzer to measure absolute phase.

An additional advantage of this scheme became apparent when testing through the satellite — the Es/No could be more quickly and easily varied by attenuating the system's noise source without involving the WSGT equipment or crew. There was only one disadvantage to the basic approach of separating the circuitry into the carrier loop and a data loop. The majority of the noise was no longer that of the actual channel. The noise introduced by the satellite link and the IFL was small compared to that supplied by the noise generator. However, with a reliable noise source, such as the one in the system, the difference was insignificant and the test results were unaffected. The overall modified HRD was shown in Figure 3.3-2 and the carrier recovery and data demodulation subsystem is shown in Figure 3.3-4.

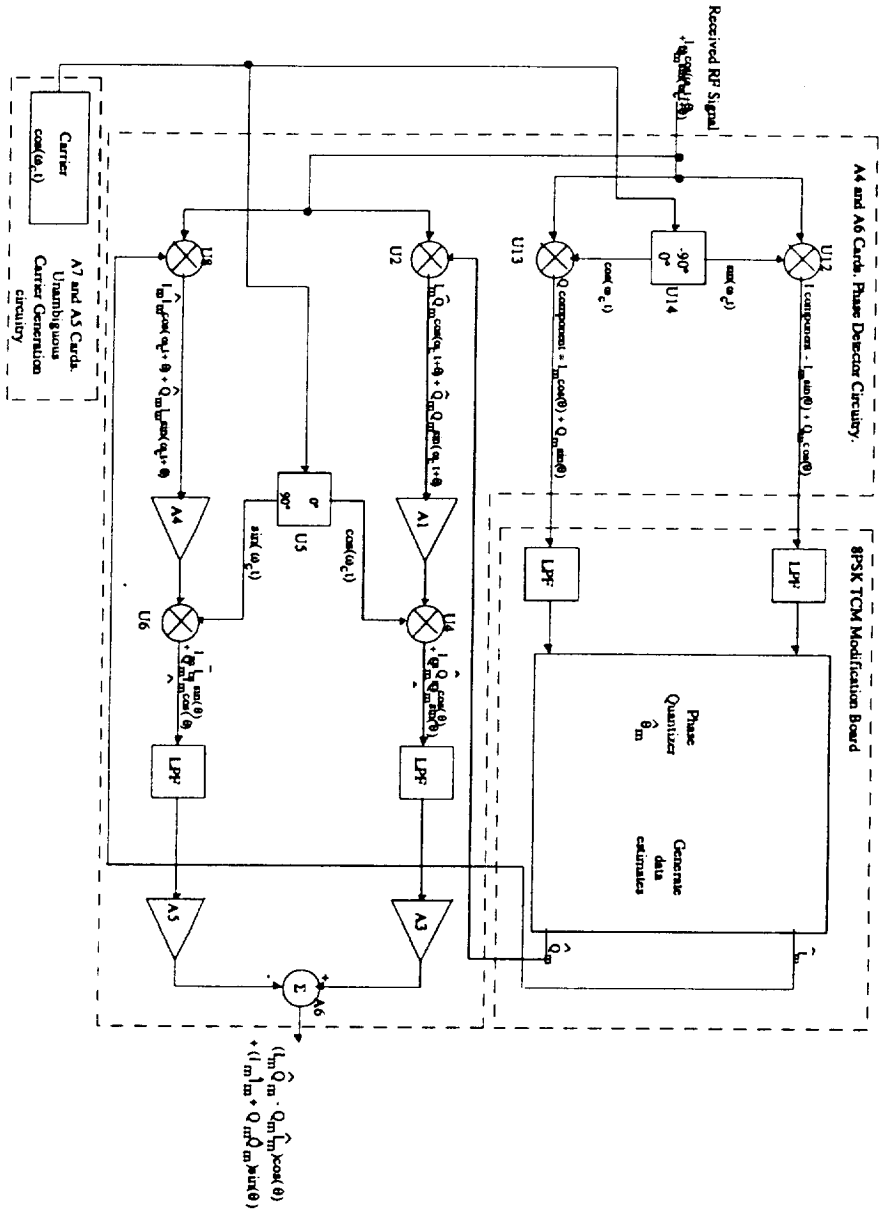


Figure 3.3-4 / HRD Block Diagram

3.4 Channel Simulation

The system used to encapsulate the data signal in noise before it is applied to the data demodulation circuitry of the HRD consists of two units in the rack: the Channel Simulator and the Up Convertor. Figure 3.4-1 shows a block diagram of the system.

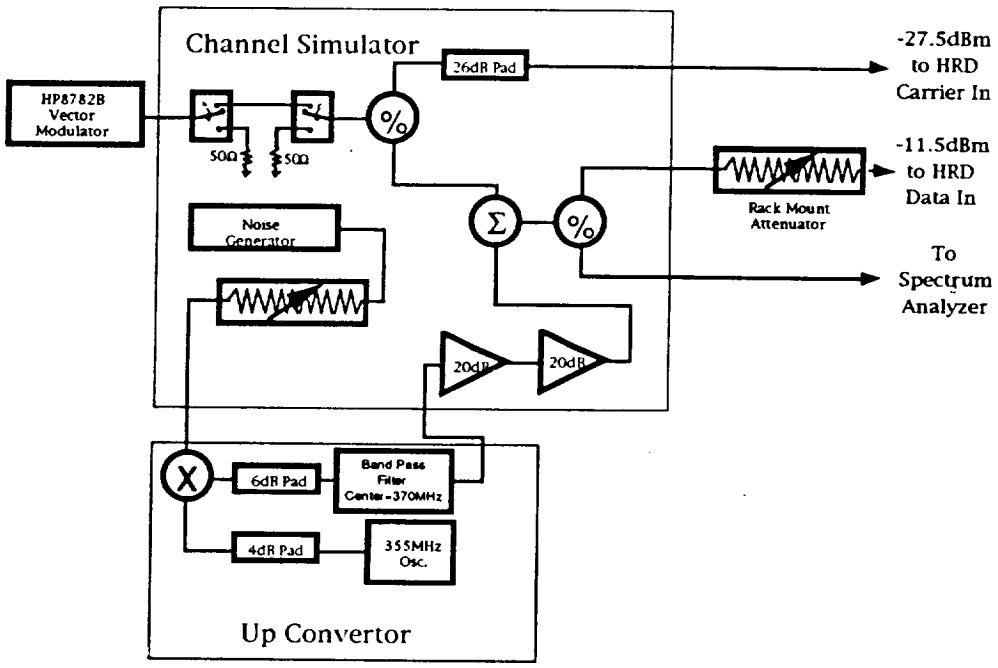


Figure 3.4-1 / Channel Simulator/Up Convertor System Diagram

The Channel Simulator and Up Convertor work together to provide a variable noise source. The noise produced is centered around the 370MHz carrier frequency used throughout the system with a span of 6MHz. Es/No can be varied by attenuating the noise signal via the attenuator knobs on the front panel of the Channel Simulator. Two switches, also on the Channel Simulator's front panel, are used to eliminate the input signal, leaving only the noise platform in the output signal.

The two-unit combination provides a total of three outputs, the first of which consists of the incoming signal adjusted to -11.5dBm, the proper level required by the HRD. This signal is supplied directly to the lock circuitry of

the HRD, giving it a signal with a high Es/No for acquisition. The second output is supplied to the HRD signal input. It consists of the signal surrounded by noise for the HRD to demodulate. This signal was set to -27.5dBm at the input of the demodulator. This was accomplished through use of the rack mount attenuators. Once this level was set for a given set of input levels it needed not be adjusted for different levels of Es/No. The final output is a copy of the second, including both the signal and the noise. But it is not attenuated and goes directly to the Spectrum Analyzer. When the modulation is off, the Spectrum Analyzer can be used to make C/kT measurements using this signal. This information is then used to calibrate the system.

The Channel Simulator is the main component of the noise system. It creates the noise, allows its attenuation, and sends it to the Up Convertor. The up-converted noise is then amplified and added to the input signal. Splitters are used with switches to produce the three required outputs. The signal supplied by the HP8782B Vector Modulator is the only input for this unit. This signal is first fed through two switches mounted on the front panel. By opening the switches, both sides of the switch combination are properly terminated with 50Ω loads. This prevents a number of problems that can arise as a result of unterminated lines. Beyond the switch combination, the signal is split into two legs. The first leg sends the signal through a 26dB pad to the front of the box. The input signal level must be adjusted to make this level -11.5dBm as required by the HRD lock circuitry. The other branch leads directly to an adder where it is combined with the noise signal.

The noise is created by a NC1106A noise generator made by Noise Com Inc. The noise has a bandwidth of 0-25MHz at the generator's output. This noise signal is fed directly to the attenuators mounted on the front panel, where the noise level is adjusted to produce the required value of C/kT. The output of the attenuators is connected to the unit's back panel, and from there to the input of the Up Convertor. The Up Convertor output is also received through the back panel and consists of the up-converted noise signal centered around 370MHz with a 6MHz bandwidth. This signal is amplified by two 20dB amps to bring the noise level up to operational levels. It is then combined with the input signal in an adder. The newly created noise+input

signal is then split. Both branches are connected to the front of the unit, one directly to the Spectrum Analyzer for measurement and the other signal to the Wavetek rack mount attenuator and the HRD input. This attenuator must be set to make the signal level at the input of the HRD -27.5dBm.

The Up Convertor's function is straightforward. It takes the input, the baseband noise signal supplied by the Channel Simulator, mixes it with a 355MHz signal then filters it with a 370MHz bandpass filter before returning it to the Channel Simulator. The 355MHz signal is supplied by a Vectron Crystal Oscillator, model CO-255B16. The oscillator is isolated by a 4dB pad and then fed to the mixer, where the input noise signal is also supplied. The up-converted noise is sent through a 6dB pad, again for isolation purposes. Finally, the signal is filtered by a 370MHz filter with a bandwidth of 6MHz. The resulting signal is returned to the back of the unit where it is routed to the Channel Simulator.

3.5 Commercial Support Hardware

In order to save both time and effort and to ensure a quality test system, the NMSU research team incorporated a number of commercially available devices into the system. Many of these devices are used for monitoring purposes and were necessary for completing the tests. Others were employed to simplify or solve problems that were encountered during construction of the test set. This section will describe each of these components and explain their place in the system.

3.5.1 HP3784A Bit Error Rate Test Set

As described in Section 2, the HP3784A Bit Error Rate (BER) Test Set is both the start and end of the data path through the system. It is capable of generating a pseudo-random number (PN) sequence of varying length along with a transmit clock synchronized to the data. The rate of this signal was easily varied as was its format. When supplied with the received data and a corresponding clock, the set measures the number of errors made. This information can be displayed as accumulated errors, time between errors, or any number of other forms. The test being performed required the

information form the unit was designed for — namely BER, a measure of bit errors per unit time.

3.5.2 HP8782B Vector Modulator

The transmitter used for testing purposes was the HP8782B Vector Modulator. This modulator is a very powerful and flexible device, capable of producing Binary, Quadrary and Octal PSK (BPSK, QPSK, 8PSK) signals as well as a range of QAM signals. Of course, only the 8PSK data format was employed for this test. The data was supplied to the transmitter in the form of three parallel data bits and a transmit clock. Both the transmit signal frequency and amplitude were set with the touch of a few buttons. Then, the modulated signal was taken from the front panel in the proper form.

The only difficulty with the modulator dealt with the use of 8PSK. When the component was designed and constructed, 8PSK was selected as its test mode. This meant that a few things about this format were not as one would expect. The only difference that actually caused a problem was a Gray-code phase map employed by the unit. Although this may be viewed as a very small point, the entire test system was based upon a naturally mapped signal constellation. To remedy the situation, an additional component was added to the system to map between the two phase constellations. This is described in Section 3.6.1.

3.5.3 HP4195A Spectrum Analyzer

One of the most important monitoring devices in the test system was the HP4195A Spectrum Analyzer. It was used extensively throughout the testing. The device has the ability to display the spectrum of any signal from 0 to 500MHz. And, it can be programmed to perform measurements and calculations.

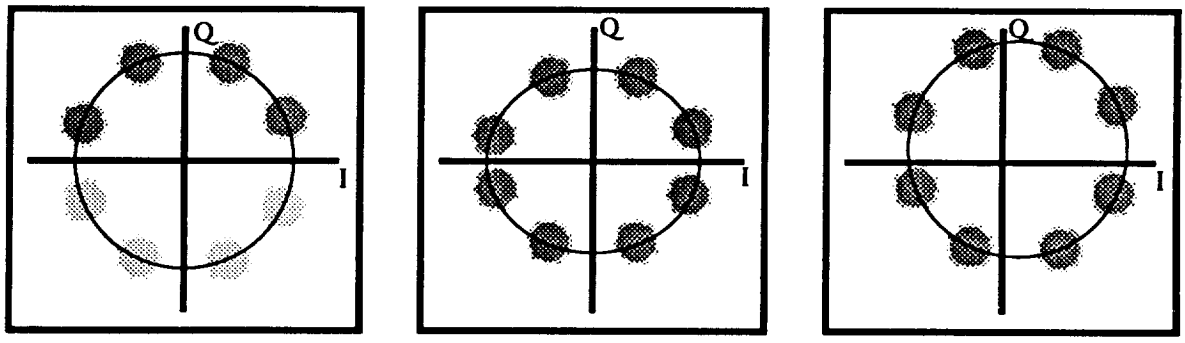
The unit was employed by the test system in two ways. First, it was used to constantly monitor the recovered carrier of the HRD. This allowed the lock status of the demodulator to be evaluated visually. This, as described in Section 3.3, allowed the tests to be completed without the design of lock detection circuitry for the demodulator. Second, by programming the device to make carrier and noise power measurements on the data signal produced

by the Channel Simulator, it was used to calculate C/kT for noise calibration purposes. Section 4 describes this process in detail, including a listing of the program used to make the measurements.

3.5.4 HP8981A Vector Analyzer

Another important measurement device in the test network was the HP8981A Vector Analyzer. It was used throughout the testing to give the operator a visual image of the data constellation being transmitted and received. The demodulated data at the output of the HRD were displayed in vector form throughout the testing to give information such as phase, magnitude and relative frequency of each of the constellation points.

The Vector Analyzer was the primary indicator of problems in the setup. By checking the display, the user could quickly see that the system was operating with the right type of data, meaning random data of equal probability in each bit. If this was not the case, some of the constellation points would appear dim or not at all. An example of this situation is shown in Figure 3.5-1 (a) below. The relative magnitude of each channel could also be confirmed when the constellation was circular. If it appeared oblong or oval, the user immediately knew that the gain of one of the channels needed to be adjusted. Similarly, if the constellation was not symmetric around the origin, the dc offset of one or both of the channels needed to be adjusted. Examples of a gain and dc offset problems are shown in Figures 3.5-1 (b) and (c).



(a) MSB not varying with same probability

(b) Q channel gain is too low

(c) both I and Q channel dc offsets are too high

Figure 3.5-1 / Example of Errors Seen on Vector Analyzer

Since the Automatic Gain Control circuitry of the HRD was disabled to make 8PSK demodulation possible, the Vector Analyzer became the indicator of the data signal's gain. By measuring the proper level at the input to the HRD's data demodulation circuitry, the proper constellation amplitude was established. Once that was known, the operator could confirm the correct data level at the input to the HRD by monitoring the size of the constellation displayed on the screen of the Vector Analyzer.

3.5.5 HP3324A Signal Generator

The Stanford Telecomm model 2110A symbol synchronizer chip, used by the Digital Processing Unit of the NMSU Symbol Synchronizer, required a reference clock for proper operation. This allowed the chip to clock in commands without the presence of the receive clock. This reference clock was supplied by an HP3324A Signal Generator.

3.5.6 Wavetek 5081 Rack Mount Attenuator

Although the gain of the data signal to be demodulated by the HRD was monitored by the Vector Analyzer (see Section 3.5.4), it was set by a Wavetek 5081 Rack Mount Attenuator. This attenuator has a range of 0 to 81dB, incremented by 10, 1 or .1dB. This allowed the user, while monitoring the level on the Vector Analyzer, to set the gain of the signal to within .1dB.

3.5.7 ARRA D2448A Phase Rotator

Since the HRD could acquire and lock to any one of eight symbols, the problems due to phase ambiguity were much more important with 8PSK than with QPSK. As discussed in Section 3.3, the NMSU codec and uncoded testing required absolute phase resolution. This was provided by the introduction of an ARRA D2448A Phase Rotator. With this device, the phase of the data could be rotated to the correct position by monitoring the constellation on the Vector Analyzer and adjusting the phase.

3.6 Other Support Hardware

Two other devices were designed and built by the research team at NMSU to solve problems encountered during construction of the test system. A Symbol Map was constructed to interface with the Vector Modulator, as described in Section 3.5.2, and a PN Generator was built to provide the additional data channels required for uncoded 8PSK testing (see Section 4.3). This section will discuss both units and their operation in the system.

3.6.1 Symbol Map

The interface between the data sources and the HP8782B Vector Modulator required a translation between symbol maps. This is because the map used by the modulator was not mapped according to natural phase like the one used throughout the rest of the system. The difference between the two phase maps is demonstrated in Figure 3.6-1.

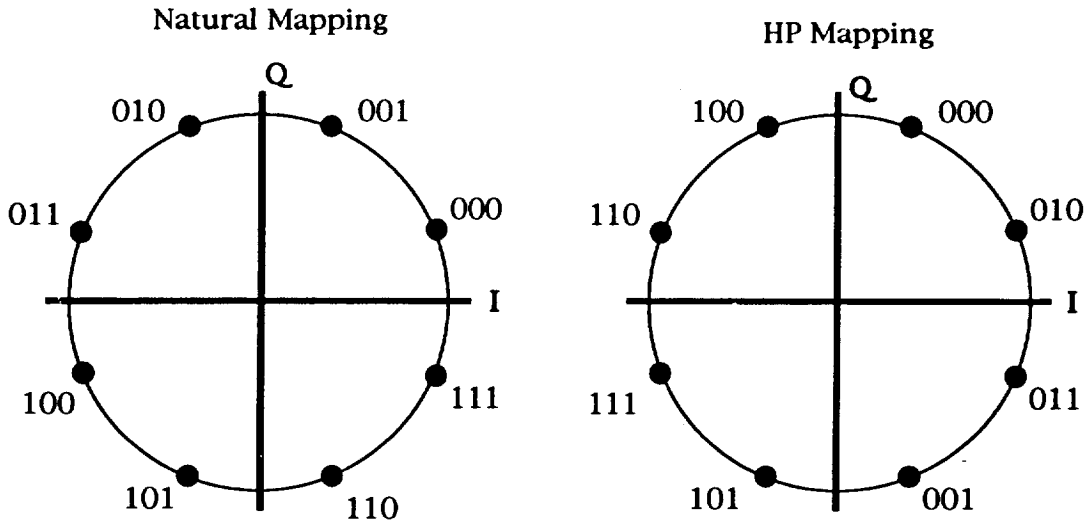


Figure 3.6-1/ Map Comparison

Translation is performed through the use of simple logic chips. Table 3.6-1 explains the required translation.

Inputs			Outputs		
X2	X1	X0	Q1	I1	I0
0	0	0	0	1	0
1	0	0	0	0	0
0	1	0	0	0	1
1	1	0	0	1	1
0	0	1	1	1	1
1	0	1	1	0	1
0	1	1	1	0	0
1	1	1	1	1	0

Table 3.6-1 / Symbol Map Translation

The equations describing the process in terms of the input bits X0, X1 and X2 and the output bits I0, I1 and Q1 are:

$$I_0 = X_0 \oplus X_1$$
$$I_1 = \overline{X_1 \oplus X_2}$$
$$Q_1 = X_0$$

where X0 and I0 are the LSBs.

Figure 3.6-2 shows the logic used to implement the equations. Only exclusive-or gates were used, one of which was implemented as an invertor as required by the equation for I1.

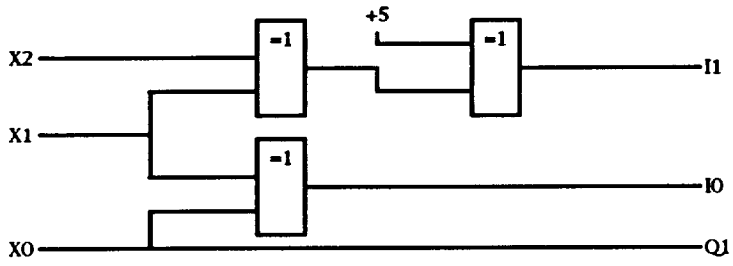


Figure 3.6-2 / Logic Diagram for Symbol Map

3.6.2 PN Generator

In order to produce 8PSK modulation during the uncoded tests, three separate data channels had to be produced. One channel was produced by the BER test set — the channel on which the BER measurements were performed.

The other two data channels were produced for the uncoded 8PSK test by the PN Generator. One of the channels was also used for the outboard data channel of the NMSU codec.

The PN Generator consists of a seven-bit shift register, as shown below in Figure 3.6-3. The data created by the BER test set was clocked into the register, while data was tapped off the third and seventh positions in the register. The register is clocked by the BER test set's transmit clock, making the data signals synchronous. This produced two copies of the data sequence delayed by three and seven bits respectively. The register is clocked by the BER test set's transmit clock, making the data signals synchronous.

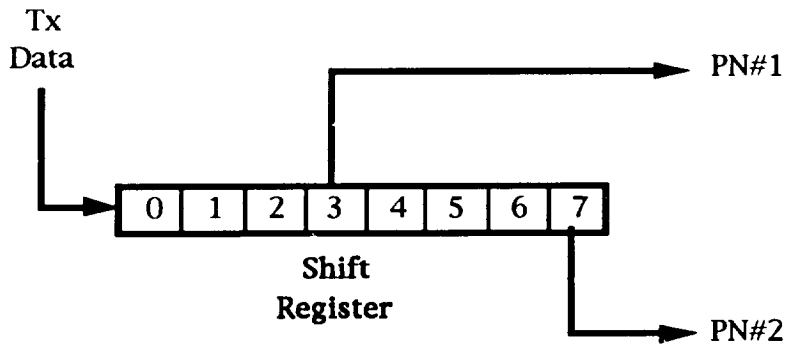


Figure 3.6-3 / PN Generator

Since the sequence created by the BER test set was very long — 2^{23} bits are transmitted before the sequence repeats, the two channels of delayed data appeared to be random data to the entire system — except the BER test set. Most importantly, the eight symbols in the 8PSK constellation were transmitted with equal probability. Another advantage that became apparent was the ability of the BER test set to synchronize to any of the three data sequences. The delay had no effect on the test set's operation. Therefore, the BER could be measured on any of the three channels. This made it possible to measure the performance of each uncoded bit as well as both the inboard and outboard channels of the NMSU codec without reconfiguring the system.

4. Theoretical Basis

To analyze the data taken during the tests, there needed to be a high confidence level in the data. Not only was it critical to be sure of the BERs measured, the value of Es/No for which each of the data points was taken was also very important. Significant errors in either of these measurements would make comparison to different tests and to theory impossible. Also, the procedure for measuring the coding gain of each of the codecs had to be performed with great care. If done without a great deal of thought, the results could lead to false assumptions of the coding gain achieved. This section will discuss each of these topics in detail.

4.1 Calibration of C/kT

Since the evaluation of the tests performed depended on an accurate measure of the signal-to-noise ratio, the calibration of the carrier-to-noise (C/kT) measurement was very important. The test required a consistently good measure of C/kT to allow comparisons to be made to different error rate curves and theoretical curves. This section will discuss the measurement of C/kT for both loopback testing, in which no external noise was present in the system, and testing through both the IFL and the TDRSS channel where external noise must be dealt with.

4.1.1 Loopback Calibration

As different tests were performed the C/kT was varied over a range of values. This allowed the measurement of the system's performance over a range of conditions. To assure that the data was accurate, this ratio had to be measured often. This was accomplished in the system itself through the use of the HP4195A Spectrum Analyzer.

The Spectrum Analyzer was programmed to make such a measurement and was calibrated against an HP435B Power Meter and a filter of known (measured) noise bandwidth. Figure 4.1-1 shows a flow diagram of the procedure used. The program used, written in Hewlett Packard's pseudo-Basic, is shown below.

```
10 CMT "C/KT MEASUREMENT"          program title
20 FNC2                            start environment setup
30 RST                             reset analyzer
40 PORT3                           select input port
50 TRGM1                           select single sweep mode
60 ATR2=30                         attenuate input port
70 R4=0                            clear register 4
80 R6=0                            clear register 6
90  FOR R7=1 TO 5                  start outer loop, repeat 5 times
100    MCF1                        select marker mode
110    SAP1                        select dBm as measurement unit
120    CENTER=370MHZ;SPAN=5KHZ     set up region for carrier measurement
130    VFTR1; RBW=1KHZ             turn on video filter, set res. bandwidth
140    SWTRG                       trigger the sweep
150    AUTO                        auto scale
160    MKMX; R1=MKR                marker to max, store freq. in R1
170    R4=10**(MKRA/10)+R4         add real values of amplitude
180    R2=R1                       copy R1 to R2
190    CENTER=370MHZ; SPAN=6MHZ    set up region for noise measurement
200    VFTR1;RBW=10KHZ             video filter on, set resolution bw
210    SWTRG                       trigger the sweep
220    AUTO                        auto scale
230    DISP "COUNT=",R7            display loop number
240    R5=-1                       set R5 to -1
250      FOR R0=1 TO 100           start noise measurement loop
260        R5=-1*R5                switch polarity of R5
270        R2=R1+R5*((R0+12000)+1000000)   calc. marker position
280        MKR=R2                  move marker to measure noise
290        R3=MKR1                 store amplitude in R3
300        R3=10**(R3/10)          turn R3 into a real number
310        R6=R6+R3                add noise measurements
320      NEXT R0                   end noise measurement loop
330    NEXT R7                     end outer loop
340    R4=10*LOG(R4/5)             average carrier in dBm
350    R3=10*LOG(R6/500)           average noise in dBm
360    R3=R4-R3+40.7               ratio + noise filter adjustment
370    DISP "C/N(DBM)= ",R3        display result
380    BEEP                        sound end of run
390    PAUSE                       wait for reading
400    PORT1                       start returning to original setup
410    CENTER=370MHZ, SPAN=2MHZ    set display window
420    RBW=100KHZ                  select resolution bandwidth
430    SWM=1                       select continuous sweep
440    VFTR0                       video filter off
450    MRK=370MHZ                  center marker at carrier frequency
460    AUTO                        auto scope
470    END                         end of program
```

Program 4.1-1 / C/kT Measurement Program

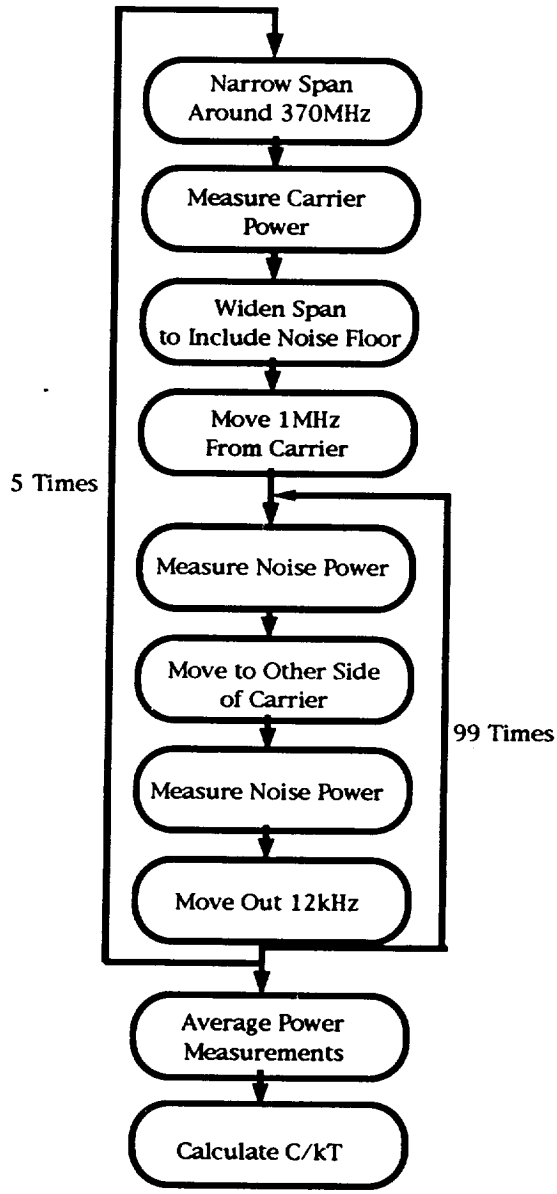


Figure 4.1-1 / Flow Diagram of C/kT Measurement

The procedure used by the program can be broken down into the following steps. First, the environment is set up for the measurements to be made. The analyzer then zooms in on the unmodulated carrier signal, finds the maximum and stores the amplitude. After moving away from the carrier, it then spans the width of the noise signal, adding 100 independent noise measurements. The program repeats these measurements five times before

finding the average carrier power and the average noise power. The ratio is found by subtracting the noise power, in dBm, from the carrier power, in dBm. A correction factor is also added to account for the noise bandwidth of the filter and the slight roll-off of the noise. The result is displayed and then the analyzer is returned to the mode used to monitor the lock status of the HRD.

The program takes a large number of measurements to guarantee the accuracy needed to perform quality tests. The results produced by this program agreed with that produced by measuring the noise through a filter of known bandwidth. Also, the result is repeatable to within .1dB of C/kT.

4.1.2 Channel Calibration

Although the same program and C/kT calibration procedure was used in both the loopback tests and the IFL and TDRSS tests, additional steps were required to account for the noise present when testing through an external channel. The value of C/kT measured by the program was still accurate with the external noise. But the attenuation of the noise was no longer linear since only the noise injected by the system was being attenuated. Unlike the loopback setup, adjusting the attenuator 1dB no longer dropped the value of C/kT by 1dB.

The total noise could be described as:

$$\text{Total Noise} = \left(\frac{\text{System Noise}}{\text{Attenuation}}\right) + \text{External Noise}$$

This equation was used to develop a lookup table to facilitate the testing. During tests with external noise, the data was taken in the same manner as in the loopback tests. Then, before the data was plotted, the values of C/kT corresponding to the data points were adjusted according to this table. The table is shown below in Table 4.1-1.

C/kT Measured (dB)	C/kT From Satellite			
	85dB	86dB	87dB	88dB
66	65.95	65.96	65.97	65.99
67	66.93	66.95	66.96	66.97
68	67.91	67.93	67.95	67.96
69	68.89	68.91	68.93	68.95
70	69.86	69.89	69.91	69.93
71	70.83	70.86	70.89	70.91
72	71.79	71.83	71.86	71.89
73	72.73	72.79	72.83	72.86
74	73.67	73.73	73.79	73.83
75	74.59	74.67	74.73	74.79
76	75.49	75.59	75.67	75.73
77	76.36	76.49	76.59	76.67
78	77.21	77.36	77.49	77.59
79	78.03	78.21	78.36	78.49
80	78.81	79.03	79.21	79.36
81	79.54	79.81	80.03	80.21
82	80.24	80.54	80.81	81.03
83	80.88	81.24	81.54	81.81
84	81.46	81.88	82.24	82.54
85	81.99	82.46	82.88	83.24

Table 4.1-1 / C/kT Adjustment Chart

4.2 Coding Gain and Implementation Loss

The measurement of coding gain was crucial to the evaluation of the test results. One of the main objects of this test was to confirm the theoretical coding gains of the two codecs under test. The procedure used is explained in this section.

During each stage of testing, an uncoded test was performed to determine exactly how the system without any coding performed as compared to theory. This yielded a measurement of the implementation loss in the system, which was also present in the coded tests. The implementation loss was measured in dB as the difference between the required values of Eb/No to perform with a given error rate, for the actual system and for theory. For example, the 8PSK theory curve crosses $5x10^{-3}$ at 8.6dB Eb/No. If the modem's curve was measured to $5x10^{-3}$ at 9.8dB Eb/No, this would

indicate an implementation loss of 1.1dB at 8.6dB – the actual modem requires an Es/No 1.2dB higher than theory predicts.

After each codec was tested, the implementation loss was used to determine how the codec would have operated had the system been lossless. If the system were operating with 1.2dB of implementation loss as in the previous example, and the codec's performance curve crossed 10^{-5} at 8.1dB Eb/No, the performance curve of the codec with a lossless system would have crossed this point at 6.9dB Eb/No.

Once the corrected performance was established, the coding gain was measured. This was done by comparing the performance of the codec to that of QPSK in the same manner implementation loss was measured. Since QPSK theory predicts an error rate of 10^{-5} at 9.6dB, the codec in the previous example would have a coding gain of 2.7dB.

4.3 Bit and Symbol Error Rates

Due to the difference in test system configurations required for uncoded and coded 8PSK testing, the form of measurement was different for each. The encoders under test produced the required data — three parallel bit streams, while three separate channels had to be used for the uncoded testing. For this reason, the performance measurement techniques varied. For the uncoded tests, one of the data channels was selected to measure the symbol error rate (SER). Coded testing allowed direct measurement of the system's BER. This section will discuss the measurement techniques used for each test format.

4.3.1 Uncoded 8PSK Performance Measurement

The first system configuration tested was uncoded 8PSK, in which the transmit data is fed directly from the BER test set to the modulator while the receive data is returned directly from the symbol synchronizer to the test set. It demonstrated the absolute capabilities of the 8PSK system. Conducting this test allowed a clear comparison to be made between 8PSK modulation and QPSK modulation, as well as allowing the measurement of the coding gain for each of the codecs.

This form of testing is not as straightforward as initially thought. The entire system operates around three-bit words, the basis of 8PSK modulation.

During coded testing, a single-bit stream is accepted by the encoder in operation, which creates the three-bit streams to be modulated. At the output of the decoder, a single-bit stream is returned to the BER test set. This allows the monitoring of errors on all three bits of each word simultaneously. Uncoded testing does not allow such luxury unless one builds a mux/demux and phase map specifically for uncoded testing. We elected not to add this complexity to the system. Instead, only one bit of each word was monitored at a time, and each bit acted differently under error conditions.

The BER on the LSB, middle bit and MSB cannot be measured in the same way. When considering only the nearest neighbor errors, errors in which only one of the closest constellation points to the one transmitted is received, errors on the different bits in the symbol occur at different rates. For example, if a nearest neighbor error occurs, there will be an error in the LSB all the time, in the middle bit half the time and in the MSB only a quarter of the time. The relationship between nearest neighbors and specific bit errors is shown in Table 4.3-1 below.

Word Transmitted	Nearest Neighbor Error	Error made		
		S_2 (MSB)	S_1	S_0 (LSB)
000	111	Yes	Yes	Yes
	001	No	No	Yes
001	000	No	No	Yes
	010	No	Yes	Yes
010	001	No	Yes	Yes
	011	No	No	Yes
011	010	No	No	Yes
	100	Yes	Yes	Yes
100	011	Yes	Yes	Yes
	101	No	No	Yes
101	100	No	No	Yes
	110	No	Yes	Yes
110	101	No	Yes	Yes
	111	No	No	Yes
111	110	No	No	Yes
	000	Yes	Yes	Yes

Table 4.3-1 / Nearest Neighbor Errors

Since nearest neighbor errors are by far the most likely, they were the only ones that needed to be considered. Taking this information into account, BER measurements on each of the bits could be made and compared effectively. The rate measured on the MSB need only be multiplied by four while multiplying that measured on the middle bit by two. By comparing these normalized rate curves, it was verified that all three bits were acting independently.

Additionally, the fact that the LSB is in error every time a nearest neighbor error occurs allowed us to measure the system's symbol error rate by monitoring that bit alone. Once it had been shown that the three bits operated independently with the same probability of symbol error, the measurement of the LSB, which shows each and every nearest neighbor error, was an effective measure of the system's SER.

Accomplishing this test then became very easy. The data stream to be transmitted and then checked upon demodulation was sent from the BER test set through the LSB during modulation. The other two bits were fed with delayed versions of the data. To the rest of the system, the delayed data appeared random, assuring that each of the eight constellation points occurred with equal probability. Upon reception and demodulation, the symbol synchronizer returned the LSB of the hard phase information (three bits of phase) to the BER test set and the SER measurements were made.

Since the data was recorded in terms of SER, this is how it will be presented in Section 5. All uncoded 8PSK measurements were compared to the 8PSK theoretical SER, in the form of error rate curves. This allowed a direct comparison between the curves for measurement of implementation loss as discussed in Section 4.2.

4.3.2 Coded 8PSK Performance Measurement

As mentioned in Section 4.3.1, the measurement of coded error rates was more straightforward than the measurement of uncoded error rates. By monitoring the output channels of the codecs, the BER of the system could be measured directly.

There was a difference between the measurement technique used for each of the codecs. Since there was only a single channel involved with testing the UND/USA codec, unlike the inboard and outboard channels of

the NMSU codec, only one measurement was required for this codec. Each channel of the NMSU codec required measurement to fully test the codec's performance. Therefore, most of the resulting curves presented in Section 5 will include a single BER curve for the UND/USA codec and two curves for the NMSU codec. The only exception was the final test of the NMSU codec over the TDRSS channel. In each of the tests leading up to this one, the outboard data channel — the channel not processed by the rate 1/2 Viterbi encoder — performed as expected. Due to limited satellite time as a shuttle launch approached, it was decided that measurement of the inboard channel alone would sufficiently measure the codec's performance through the channel.

Since each of the codec's curves were plotted as measured BER versus Eb/No, they could be compared directly to uncoded QPSK theoretical probability of bit error. This allowed measurement of coding gain as discussed in Section 4.2. To maintain consistency of coding gain measurement, each of the coding gain calculations were based on QPSK's theoretical performance of a 1×10^{-5} BER at 9.6dB Eb/No. Each of the curves in Section 5 showing coding gain will include this point.

4.4 Bit Error Rate Measurement Validation

While making BER measurements, one cannot be completely confident in the measurement made without allowing an infinite number of symbols to be transmitted. Since this is not feasible, a level of confidence must be specified that will be acceptable for the test being made. A higher confidence level requires that more bits be sent over the link.

For the testing to be performed, the Chernoff Bound [7] was used to find the number of transmitted bits required to ensure that the BER measurement made will be within 5% of the actual value, with a 95% probability. Figure 4.4-1 shows the results in graphic form.

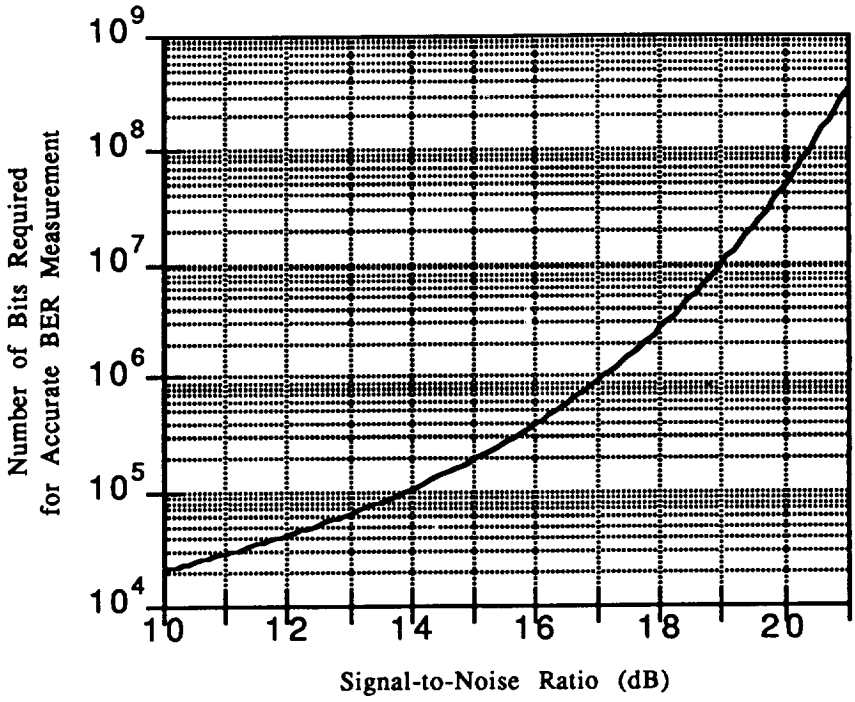


Figure 4.4-1 / Number of Bits Required vs. Es/No

The procedure used was as follows:

The Chernoff Bound states that:

$$P(\frac{1}{N}\sum_{i=0}^{N} y_i > d) \leq E^N(e^{\lambda_o(y-d)})$$

where,

$$d = p+\varepsilon = \frac{E[ye^{\lambda_o y}]}{E[e^{\lambda_o y}]}$$

For the binary symmetric channel,

$$\lambda_o = \ln(\frac{d(1-p)}{p(1-d)})$$

For the accuracy required,

$$\varepsilon = 0.05p$$
$$d = p + \varepsilon = 1.05p$$

and,

$$E^N[e^{\lambda_o(y-d)}] = \left(\frac{p}{d}\right)^d \left(\frac{1-p}{1-d}\right)^{1-d}$$

So,

$$.0005 = \left[\left(\frac{p}{d}\right)^d \left(\frac{1-p}{1-d}\right)^{1-d}\right]^N$$

Solving for N,

$$N = \frac{\log_{10}(.0005)}{\log_{10}\left[\left(\frac{1}{1.05}\right)^{1.05p} \left(\frac{1-p}{1-1.05p}\right)^{1-1.05p}\right]}$$

A program was developed to solve this equation. The probability of error, p, is chosen for the different values of Es/No according to the theoretical value for the given modulation format. These theoretical values are found using

$$P(\varepsilon) = 2Q\left[\sqrt{\frac{E_s}{N_o}} \sin\left(\frac{\pi}{8}\right)\right] \text{ for 8PSK}$$

where

$$Q[x] = \frac{1}{\sqrt{2p}} \int_x^\infty \exp\left(-\frac{u^2}{2}\right) du$$

The program used to develop this information, written in C, is as follows:

```
/* Chernoff bound calculation */
/* Ted Wolcott and Brian Kopp */

#include <stdio.h>
#include <stdlib.h>
#include <math.h>

main()
{

int i;                          /* count through Es/No in dB */
int n;                          /* count through integration */
double es_no;                   /* real value of Ex/No */
double epskraw;                 /* P(e)8psk = 2 Q[epskraw] */
```

```
double int8;                                    /* integration variable for 8PSK */
double p8;                                      /* prob. of error for 8PSK */
double d18;                                     /* denominator term 1 for 8PSK */
double d28;                                     /* denominator term 2 for 8PSK */
double N8;                                      /* # of samples required 8PSK */

/*declare output file parameters*/

FILE *outfile;                                  /* output file */
char *modehold;                         /* mode (read/write) */
char *namehold1;                                /* output file name */

/*initialize file output parameters*/

modehold = "w";
namehold1 = "NvsEs/No";
outfile = fopen(namehold1,modehold); /* open the output file */

for(i=0;i<220;i=i+1)                            /* loop from Es/No=0 to 22 dB */
{

        es_no = pow(10.0,(i*1.0)/100.0);        /* convert from dB */


        /* find Q[ ] arguments */

        epskraw = sqrt(es_no)*0.382683;

        int8 = 0.0;                             /* reset integration variable */


        for(n=0;n<=10000;n=n+1)                 /* loop through 10000 samples */
        {
                int8 = int8 + (1/1000.0)
                        *exp(-(epskraw+n/1000.0)
                        *(epskraw+n/1000.0)/2);
        }

        p8 = int8*0.797885;                     /* find p(e) */

        d18 = pow(0.952381,1.05*p8);            /* determine den. terms */

        d28 = pow((1.0-p8)/(1.0-1.05*p8),(1-1.05*p8));

/* calculate Number of samples */
        N8 = log10(0.0005)/log10((d18*d28));

/* output data to data file */
        fprintf(outfile,"%f %f\n",i/10.0,ceil(N8));
}
fclose(outfile);                                /* close the data file */
}
```

Program 3.5-1 / Transmitted Bit Requirement Calculations

5. Test Results

This section will present all the data collected in graphical form. The analysis performed on the data will also be presented as will the conclusions drawn from each test.

5.1 In-Lab Performance

Testing was performed in the NMSU laboratory to determine exactly how the test system, including the codecs, would behave under test conditions. This provided the baseline for each test — a basis for comparison during each stage of testing. This section will present the results of these tests.

5.1.1 Uncoded 8PSK Testing

The uncoded 8PSK test was performed to measure the implementation loss of the test system. Two graphs are presented below. Figure 5.1-1 shows the performance of the HRD system operating with uncoded QPSK modulation. This shows the original implementation of the system before the modifications to the HRD were made. As can be seen, the original system had 1.0dB of implementation loss, compared to theoretical QPSK performance, at 8dB Eb/No. 8PSK theory is also shown for comparison.

Figure 5.1-2 shows the performance of the HRD system operating with uncoded 8PSK modulation after modifications were made. Just as in the first curve, the actual performance of the HRD followed the theoretical curve well. There was a small degradation in performance due to the modifications made. This can be seen in the implementation loss of 1.2dB at 8dB Eb/No, which is .2dB higher than the unmodified performance.

This implementation loss will be used for each of the codec tests performed in the lab. It will be measured again during each stage of testing to give a true measure of the loss the codecs were faced with under the different circumstances.

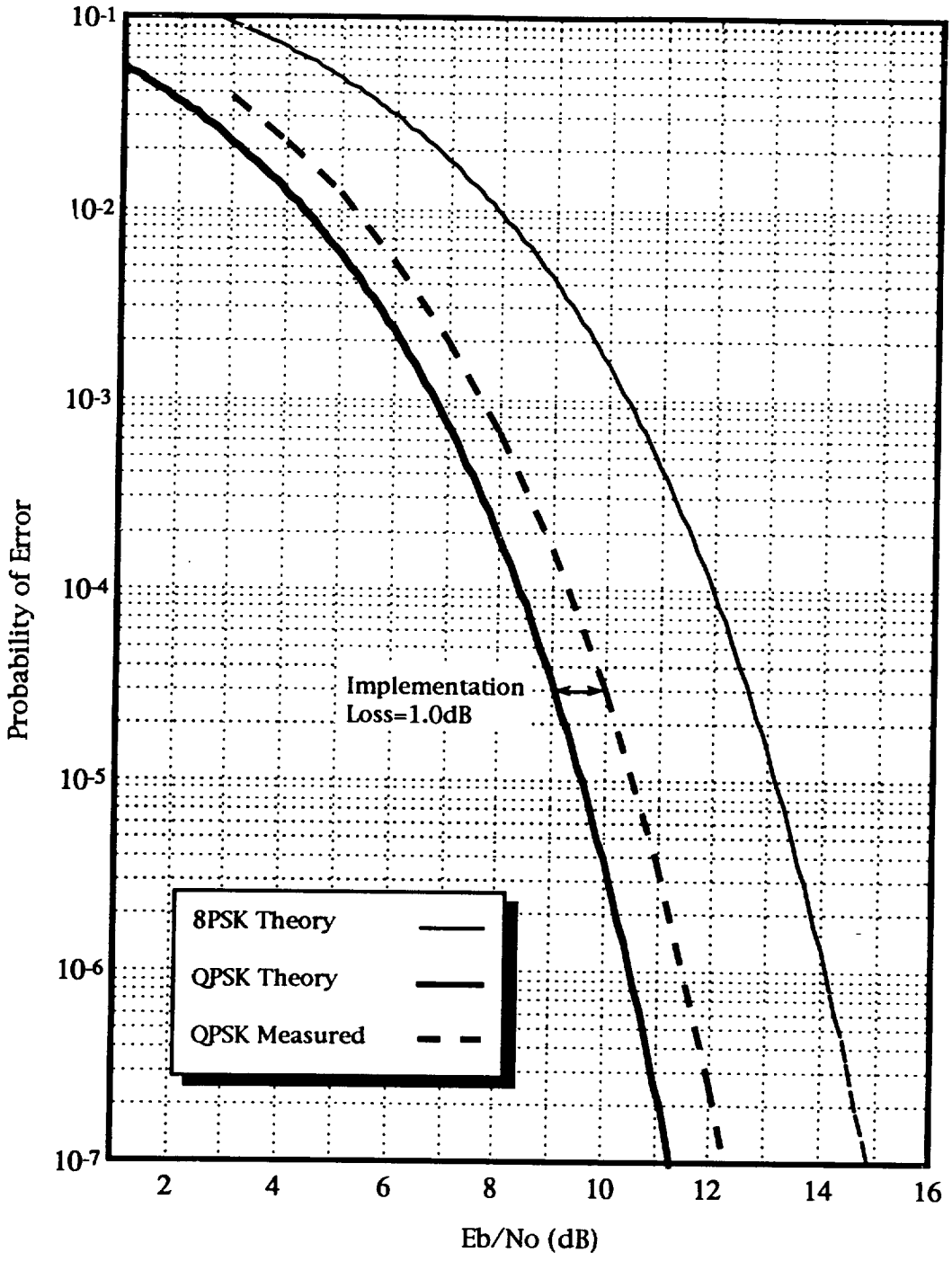


Figure 5.1-1 / Unmodified HRD QPSK Performance

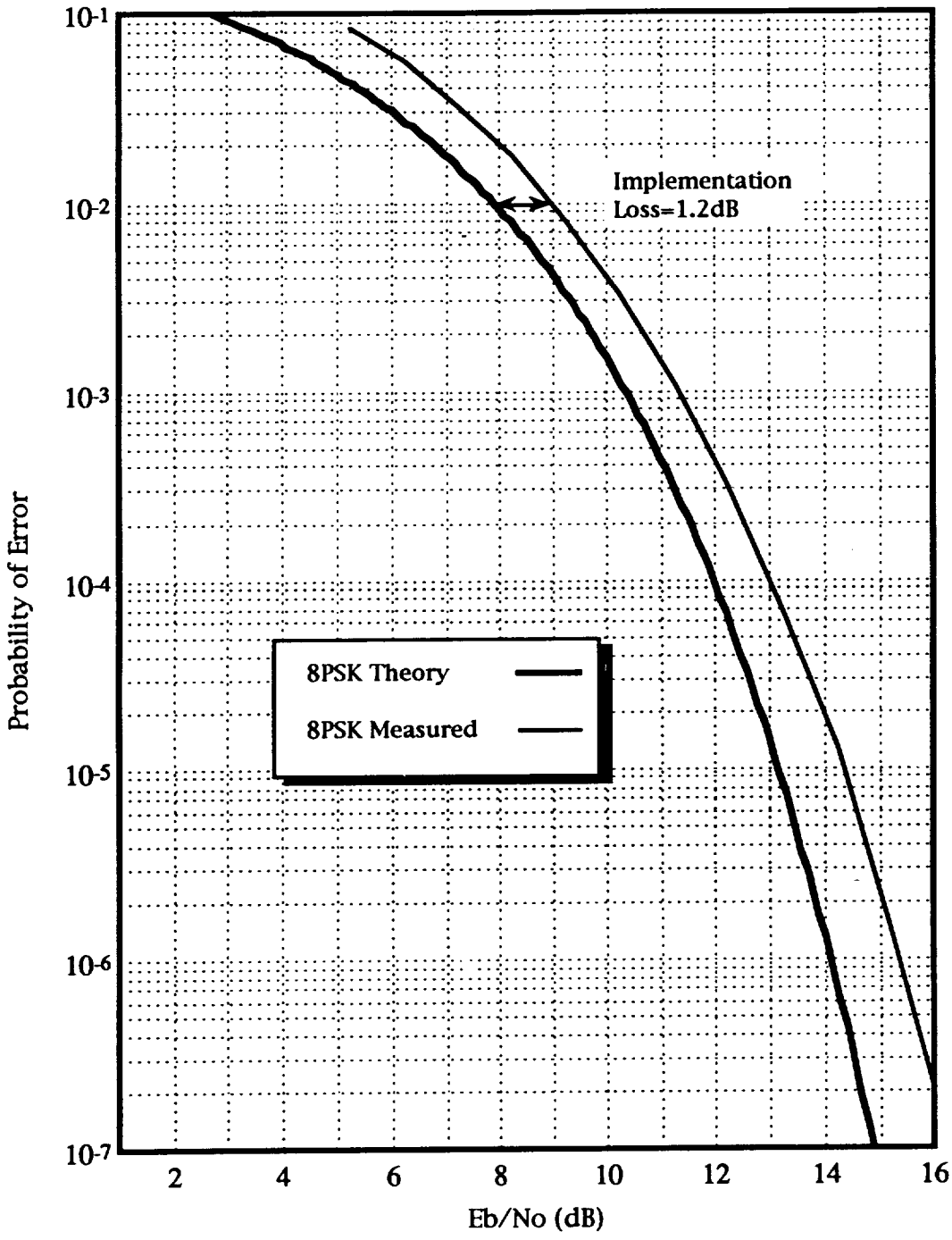


Figure 5.1-2 / Modified HRD 8PSK In-Lab Performance

5.1.2 NMSU Pragmatic Codec Testing

The results of the test performed with the NMSU codec while in the NMSU laboratory are shown below in Figure 5.1-3.

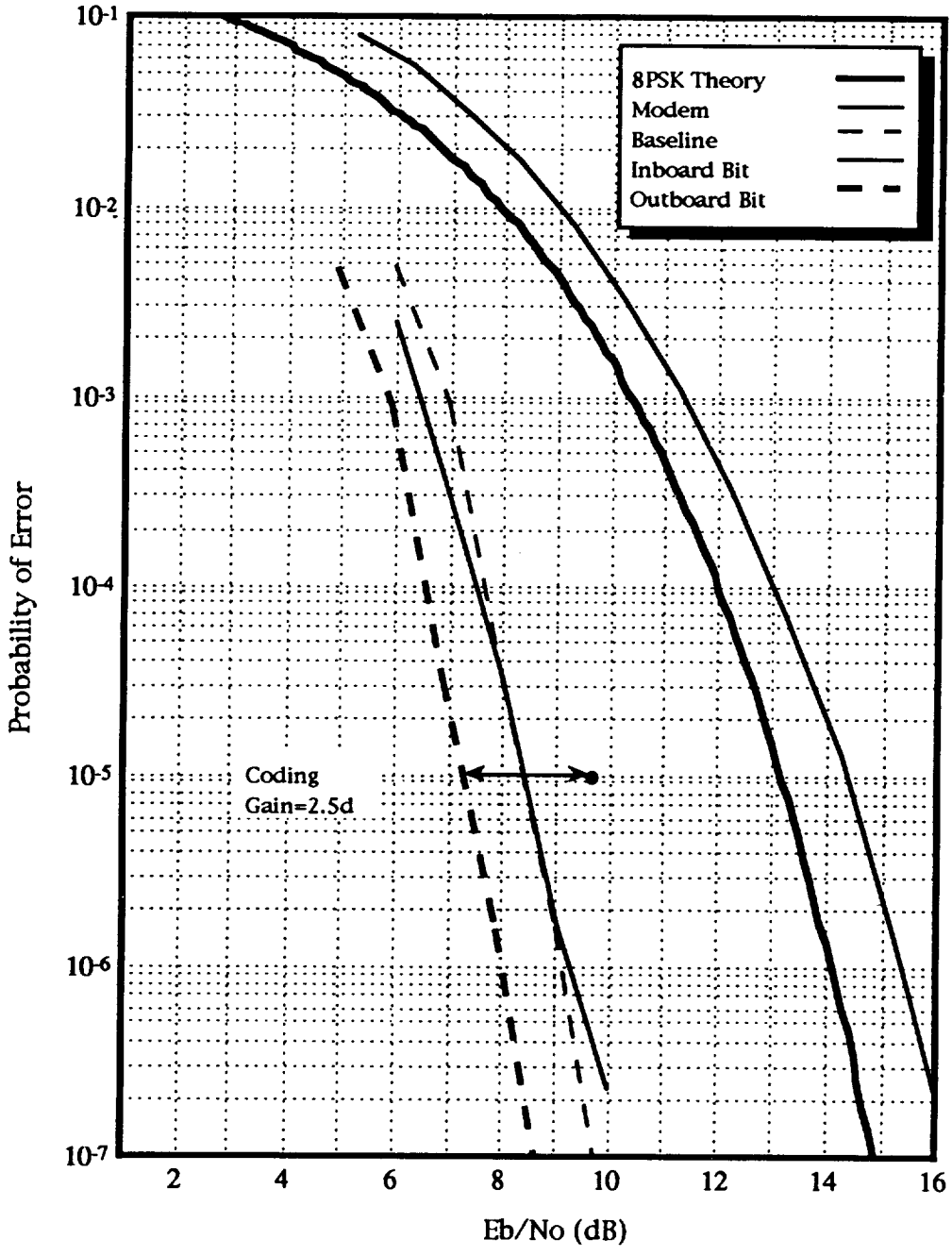


Figure 5.1-3 / NMSU Codec In-Lab Performance

The graph shown in Figure 5.1-3 presents five curves: 8PSK theory, the modem baseline, the performance of the codec's inboard channel, the performance of the codec's outboard channel and the inboard channel's performance corrected for implementation loss. The modem baseline is a copy of the data plotted in Figure 5.1-2, the measured performance of the modified HRD with 8PSK modulation.

Both the inboard and outboard channel BERs were measured during this test and their performance curves show no surprises. Note that at an error rate of 10^{-5}, the two channels are operating with the same Eb/No.

The corrected performance curve is the inboard curve shifted to take into account the implementation loss at 8.4dB Eb/No. This point was chosen because it is the level at which the inboard performance curve crossed 10^{-5}, the point at which coding gain was measured.

The coding gain is also shown on the curve. It is measured between the point marking QPSK's theoretical performance at an error rate of 10^{-5} and the point at which the corrected curve crossed 10^{-5}. This resulted in a measured coding gain of 2.5dB compared to QPSK.

5.1.3 UND/USA Rate 5/6 8PSK Codec Testing

The UND/USA codec was evaluated both by its designer in Australia and by the research team at NMSU. This section will compare the results taken at NMSU to those taken in Australia, after showing the coding gain measured in the NMSU laboratory.

The coding gain was measured by plotting (see Figure 5.1-4) the performance of the codec along with the performance of the uncoded system along with 8PSK theory. Four curves are shown in Figure 5.1-4, 8PSK theory, 8PSK measured, — the uncoded performance measured in the lab —- the codec's performance measured by the NMSU research team and the corrected performance, which takes into account the implementation loss. The implementation loss was measured at about 8.8dB Eb/No, the point at which coding gain was measured. The coding gain was again referenced to QPSK's theoretical performance of 10^{-5} BER at 9.6dB Eb/No, marked on the plot. This indicated a coding gain of 1.8dB, which is very close to theory for this codec design.

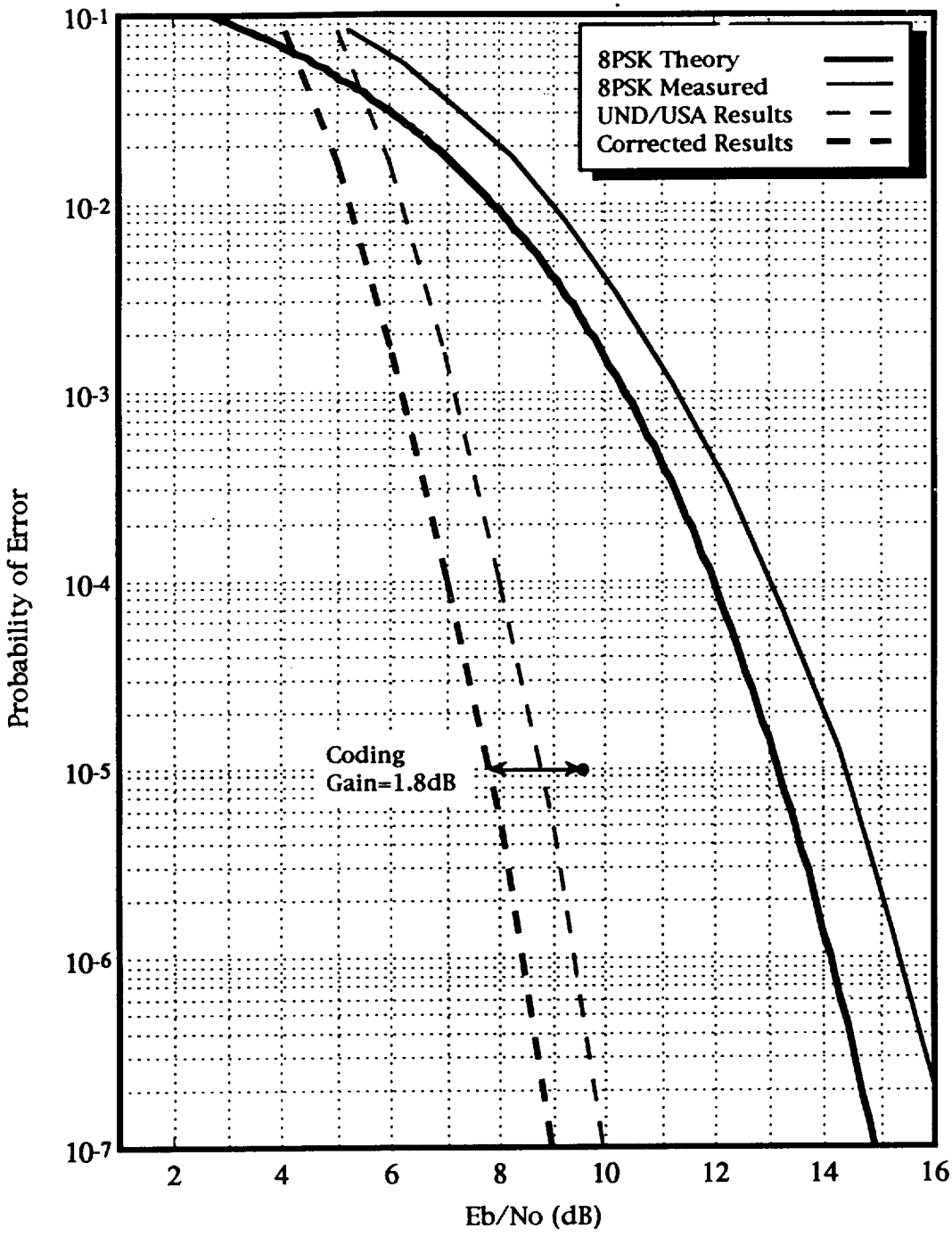


Figure 5.1-4 / UND/USA Codec Coding Gain

The results gathered in Australia are presented below in Figure 5.1-5. The theoretical performance of the ideal codec with infinite quantization and the measured performance for seven and five (as in our system) bits of quantization are shown.

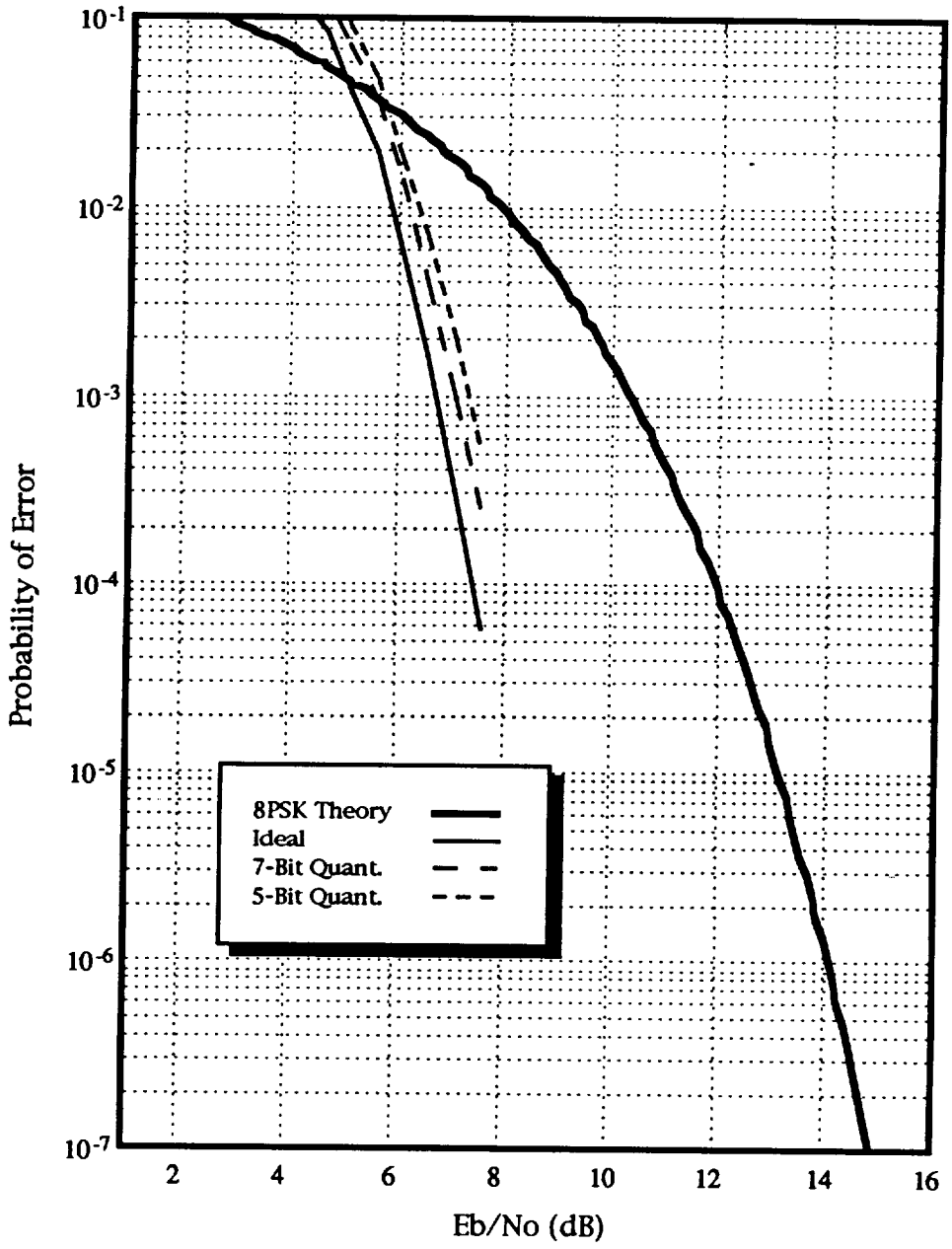


Figure 5.1-5 / UND/USA Codec Australian Results

Figure 5.1-6 demonstrates how well the results recorded in the separate labs compared.

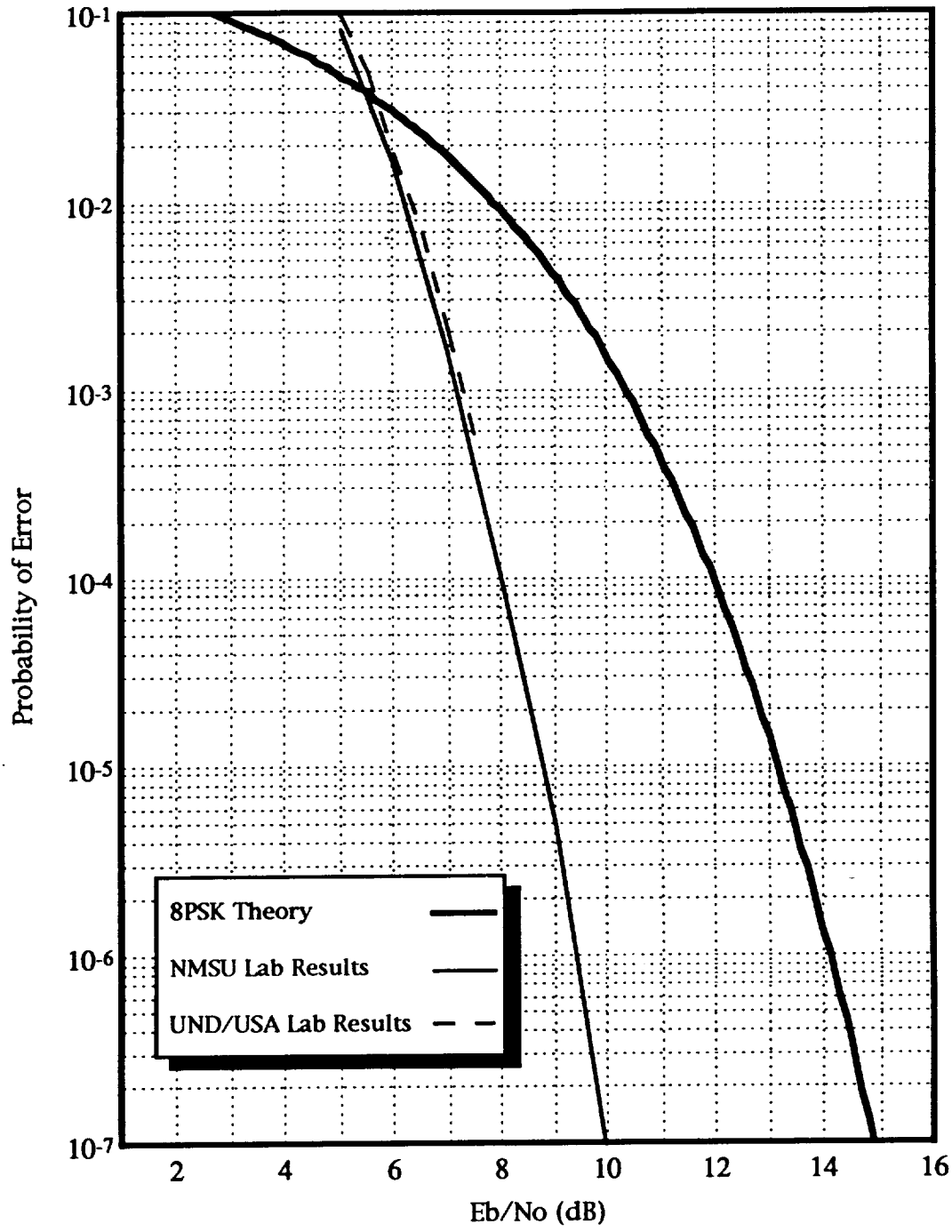


Figure 5.1-6 / UND/USA Codec Lab Results

5.2 On-Site Performance

A complete set of tests was performed once the system had been moved from NMSU to WSGT. This was done to ensure that the equipment was not damaged during the trip. This section will present the data collected during these tests.

5.2.1 Uncoded 8PSK Testing

Figure 5.2-1 compares the uncoded performance during the on-site tests to the lab results. Three curves are presented on the graph. 8PSK theoretical performance is shown with the on-site results and the results recorded before the equipment was moved. The small difference present is due to measurement accuracy.

This data showed that the modem was not damaged during the move.

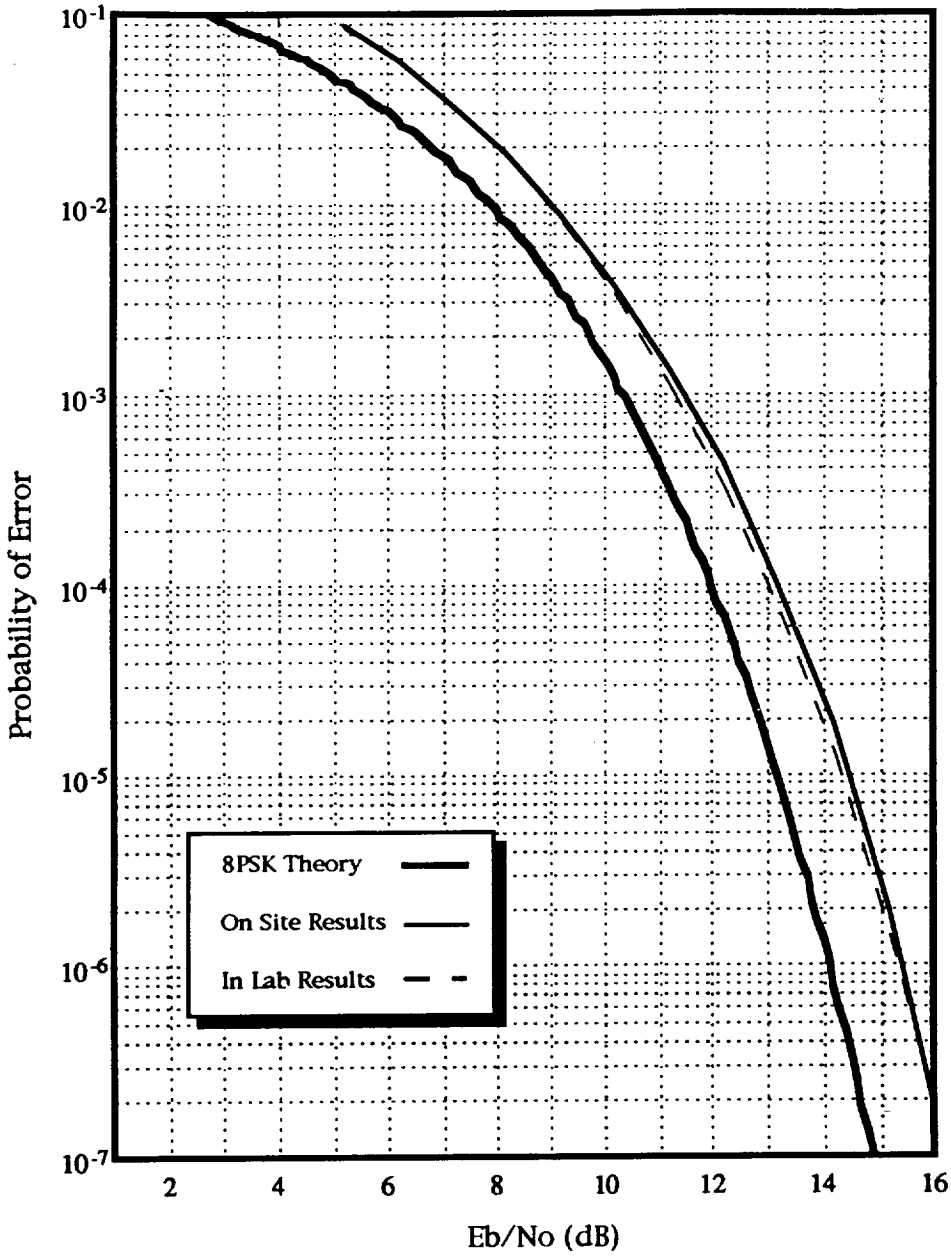


Figure 5.2-1 / Uncoded Results On-Site

5.2.2 NMSU Pragmatic Codec Performance

Once it was ascertained that the modem was operating as expected, the NMSU codec was tested. Figure 5.2-2 shows the results taken during this test.

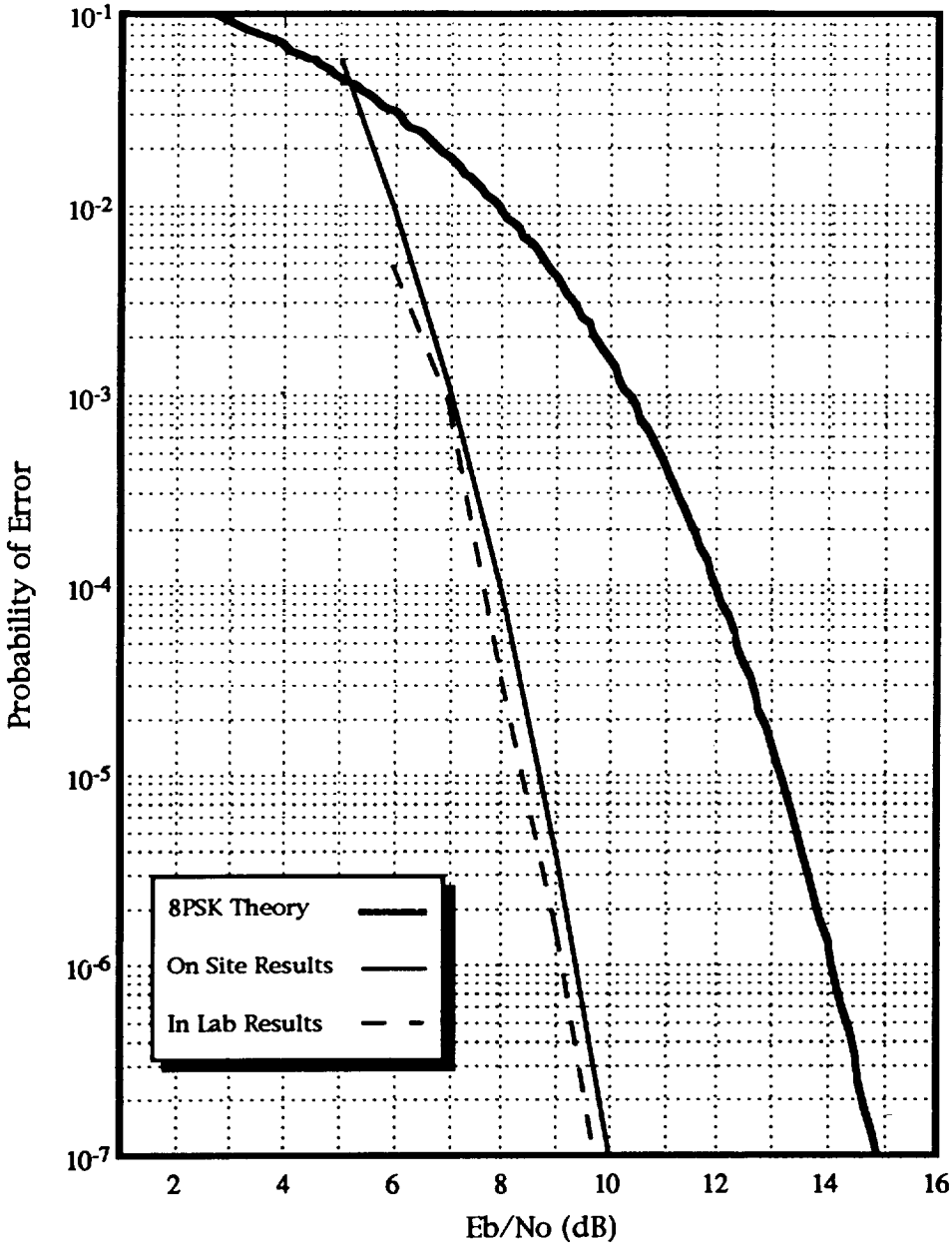


Figure 5.2-2 / NMSU Codec Performance On-Site

The graph above shows three curves: 8PSK theory, the codec's inboard channel performance measured at WSGT and the inboard performance measured at NMSU. The outboard data has been omitted for clarity. These curves show a slight degradation in the codec's performance. This was due to

different phase alignments, not to problems with the codec or modem. The difference is within about .2dB and was of no significant concern.

5.2.3 UND/USA Rate 5/6 8PSK Codec Testing

The UND/USA codec was unavailable during this stage of testing. Results taken during later stages will be compared to the in-lab results.

5.3 Inter Facility Loopback Performance

Before the system was tested through the TDRSS channel, it was demonstrated that the test system was compatible with the WSGT network. This was done by completing a set of tests through WSGT's inter facility loopback (IFL) system. The IFL system is used to simulate the satellite channel for testing and maintenance purposes. By running a complete test through the system, the test system was proved to be compatible with the WSGT equipment.

Testing through the IFL system also gave the NMSU research team a chance to better understand the system's performance through the actual channel. The simulator in the IFL was a much better approximation of the channel than was present in loopback systems.

The level of the signal returned to the test system by the IFL system was set at approximately 90dB C/kT. This was required to allow the HRD to track and demodulate the received data signal as discussed in Section 3.3. This section will discuss the results gathered during this stage of testing.

5.3.1 Uncoded 8PSK Testing

The first test performed through the IFL system consisted of developing an uncoded baseline to compare the codec test to. Figure 5.3-1 shows the results of this test. This curve shows 8PSK theory along with both the IFL and on-site performance curves.

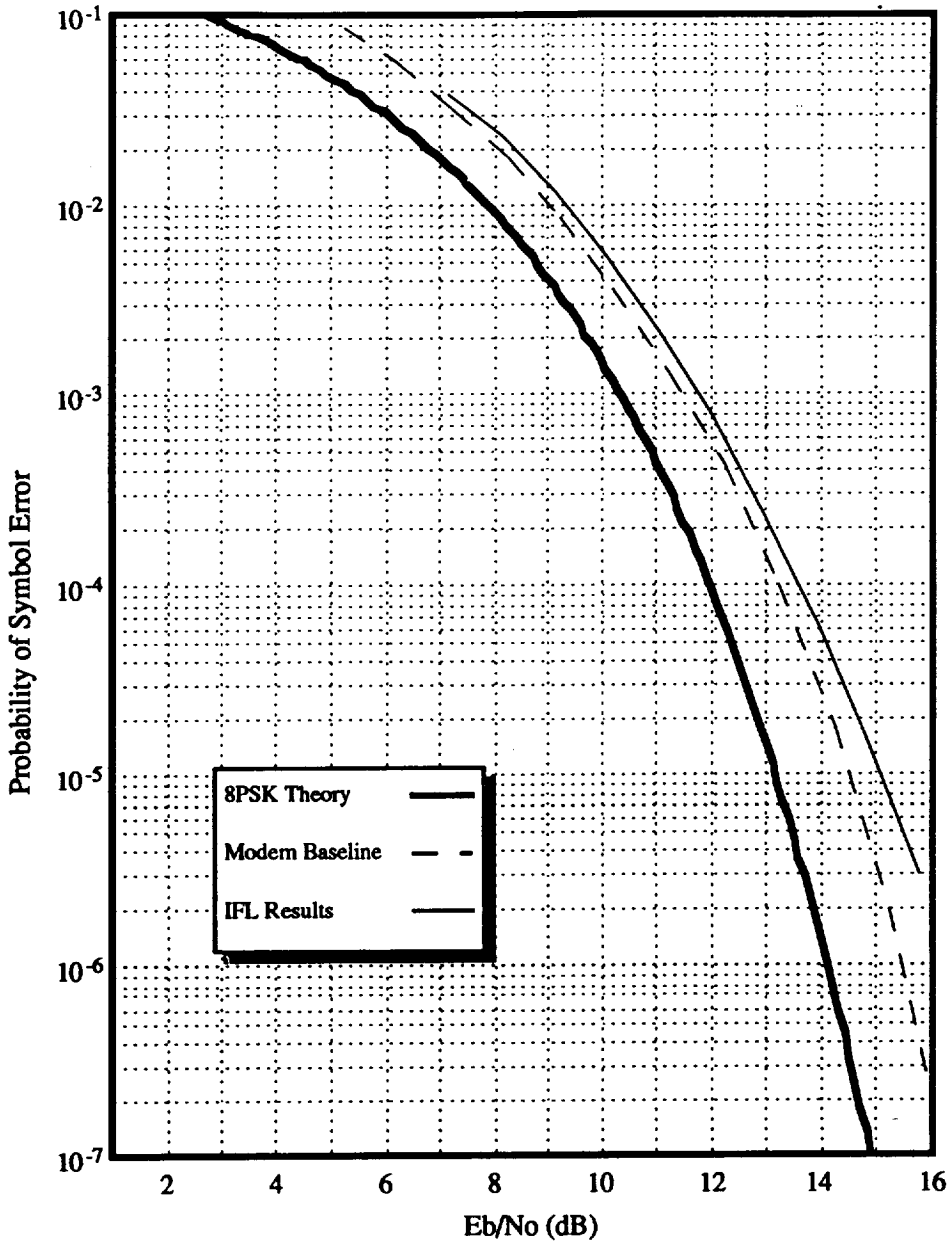


Figure 5.3-1 / Uncoded 8PSK Results Through IFL System

This graph shows a small amount of flare in the IFL performance curve at high levels of Eb/No. It was determined that this was due to phase jitter, visible on the Vector Analyzer, not present in the loopback tests. To confirm this decision, the effects of phase jitter were investigated. Figure 5.3-2 demonstrates the theoretical effect of phase jitter on 8PSK modulation. Curves

are shown for 0°, 1.5°, and 3° of phase jitter. This indicated that phase jitter of about 2° would produce the flare measured over the IFL system. This agreed with the amount of jitter seen on the Vector Analyzer.

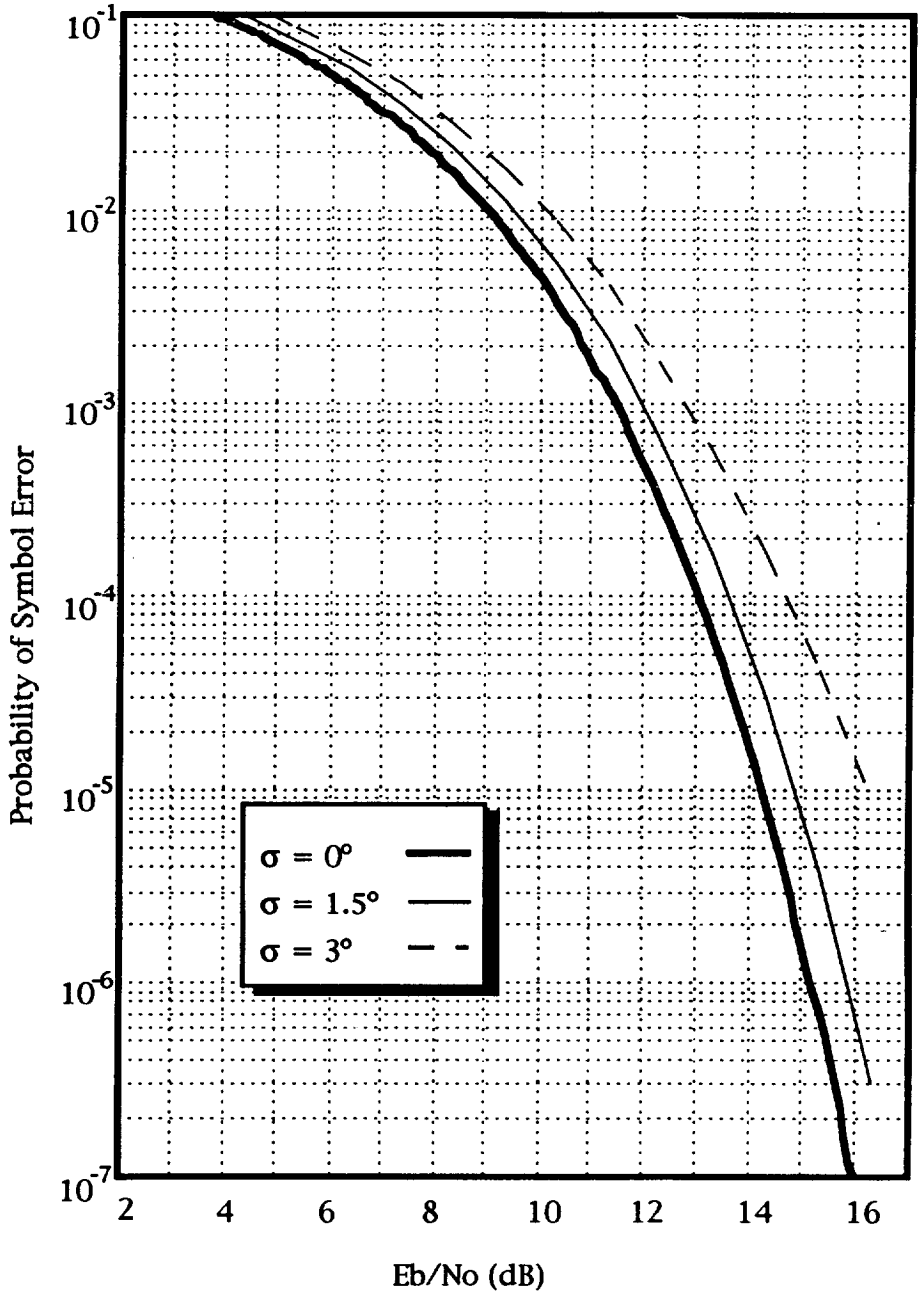


Figure 5.3-2 / Effects of Phase Jitter on 8PSK Modulation

5.3.2 NMSU Pragmatic Codec Testing

Once a baseline was established for the IFL system, the NMSU codec's inboard and outboard channel were tested through the channel. The resulting curves were compared with the uncoded baseline to measure the coding gain of the codec. Figure 5.3-3 shows the performance curves, the uncoded baseline and 8PSK theory, along with the measured coding gain.

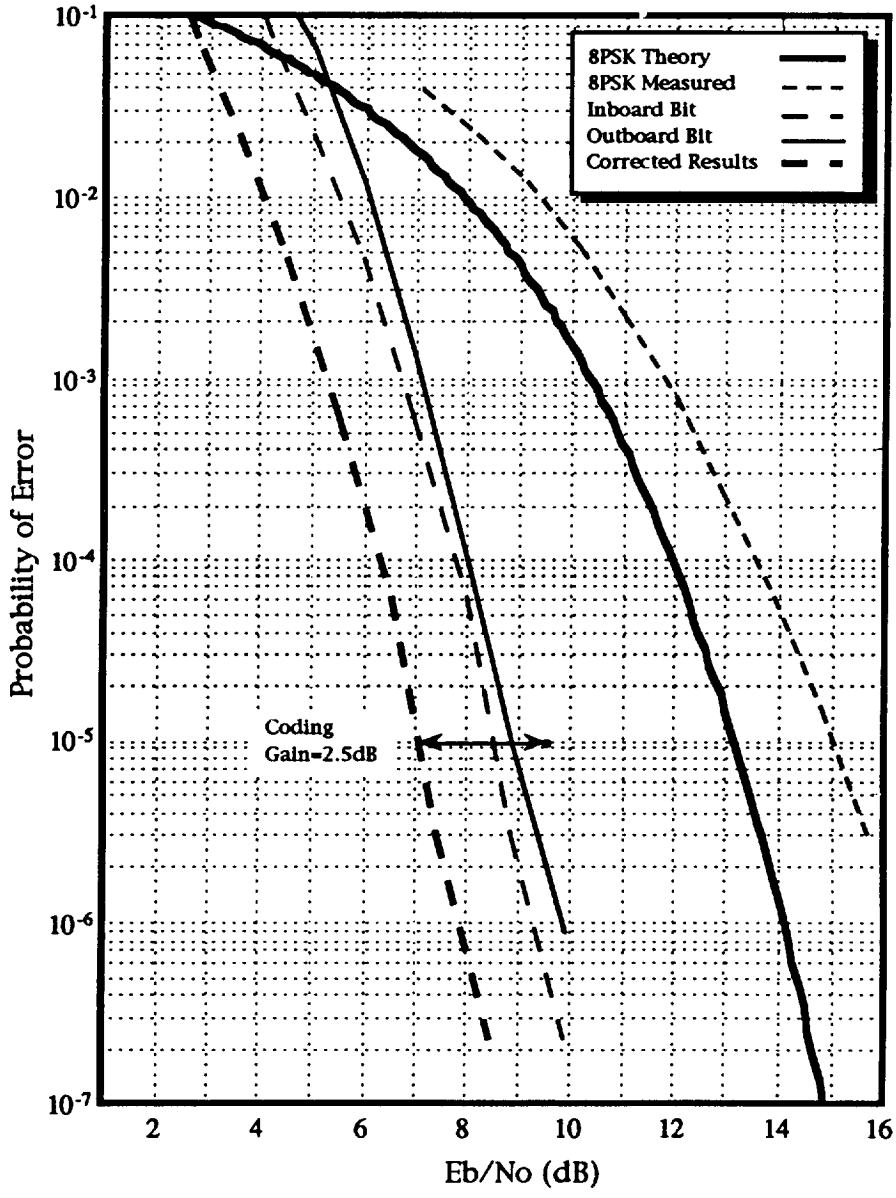


Figure 5.3-3 / NMSU Codec Performance through IFL System

The coding gain was measured in the same manner as in previous tests. The implementation loss was measured at 8.8dB Eb/No, which corresponds to an uncorrected BER of 1×10^{-5}. The inboard channel's performance curve was shifted to account for this implementation loss. The coding gain was then measured relative to QPSK's performance of 1×10^{-5} BER at 9.6dB Eb/No. This indicates a coding gain of 2.5dB relative to QPSK at this point. This measurement agrees with the one made during the testing of this codec while at NMSU.

Next, the performance of the inboard channel through the IFL system was compared to the inboard performance measured during the on-site test. The two performance curves are plotted, along with 8PSK theory, in Figure 5.3-4. This demonstrated that the phase jitter encountered in the IFL channel had little or no effect on the performance of the codec. This was verified by again looking at the graph in Figure 5.3-2. This graph shows that although phase jitter has a significant effect in the performance of 8PSK at high levels of Eb/No, its effect is minimal when encapsulated in noise – low Es/No. Therefore, in the region of Es/No that the codecs operate in is not significantly affected by the phase jitter in the IFL system.

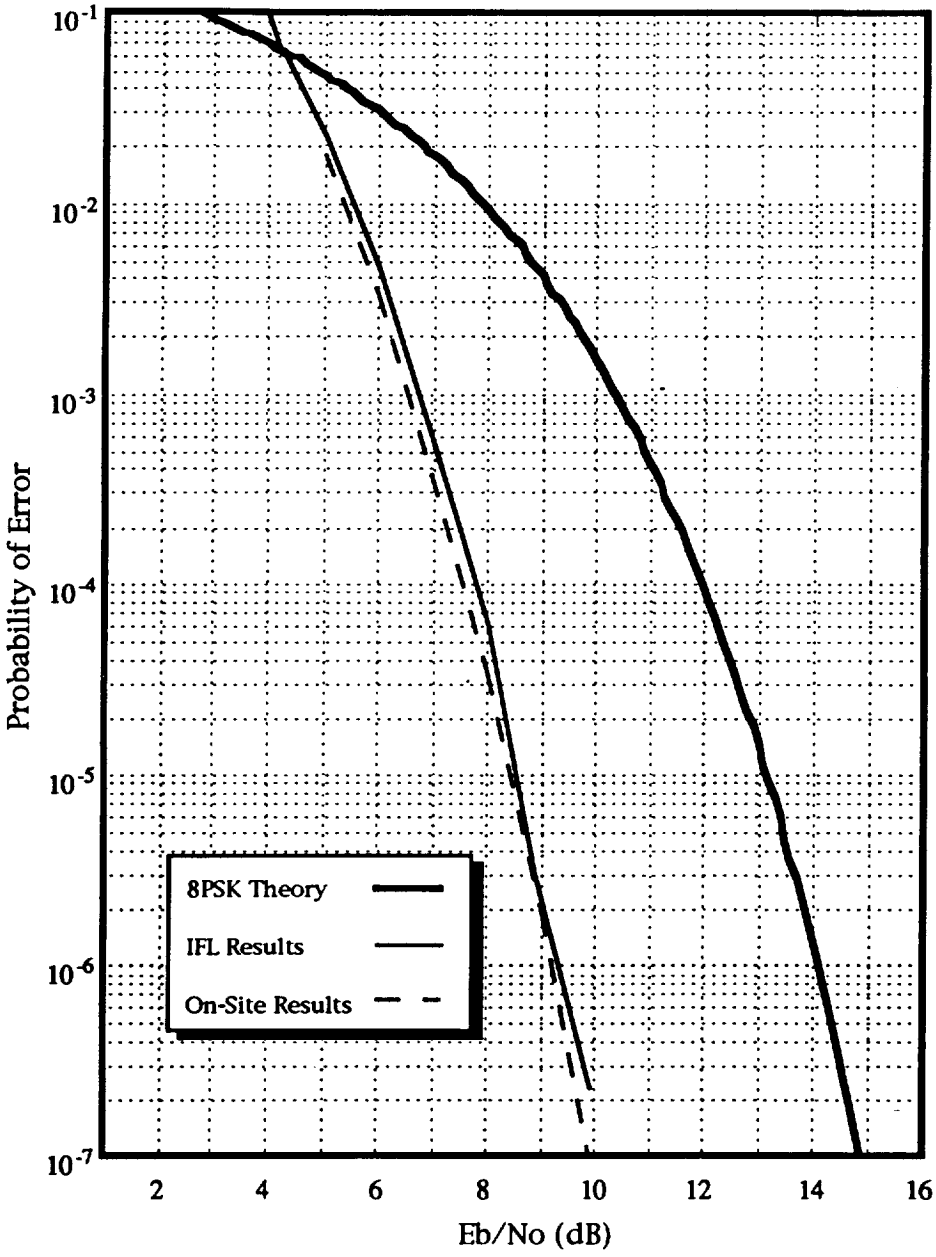


Figure 5.3-4 / NMSU Channel Performance Comparison

5.3.3 UND/USA Rate 5/6 8PSK Codec Testing

Once again, the UND/USA codec was unavailable for this stage of testing. The performance of the NMSU codec through the IFL system indicates that there should have been no change in the UND/USA codec's performance.

5.4 TDRSS Channel Performance

The final test performed involved the actual TDRSS channel. This was the final test to measure the performance of the two codecs, as well as the uncoded system, over the actual satellite channel.

All tests were performed with a high C/kT from the satellite. The signal's high level allowed the HRD to track and demodulate the received signal. This also allowed the level of noise to be varied by the test system operators, freeing the WSGT operators to continue with other tasks. This section will discuss the results of the tests performed through the channel.

5.4.1 Uncoded 8PSK Testing

In order to correctly evaluate the performance of the codecs over the TDRSS channel, an uncoded baseline was established. The test was performed on August 14, 1992 at 18:15 Zulu over the TDRS SA2 SSAR satellite link. The received C/kT level was set at 86.2dB at the input to the test system.

Figure 5.4-1 shows the results of the test performed. This graph includes 8PSK theory, the modem's performance through the satellite channel and the modem's performance through the IFL system. The similarity between the curve demonstrates that the IFL system was a very good simulator for the actual channel. In fact, this satellite channel had a high level of Doppler present, which had no effect on the test results.

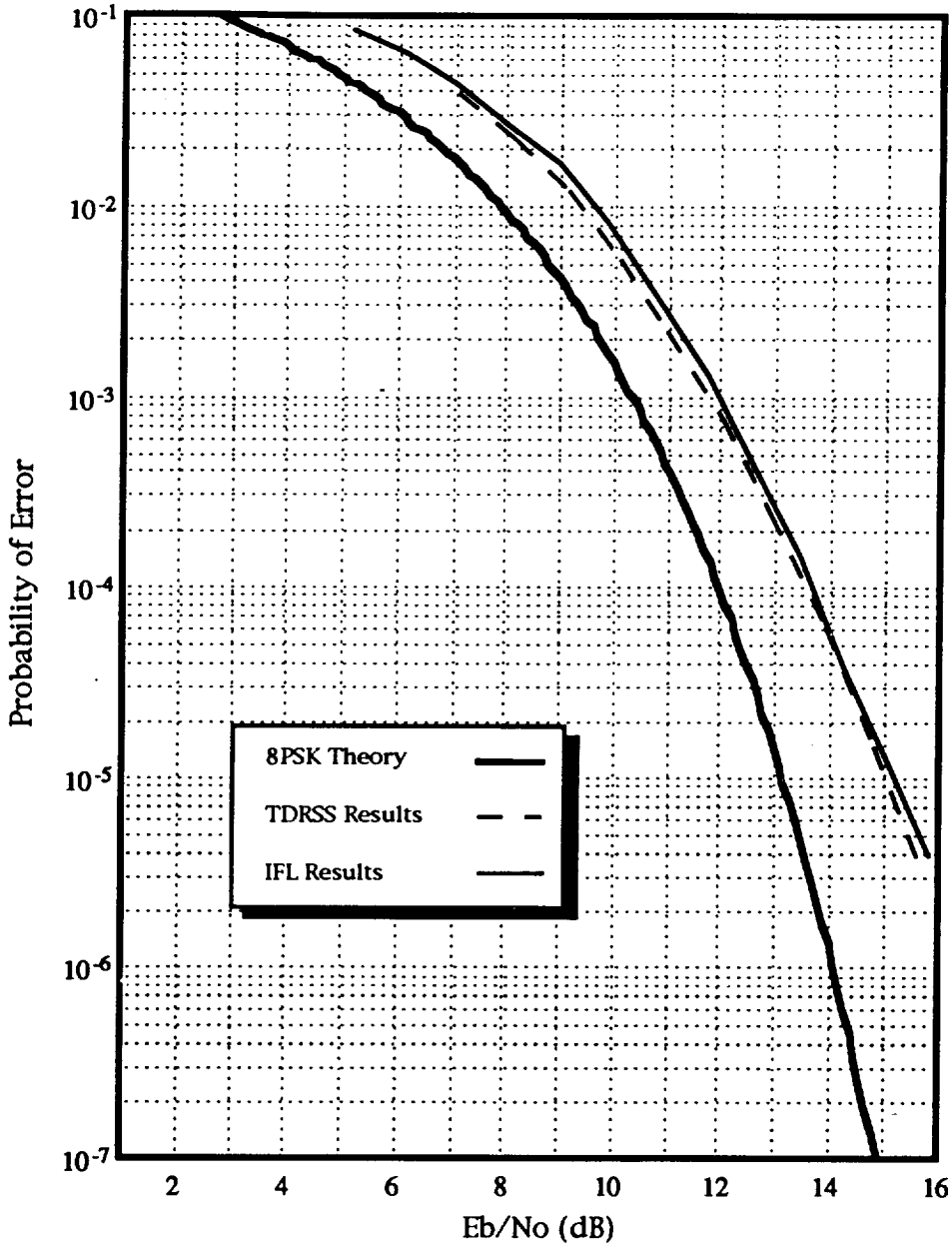


Figure 5.4-1 Uncoded 8PSK Performance Through TDRSS

5.4.2 NMSU Pragmatic Codec Testing

With the uncoded 8PSK baseline information to look at, the NMSU codec was tested over the TDRSS channel. This test was performed on September 3, 1992 at 15:15 Zulu over the TDRSS SatD SA1 satellite link. The received signal level was set at 86.3dB C/kT at the input to the test system.

The graph shown in Figure 5.4-2 includes the 8PSK theoretical curve, the modem's 8PSK measured performance through TDRSS and both the uncorrected and corrected curves for the codec's inboard channel. To conserve time on the satellite, the outboard channel was not tested.

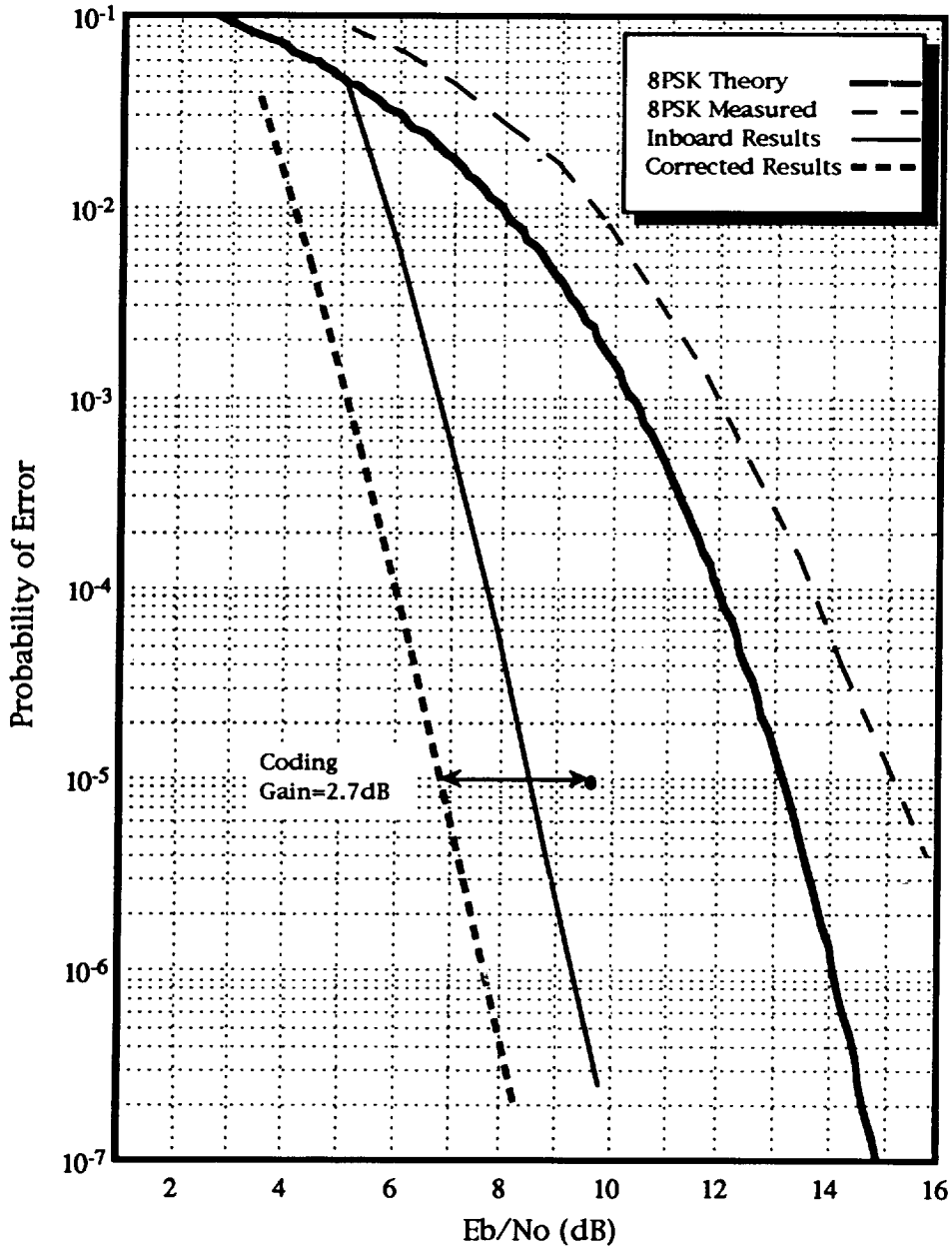


Figure 5.4-2 / NMSU Codec Performance Through TDRSS

The coding gain of the NMSU codec was measured, in the same manner as in previous tests, to be 2.7dB at 1×10^{-5} BER. This gain is only slightly better than previously measured.

The effects of the satellite channel on the codec as compared to the IFL system were investigated by plotting the inboard channel's performance curve from each test on the same graph. This is shown below in Figure 5.4-3.

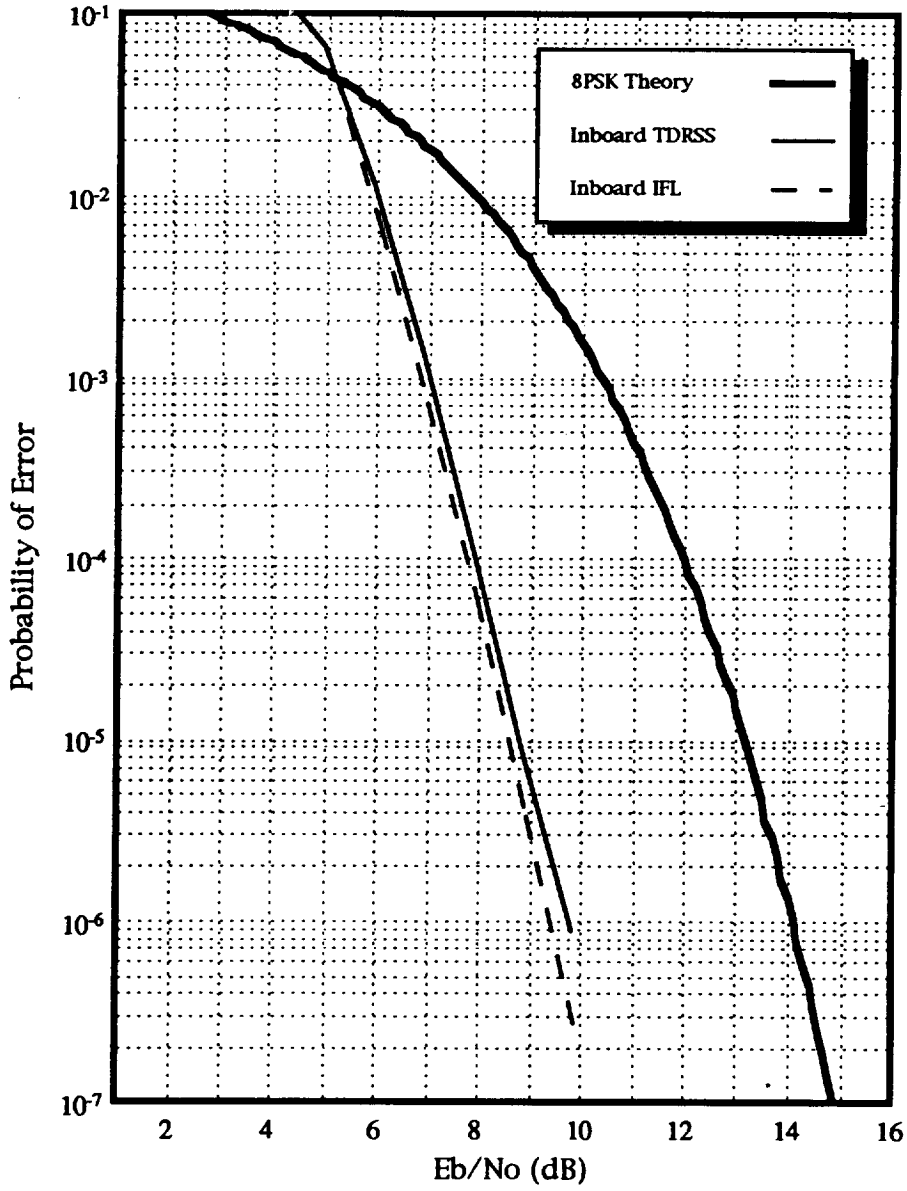


Figure 5.4-3 / NMSU Codec's Inboard Performance Comparison

The similarity between these curves shows that the IFL system was good in its approximation of the TDRSS channel. No unexpected effects due to the satellite channel were present.

5.4.3 UND/USA Rate 5/6 8PSK Codec Test

The final test performed involved the UND/USA codec through the TDRSS channel. Although it had been unavailable for testing during both the on-site and IFL system testing, it was returned to the NMSU research team in time to test it through the satellite. Therefore, all the results are compared to those taken in the first stage of testing. This test was performed on August 24, 1992 at 16:15 Zulu over the TDRSS SatA SA2 channel. The input level to the test system was set at 86.3dB C/kT.

Figure 5.4-4 shows the codec's performance over the satellite channel. The coding gain was measured to be 2.1dB as compared to uncoded QPSK at a BER of 1×10^{-5}. Again, this is slightly higher than that measured in the lab. This difference was contributed to phase alignment and measurement accuracy. Overall, it will be said that the codec performs with approximately 2dB of coding gain with respect to uncoded QPSK, as predicted by theory.

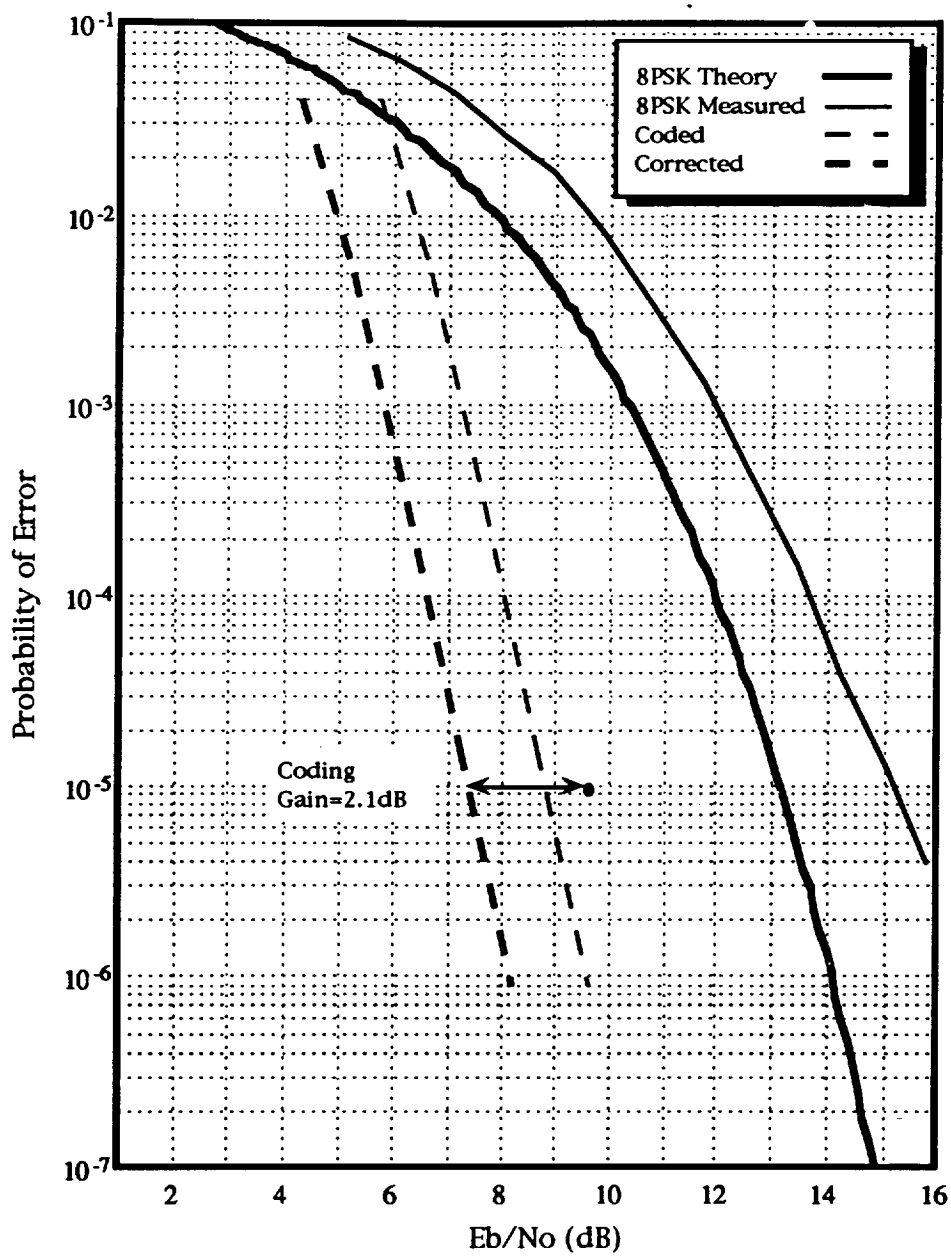


Figure 5.4-4 / UND/USA Codec Performance through TDRSS

The codec's performance through TDRSS was compared to that measured at NMSU. This comparison is shown in Figure 5.4-5. The graph shows a strong agreement between the two performance curves. Therefore, the TDRSS channel had very little effect on the performance of this codec.

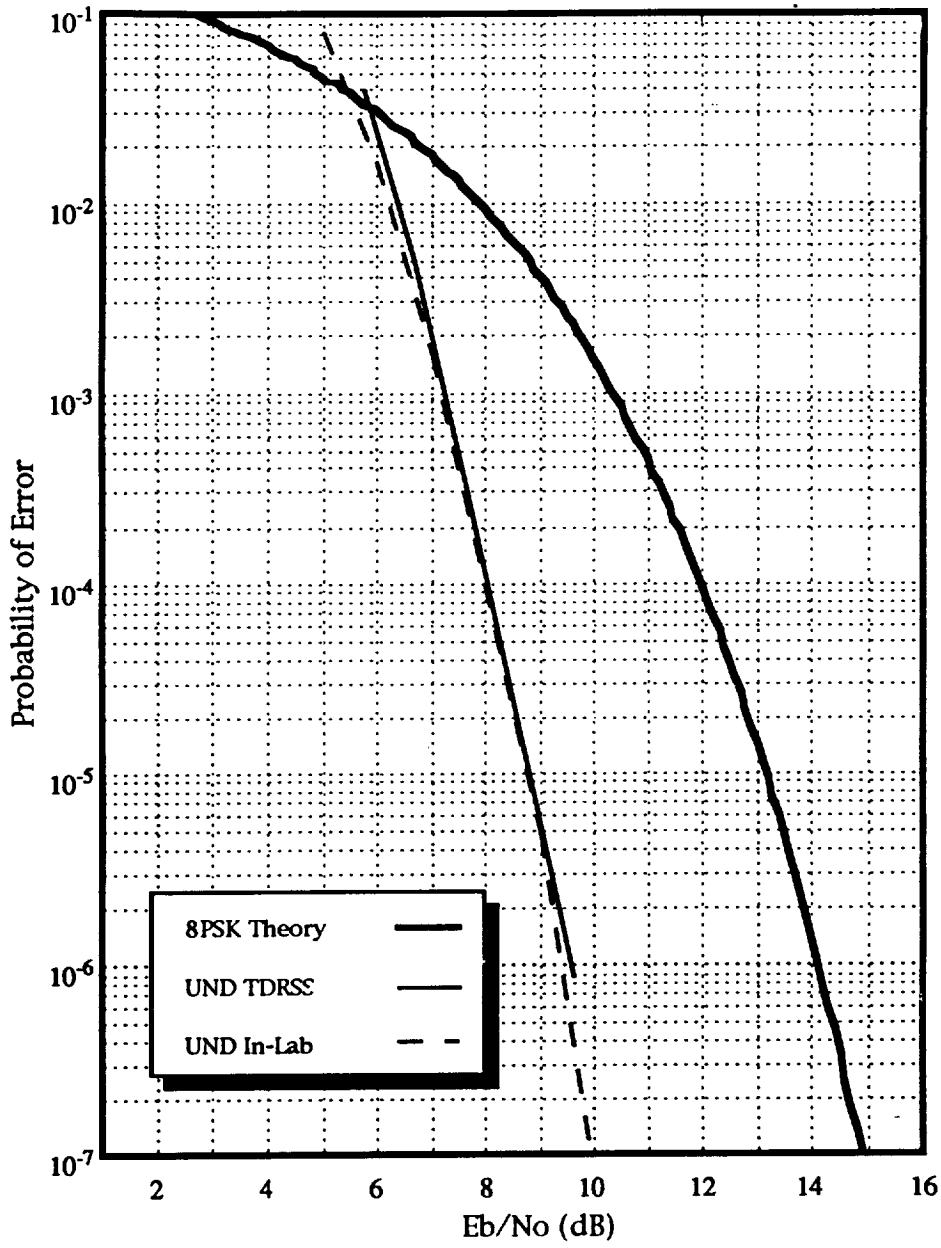


Figure 5.4-5 / UND/USA Codec Performance Comparison

6. Summary

Through its research in conjunction with NASA, New Mexico State University's Center for Space Telemetering and Telecommunications believes it has found a strong candidate for a modulation scheme to be used for high data rate applications through the TDRSS channel in the near future. The test of 8PSK TCM through the satellite system, under NASA grant NAG 5-1491, proved to be a complete success.

The test performed at WSGT by NMSU demonstrated that 8PSK with trellis coding is a modulation scheme that will increase the data rate capabilities through the TDRSS spacecraft while still achieving better bit-error-rate versus signal-to-noise-ratio performance than uncoded QPSK. This will help with the high demands expected to be put on the TDRSS network by programs such as Space Station Freedom and a manned mission to Mars.

Two TCM codecs, implementing different levels of bandwidth efficiency, were tested and proved to be unaffected by the TDRSS channel. The codec designed and built by NMSU achieved a coding gain of 2.7dB with respect to uncoded QPSK while increasing the data rate per unit of occupied bandwidth by a factor of 2. The second codec, built by the University of Notre Dame with the University of South Australia, demonstrated a coding gain of 2dB over QPSK with a 2.5-to-1 increase in data rate per unit bandwidth.This applied to both SSA service and KSA service.

It was also shown that existing hardware such as WSGT's High Rate Demodulator could be modified to operate with 8PSK modulation. But in the future, the research team at NMSU does not recommend this approach. After encountering a great deal of trouble with the HRD modifications, it was decided that construction of a device to demodulate a range of M-ary PSK formats, including QPSK, 8PSK and 16PSK, would be worth the effort involved. Today's technology would make the construction of such a demodulator far easier than modification of existing demodulators.

The modulation technique was not fully tested though. Further tests performed at rates higher than 1Msps are required to stress the channel. SSA service should be tested at 6 or 12Msps, while KSA service should be tested with data rated in the 300 to 600Mbps range. Tests must also be performed to investigate the effects of RFI and burst errors on the performance of TCM.

Overall, the proof-of-concept test was deemed a success. It was shown that the 8PSK TCM system built operated in the TDRSS channel with the same coding gains achieved in the laboratory — the TDRSS channel did not degrade the TCM format in any unusual way. And, the researchers at NMSU are confidant that this modulation scheme will pass all future tests and can safely be selected as one of the modulation schemes for future high rate TDRSS applications.

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