TWO- AND THREE-DIMENSIONAL HIGH PERFORMANCE, PATTERNED OVERLAY MULTI-CHIP MODULE TECHNOLOGY

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ABSTRACT

A two- and three-dimensional multi-chip module technology has been developed in response to the continuum in demand for increased performance in electronic systems, as well as the desire to reduce the size, weight, and power of space systems. Though developed to satisfy the needs of military programs, such as the Strategic Defense Initiative Organization, the technology, referred to as High Density Interconnect, can also be advantageously exploited for a wide variety of commercial applications, ranging from computer workstations to instrumentation and microwave telecommunications. The robustness of the technology, as well as its high performance, make this generality in application possible. More encouraging is the possibility of this technology for achieving low cost through high volume usage.

INTRODUCTION

Size, weight, power. To a space system, they represent cost and complication. Reducing them, at least as far as the electronic subsystems are concerned, became the central focus of the Phillips Laboratory (PL) Wafer Scale Integration (WSI) program, sponsored largely by the Strategic Defense Initiative Organization (SDIO). At the same time, the Defense Advanced Research Preparedness Agency (DARPA) recognized the tremendous potential of such a technology to improve the performance of electronics systems, military and commercial. When DARPA and PL initiated programs in the mid-1980's to explore these new possibilities, they participated in developing a new approach within an emerging class of technologies called *multi-chip modules* (MCMs), which themselves are a part of a broader class of technologies known as *wafer scale integration* (WSI) technologies. The MCM technology discussed in this paper, known as *High Density Interconnect* (HDI), developed by complementary support from DARPA and PL with the General Electric company, is a novel technique for re-assembling bare integrated circuits in a manner that dramatically improves size, weight, and performance [1]. Perhaps more novel is the potential of this technology to address an exceptionally large class of applications: military and civilian, space and terrestrial, strategic and commercial.

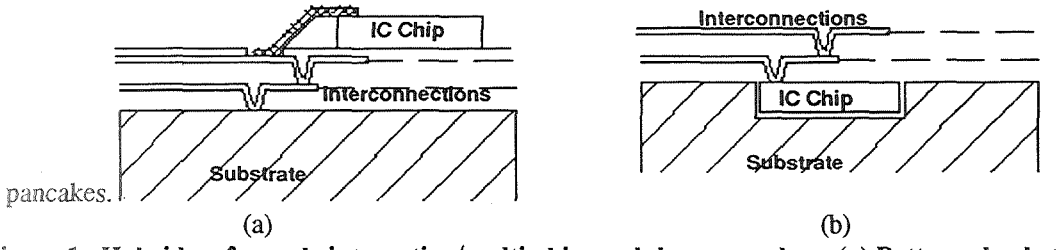
BACKGROUND

Traditionally, an integrated circuit (IC) chip is placed in a single chip package (SCP) to protect it from mechanical damage and to provide electrical access to its tiny electric terminals. The problem associated with conventional electronics assembly methods based around the SCP is that they exact significant penalties upon the size, weight, power, performance, and reliability of an electronics system. Furthermore, the reliability of a system built in a manner is also non-optimal, due to extraneous materials and structural interfaces, each representing an additional failure opportunity and thermal barrier. Finally, SCPs limit the electrical design complexity that is projected for systems near and beyond the year 2000. It is suggested that for these systems, many hundreds if not thousands of signals will emanate from the terminals of individuals IC chips [2].

Phillips Laboratory, in the mid-1980's, launched the Wafer Scale Integration (WSI) program in search of better packaging approaches. Here, a special emphasis was placed on technologies that were suitable for

space strategic missions. Some of the missions envisioned for the SDIO were based on capabilities that were prototyped with large brassboards. For these missions to be practical, the same functionality demonstrated in the brassboards, sometimes one or more racks full of electronics, had to be compressed into compartments that were measured in cubic centimeters rather than cubic feet.

MCM approaches can be delineated into patterned-substrate and patterned overlay approaches (Figure 2). In the *patterned-substrate* approach (Figure 2a), the interconnections between components are formed *a priori*, like a micro-printed circuit board. In the *patterned overlay* approach (Figure 2b), the approach used for the HDI process, the interconnections are not formed until all components are placed within the substrate.



pancakes.

Figure 1. Hybrid wafer scale integration/multi-chip module approaches. (a) Patterned substrate. (b) Patterned overlay.

THE HIGH DENSITY INTERCONNECT (HDI) PROCESS

A simplified version of the sequence used to create HDI modules is depicted in Figure 2. Construction of an HDI module starts with a blank piece of substrate material of suitable flatness and quality. The substrate is processed first by forming wells or recesses into which the components are placed. Different component thicknesses are accommodated by recesses of different depths, formed in such a way as to yield an assembly that is essentially planar (within 0.0005 inches) after all components are placed. Components are mounted into the substrate with computer-controlled component placement equipment that uses the opposite corners of each component as alignment fiducials. Components are secured to the substrate with a special thermoplastic, chosen for its thermal conduction, thermal coefficient of expansion, and flow viscosity properties. Aluminum can be sputtered on areas of the substrate not already covered by components to facilitate the longer direct current interconnections (such as power and ground) and the terminals of the HDI modules.

Subsequent steps of the HDI processing sequence relate to the novelty of the formation of the so-called patterned overlay. This sequence begins with the lamination of Kapton dielectric to the entire substrate. Tiny opening holes or *vias* to the surface below the lamination are laser-formed and metallized to complete electrical connection to the ICs below. The metal system consists of sputtered titanium and copper, electroplated copper, and sputtered titanium. To pattern the metallization configuration, a sprayed photoresist layer is laser-exposed as required with an adaptive lithography system. The adaptive process is used to dynamically correct for the slight but inevitable errors that occur in component placement. Eventually, 2 to 4 additional layers of this dielectric-metal system are formed onto the HDI assembly, depending on the wiring capacity demands of a particular application [3].

Final packaging of HDI modules for military and space applications typically involves using a laser- or seam-welded kovar flat package to hermetically encapsulate the HDI substrate. These packages interface electrically to the HDI substrate through lead wires, which pass through insulating glass beads in the wall of the package. Simple wirebonds between the HDI substrate and the leads facilitate the electrical connections required. Other hermetic and non-hermetic packaging methods have been explored and remain an active area of research. These include: (1) the *integral package*, which uses the substrate itself as a final, hermetic package, eliminating *all* wire-bonds; (2) non-hermetic, direct attach techniques,

which interface inverted HDI modules directly to a PWB using an appropriate interposer (e.g., cinch connector, elastomeric, etc.); and (3) special high pin count package designs, extendible to three-dimensional HDI modules [4].

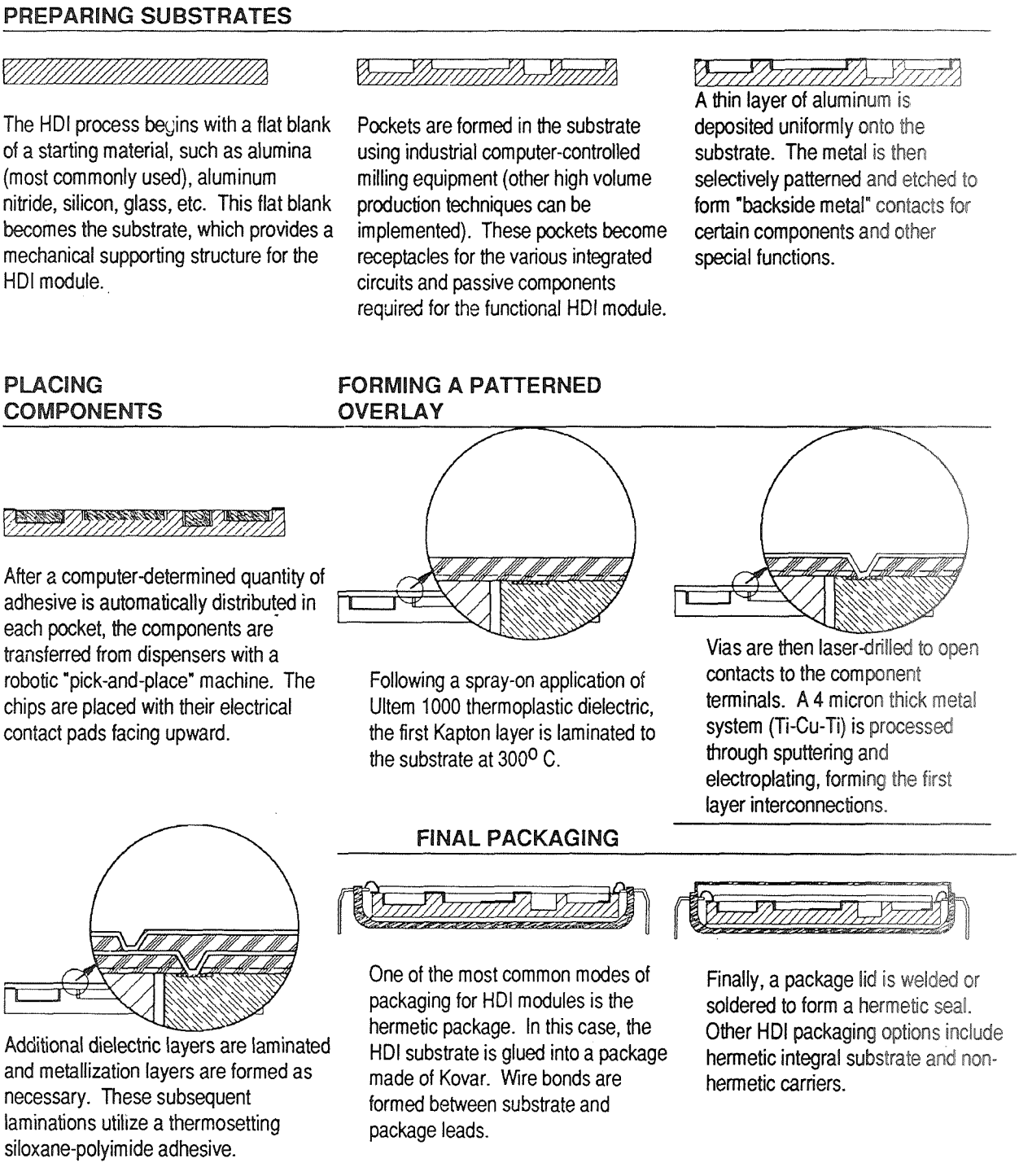


Figure 2. The two-dimensional HDI process.

Process Repair and Component Pre-Test

The ability to repair any MCM process is important for two reasons: (1) the value of the collection of components committed to an MCM is sometimes very significant, particularly for military applications; and (2) component yields are often too low to produce a first-pass functional MCM. Repair of the HDI process is routinely accomplished by removing the overlay, selectively removing and replacing bad components, and rebuilding the overlay. Recent tests have demonstrated as many as eleven consecutive repair cycles on individual HDI modules with no measurable differences in the physical or electrical performance characteristics of the components. Several "known good die" techniques can be employed with the HDI process to mitigate the need for module repair. One technique involves the burn-in on partially completed HDI assemblies. Unlike patterned substrate approaches, HDI allows interim testing to be performed after the metallization of each layer, if desired. A simpler technique for high volume production involves the use of a dedicated electronic membrane, built from HDI itself and configured to interface with all critical substrate components upon (temporary) contact to the substrate. Finally, a more elegant technique that mimics the conventional IC burn-in approaches can be used, which involves the use of a special adaption of the HDI process to actually create recoverable ICs. This *temporary interconnect* process, forms single-layer temporary patterned overlays on individual ICs, which can be removed after the IC is burned in. Each of these testing techniques represents an interim solution for a problem that will ultimately be solved by the semiconductor vendor.

Three Dimensional HDI

Recent SDIO-sponsored research under the PL program has resulted in the development of a three-dimensional extension of the HDI process. This "3D HDI" is unique among the various approaches that have been proposed to achieve a three-dimensional packaging system in that it is based on direct extensions of the two-dimensional HDI process. A simplified sequence for achieving 3D-HDI is shown in Figure 3. 3D-HDI combines a collection of identically-sized two-dimensional HDI modules into a very compact assembly through direct stacking. In this case, electrical contacts are formed in on the edges of individual HDI modules to be combined into a three-dimensional assembly. After the stack of HDI modules is laminated together, new HDI patterned overlays are created, which interconnect the edges of individual layers together, like a miniature backplane. Depending on the module level wiring capacity requirements, two or all four edges are utilized for patterned overlay interconnection. Several demonstration three-dimensional HDI modules have been constructed, including interconnectivity modules (Figure 4a), thermal profiling modules, and functional memory modules (Figure 4b-4d). Final packaging can be accomplished using kovar packages similar to those previously described for 2D-HDI.

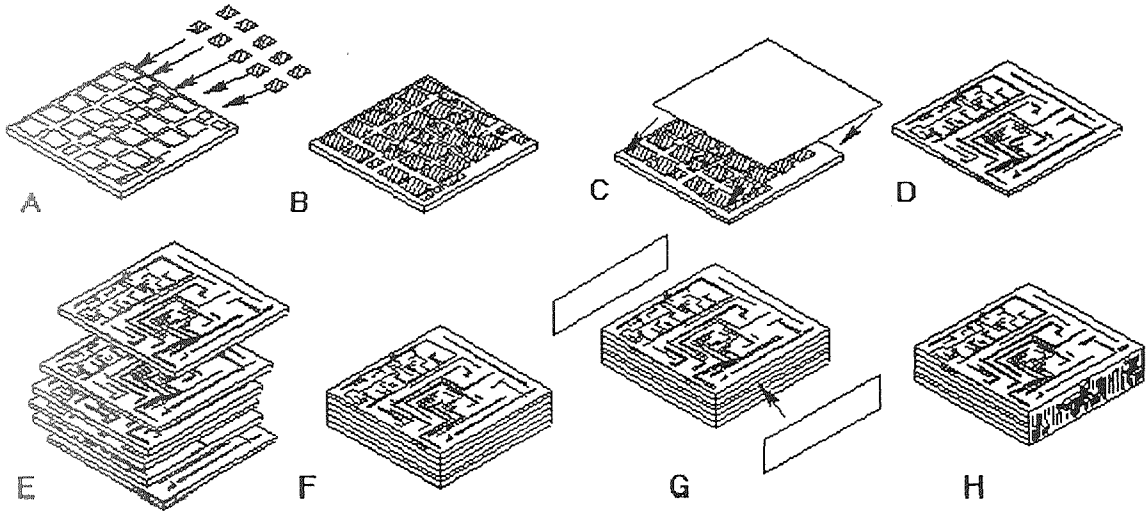


Figure 3. Three-dimensional HDI process.

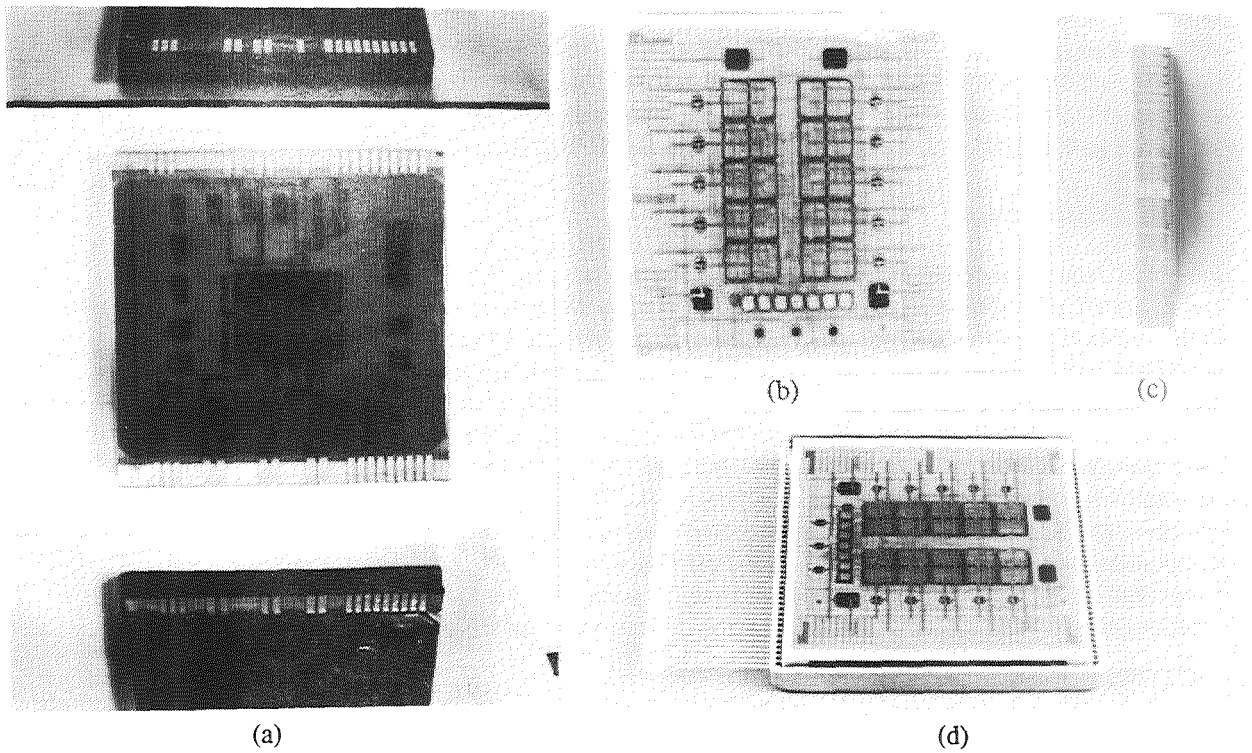


Figure 4. Three-dimensional HDI modules. (a) Interconnectivity Module. (b) Memory Module. (c) Edge view of memory module. (d) Memory module in final package.

Properties of HDI

This section addresses further the electrical and mechanical properties of the HDI process that make it viable for general application and discusses reliability and manufacturability issues.

Electrical Performance

Perhaps the greatest motivation for the development of MCM technologies is electrical performance. As the performance of digital systems built with silicon ICs exceeds 100 MHz, high fidelity interconnections structures are required. The interconnections of a PWB are reasonably high in performance, but their physical span, resulting from the use of SCPs for a conventional system forces the designer to implement transmission line design rules at a sufficiently high frequency. Although transmission line behavior is well understood, the prospect of re-designing hundreds of digital signal lines to accommodate controlled impedances is formidable. Converting such designs to MCM technologies such as HDI allows the system designer to create better systems while still employing the simpler, lumped circuit analysis and design procedures. With HDI in particular, the quality of the interconnection system is very high. The thick copper interconnections minimize series loss, and the relatively thick, low permittivity, planar intermetal dielectrics provide a relatively low capacitance. In this respect, HDI interconnections are superior in quality to the lossy interconnections that are characteristic of the integrated circuit itself.

As promising as HDI is for digital circuits operating in the lumped element regime, it is even a more enabling solution for digital and analog circuits operating in the transmission line regime and even beyond. Measurements recently performed by the Mayo Foundation indicate the capability of two-inch

HDI substrates to support impressed digital signals well above one gigahertz [5]. One of the most significant advantages in electrical performance for HDI is that the high quality interconnection structure terminates directly to the IC itself. The physically smooth transition of an HDI via is particularly important at microwave frequencies, where low-inductance, high quality terminations are desired. As such, HDI provides much higher quality transitions than those provided by wire bonds, tape automated bonding, and even solder (as used in controlled collapse chip interconnection approaches). To better understand these advantages, an effort was recently undertaken by GE to compare ordinary microwave structures built in HDI to those built with more traditional technologies.

Mechanical Design

Patterned overlay processes offer several significant advantages. First, the thermal and electrical paths are separated, providing a more efficient utilization of the available area. All contacts to the components in the substrate are formed simultaneously during assembly, using high yield fabrication methods developed originally for the construction of ICs. The patterned overlay design also supports maximal component densities. In some cases, more than 90% of a substrate area is covered by components, compared to the 6-20% in conventional packaging approaches. The interconnection capability of a patterned overlay process is great compared to MCM approaches based upon wire bonds or tape automated bonding, which are predominantly limited to connecting only the peripheral regions of components. The ability to support to interconnection of contacts distributed throughout the surface of a component is promising for future generations of ICs, which will require greater communication bandwidths. The patterned overlay is more compact vertically, due to its planar construction. This planarity allows very rugged and compact three-dimensional structures to be formed.

Reliability

The robustness of HDI has been graphically demonstrated in a series of tests by PL and GE to test the performance of HDI in extreme thermal, mechanical, and nuclear environments. A summary of these tests are presented in Table 1. Central to the design of the HDI process was the selection of appropriate materials, since many failure mechanisms are related to the interactions that can occur at the interfaces of dissimilar materials. The compatibility of these materials are often exercised by the batteries of tests prescribed in military standards and specifications. For example, several thermal shocks between two temperature extremes tests the differences in thermal expansions of the various materials used in the HDI process. Underground nuclear tests demonstrate the ruggedness of a technology to withstand high amounts of total ionizing dose and thermomechanical shock. On these and other bases, the HDI process has been demonstrated quite spectacularly.

The research to further refine the understanding of HDI reliability continues. One effort, a joint venture of reliability analysts within the Department of Defense and NASA, is exploring the value of the so-called traditional military reliability tests to adequately exploit reliability problems in various MCM technologies, including HDI. This "Reliability Technology" or "RelTech" effort is conducted through theoretical modeling, test, and destructive and non-destructive analysis of groups of HDI test structures of representative complexity. These structures are instrumented with reliability monitoring structures (miniature test ICs developed by Sandia National Laboratories), as well as representative digital logic, memory, analogy, and transmission line circuits. The findings from this effort may lead to future refinement of the criteria used by NASA and the military to evaluate, qualify, and certify MCM technologies for military applications and those commercial applications which rely on military specifications for guidance in technology selection (e.g., heart pacemakers, etc.).

Manufacturability

For both engineering prototypes and high volume production, HDI has several significant manufacturability features. For low-volume production, flexibility is important. In some MCM approaches, significant non-recurring expenses (NRE) are required for the formation of many

photolithographic masks and often the construction of specialized tape automated bonding (TAB) frames. For low volume prototype fabrication, the HDI process, which is maskless and requires no TAB frames, can be particularly cost effective. Engineering changes can and have been performed overnight, in contrast to other approaches, such as cofired ceramics, which often require substantial turn-around times for even minor patterning changes. At the high-volume end of the production spectrum, the impact of NRE is, of course, amortized across a much larger number of units. While primarily a maskless process, HDI can also employ mask-based processing, due to newer, high-accuracy automated die placement equipment. With other production enhancements and the advantage of the patterned overlay process, which forms all interconnections to components as a by-product of fabrication (in contrast to patterned substrate approaches), HDI can potentially realize one of the lowest per-unit costs of any MCM process produced in volume.

Table 1. Representative test data on two-dimensional High Density Interconnect (HDI) substrates (after [1]).

Category	Test	Description
Mechanical	Constant acceleration	7,000 G
	Drop Shock	1,500 G, 0.5 ms
	Extreme mechanical shock	68,000 g linear 178,000 g centrifugal
Thermal	Thermal Cycle	1,000 Cycles -55^{o} to 125^{o} C
	Severe Acceleration	1,000 Cycles -200^{o} to 155^{o} C
Radiation	Thermomechanical Shock	Underground Nuclear Test
	Total Dose	Tested above ground to 40 Megarads total dose

APPLICATIONS OF THE HDI TECHNOLOGY

Since the inception of the PL WSI program, the interest in MCM technologies has become widespread, both in the government and private sector. Clearly, an increased level of integration allows higher performance systems to be constructed, some of which would be impossible to assemble with conventional packaging approaches. The two key considerations for candidate applications are those that would most dramatically benefit from: (1) a overall consistent reduction in interconnection path lengths in a highly controlled manner and (2) a greatly improved wiring capacity. In other cases, 2D- and 3D-HDI can facilitate the assembly of an existing system in a form compact enough to make it useful in ways not previously conceived. Finally, in those applications where "more is better", 2D- and 3D-HDI allow systems of much greater capacity in an equivalent weight and volume. A sampling of those applications that would most dramatically benefit from these traits are presented in the following paragraphs.

Magnetic Recording System Replacements

Every space system, aircraft, and many ground systems require recording systems for data storage. For space systems, an orbit's worth of data must be collected for relay to a ground station located in one position on the surface of the earth. Flight recorders are required in all military and commercial aircraft to hold key information for crash investigations or routine reliability surveys. Finally, the use of data recording systems for instrumentation is widespread in many systems. The traditional use of magnetic recorders becomes less attractive, because of the limited reliability, data recording speed, and ease of

access. For these reasons, solid state storage is being actively considered by the military and NASA. HDI has already been demonstrated in several different memory module designs, fabricated for an upcoming satellite experiment (Figure 5a). Additionally, ruggedized memory module of two different designs have been fabricated for the Defense Nuclear Agency. HDI, particular the 3D-HDI, gives semiconductor memory storage a much greater density, making the solid state storage alternative a lucrative one.

Medical Imaging System Enhancement

A medical imaging system is only one example of a system where the ability to rapidly acquire and process data is an important consideration. One of the key components of any data acquisition system is the analog-to-digital convertor (ADC), which samples a continuously variable signal and provides it a computer in a digital form. It is possible to construct fast, coarse ADCs or higher resolution but slower ADCs with existing monolithic IC processes. While in principle it is possible to assemble fast ADCs with high resolution from a group of low resolution ADCs, the variability in electrical path lengths create electrical skew and differential resistance between channels render this approach impractical when using conventional packaging methods. The first 8-bit video rate flash converters were not routinely used, for example, until companies such as TRW were able to build them monolithically. With HDI, however, the construction of multi-component ADCs may now be practical, since electrical path lengths and electrical contact terminations are directly and precisely controlled through layout. This feature, along with the low permittivity dielectrics used in the patterned overlay, create the electrical performance characteristics needed to build composite, high-performance ADCs.

Mixed-signal applications

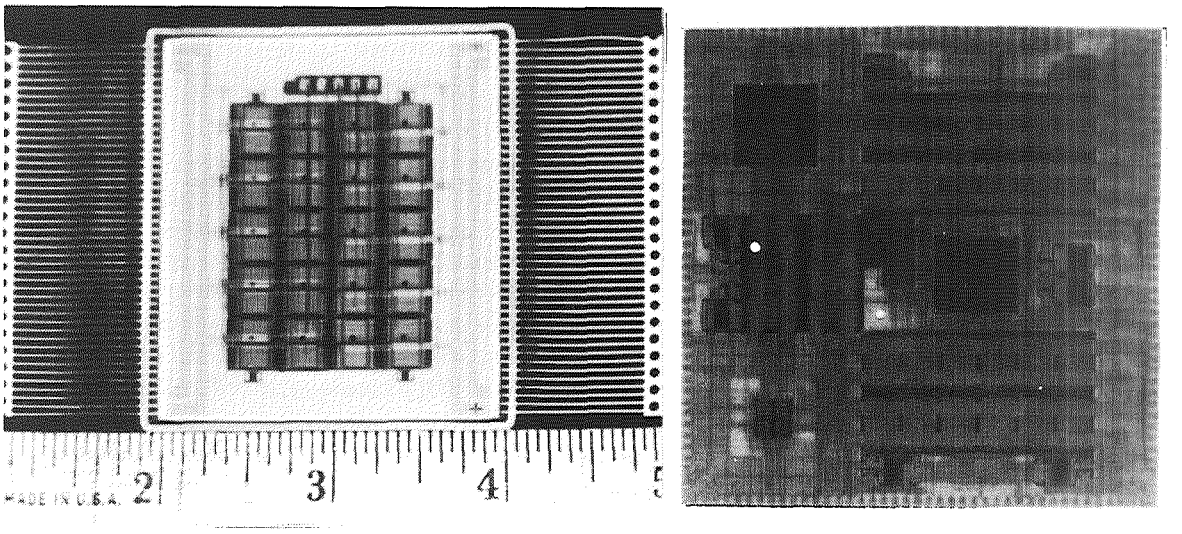
More generally, the construction of superior mixed signal (analog plus digital) systems, such as dc-to-dc power convertors are made possible through HDI. While excellent monolithic, mixed-signal IC processes exist today, it is typically not possible to create both analog and digital devices of superior quality and density within the same IC processes. HDI allows the mixture of a wide variety of device technologies. In the same module, optimal digital (e.g., sub-micron CMOS), analog (e.g., high quality bipolar), and microwave (e.g., GaAs) IC processing technologies can be present. The superior interconnection design afforded by the patterned overlay interconnection system allows the construction of functional blocks that have a performance superior to that in a monolithic or conventionally packaged multi-component approach. The performance advantages of this capability can be considerable. For example, GE, in their own internal research, have developed dc-dc power convertors that approach 100 W/in^3 density with an efficiency above 85%. Monolithic dc-dc power convertors do not presently achieve this efficiency because of the slight compromises made in the mixed-signal monolithic IC processes which accumulate to an overall lower efficiency at the system level.

Telecommunications and Microwave

The increasing emphasis on high-speed telecommunications is driving the performance of electronics. One example of a high-speed telecommunications product is the radio-frequency (rf) modem, which sends information normally transmitted through telephonic or direct-line media through radio transmission. Presently, rf modems are bulky and expensive, and will be prevalent only when they are made compact and inexpensive. They represent one of many opportunities in the telecommunications field where a high-performance MCM technology such as HDI can accelerate use through size, weight, and even cost reduction. The extension of HDI to other applications in the microwave region is also promising, due to its superior electrical performance.

Computers

Faster computers can be constructed using HDI. In several early programs with DARPA, HDI was used to construct a computer based on Texas Instruments TMS320C25 16 bit fixed point microprocessors. The HDI version of a computer previously built on PWB was shown to achieve in some cases above 80 MHz performance, substantially higher than the IC's rated performance of 40 MHz. Other experiments at PL demonstrated a measured performance of up to 71 MHz from memory components rated as 40 MHz components. More recent experiments with Lawrence Livermore National Laboratory on R3000 based computer cores (Figure 5b) built in HDI demonstrated at least a 70% performance improvement. In this case, several of the 16 MHz units (54 components, including an R3000 central processor, R3010 floating point unit, and 256 kilobytes external cache) were functionally operating up to the 27.5 MHz limit of the testing configuration.



(a) (b)

Figure 5. Memory and computer HDI modules. (a) Space-qualified memory module. (b) R3000/R3010 computer core, complete with 256 kilobytes of instruction and data cache.

Future supercomputers will require extraordinary interconnectivity for maximal data bandwidths. Even though monolithic ICs could be constructed to support these high interconnectivity requirements, single chip packages are pin limited, even as they hinder the electrical performance needed by a supercomputer. HDI, particularly 3D-HDI, will allow system designers to re-think and re-define the previously accepted limitations of performance with available packaging technologies. The construction of multi-processor nodes in an exceptionally small space is now possible. Since HDI can support wiring capacities that would allow individual integrated circuits to support thousands of input/output interconnections, multiple-instruction, multi-data stream (MIMD) star topologies for a limited number of 32/64 bit processors operating at very high speeds can be explored. This feature combined with the circuit compression factors provided by 3D-HDI make possible the definition of a new state-of-the-art in computing. Since HDI, for example, allows individual ICs to be placed together within several thousandths of an inch, interconnected with a high performance metal/dielectric system, larger synchronous cache memories, additional co-processors, and associated input/output circuitry can be tightly integrated with a net performance increase, as the new Intel "DX2" microprocessors do at the IC level.

Integrated Sensor/Actuator Assemblies

One trend in advanced packaging is to pack more of a given type of circuitry in the same volume (e.g., more memory). Another is to make a higher performance functional block (e.g., a computing engine). Still another is to integrate more of a system, even a complete system, into a module. Many applications in robotics and automotive electronics could benefit from the ability to build a sensor and processor in the same module. The abilities to place a computer in the arm or joint of a robot or inside the brakes of an automobile allow greatly simplified central control concepts to be applied: less complex communications would be required, bulky wiring harnesses could be reduced or eliminated, and lighter and more rapidly responding systems could be developed. A still more intriguing possibility is that an *entire* electronics system, from sensor to actuator, could be constructed in a two- or three-dimensional HDI system. For example, micro-miniature roving systems, equipped with infrared focal plane arrays or charge-coupled device displays, could be constructed for the exploration of seascapes, the insides of tunnels and mineshafts, or perhaps for the exploration of the surface of another planet. These and other concepts, some still perhaps in the realm of not-so-old science fiction, are achievable through dramatically increased integration capability.

CONCLUSIONS

Through significant research and development activities sponsored by the government, a revolutionary patterned overlay MCM technology has been developed. The HDI technology is as versatile as it is robust, fully capable of meeting the demanding needs of military and commercial applications. It is uniquely capable among MCM technologies in its ability to accommodate a wide variety of existing component technologies, application regimes, operating environments, and ready extension to an even denser three-dimensional form. It is being actively researched for many applications already and is available presently in limited production quantities for evaluation, with large production availability closely following. The benefits of the two- and three-dimensional HDI technology, to reduce the size, weight, and power of electronic systems, and perhaps more importantly, to dramatically improve their performance, make it one of the most significant new technologies for advanced electronics packaging since the original single chip package for the integrated circuit.

REFERENCES

1. Carlson, C.W. *et al.*, "A High Density Copper/Polyimide Overlay Interconnection", *International Electronics Packaging Society (IEPS) Proceedings*, 1988.

2. Bagoklu, H.B. *Circuits, Interconnections, and Packaging for VLSI*, Addison-Wesley, New York, 1990.

3. Cole, H.S. *et al.*, "Polymeric Materials for the GE High-Density Interconnect Process", *Proceedings of 1992 International Society for Hybrid Microcircuits Conference.*

4. Lyke, J.C. *et al.*, "Development and Application of Practical Three-Dimensional Hybrid WSI Technology", *Government Microcircuit Application Conference (GOMAC)*, November 1992.

5. Haller, T.R. *et al.*, "High-Frequency Performance of GE High-Density Interconnect Modules", *Proceedings of the 42nd Electronic Components and Technology Conference, Institute of Electrical and Electronic Engineers*, 1992.