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Walsh Function Generator for the Electronically Scanned Thinned Array Radiometer (ESTAR) Instrument

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Abstract: *A prototype Walsh Function Generator (WFG) for the ESTAR (Electronically Scanned Thinned Array Radiometer) instrument has been designed and tested. Implemented in a single Xilinx XC3020PC68-50 Field Programmable Gate Array (FPGA), it generates a user-programmable set of 32 consecutive Walsh Functions for noise cancellation in the analog circuitry of the Front-End Modules (FEMs). It is implemented in a 68-pin plastic leaded chip carrier (PLCC) package, is fully testable and can be used for noise cancellation periods as small as 2 msec.*

1. Introduction

ESTAR (Electronically Scanned Thinned Array Radiometer) is a passive synthetic-aperture radiometer designed to sense soil moisture and ocean salinity in L-band. It is being developed as an earth probe mission intended for launch in the late 1990's as part of the Earth Observing System (EOS).

A recent feasibility study [1] of the ESTAR concept recommended that a two-dimensional prototype be built in order to study further the design issues involved. Grand Valley State University Professor William A. Chren, Jr. was awarded NASA JOVE Grant NAG 8-226 to design and build four subsystems that will be part of the digital data subsystem (DDS) in this prototype. The second of these four subsystems, the Walsh Function Generator (WFG), has been completed and is the subject of this memorandum. A previous memorandum [2] presented the specifications of the first of the subsystems, called the Output Data Formatter (ODF).

Section 2 is a presentation of background information about the ESTAR. Subsequent sections present the details of the WFG.

2. ESTAR Background

The synthetic aperture sensing technique employed by ESTAR is a method whereby the high spatial resolution and sensitivity of a large dish antenna can be duplicated with a small, lightweight cross-shaped array of dipole antennas (see Figure 1).

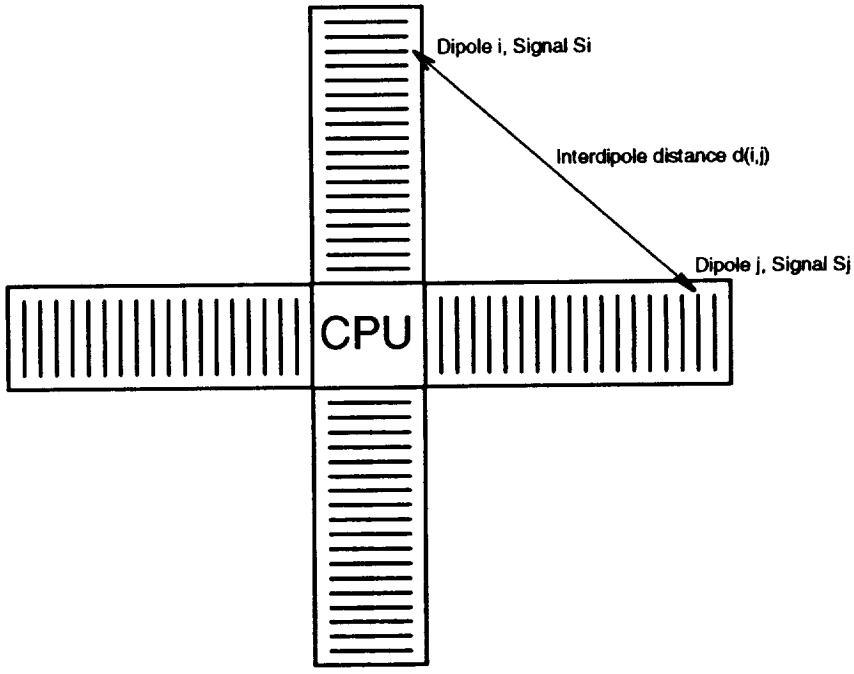

Figure 1: Dipole Antenna Locations on ESTAR Instrument

Such a duplication yields size and weight advantages which make it attractive for use on earth-sensing spacecraft. It is made possible by the calculation, for all pairs (i,j), of the pairwise complex correlation between dipole signals S_i and S_j using the formula

$$< S_i, S_j >= \frac{1}{T} \int_0^T S_i(t) S_j^*(t) dt, \quad (1)$$

in which "*" denotes the complex conjugate and T is a suitably chosen integration period. It can be shown that each of these correlations is a sample, in frequency space, of the spatial Fourier Transform of the brightness temperature distribution over the field-of-view (FOV) of the antenna. Consequently, the visibility function in the FOV can be computed by inverting the sampled transform. Furthermore, the location of the sample in frequency space is determined only by the inter-dipole distance and not by the absolute locations of the dipoles themselves [3].

The data processing system on ESTAR will compute, in real time, these correlations for each dipole pair (i,j). Sensitivity and resolution specifications dictate that 145 dipoles (73 on each leg of the cross) must be used for a full ESTAR mission, or 73 (37 on each leg) for a reduced mission [4]. The correlations will be done digitally at a centrally located processing unit called the CPU, as shown in the figure. The results will then be sent to earth where the inverse transform will be computed. Necessary dipole signal preprocessing, including down-mixing and A/D conversion, will be done at each dipole by circuitry contained in a "Front End Module" (FEM).

2.1 Major Digital Data Subsystem Components

At the functional level, the digital data subsystem (DDS) consists of six major components [5]. The first of these, the Digitizer, must convert the FEM data to digital form before sending it to the CPU. This will be done by an A/D converter in each FEM. The second, the Data Bus, must transport the digitized data from the FEMs to the CPU. The third, the CPU, must compute the correlations for each pair of FEMs. It is also responsible for overall control of the DDS. Furthermore, it must interface with the Small Explorer Data System (SEDS), which is a software and hardware "operating system" on the space vehicle. Among other tasks, SEDS performs overhead functions such as data encoding and transmission to earth, earth command processing and system test. The CPU must pass the correlation products to SEDS for transmission to earth. The fourth component, the System Clock, is necessary to ensure that dipole data samples are generated synchronously by all FEMs. In effect, the Clock signals the FEMs to generate data samples at the same instant. The fifth part, the Phase-Aligner (PA), removes the phase differences between FEM samples when they arrive at the CPU. These differences are caused by unequal data propagation times to the CPU from distant and nearby FEMs. The PA must hold the early-arriving data until the late-arriving data is available. Only when all FEM data for a particular sample time have arrived at the CPU will the PA signal the CPU that the data is ready for correlation. The sixth component, the Walsh Function Generator (WFG), generates a unique Walsh function signal for each FEM. This signal is used to cancel low frequency noise generated by the analog circuitry in the FEM.

These six components fit together as shown in Figure 2. Note that the Walsh Function Generator is distributed among the legs of the cross-shaped array. Such a scheme reduces the amount of wire needed to distribute the walsh signals to the FEMs, and requires that the CPU generate a single walsh generator clock signal for synchronization.

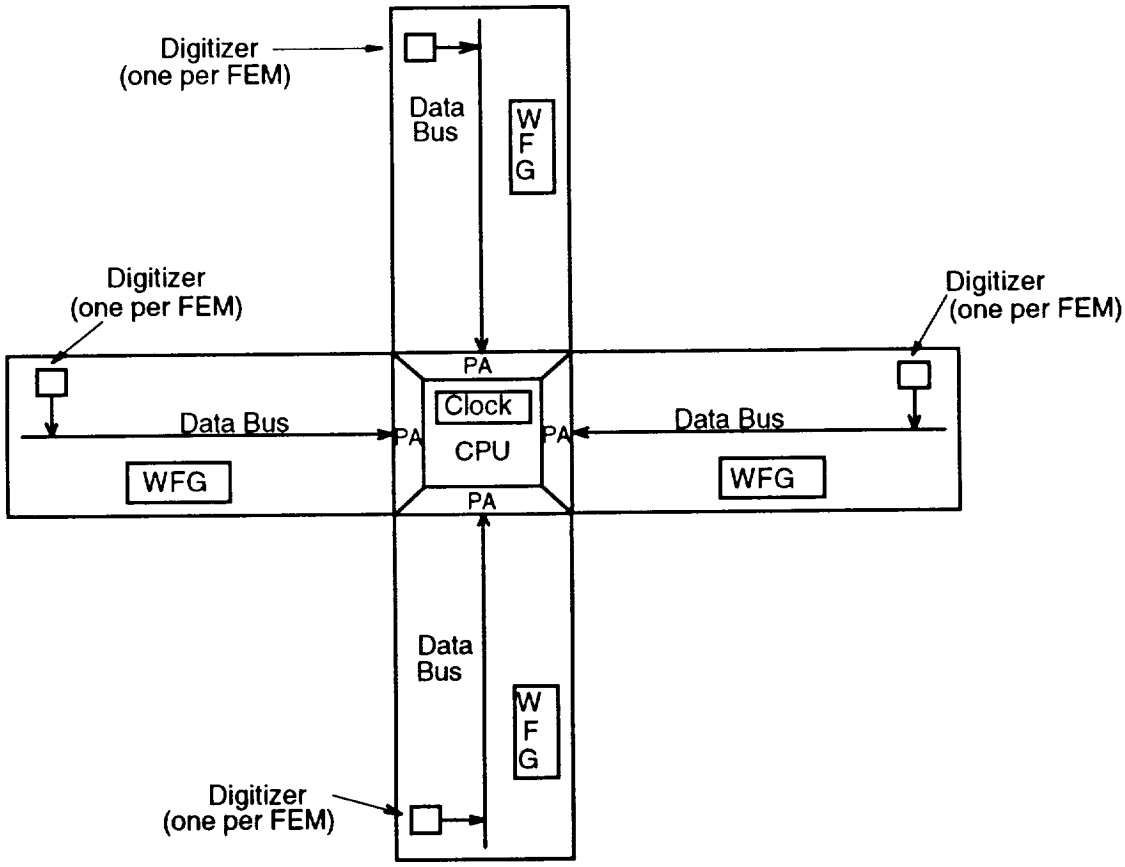

Figure 2: Six Major Components of the DDS

2.2 Noise Removal by Walsh Functions

The Front End Modules (FEMs) include circuitry for splitting the received L-band signal into inphase and quadrature channels, down-mixing to an intermediate frequency, low-pass filtering, amplifying and converting to digital form (see Figure 3). The analog circuitry required

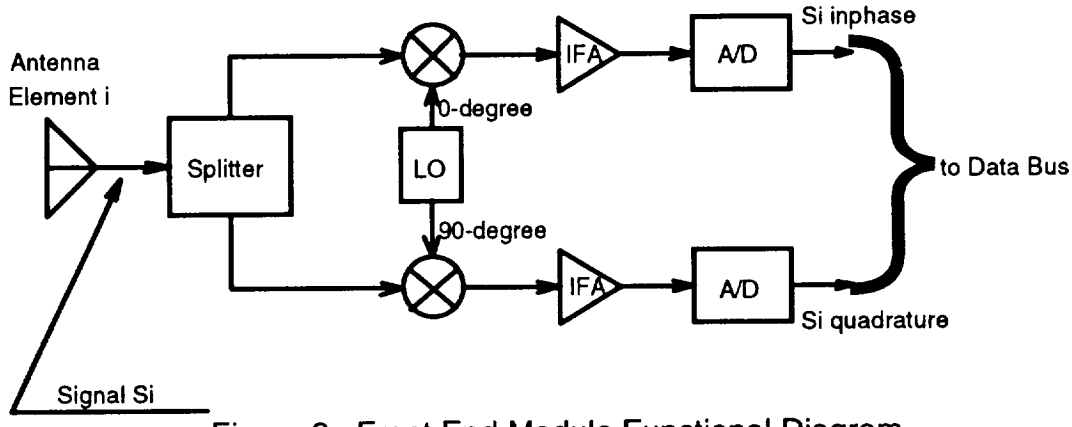

Figure 3: Front End Module Functional Diagram

produces low-frequency ("almost DC") noise due to thermal and aging effects. The magnitude of this noise is large enough to degrade seriously the signal-to-noise ratio of the system, and must therefore be removed.

The noise generated in the ith FEM is removed by multiplying it with a bi-valued (+1,-1) signal called the ith Walsh Function W_i. This method is called "generalized Dicke switching" and is widely used in analog correlation receiving systems. The method can be understood by considering a model for FEM_i shown in Figure 4. In the figure, noise generation has been modeled by the adder just below the Analog Electronics, and the FEM has been modified to include two multipliers which are necessary for noise removal.

In the figure, the received signal S_i is multiplied by W_i immediately upon reception, before it is processed by the analog circuitry. The multiplication is done by selectively phase shifting the signal by 180° using, for example, an analog switch and a half-wavelength section of coax cable. Switching is controlled by the value of W_i. After this phase-switched signal is digitized, it is again multiplied by W_i. This is done by toggling the sign bit of the output of the A/D converter. Since W_i assumes only the values +1 or -1, the digitized S_i is unaffected. However, the noise has been phase shifted synchronously with W_i, and will be removed when the correlation is done in the CPU, as will now be explained.

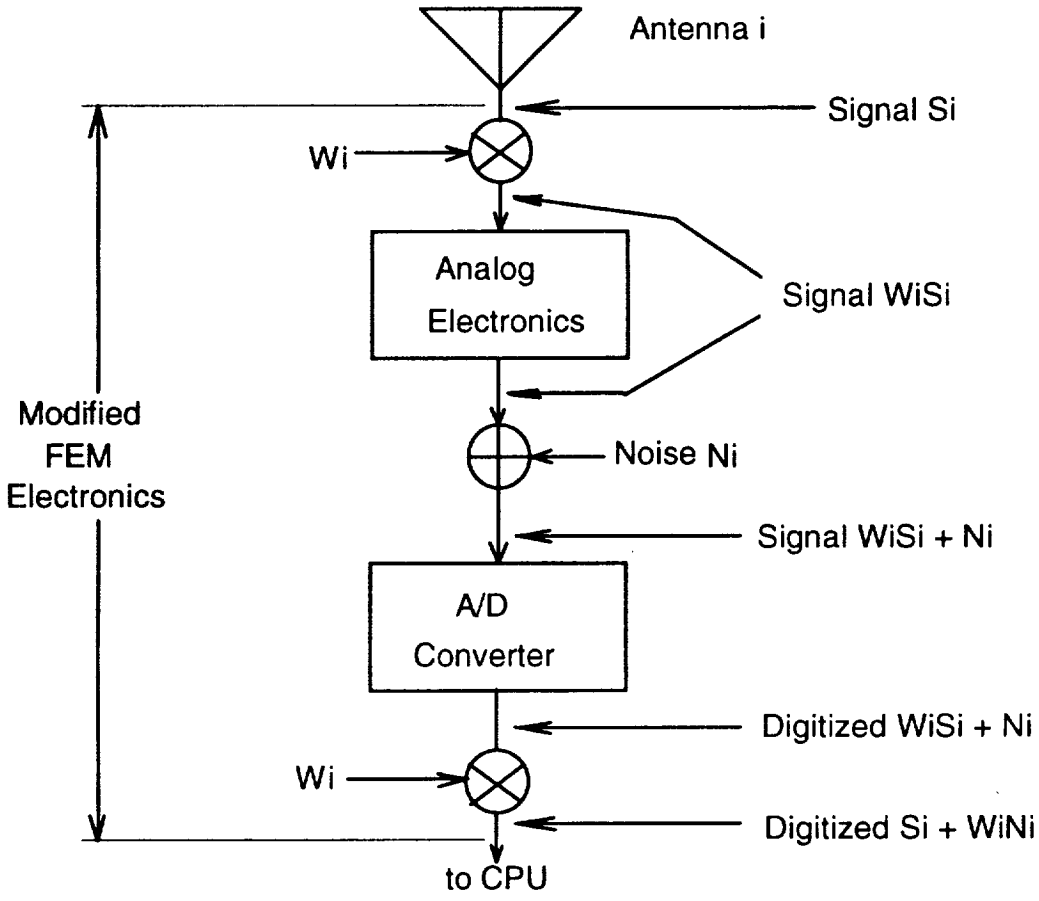

Figure 4: Noise Removal Model for FEM_i

The CPU computes the correlation product given in equation (1) with the noisy signal as

$$< S_i, S_j >= \frac{1}{T}\int_0^T (S_i + W_i N_i)(S_j + W_j N_j)^* dt. \quad (2)$$

This can be expanded as

$$= \frac{1}{T}\int_0^T S_i S_j^* dt + \frac{1}{T}\int_0^T S_i W_j^* N_j^* dt + \frac{1}{T}\int_0^T W_i N_i S_j^* dt + \frac{1}{T}\int_0^T W_i N_i W_j^* N_j^* dt. \quad (3)$$

The desired correlation result is the first term in equation (3). The remaining terms are noise. The second and third terms can be removed by low pass filtering because they possess large components at the same frequencies as the desired signals. The fourth term can be simplified because the Walsh Functions are real and the noise N_i is very low frequency and can be considered constant over the integration period T. We therefore conclude that the last term can be written as

$$\frac{1}{T} N_i N_j^* \int_0^T W_i W_j dt. \quad (4)$$

However, the Walsh Functions are pairwise orthogonal, so that

$$\int_0^T W_i W_j dt = 0 \quad , \; i \neq j \quad (5)$$

and therefore the fourth term in equation (3) is zero.

The remainder of this paper is as follows. Section 3 presents the mathematical definition of Walsh Functions and the design of the WFG. Subsequent sections present the specifications of the integrated circuit.

3. Walsh Function Generator Design

3.1 General Description

The Walsh Function Generator (WFG) must compute a unique Walsh Function for each FEM. The number of FEMs will depend on which ESTAR mission, full (145) or reduced (73) [4], will be flown. The WFG has been designed for up to 256 FEMs (viz., it produces 256 unique Walsh Functions) in order to accomodate future expansions. Modifications of the number of Walsh Functions generated by the circuit can easily be made when a firm number of FEMs has been established.

As explained in Section 2, the WFG is a distributed subsystem consisting of four identical subcircuits, as shown in Figure 2. Each subcircuit is implemented with a Xilinx FPGA. These devices were chosen because they are reprogrammable and allow rapid prototyping and design enhancement. They can be converted to permanent, "hard wired" parts when the complete DDS design has been integrated and tested. The subcircuit design was made programmable in order to accomodate chip packaging constraints. In the discussion that follows, the acronym WFG will retain its original distributed meaning, and in addition will sometimes refer to the circuitry residing in any of the identical subcircuits. The intended meaning will be clear from the context.

The WFG generates 32 consecutive Walsh Functions W(i,t) in one of eight user selectable ranges (0,31), (32,63), (64,95), . . . (224,255). The functions have a period which is equal to T, the correlation period of the CPU, when the WFG is supplied with a clock input of frequency

$$f = \frac{8192}{T}. \tag{6}$$

The inputs and outputs of the WFG are shown in Figure 5. The inputs S0, S1 and S2 determine

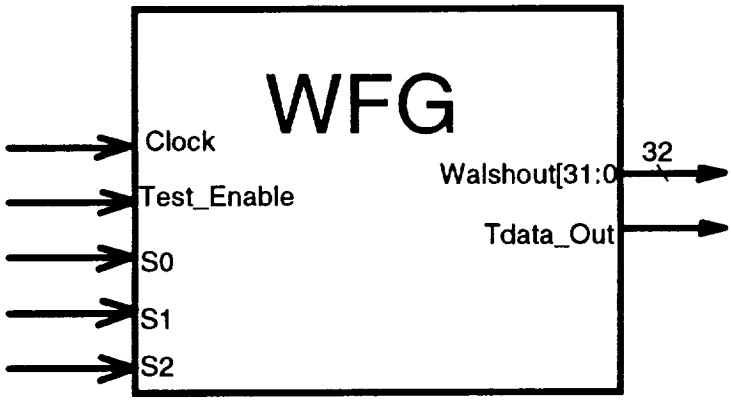

Figure 5: WFG Inputs and Outputs

the set of Walsh Functions according to the truth table in Figure 6. The CLOCK input

S2	S1	S0	Walsh Function Set
0	0	0	[0,31]
0	0	1	[32,63]
0	1	0	[64,95]
0	1	1	[96,127]
1	0	0	[128,159]
1	0	1	[160,191]
1	1	0	[192,223]
1	1	1	[224,255]

Figure 6: Programming Truth Table

must be a square wave of frequency as given by equation (6). The TEST_ENABLE input allows the Walsh values to be serially read by the CPU from the TDATA_OUT pin in order to ascertain
functionality.

A simplified block diagram of the WFG is shown in Figure 7. In the figure, W(i,t) is a

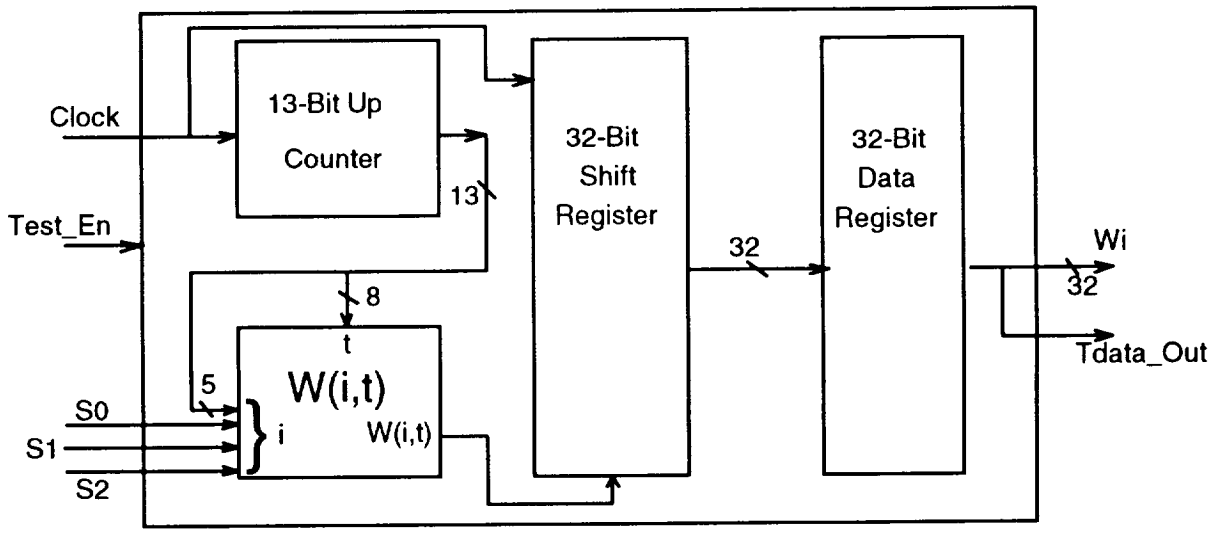

Figure 7: WFG Functional Block Diagram

subcircuit which generates the value of function i at time t, where both i and t are encoded in 8 bits. The result, W(i,t), is stored in the shift register. The more significant eight bits of the output of the 13-bit up counter form the t value, and the five less significant form the low-order bits of i. S0, S1 and S2 form the remaining bits of i, with S2 being the most significant. At the time t specified by the t input lines, the values of the 32 Walsh Functions specified by the i input lines as the counter is incremented, are stored, in turn, in the shift register. When it is full, the data is loaded into the data register. This method holds previous Walsh values steady while new ones are being computed.

The design of subcircuit W(i,t) is based on the fact that

$$W(i,t) = \prod_{r=0}^{p-1} (-1)^{t_{p-1-r}(n_r + n_{r+1})}, \tag{7}$$

where i and t, expressed in binary, respectively are

$$i = (n_{p-1}, n_{p-2}, \ldots, n_0) \tag{8}$$

and

$$t = (t_{p-1}, t_{p-2}, \ldots, t_0). \tag{9}$$

It can be shown that, under the convention that binary 1 represents Walsh value -1, and binary 0 represents Walsh value 1, equation (7) can be computed as the exclusive-or of selected bits of t. Those bits that are selected correspond to the positions of the nonzero bits g_r in the Gray Code representation of i, that is

$$W(i,t) = \bigoplus_{g_r \neq 0} t_{p-1-r}. \tag{10}$$

The circuit diagram for W(i,t) is shown in Figure 8. Figure 9 is a plot of the first 32 functions as generated by the WFG. In the plot, a logic 0 represents a walsh value of +1, and a logic 1 represents a value of -1.

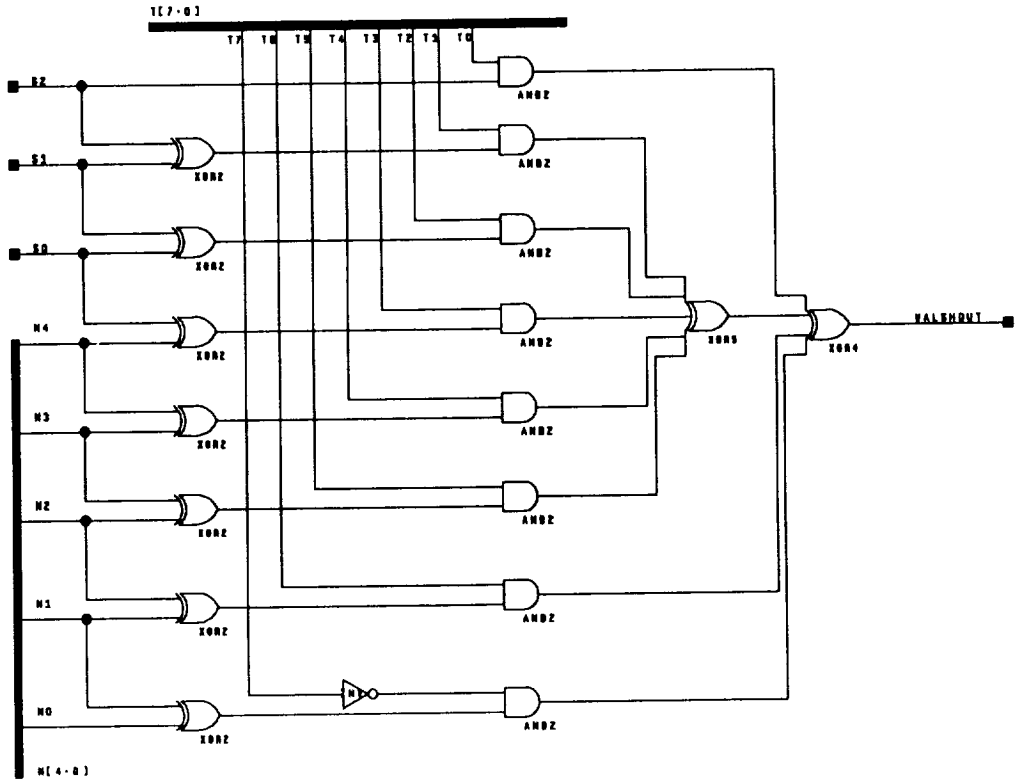

Figure 8: W(i,t) Schematic

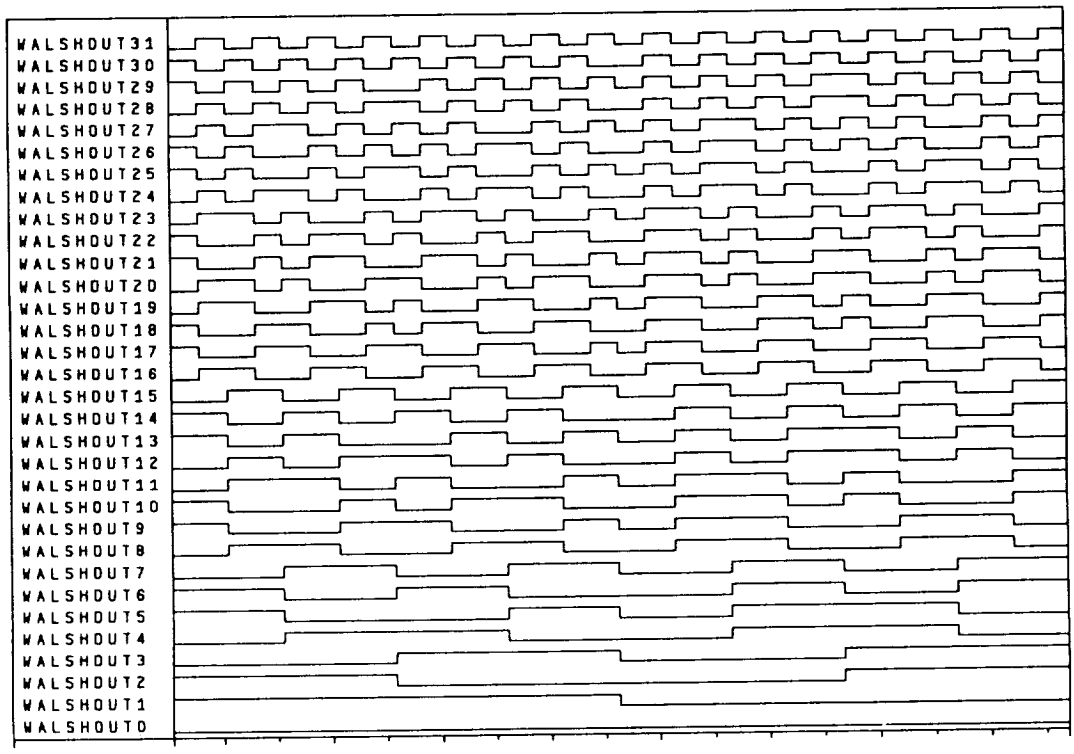

Figure 9: The first 32 Walsh Functions

3.2 Circuit Operation

Initialization

Initialization is performed by applying 32 complete pulses to the CLOCK input after reset has been performed. This generates the initial values of the chosen functions on the 32 WALSHOUT lines. Reset is performed by asserting the MASTER RESET pin (active low) on the FPGA.

Walsh Function Generation

One complete period of the selected functions is generated for every 8192 CLOCK pulses after initialization. Updated values are output every 32 CLOCK pulses. The frequency of the CLOCK signal is related to the correlation period by equation (6).

Test Mode

Test mode allows all output values to be read serially on the TDATA_OUT output line. The values are output in groups of 32, each group corresponding to a fixed time t. The groups are output in order of increasing t. Within each group, the bits are presented in order of increasing index i.

Test mode is entered by first reseting and then initializing the WFG while asserting the TEST_EN input. After initialization is completed, bit zero of group zero (viz., W(0,0) assuming that S0, S1 and S2 are zero) is available on the TDATA_OUT line. For each subsequent high-to-low transition on the CLOCK input the next value is presented (W(1,0), W(2,0),...,W(31,0), W(0,1),...,W(31,1), etc.). This mode allows the CPU to interrogate the WFG and ascertain functionality.

4. Specifications

The schematic diagram of the WFG is shown in Figure 10. The five-input AND gate is

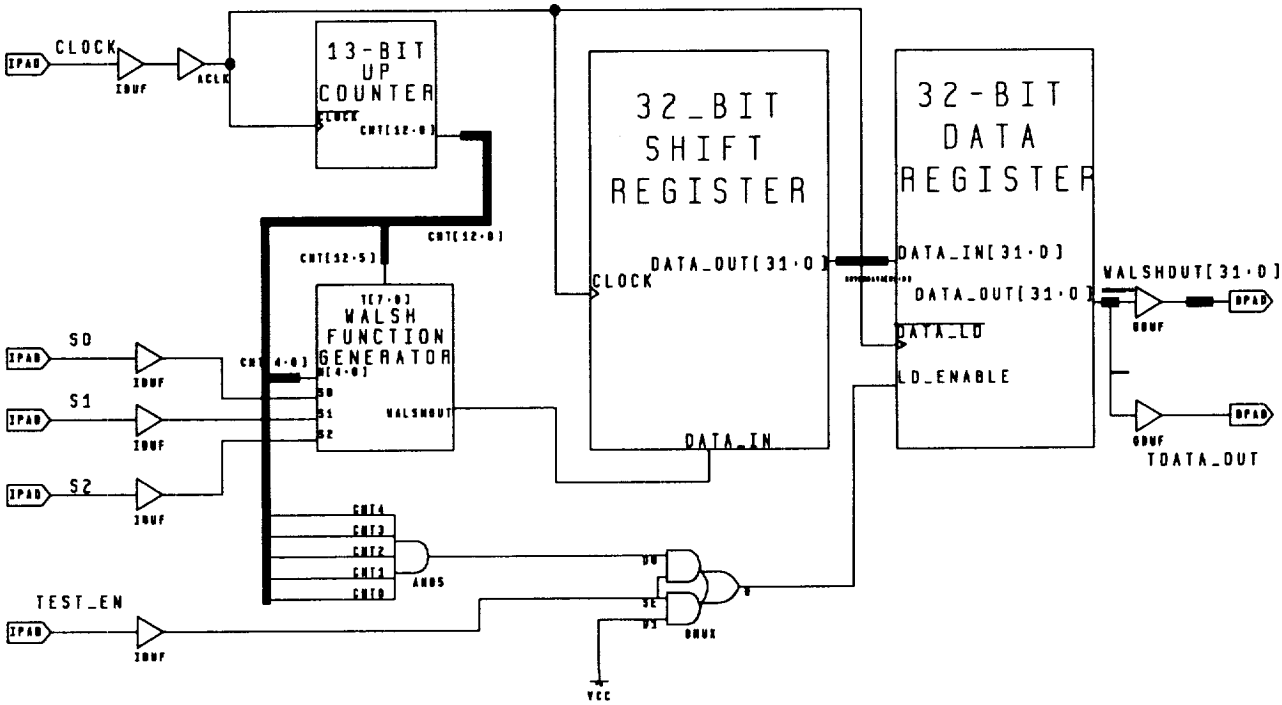

Figure 10: WFG Schematic Diagram

used to enable a loading of the data register when the shift register has reached capacity. The ACLK buffer allows fast driving of the highly-loaded CLOCK and DATA_LD inputs of the shift and data registers, respectively.

4.1 Electrical Specifications

Maximum Absolute Ratings:

Symbol	Description	Value	Units	Conditions
V_{cc}	Supply Voltage	-.5 to +7.0	V	
V_{in}	Input Voltage	-.5 to Vcc + .5	V	
V_{TS}	Tri-state applied voltage	-.5 to Vcc + .5	V	
T_{STG}	Storage Temperature	-65 to +150	Degrees Centigrade	
T_{SOL}	Max. Soldering Temperature	+260	Degrees Centigrade	
T_J	Junction Temperature	+125	Degrees Centigrade	

Recommended Operating Conditions:

Symbol	Description	Min	Max	Units	Conditions
V_{cc}	Supply Voltage 0°C to 70°C	4.75	5.25	V	
V_{IHT}	TTL High-Level Input	2.0	Vcc	V	
V_{ILT}	TTL Low-Level Input	0	0.8	V	
V_{IHC}	CMOS High-Level Input	70%	100%	V	
V_{ILC}	CMOS Low-Level Input	0	20%	V	
T_{IN}	Input Transition Time		250	ns	

DC Characteristics Over Operating Conditions:

Symbol	Description	Min	Max	Units	Conditions
V_{OH}	High-Level Output Voltage	3.86		V	I_{OH}=-4.0mA V_{CC} min
V_{OL}	Low-Level Output Votage		.32	V	I_{OL}=4.0 mA V_{CC} max
V_{CCPD}	Power-Down Supply Voltage	2.3		V	
I_{CCPD}	Power-Down Supply Current		120	µA	V_{CC} max T max
I_{IL}	Input Leakage Current	-10	+10	µA	
C_{IN}	Input Capacitance		10	pF	Sample Tested

AC Electrical Characteristics Over Operating Conditions:

Symbol	Description	Min	Max	Units	Conditions
t_{rise}	Input rise time		250	ns	Worst case[2]
t_{fall}	Input fall time		250	ns	Worst case[2]
t_{data}	Negative-going CLOCK edge to DATA[1] valid		30	ns	Worst case[2]
f	CLOCK frequency		5	MHz	Worst Case[2]

Notes:

1) The signal DATA is shorthand for any WALSHOUT line.

2) 70° C and 4.75 volt supply.

5. Signal Descriptions

5.1 Control Inputs

TEST_EN	High signifies test mode; low signifies normal walsh generation mode
CLOCK	Controls rate of function generation; Walsh outputs are updated every 32 pulses, and repeat every 8192 pulses. Must have frequency given by Equation (6)

5.2 Control Outputs

None.

5.3 Data Inputs

S0, S1, S2	Programming inputs for determining the output Walsh range, as specified in Figure 6

5.4 Data Outputs

WALSHOUT[31:0]	Output pins for the chosen Walsh Functions. Upon initialization, these outputs are updated every 32 CLOCK pulses and cycle every 8192
TDATA_OUT	Serial output pin containing all Walsh values during test mode

6. Package Type

The WFG is implemented in a 68-pin PLCC package with a speed grade of 50 MHz (part number XC3020PC68-50). The FPGA gate density is 81% (52/64 available CLBs used); the pin density is 66% (38/58 available I/O pins used).

7. References

[1] Levine, D. M., Hilliard, L., et. al., 1990, *Electronically Scanned Thinned Array Radiometer (ESTAR) Earth Probe Concept: An Engineering Feasibility Analysis*, Goddard Space Flight Center, page 9.

[2] Chren, W. A., Jr., 1992, *Output Data Formatter for the ESTAR Instrument*, NASA Technical Memorandum.

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[4] Levine, D. M., Gatlin, J., et. al., *Peer Review of LaRC Six-Month Study of "ESTAR" Small S/C Mission*, Langley Research Center/Goddard Space Flight Center internal document, 10/9/92.

[5] *A Digital Data Subsystem Design for an L-band ESTAR Instrument: A Summary of Research Performed in the JOVE Fellowship Program, 6/1/91 thru 11/30/91*, page 5, Appendix A of *ESTAR Digital Data Subsystem Development*, Chren, W. A., Jr., Grand Valley State University, 12/15/91.

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13. ABSTRACT *(Maximum 200 words)*

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