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## Summary

The NASA Lewis Research Center is developing an information-switching processor for future meshed very-small-aperture terminal (VSAT) communications satellites. The information-switching processor will switch and route baseband user data onboard the VSAT satellite to connect thousands of Earth terminals. Fault tolerance is a critical issue in developing information-switching processor circuitry that will provide and maintain reliable communications services. In parallel with the conceptual development of the meshed VSAT satellite network architecture, NASA designed and built a simple test bed for developing and demonstrating baseband switch architectures and fault-tolerance techniques. This report describes the meshed VSAT architecture and the switching demonstration test bed and discusses the initial switching architecture and the fault-tolerance techniques that were developed and tested.

## Introduction

NASA envisions the need for a meshed very-small-aperture terminal (VSAT) satellite communications system that could provide low-data-rate, direct-to-user, commercial communications services for the transmission of data, voice, facsimile, datagram, video, and teleconferencing information. Such a system would enhance current communications services as well as enable new services. Current efforts focus on developing the space segment of the satellite communications system, although the ground segment will be considered concurrently to ensure cost efficiency and realistic operational constraints. The focus of space segment developments is a flexible, high-throughput, fault-tolerant, onboard information-switching processor for regenerative satellite communications systems. This information-switching processor (ISP) is a baseband space and time switch for routing user information between various user Earth terminals.

The satellite architecture (fig. 1) is part of a flexible, low-cost, meshed VSAT network (ref. 1) that provides coverage of the continental United States through eight fixed uplink antenna beams and eight hopping downlink antenna beams. The ISP onboard the satellite connects the uplink and the downlink beams enabling thousands of low-rate users to communicate with each other. The ISP supports two types of user traffic, packet data (packet switched) and nonpacket data (circuit switched). The ISP also connects an onboard autonomous network controller to all the Earth terminals through the uplink and downlink beams for orderwire communications traffic. In addition to its traffic allocation and routing control functions, the autonomous network controller allocates the space and ground resources and performs real-time health monitoring and fault recovery for the onboard communications systems.

Fault tolerance and fault avoidance must be widely considered in the ISP architecture and designs, as well as in the other onboard systems, to obtain reliable communications through the satellite. In order to evaluate candidate circuit and packet switching architectures and to demonstrate fault-tolerance techniques, NASA has developed a simple baseband switching test bed. Several switching architectures were considered, and one was chosen for implementation in this test bed. The design approach, test results, the advantages of the chosen architecture, as well as its status and future directions, are discussed herein.

## Onboard Switching Architectures

Two switching techniques are typically used in onboard-processing satellite systems, namely space switching and time switching. Space-switching techniques set up routing paths that are physically separated from each other (i.e., they are separated in space) (ref. 2). The ISP must utilize space-switching techniques to route data from the input ports (uplink) to the output ports (downlink). Time-switching techniques combine a user's data stream with other users' data into a higher rate data stream in which each user's data is contained in a time slot. In addition to space switching, the ISP must also utilize time switching because of the time-division multiplexed (TDM) formats on both the input ports and the output ports.

The ISP architecture is required to support both circuit traffic and packet traffic. Circuit traffic is typically high volume and requires a relatively long-term dedicated path through the satellite switch. This path is set up by network control prior to the data transmission. In contrast, packetized data are typically bursty, so that a dedicated path allocated to packet data would be underutilized. A much more efficient way to handle packet data is to establish the switching path upon demand (i.e., on a packet-by-packet basis where the packet destination is derived

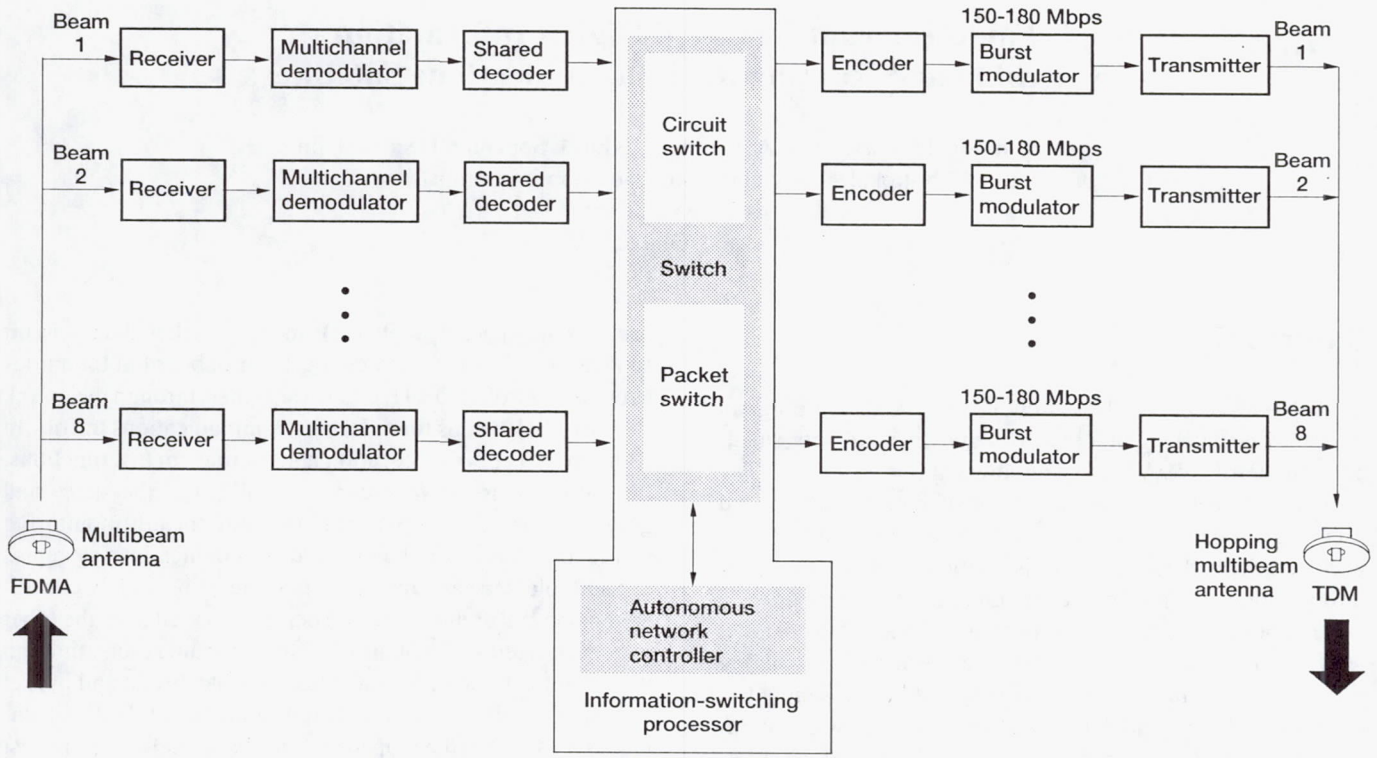


Figure 1.—Meshed VSAT satellite network architecture.

from the packet header (ref. 3). The ISP architecture could be designed with two separate switches, one for packet switching and one for circuit switching, or it could be designed as an integrated switch that handles both types of traffic. The latter case introduces some inefficiencies but is easier to implement. The inefficiencies can occur (1) when circuit-switched data are packetized, causing extra overhead to be introduced; and (2) when packet data are handled by a circuit switch, causing the switching path to be underutilized.

Several switching architectures have been examined for their applicability to the ISP. These architectures can be used for either circuit switching or packet switching although they may more readily support one message type better than the other. They include space-division switching, time-space-time switching, single-stage memories, multistage interconnection networks, and shared-medium switches. These architectures are described here.

Space-division switching is used in systems where time switching is not necessary or as a space stage of a more complicated switch. Space switches are used to route data between two separate locations. Switches that fall into this classification include crosspoint switches and multistage interconnection networks, such as the Banyan, Benes, Clos, and Omega networks. Some multistage interconnection networks are self-routing, which makes them highly suited for packet-switching applications.

Time-space-time switches allow data to be routed from any uplink beam and time slot to any downlink beam and time slot. Time-space-time switches consist of three switching stages, two time stages and a space stage. The time stages are typically implemented by using memories that are often organized in a ping-pong arrangement to allow one frame of data to be written into the memory while the previous frame of data is read out of the memory (ref. 4). Time switching is performed by carefully managing the order in which data are written to and read from the memories. Control memories are used to manage the reading and writing of the time-stage memory by supplying the proper addresses to the memories. The control memories are also ping-ponged so that routing addresses can be updated without interrupting the data flow. The space stage could utilize a space-division switch, such as a crosspoint switch or a multistage interconnection network.

Single-stage memory switches (refs. 5 and 6) can perform both time and space switching, like the time-space-time switch, but require only about one-half of the memory and involve simplified routing techniques. Switching is performed by multiplexing data from each input port onto a TDM bus and then storing the data in the correct memory location according to the destination downlink beam and dwell. The memory is read sequentially on the output side.

Shared-medium switches perform switching by multiplexing all the data onto a common medium and controlling when the data are removed from this medium. An example is a fiber optic ring switch, in which all the input ports time-multiplex their data on the fiber optic bus and switching is performed by controlling which output ports remove the data from the bus (ref. 7).

The single-stage memory switch was chosen for imple-

mentation in the switching demonstration test bed because of its simple architecture, low memory requirement, and ability to support both circuit and packet switching.

## Design Approach

The switching demonstration test bed (figs. 2 and 3) consists of three elements: a baseband switch, fault-tolerant memory, and special test equipment. The baseband switch utilizes a single-stage memory technique and contains four input ports and four output ports. Input and output data are formatted into TDM frames that are 128 bytes long and contain four 32-byte-long time slots. The baseband switch receives its input data from the special test equipment (STE) and sends its output data back to the STE for verification of proper routing. The STE controls and operates the switching test bed. In circuit-switching cases the STE also performs the role of network control and provides the data routing addresses to the baseband switch. The fault-tolerant memory is designed to replace one memory component in the baseband switch. The fault-tolerant memory error-encodes the data before storage, simulates faults in the memory, detects and corrects errors at the memory output, and switches to a redundant memory in the case of a memory failure. The STE monitors and reports the status of the fault-tolerant memory.

### Baseband Switch

The baseband switch was developed to demonstrate simple circuit and packet switching in conjunction with fault-tolerance techniques. The baseband switch (figs. 4 and 5) is configured with four input ports and four output ports, each in

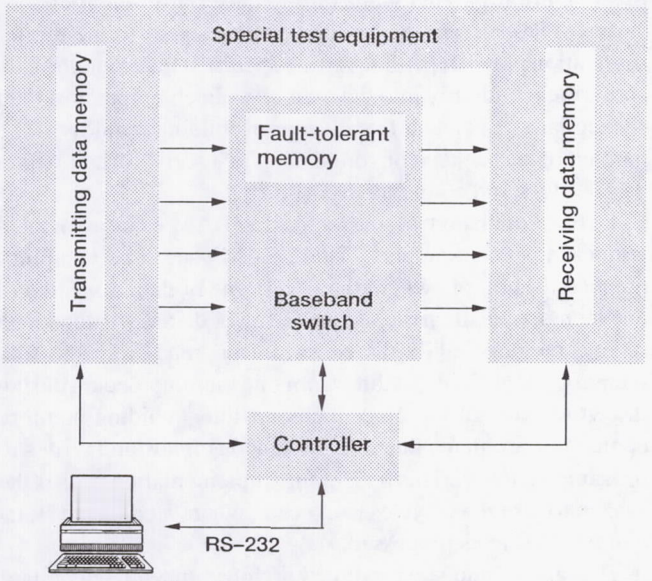


Figure 2.—Block diagram of baseband switching demonstration test bed.

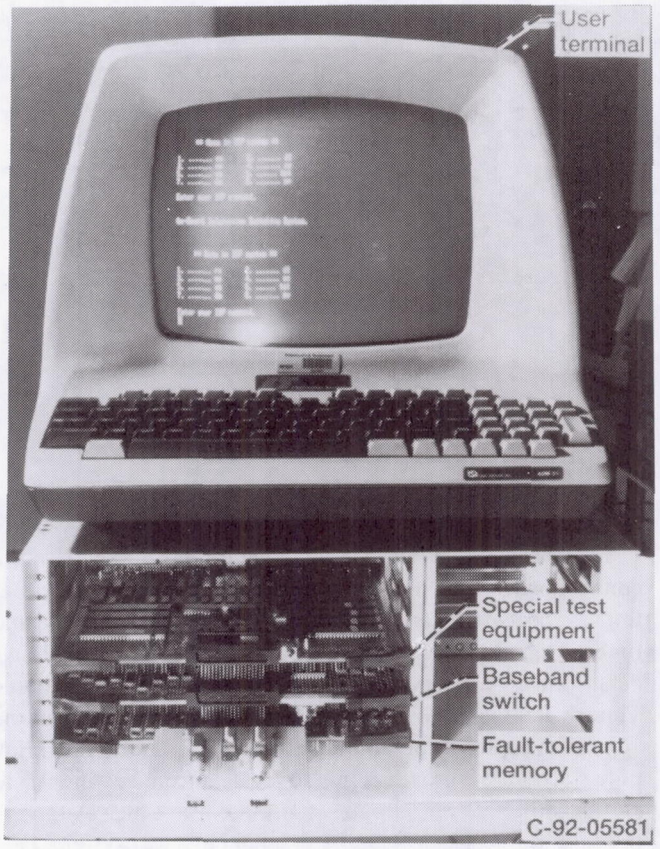


Figure 3.—Switching demonstration test bed hardware.

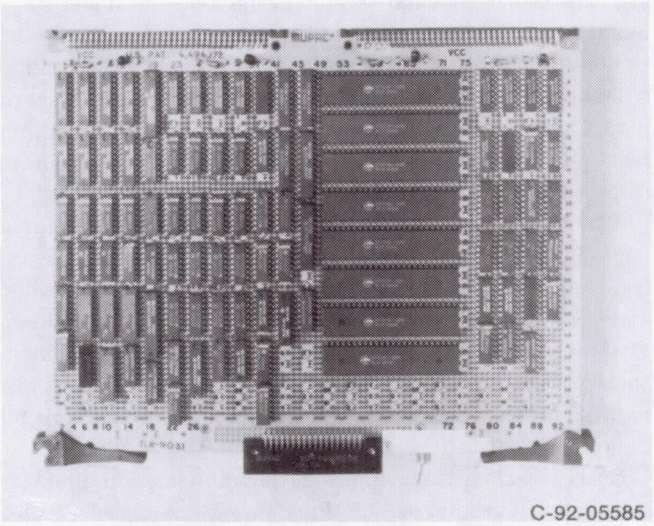


Figure 4.—Switching demonstration subsystem wirewrap bread-board—baseband switch.

a TDM format. In this format the communication data are organized into frames that are subdivided into different time slots. Input data are switched not only to the proper destination port, but also to the proper time slot. For this demonstration a TDM frame consisted of four time slots each containing 32 bytes. This configuration allowed the switch to route data from 16 different sources to 16 different destinations in each frame.

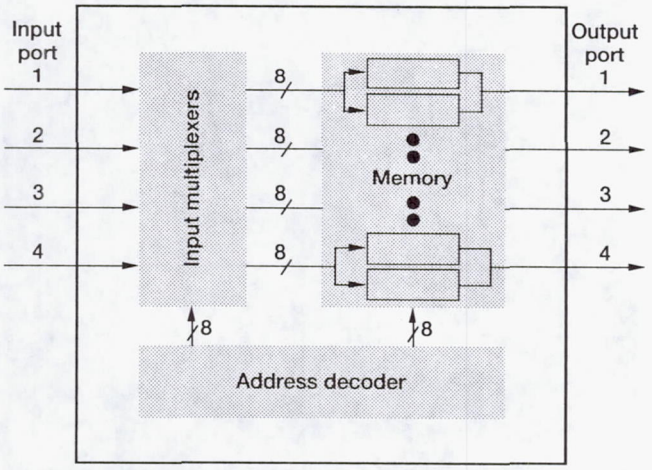


Figure 5.—Block diagram of baseband switch.

The baseband switch features single-point to single-point connections as well as single-point to multiple-point connections. The switch can thus perform point-to-point space and time switching as well as broadcasting. Space switching allows data from any input port to be routed to any or all output ports. Time switching allows the data to be switched from any of the 16 possible uplink time slots to any of the 16 possible downlink time slots. In the broadcast mode the data from any input will be transmitted to all outputs, at any point in time. Although multicasting services are more practical in a real system, only broadcasting was chosen for this demonstration.

The baseband switch design is based on a single-stage memory architecture, where the inputs and outputs of the switch are time-division multiplexed. The switching and routing operation is performed by synchronously controlling a set of input multiplexers and the switch memory addresses, enabling the switch to perform both space and time switching, respectively.

The destination address for the input data is contained in a control memory, which is set up prior to routing by the special test equipment. Each input port and time slot has a separate address stored in the control memory. The destination address, as shown in figure 6, is composed of five bits: Two of them specify one of four possible destination ports, two more bits indicate the time slot within that destination port, and one bit indicates broadcasting.

Space switching is accomplished through a set of multiplexers at the input of the time switch. First, the destination address for each input port is read from the control memory and decoded, producing the control signals to the multiplexers that will route the incoming data to the correct destination port. The data, directed by the multiplexers, are then written to the memory module that is associated with the corresponding destination port.

Time switching is performed by randomly writing data to the switch memory and sequentially reading from it. The destination port memory modules are divided into four sections, each corresponding to a downlink time slot. The destination time

| X | X | X | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|

| | |
|---|---|
| A4 | Broadcasting bit |
| A3, A2 | Destination bits for spacial switching |
| A1, A0 | Time-slot destination for temporal switching |
| X | Don't care bits |

Examples:

| Input address | Destination |
|---|---|
| 00000 | Output port 1, time slot 1 |
| 00001 | Output port 1, time slot 2 |
| 00010 | Output port 1, time slot 3 |
| 00011 | Output port 1, time slot 4 |
| 00100 | Output port 2, time slot 1 |
| • | • |
| • | • |
| • | • |
| 1XX00 | Broadcast time slot 1 |
| 1XX01 | Broadcast time slot 2 |
| 1XX10 | Broadcast time slot 3 |
| 1XX11 | Broadcast time slot 4 |

Figure 6.—Definition of baseband switch destination address.

slot is determined from the destination address, and the data are then written into the section of memory corresponding to the correct time slot.

A broadcast message, which is indicated by the broadcasting bit set to 1 in the destination address, is transmitted to all four output ports simultaneously in the time slot that is indicated by the destination address. In order to avoid output port contention, a broadcasting message has priority over any other information going to the same destination and time slot. This type of contention would be avoided in a real system, where network control would allocate resources prior to routing.

The data flow through the baseband switch is simple. Serial data are received at each of the four input ports and converted to an eight-bit parallel word through a serial-to-parallel converter. The data are then routed (multiplexed) to the proper destination port. Depending on the specified time slot, the data are written randomly into the memory. Each output port then sequentially reads data from its corresponding memory. The parallel data are then converted back to a serial format with a parallel-to-serial converter.

Two sets of random access memories (RAM's) are associated with each destination port. These RAM's are used in a ping-pong configuration, where the first frame of data is written to one memory and then the second frame of data is written to the second memory while the first frame is read from the first memory. In general, reading from one memory occurs during the write cycle of the other memory, thus avoiding memory contention problems due to simultaneous reads and writes to the same memory. This ping-pong implementation causes the system to take $n + 1$ cycles to execute, where $n$ equals the total number of frames processed.

The same single-stage memory architecture with only minor modifications can also support packetized user traffic. The proposed packet switch implementation would feature

multicasting functions and would demonstrate contention problems within the switch. In the packet-switching architecture the packet destination will be contained in the header of each packet, in contrast to the circuit-switching architecture, where the destination address is provided by the STE (or network control). This header contains parity bits for coding purposes as well as packet priority bits. The packet priority information will be used by the switch to deal with possible contention problems. When two or more packets contend for the same downlink destination and time slot, the higher priority packet will be transmitted and the lower priority packet (or packets) will be discarded. For demonstration purposes the discarded packets will be stored in a lost-packet RAM for examination after test execution is complete. In the circuit-switching demonstration contention is not an issue because the microcontroller (network control) prevents the user from transmitting to a time slot or destination port that has been already allocated for another user.

The packet switch would also feature multicasting services, allowing any packet to be transmitted to some or all of the dwells for various beams. Minor modifications to the decoding logic and multiplexing units would be needed for this packet-switching demonstration to handle the multicasting services. For a less complex system that is compatible with the circuit switch already developed, the packet switch would be interfaced with the same STE and fault-tolerance board. Therefore, the approach is basically the same: a single-stage architecture with four uplink beams, four downlink beams, and four dwells within each beam.

## Fault-Tolerant Memory

Fault isolation, detection, and correction are becoming more important as newer, more complex satellite architectures evolve that use onboard processing. As these architectures are developed, fault tolerance and autonomy play a crucial role in maintaining reliable operation of the satellite. Therefore, in order to demonstrate fundamental fault tolerance, a fault-tolerant memory was implemented and integrated into the baseband switch design.

The fault-tolerant memory board (FTMB) operates in two modes: as a stand-alone unit or in conjunction with the baseband switch board by replacing one of its dual port RAM's. The FTMB (fig. 7) detects a one-bit error, corrects it, and reports the error status to the STE microcontroller. The data are protected by using a Hamming error correction code that can correct one-bit errors and identify two-bit errors. When errors of two or more bits are detected, a memory failure has occurred, and the FTMB circuit automatically reconfigures to a redundant RAM.

The FTMB sends a status report to the STE microcontroller by using a hardware interrupt and a parallel input port. The four status flags indicate one bit in error, two bits in error, single error corrected, and redundant RAM switched on-line. The microcontroller acknowledges the status interrupt by sending a

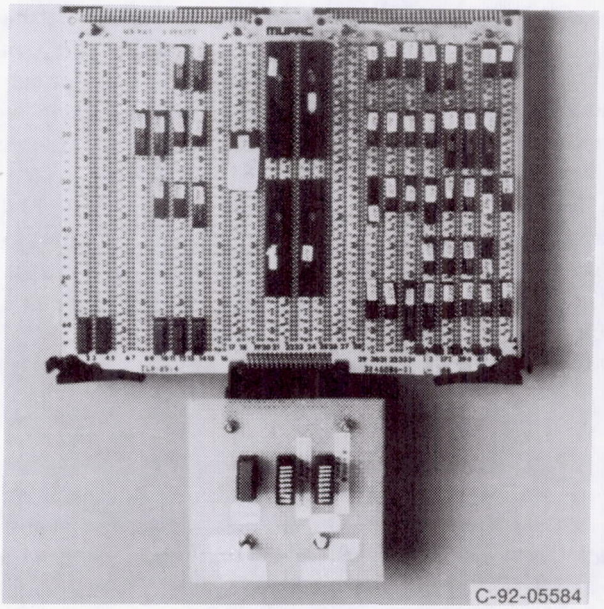


Figure 7.—Switching demonstration subsystem wirewrap breadboard—fault-tolerant memory.

"handshaking" signal back to the FTMB once the status flags are read. These status flags are then interpreted by the STE and a status report is displayed on the monitor.

The overall approach that was taken to demonstrate these features is shown in figure 8. The data from the baseband switch were multiplexed with the onboard erasable, programmable read-only memory data (used for the stand-alone mode only), and the selected data were passed on to the encoder portion of the error detection and correction (EDAC) circuit during a write cycle. This encoder generates a five-bit parity from an eight-bit data word. This parity will be used later for error detection and correction. The encoded input data are stored in both an on-line RAM and a spare RAM. When a failure occurs in the on-line RAM, the spare RAM is ready to take over with minimum data loss.

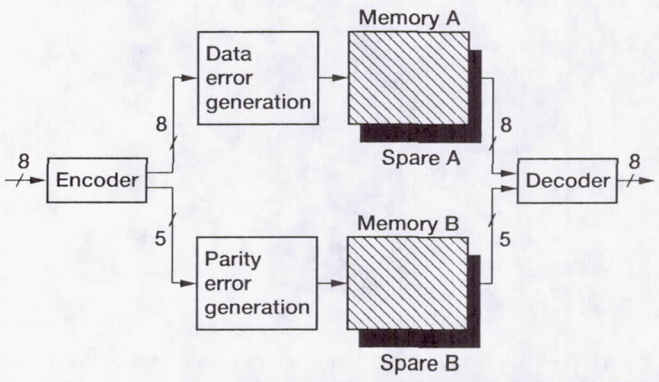


Figure 8.—Fault-tolerant memory data flow.

In order to simulate faults occurring in an onboard memory, errors are induced at the input of the memory. An error can be induced in either the data bits or the parity bits by setting a dual, in-line package switch and exclusive-ORing the switch output with the data. The EDAC decode phase takes the output data and parity from the on-line RAM. If only one bit is in error, the EDAC will correct the error and provide the baseband switch with the corrected data. If dual-bit errors are located by the EDAC, they are flagged but cannot be corrected. In this case, a memory failure is reported and the FTMB switches the spare RAM on-line and takes the corrupted RAM off-line. Once the redundant RAM is on-line, the integrity of the remaining data is preserved. However, the byte where the dual-bit error occurred remains corrupted.

### Special Test Equipment

The special test equipment provides the mechanism for testing the 4×4 baseband switch and fault-tolerance capabilities and also monitors the subsystem status and reports the test results. The STE (fig. 9) has two major parts: (1) microcontroller hardware and software, and (2) custom hardware that interfaces to the baseband switch, the fault-tolerant memory board, and the microcontroller for controlling data transmission and for status reporting. As shown in figure 10, the major components of the STE are the data storage source and sink RAM's, a control (routing address) RAM, control and timing logic, and a user terminal to interface to the microcontroller.

The STE provides two testing modes: the normal mode and the bit-error-rate testing (BERT) mode. In the normal mode data are transmitted from the source RAM's, routed through the baseband switch, and then stored in the sink RAM's. Proper routing is determined by comparing the actual sink RAM contents with the expected sink RAM contents. The STE reports the status of the switching on the user terminal, indicating if a routing error has occurred. In the BERT mode a bit-error-rate tester feeds data through the STE hardware to the baseband switch. Channel selection capability in the BERT mode enables a user to select any of the 16 possible switch channels and test the performance of that channel.

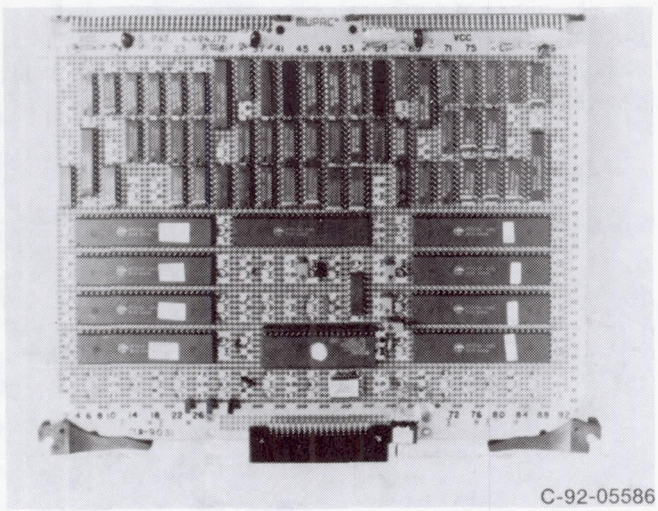


Figure 9.—Switching demonstration subsystem wirewrap breadboard—special test equipment.

Communication between the user terminal and the STE is established through an RS–232 serial interface. An Advanced Micro Devices 87C52T2 microcontroller is used as the system controller. Dual-port RAM's were selected for use as the source and sink RAM's to reduce multiplexers and control logic. One port of each dual-port RAM is connected to the microcontroller, and the other is connected to the parallel-to-serial (P/S) and serial-to-parallel (S/P) converters that transmit and receive data to and from the baseband switch. Eight-bit parallel data from the source RAM's are converted into serial format with a P/S converter and fed into the baseband switch. The switched serial data output from the baseband switch is converted back to an eight-bit parallel format by an S/P converter and is stored in the sink RAM's. The control (routing address) memory stores the destination addresses for the input data (fig. 6). This control memory is loaded with 32 bytes of destination address data corresponding to two frames of data for four input ports where each frame consists of four time slots. The baseband switch fetches the destination addresses from the control memory, decodes the addresses, and routes the input data accordingly.

The STE also generates all clocks that are needed for the system operation. The system clock, which ran at 1 MHz for this demonstration, is provided through an external frequency generator.

The microcontroller software, which is written in PLM/51, has the following system-operation commands: START, RESET, VERIFY, DISPLAY MEMORY, DOWNLOAD, MODE SELECT, and SET CONFIGURATION. The specific function of each command is described in table I.

Finally, two external interrupt program modules, End Test and Status Report, are written for monitoring the test status. The status data from the fault-tolerant memory board are configured as shown in figure 11.

At system powerup all systems are reset. Typical testing sequences are as follows:

(1) Download data.
(2) Download routing addresses.
(3) Start test.
(4) Report status if errors occur.
(5) End test.
(6) Verify test result.
(7) Reset system.

The baseband switch has been tested with four different switching profiles in the control RAM. First, straight-line connections that direct data from sources of RAM1, RAM2, RAM3, and RAM4 to sink RAM1, RAM2, RAM3, and RAM4, respectively, were attempted successfully. Broadcasting and dynamic switching were then each tested separately. In the dynamic switching mode all source RAM data can be transmit-

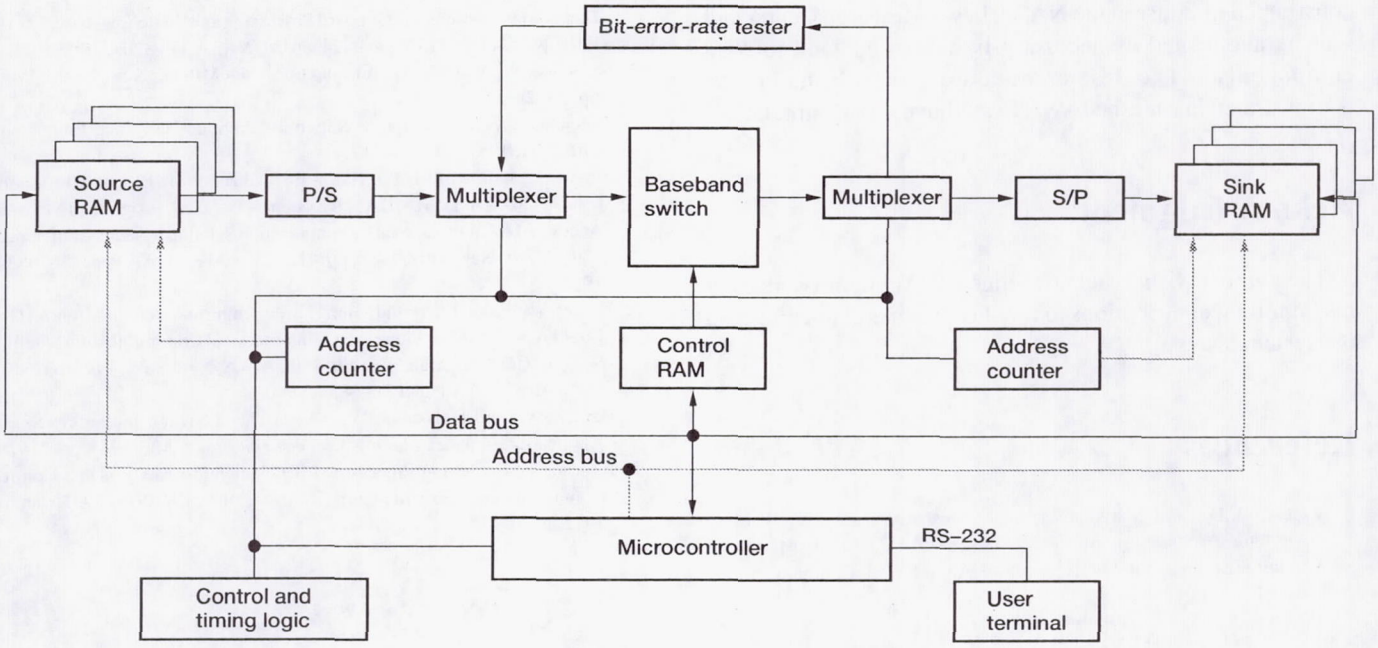


Figure 10.—Block diagram of special test equipment.

TABLE I.—DEFINITION OF MICROCONTROLLER USER COMMANDS

| | |
|---|---|
| START | Execute system test. |
| RESET | Reset system. |
| VERIFY | Compare contents of transmitting RAM and receiving RAM to see if switching was performed correctly. |
| DISPLAY MEMORY | Show contents of all RAM's. |
| DOWNLOAD | Download test data to source RAM's. |
| MODE SELECT | Select operating mode: normal or BERT. |
| SET CONFIG-URATION | Configure switching profile and store destination addresses in control memory. |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | X | S3 | S2 | S1 | S0 |

S0 Error corrected
S1 Double fault
S2 Single fault
S3 Redundant components
X Don't care

Figure 11.—Data format for fault-tolerant memory status report.

ted to any receiving RAM so that the spacial and temporal switching capabilities of the baseband switch can be fully tested. Finally, a test consisting of combined straight-line connections and broadcasting was performed, and proper routing was verified. For easy demonstration, in addition to automatic microcontroller verification of routing, visual verification was made possible by using text type data and by displaying the received memory contents on a terminal.

For BERT mode testing the STE provides a reference clock to the bit-error-rate tester. The serial data and corresponding clock from the bit-error-rate tester are fed back to the STE. Various fixed data patterns in different block sizes were sent through the baseband switch and received in the bit-error-rate tester correctly. Also, pseudorandom data were transmitted, routed, and received flawlessly. For both the normal and BERT modes the fault-tolerant features were successfully tested.

## Status and Future Directions

The switching test bed described herein has been utilized to successfully demonstrate fundamental satellite baseband switching architectures and fault-tolerance techniques. As the development of the meshed very-small-aperture (VSAT) satellite network architecture nears completion, NASA is beginning the conceptual design of candidate baseband switching architectures for the information-switching processor (ISP). Once the best switching architecture is selected, NASA will develop a proof-of-concept ISP that will include the baseband switching system and the onboard controlling processors. The proof-of-concept model will be designed and

constructed in-house at the NASA Lewis Research Center and will be augmented as necessary by advanced fault-tolerant components. The ISP architecture will ultimately be demonstrated in a meshed VSAT satellite network simulation.

## Acknowledgments

The authors wish to acknowledge Mr. William Ivancic for his important contributions to the subsystem architectures and the system test plan.

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The NASA Lewis Research Center is developing an information-switching processor for future meshed very-small-aperture terminal (VSAT) communications satellites. The information-switching processor will switch and route baseband user data onboard the VSAT satellite to connect thousands of Earth terminals. Fault tolerance is a critical issue in developing information-switching processor circuitry that will provide and maintain reliable communications services. In parallel with the conceptual development of the meshed VSAT satellite network architecture, NASA designed and built a simple test bed for developing and demonstrating baseband switch architectures and fault-tolerance techniques. This report describes the meshed VSAT architecture and the switching demonstration test bed and discusses the initial switching architecture and the fault-tolerance techniques that were developed and tested.

**14. SUBJECT TERMS**

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