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Digital Tracking Loops for a Programmable Digital Modem

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ABSTRACT

In this paper, an analysis and hardware emulation of the tracking loops for a very flexible programmable digital modem (PDM) will be presented. The modem is capable of being programmed for 2, 4, 8, 16-PSK, 16-QAM, MSK, and Offset-QPSK modulation schemes over a range of data rates from 2.34 to 300 Mbps with programmable spectral occupancy from 1.2 to 1.8 times the symbol rate; and these operational parameters are executable in burst or continuous mode. All of the critical processing in both the modulator and demodulator is done at baseband with very high-speed digital hardware and memory. Quadrature analog front-ends are used for translation between baseband and the IF center frequency.

The modulator is based on a table lookup approach, where precomputed samples are stored in memory and clocked out according to the incoming data pattern. The sample values are predistorted to counteract the effects of the other filtering functions in the link as well as any transmission impairments.

The demodulator architecture has been adapted from a joint estimator-detector (JED) mathematical analysis. Its structure is applicable to most signalling formats that can be represented in a two-dimensional space. The JED realization uses interdependent, mutually aiding tracking loops with post-detection data feedback. To expedite and provide for more reliable synchronization, initial estimates for these loops are computed in a parallel acquisition processor. The cornerstone of the demodulator realization is the pre-averager receive data filter which allows operation over a broad range of data rates without any hardware changes, and greatly simplifies the implementation complexity.

The emulation results confirmed tracking loop operation over the entire range of operational parameters listed above, as well as the capability of achieving and maintaining synchronization at BERs in excess of 10^{-1}. The emulation results also showed very close agreement with the tracking loop analysis, and validated the resolution apportionment of the various hardware elements in the tracking loops.

INTRODUCTION

In 1977, a generic demodulator structure for digital data transmission was derived from multidimensional detection and estimation theory, and succesfully implemented with primarily analog hardware. [1] Six years later a patent, "Concurrent Carrier and Clock Synchronization (CCCS) for Data Transmission Systems" was granted on its implementation; and the following year, 1984, a paper, "A Joint Estimator-Detector (JED) for QPSK Data Transmission" was published on its theory. [2,3] The JED structure is based on a mathematical description of amplitude modulated carriers in phase-quadrature. As a result, it is applicable to many widely used, filtered signal constellations that can be represented in a two-dimensional space; for example: M-ary PSK, M-ary QAM, MSK, Offset-QPSK, etc. [4]

The detection and estimation operations are interdependent, such that all of the post-detected values and estimates developed coherently aid one another. The upshots of this coherency are: 1) negligible degradation in the bit error rate (BER) for nominal tracking loop bandwidths, 2) the post-detected data feedback used in the estimator loop phase detectors results in less output jitter and cycle skipping at a given SNR than other well known techniques, and 3) the loops can achieve and maintain synchronization at BERs in excess of 10^{-1}.

Over the years, numerous realizations of the JED approach, both analog and digital, have been built and tested. They have primarily been QPSK implementations at data rates ranging from 64 Kbps to 20 Mbps. The subject version has been designed for 2, 4, 8, 16-PSK, 16-QAM, MSK, and Offset-QPSK schemes over a range of symbol rates from 2.34 to 75 Msps. The transmission rate for the 16-ary modulation then can be as high as 300 Mbps.

An extensive hardware emulation program has been written to evaluate the hardware design. All of the performance results which will be presented have been taken from the emulations. The hardware is currently being fabricated, so no measurements are yet available.

MODEM IMPLEMENTATION

The modulator and demodulator conceptual architectures have been described in detail in reference 5, so they will only be outlined in this paper to provide continuity in analyzing the tracking loops. Both architectures were chosen to provide the maximum practical flexibility consistent with the modulation techniques, data rates, operational modes, and spectral occupancies required.

MODULATOR

To achieve the greatest degree of programmability, the critical processing elements in the modulator architecture are digital. The output of the digital processing are in-phase and quadrature (I and Q) baseband sample sequences. These are converted into the analog domain at baseband and mixed with quadrature carriers to an IF. A block diagram of the modulator is shown in Figure 1 and a brief description of its functionality follows.

Many of the most widely used modulation techniques can be represented in a two-dimensional in-phase and quadrature (I and Q) format, for example: M-ary PSK, M-ary QAM, MSK, etc. Therefore, a quadrature data mapping (QDM) between "ABCD" and I, Q is necessary prior to spectral shaping.

Nyquist bandlimiting of the I, Q digital data is most easily realized in the modulator hardware by means of a table lookup. [6] This is because the signal input for bandlimiting has only a few deterministic levels, whereas a true filter would have to operate on signals and noise which exist over a range of values.
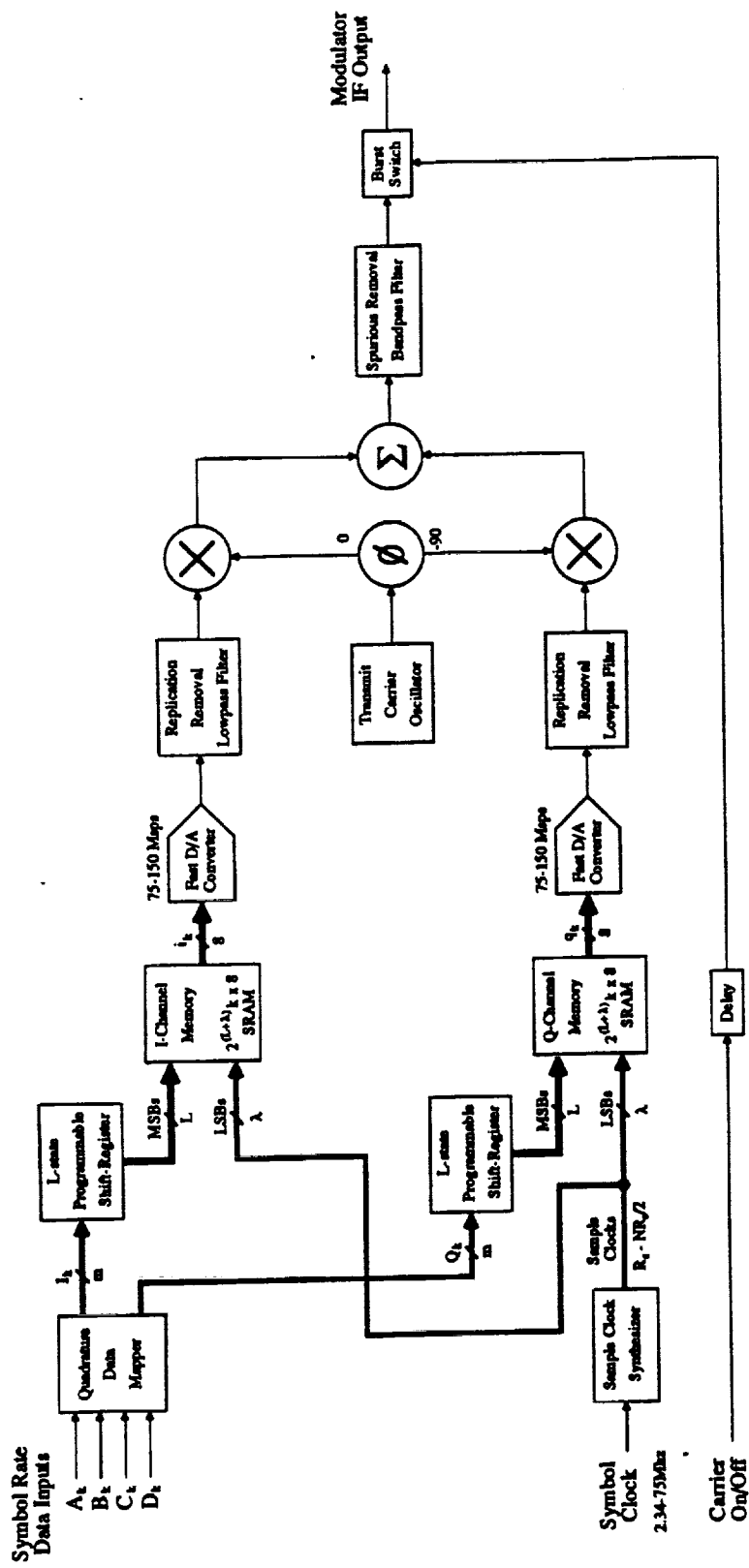
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Figure 1. Modulator Block Diagram

Symbol Rate
Data Inputs

A_k
B_k
C_k
D_k

Quadrature Data Mapper

i_k m

L-state Programmable Shift-Register

MSBs L

I-Channel Memory $2^{(L+\lambda)}$ x 8 SRAM

LSBs λ

i_k 8

Fast D/A Converter

75-150 Msps

Replication Removal Lowpass Filter

Q_k m

L-state Programmable Shift-Register

MSBs L

Q-Channel Memory $2^{(L+\lambda)}$ x 8 SRAM

LSBs λ

q_k 8

Fast D/A Converter

75-150 Msps

Replication Removal Lowpass Filter

×

×

Ø
0
-90

Transmit Carrier Oscillator

Σ

Spurious Removal Bandpass Filter

Burst Switch

Modulator IF Output

Symbol Clock
2.34-75 MHz

Sample Clock Synthesizer

Sample Clocks
$R_s \cdot NR_s/2$

Carrier On/Off

Delay

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Multirate Operation

To provide maximum flexibility, it's desirable to use a single analog replication-removal (RR) filter for the broadest practical range of data rates. This implies that the first sample-rate-replicated spectral lobe of the data always be above a given cutoff frequency. This is accommodated by keeping the sample rate sufficiently high such that the first replica remains above the RR filter cutoff. In other words, as the data symbol rate is lowered, the number of samples per symbol must be increased proportionally. However, this technique is more easily implemented in discrete sample-per-symbol (s/s) steps rather than continuously, and henceforth will be referred to as "gear shifting". A convenient and practical size for each step is an octave in data rate. The ranges of data rates for this design are listed in Table 1. The table only goes up to 32 s/s because of transmit spectral shaping size limitations.

Table 1. Modulator Gear Shifting Rates

Symbol Rate Range (Msps)	Samples/Symbol
37.5 - 75	2
18.75 - 37.5	4
9.375 - 18.75	8
4.6875 - 9.375	16
2.34375 - 4.6875	32

For all the modulation techniques listed, 8-bits are sufficient to yield better than 40 dB of spectral quantization noise. To remove the replicated spectra due to sampling, an elliptic lowpass filter is used. It has a 0.2 dB equiripple passband extending from DC to 48 Mhz (64% of the maximum symbol rate) with a stopband beginning at 60 Mhz of minimum attenuation greater than 30 dB. The sample-and-hold effect of the D/A provides additional filtering to suppress the sample clock replications below 40 dB. To avoid implementing additional analog hardware, group delay dispersion in the replication-removal filter will be compensated in the modulator table lookup. In addition, the transmit spectral shaping will be predistorted to account for IF and anti-aliasing filters, as well as transmission link impairments.

DEMODULATOR

Like the modulator, to achieve the greatest degree of programmability the critical processing elements in the demodulator architecture will also be digital; and quadrature down-conversion as well as baseband sampling will be used in the demodulator front-end.

The anti-aliasing (AA) filter requirements for limiting the incoming bandwidth prior to A/D conversion are very comparable to those for the replication-removal (RR) filter in the modulator. Hence, both filters will be designed with identical passband, transition-band, and stopband parameters.

A general block diagram of the demodulator is shown in Figure 2. Fundamentally, it consists of in-phase and quadrature (I & Q) detection paths and three estimation or tracking loops, namely, AGC, carrier phase, and symbol timing. As indicated in the figure, the detection and estimation operations are interdependent, such that all of the estimates developed coherently aid one another. Pre-averaging receive data filters in both the I and Q channels are critical up-front digital processing elements.

For burst mode operation, a parallel acquisition estimate processor is employed to develop initial tracking loop startup values to expedite synchronization and minimize the probability of PLL hangup. [7, 8, 9] Its estimates are injected directly into the digital tracking loop accumulators.

The analog front-end converts the incoming modulated RF signal down to baseband with a fixed local oscillator, such that a carrier offset beat frequency is superimposed on the baseband I and Q channels. Therefore, after A/D conversion the I and Q paths are passed through a carrier phase rotator to remove the beat, thereby simplifying the subsequent processing. The A/D sample clock is always an integer-multiple of the recovered symbol clock. Hence, its phasing is properly aligned with the detection and transition sample points.
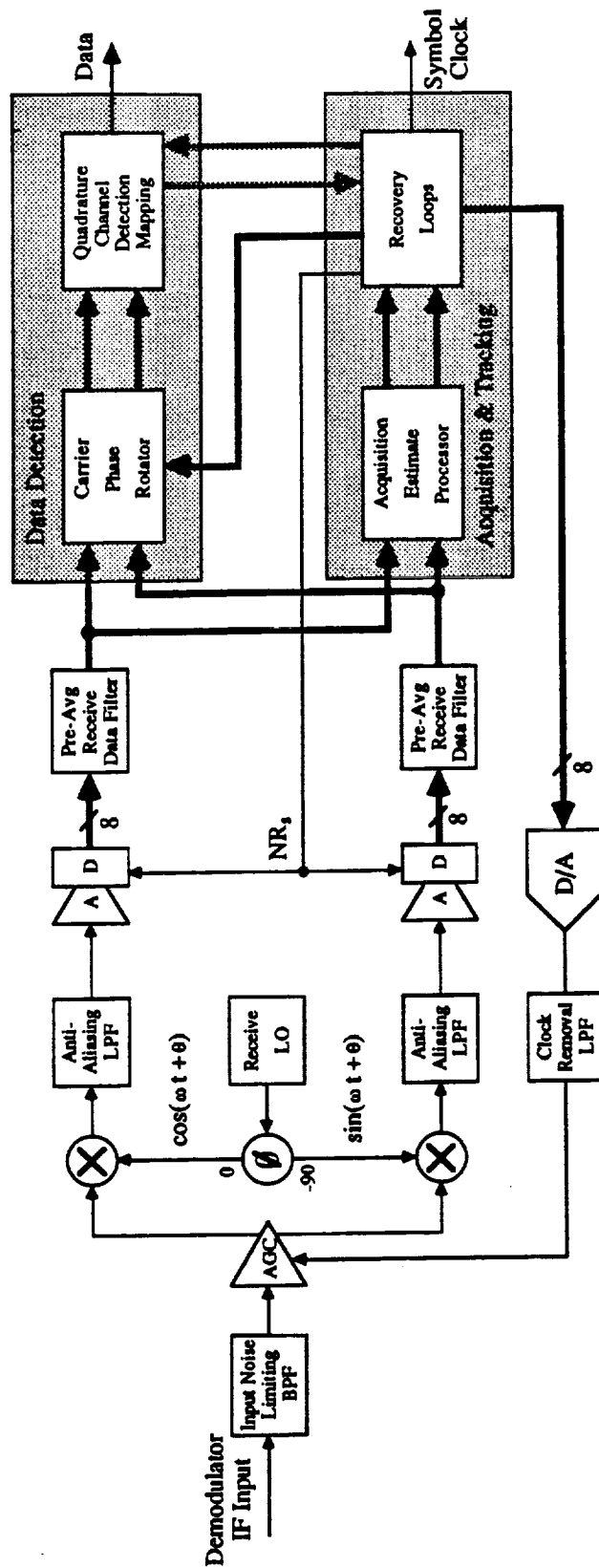
Figure 2. Demodulator Block Diagram

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Detection Path Processing

There are three major processing blocks in the I, Q data detection paths: the pre-averager (PA) receive data filter, the carrier phase rotator (CPR), and the quadrature channel detection mapper (QCDM). The detection path is aided by the tracking loop estimates in the following ways. The arithmetic is fixed point, so to avoid overflow the amplitude level estimate is used to control the gain of the incoming signal. Automatic gain-control (AGC) is also important when the modulation technique has an amplitude level dependency, such as QAM. The carrier phase estimate simply rotates out the carrier beat. The symbol timing phase estimate is embedded in the sample clock at the A/D converter. Hence, the detection path samples are phase-coherent at their inception.

Pre-Averager Receive Data Filter

The PA performs three very important functions in the demodulator:

1) it provides for a very broad range of data rate operation without any hardware changes (typically a factor of 32),

2) it functions as a receive data filter and limits the single-sided incoming bandwidth to $R_s/2$,

3) and it decimates the sample rate to 1 s/s for subsequent processing. [10]

One patent has been granted on its basic conceptual implementation, and another is pending on its extension to provide more selective filtering. [11] For the pre-averager realization used, the effective impulse response aperture length was two symbols wide, and the output sample rate was 1 s/s in the data detection and transition sample paths.

Notation

The notation that will be used throughout this paper is listed in Table 2. The $2k$ and $2k-1$ (even and odd) subscripts denote sample values at the data detection and transition timing instants, respectively; whereas the k subscripts refer to all sample points. Hats denote estimated or detected values.

Table 2. Notation

I'_k	Incoming baseband in-phase samples
Q'_k	Incoming baseband quadrature samples
A_k	Unknown incoming amplitude level
θ_k	Random incoming carrier phase
τ_k	Random incoming symbol time
I_{2k}	Post carrier phase rotated in-phase "detection" samples
Q_{2k}	Post carrier phase rotated quadrature "detection" samples
I_{2k-1}	Post carrier phase rotated in-phase "transition" samples
Q_{2k-1}	Post carrier phase rotated quadrature "transition" samples
$\hat{I}_{2k}$	In-phase post-detected data feedback samples
$\hat{Q}_{2k}$	Quadrature post-detected data feedback samples
$\Delta\hat{I}_{2k-1}$	In-phase post-detected data feedback difference samples
$\Delta\hat{Q}_{2k-1}$	Quadrature post-detected data feedback difference samples
$\Delta\hat{A}_o$	Initial amplitude level offset estimate
$\hat{\theta}_o$	Initial carrier phase estimate
$\Delta\hat{\theta}_o$	Initial carrier Frequency estimate
$\hat{\tau}_o$	Initial symbol timing estimate
$\hat{A}$	Amplitude reference level
ΔA_{2k}	Amplitude level error
$\Delta\theta_{2k}$	Carrier phase error
$\Delta\tau_{2k-1}$	Symbol timing error
K_d	Carrier and Clock phase detector gain constant
K_A	AGC loop gain constant
K_θ	Carrier phase gain constant
$K_{\Delta\theta}$	Carrier frequency gain constant
K_τ	Symbol timing loop gain constant
$\Delta\hat{A}_{2k}$	Amplitude level offset output estimate
$\hat{\theta}_{2k}$	Carrier phase output estimate
$\Delta\hat{\theta}_{2k}$	Carrier Frequency output estimate
$\hat{\tau}_{2k-1}$	Symbol timing output estimate

Carrier Phase Rotator

The carrier phase rotator (CPR) removes the frequency beat in the I and Q channels resulting from the use of a fixed carrier LO, frequency translation. Prior to the CPR the I and Q channels may be described by

$$I'_k = A_k [i_k \cos(\theta_k) + q_k \sin(\theta_k)] \tag{1a}$$

$$Q'_k = A_k [q_k \cos(\theta_k) - i_k \sin(\theta_k)] \tag{1b}$$

If the carrier phase tracking is sufficiently accurate, the frequency beat is taken out by performing the two 1x2 matrix multiplications of equations (2a, b).

$$I_k = [\cos(\hat{\theta}_k) \quad -\sin(\hat{\theta}_k)] [I'_k]$$

$$= A_k [i_k \cos(\theta_k-\hat{\theta}_k) + q_k \sin(\theta_k-\hat{\theta}_k)] = A_k [i_k] \tag{2a}$$

$$Q_k = [\sin(\hat{\theta}_k) \quad \cos(\hat{\theta}_k)] [Q'_k]$$

$$= A_k [q_k \cos(\theta_k-\hat{\theta}_k) - i_k \sin(\theta_k-\hat{\theta}_k)] = A_k [q_k] \tag{2b}$$

Quadrature Channel Detection Mapper

The quadrature channel detection mapper (QCDM) performs the inverse operation of its counterpart in the modulator, but at a much higher resolution because of the inclusion of noise in the demodulator. In general, the QCDM maps the post-CPR baseband I and Q channels into as many as four parallel data streams (ABCD) for 16-ary signalling. For PSK modulation techniques, the decision boundaries are radial lines that bisect the distance between adjacent signals in the constellation (assuming equally likely a-priori signal probabilities); whereas for QAM, the boundaries form an amplitude-dependent grid pattern. The different mappings are most easily implemented as a table lookup.

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Tracking Loop Analysis

To facilitate coherent detection of the digital data, three tracking loops are typically necessary: amplitude level or automatic gain control (AGC), carrier phase, and symbol timing. In each loop there is a nominal operating setting, for example, an amplitude reference level or a numerically-controlled oscillator (NCO) center frequency. An error signal is added to the nominal settings in each of the three loops to make corrections for tracking. The error signals were derived in reference 3 for QPSK modulation, but are readily extendable to most two-dimensional signalling formats. These include such popular modulation techniques as 2-, 4-, 8-, 16-PSK, MSK, Offset-QPSK, and 16-QAM. The three digitally implemented, interdependent tracking loops will now be analyzed.

AGC Tracking Loop

For signal constellations that can be placed on a common power circle such as the PSK and MSK formats listed above, AGC isn't explicitly necessary for the detection process because the decision boundaries are radial lines which aren't amplitude dependent. However, the error signal detector gain in all three tracking loops scales with the incoming signal level; so the incoming amplitude level affects their open loop gains and closed loop bandwidths. In addition, with a fixed-point arithmetic digital implementation, the maximum sample value excursions must be limited to prevent overflow.

Incoming gain or level fluctuations are generally extremely slow relative to the data rate. Hence, for most applications a first order tracking loop is sufficient; whereas for operation with relatively short bursts and a sufficiently accurate acquisition estimate, the estimate can be held for the duration of the burst and no AGC tracking is necessary. [7, 12]

A block diagram for a gain parameter model of the AGC tracking loop is depicted in Figure 3. It consists of a gain-controlled amplifier, amplitude level error detector, and a multiplier-accumulator (MAC) to provide filtering. The input data and error detector multiplier input resolutions were 8-bits. The accumulator resolution was 24-bits of which the 8 most significant were used to control the gain.
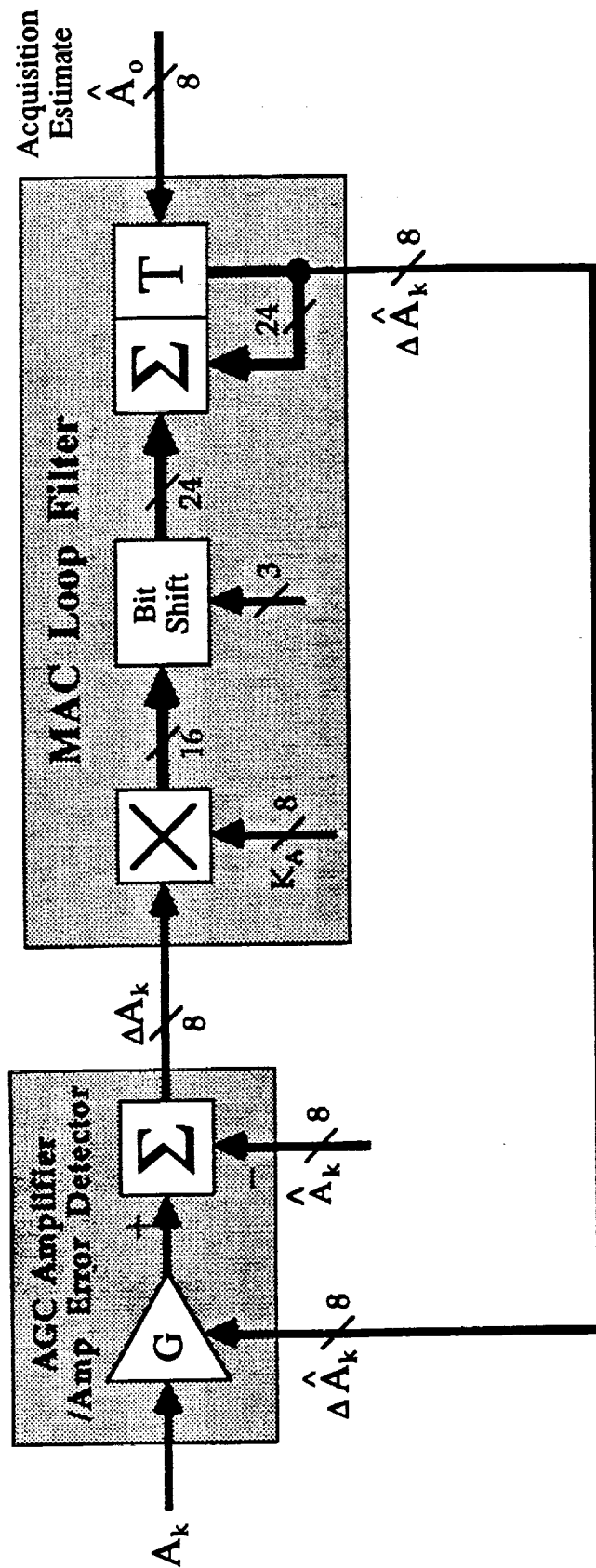
Figure 3. AGC Tracking Loop Model

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AGC Error Detector

The AGC tracking error signal is defined in equation (3);

$$\Delta A_{2k} = (I_{2k} \hat{I}_{2k} + Q_{2k} \hat{Q}_{2k}) - \hat{A}$$

$$= A_{2k} (i_{2k} \hat{I}_{2k} + q_{2k} \hat{Q}_{2k}) - \hat{A} \tag{3}$$

with $\hat{A} = (\hat{I}_{2k} \hat{I}_{2k} + \hat{Q}_{2k} \hat{Q}_{2k})$. When the signals all reside on the same power circle as with the PSK modulation family, $\hat{A}$ is a constant; but for constellations such as 16-QAM, $\hat{A}$ takes on three values as a function of the post-detection data feedback.

AGC Closed Loop Transfer Function

Dropping the subscripts for clarity, the amplifier gain may be expressed in terms of the amplitude level error output estimate as

$$G(\Delta\hat{A}) = G_{nom} \hat{A}/(\hat{A} + \Delta\hat{A}), \text{ such that } \Delta\hat{A} > -\hat{A} \tag{4}$$

Note when $\Delta A = 0$, the amplifier is set to its nomimal gain.

The MAC transfer function may be written in terms of its z-transform as

$$\Delta\hat{A} = K_A \Delta A / (z-1) \tag{5}$$

where $\Delta A = G(\Delta\hat{A}) A - \hat{A}$. Substituting for ΔA into equation (5) gives

$$\Delta\hat{A} = K_A [G(\Delta\hat{A}) A - \hat{A}] / (z-1)$$

$$= K_A \hat{A}[G_{nom} A - (\hat{A} + \Delta\hat{A})] / [(z-1)(\hat{A} + \Delta\hat{A})] \tag{6}$$

Equation (6) can be rewritten in standard second order polynomial format as

$$\Delta\hat{A}^2 (z-1) + \Delta\hat{A} \{\hat{A}[(z-1) + K_A]\} + K_A \hat{A} (\hat{A} - G_{nom} A) = 0$$

$$\Delta\hat{A}^2 (a) + \Delta\hat{A} (b) + (c) = 0 \tag{7}$$

The roots of equation (7) may be found from

$$\Delta\hat{A} = -b (1 \pm \sqrt{1 - 4ac / b^2}) / 2a$$

$$= -b \{1 \pm [1 - 2(ac / b^2) + 2(ac / b^2) - \ldots]\} / 2a$$

$$= -c / b \tag{8}$$

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where only the first term in the expansion has been used since $b^2 \gg ac$. The resultant transfer function is then

$$\Delta \hat{A} = K_A \, (\, G(\Delta \hat{A}) \, A - \hat{A} \,) \, / \, [\, z + (K_A - 1) \,]$$ (9)

A great deal is known about setting the closed loop parameters to maintain stability and the desired transient response for analog tracking loops. [13] Hence, the impulse invariance technique will be used to find the corresponding digital loop roots. The conversion is related as

$$z_{root} = \exp(-\omega_A T_s) = - (K_A - 1)$$ (10)

The loop gain constant is then determined by

$$K_A = 1 - \exp(-\omega_A T_s)$$

$$= 1 - (1 - \omega_A T_s)$$

$$= \omega_A T_s$$

$$= 4(B_A / R_s)$$ (11)

where $\omega_A = 4B_A$ and $T_s = 1/R_s$. The AGC closed loop time constant in symbol time units is then

$$(\tau_A / T_s) = (1/4) \, (R_s / B_A)$$ (12)

with $\tau_A = 1/\omega_A$.

Symbol Timing Tracking Loop

Like the AGC loop, the symbol timing loop is first order and requires only a single phase accumulator. Since a numerically-controlled oscillator (NCO) is used to reconstruct the clock, its inherent phase accumulator serves as the loop filter. A block diagram of the loop is given in Figure 4. Note that the loop also contains a multiplicative gain, M before the NCO, as well as a divide-by-N gain after the NCO. The multiplicative gain comes about because the NCO input sample clock is higher than the incoming sample rate. Thus, incoming samples are typically accumulated more than one-for-one. Also, since the NCO output is at the sample rate frequency, NR_s, there is a divide-by-N in the loop. The input data and error detector multiplier input resolutions were 8-bits. The timing phase accumulator resolution was 24-bits of which the 10 most significant were mapped into sinusoidal sample values. After

Symbol Timing Phase Error Detector

The symbol timing phase error signal is defined in equation (13);

$$\Delta \tau_{2k-1} = I_{2k-1} \Delta \hat{I}_{2k-1} + Q_{2k-1} \Delta \hat{Q}_{2k-1}$$

$$= A_{2k-1} (i_{2k-1} \Delta \hat{I}_{2k-1} + q_{2k-1} \Delta \hat{Q}_{2k-1}) \tag{13}$$

where $\Delta \hat{I}_{2k-1} = (\hat{I}_{2k} - \hat{I}_{2k-2})$. If no data transitions occur, the symbol timing phase detector output is zero. The loop gain and bandwidth are then effectively zero, and the loop time constant is extremely long. Moreover, the best the loop can do in the absence of data transition information is to hold its last accumulated error value and coast. For multilevel modulation techniques, the error signal is weighted in proportion to the differential magnitude of the data transition.

Symbol Timing Closed Loop Transfer Function

The NCO transfer function may be written in terms of its z-transform as

$$\hat{\tau} = (M/N) K_\tau \Delta \tau / (z-1); \tag{14}$$

where $\Delta \tau = K_d (\tau - \hat{\tau})$. To avoid using an extra multiplier, the loop gain parameter, K_τ is incremented in powers-of-two by shifting the bits coming in to the NCO up or down. The phase detector gain, K_d is proportional to the incoming signal amplitude, A_{2k-1}, and the number as well as the magnitude of the transitions in the data pattern. For example, for QPSK with "10..." data patterns in both the I and Q channels, K_d is maximized; whereas with PN data, K_d would be half of that maximum value.

Substituting for $\Delta \tau$ in equation (14) gives

$$\hat{\tau} = (M/N) K_\tau K_d (\tau - \hat{\tau}) / (z-1) \tag{15}$$

Equation (15) may be written in standard form as

$$\hat{\tau} = (M/N) K_\tau K_d \tau / [z + ((M/N) K_\tau K_d - 1)] \tag{16}$$

Again, the impulse invariance conversion is related as

$$\exp(-\omega_\tau T_s) = - ((M/N) K_\tau K_d - 1); \tag{17}$$

and this yields

$$K_\tau = (4/K_d)\,(N/M)\,(B_\tau/R_s);$$ (18)

with the symbol timing closed loop time constant in symbol time units as

$$(\tau_\tau/T_s) = (K_d/4)\,(M/N)\,(R_s/B_\tau).$$ (19)

Carrier Phase Tracking Loop

The carrier phase loop is second order so it can track frequency as well as phase variations. A block diagram of the loop is depicted in Figure 5. It consists of a phase detector, two MACs (one for phase and one for frequency), a quadrature component generator, and a carrier phase rotator. As before, the input and multiplicative processing uses 8-bit resolution, whereas the phase and frequency accumulators employ 24-bits. The quadrature component generator table lookup uses the most significant 10-bits from the output phase estimate accumulator.

Carrier Phase Error Detector

The carrier phase detector response is described by

$$
\begin{aligned}
\Delta\theta_{2k} &= I_{2k}\hat{Q}_{2k} - Q_{2k}\hat{I}_{2k} \\
&= A_{2k}\,(i_{2k}\hat{Q}_{2k} - q_{2k}\hat{I}_{2k}) \\
&= K_d \sin(\theta_{2k} - \hat{\theta}_{2k})
\end{aligned}
$$ (20)

When the phase difference is sufficiently small, linear tracking results

$$\Delta\theta_{2k} = K_d\,(\theta_{2k} - \hat{\theta}_{2k})$$ (21)

Carrier Phase Closed Loop Transfer Function

The z-transform for the two accumulators is

$$\hat{\theta} = [K_\theta\,\Delta\theta/(z-1) + K_{\Delta\theta}\,\Delta\theta/(z-1)^2]$$ (22)

Substituting in equation (21) gives

$$\hat{\theta} = [K_\theta\,K_d\,(\theta - \hat{\theta})/(z-1) + K_{\Delta\theta}\,K_d\,(\theta - \hat{\theta})/(z-1)^2]$$ (23)

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D/A conversion and lowpass filtering, the sinusoidal samples were passed through a limiter to produce the properly phased clock waveform.

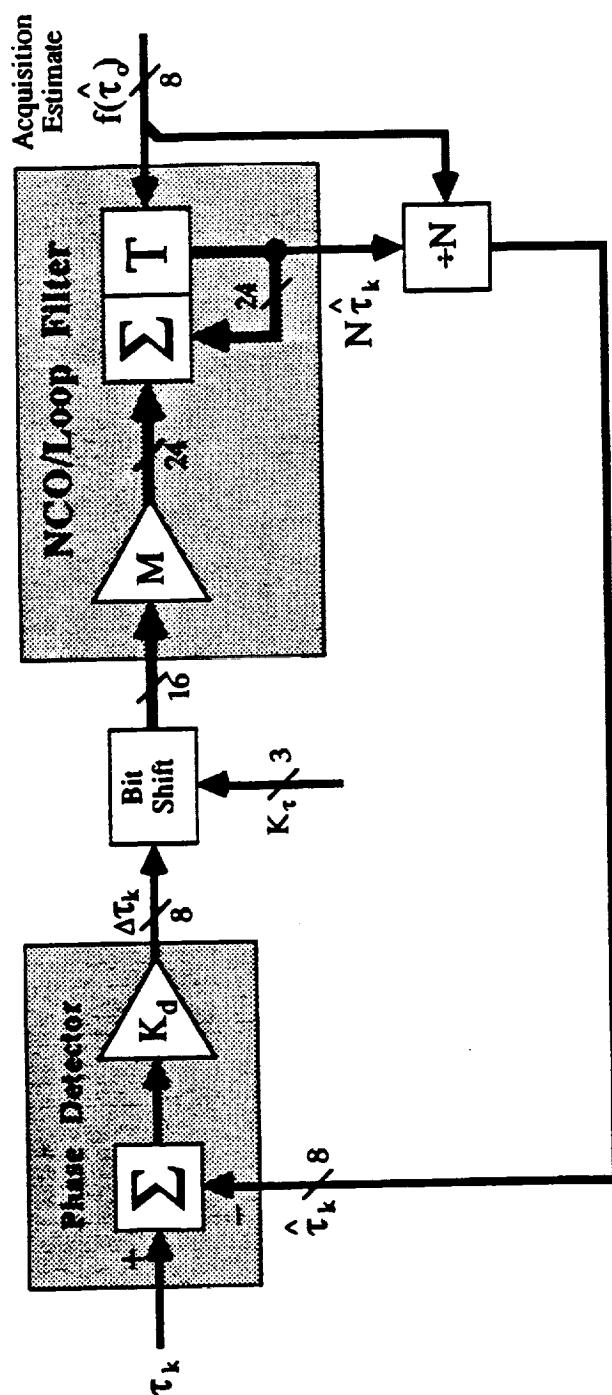

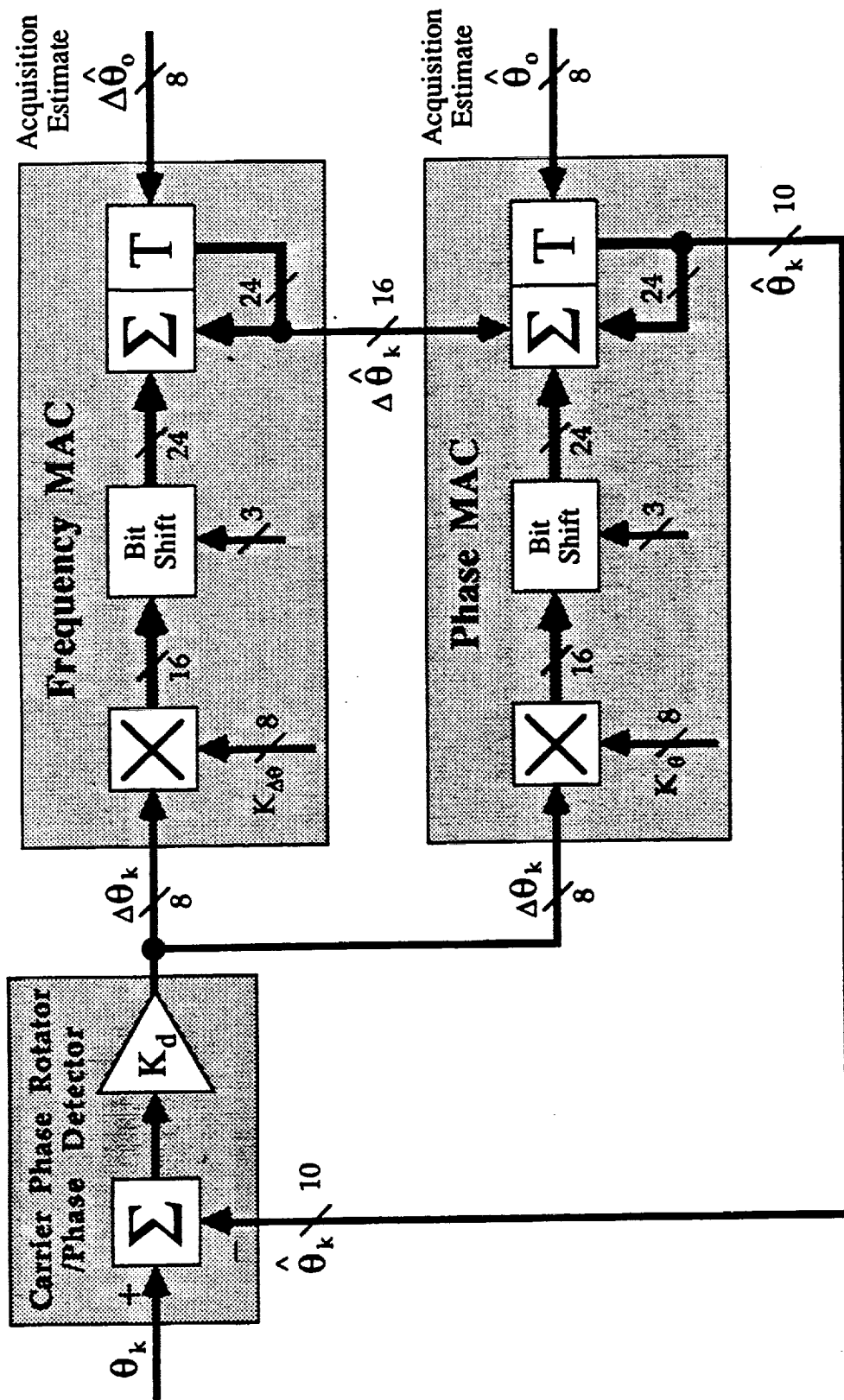*Figure 4. Symbol Timing Tracking Loop Model*

Figure 5. Carrier Phase Tracking Loop Model

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Grouping terms and rewriting equation (23) into a transfer function format yields

$$\hat{\theta}/\theta = [K_\theta K_d (z-1) + K_{\Delta\theta} K_d] / [(z-1)^2 + K_\theta K_d (z-1) + K_{\Delta\theta} K_d]$$

$$= K_d [K_\theta (z-1) + K_{\Delta\theta}] / [z^2 + z (K_\theta K_d - 2) + K_d (K_{\Delta\theta} - K_\theta) + 1] \quad (24)$$

Because the analysis of analog tracking loops is well known, the discrete-time response of equation (24) will be related to the analog transient response as follows. In standard second order notation, the complex roots in the analog s-domain are

$$s = -\omega_n (\zeta \pm j \sqrt{1 - \zeta^2}) \quad (25)$$

To preserve the closed loop phase stability predicted by the s-plane analysis, the impulse invariance transform of equation (10) is combined with equation (25) to give

$$z_{roots} = - \exp [-\omega_n T_s (\zeta \pm j \sqrt{1 - \zeta^2})] \quad (26)$$

Expanding equation (26) and equating it with the denominator of equation (24) yields two simultaneous equations for setting the carrier tracking loop parameters

$$K_d (K_{\Delta\theta} - K_\theta) + 1 = \exp (-2\zeta\omega_\theta T_s) \quad (27a)$$

$$K_\theta K_d - 2 = -2 \exp (\zeta\omega_\theta T_s) \cos [\omega_\theta T_s(\sqrt{1 - \zeta^2})] \quad (27b)$$

These equations may be expanded in series form as

$$K_d (K_{\Delta\theta} - K_\theta) + 1 = 1 - (2\zeta\omega_\theta T_s) + (2\zeta\omega_\theta T_s)^2/2 - \ldots \quad (28a)$$

$$K_\theta K_d - 2 = -2 [1 - (\zeta\omega_\theta T_s) + (\zeta\omega_\theta T_s)^2/2 - \ldots] [1 - (\omega_\theta T_s)^2 (1 - \zeta^2)/2 + \ldots] \quad (28b)$$

Recall that the sampling rate of these loops is one sample/symbol, and the closed loop bandwidths typically average sample values over hundreds of symbol times. Hence, $2\zeta\omega_\theta T_s \ll 1$, so equations (28) may be approximated with lower order terms as

$$K_d K_{\Delta\theta} = (\omega_\theta T_s)^2 \quad (29a)$$

$$K_d K_\theta = 2\zeta\omega_\theta T_s \quad (29b)$$

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For a second order tracking loop, the carrier noise equivalent bandwidth, B_θ is equated with the natural frequency, ω_θ by

$$B_\theta = [\zeta + 1/(4\zeta)] \, \omega_\theta/2$$

$$= 0.5303 \, \omega_\theta \tag{30}$$

when the damping ratio, $\zeta = 1/\sqrt{2}$. Then, equations (29) can be related in terms of the normalized ratio of symbol rate to bandwidth as

$$K_{\Delta\theta} = (3.556/K_d) \, (B_\theta/R_s)^2 \tag{31a}$$

$$K_\theta = (2.667/K_d) \, (B_\theta/R_s) \tag{31b}$$

EMULATION RESULTS

The transient responses of the three tracking loops was emulated as a means for validating the analysis. The tracking loop output estimate frequency domain quantization noise was also emulated to verify the hardware bit resolutions selected. Finally, the acquisiton and tracking behavior of the loops with additive white Gaussian noise (AWGN) was evaluated at very low SNR. Although the emulations were run for all of the two-dimensional modulation techniques described in the introductory section, space limitations dictate that only the QPSK results will be presented.

TRANSIENT RESPONSE

To evaluate the transient response of the tracking loops, the acquisition estimate injection was disabled. The first order AGC tracking loop has a normalized time constant of $R_s/4B_A$ symbol times, whereas the symbol timing loop is $R_s/2B_\tau$. Their respective transient responses are shown in Figures 6a, b for normalized design time contants of 75 and 150, respectively. The marks on the horizontal axes indicate the measured emulation time constants of approximately 80 and 130 symbol times. The agreement is actually very close considering that only 7-bits are available to quantize the gain coefficients over a relatively broad range of R_s/B. In addition, the AGC loop analysis was non-linear, and the symbol timing loop transient is pattern dependent; such that it is faster or slower depending on whether the probability for the localized groups of data transitions is greater or less than 0.5, respectively.
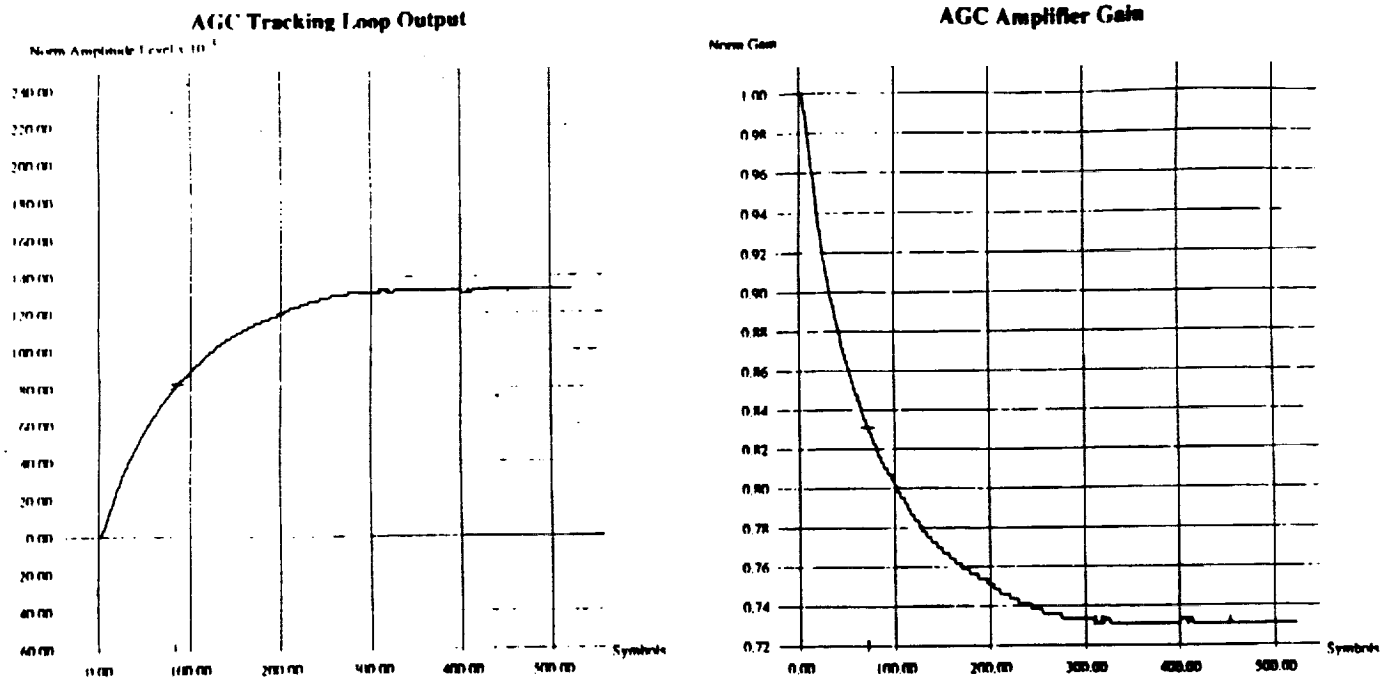
AGC Tracking Loop Output

AGC Amplifier Gain

Figure 6a. *AGC Tracking Loop Transient with Acquisition Estimate Disabled*

Symbol Timing Loop Output
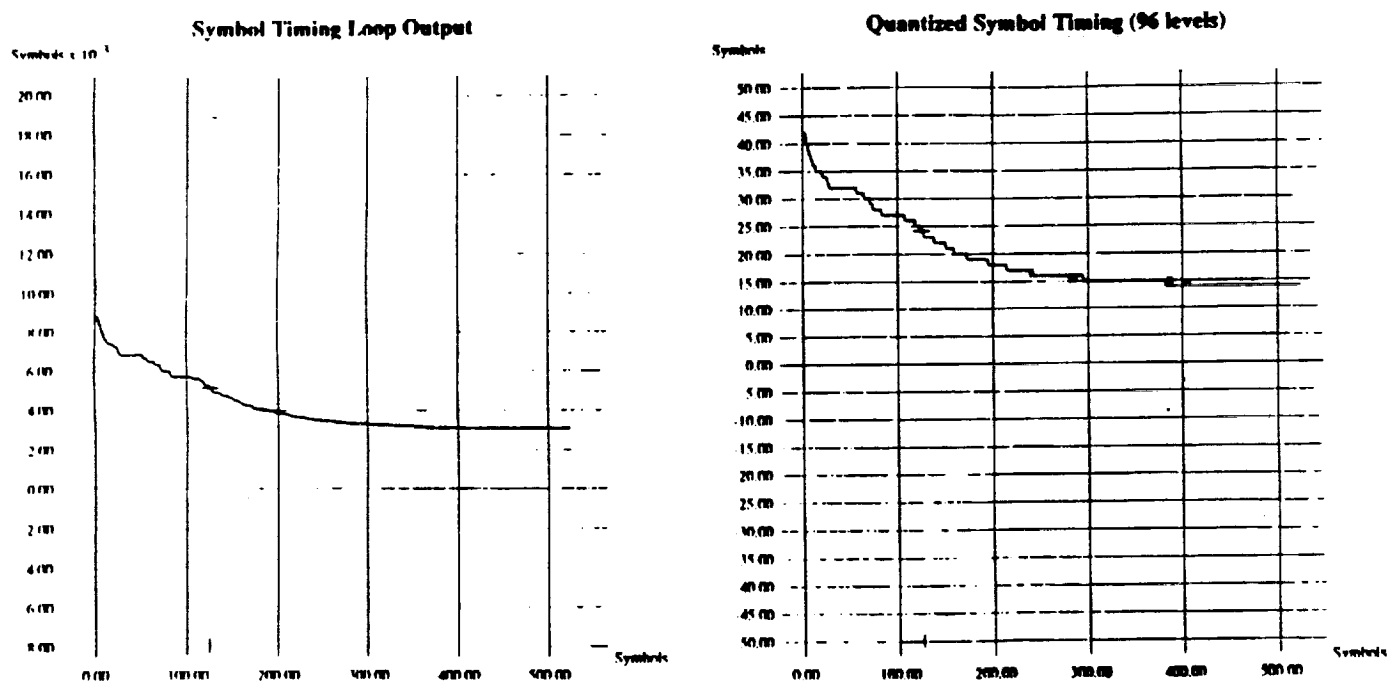
Quantized Symbol Timing (96 levels)

Figure 6b. *Symbol Timing Tracking Loop Transient with Acquisition Estimate Disabled*

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The second order carrier tracking loop transient is depicted in Figure 7. With the damping ratio, $\zeta = 1/\sqrt{2}$ the overshoot should be about 22% or 10°, and the first zero crossing of the transient should occur at 0.583 (R_s/B_θ) = 175 symbol times. The emulated values in the figure agree quite precisely with these predictions which are based on the analysis.
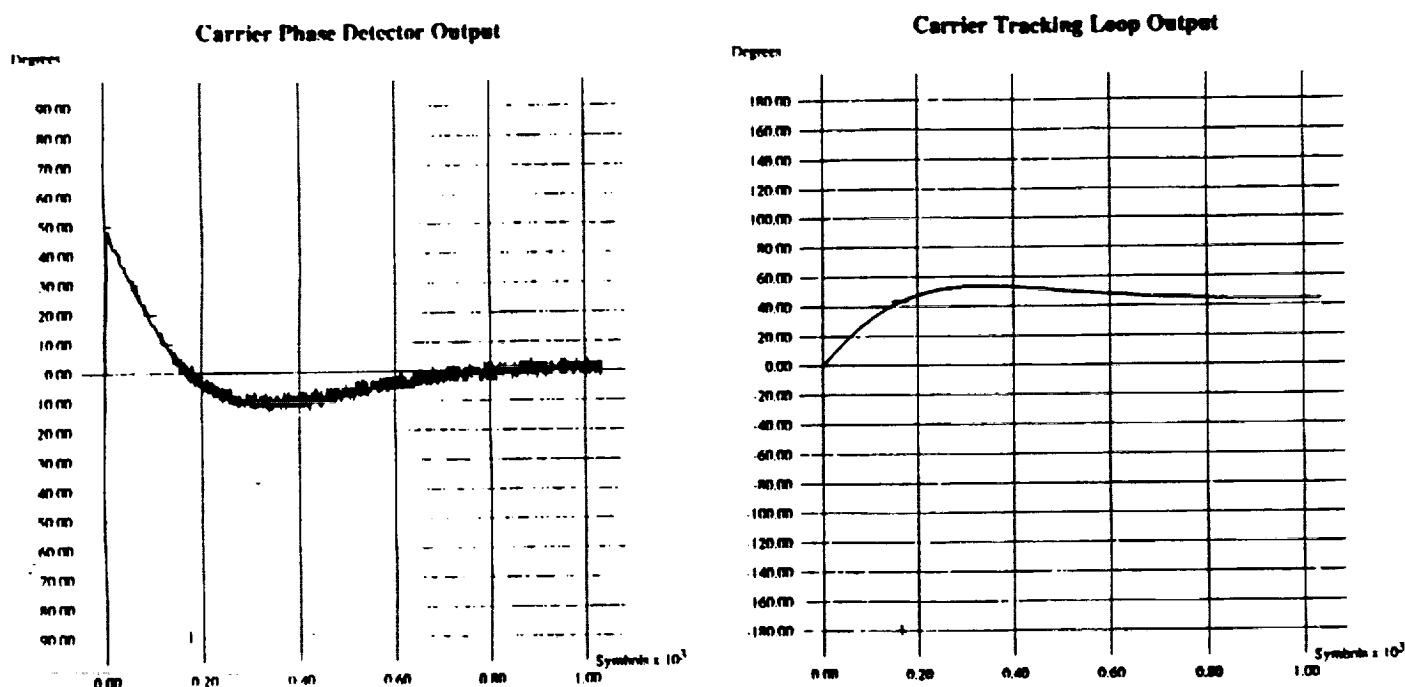
Figure 7. *Carrier Phase Tracking Loop Transient with Acquisition Estimate Disabled*

OUTPUT ESTIMATE QUANTIZATION NOISE

The worst case output estimate quantization noise is illustrated in Figures 8a, b, and c, for operation at the minimum symbol rate, 2.34375 Msps with no noise added. All three outputs are exceptionally pure and exhibit negligible quantization noise levels that are well below 40 dB.
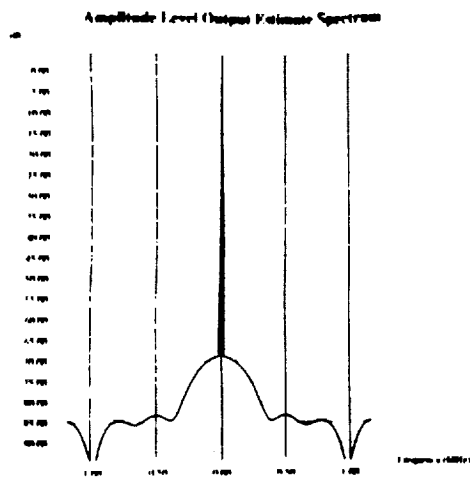
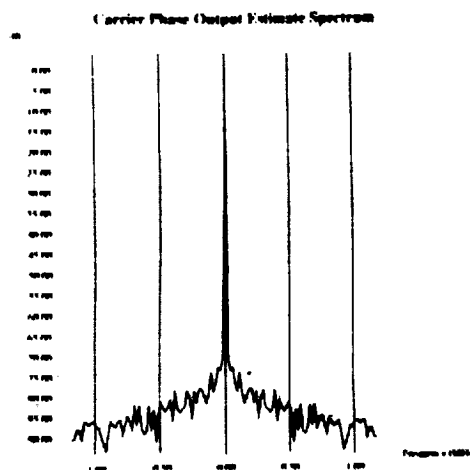*Figure 8a. AGC Tracking Loop Output Phase Noise*

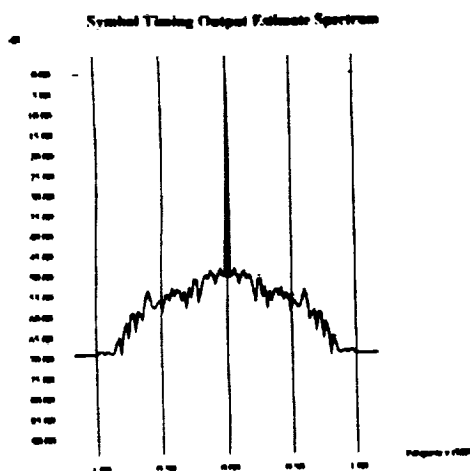*Figure 8b. Carrier Phase Tracking Loop Output Phase Noise*

Figure 8c. Symbol Timing Tracking Loop Output Phase Noise

MINIMUM SNR REQUIRED FOR ACQUISITION AND TRACKING

Tracking loop operation at low SNRs was evaluated by including AWGN in the emulation channel. The minimum SNR, rounded up to the nearest half dB, at which the demodulator could consistently acquire and track in burst mode is listed in Table 3. Because of the complexity of the emulation and the relatively long period of time it took to run a single data burst, these measurements were made on a burst-by-burst basis and as such cannot be directly related to a burst detection reliability.

Observe that the BERs are all on the order of 10^{-1}. This is due to the effect of data feedback, where the tracking loop SNR drops by approximately 3 dB when the BER = 1.5 e-1. That is, 85% of the feedback is correct, and 15% drives the loop in the wrong direction.

Table 3. Minimum SNR for Acquisition and Tracking

Mod. Technique	E_b/N_o	BER	Preamble Length
BPSK	0.0	1.0 e-1	32
QPSK	0.0	1.0 e-1	64
Offset-QPSK	1.5	1.2 e-1	64
8-PSK	4.0	1.3 e-1	96
16-QAM	2.5	1.6 e-1	112
16-PSK	5.0	2.2 e-1	144

The three time-domain tracking loop outputs are shown in Figures 9a, b, and c, for E_b/N_o = 0 dB. Observe that there is little discernable noise on their outputs with the exception of the symbol timing, which has been amplified by a factor of 1024/96 relative to the actual design output level, because of limitations in the emulation run time.
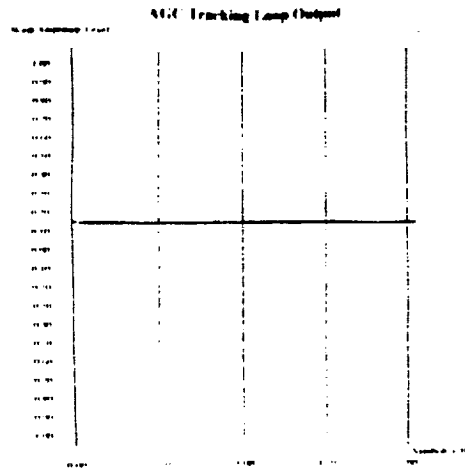
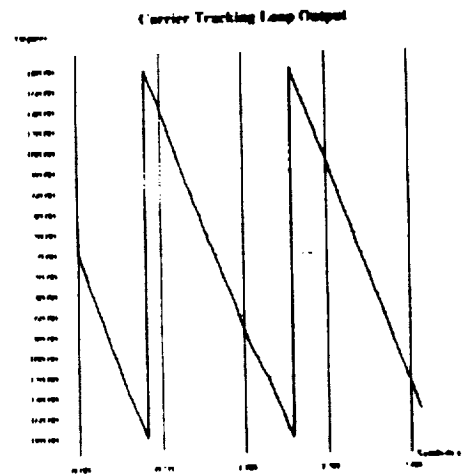*Figure 9a. AGC Tracking Loop Output Estimate*

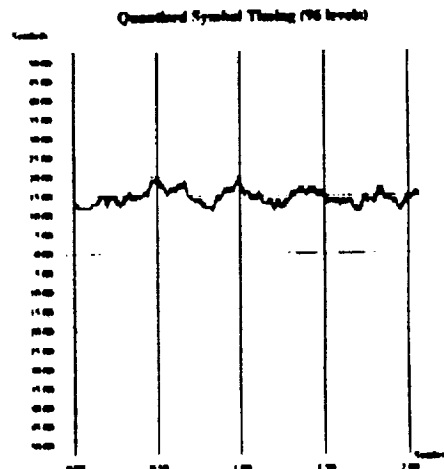*Figure 9b. Carrier Phase Tracking Loop Output Estimate*

Figure 9c. Symbol Timing Tracking Loop Output Estimate

CONCLUSIONS

The tracking loop architecture based on the JED approach does indeed perform very well for a broad class of modulation techniques. The analysis is quite accurate in setting the loop parameters as well as predicting their transient behavior. Both acquisition and tracking performance abruptly degrade at BERs on the order of 10^{-1} as a result of an effective reduction in loop SNR through errors in the data feedback. It was not possible to run emulations over a large number of bursts because a single burst required on the order of 10 minutes to process. Although the measurements presented in this paper were confined to QPSK signalling, the measured results were analogous for all of the two-dimensional modulation techniques mentioned in the introduction.

ACKNOWLEDGMENTS

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13. ABSTRACT (Maximum 200 words)

In this paper, an analysis and hardware emulation of the tracking loops for a very flexible programmable digital modem (PDM) will be presented. The modem is capable of being programmed for 2, 4, 8, 16-PSK, 16-QAM, MSK, and Offset-QPSK modulation schemes over a range of data rates from 2.34 to 300 Mbps with programmable spectral occupancy from 1.2 to 1.8 times the symbol rate; and these operational parameters are executable in burst or continuous mode. All of the critical processing in both the modulator and demodulator is done at baseband with very high-speed digital hardware and memory. Quadrature analog front-ends are used for translation between baseband and the IF center frequency. The modulator is based on a table lookup approach, where precomputed samples are stored in memory and clocked out according to the incoming data pattern. The sample values are predistorted to counter-act the effects of the other filtering functions in the link as well as any transmission impairments. The demodulator architecture has been adapted from a joint estimator-detector (JED) mathematical analysis. Its structure is applicable to most signalling formats that can be represented in a two-dimensional space. The JED realization uses interdependent, mutually aiding tracking loops with post-detection data feedback. To expedite and provide for more reliable synchronization, initial estimates for these loops are computed in a parallel acquisition processor. The cornerstone of the demodulator realization is the pre-averager received data filter which allows operation over a broad range of data rates without any hardware changes, and greatly simplifies the implementation complexity. The emulation results confirmed tracking loop operation over the entire range of operational parameters listed above, as well as the capability of achieving and maintaining synchronization at BERs in excess of 10^{-1}. The emulation results also showed very close agreement with the tracking loop analysis, and validated the resolution apportionment of the various hardware elements in the tracking loops.

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