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Microwave Characterization of Slotline on High Resistivity Silicon for Antenna Feed Network

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MICROWAVE CHARACTERIZATION OF SLOTLINE ON HIGH RESISTIVITY

SILICON FOR ANTENNA FEED NETWORK

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ABSTRACT

This paper presents, the effective dielectric constant (ε_{eff}) and attenuation constant (α) of a unshielded slotline on a high resistivity (5000 to 10,000 Ω-cm) silicon wafer. The ε_{eff} (DC to 40 GHz) and α (DC to 26.5 GHz) are determined from the measured resonant frequencies and the corresponding insertion loss of a slotline ring resonator. The measurements are carried out at room temperature and without the application of a DC bias. The attenuation for slotline on silicon are compared with microstrip line and coplanar waveguide on other semiconductor substrate materials. Finally, applications of the slotline to antenna feed network are addressed.

I. INTRODUCTION

There are several reasons why silicon is now a viable microwave material. One reason is that silicon MOSFET's with cutoff frequencies as high as 89 GHz have been reported (ref.1). Another, is that silicon MMIC amplifiers, mixers and IMPATT diodes are now commericially available (refs. 2 thru 4). The final reason is that transmission lines, such as, microstrip line (refs. 5 thru 9) and Coplanar Waveguide (CPW) (ref. 10) with low loss have been demonstrated on high resistivity silicon. Silicon has several advantages over GaAs and InP technologies, such as: better thermal conductivity, higher reliability, higher circuit complexity, availability of wafers of very large diameters, better mechanical properties, and lower cost (ref. 9). Furthermore, integration of MMIC's with digital control circuits and radiating elements on a single silicon wafer is possible. This can enhance the reliability, efficiency and lower the cost of phased array antenna systems. However, silicon substrates do have slightly higher dielectric loss than traditional microwave substrates. DC bias and high operating temperatures can increase this loss. Additional loss can be introduced, if during processing, the wafers are exposed to temperatures high enough to significantly lower their resistivity (ref. 9).

Conventional silicon wafers have low resistivity and consequently an unacceptably high value of dielectric attenuation. Therefore, microwave circuits for phased array antenna systems fabricated on these wafers have low efficiency. By choosing a silicon substrate with sufficiently high resistivity it is possible to make the dielectric attenuation of the interconnecting microwave transmission lines approach those of GaAs or InP (refs. 6 and 7).

In order to fabricate microwave circuits on silicon, the transmission lines on this material must be characterized. Recently, the attenuation of microstrip transmission lines on high resistivity, bare and passivated silicon as a function of frequency, temperature and DC bias have been measured (ref. 9). Also, attenuation and ε_{eff} of CPW lines as a function of resistivity, frequency and geometry on silicon substrates has been examined experimentally and theoretically (ref. 10). This paper presents the effective dielectric constant (ε_{eff}) and attenuation constant (α) of an unshielded slotline on a high resistivity (5000 to 10,000 Ω-cm) silicon wafer over the frequency ranges DC to 40 GHz and DC to 26.5 GHz respectively. The measurements are carried out at room temperature and without the application of a DC bias.

II. THEORY

An experimental slotline ring resonator is shown in figure 1. The advantage of a ring resonator over a series gap coupled linear resonator is that the ring resonator is free of end effects. The loaded Q-factor, Q_L, of the resonator is determined from the following equation relating the measured resonance frequency, f_0, and the frequency range, Δf, between the 3-dB points on either side of the resonance:

$$Q_L = f_0 / \Delta f. \tag{1}$$

The unloaded Q-factor, Q_u, of the resonator is determined from the following equation relating the measured peak insertion loss, L, at resonance and Q_L:

$$L\ (dB) = 20 \text{ Log } \{1 - [Q_L/Q_u]\}. \tag{2}$$

The ε_{eff} is determined from the following equation:

$$\varepsilon_{eff} = (30\ n/f_0\ l)^2 \tag{3}$$

Where n is an integer and denotes the order of resonance. Therefore for n resonances of a particular resonator, n values of ε_{eff} can be obtained. l is the mean circumference of the ring in cm. f_0 is in GHz.

The phase velocity, v_{ph}, of the electromagnetic wave on the slotline is equal to

$$v_{ph} = 3 \times 10^8 / \sqrt{\varepsilon_{eff}} \quad (mt/sec). \tag{4}$$

Finally, the attenuation constant α of the slotline is determined from the relation:

$$\alpha = \pi\ f_0 / Q_u\ v_{ph} \quad (Np/mt). \tag{5}$$

III. RESONATOR FABRICATION AND EXPERIMENTAL RESULTS

The slotline ring resonator is fabricated on a silicon wafer which is coated sequentially with 700 Å of silicon dioxide, 200 Å of chromium and 2.5 μm of gold. The thickness, T, of the gold metalization is greater than three times the skin depth at 8.5 GHz and above. The measured resistivity of the silicon dioxide layer is 10^{14} Ω-cm. The ε_{eff} and α are determined by substituting the measured resonant frequencies and the corresponding insertion loss in equations 1 thru 5. Figure 2 presents the ε_{eff} as a function of the frequency. In this figure the slot width W, wafer thickness D, and relative dielectric constant ε_r, are equal to 0.1 mm, 0.381 mm and 11.7, respectively. Also shown in Fig.2 is the computed ε_{eff} which is obtained as described in ref.11. The measured and computed ε_{eff} are in good agreement.

The intrinsic peak insertion loss L of the resonator is corrected for the insertion loss due to the microstrip feed lines and the coaxial connectors of the fixture. This is done by subtracting the feed and connector loss from the overall measured insertion loss. These excess losses are determined from a separate set of measurements using a thru line of length equal to the sum of the feed line lengths in the test fixture. Figure 3 presents the measured attenuation α as a function of the frequency. The W, D and ε_r of the slotline are the same as those in Fig. 2. The attenuation of slotline is compared in Table 1 with the measured results from the open literature for microstrip line and coplanar waveguide on various other semiconductor substrate materials. It is worth mentioning here that the attenuation values quoted in Table 1 depend on the substrate thickness, metalization thickness and also the strip conductor width and/or slot width which are not the same in all cases.

IV. CONCLUSIONS AND DISCUSSIONS

The ε_{eff} and α for a slotline on a high resistivity silicon substrate have been experimentally obtained. The attenuation constant for slotline has been compared with that of microstrip line and coplanar waveguide on other semiconductor substrate materials. The value of attenuation for slotline was found to be comparable to other transmission lines. This, however, can only be a rough comparison because attenuation depends upon the substrate thickness, metalization thickness and strip conductor width and/or slot width which are not the same in all the cases. However our experiments demonstrate the viability of high resistivity silicon for low loss antenna feed network. Application of this information to the feed network will be presented at the symposium.

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TABLE 1
Comparision of Attenuation Constant of Microwave Transmission Lines on Semiconductor Substrates

TRANSMISSION LINE	SUBSTRATE MATERIAL	DIMENSIONS (Inch)	ATTENUATION @ 10 GHz (dB/cm)	REFERENCE
Microstrip ($Z_0 = 50\ \Omega$)	SI GaAs	D = 0.025 W = 0.025 T = 3 μm*	0.105	12
Coplanar Waveguide (CPW) ($Z_0 \approx 50\ \Omega$)	SI GaAs	D = 0.025 S = 0.025 W = 0.0125 T = 3 μm*	0.16	12
Coplanar Waveguide (CPW)[1] ($Z_0 \approx 35\ \Omega$)	SI InP	D = 0.5 mm S = 88 μm W = 16 μm T = 0.25 μm*	4.5	14
Coplanar Waveguide (CPW) ($Z_0 = 50\ \Omega$)	SI GaAs	D = 0.5 mm S = 75 μm W = 56 μm T = 3 μm*	0.45	13
Microstrip ($Z_0 = 50\ \Omega$)	High Res. silicon (1.5 k Ω-cm)	D = 0.01 W = 0.006$	0.5	5
Microstrip ($Z_0 \approx 50\ \Omega$)	High Res. Silicon (8 k Ω-cm)	D = 0.021 W = 0.016 T ≈ 3 μm	0.16	9
Coplanar Waveguide (CPW)[2] ($Z_0 \approx 50\ \Omega$)	High Res. Silicon (2.5 - 3.3 k Ω-cm)	D = 0.008 S = 0.004 W = 0.002 T = 2.5 μm*	0.62	10
Coplanar Waveguide (CPW)[2] ($Z_0 \approx 60\ \Omega$)	High Res. Silicon (4 k Ω-cm)	D = 400 μm S = 30 μm W = 35 μm T = 1 μm$	3	8
Slotline[2] ($Z_0 = 60\ \Omega$)	High Res. Silicon (5 - 10 k Ω-cm)	D = 0.015 W = 0.004 T = 2.5 μm*	0.25	This work

D is substrate thickness and T is metalization thickness
Microstrip: W is strip width
Coplanar Waveguide: S is center strip width and W is slot width
[1]Metal thickness less than one skin depth
[2]A SiO_2 interfacial layer is present
*Gold conductors, $Aluminium conductors

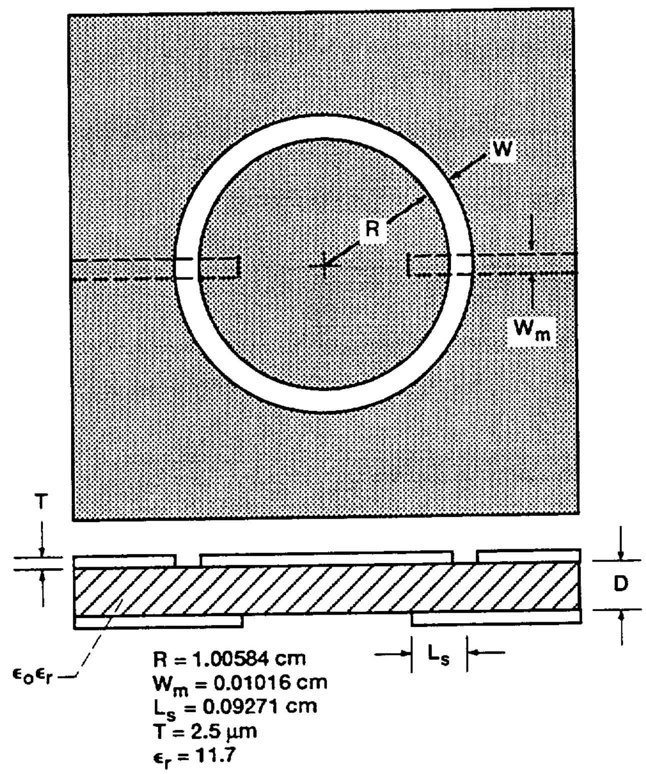

Figure 1.—Slotline ring resonator electromagnetically coupled to microstrip feed lines.

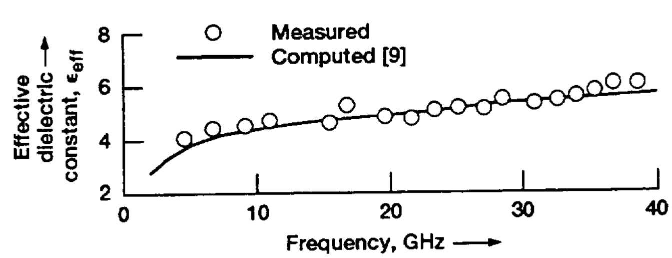

Figure 2.—Effective dielectric constant.

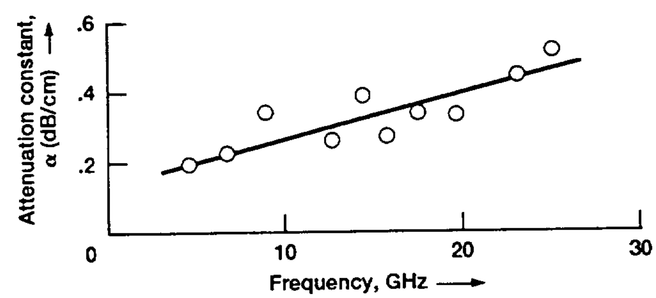

Figure 3.—Attenuation constant.

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13. ABSTRACT ***(Maximum 200 words)***

Conventional silicon wafers have low resistivity and consequently unacceptably high value of dielectric attenuation constant. Microwave circuits for phased array antenna systems fabricated on these wafers therefore have low efficiency. By choosing a silicon substrate with sufficiently high resistivity it is possible to make the dielectric attenuation constant of the interconnecting microwave transmission lines approach those of GaAs or InP. In order for this to be possible, the transmission lines must be characterized. In this presentation, the effective dielectric constant (ε_{eff}) and attenuation constant (α) of a slotline on high resistivity (5000 to 10 000 Ω-cm) silicon wafer will be discussed. The ε_{eff} and α are determined from the measured resonant frequencies and the corresponding insertion loss of a slotline ring resonator. The results for slotline will be compared with microstrip line and coplanar waveguide.

14. SUBJECT TERMS
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