ELECTRONIC NEURAL NETWORKS

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ELECTRONIC NEURAL NETWORKS

JET PROPULSION LABORATORY

BACKGROUND

- NEURAL NETWORKS OFFER A TOTALLY NEW APPROACH TO INFORMATION PROCESSING THAT IS ROBUST, FAULT-TOLERANT, AND FAST.
- MODELS OF NEURAL NETWORKS ARE BASED ON HIGHLY PARALLEL AND DISTRIBUTIVE ARCHITECTURES.
- JPL IS DEVELOPING ELECTRONIC IMPLEMENTATIONS OF ARTIFICIAL NEURAL NETWORKS TO EXPLOIT THEIR EMERGENT PROPERTIES FOR "INTELLIGENT" KNOWLEDGE ENGINEERING APPLICATIONS.
- IN AN ELECTRONIC EMBODIMENT, "NEURONS" ARE REPRESENTED BY THRESHOLD AMPLIFIERS, AND "SYNAPSES" BY RESISTORS. INFORMATION IS STORED IN THE VARYING STRENGTHS OF SYNAPTIC CONNECTIONS.
- ELECTRONIC IMPLEMENTATIONS OF APPLICATION – SPECIFIC HIGH SPEED NEUROPROCESSORS FOR:
  - ASSOCIATIVE RECONSTRUCTION
  - CARTOGRAPHIC ANALYSIS
  - RESOURCE ALLOCATION
  - GLOBAL OPTIMIZATION
  - AUTONOMOUS CONTROL

INTRODUCTION

- ARTIFICIAL NEURAL NETWORKS :
  - MASSIVELY PARALLEL ARCHITECTURES INSPIRED BY THE NATURE'S APPROACH TO INTELLIGENT INFORMATION PROCESSING
- KEY QUESTIONS :
  - WHAT GOOD ARE THEY ?
  - CAN THEY DO SOMETHING UNIQUE FOR SPACE STATION ?
  - WHEN WILL THEY DELIVER ?

NUMBERS !

- A HUMAN BRAIN HAS OVER 10^{10} NEURONS AND 10^{14} SYNAPSES.
- HARDWARE IMPLEMENTATIONS TODAY ARE AT ABOUT 10^{3} NEURONS AND 10^{5} SYNAPSES.

BUT

- THE BRAIN IS NOT FULLY CONNECTED !
- THE CURRENT ARTIFICIAL NEURAL NETWORKS ARE ALREADY PROVING THEMSELVES EXTREMELY USEFUL.
- NEURAL NETWORKS ARE NOT GENERAL PURPOSE COMPUTERS. THEY ARE SPECIAL-PURPOSE HIGH PERFORMANCE CO-PROCESSORS.

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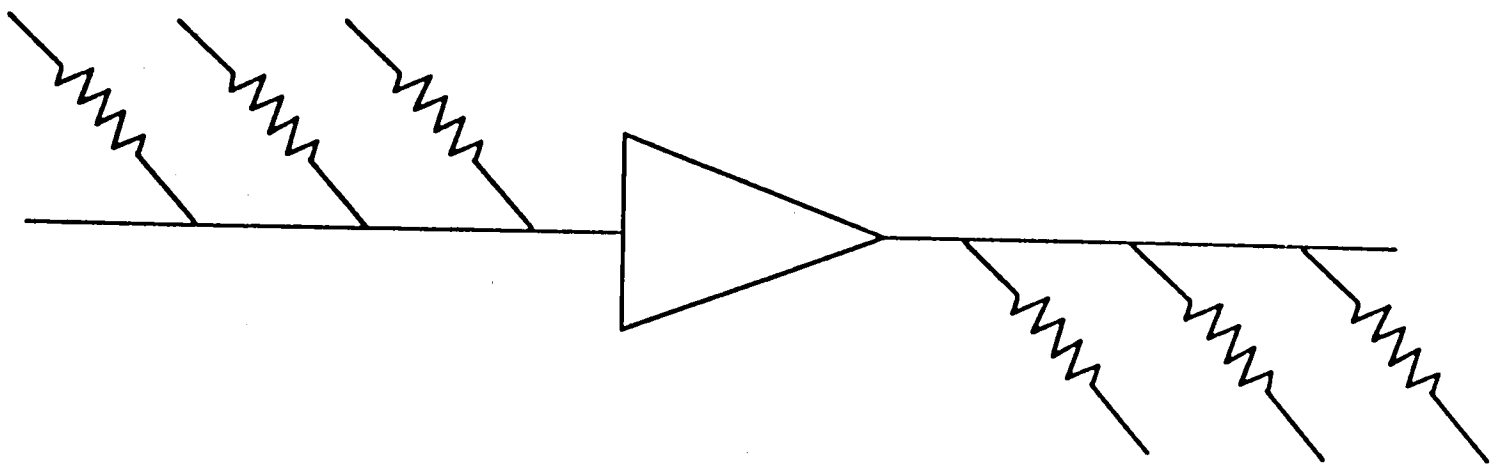
NEURAL NETWORK

BASIC COMPONENTS: NEURONS

SYNAPSES

ELECTRONIC IMPLEMENTATION:



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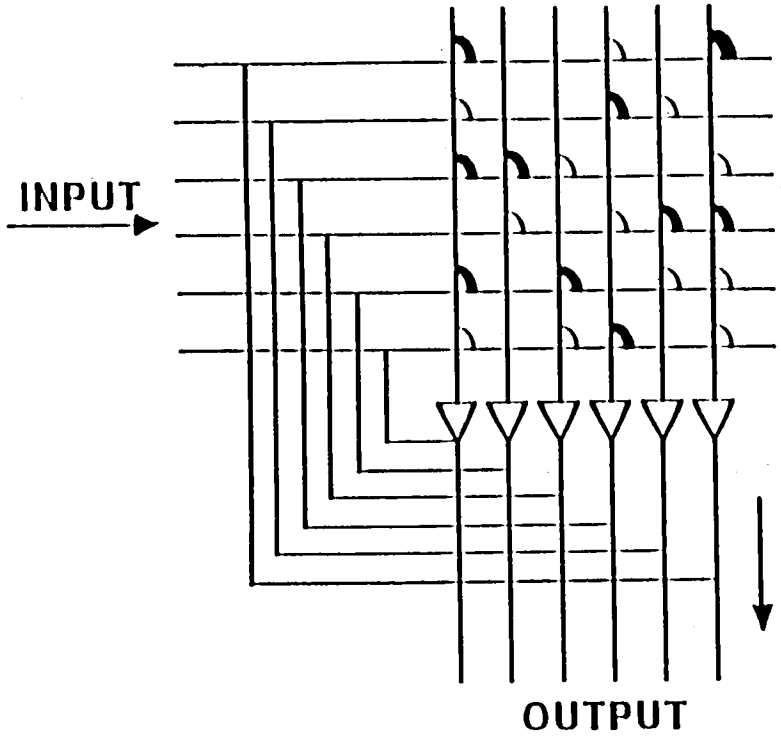
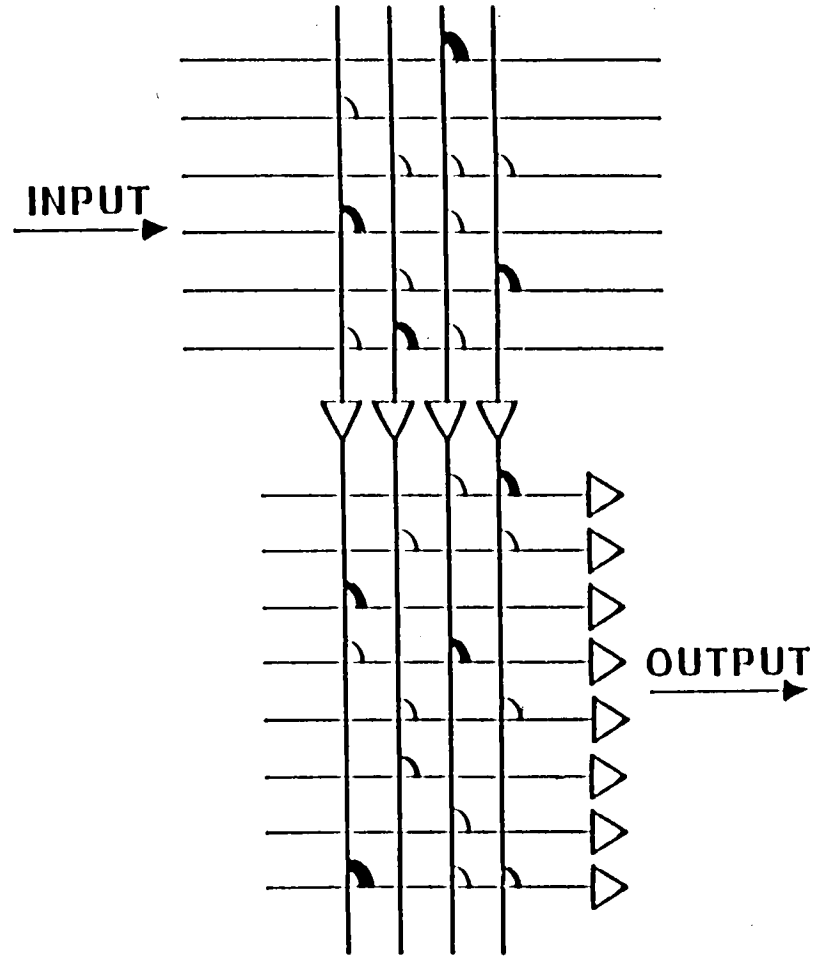
NEURAL NETWORK ARCHITECTURES



FEEDBACK NETWORK

$$C_i \frac{du_i}{dt} = \sum T_{ij} V_j - \frac{u_i}{R_i} + I_i$$



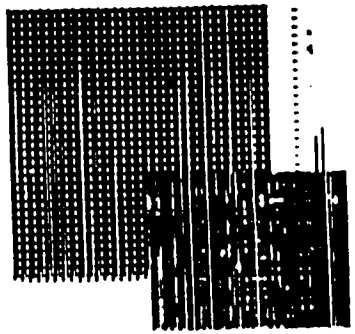
FEEDFORWARD, LAYERED

ELECTRONIC IMPLEMENTATIONS

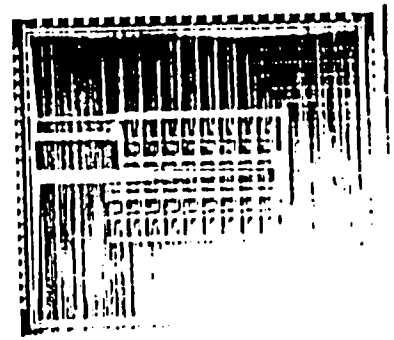
- JPL'S APPROACH HAS BEEN:
  - TO DEVELOP NEURAL NET "BUILDING BLOCKS" FOR MODULAR HARDWARE
  - TO VERIFY DESIGN OF NEUROCIRCUITS IN SIMULATION
  - TO TAILOR "NEUROPROCESSORS" FOR SELECTED APPLICATIONS
- TECHNOLOGIES:
  - VLSI: CMOS, BIPOLAR, AND EEPROM (FLOATING GATE)
  - THIN FILM: AMORPHOUS SEMICONDUCTORS, ELECTROCHROMIC MATERIALS, AND CHEMICAL MICROSWITCHES
  - HYBRID: VLSI/THIN FILM, SINGLE/MULTI-CHIP, WAFER-LEVEL INTEGRATION

VLSI/THIN FILM HYBRID HARDWARE FOR NEUROCOMPUTING

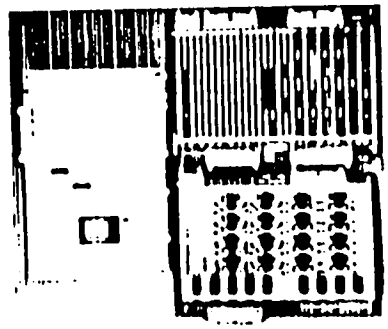
1024 CAPACITOR-REFRESH, ANALOG SYNAPSE CHIP



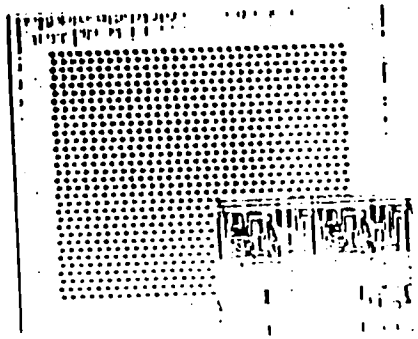
17-NEURON ARRAY CHIP



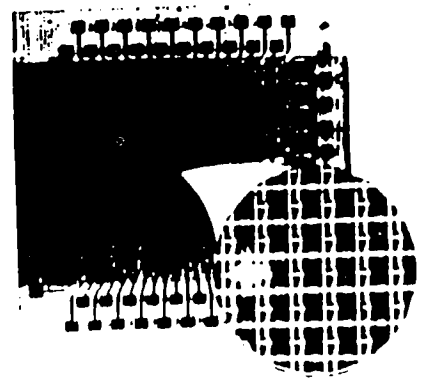
A NEURO-PROCESSOR



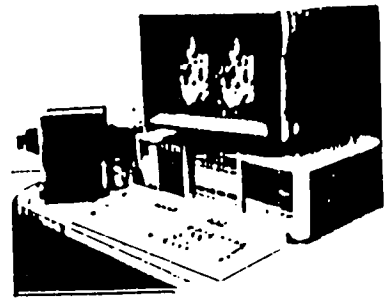
32 x 32 BINARY SYNAPSE CHIP



HIGH DENSITY, THIN FILM SYNAPTIC ARRAY



A NEURAL-DIGITAL HYBRID COMPUTER SYSTEM



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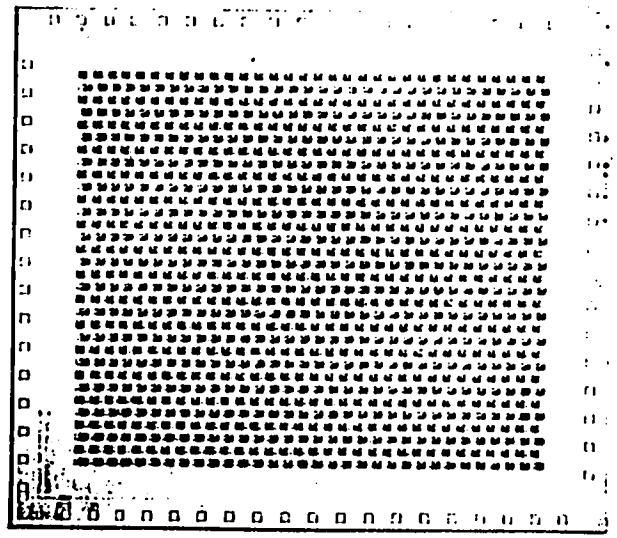
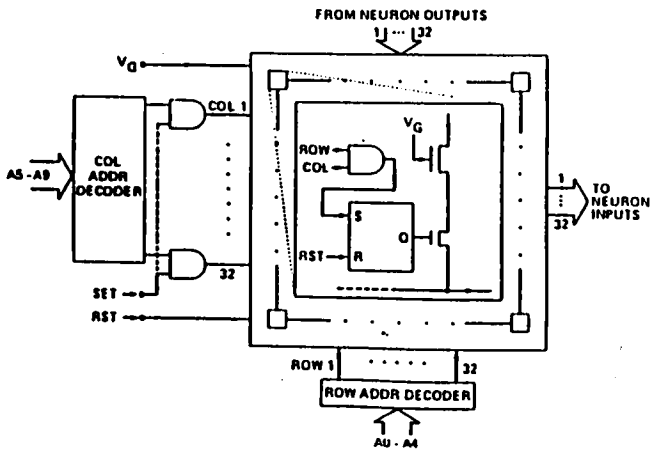
CASCADABLE, PROGRAMMABLE, 32 × 32 SYNAPTIC CMOS CHIP





- A BUILDING BLOCK FOR VLSI NEURAL NET HARDWARE
- PROVIDES OVER 10^9 ANALOG OPERATIONS/SEC
- POTENTIAL APPLICATIONS:
  - — MULTI SENSOR DATA FUSION
  - — ASSOCIATIVE RECONSTRUCTION
  - — PATTERN RECOGNITION

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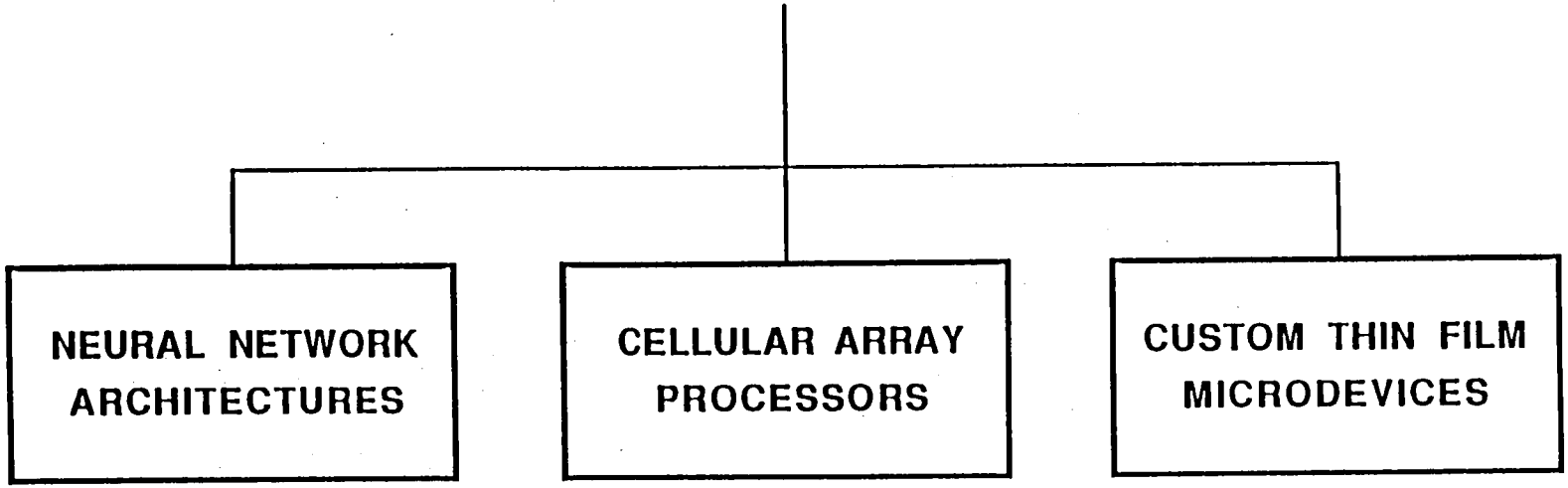
COMPUTATION WITH ANALOG PARALLEL PROCESSING



- ASSOCIATIVE MEMORY
- AUTONOMOUS CONTROL
- GLOBAL OPTIMIZATION
- CARTOGRAPHIC ANALYSIS

- PATH PLANNING
- RESOURCE ALLOCATION

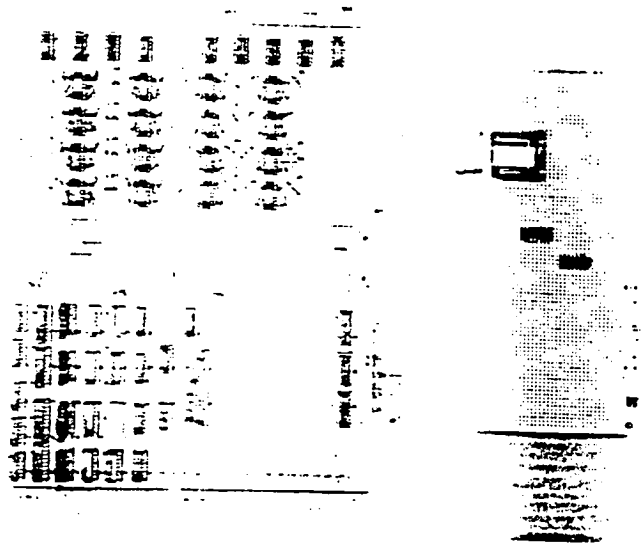
- HIGH-DENSITY INTERCONNECTIONS
- NON-VOLATILE ANALOG MEMORIES

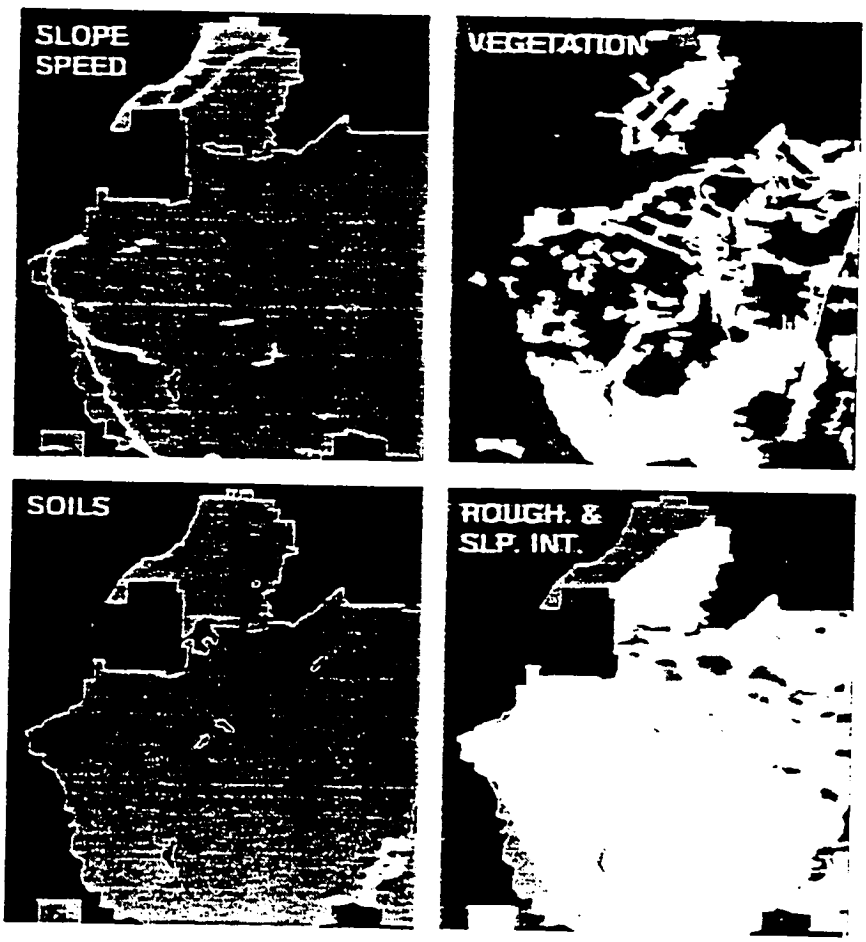
FEATURES OF NEUROPROCESSORS

- APPLICATION-SPECIFIC ARCHITECTURES
- FINE-GRAIN, MASSIVELY PARALLEL, ANALOG, ASYNCHRONOUS PROCESSING
- EXTREMELY HIGH SPEED : TERRA-OPS RANGE
- INHERENT FAULT-TOLERANCE
- UNIQUE CAPABILITIES TO "LEARN" FROM EXPERIENCE AND SELF-ORGANIZE
- TRULY ENABLING NATURE, COMPLEMENTING THE ABILITIES OF HIGH SPEED DIGITAL MACHINES

APPLICATIONS OF NEUROPROCESSORS

- AUTOMATION AND ROBOTICS
- ON-BOARD, REAL-TIME, GLOBAL OPTIMIZATION
    - ALLOCATION AND MANAGEMENT OF RESOURCES
- AUTONOMOUS, SCHEDULING, SEQUENCING, AND EVENT-DRIVEN MISSION REPLANNING
- SCIENCE DATA ANALYSIS AND MANAGEMENT
    - PATTERN RECOGNITION, CLASSIFICATION
    - MODELING OF LARGE SYSTEMS
    - CODING, DECODING, ASSOCIATIVE RECONSTRUCTION FROM CORRUPT DATA





A set of four [illegible] each color represents a parti[illegible]

Neural network classification results. Each color denotes a particular decision or classification for a pixel, e.g., green = "GO", yellow = "GO SLOW", orange = "GO VERY SLOW", and red = "NO GO".

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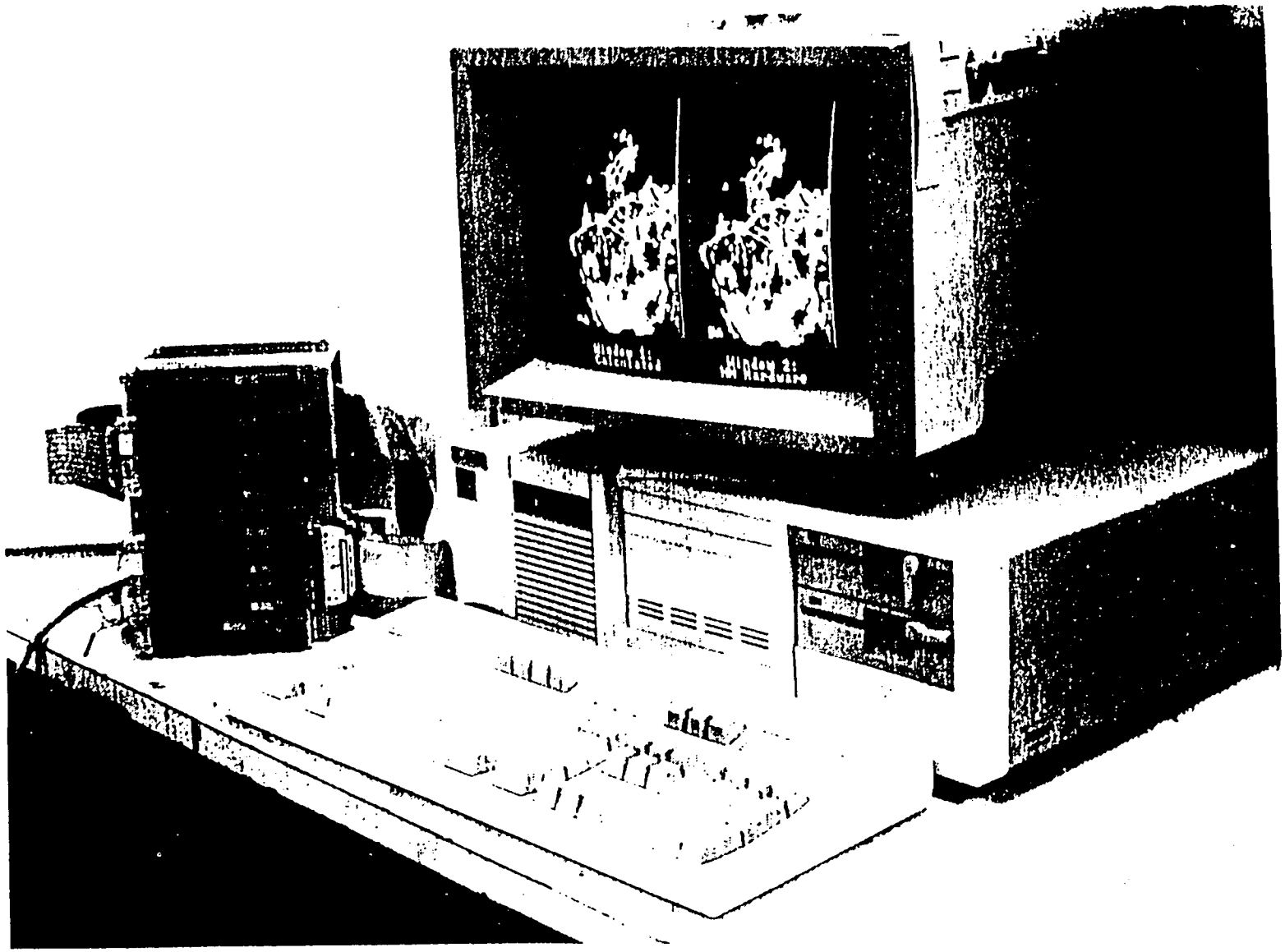
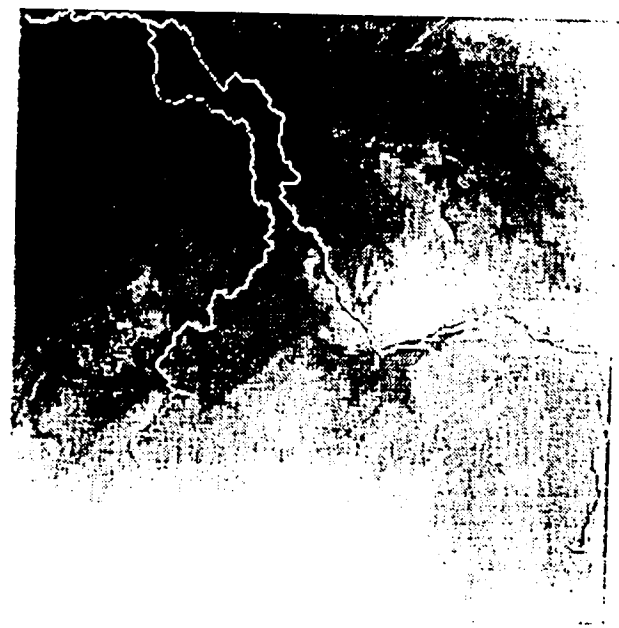
NEURAL NETWORK HARDWARE FOR TERRAIN TRAFFICABILITY DETERMINATION



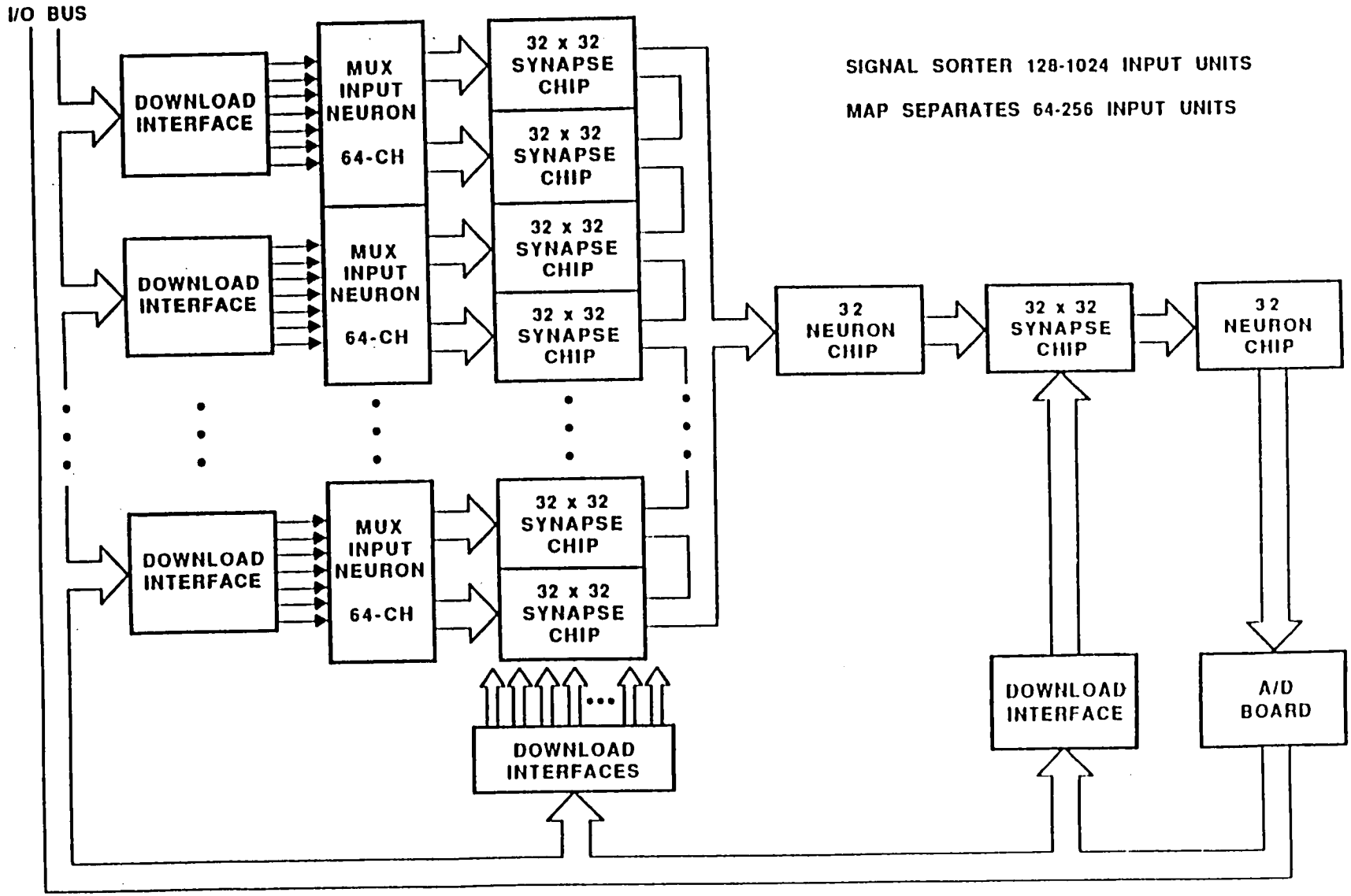
A DEDICATED PROCESSOR FOR PATH PLANNING

- MASSIVELY PARALLEL, ANALOG, ASYNCHRONOUS PROCESSING
- ACCEPTABLE SOLUTION IN REAL TIME, THAN THE BEST SOLUTION AFTER A LONG TIME
- ORDERS OF MAGNITUDE SPEED IMPROVEMENT, PARTICULARLY FOR "WHAT IF" EXPERIMENTS

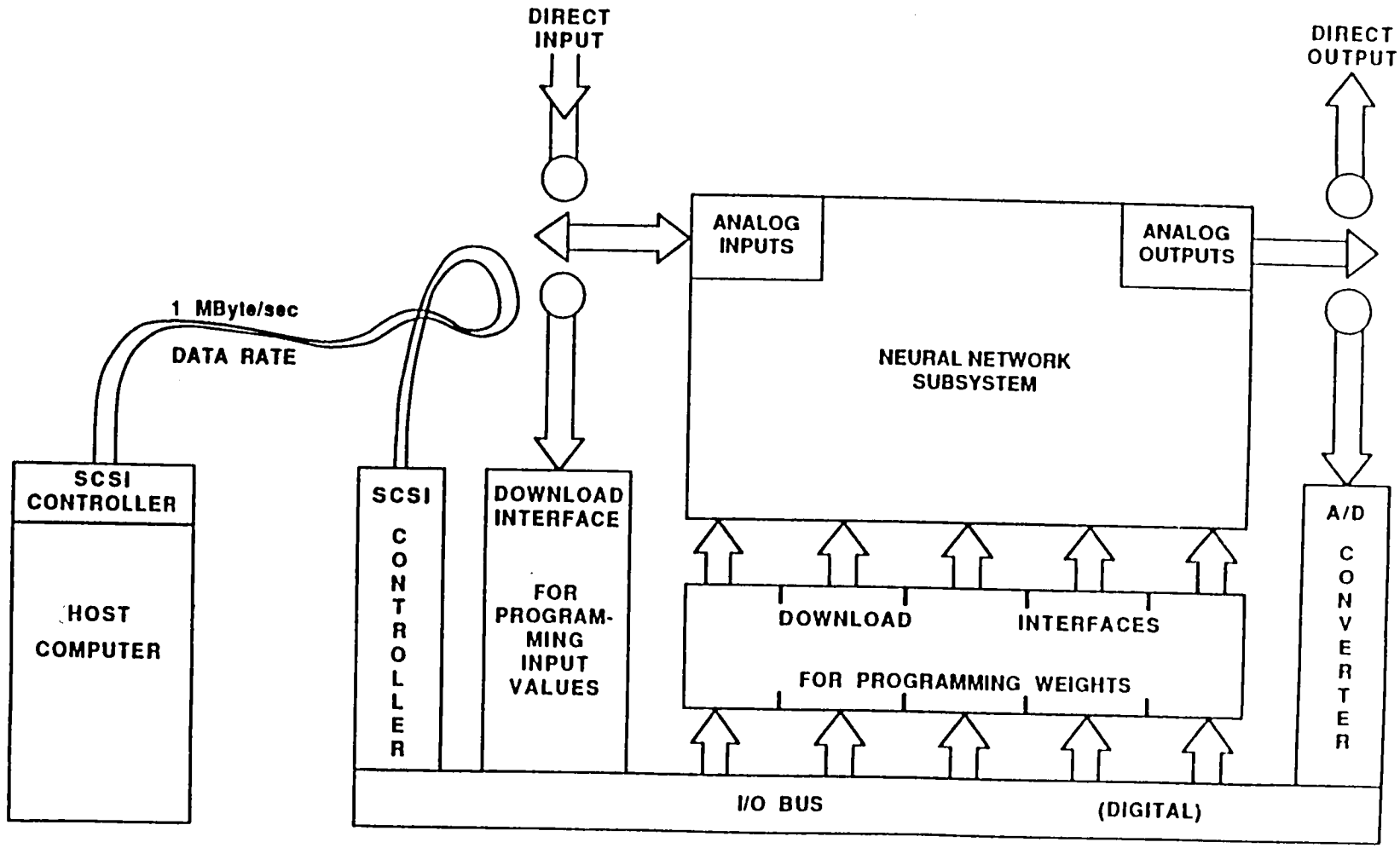
PATH COMPUTATION



HARDWARE DETAIL FOR SIGNAL SORTER AND MAP SEPARATES APPLICATIONS



JPL NEURAL NETWORK SYSTEM INTERFACE



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ELECTRONIC NEURAL NETWORKS
RAPID HARDWARE PROTOTYPING OF NEURAL PROCESSORS FOR "REAL" PROBLEMS

THE PROBLEMS

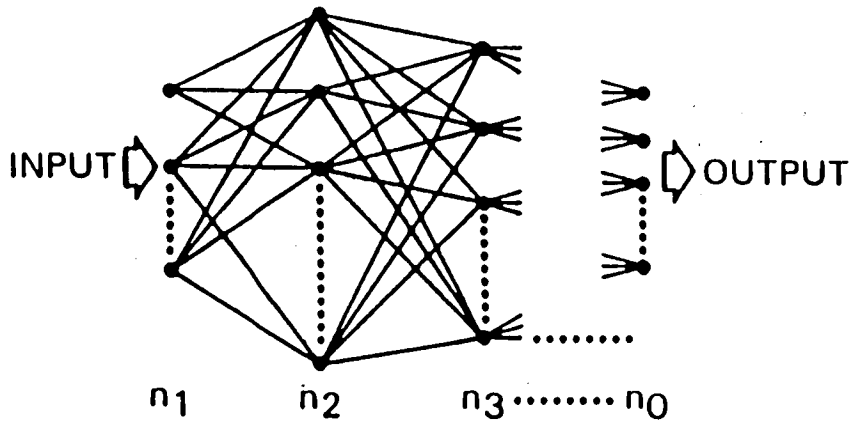
- MAP KNOWLEDGE BASE APPLICATIONS REQUIRING LARGE AMOUNTS OF DATA AND HIGH SPEED PROCESSING
  - CROSS-COUNTRY MOBILITY DETERMINATION: A MULTIDIMENSIONAL EUCLIDEAN DISTANCE MINIMIZATION PROBLEM
  - GENERATION OF MAP SEPARATES: AN IMAGE SEGMENTATION PROBLEM
  - DETERMINATION OF "BEST" PATH: A ROUTING PROBLEM

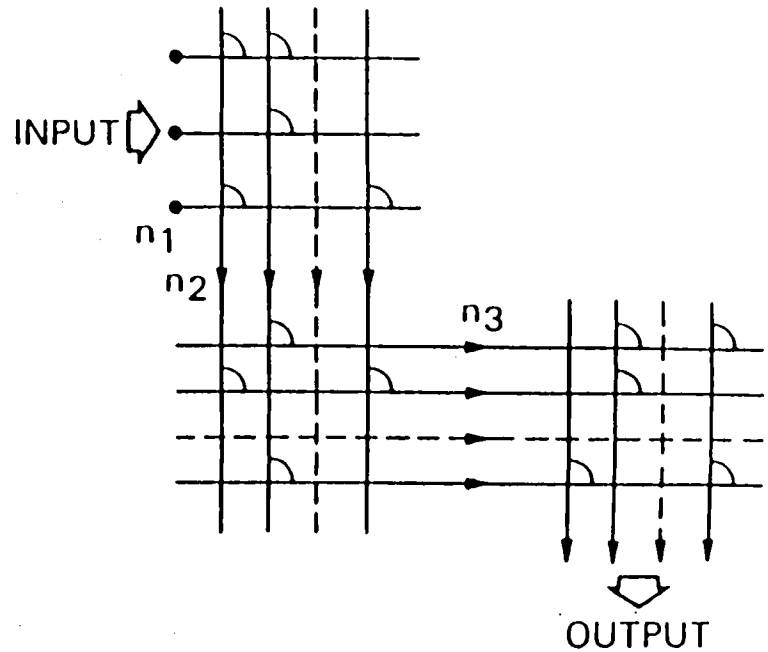
THE SOLUTION

- DEDICATED NEUROPROCESSORS IMPLEMENTING NEURAL ALGORITHMS FOR SOLVING THESE PROBLEMS
- THESE NEUROPROCESSORS WILL BE INTERFACED WITH A PORTABLE ASAS WORK STATION (PAWS) FOR USER EVALUATION AT THE CENTER FOR SIGNALS WARFARE (CSW)

JPL NEURAL NETS FOR ROBOTIC CONTROL

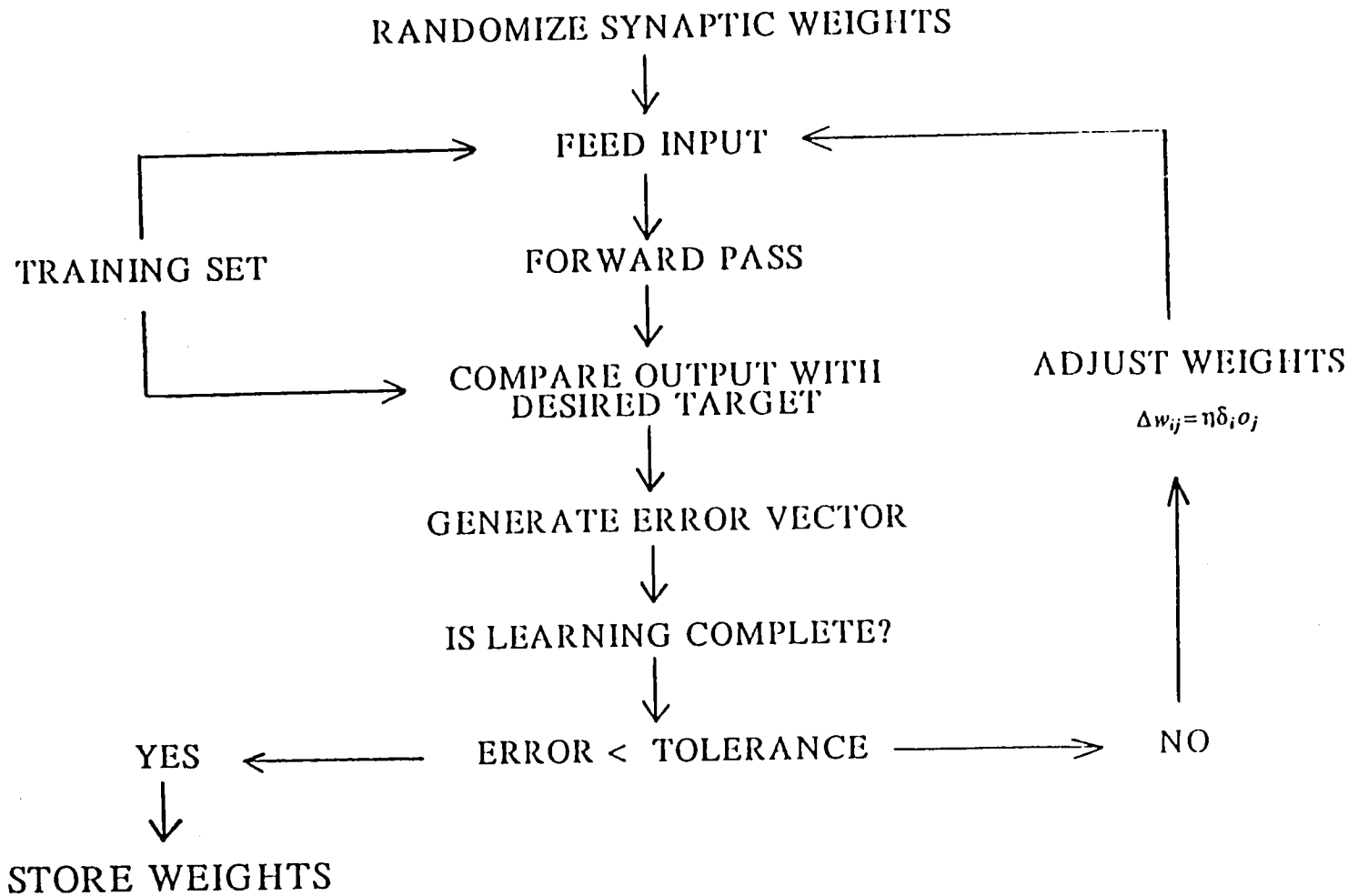
LAYERED, FEED-FORWARD NETS WITH ABILITIES TO 'LEARN' FROM 'EXPERIENCE'



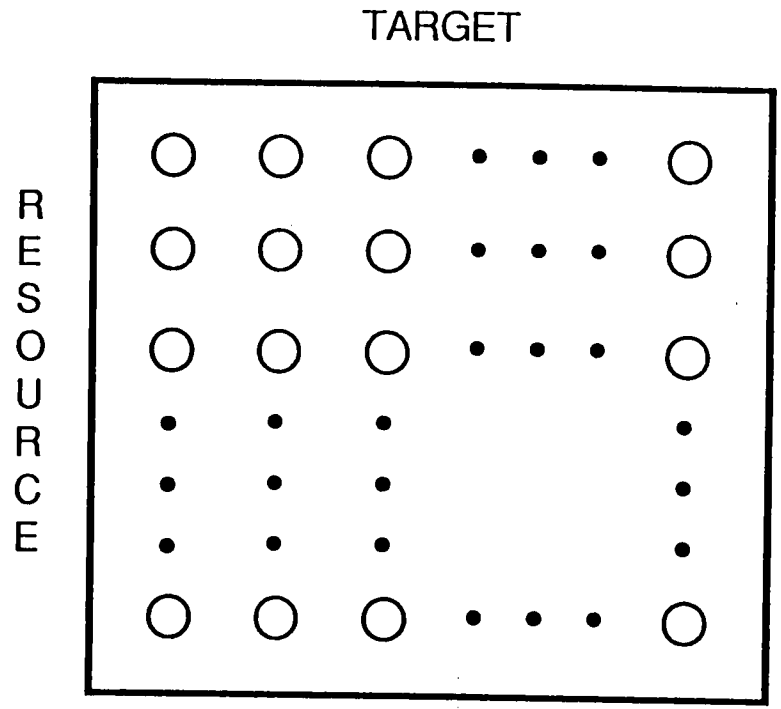


- LEARNING ALGORITHM: ERROR BACK PROPAGATION
- 'KNOWLEDGE' IS ACCUMULATED IN THE ANALOG SYNAPTIC WEIGHTS

ERROR BACKPROPAGATION ALGORITHM FOR LEARNING

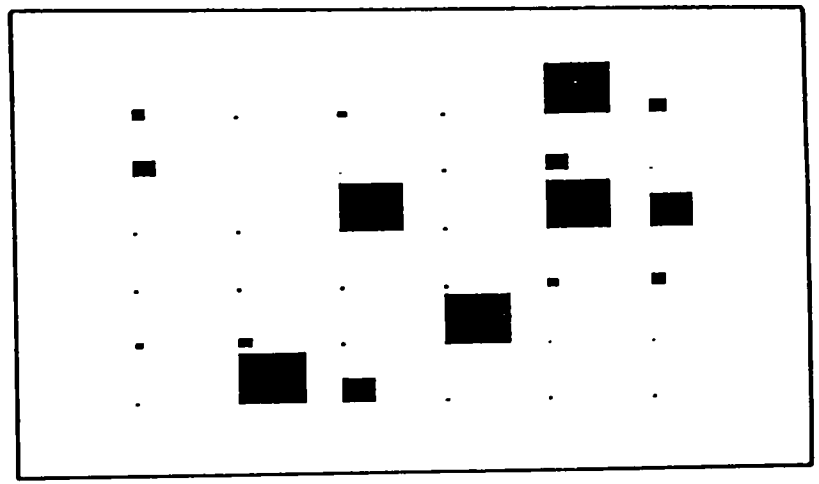


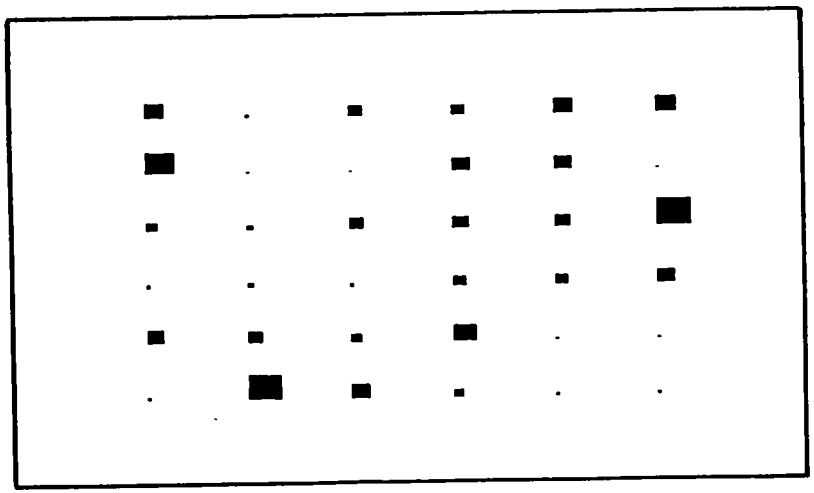
JPL RESOURCE ALLOCATION MATRIX

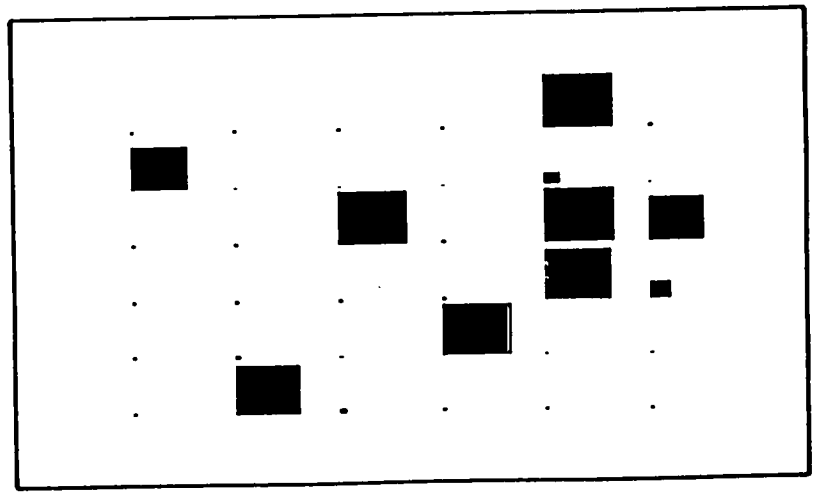


RESOURCE ALLOCATION PROCESSOR SIMULATION

01/01	01/01	01/02	01/01	01/04	01/01	
2	9	4	4	3	2	01/02
1	9	9	2	3	9	01/01
5	6	4	3	4	2	01/03
8	6	8	4	5	3	01/01
3	4	5	1	9	9	01/02
9	2	3	5	9	9	01/01
	08/10					

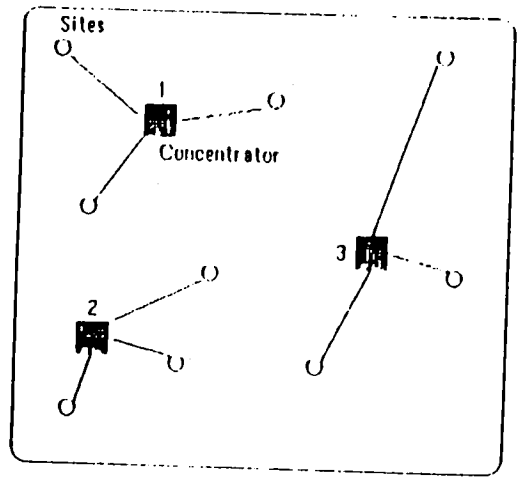






GLOBAL OPTIMIZATION NEUROPROCESSOR

- RESOURCE ALLOCATION
- DYNAMIC ASSIGNMENT
- MESSAGE ROUTING
- TARGET-WEAPON PAIRING
- LOAD BALANCING
- MULTI-TARGET TRACKING
- SEQUENCING / SCHEDULING
- REAL TIME, ADAPTIVE MISSION RE-PLANNING



NINE SITES
3 CONCENTRATORS

ALLOT 3 SITES TO EACH CONCENTRATOR TO ACHIEVE MINIMUM OVERALL COST

•• NEUROPROCESSING APPROACH OFFERS OVER 4 ORDERS OF MAGNITUDE SPEED ENHANCEMENT OVER THE CONVENTIONAL COMPUTING TECHNIQUES.

•• ARBITRARY MULTIPLE TO MULTIPLE ASSIGNMENTS ARE POSSIBLE, WHICH ARE NOT EASILY ACCOMPLISHED BY CONVENTIONAL TECHNIQUES.

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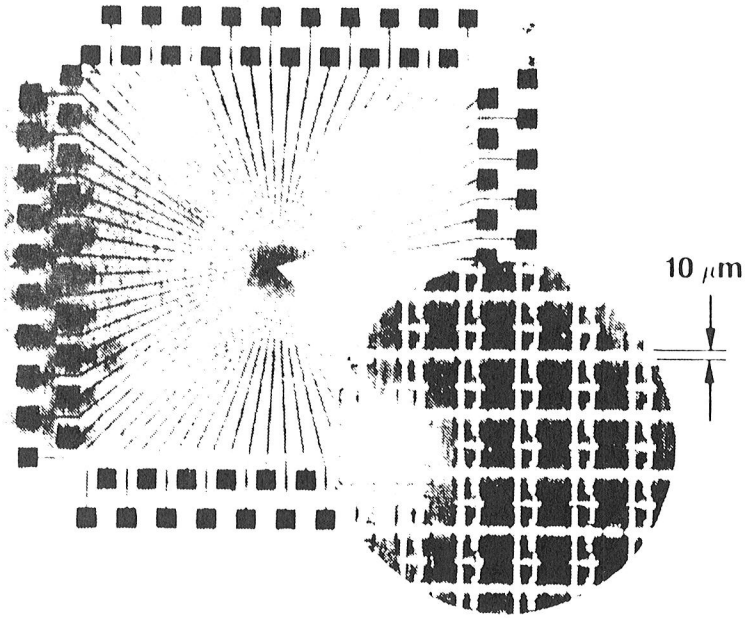
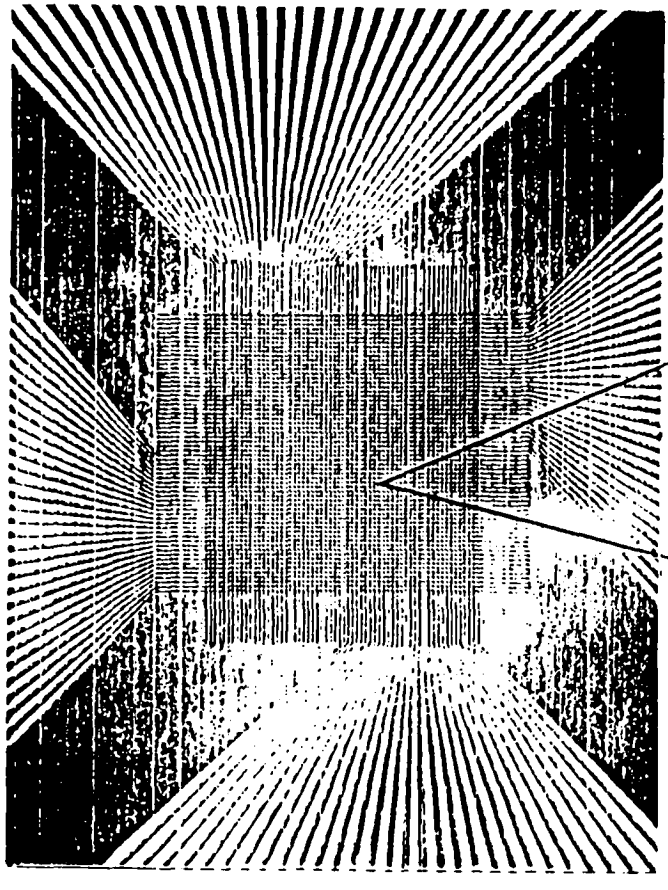
JET PROPULSION LABORATORY

PROGRAMMABLE, NONVOLATILE, HIGH-DENSITY, THIN FILM SYNAPTIC ARRAY FOR INFORMATION STORAGE

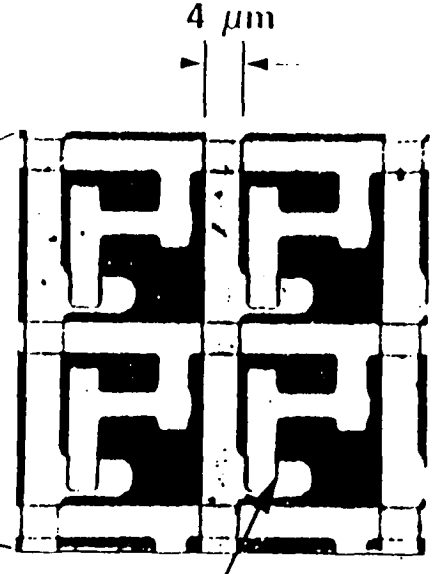


- POTENTIAL FOR HIGH DENSITY APPROACHING 10^9 BITS/CM^2
- FAULT-TOLERANCE
- ASSOCIATIVE, CONTENT-ADDRESSABLE RECALL
- NO MOVING PARTS
- STORAGE IN "PASSIVE," RAD-HARD INTERCONNECTIONS

ELECTRICALLY PROGRAMMABLE READ ONLY THIN-FILM SYNAPTIC ARRAY



A 62 x 62 SYNAPSE TEST ARRAY WITH
4-μm FEATURE SIZE



a-Si:H MICROSWITCH
AND RESISTOR SANDWICHED
BETWEEN METAL ELECTRODES

CONCLUSIONS

- THE FIELD OF NEUROPROCESSING HAS SIGNIFICANTLY ADVANCED IN RECENT YEARS. INVESTMENTS OF DOD AND NASA ARE RESULTING IN THE DEVELOPMENT OF APPLICATION-SPECIFIC, HIGH PERFORMANCE, MODULAR NEUROPROCESSORS.

- SUCH NEUROPROCESSORS OFFER TOTALLY NEW CAPABILITIES, COMPUTATIONAL BREAKTHROUGHS, AND ORDERS OF MAGNITUDE PERFORMANCE ENHANCEMENT WHERE CONVENTIONAL PROCESSING METHODS CHOKE.

- DOD IS MOVING AHEAD IN THE DIRECTION OF HARDWARE PROTOTYPING OF DEPLOYABLE NEUROPROCESSORS FOR COMPLEX PROBLEMS IN BATTLEFIELD MANAGEMENT AND TACTICAL FUSION OF INTELLIGENCE, ETC.

- *TIME IS RIGHT FOR NASA TO TAKE ADVANTAGE OF THIS POWERFUL TECHNOLOGY. TAILORED NEUROPROCESSORS WILL BE IDEALLY SUITED TO SATISFY NASA'S UNIQUE AND GROWING DEMANDS IN COMPUTATION AND DATA MANAGEMENT WITH THE EVOLUTIONARY DEVELOPMENT OF SPACE STATION.*