A NEW FABRICATION TECHNIQUE FOR BACK-TO-BACK VARACTOR DIODES

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Abstract: A new varactor diode process has been developed in which much of the processing is done from the back of an extremely thin semiconductor wafer laminated to a low-dielectric substrate. Back-to-back BNN diodes were fabricated with this technique; excellent DC and low-frequecy capacitance measurements were obtained. Advantages of the new technique relative to other techniques include greatly reduced frontside wafer damage from exposure to process chemicals, improved capability to integrate devices (e.g., for antenna patterns, transmission lines, or wafer-scale grids), and higher line yield. BNN diodes fabricated with this technique exhibit approximately the expected capacitance-voltage characteristics while showing leakage currents under 10 mA at voltages three times that needed to deplete the varactor. This leakage is many orders of magnitude better than comparable Schottky diodes.

Introduction:

Planar varactor diodes[1] are being developed in place of whisker-contacted devices in order to improve the performance and ruggedness of spaceborne submillimeter-wave heterodyne receivers; at the same time thin heterostructure layers are being used to improve diode performance, making processing more demanding. Such devices could be more useful if integrated into relatively large arrays that could potentially be used for communications systems. It is expected that such back-to-back multiplier diodes with Schottky contacts and heterostructure barriers can be made to operate reasonably efficiently at frequencies over one terahertz[2,3,4]. In this paper we present results from devices in which the isolation was performed from the back. This technique simplifies processing, greatly increasing yield and providing a much lower dielectric constant, and thus low loss, environment for antennas and other circuit patterns.

Conventional multiplier diode isolation techniques have a number of problem areas. Isolation implants are commonly used, but the removal of masking materials from the wafer often presents difficulties. An alternative technique for isolating the active devices is to perform a mesa etch, but connection of the contacts to the top of the mesa is problematic. One approach attempted here requires relatively difficult planarization processing that can potentially damage the thin barrier layer. Metal step coverage may be also a problem with this approach. Air bridging can also be used with mesa isolation, but this also exposes the top of the semiconductor material to a larger number of process steps. Some inactive semiconductor material, with its associated high dielectric constant, is generally left in place with all of these approaches.

We have developed an alternative processing technique that promises to be simpler and more robust. In this process, no inactive semiconductor material is left, and the front of the wafer is exposed to the absolute minimum of processing possible for a front-side back-to-

back diode process. In our work, the remaining process steps were completed with the devices laminated to a 3 mil quartz substrate. This quartz is the same as is typically used for the crossed-field waveguide multiplier filter structures for which the devices were intended. Clearly, there is a wide lattitude in substrate material, which adds a great deal of flexibility to the design of submillimeter-wave components. The total number of steps is relatively low, improving yield. Since thinned[1] or lifted off[5] devices never need to be handled off of the substrate material, relatively large scale integration can potentially be achieved with this process.

Initial fabrication runs have been successful. Back-to-back BNN diodes have been fabricated using the new technique and then measured for DC and low-frequency capacitance characteristics. Eight micron mesas with 1.5 and 3.75 micron wide Schottky metalization showed good C-V and outstanding I-V characteristics. While the C-V pulses were approximately two to three volts wide (full-width half-maximum), leakage currents were as low as 50 nA with 10 volts between pads. Mesas as small as 1 micron were successfully patterned.

Device Fabrication:

A. Semiconductor layer structure

Details regarding appropriate BNN layer structures have been addressed before[2,3,4]. The general approach for a GaAs-based BNN diode, from the top surface down, is to include: (1-optional) a thin GaAs cap layer, (2) an AlGaAs layer that is sufficiently thick to preclude tunneling but sufficiently thin to allow a large capacitance per unit area - 15 to 20 nm of $Al_{0.45}Ga_{0.55}As$ is typical, (3) near the AlGaAs, a highly doped region in order to ensure that the high capacitance mentioned above is achieved at zero voltage, (4) a moderately doped GaAs drift/varactor region in which all of the doping can be depleted with little parasitic conduction to the metal pads, and (5) a highly doped region that provides a low-resistance path between the two Schottky pads.

The structure used for these devices is as follows: (1) a 2 nm GaAs cap, (2) a 15 nm $Al_{0.45}Ga_{0.55}As$ barrier, (3) a 3 nm GaAs spacer followed by $5 \times 10^{12}/cm^2$ silicon planar doping, (4) a $1 \times 10^{17}/cm^3$ by 125 nm drift region, and (5) a $5 \times 10^{18}/cm^3$ by 900 nm conducting base. A 600 nm undoped $Al_{0.45}Ga_{0.55}As$ layer for use as an etch stop layer was located just below the active device layers, although much thinner layers have also been successfully used. The layer structure is shown schematically in Figure 1. Capacitance-voltage measurements between large capacitance pads on another area of the same wafer gave the data shown in Figure 2.

The process is shown in Figure 3. We processed GaAs wafer pieces about 1.7 cm on a side that were laminated onto quartz pieces 76 microns (3 mils) thick by 2.5 cm in diameter. The GaAs wafers were initially 510 microns (20 mils) thick.

The Schottky contacts are defined by exposing AZ 5214 with a standard image reversal technique and then evaporating and lifting off Ti/Pt/Au. While we did not do a surface isolation, the devices should show less leakage current and particularly less parasitic capacitance if etching (or implanting) were done through (or into) the delta-doped layer. Etching by using the metal as a mask has been done successfully but not on the wafers processed in this work.

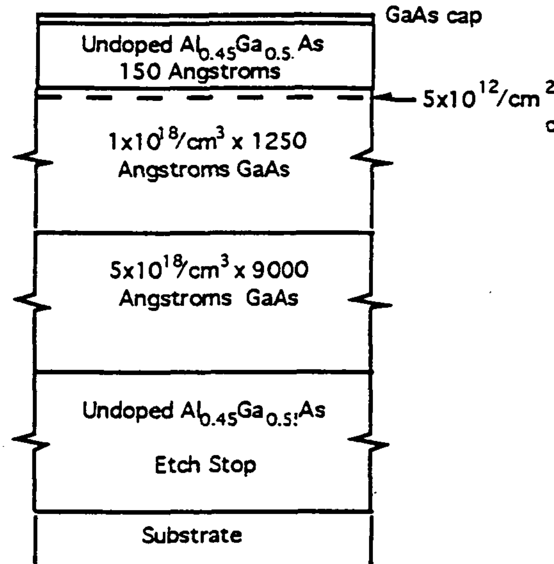

Figure 1: Epitaxially grown GaAs/AlGaAs layer for BNN diodes used in this study. Wafer layers were grown with molecular beam epitaxy. Doping is silicon.

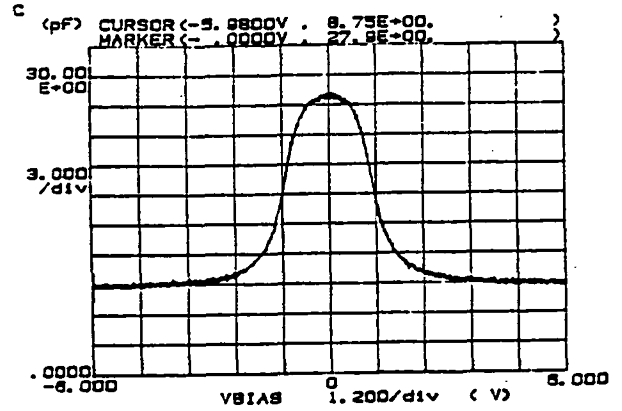

Figure 2: Capacitance-voltage characteristics measured at 1 MHz using large dots.

B. Device Processing

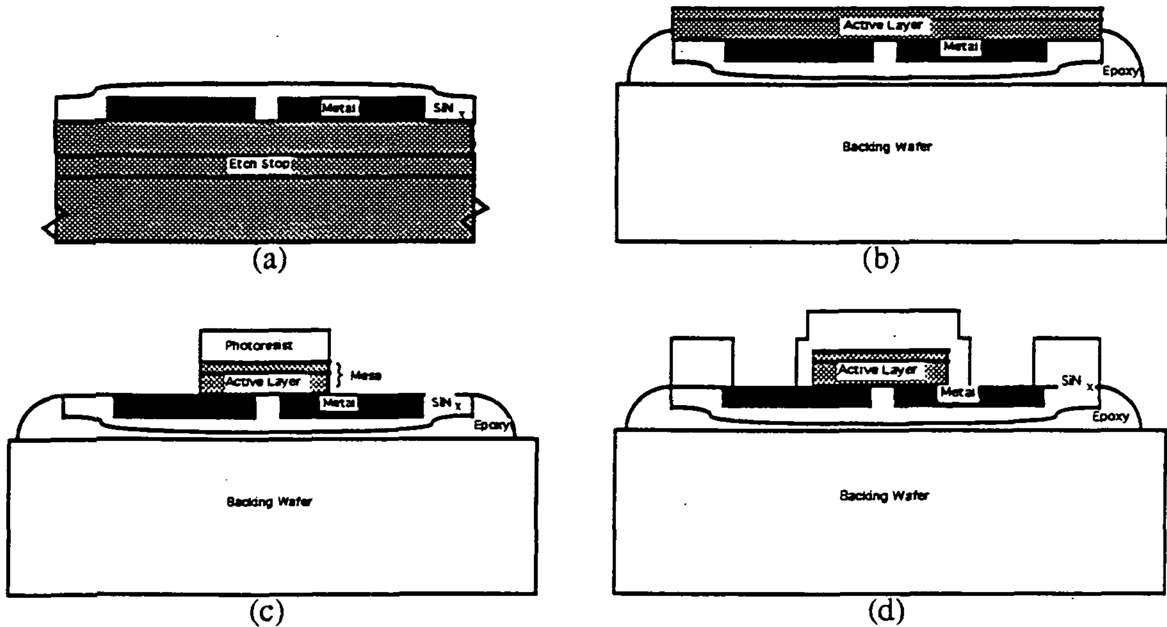

Figure 3: (1-a) The Schottky contacts are deposited, and a thin isolation through the delta-doped region is etched optionally, (2-a) front-side passivation is deposited, (3-b) the wafer is mounted face-down on a quartz wafer with wax for thinning (this wafer must be suitably thin to serve as the final substrate for the device and may be mounted in turn on a sturdier substrate), (4-b) conventional lapping and then selective thinning to an AlGaAs etch stop layer located just below the active layer, (5-c) lithography for mesa isolation is performed from the back of the wafer (at this point the wafer is sufficiently thin that the front-side metal can be viewed from the back through the substrate), and (6-c) the wafer is etched, (7-d) thin Si_3N_4 or SiO_2 is deposited in order to passivate the back and, if necessary, opened for bonding pads, and (8-d) the thin quartz wafer is diced.

The GaAs wafers were glued face down to a 75 micron thick quartz wafer, 2.5 cm in diameter, with UV-curing glue. The GaAs wafers were then lapped down to a 100 micron thickness using 5 micron, 1 micron, and finally 0.3 micron grit. Polishing was done with a silica colloidal suspension and pad. Selective thinning to the etch stop layer (5, above) was done using a 95/5 solution of ammonia and peroxide[1]. The peroxide/ammonia etch undercut the edges of the wafer two to three hundred microns, two to three times the vertical etch distance. Little damage of scale larger than pinholes of a micron or two in diameter could be seen over most of the wafers processed. A brief dip in HCl and water was used to remove the remaining oxide layer.

It should be noted that the wafers were remarkably rugged. The single cracked wafer observed so far occured during the lapping operation, which in our lab is performed using a relatively violent vibration table. The wafer that broke lost some small portions of the edge, but the area on which the GaAs was epoxied proved to be extremely tough despite cracks through the quartz. The wafer was processed to completion despite the cracks, with no allowances made to ease the normal rigors of microelectronic processing (spinning, contact lithography, etc.).

Mesas were defined by standard positive photolithography and dry etching. Wet etching was unsuccessful using either photoresist masks (excessive undercutting for the smaller, 1 micron mesas) or nitride masks (adhesion problems). The mesas were aligned to the frontside metal with IR backlighting, although the semiconductor is thin enough to permit aligning with optical backlighting if available.

Additional process steps have been done, including backside passivation with more ECR nitride and etching of contact holes with a CF4/O2 plasma. Clearly, the ability to deposit more metal in order to further reduce loss and to make MIM capacitors with the frontside metal and backside nitride is very attractive. Also, we have tried thinning the glue with acetone prior to spinning; this results in a much thinner layer (roughly 10 microns) between the GaAs wafer and the quartz substrate.

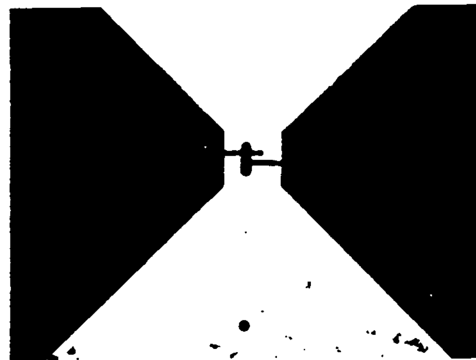

Figure 4: Backlit photograph of central portion of device. The small dark rectangle in the center is the approximately 4 x 16 micron micron mesa. The larger, dark portions with the thinner protrusions (2 micron fingers) are the Ti/Pt/Au pads. The remaining area is quartz.

The ECR nitride process is then repeated on the back, with windows opened with CF4/O2 RIE to the frontside metal for contacting. Other MMIC-style processing, including plating, MIM capacitor formation, etc. could be performed at this point.

Figure 4 shows a photograph of a completed device.

Electrical Measurements

Devices were checked for DC and capacitance characteristics after processing. Figure 5 shows the 1 MHz capacitance of a 3.75 x 8 micron device. While the peak capacitance is lower than expected from the capacitance data shown in Figure 2, it is thought that the difference is probably due to the fact that the processed wafer piece is from the edge of the MBE wafer. Figure 6 shows the DC current leakage before backside passivation. The measured current is many orders of magnitude lower than would be observed with comparable Schottky diodes, leading us to believe that the BNN is potentially superior as a multiplied power source.

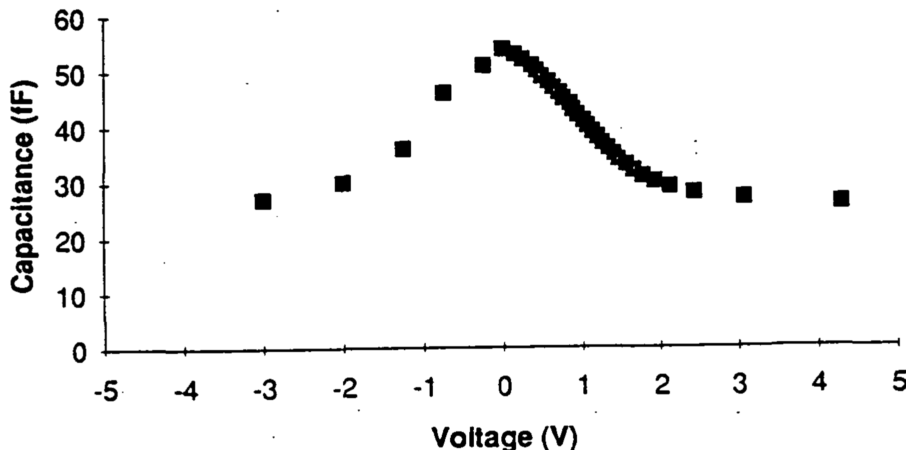

Figure 5: Measured C-V characteristics of a device with back-to-back 3.75 x 8 micron BNN diode.

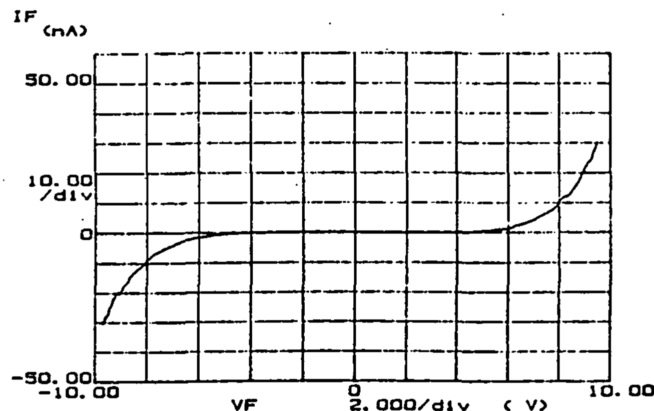

Figure 6: Measured DC leakage current for back-to-back 3.75 x 8 micron diode. Traces for positive and negative voltages were taken by sweeping away from zero volts. Higher leakage currents can be measured instantaneously if the voltage is not slowly swept; similar behavior commonly observed in MESFETs leads us to believe that the method used above is the most relevant.

Conclusions

We have demonstrated a new process for back-to-back diode fabrication using a BNN structure. The process should make integration of submillimeter-wave diodes much easier while simultaneously reducing RF losses through the elimination of all non-essential high-dielectric semiconductor. The BNN diodes constructed with this process show a strikingly low leakage current.

Acknowledgements

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References

1 W.L. Bishop, E.R. Meiburg, R.J. Mattauch, and T.W. Crowe, "A Micron Thickness Planar Schottky Diode Chip for Terahertz Applications with Theoretical Minimum Capacitance," 1990 IEEE MTT-S International Microwave Symposium Digest, p. 1305.

2 U. Lieneweg and U. Maserjian, "Harmonic generation in the near-millimeter-wave range by thin-MOS structures," presented at Sixth International Conference on Infrared and Millimeter Waves, Miami, FL, 1981.

3 U. Lieneweg, T. Tomunen, M. Frerking, and J. Maserjian, "Design of Planar varactor Frequency Multiplier Devices with Blocking Barrier," submitted to IEEE MTT Special Issue on Terahertz Technology, 1991.

4 E. Kollberg, T. Tolmunen, M. Frerking, and J. East, "Current Saturation in Submillimeter Wave Varactors," submitted to thte IEEE MTT Special Issue on Terahertz Technology, 1991.

5 E. Yablonovich, T. Gmitter, J.P. Harbison, and R. Bhat, "Extreme Selectivity in the Lift-Off of Epitaxial GaAs Films," Appl. Phys. Lett. vol. 51, p. 2222 (1987).

6 Norland Optical Adhesive 61, Norland Products Inc., P.O. Box 145, New Brunswick, NJ 18902.