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Development of $Si_{1-x}Ge_x$ Technology for Microwave Sensing Applications

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Abstract

This report discusses the progress for the first year of the work done under the Director's Discretionary Fund (DDF) research project entitled, "Development of $Si_{1-x}Ge_x$ Technology for Microwave Sensing Applications". This project includes basic material characterization studies of silicon-germanium (SiGe), device processing on both silicon (Si) and SiGe substrates, and microwave characterization of transmission lines on silicon substrates. The material characterization studies consisted of ellipsometric and magneto-transport measurements and theoretical calculations of the SiGe band-structure. The device fabrication efforts consisted of establishing SiGe device processing capabilities in the Lewis cleanroom. The characterization of microwave transmission lines included studying the losses of various Coplanar transmission lines and the development of novel transitions on silicon. This report discusses, individually, each part of the project and presents the findings for each. Future directions are also discussed.

Introduction

Silicon technology has never been considered viable for microwave applications because of its lack of high frequency active devices and the extremely high dielectric loss associated with silicon substrates. But silicon technology provides many benefits for microwave applications. Among them are: integration with digital circuitry, mature, well-defined processing procedures and low cost. Recently, a new material, SiGe (silicon-germanium), has emerged that can produce high frequency active devices in a silicon based technology. Using SiGe it is possible to fabricate devices with a two-dimensional electron gas (2DEG). This type of structure has advantages in terms of frequency of operation, noise

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performance and performance improvements at low temperatures. To reduce the dielectric losses associated with silicon substrates, it has been theorized that silicon of sufficiently high resistivity must be used [1].

The purpose of this research project is the development and characterization of microwave devices, both passive and active, using newly-developed SiGe technology at frequencies required for microwave sensing applications. This effort has included basic material studies of SiGe, the development of high electron mobility transistor (HEMT) devices and characterization of microwave transmission lines on high resistivity silicon.

In order to carry out the goals of the program, a working group was established consisting of several members of the Solid State Technology Branch. In this manner, people representing different areas of expertise were brought together. Material, device and circuit experts were all present from the onset of the program. This allowed all areas to be taken into account during planning. Since Lewis does not have the facilities necessary to grow SiGe material, industry and universities were relied upon for the preparation of the SiGe samples. Collaboration was established with UCLA, University of Michigan, Cornell University, Hughes and Spire Corporation. These universities and companies have provided HEMT structures, both n-type and p-type, as well as single strained layers for material characterization studies and device fabrication. It was important to find several sources for material preparation because SiGe technology is in its infancy and there are many uncertainties involved in its growth.

The program consisted of three different areas of research while maintaining a common objective among the members of the working group. The research areas consisted of: basic material studies, device processing and, microwave characterization studies. In a relatively short period of time, many of the goals of this three year program have been accomplished. This report describes the progress for the first year and discuss future directions.

Basic Material Characterization Studies

Theoretical Study

The objective of the theoretical study was to gain a better understanding of the relationships between the physical parameters of the layers in a SiGe structure (composition, grading, doping, and mobility), and the device performance parameters (unity current gain frequency and maximum oscillation frequency). The knowledge of these relationships is required in order to design an optimum structure for high-speed, low-temperature applications.

The procedure used to analyze these relationships was to calculate the band structure of the layers and then calculate the performance which results from that band structure. Because of the complexity of the mathematical problem associated with these calculations, as well as some other non-trivial aspects, a collaboration with the Computational Material Lab at NASA Lewis was established. This lab specializes in complicated matter-related numerical calculations. With the help of the Computational Material Lab, the creation of a sophisticated computer code that solves the Poisson equations and calculates the band structure and the currents of SiGe was recently completed. The I-V characteristics of some simple SiGe structures have been calculated and plotted.

Ellipsometry Work

SiGe material samples were obtained from Spire, UCLA, University of Michigan and Hughes. They included: single SiGe strained layers on silicon, Supperlattice SiGe-silicon, and n- and p-type HEMT structures. Only the results obtained for the n-type MODFET structures provided by UCLA and Spire will be discussed here. These samples consisted of a strained silicon layer for improved carrier confinement and are labeled as follows: 1) Spire D-5983, 2) UCLA MT-115. The results of Ellipsometric characterization of these samples is shown in Table 1.

Ellipsometric characterization of the samples included three steps: measurement, modeling and linear regression analysis. In the first step, the change in the state of polarization of a monochromatic light, that is reflected from the sample, is measured. This change in polarization is represented quantitatively using the ellipsometric parameters φ and Δ. The measurement was repeated for approximately 50 wavelengths and several angles of incidence. Thus, a large number of experimental φ and Δ are estimated. The sample is modeled using the estimated composition and thickness of all the layers in the sample. In the present case, the model consisted of the nominal compositions and thicknesses of all layers as supplied by the sample grower. They are denoted "nominal" in Table 1. The last step included a linear regression least square fit of all the experimental φ and Δ to the theoretically evaluated φ and Δ associated with the model. The minimization parameters were the composition of the SiGe layer and all layer thicknesses. The theoretical φ and Δ associated with the model were calculated using standard Fresnel reflection equations, and published dielectric functions of all material constituents.

The calculation was done using unpublished calibration functions supplied by J. Jellison from Oak Ridge National Laboratories. The dielectric functions supplied by Jellison were interpolated using a numerical algorithm. These functions were measured on relaxed layers of SiGe on silicon. Measurements were done at 3-5 angles of incidence in the range 3000-7500A using 100A steps. The wavelength (λ) range was limited so that the light did not penetrate the SiGe buffer layer into the silicon substrates. The concentration 'x' in the SiGe top layer and the "substrate" was assumed to be the same and no roughness was assumed. Graphs of the experimental DELTA (Δ) and PSI (φ) verses model calculations are shown in Fig. 1a,1b,1c,1d.

The reason the strained silicon layers have a lower thickness than the nominal value is probably due to the fact that the unstrained calibration function was used. This was done, because, as of now, no strained silicon calibration function exists. The results for D-5983 indicate that it was a poor quality sample, because the thickness and composition were very different from the nominal values. In comparison, sample UCLA MT-115 appeared much better.

Magneto-Transport Measurements

The most important characteristic of a HEMT structure is the two dimensional nature of its transport properties. This characteristic enables very high speed, low noise performance in active semiconductor devices. SiGe n-type structures have been shown to have very high mobilities, as high as 10^5 cm^2/V·s at low temperatures, which indicate that this is an excellent structure for microwave applications. It is very difficult however, to obtain two dimensionality in this structure since the conduction band discontinuity between silicon and SiGe is very small. This makes it difficult to achieve quantization of the carriers at the interface of the two layers. Two dimensional transport has only been obtained in the n-type structures by growing a strained silicon layer on top of a fully relaxed SiGe layer. The strain pushes down on the conduction band of the higher bandgap silicon layer, relative to the SiGe conduction band and thus makes possible the quantization. High quality strained layers are very difficult to grow as a result of misfit dislocations that arise from the lattice mismatch growth of the epitaxial layers. Because of this, the transport characteristics of the received samples had to be characterized.

N-type SiGe structures have been received from Spire, UCLA, University of Michigan and AT&T. Hall and Shubnikov-de Haas measurements were carried out using a 1.4 Tesla magnet at temperatures from room temperature down to 1.4K. Two dimensional transport was not detected in any of the structures. Therefore, transport must have occurred in either the bulk of the silicon or SiGe layers; as evident by the large carrier freeze-out at lower temperatures and the large magneto-resistance observed in the samples. Carrier freeze-out in a two dimensional electron gas (2DEG) leads to only a small decrease in the carrier concentration. In the structures examined here, the carrier concentration decreased by orders of magnitude as the temperature decreased. For example, the Spire sample went from a concentration of $7.22 \cdot 10^{12}/cm^2$ at 300K to a concentration of $1.5 \cdot 10^{7}/cm^2$ at 22K. This type of behavior was typical of all the samples. The freeze-out temperature of the samples varied between 20K and 50K.

Two dimensional transport was detected in the p-type structure provided by Hughes. As compared with the n-type structures, two dimensional transport in p-type structures is easier to achieve. This is due to the larger band discontinuity in the valance band of the silicon and SiGe layers. Doping the layers is also more simple for p-type structures and thus more accurately controlled. The mobility increased with decreasing temperature due to a reduction in phonon scattering effects. The drop in concentration is consistent with carrier freeze-out in the quantized states.

These results have been provided to the material suppliers and has led to modifications in their growth process. UCLA is attempting to lower the concentration of the capping layer (used for contact purposes), in order to reduce the band bending that occurs at such high concentrations. At Lewis, there is an attempt being made to etch away some of the doped layers, with the intent of reducing the band bending and increasing the energy discontinuity.

Device Processing

Much like the GaAs based high electron mobility transistor (HEMT) technology, SiGe HEMT technology offers the ability to fabricate active devices with low noise and high speed performance. SiGe HEMT technology has the added advantage of silicon's native oxide for metal-oxide-semiconductor (MOS) devices. The advantages of the MOS structure is the decrease in gate leakage and the improvement in device stability as compared to Schottky barrier structures.

To achieve device fabrication capability at Lewis, initial design and fabrication development projects were conducted. The intention of these projects was to develop processing techniques necessary for the fabrication of devices. Etching of SiGe materials was the first processing step required to achieve device patterning and was also needed to expose material layers for further device fabrication. Experiments were conducted to characterize etch rates for SiGe materials.

To achieve optimum device operation, low resistance contacts are critical. Therefore, development of a contact structure has been investigated. The focus of this research has been on antimony based contacts and ion implantation of the contact regions. Antimony based contacts studies were conducted using metal type, metal thickness, alloy temperature and alloy time as variables to determine optimum contact resistance. Figure 2 illustrates some of the results used to determine the proper contact procedure for SiGe devices. The figure shows the effect of various alloying temperatures on the series resistance on contacts of various composition. Studies were also conducted by ion implanting phosphorus ions into the material to create contact regions suitable for aluminum based contacts. Because a heterostructure is being used, contact to the 2DEG is required to provide ohmic contact to the carriers. Ion implantation is used because it creates a conduction path from the upper contact region to the channel.

In order to fabricate MOS type devices, an oxide is necessary. Oxide characteristics were investigated by examining C-V and I-V measurements. To insure that no interdiffusion of the germanium or donor impurity into the silicon channel layer occurred, a low temperature plasma enhanced chemical vapor deposition (PECVD) technique was used. A characteristic C-V curve is shown in Figure 3. It illustrates the ability to invert the channel region under the oxide and good saturation in the accumulation region. Analysis of the interface state density shows a minimum of $3 \cdot 10^{10}$ states/cm^2 using the Terman method. The capacitor turn on voltage can be adjusted via processing techniques to plus or minus 5 volts to compensate for charge screening at the inversion layer of the oxide, thus achieving an effective modulation of the 2D carriers.

This work was then used to fabricate a preliminary transistor design. Ion implantation was used in fabricating the contacts. A cross section of the device structure and a finished device are shown in Figures 4 and 5, respectively. Initial evaluation of the device indicated a suppressed transconductance. This was most likely caused by poor material. Contact and oxide resistivities were acceptable but the modulated carrier concentration was extremely low. This resulted in poor device performance. Future device fabrication will be conducted on improved materials. At that time, rf performance as a function of temperature will be measured.

Microwave Transmission Line Studies

To make microwave applications on silicon possible, silicon with sufficiently high resistivity must be used to minimize the dielectric loss. The aim of this segment of the DDF is to investigate the effective dielectric constant (ε_{eff}) and attenuation of various transmission lines on silicon as a function of resistivity. We investigated Coplanar Waveguide (CPW), Coplanar slotline and Coplanar stripline structures.

The CPW structures were evaluated theoretically and experimentally. The theoretical analysis was based on the expressions in [2] for ε_{eff} and attenuation. The data for attenuation is shown in Figure 6. These calculations are for 2μm gold lines on 203μm thick silicon wafers. In this figure, dielectric loss is shown as a function of silicon resistivity for CPW lines of various geometries. Conductor loss is not shown because it is independent of the substrate. It can be seen that the loss is independent of CPW geometry. Losses for wafers of low resistivities are extremely high, but they decreases quickly with increasing resistivity. At a resistivity of 3000 ohm-cm, the dielectric loss is approximately 0.1 dB/cm, which is acceptable. The effective dielectric constant, ε_{eff} was calculated to be 6.06 for a CPW line, S=100μm, W=50μm. Experimentally, the ε_{eff} and attenuation were obtained by deembeding these parameters from measurements of several CPW lines on silicon using software from NIST. The theoretical results showed that if silicon with resistivity of 3000 ohm-cm was used, the losses would be comparable with those of the same CPW lines on GaAs (Gallium Arsenide). CPW lines of varying geometries were fabricated on silicon with resistivity of 3000-4000 ohm·cm. The values obtained for ε_{eff} and attenuation are shown in Figures 7 and 8 respectively. For the data shown, S=50μm, W=25μm, wafer thickness = 300μm and the gold thickness is approximately 1.7μm. Although no exact theoretical calculations have been done for these particular lines, the measured values are in the expected range. The noise in both curves around 34 GHz was found to be due to cable resonances.

The Coplanar Stripline and slotline structures were evaluated experimentally using resonator methods (since the NIST deembeding software only works for CPW structures).

These methods were first validated on a much cheaper and easier to handle microwave material - RT Duriod 5810.5. This material has a dielectric constant (ε_r) of 10.5 (silicon has one of 11.7) and a loss tangent of 0.0028. The slotline structure was evaluated using a ring resonator that produces multiple resonances allowing many frequencies to be evaluated. The Coplanar stripline was evaluated using a series gap coupled straight resonator. The results, experimental and theoretical are summarized in Table 2.

In order to test the slotline, a transition from a CPW to the slotline was developed, since CPW lines can be wafer-probed and slotlines cannot. Two different transitions were developed. The first makes use of a finite ground plane coplanar waveguide (FCPW) which is electromagnetically coupled to a slotline. The second makes use of a conventional CPW which is coupled to the slotline with an airbridge. The average measured performance of both transitions (measured using two back-to-back transitions with about 0.8" of slotline in between) on Duroid substrate gave a maximum insertion loss of -1.5 dB and return loss of better than -10 dB over the frequency range of 3 to 8 GHz.

Second Year Objectives

The efforts of the second year will focus on continuing the collaboration that has been established with the various universities and corporations. The team at Lewis will work more closely with these organizations in the growth and preparation of the SiGe material structures. Results obtained from ellipsometric and magneto-transport measurements carried out at Lewis, will be used to calibrate the growth process and to further understand the material characteristics of various SiGe structures.

The device processing efforts established during this first year will also be continued. The focus will be on improving the performance of the MOS transistor fabricated here at Lewis. Higher quality material, as well as a more complete understanding of processing procedures, will help make this possible. Once suitable material has been obtained and a device fabricated, the rf performance as a function of temperature, will be characterized using an custom variable temperature cryostat. Dramatic improvement in the rf performance is expected at the lower temperatures because of the increase in the mobility of the majority carriers.

Microwave studies will continue and expand to include the development of passive microwave applications on silicon. This will include determining loss as a function of resistivity for CPW lines and the continuing development of slotline and CPW striplines on silicon. Applications such as: phase shifters and antennas will be developed. This is in preparation for the third year effort which will involve combining the microwave passive with the active devices to form truly integrated SiGe circuits.

Conclusion

We have been successful in establishing collaboration with universities and industry for the growth of the SiGe structures. Results obtained from ellipsometric and magneto-transport measurements, carried out at Lewis, were used in the calibration of the growth process as well as to further understand the material characteristics of SiGe. Also, theoretical calculations of the band structure and I-V characteristics of some simple structures, were carried out using a code that was developed at Lewis. We have also been successful in establishing a SiGe device processing capability in the Lewis cleanroom. Preliminary results have been obtained for a MOS transistor device. Finally, we have favorably ascertained the feasibility of silicon as a substrate for microwave applications. Theoretical calculations have shown that transmission line losses are similar to those of GaAs if the substrate resistivity is kept above a certain value. We have also evaluated experimentally Coplanar Stripline and slotline structures using resonator methods.

References

[1] Rosen, A., et al. "Silicon as a Millimeter-wave Monolithically Integrated Substrate-a New Look", RCA Rev., 1981, 42, pp. 633-660.
[2] Gupta, K.C., R. Garg, I.J. Bahl. Microstrip Lines and Slotlines. Artech House, Inc. 1979. pp. 285-287 and 275-276.

a) Layer	Nominal	Ellipsometry
SiO_2	---------	6 ± 1
Silicon	200 angstroms	113 ± 3
$Si_{1-x}Ge_x$	500 angstroms	498 ± 6, $x=0.233\pm0.011$
Silicon	500 angstroms, x=0.30	114 ± 11
$Si_{1-x}Ge_x$	x=0.30	$x=0.233\pm0.011$
	Substrate	

b) Layer	Nominal	Ellipsometry
SiO_2	------------	26 ± 1
Silicon	400 angstroms, x=0.35	428 ± 3
$Si_{1-x}Ge_x$	150 angstroms	0.338 ± 0.004
Silicon	x=0.35	135 ± 4
$Si_{1-x}Ge_x$	Substrate	0.338 ± 0.004

Table 1: Results of ellipsometric study of SiGe structures. a) D-5983,mean square error= 7×10^{-4} b) UCLA MT-115, $\lambda\leq$ 6400 angstroms mean square error= 2×10^{-3}

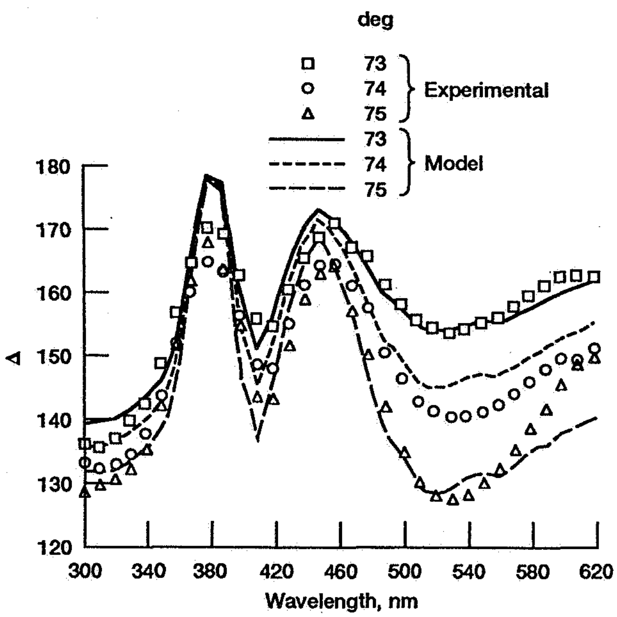
a) Slotline

Frequency (GHz)	Measured ε_{eff}	Computed ε_{eff}	Measured Attenuation
25.4	4.1918	4.2093	0.4374
18.8	4.0415	3.9413	0.3471
12.1	3.7996	3.5932	0.2189

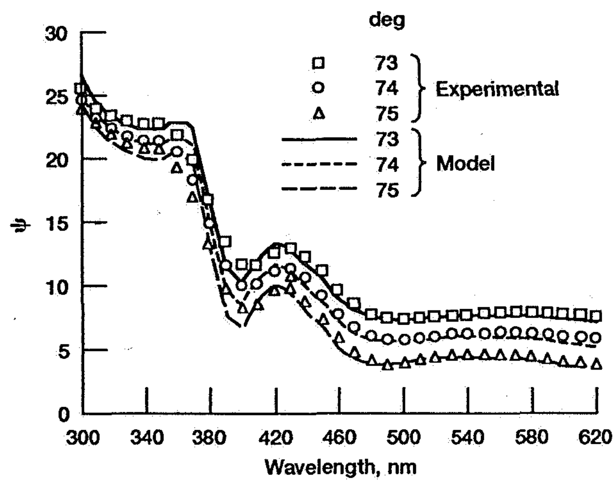
b) Coplanar Stripline

Frequency (GHz)	Measured ε_{eff}	Computed ε_{eff}	Measured Attenuation	Computed Attenuation
6.2	*	3.9872	0.139	0.111
11.0	*	4.7451	0.158	0.150

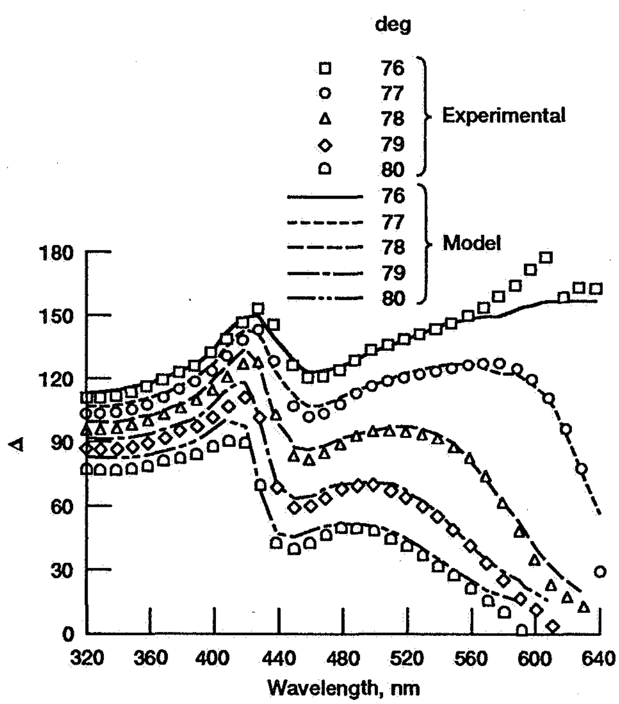
Table 2: Characteristics of ring resonators on high resistivity silicon a) Slotline b) Coplanar Stripline



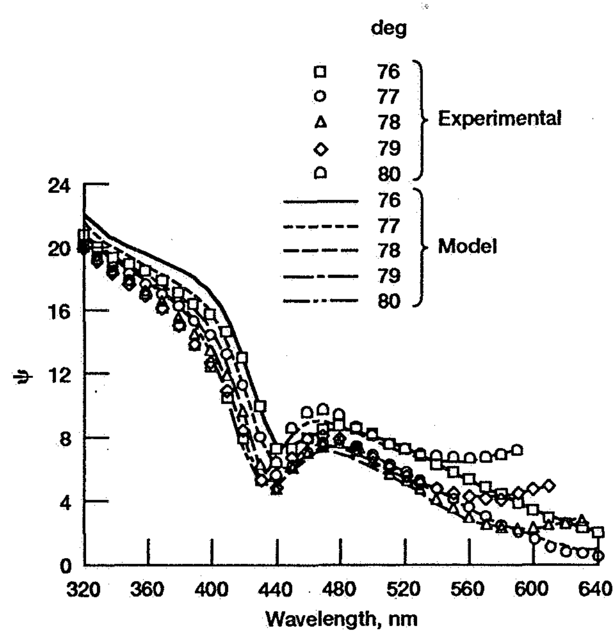
(a) Spire Corporation D-5983; measurement versus model.



(b) Spire Corporation D-5983; measurement versus model.



(c) UCLA MT-115; measurement versus model.



(d) UCLA MT-115; measurement versus model.

Figure 1.—Ellipsometry data.

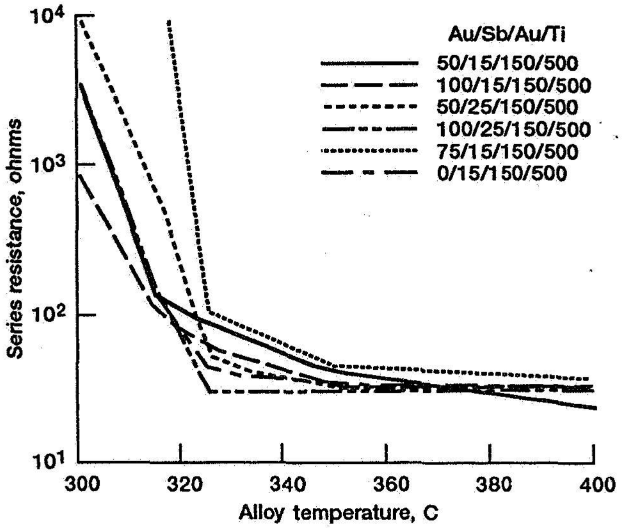


Figure 2.—Series resistance as a function of temperature for various Au/Sb/Au/Ti contacts on silicon.

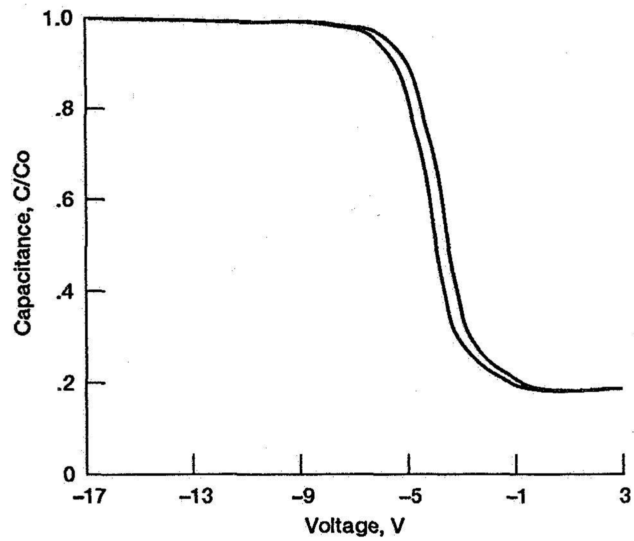


Figure 3.—C-V curve of oxide on SiGe.

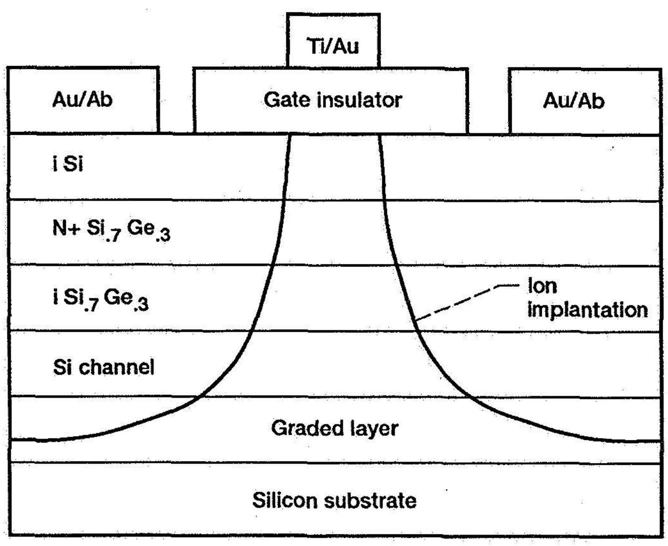


Figure 4.—Self gate aligned SiGe MOS-MODFET-device structure.

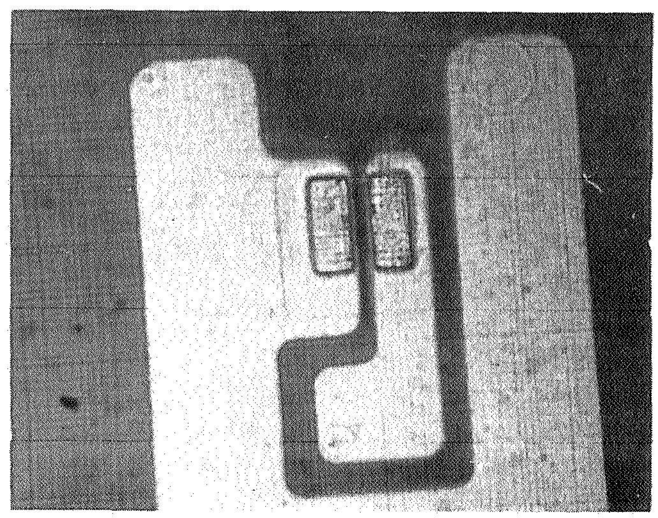


Figure 5.—Self gate aligned SiGe MOS-MODFET finished device.

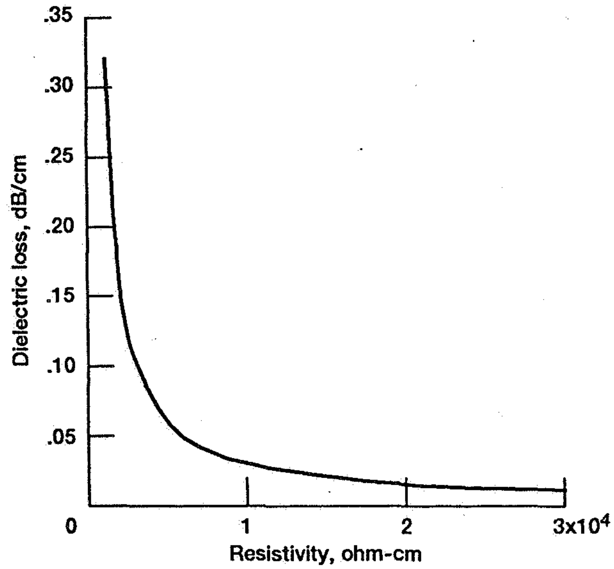


Figure 6.—Theoretical dielectric losses of CPW lines on silicon as a function of resistivity.

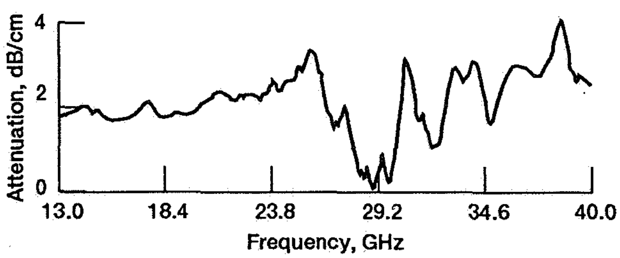


Figure 7.—Measured attenuation.

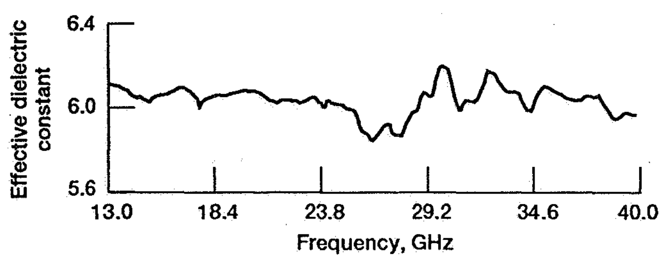


Figure 8.—Measured effective dielectric constant.

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13. ABSTRACT ***(Maximum 200 words)***

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