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LOW COST HIGH EFFICIENCY GaAs MONOLITHIC RF MODULE

FOR

SARSAT DISTRESS BEACONS

IN-33-CR

SBIR PHASE II FINAL REPORT
CONTRACT NO. NAS3-25712

PREPARED FOR:
NASA LEWIS RESEARCH CENTER
CLEVELAND, OH 44135

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DECEMBER 1991

PROJECT SUMMARY

Low cost high performance (5 Watts output) 406 MHz beacons are urgently needed to realize the maximum utilization of the Search and Rescue Satellite-Aided Tracking (SARSAT) system spearheaded in the U.S. by NASA. Although current technology can produce beacons meeting the output power requirement, power consumption is high due to the low efficiency of available transmitters. Field performance is currently unsatisfactory due to the lack of safe and reliable high density batteries capable of operation at -40°C. Low cost production is also a crucial but elusive requirement for the ultimate wide scale utilization of this system.

Microwave Monolithics Incorporated (MMInc.) has proposed to make both the technical and cost goals for the SARSAT beacon attainable by developing a monolithic GaAs chip set for the RF module. This chip set consists of a high efficiency power amplifier and a bi-phase modulator. In addition to implementing the RF module in Monolithic Microwave Integrated Circuit (MMIC) form to minimize ultimate production costs, the power amplifier has a power-added efficiency nearly twice that attained with current commercial technology. A distress beacon built using this RF module chip set will be significantly smaller in size and lighter in weight due to a smaller battery requirement, since the 406 MHz signal source and the digital controller have far lower power consumption compared to the 5 watt power amplifier.

All the program tasks have been successfully completed. The GaAs MMIC RF module chip set has been designed to be compatible with the present 406 MHz signal source and digital controller. A complete high performance low cost SARSAT beacon can be realized with only additional minor iteration and systems integration.

FORWARD

This is the final report for contract NAS3-25712 with NASA Lewis Research Center, entitled "Low Cost High Efficiency GaAs Monolithic RF Module for SARSAT Distress Beacons", covering the period from July 11, 1989 to November 10, 1991. Dr. W.C. Petersen and Dr. D.P. Siu were the co-principal investigators for this effort, and were responsible for the design and characterization of the monolithic circuits. Dr. D.P. Siu was also responsible for materials qualification and preparation. Dr. D.R. Ch'en was the program manager for this effort, and was also responsible for the fabrication of the beacon monolithic chips. Mr. H.F. Cook served as a consultant in the areas of device and circuit characterization. Mr. M.A. Cauley was the NASA technical monitor for the entire program.

LIST OF FIGURES (Continued)

LIST OF TABLES

1) INTRODUCTION

In response to aviation and marine emergency situations, the Search and Rescue Satellite-Aided Tracking (SARSAT) system has been instrumental in rescuing well over 1000 persons in the past twelve years. The enhanced flexibility designed into the 406 MHz SARSAT beacon system, spearheaded in the U.S. by NASA, has substantially reduced response time and allows rapid identification and sorting of each alarm signal. Maximum utilization, however, depends critically on the development and commercialization of high performance (5 Watts output) low cost beacons. Such high power beacons are, however, currently not feasible due to the lack of safe and reliable high density batteries capable of operation at $-40^{o}C$. Sufficient advances in battery technology are unlikely in the foreseeable future. Only when high efficiency beacons with low battery drain become readily available can widespread use and world-wide deployment become a reality in the civilian, commercial, and military arenas.

Several years ago Microwave Monolithics Incorporated (MMInc.) developed a proprietary high efficiency power GaAs FET for microwave applications. It was suggested in the phase I proposal that this device, when applied to UHF power amplification, will resolve the beacon battery dilemma by reducing battery load rather than improving battery performance. The coarse geometries possible at these low frequencies would also provide the high production yields required for low cost. In program phase I MMInc. demonstrated that its proprietary high efficiency GaAs power FETs provide truly spectacular performance at 406 MHz, with MMIC compatible power FETs yielding 80% drain efficiency. In program phase II MMInc. developed a GaAs MMIC chip set for the SARSAT beacon RF module, consisting of a high efficiency five watt power amplifier and a bi-phase modulator. The performance of these monolithic components meet, and exceed, the phase II program goals. This RF chip set, combined with a stable RF signal source and large scale silicon integrated circuit implementation of the low frequency control and signal processing circuitry, will result in a high performance, high reliability, production worthy beacon.

This report covers phase II of the beacon RF module development effort, in which proof of concept has been demonstrated. The preliminary MMIC designs for the power amplifier and the bi-phase modulator from program phase I were finalized and completed. The bulk of the program effort then centered on fabrication, characterization and design iteration of these chips. An executive summary is provided in section 2. This is followed by a detailed description of the SARSAT beacon RF module MMICs in section 3. Fabrication techniques utilized for these high performance MMICs are described in section 4, and measured performance of the monolithic beacon RF module components are presented in sections 5 and 6. Design iteration of the MMIC components is described in section 7, and measured performance of the iterated MMIC components are presented in section 8. Preliminary production design and cost estimates are described in section 9. Conclusions and recommendations for future work are presented in section 10. Finally, a description of the circuit test configurations used in the measurements is provided in Appendix A.

2) EXECUTIVE SUMMARY

This is the final report for contract No. NAS3-25712 with NASA Lewis Research Center, covering phase II of a multi-phase program to develop a "Low Cost High Efficiency GaAs Monolithic RF Module for SARSAT Distress Beacons". Such low cost high performance (5 Watts output) 406 MHz beacons are urgently needed to realize the maximum potential of the Search and Rescue Satellite-Aided Tracking (SARSAT) system spearheaded in the U.S. by NASA. Although current technology can produce beacons meeting the output power requirement, power consumption is high due to the low efficiency of available transmitters. Field performance is currently unsatisfactory due to the lack of safe and reliable high density batteries capable of operation at $-40^{o}C$. Low cost production is also a crucial but elusive requirement for the ultimate wide scale utilization of this system.

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In this phase of the program, the preliminary chip designs from program phase I for the power amplifier and the phase modulator were finalized and completed. Following several iterations of fabrication, characterization, modification, and re-characterization, impressive performance results were obtained. An output power of over 5 watts with approximately 60 % power-added efficiency was measured from a power amplifier. The associated gain of the two-stage amplifier was in excess of 25 dB. Output powers as high as 7 watts have been observed. Very accurate phase states were also achieved in the phase modulators. The average phase error was only 0.03 radians. All the program tasks shown in Table 2-1 have been successfully completed. The GaAs MMIC RF module chip set was designed to be compatible with the present 406 MHz signal source and digital controller. A complete high performance low cost SARSAT beacon could therefore be realized with only additional minor iteration and systems integration. A functional block diagram of such a SARSAT distress beacon using the GaAs MMIC RF module chip set is shown in Figure 2-1.

Considerable delay in program progress occurred as the first iteration mask tool set was being procured. On May 14, 1990 MMInc.'s primary mask tooling vendor notified MMInc. that they were going out of business. New negotiations with MMInc.'s alternate mask tooling vendors were immediately begun. A no cost extension for the estimated four months delay in program progress was requested by MMInc. and subsequently approved by NASA. As described above, in spite of these obstacles all technical tasks were completed within the extended period, and all program goals have been either met or exceeded.

Table 2-1) PHASE II STATEMENT OF WORK

TASK 1) Finalize the design of the monolithic SARSAT distress beacon circuits designed in program phase I, i.e. the phase modulator and the power amplifier output stage. Generate layouts and procure a mask tool set which includes all necessary proprietary process evaluation and test structures, and any additional test structures needed for complete DC and RF circuit evaluation.

TASK 2) Utilizing the mask tool set from task 1 and MMInc.'s proprietary flash annealed ion implanted MMIC fabrication technology, fabricate the high efficiency power amplifier output stage and the phase modulator for the SARSAT RF module designed in program phase I.

TASK 3) Characterize the MMIC SARSAT beacon power amplifier fabricated in task 2 for gain, efficiency, output power, etc. Characterize the monolithic phase modulator for phase shift, switching speed, insertion loss, and related performance parameters. Design and procurement of all necessary test fixturing is included as part of this task.

TASK 4) Based on the results of tasks 1 through 3 and the predicted performance estimates from program phase I, iterate the design and layout of the SARSAT beacon power amplifier output stage and the monolithic phase modulator.

TASK 5) Fabricate and characterize the iterated designs from task 4, and repeat as necessary to approach the performance goals identified in program phase I. As part of this task, identify potentially yield limiting process, layout, and circuit parameters, and attempt to maximize ultimate production yields.

TASK 6) Based on the experience gained in tasks 4 and 5, reassess the partitioning of the SARSAT beacon to minimize production costs, and updated estimates of high volume production costs for the SARSAT RF module.

TASK 7) Based on the results of tasks 1 through 6 and interactions with consultants and NASA personnel, initiate design of a fully integrated (or TBD integration level) GaAs modulator / high gain (35 dB) high efficiency (~60%) power amplifier for the SARSAT rescue beacon. As program resources permit, finalize these designs, generate layouts, procure a mask tool set, fabricate and characterize the MMICs, and iterate to reach performance goals.

TASK 8) Deliverables:

1) 1 each monolithic power amplifier output stage mounted on carrier.
2) Test fixture for item 1.
3) Data package for item 1.
4) 1 each monolithic GaAs SARSAT beacon phase modulator mounted on carrier, with test fixture if different from item 2.
5) Data package for item 4.
6) Within program constraints, 1 each SARSAT beacon RF module modulator/power chain, on carrier, with fixture and data package.
7) A final report to be prepared and submitted within 45 days of completion of the technical tasks.

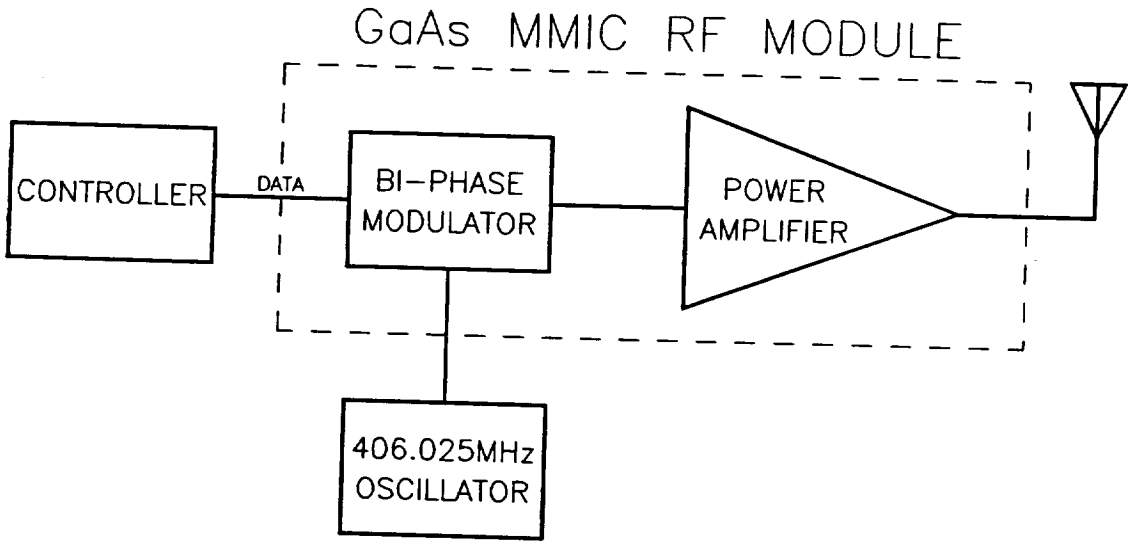


Figure 2-1) FUNCTIONAL BLOCK DIAGRAM OF SARSAT DISTRESS BEACON USING GaAs MMIC RF MODULE CHIP SET

Two power amplifiers and two phase modulators were delivered to NASA Lewis Research Center for engineering data correlation. Each circuit was contained in a hermetically sealed package of about 2.5 cm square complete with 50 ohm SMA connectors and bias / control pins for convenient laboratory evaluation. A photograph of the items delivered to NASA is shown in Figure 2-2. Although to date only R&D quantities of the MMICs have been fabricated, initial yields indicate that low production costs at high volumes should be readily attainable.

Proof of concept for MMInc.'s low cost high performance 406 MHz SARSAT beacon RF module design has therefore been established. As originally envisioned by MMInc., a low risk phase III program consisting of a final MMIC design iteration followed by systems integration with the available 406 MHz signal source and digital controller will lead to completion of the depicted SARSAT distress beacon shown in Figure 2-1. Completing development of this unit will greatly promote widespread use and worldwide deployment of the 406 MHz SARSAT beacon system.

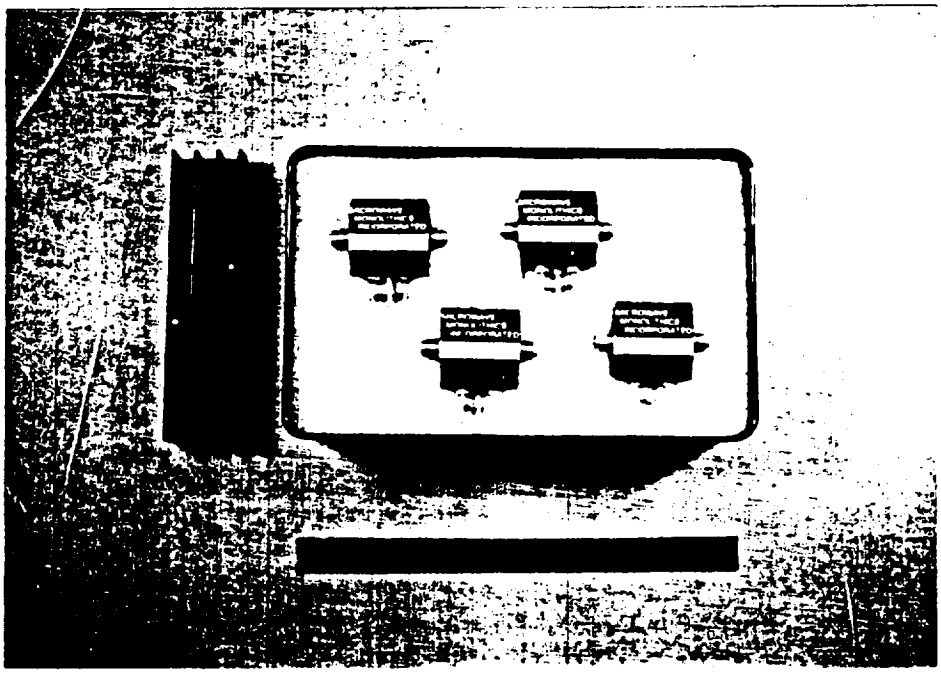


Figure 2-2) PHOTOGRAPH OF PACKAGED POWER AMPLIFIERS AND PHASE MODULATORS DELIVERED TO NASA LEWIS RESEARCH CENTER

3) GaAs MONOLITHIC SARSAT BEACON RF MODULE DESIGN

The design of the monolithic GaAs components for the SARSAT beacon RF module and their predicted performance are presented in this section. A simplified block diagram of a SARSAT beacon is shown in Figure 3-1. A controller implemented in silicon LSI parts[1] provides the coded distress message as well as powering up and down the other components of the beacon during signal transmission cycle of approximately 50 seconds. A stabilized oscillator serves as the source of the 406.025 MHz signal. The subject of this program is the RF module consisting of a high efficiency power amplifier preceded by a bi-phase modulator. The gain budget of the RF module components is shown in Figure 3-2. The power levels at the component interfaces are also shown. Performance goals for the high efficiency power amplifier are given in Table 3-1. Performance goals for the bi-phase modulator are given in Table 3-2.

In actual implementation of the monolithic circuits, each of these components may employ multiple stages. Note that the goals shown in Table 3-1 are appropriate for the output stage of the power amplifier. The overall gain of the power amplifier should be about 23 dB to provide the +37 dBm (5 watts) output using an overall gain for the modulator of -3 dB. MMInc. therefore undertook the task of developing a driver stage for the power amplifier as well, resulting in a two-stage design for the power amplifier, each with 10 to 13 dB of gain. The power amplifier accounts for most of the current drawn by the RF module; the current used by the modulator is not significant from the overall systems point of view. The design of this component should therefore center on small size and high yield. In particular, the design of the passive phase shifting elements need not be over constrained by the insertion loss of the "modulator". A suitable buffer amplifier can make up the loss while staying close to the power supply current budget.

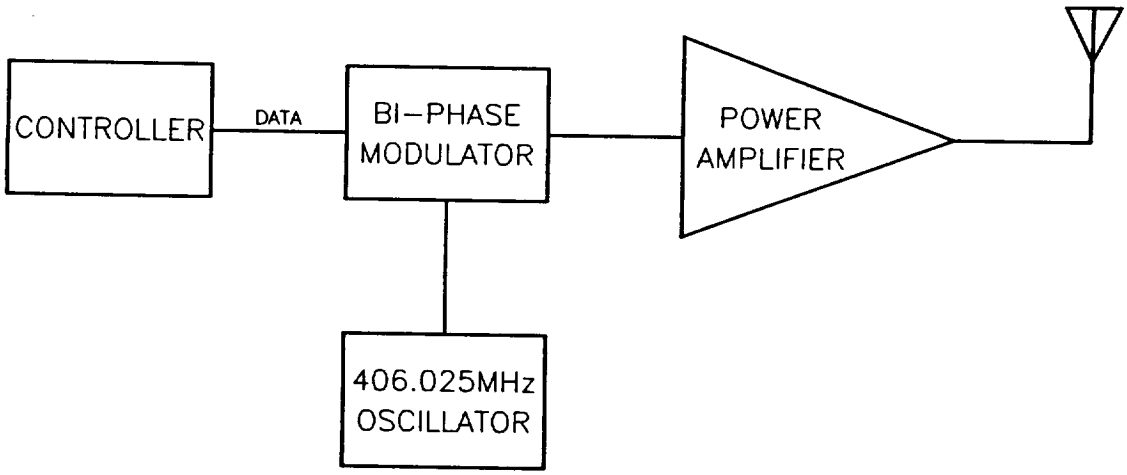


Figure 3-1) SIMPLIFIED BLOCK DIAGRAM OF A SARSAT DISTRESS BEACON

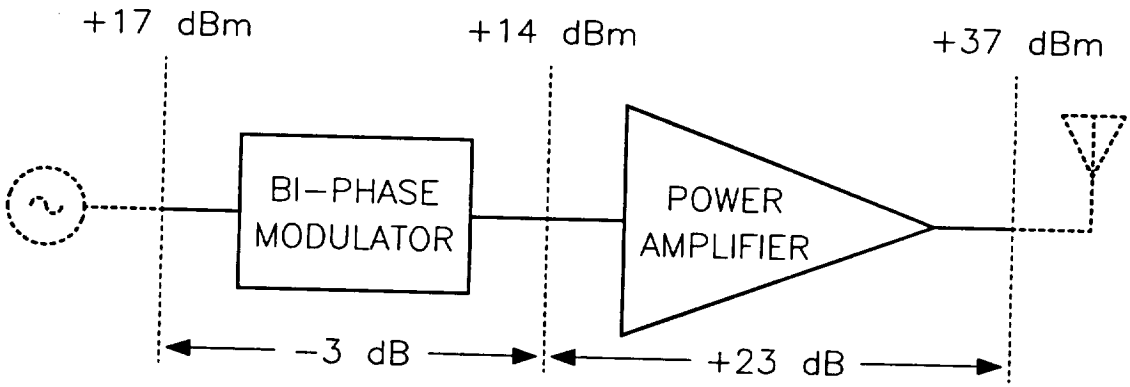


Figure 3-2) BLOCK DIAGRAM OF THE SARSAT BEACON RF MODULE

Table 3-1) PERFORMANCE GOALS FOR THE MONOLITHIC GaAs SARSAT BEACON POWER AMPLIFIER

Operating Frequency	406.025 MHz
Input Impedance	50 ohms
Output Impedance	50 ohms
Output Power	5 Watts
Power Gain	10 dB
Power-Added Efficiency	> 50%
DC Supply Voltage	9 to 15 Volts
Idle DC Supply Current	< 5 mA

Table 3-2) PERFORMANCE GOALS FOR THE MONOLITHIC GaAs SARSAT BEACON PHASE MODULATOR

Operating Frequency	406.025 MHz
Input Impedance	50 ohms
Output Impedance	50 ohms
Phase States	0.0 degrees
	+1.1 radians ($\pm$ 0.1 radians)
	-1.1 radians ($\pm$ 0.1 radians)
Insertion Loss	< 3 dB for all phase states
DC Supply Voltage	9 to 15 Volts
DC Supply Current	< 10 mA

Based on this concept, the components of the RF module during the first design iteration consisted of four circuits: the output stage, the driver stage, the buffer amplifier, and the "phase modulator". The block diagram of the RF module components is shown in Figure 3-3. Note that the gain of each component is still somewhat arbitrary since only the overall gain (20 dB based on the nominal oscillator output of 17 dBm) and output power (5 watts) of the entire module have significance to system performance.

Design of these components and their predicted performance is described in the following subsections.

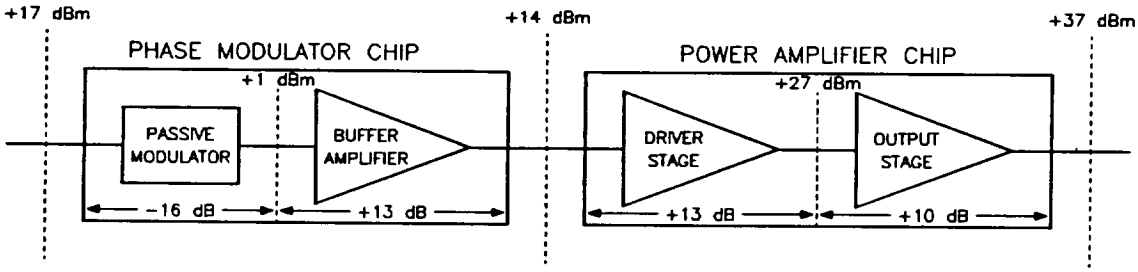


Figure 3-3) BLOCK DIAGRAM OF THE SARSAT BEACON RF MODULE COMPONENTS

3.1) HIGH EFFICIENCY POWER AMPLIFIER

The GaAs FETs in the present circuits are operating well below their frequency limitations, even considering the relaxed geometries which were utilized for high yield. A FET gate length of 1 micron (twice the length routinely processed at MMInc.) combined with gate to source and drain spacings of over 2 microns provide more than enough gain; in fact the devices are still potentially unstable at 406 MHz making stabilization circuitry necessary. Lumped element matching networks are essential at UHF frequencies, since a single quarter wavelength line on GaAs is over 25 cm long. Interactions among circuit elements are less compared to microwave frequencies; however the frequency is high enough that they can not be totally ignored.

The preliminary design of the high efficiency output power amplifier from program phase I was used as a starting point for the initial phase II design. MMInc.'s large signal FET model was used in conjunction with MMIC-SPICE, MMInc.'s enhanced version of the SPICE2 program, to optimize the design. Note that for this type of amplifier design, standard considerations of "watts per millimeter of FET gate periphery" are not applicable since the FET is operating in a highly saturate region and could almost be considered as a switch. Thus the total gate periphery chosen was larger than normally anticipated for a 5 Watt power amplifier.

A schematic diagram of the power amplifier output stage is shown in Figure 3.1-1. Complexity was kept to a minimum to reduce overall chip size. The input matching network consists of a lumped element impedance transformer which provides the high voltage swing necessary for high efficiency "switching" operation. Gate bias is injected through a spiral inductor which also absorbs the parasitic input capacitance of the power FET. The output matching network contains a resonant tank circuit which "rings" at the desired fundamental output frequency and reflects the second harmonic component back to the drain at an optimized phase angle. Drain bias is again provided through the matching structure. Two devices sharing the same input matching network and separate output matching networks are employed, and a lumped element power combiner / impedance transformer is used to arrive at the 5 watts power output level. Blocking and tuning capacitors complete the circuit design.

While the available gain of the FET is fairly high at these frequencies, loss in the passive circuit elements can be quite detrimental to the amplifier efficiency. Since these high performance FETs are only conditionally stable in the UHF band, maximum available gain is undefined; maximum stable gain is nevertheless well over 20 dB. The goal of "gain per stage" between 10 and 13 dB should be therefore be readily achievable. However a loss of 1 dB in the output network, for example, will result in a 20 % reduction of an amplifier's efficiency. Although a fully monolithic implementation of the power amplifier will result in small overall size and low assembly cost, higher efficiency may be obtainable by using some "off-chip" elements where lower loss is possible due to size and other considerations, e.g. wound coils instead of planar spiral inductors.

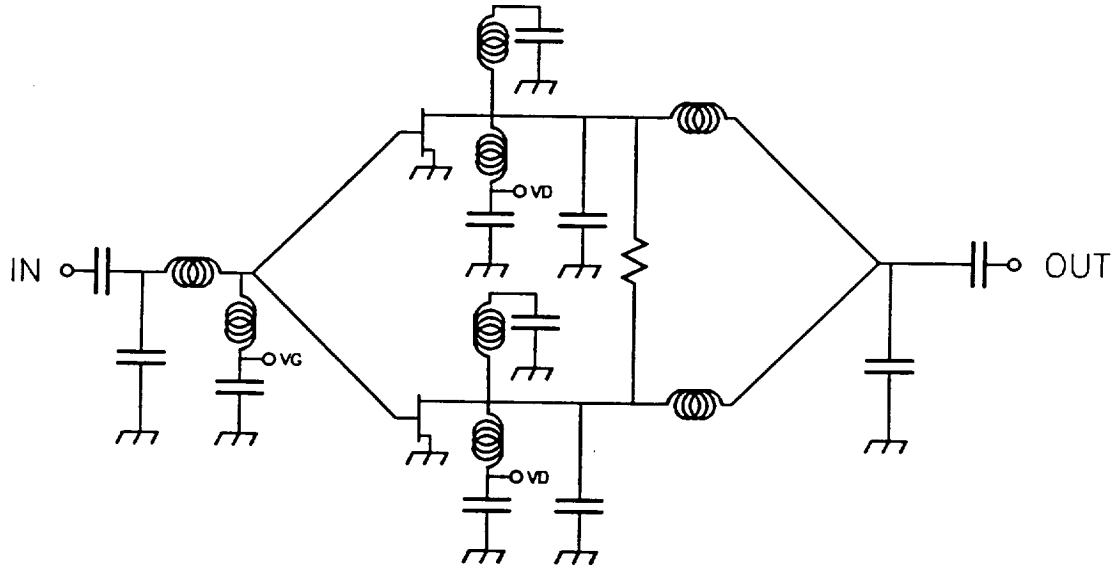


Figure 3.1-1) SCHEMATIC DIAGRAM OF GaAs MONOLITHIC POWER AMPLIFIER OUTPUT STAGE

The power amplifier output stage was therefore analyzed for three possible levels of integration. In the first case all elements are monolithically integrated "on-chip". In the other extreme all elements in the output network are located "off-chip". Other intermediate cases are possible; however the use of an off-chip power-combiner is the most likely since this can be merged into the chip carrier / package. The predicted performance for these cases is shown in Table 3.1-1. The design of the first iteration power amplifier included provisions to characterize chip operation for the various cases.

As stated above, a driver stage is needed to raise the power amplifier gain to the desired level of 23 dB beyond the phase modulator. The performance of this stage, although not as critical the output stage, should nevertheless be close to that of the latter to maintain high overall efficiency. Hence its design was similar using an appropriately-scaled power FET device. In this case, however, a fully monolithic version should provide sufficiently high efficiency. A schematic diagram of the power driver stage is shown in Figure 3.1-2. The predicted performance of this monolithic circuit is shown in Table 3.1-2.

Table 3.1-1) PREDICTED PERFORMANCE OF GaAs MONOLITHIC POWER AMPLIFIER OUTPUT STAGE @ 406.025 MHz

	GAIN	OUTPUT POWER	POWER-ADDED EFFICIENCY
ALL ELEMENTS "ON-CHIP"	11.2dB	37.3dBm (5.4W)	62 %
POWER COMBINER "OFF-CHIP"	11.8dB	37.9dBm (6.2W)	72 %
POWER COMBINER & DRAIN RESONATOR / BIAS "OFF-CHIP"	12.5dB	38.6dBm (7.2W)	83 %

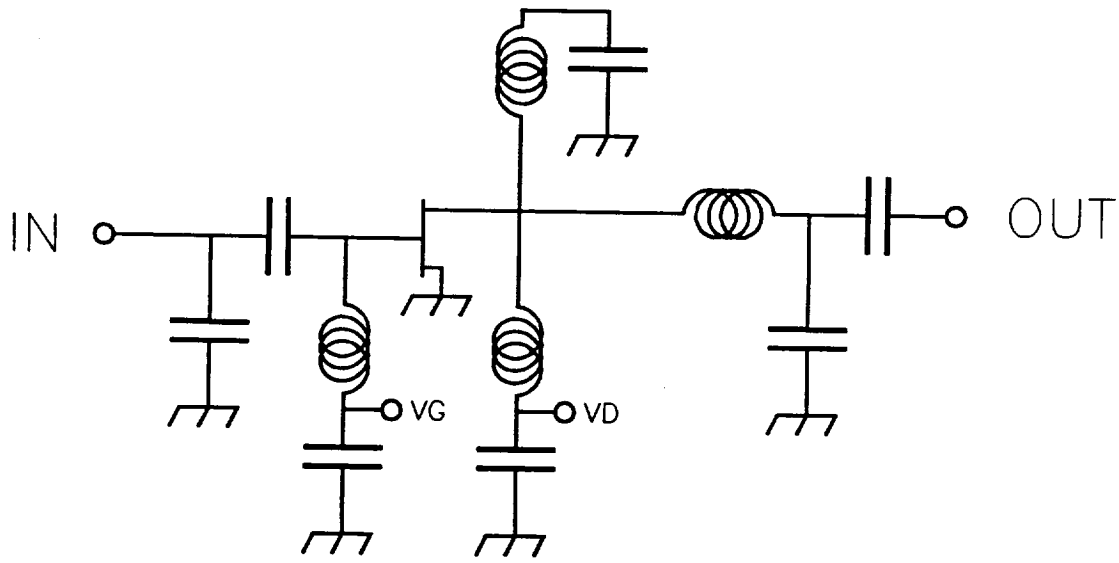


Figure 3.1-2) SCHEMATIC DIAGRAM OF GaAs MONOLITHIC POWER AMPLIFIER DRIVER STAGE

Table 3.1-2) PREDICTED PERFORMANCE OF GaAs MONOLITHIC POWER AMPLIFIER DRIVER STAGE @ 406.025 MHz

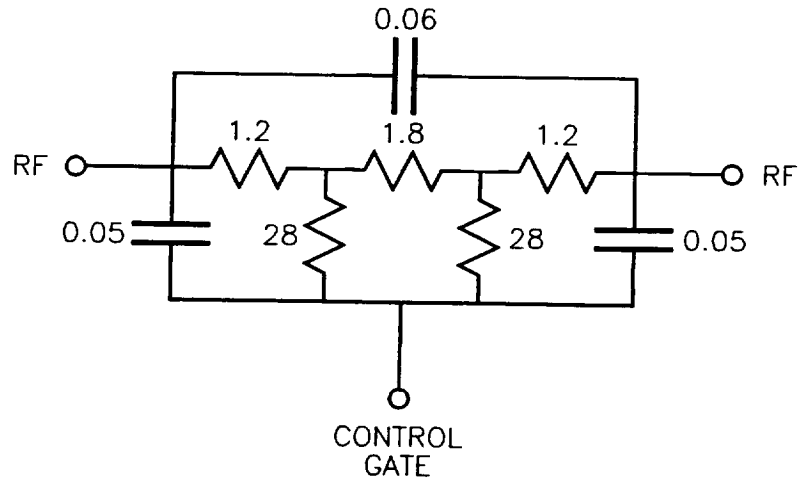
GAIN	= 11.5 dB
OUTPUT POWER	= 27.8 dBm (610 mW)
POWER-ADDED EFFICIENCY	= 61 %

3.2) BI-PHASE MODULATOR

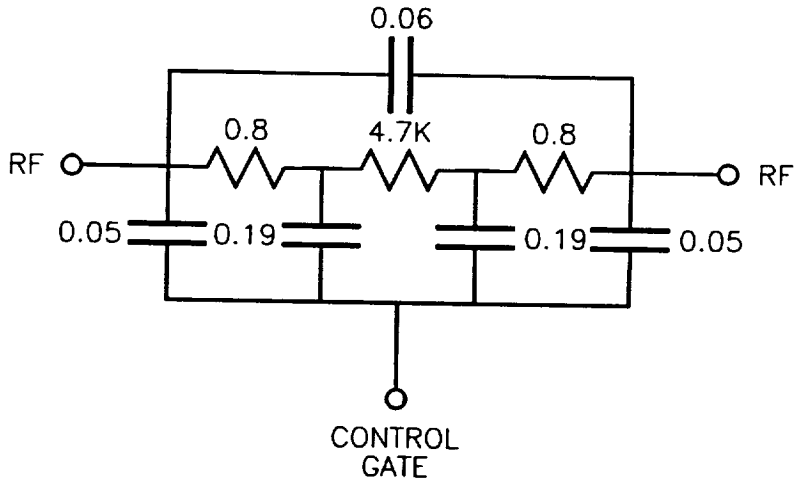
Phase modulation of the 406 MHz signal in the present circuit design is conceptually achieved by switching the input signal between two paths, each path with a phase shift equal to the two respective phase states. Switched modulators rely on highly repeatable passive elements to provide the phase shift, thus as opposed to active structures, they should provide better performance stability over temperature. Small signal GaAs FETs are used as passive switching elements. A small signal equivalent circuit model of a GaAs FET operating as a switch is shown in Figure 3.2-1. A compound switch configuration consisting of shunt and series FETs can be used to achieve high "on/off" ratio. A schematic of a compound FET switch is shown in Figure 3.2-2.

The approach taken here utilized a resistive power splitter on the input, two lumped element delay lines, matched SPDT switches for phase selection, and a resistive power combiner on the output. This is shown in Figure 3.2-3. A "pass" state is possible by switching both paths on and let the signals combine vectorially; the angle of 1.1 radians would however result in a lower signal level in the absence of additional design considerations. A "block" state is also possible by switching both paths off. The resistive networks give good match for all states. Fairly compact chip size is possible with this design. The disadvantage is that the insertion loss in each resistive network is 6 dB, resulting in a 12 dB loss in addition to the losses associated with the phase shift circuitry and the switches.

The higher insertion loss in the "pass" state for the simple-minded switched modulator can be overcome by using switched attenuators, i.e. the "switches" provide definite low and high attenuation states rather than simply "on" and "off". This was implemented as a "pi" network using additional resistors in series with the shunt FETs and in parallel with the series FET in the compound FET switch, as shown in Figure 3.2-4. Proper attenuations were obtain by adjusting the size of the FETs and selecting the resistor values.



a) In the "On" State



b) In the "Off" State

Figure 3.2-1) SMALL SIGNAL EQUIVALENT CIRCUIT OF A FET SWITCH

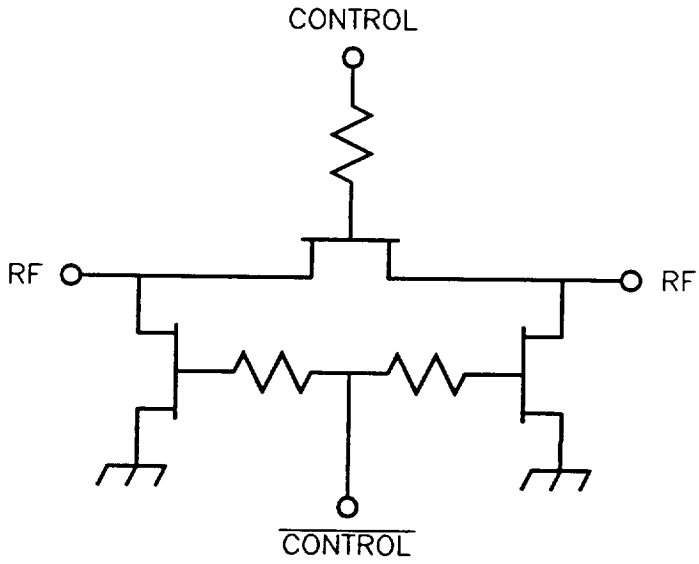


Figure 3.2-2) SCHEMATIC DIAGRAM OF A COMPOUND FET SWITCH

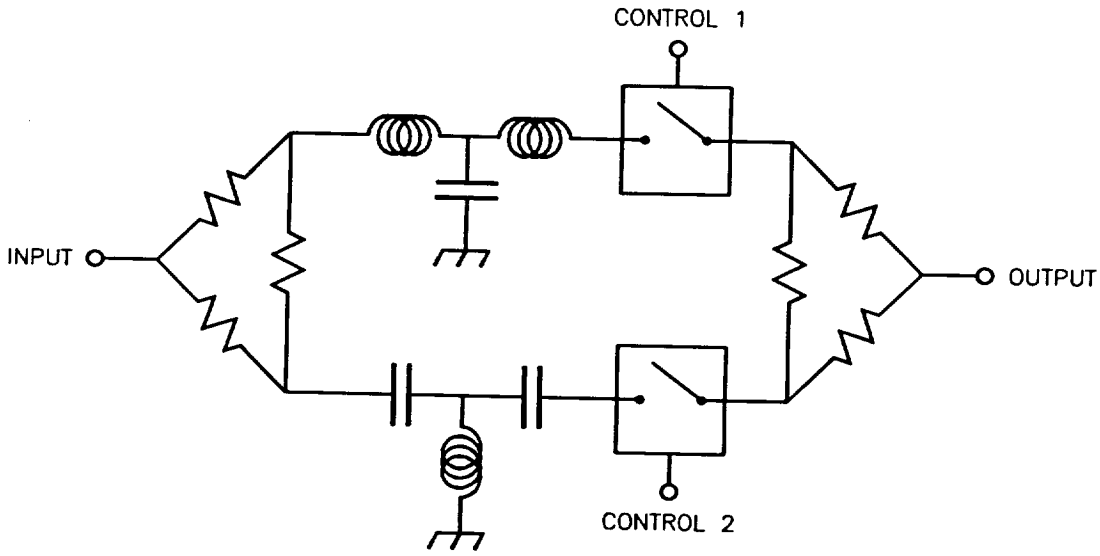


Figure 3.2-3) SCHEMATIC DIAGRAM OF A SWITCHED PHASE MODULATOR

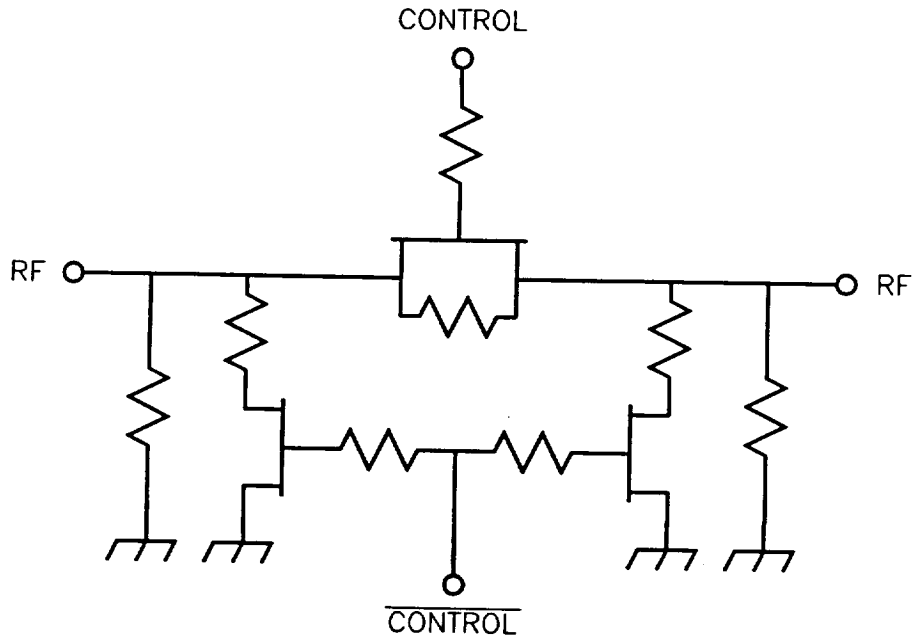


Figure 3.2-4) SCHEMATIC DIAGRAM OF A SWITCHED ATTENUATOR

A schematic diagram of the passive portion of the bi-phase modulator is shown in Figure 3.2-5. Additional on-chip internal blocking capacitors have been included so that each switched attenuator can be independently controlled with only one respective line. For simplicity this circuit was designed to operate with control signals between 0 and -5 volts to directly control the depletion mode GaAs MESFET switches. The DC ground of the entire circuit can however be level-shifted to +5 volts, either with an external capacitor or additional on-chip elements in future iterations, so that standard logic levels of 0 and +5 volts may be used.

One of the requirements for the SARSAT beacon modulator is that all phase transitions be "slow", as described in the "Specifications for COSPAS-SARSAT 406 MHz Distress Beacons".[2] Note that in the present "switched attenuator" design, the transition between the low and the high attenuation "switch" state is a smooth function of the control voltage, although the change naturally occurs rapidly within a relatively narrow range centered around the threshold voltage of the FET switching element. This can be exploited to provide the desired "slow transition" by overlapping the internal control signal waveform so that the RF signal goes from the "+1.1 radian" state (one switch at low attenuation and the other high) through the "0 radian" state (both switches at low attenuation) to the "-1.1 radian" state (one switch at high attenuation and the other low), and vice versa. The rise and fall times of the (complementary) waveforms are independently chosen so that the high attenuation "block" state (both switches at high attenuation) is never encountered. For the present effort this idea has been realized using a resistor / capacitor / diode network. The schematic diagram of this network is shown in Figure 3.2-6. This portion of the phase modulator has been implemented "off-chip" due to size considerations.

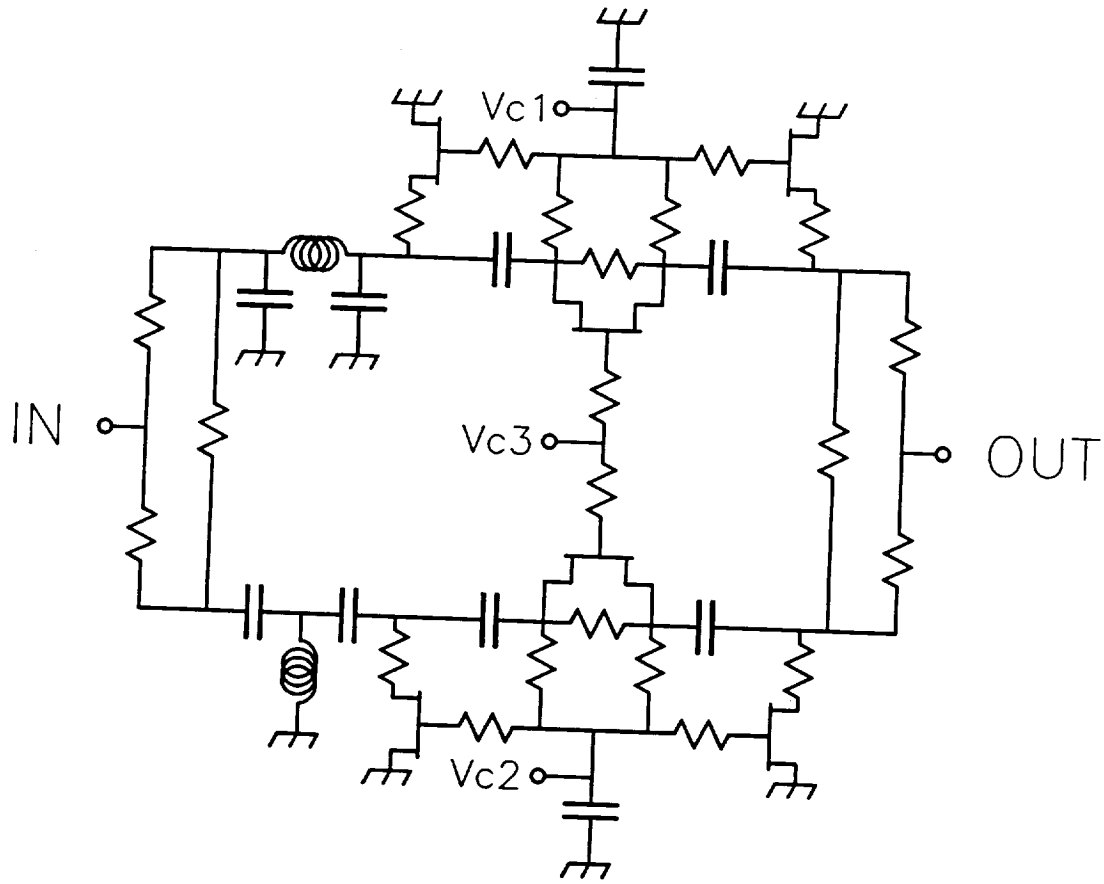


Figure 3.2-5) SCHEMATIC DIAGRAM OF THE BI-PHASE MODULATOR

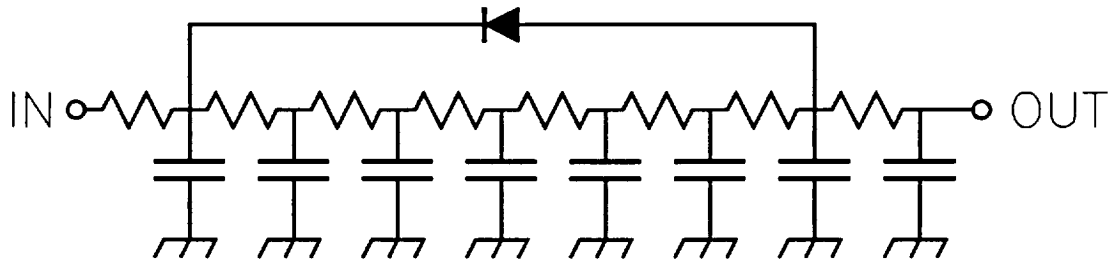


Figure 3.2-6) SCHEMATIC DIAGRAM OF DISTRIBUTED R-C SLOW-WAVE STRUCTURE

Other methods to achieve the slow phase transition are possible besides the "slow-wave" passive network. For example, the digital controller used to provide data coding and power management functions can also be used to generate the necessary waveform. Versions of microcontrollers with on chip analog input and output capability already exist with several popular architecture families, including the type used in the design of reference 1. This is a distinct possibility when the entire system is integrated.

As discussed above, a passive phase modulator followed by a buffer amplifier appeared to be a viable approach to meet the insertion loss goals. Since the FET switches do not consume any significant current, this arrangement will still stay within the power budget. The design of the buffer amplifier was similar to that of the driver amplifier. The size of GaAs FET element was scaled down appropriately, and the second harmonic resonance element was not included since this stage operates in the linear mode. The schematic diagram of this circuit is shown in Figure 3.2-7.

The predicted phase states for the "switched-attenuator" bi-phase modulator are shown in Figure 3.2-8 as a function of frequency. The predicted insertion loss of this circuit for the various phase states is shown in Figure 3.2-9. The predicted phase transition of the phase modulator with the "slow-wave" control network is shown in Figure 3.2-10. The predicted transient insert loss of the circuit is shown in Figure 3.2-11. The predicted performance of the buffer amplifier is summarized in Table 3.2-1. Both circuits are well matched to 50 ohms thus making them easy to characterize as individual circuits as well as a combined unit.

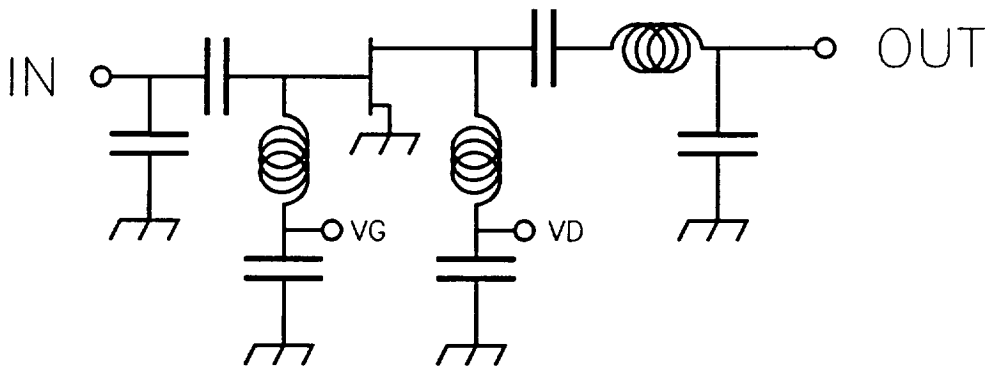


Figure 3.2-7) SCHEMATIC DIAGRAM OF THE BUFFER AMPLIFIER

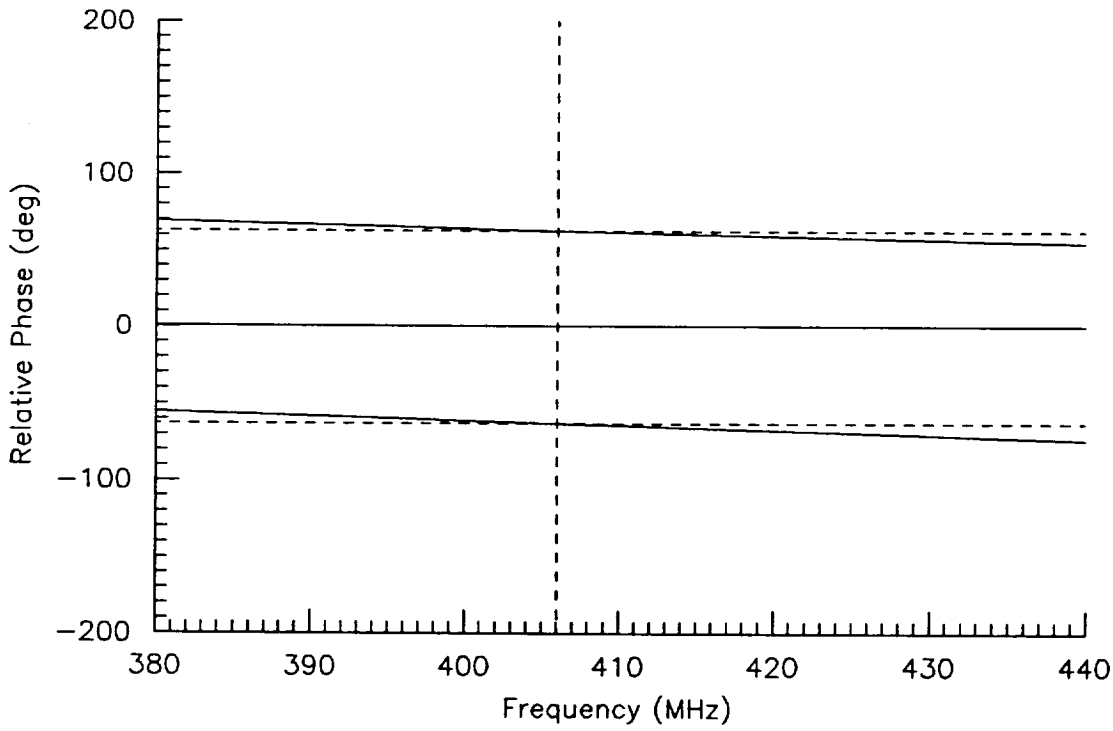


Figure 3.2-8) PREDICTED PHASE STATES VERSUS FREQUENCY OF THE BI-PHASE MODULATOR

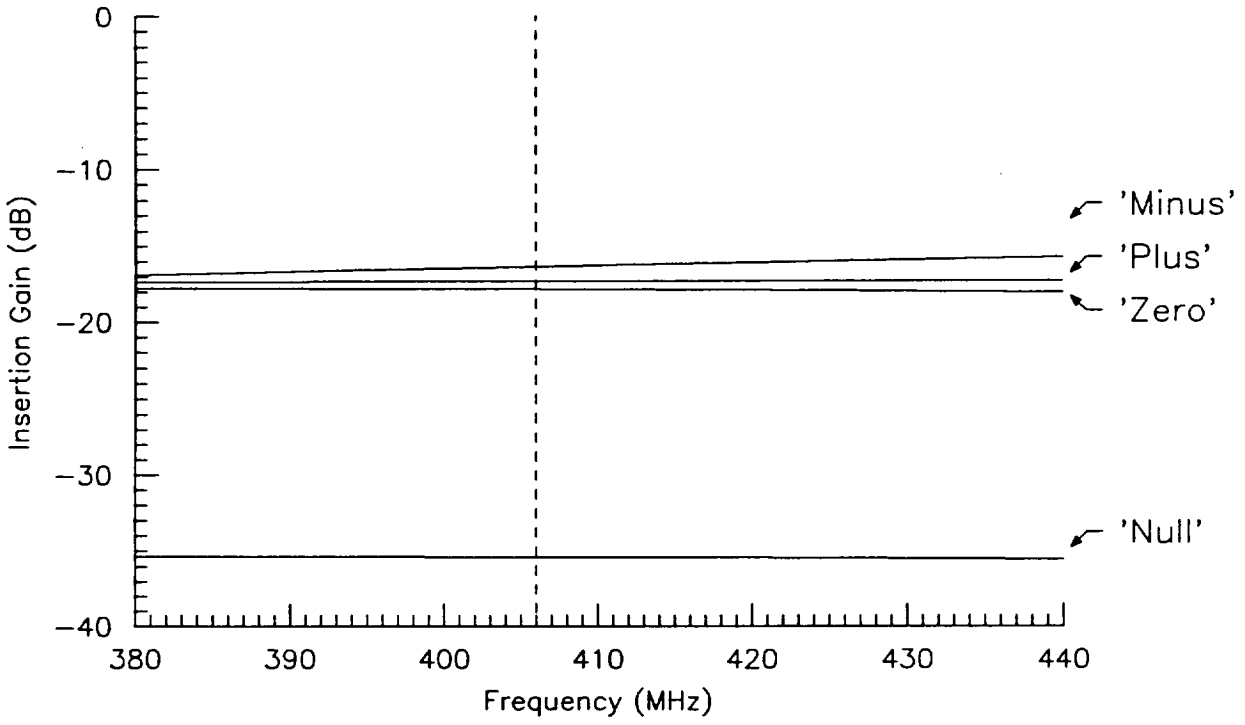


Figure 3.2-9) PREDICTED INSERTION LOSS VERSUS FREQUENCY OF THE BI-PHASE MODULATOR

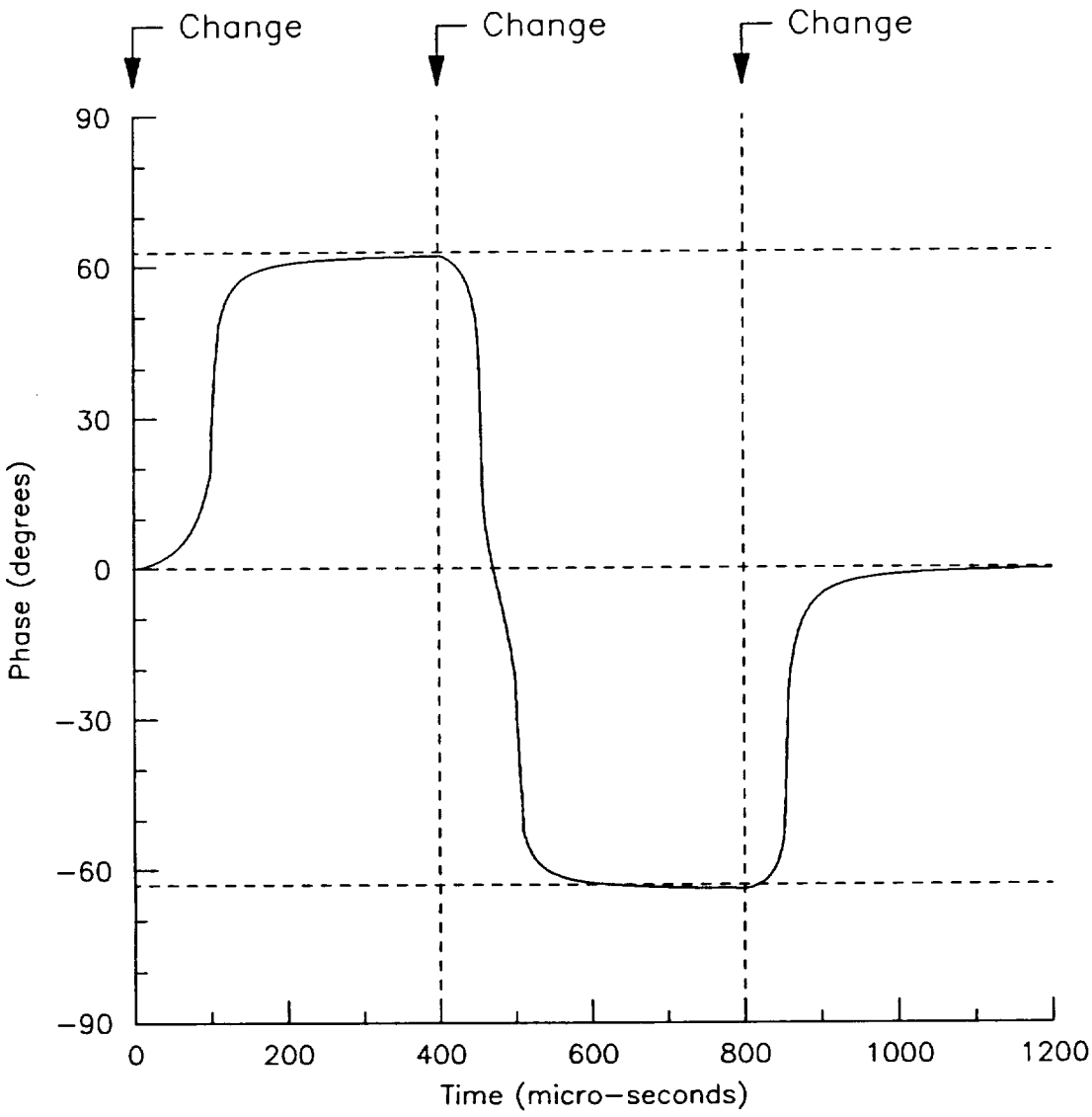


Figure 3.2-10) PREDICTED PHASE TRANSITION OF THE BI-PHASE MODULATOR

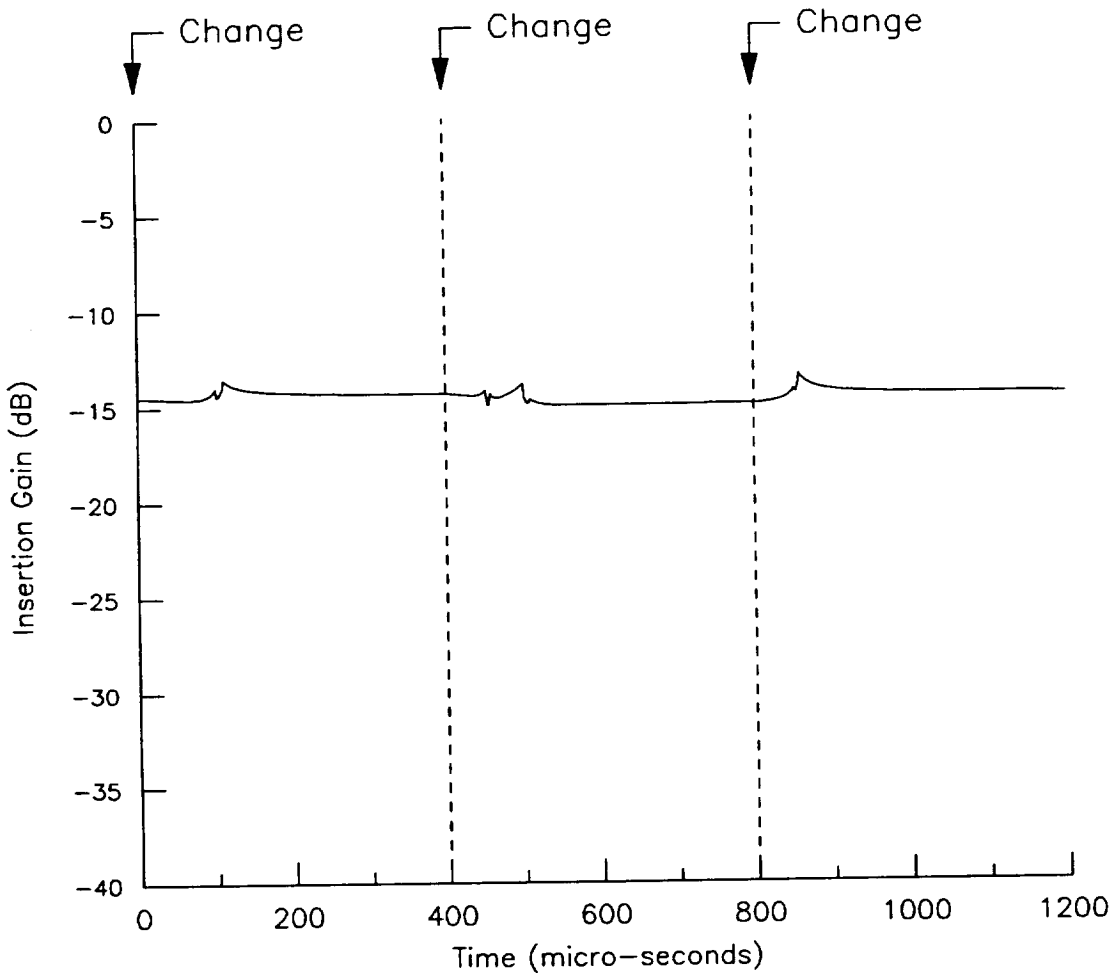


Figure 3.2-11) PREDICTED TRANSIENT INSERTION LOSS OF THE BI-PHASE MODULATOR

Table 3.2-1) PREDICTED PERFORMANCE OF GaAs MONOLITHIC BUFFER AMPLIFIER @ 406.025 MHz

SMALL SIGNAL GAIN	= 12.5 dB
OUTPUT @ 1 dB COMP.	= 19.3 dBm (85 mW)
STAND-BY DRAIN CURRENT	= 5 mA

3.3) MASK TOOL SET LAYOUT

After the circuits were designed and optimized using MMInc.'s extensive linear and nonlinear circuit analysis tools, layouts of the monolithic circuits were generated. Trade offs between chip compactness and undesirable inter-element interactions were considered, and the designs were re-optimized. The database for the finalized layout was then transmitted to the mask tool vendor to fabricate the photolithographic mask tool plates.

As discussed above, it was desirable during the first iteration to investigate the effect of different levels of monolithic integration to the performance of the power amplifier output stage. This option was therefore designed into this iteration as a separate circuit matched to 50 ohms for convenient characterization. Provisions were included to selectively replace on-chip output matching elements with off-chip components during assembly for testing. A computer generated pen plot of the power amplifier output stage is shown in Figure 3.3-1. The size of this chip is 4.0 mm by 2.9 mm.

It is also desirable during the initial iteration to test the various parts (the power splitter / combiner, the delay lines, and the FET switched attenuator) of the passive phase modulator. To accomplish this, probing and bonding areas were included in the interior of the chip. On the other hand, both the driver amplifier and the buffer amplifier resulted in fairly compact layouts. Hence the two amplifier stages were grouped together as one "circuit" in the first iteration mask tool set with the provision to separate them for individual characterization. A pen plot of this "circuit" is shown in Figure 3.3-2. The size of this chip is 3.3 mm by 2.6 mm. A pen plot of the passive portion of the phase modulator is shown in Figure 3.3-3. The size of this chip is 4.0 mm by 1.7 mm. A pen plot of the complete MMIC RF module is shown in Figure 3.3-4.

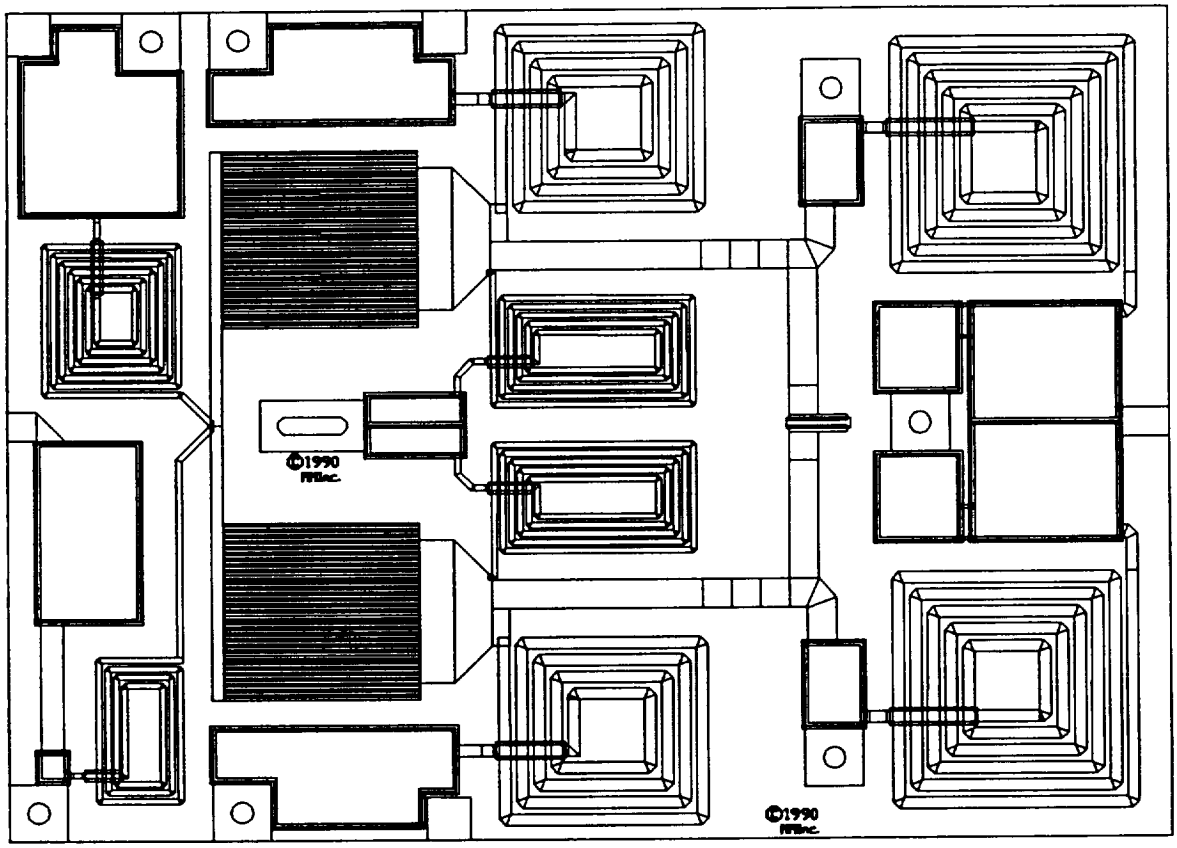


Figure 3.3-1) PEN PLOT OF THE FIRST ITERATION
POWER AMPLIFIER OUTPUT STAGE

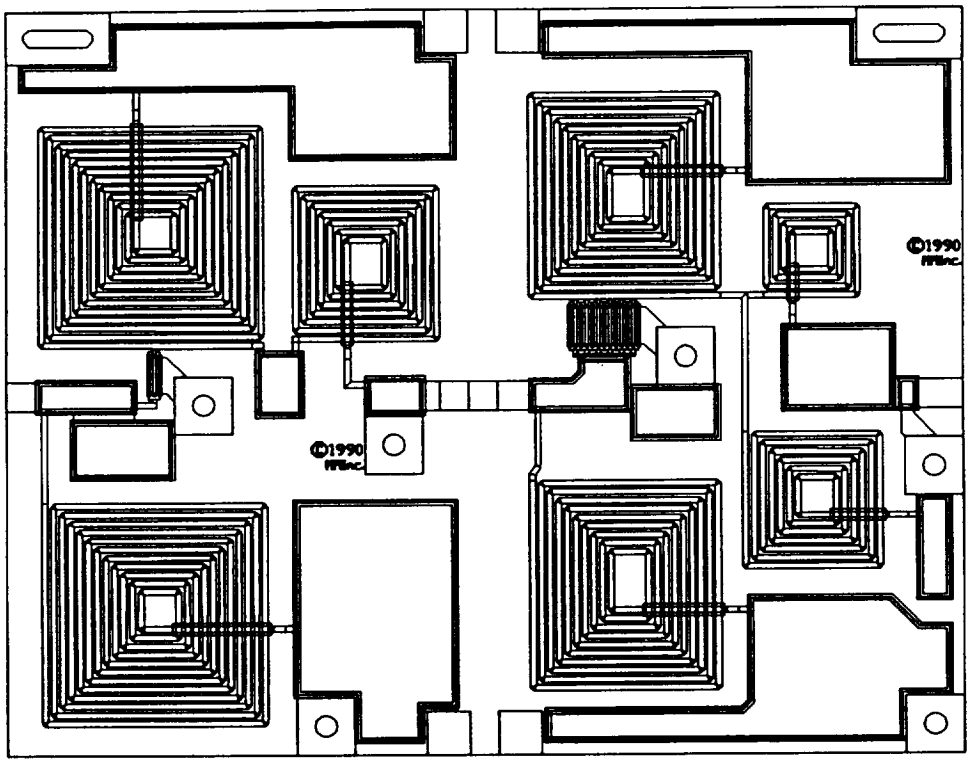


Figure 3.3-2) PEN PLOT OF THE FIRST ITERATION POWER AMPLIFIER DRIVER STAGE AND BUFFER AMPLIFIER

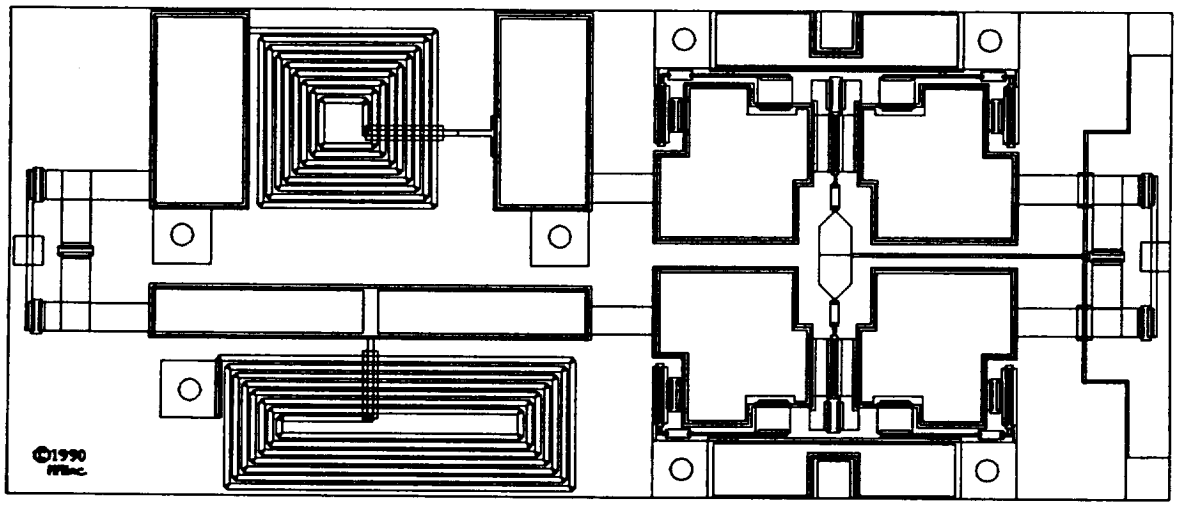


Figure 3.3-3) PEN PLOT OF THEN FIRST ITERATION PASSIVE PHASE MODULATOR

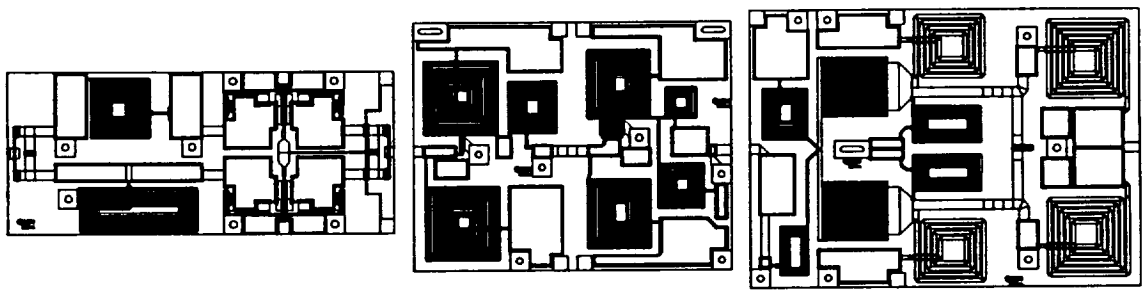


Figure 3.3-4) PEN PLOT OF THE FIRST ITERATION MMIC RF MODULE CHIP SET

4) MMIC BEACON RF MODULE FABRICATION

MMInc.'s GaAs wafer processing technology utilized in the fabricating of the beacon RF module MMIC components is described in this section. High efficiency GaAs power MESFET technology is essential to the power amplifier circuit, and is described in section 4.1. MMInc.'s proprietary "Flash Annealing" process is a important materials technique towards realizing these devices, and is described in section 4.2. MMIC fabrication is described in section 4.3.

4.1) HIGH EFFICIENCY POWER FET DEVICE

In order to obtain optimal performance from a power FET at microwave frequencies, considerations must be given in the design phase to areas related to the electrical, mechanical, and thermal characteristics. For example, based on the requirements of frequency of operation and output power, one can determine relevant parameters such as device size and pinch-off voltage. However, since the electrical characteristics are temperature-dependent, one must also take the rise in junction temperature due to the dissipated power into account. This could influence the device layout as well as other aspects such as final wafer thickness. For MMICs the latter is of course not a free variable. In addition to the usual consideration of mechanical strength for handling purposes the GaAs substrate also forms the dielectric for the transmission lines (microstrips) and spiral inductors, its thickness therefore directly affects the attainable impedance and loss. Thus a successful FET design must come from a self-consistent set of considerations and trade-offs among these areas.

The ideal doping profile for power FETs should provide the following features:

1. Abrupt Pinch-off
2. Good Linearity
3. High Breakdown Voltage
4. High and Uniform Transconductance

All these factors affect the performance of the power FET in terms of maximum output power, efficiency, and dynamic range. The general shape of such a doping profile starts with a low surface concentration, followed by a retrograde shape of rising doping level with depth, and ending in a abrupt drop in doping level at the active layer-substrate interface. In reality, a perfectly abrupt carrier profile cannot be obtained at finite temperature due to diffusion. It is therefore sufficient in tailoring the profile to choose a falling slope that is consistent with the given peak doping concentration.

MMInc.'s existing high efficiency GaAs power FETs had already demonstrated spectacular performance at the 400 MHz band during program phase I. These devices were originally designed for linear power amplification (Class A to Class B) at microwave frequencies. Additional power devices have been fabricated at the onset of program phase II using a doping profile suitable for "switching" operation and relaxed gate dimension for high yield. Typical DC characteristics of a small size test FET structure is shown in Figure 4.1-1. A device with a periphery of one quarter of the total device periphery used in the 5 watt power amplifier output stage has been characterized to extrapolate the monolithic circuit performance. Large signal performance of this device has been measured using external tuners, and the results are shown in Table 4.1-1. An output power of 1.4 watts with a power-added efficiency of 75 % and an associated gain of 15 dB have been measured. Since this exercise was intended to check out the refined doping profile design and relaxed device geometry, no attempt was made to determine the "ultimate" performance.

As a check of the device characteristics prior to MMIC fabrication, a simple "hybrid amplifier" was also constructed using one of these devices. The measured performance is also shown in Table 4.1-1. In spite of the crude matching networks used for expediency, the "hybrid amplifier" nevertheless performs fairly well and provided further confidence for the following efforts.

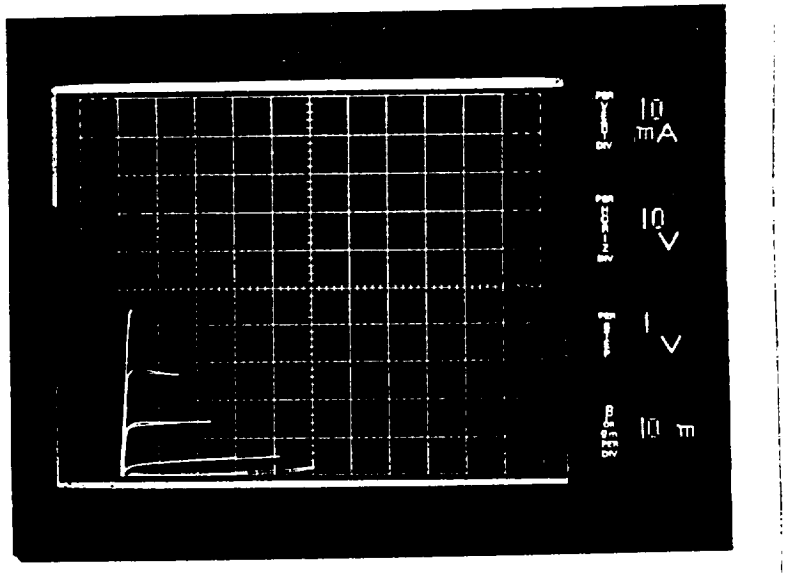


Figure 4.1-1) TYPICAL DC CHARACTERISTICS OF A POWER FET TEST STRUCTURE

Table 4.1-1) MEASURED FET AND "HYBRID AMPLIFIER" PERFORMANCE

1/4 SIZE POWER FET:	OUTPUT POWER	1.4 WATTS
	EFFICIENCY	75 %
	GAIN	15 dB
	DRAIN VOLTAGE	9 VOLTS
"HYBRID AMPLIFIER":	OUTPUT POWER	1.1 WATT
	PEAK EFFICIENCY	60 %
	GAIN	12 dB
	DRAIN VOLTAGE	9 VOLTS

4.2) FLASH ANNEALING

Ion implantation is a proven materials technology for GaAs FET and MMIC fabrication. Its advantages include simplicity of process, high uniformity and repeatability, and potential high throughput in volume production. The very thin active layer required by the present FETs is usually difficult to reproducibly prepare by other methods such as VPE (vapor phase epitaxy). The doping profile of ion implanted active layers, on the other hand, is determined by scattering at the atomic level, and is inherently predictable. Implantation into state-of-the-art bulk grown semi-insulating GaAs and high purity buffer layers has demonstrated excellent control of activation. This is hence a viable materials technology for accomplishing the program goals.

A severe limitation associated with conventional ion implantation technology is the requirement of annealing at temperatures of 850^{o}C for periods of 30 minutes. For example, the diffusion length of Si in GaAs due to this annealing cycle is about 0.06 micron. This would certainly degrade the implant layer for the required devices. A method developed at MMInc., the Flash Annealing technique, reduces the dwell time at high temperature drastically, from typically 30 minutes to less than 10 seconds. A typical temperature versus time profile of a flash annealing cycle is shown in Figure 4.2-1. A peak temperature of nearly 1000^{o}C can be reached in about 5 seconds. Good activation has been obtained at peak temperatures as low as 800^{o}C. Diffusion of impurities has been shown to be minimal. The quality of the annealed material is excellent as indicated by the high mobility. Low sheet resistivity n^{+} layers have also been obtained using this method. Ti-W/Au Schottky barrier gates on n-GaAs which have been shown to exhibit insignificant degradation in diode characteristics at processing temperatures up to 900^{o}C are also compatible with the Flash Annealing process.

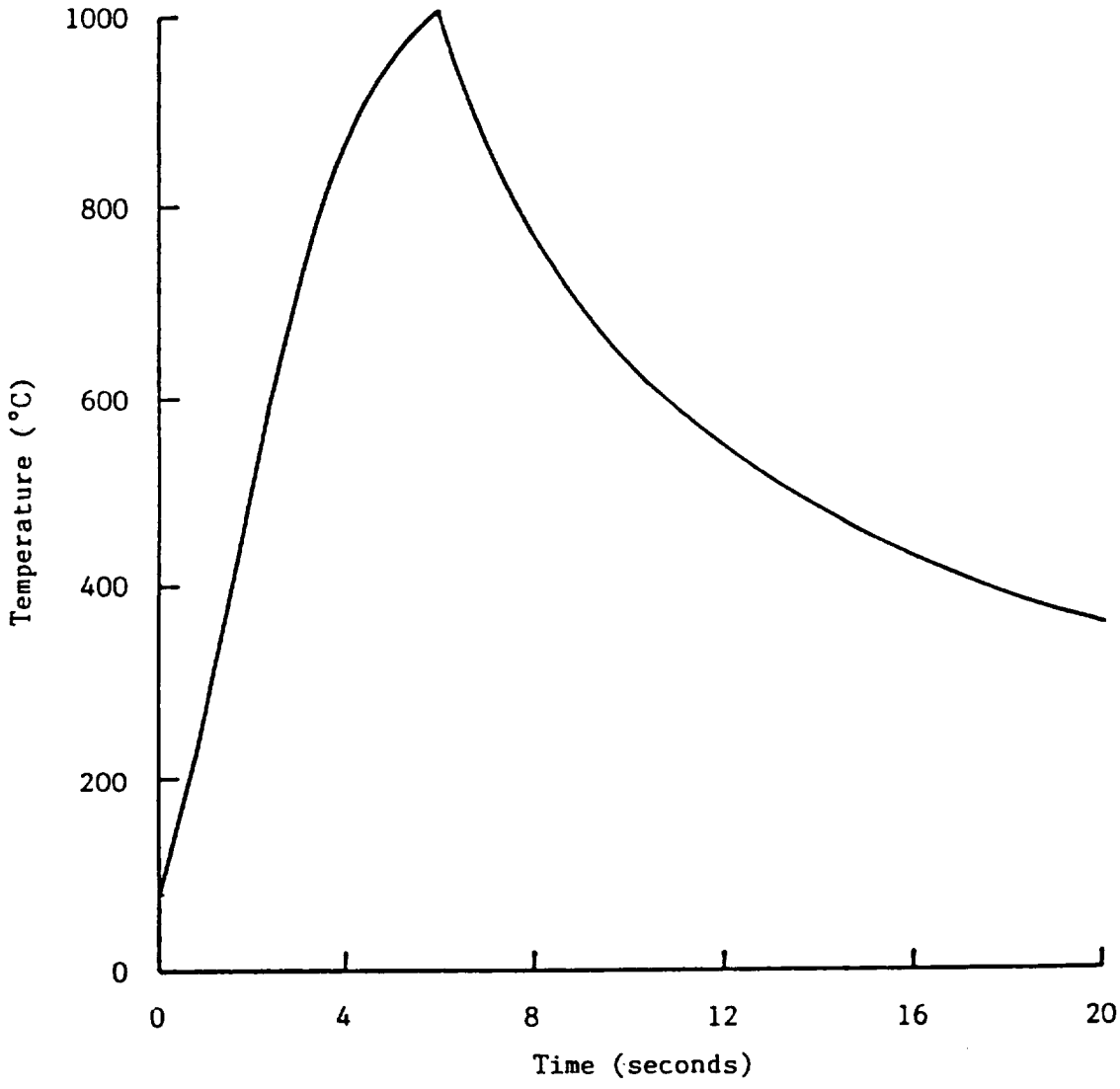


Figure 4.2-1) TYPICAL TEMPERATURE VERSUS TIME PROFILE OF A FLASH ANNEALING CYCLE

4.3) MMIC Processing Sequence

A summary of the processing sequence for the MMICs fabricated under this program is shown in Table 4.3-1. The processing starts with properly prepared GaAs substrates.

Resistors can be implemented by either ion implantation or metalization. In the former case the FET implant doses or separate implants can also be used if a selective implant scheme is employed. Ohmic contacts and electrode metalizations are then formed at the same time as the FETs, and hence no additional processing steps are required.

For low inductance on-chip grounding, substrate via connections are used. Via holes are formed after the wafers have been thinned to their final thickness. The backside of the wafer is then metalized for ease of die-attach and low thermal resistance. This also forms the ground plane for the RF circuitry in MMICs. Individual chips are obtained following dicing.

Table 4.3-1) STANDARD MMIC PROCESSING SEQUENCE

1.	Ion Implantation		1'. Implant Mask
2.	Annealing	or	2'. Ion Implantation
3.	Mesa Etch		3'. Annealing

- - - - - - - - - -

4. Ohmic Contact
5. Gate
6. Overlay (First Layer) Metalization
7. Dielectric(s)
8. Additional Layer(s) Metalization
9. Wafer Thinning, Via Hole Etching, and Backside Metalization
10. Dicing

5) BEACON RF MODULE MMIC COMPONENT CHARACTERIZATION

The approach in the design and fabrication of circuits at MMInc. is to take full advantage of computer modeling and analysis using the full extent of computer resources available. Toward this end all aspects of the circuit design and fabrication process were modeled, including circuit responses, parasitic effects, mask layouts, interference coupling, doping profiles, via hole construction, FET equivalent circuit models, etc. In addition to this growing data base of design information; a sophisticated, proprietary software package has been developed to analyze and optimize the various characteristics that are somewhat unique to monolithic circuits. Because of the extensive analysis conducted on each circuit prior to fabrication, a high probability of success can be assured with very few iterations.

As each circuit is built, several built-in monitoring points are tested and evaluated during each step of the fabrication process. At each step measured data samples are taken and correlated with the computer model. This multi-step process assures that each wafer is made according to specification, and that the computer models are continuously updated. When new circuit elements or processing steps are introduced, computer models are updated and refined to reflect the characteristic performance of the final circuit.

In-processing tests designed to monitor and adjust the processing sequence are routinely conducted. These tests are done using probes on a test pattern which is built into every wafer. Both DC and low frequency wafer measurements are used to monitor the fabrication process. This data is analyzed and compared with the original models so that predictions of the final chip characteristics can be made in the early processing stages of the wafer. The technique of using process monitoring data is an extremely valuable part of the manufacturing process at MMInc. not only because it allows prediction of the final performance of the chips being processed, but also because it allows updating of the data base to maintain precise control of the fabrication process on all future wafers.

5.1) MMIC TEST CARRIER AND FIXTURING

As a practical matter and to prevent damage during RF testing the chips are soldered down on a gold plated carrier whose thermal expansion coefficient matches that of the GaAs. A Cu/W composite material produced by powdered metallurgy is used as it is a hard, stable material that will not bend easily, matches the thermal coefficient of expansion of GaAs, and is a good thermal conductor. This material can be readily plated with gold so that monolithic chips can be soldered to it with a suitable eutectic solder.

The MMIC chips designed and fabricated in this program were first tested and characterized in a test fixture routinely used at MMInc. for measurements at much higher frequencies (beyond 20 GHz). Extensive de-embedding of the test fixture is not required for the present 406 MHz measurements. The excellent match to 50 ohms provided by this fixture nevertheless permits later mounting of the chips on carriers into packages without significant perturbation to their performance. The packaged circuits were subsequently measured to verify the data.

5.2) RF MEASUREMENT SETUP

RF testing of small signal circuits (phase modulator and buffer amplifier) was performed on a HP-8510 vector network analyzer with a HP-8340 frequency synthesizer source. The signal source and the network analyzer are connected to a personal computer based data acquisition system which is in turn networked with a RISC server computer for additional resources in data analysis.

Measurement on the large signal circuits (power amplifier) was performed using the setup shown in Figure 5.2-1. The signal from the source was further amplified by a custom constructed UHF power amplifier to the level required by the "device under test". The incident and output powers were measured using RF power meters with appropriated power attenuators attached to the detectors. The output signal was also monitored for harmonic content through a Tektronix 492 spectrum analyzer.

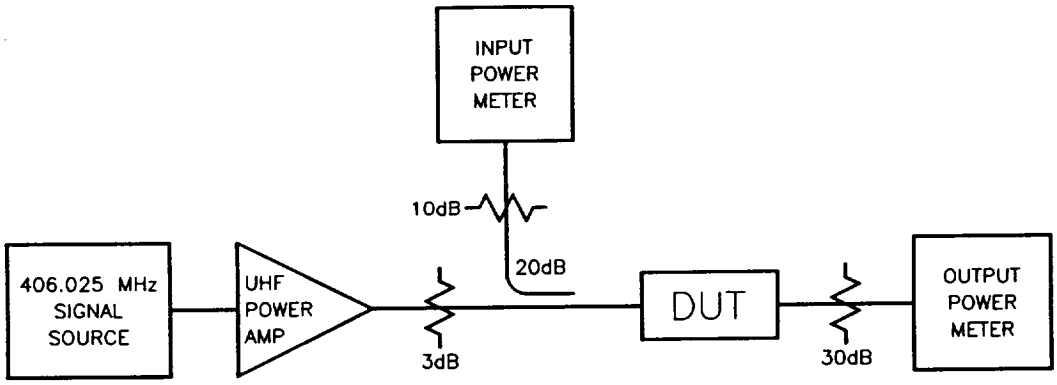


Figure 5.2-1) LARGE SIGNAL POWER AMPLIFIER MEASUREMENT SETUP

6) MEASURED PERFORMANCE OF FIRST ITERATION MMIC COMPONENTS

As discussed in section 4, the first iteration monolithic circuits were designed to allow characterization of the individual stages. This is preferred to extract the maximum amount of data for the next iteration. Hence the performance of the power output stage, the driver, the passive phase modulator, and the buffer amplifier had individually been measured, and the results are described in the following sections.

6.1) HIGH EFFICIENCY POWER AMPLIFIER

The measured performance of a first iteration power amplifier output stage is shown in Table 6.1-1. The circuit was biased at a drain voltage of 9 volts, which is the lower limit depicted for the program goals shown in Table 2.1-1. The measured output power was within -1.5 dB of the goal of 5 watts. The associated gain of 13 dB agreed well with predictions. The power-added efficiency of this monolithic circuit was however only in the high forty percent range. This is due to excessive loss in the output matching network. Investigation of this aspect during the second design iteration is described in section 7.

The measured output power versus frequency under fixed input power is shown in Figure 6.1-1. A fairly wide frequency range of operation was observed. The measured data was in fact limited by the UHF amplifier in the present 406 MHz measurement system which has a range of 403 to 440 MHz.

The power amplifier driver stage was also separated from the buffer amplifier and measured. The results are shown in Table 6.1-2. The performance was fairly close to predictions and well within expectations for the first iteration. The measured output power versus input power of a power amplifier driver stage is shown in Figure 6.1-2.

Table 6.1-1) MEASURED PERFORMANCE OF A FIRST ITERATION POWER AMPLIFIER OUTPUT STAGE

FREQUENCY	406.025 MHz
OUTPUT POWER	3.5 Watts
ASSOCIATED GAIN	13 dB

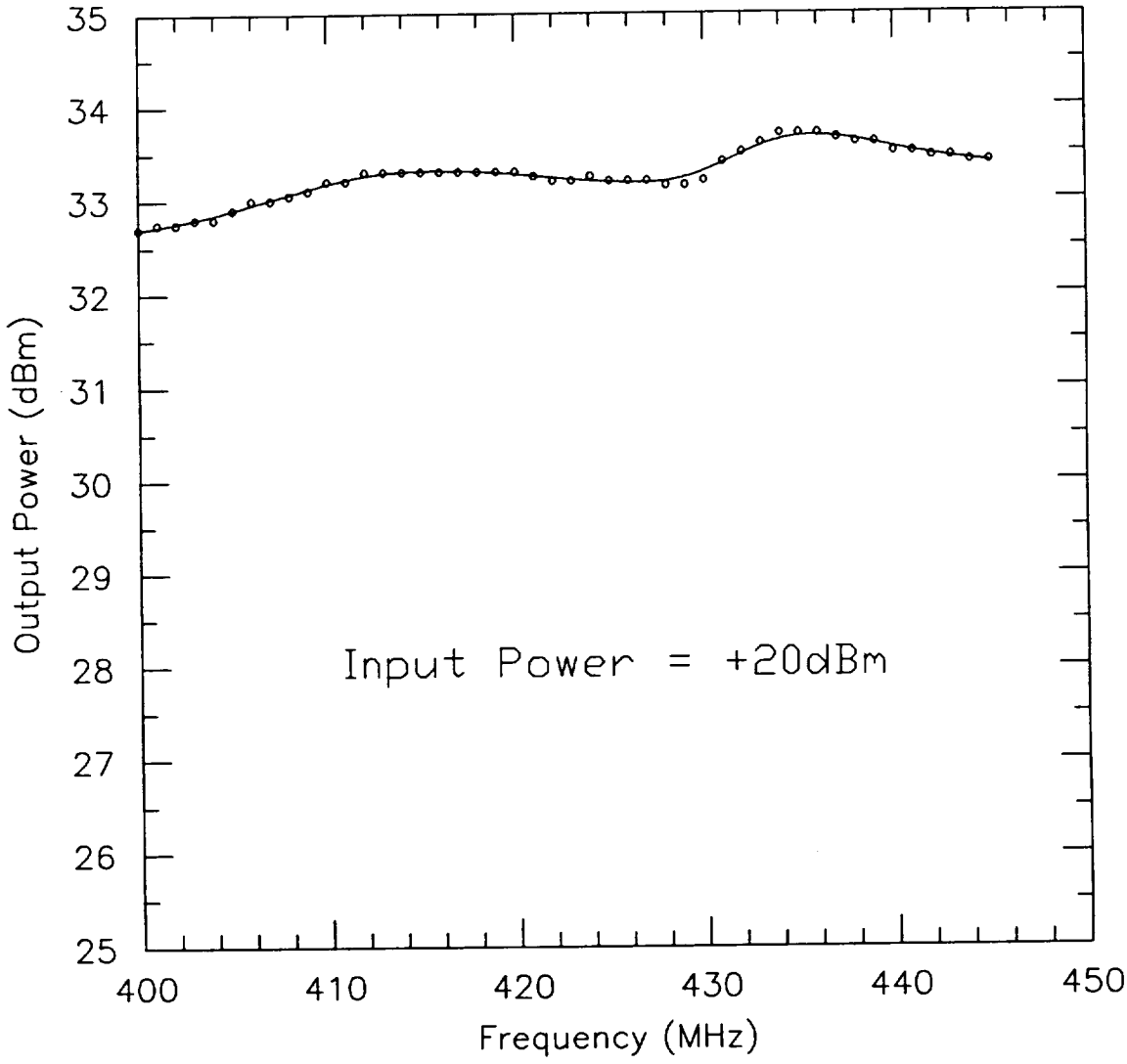


Figure 6.1-1) MEASURED OUTPUT POWER VERSUS FREQUENCY OF A FIRST ITERATION POWER AMPLIFIER OUTPUT STAGE

Table 6.1-2) MEASURED PERFORMANCE OF A FIRST ITERATION POWER AMPLIFIER DRIVER STAGE

FREQUENCY	406.025 MHz
OUTPUT POWER	0.43 Watts
ASSOCIATED GAIN	11 dB

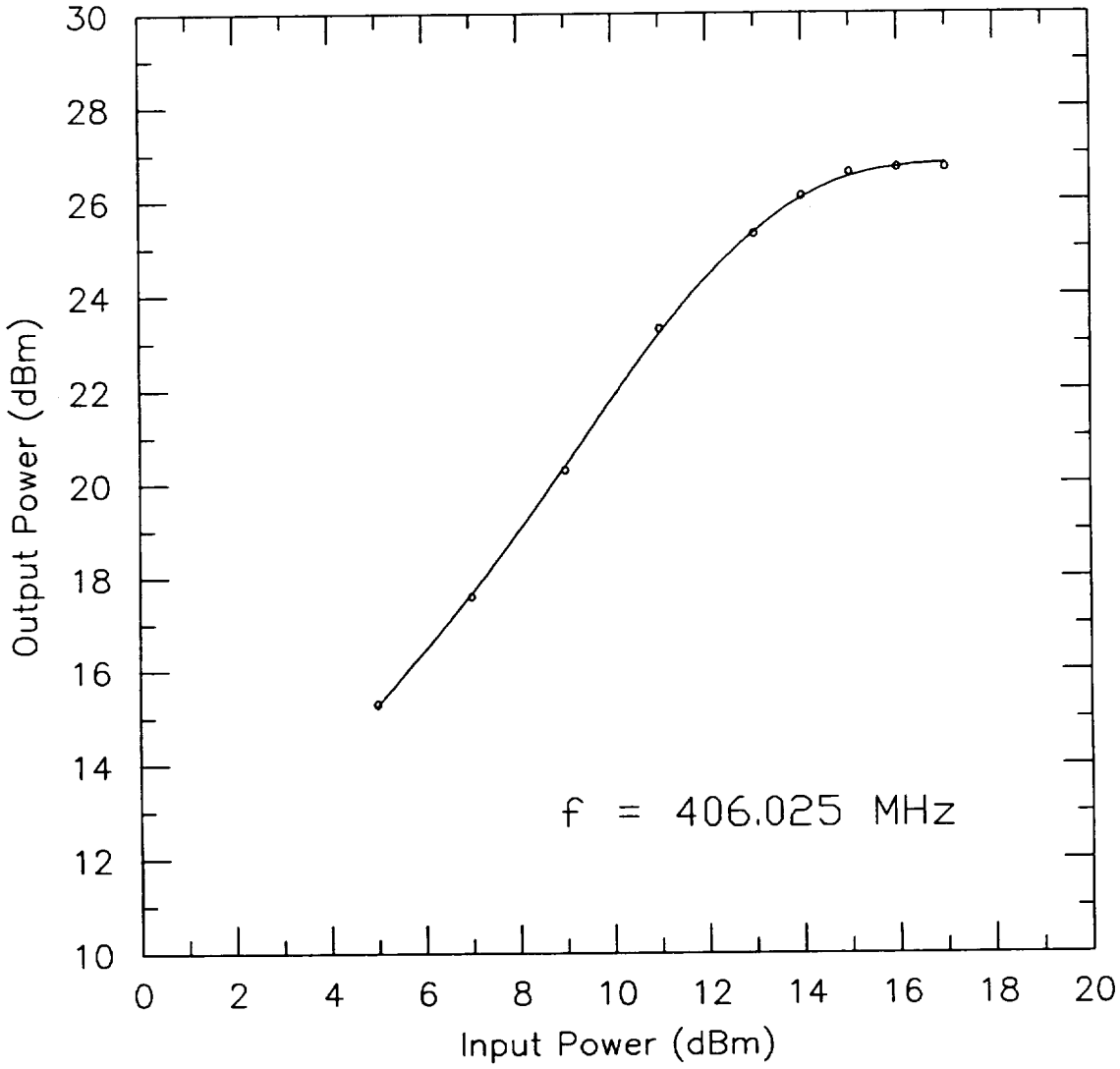


Figure 6.1-2) MEASURED OUTPUT POWER VERSUS INPUT POWER OF A FIRST ITERATION POWER AMPLIFIER DRIVER STAGE

6.2) BI-PHASE MODULATOR

Characterization of the first iteration bi-phase modulator, both the passive portion and the buffer amplifier, was delayed considerably by mask fabrication errors by the vendor and additional problems encountered by the vendor in several attempts to correct them. A workable mask tool set was eventually obtained to fabricate a sufficient number of first iteration circuit for data extraction.

Measured insertion phase of the (passive) phase modulator is shown in Figure 6.2-1 for the various phase states. While the phase difference between the "plus" and the "minus" states was approximately correct, there was a offset in the "zero" state leading to apparent phase errors in the data referenced to the "zero" state. The problem was in the FET-switched attenuator. This was subsequently analyzed separately and the results were used in making the second design iteration. The insertion loss of the (passive) phase modulator is shown in Figure 6.2-2. The problem with the switched attenuators is more evident here where the insertion losses in the "plus" and "minus" states were reasonably close to the expected -16 dB range whereas the "zero" state was much higher. As expected, the "null" state provided an additional attenuation of about 10 dB.

The measured performance of the buffer amplifier is shown in Figure 6.2-2. The peak gain was fairly close to expectation, except its location was shifted to a higher frequency. This was adjusted in the second design iteration.

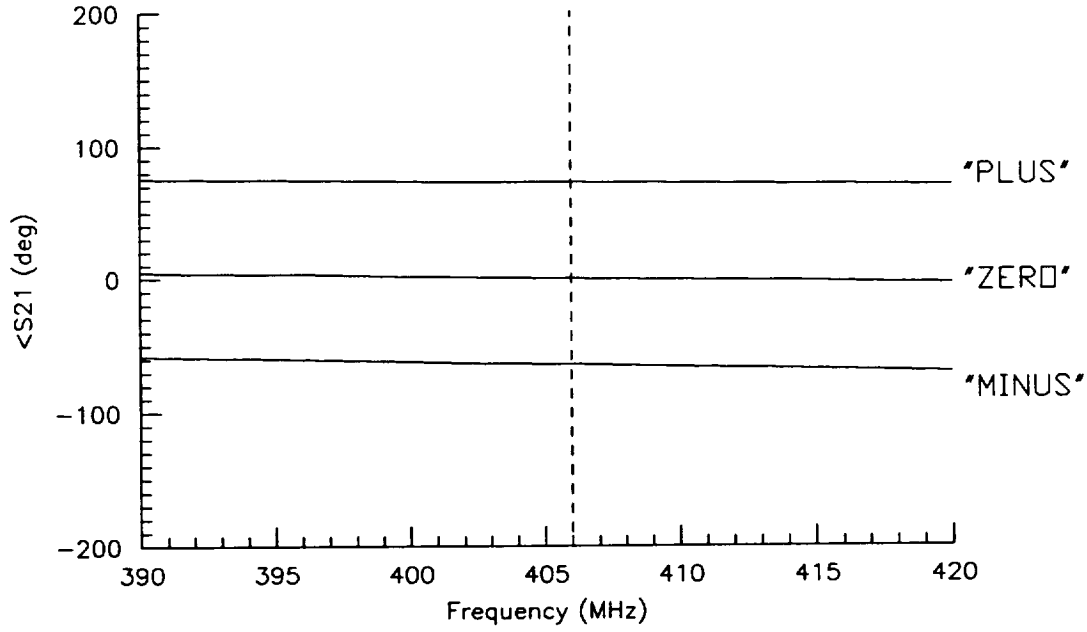


Figure 6.2-1) MEASURED PHASE STATES VERSUS FREQUENCY OF A FIRST ITERATION PHASE MODULATOR

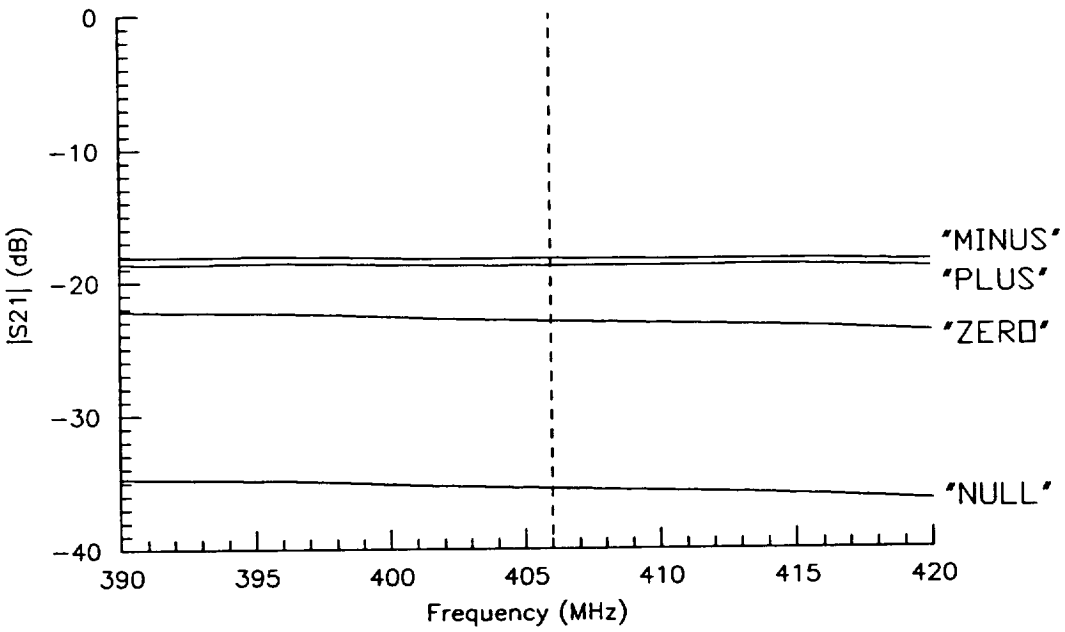


Figure 6.2-2) MEASURED INSERTION LOSS VERSUS FREQUENCY OF A FIRST ITERATION PASSIVE PHASE MODULATOR

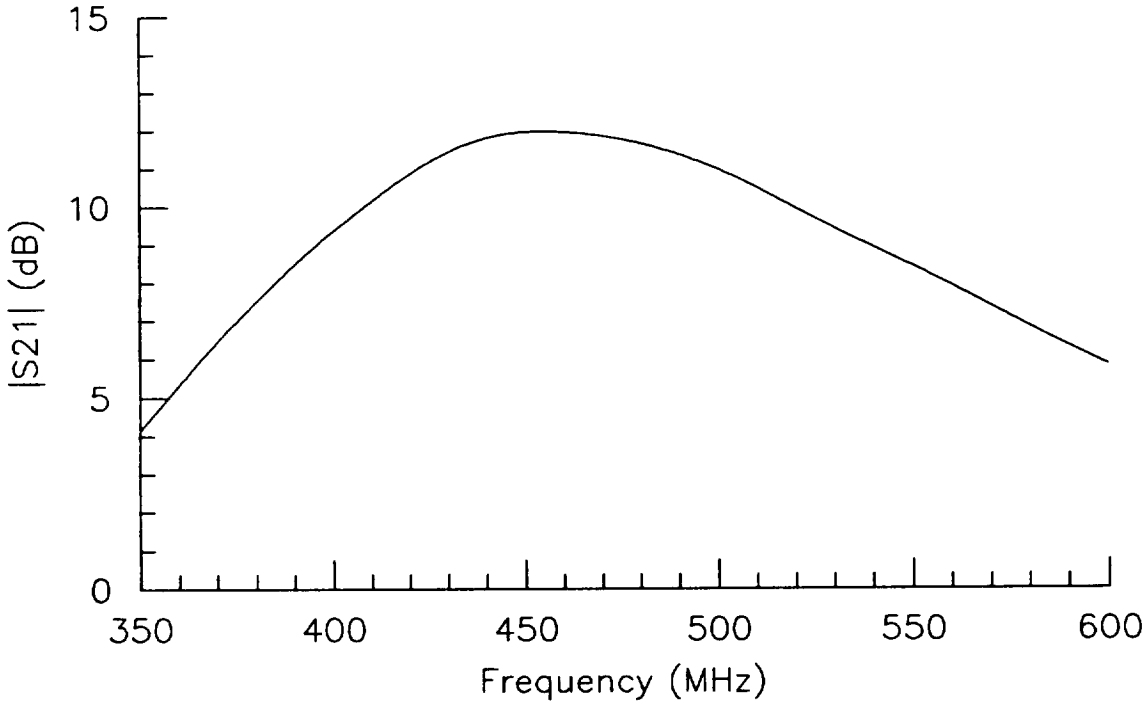


Figure 6.2-3) MEASURED GAIN VERSUS FREQUENCY OF A FIRST ITERATION BUFFER AMPLIFIER

7) GaAs MONOLITHIC RF MODULE DESIGN ITERATION

A second design iteration of the RF module MMIC chip set has been performed based on comparison of predicted performance and measured results of the first iteration circuits. The circuits were adjusted and further optimized. Chip partitioning was re-addressed based on this experience and other considerations, and a second mask tool set was procured.

This design iteration of the monolithic circuits is described in the following sections.

7.1) HIGH EFFICIENCY TWO-STAGE POWER AMPLIFIER

The measured results for the first iteration power amplifier agreed reasonably well with the predicted performance. The power gains of both stages were fairly high. The output powers were slightly lower than expectation. This was found to correlate well with the lower than predicted power-added efficiency. Note that a 1 dB loss in the output network will result in a reduction by 20 % in efficiency. Considerable experience had been obtained through detailed characterization of the amplifier circuit under the various levels of integration by selectively replacing on-chip elements with off-chip components, as anticipated during the first design iteration and described in section 3. One of the changes suggested by analyzing the data was to use a single output network in place of the power combiner in the output. A schematic of this design is shown in Figure 7.1-1. The configuration of some circuit elements such as spiral inductors was altered for lower loss. Other circuit elements have also been adjusted to center the performance peak at 406 MHz. The design of the driver stage remained similar to the first iteration, with minor "tweaks" to improve its output power and power-added efficiency.

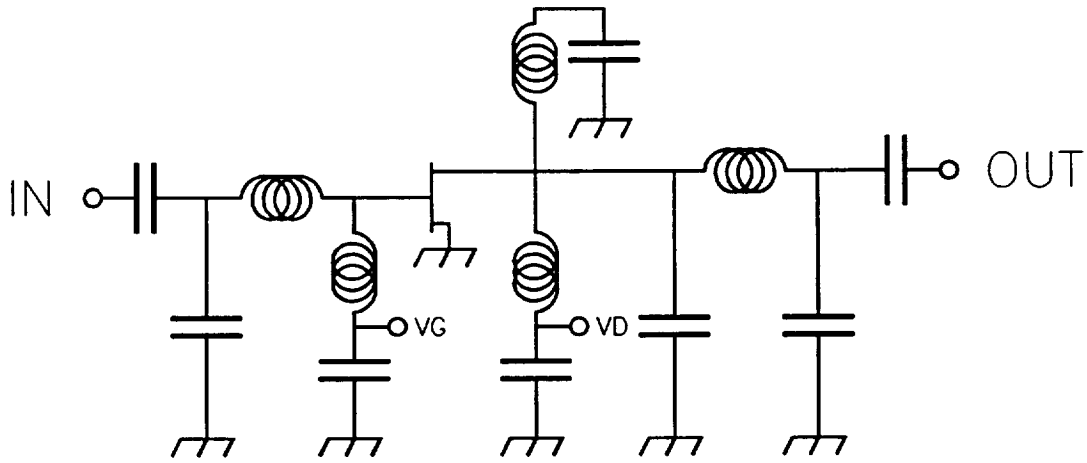


Figure 7.1-1) SCHEMATIC DIAGRAM OF THE OUTPUT STAGE OF A SECOND ITERATION POWER AMPLIFIER DESIGN

7.2) BI-PHASE MODULATOR WITH INTEGRAL BUFFER AMPLIFIER

The design of the passive phase modulator was adjusted to correct the difference between measured and predicted performance. Detailed characterization of the switched attenuator section including measurement of the actual values of the resistors as well as the "on" resistance of the FET switches had accounted for the observed difference. The sizes of the FET switches as well as the values of the resistors were changed to bring the performance back to the original predictions. The values of the delay line elements were also adjusted.

The shift in location of the gain peak towards higher frequency in the buffer amplifier was compensated in the second iteration design.

7.3) MASK TOOL SET LAYOUT

Layout of the monolithic circuits for the second iteration mask tool closely follow the architecture of the MMIC RF module chip set originally shown in Figure 2.1-1. The set consists of two chips: a two stage power amplifier, and a phase modulator with integral buffer amplifier. A pen plot of the power amplifier MMIC is shown in Figure 7.3-1. The size of this chip is 4.1 mm by 2.5 mm. A pen plot of the phase modulator MMIC is shown in Figure 7.3-2. The size of this chip is also 4.1 mm by 2.5 mm. The complete RF module MMIC chip set is shown in Figure 7.3-3.

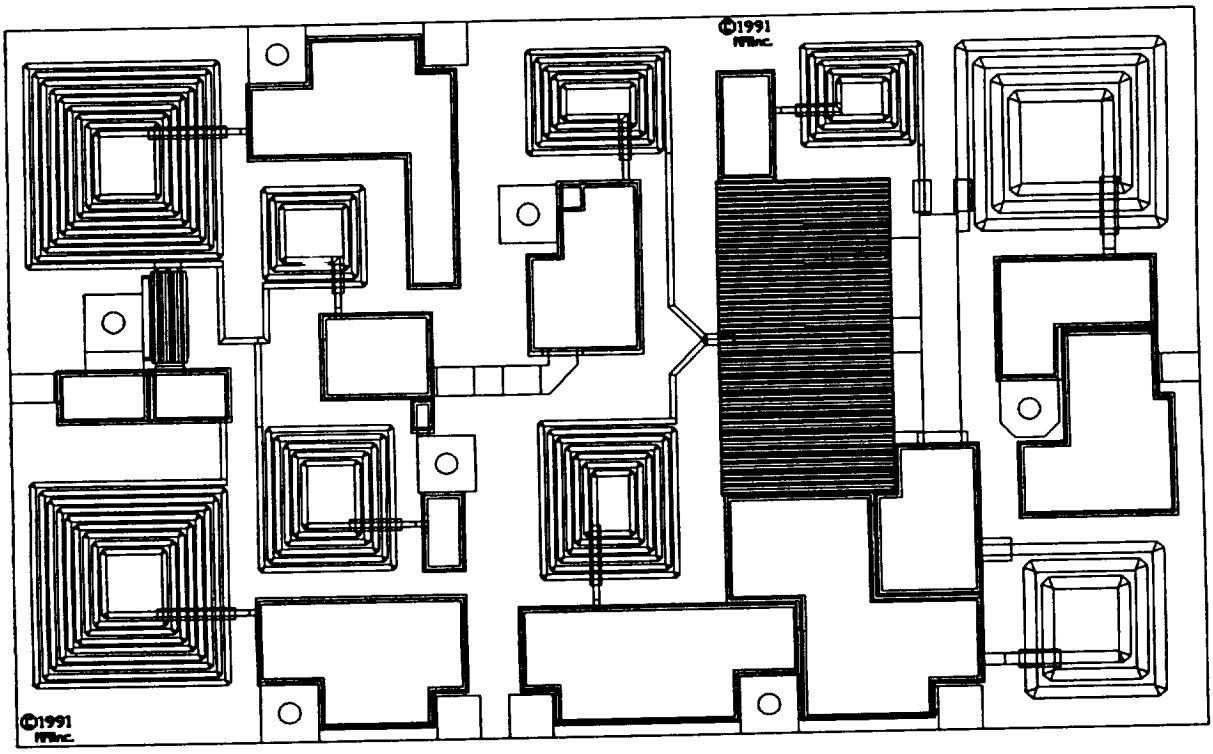


Figure 7.3-1) PEN PLOT OF A SECOND ITERATION MMIC POWER AMPLIFIER

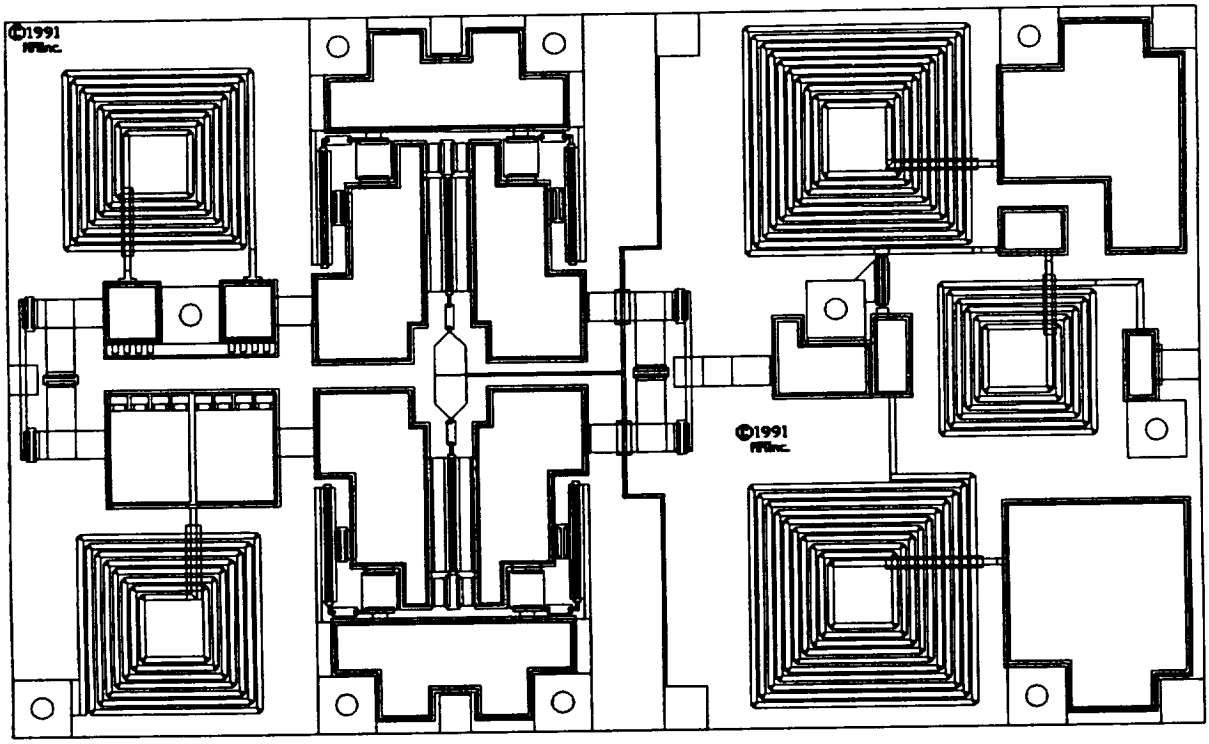


Figure 7.3-2) PEN PLOT OF A SECOND ITERATION MMIC PHASE MODULATOR

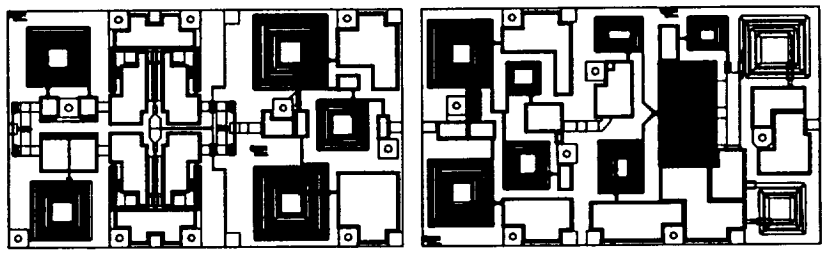


Figure 7.3-3) PEN PLOT OF THE SECOND ITERATION MMIC RF MODULE CHIP SET

8) MEASURED PERFORMANCE OF ITERATED MMIC COMPONENTS

More GaAs MMIC wafers were processed using the second iteration mask tool set. The design of this mask tool set included additional space on the interconnect level, which determines the value of the inductors and the capacitors, for some adjustments. This allowed batch fabrication of the wafers to near completion yet still permitting a quick turnaround (a few days' to a week's time) change to implement a final "tweak". A number of monolithic circuits were next assembled on carriers and characterized in the test fixture. These were then put into connectorized housings and subsequently sealed. The packaged circuits were again tested.

The measured performance of the second iteration GaAs MMIC power components are described in the following sections.

8.1) POWER AMPLIFIER

As originally predicted, best power performance was obtained in circuits with monolithic input matching network and off-chip output network elements. A schematic diagram of the output stage portion of the power amplifier is shown in Figure 8.1-1. The large signal performance of the two stage power amplifier has been measured under a drain voltage supply of 9 volts, which is the lower limit (worst case) of the specifications. The results at 406 MHz are shown in Table 8.1-1.

The drain voltage supply of 9 volts represents is the lower limit (worst case) specified in the program goals. This circuit is intended for a battery operated portable application. To conserve limited battery resources the power amplifier should not be operated substantially above the nominal 9 volt level. In fact the lowest possible voltage consistent with the required output power and the high efficiency goal may actually be desired.

Although the GaAs MMIC power amplifier was designed to operate within a rather narrow frequency band, this circuit has also been characterized over a wider frequency range. The output power, associated gain, and power-added efficiency were essentially constant over a frequency range between 400 MHz to 420 MHz. The input drive available from the present test setup drops rapidly below 400 MHz which precluded meaningful measurements below that frequency.

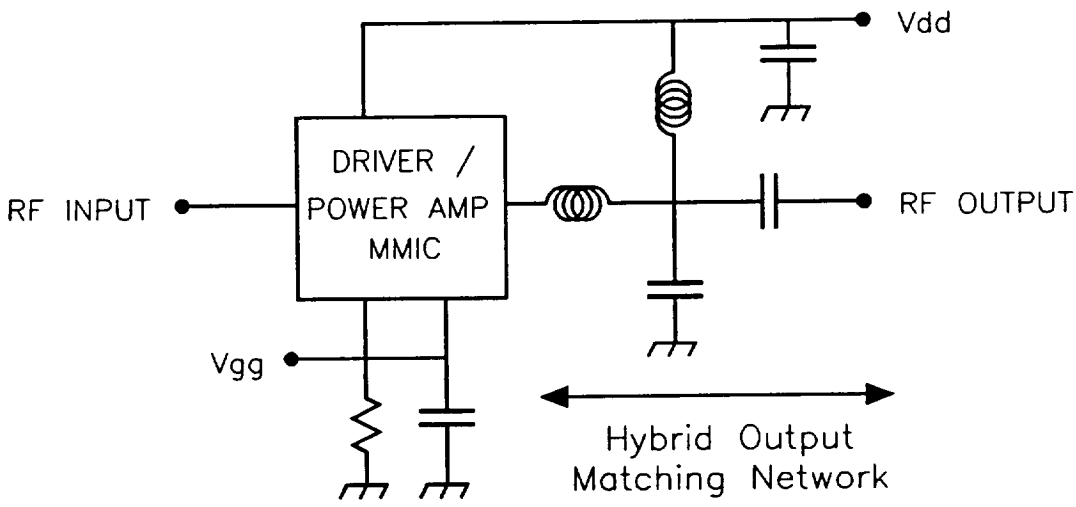


Figure 8.1-1) SCHEMATIC DIAGRAM OF THE OFF-CHIP ELEMENTS FOR THE POWER AMPLIFIER OUTPUT STAGE

Table 8.1-1) MEASURED PERFORMANCE OF A SECOND ITERATION TWO STAGE POWER AMPLIFIER

	CHIP "A"	CHIP "B"
Power Output	5.6 Watts	7.0 Watts
Gain	25.3 dB	28.3 dB
Power-Added Efficiency	59 %	56 %

8.2) BI-PHASE MODULATOR

The bi-phase modulator with integral buffer amplifier was characterized over a range of frequencies around 406 MHz. The insertion phase of a typical modulator is shown in Figure 8.2-1 for the three allowed phase states of 0, +1.1, and -1.1 radians respectively. The insertion gain of the modulator is shown in Figure 8.2-2 for these states and the "null" state. The input match of this circuit is shown in Figure 8.2-3 and the output match is shown in Figure 8.2-4. The input VSWR was less than 1.6:1 for all phase states while the output VSWR was less than 1.2:1. The output match is independent of the selected phase state due to the unilateral nature of the GaAs FET buffer amplifier.

The "large signal" performance of the bi-phase modulator has also been measured. The output level at 1 dB "gain" compression was about +14 dBm. This is more than adequate to drive the power amplifier described in the previous section.

The measured results for the MMIC bi-phase modulator with integral buffer amplifier are summarized in Table 8.2-1.

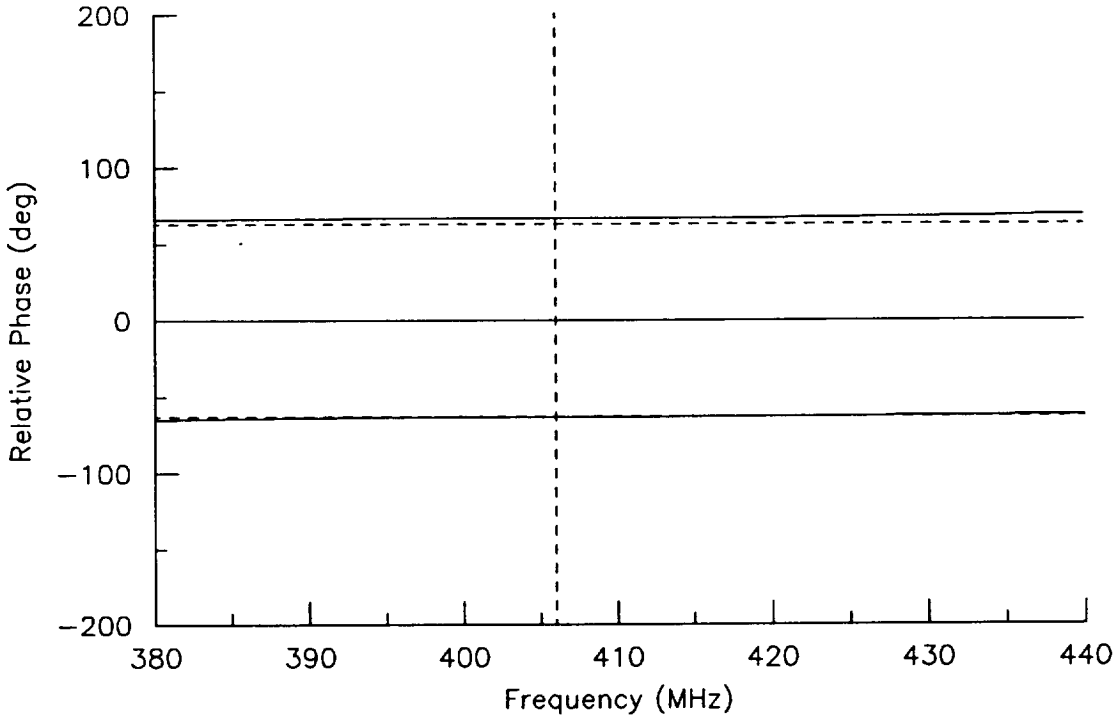


Figure 8.2-1) MEASURED PHASE STATES OF A SECOND ITERATION PHASE MODULATOR

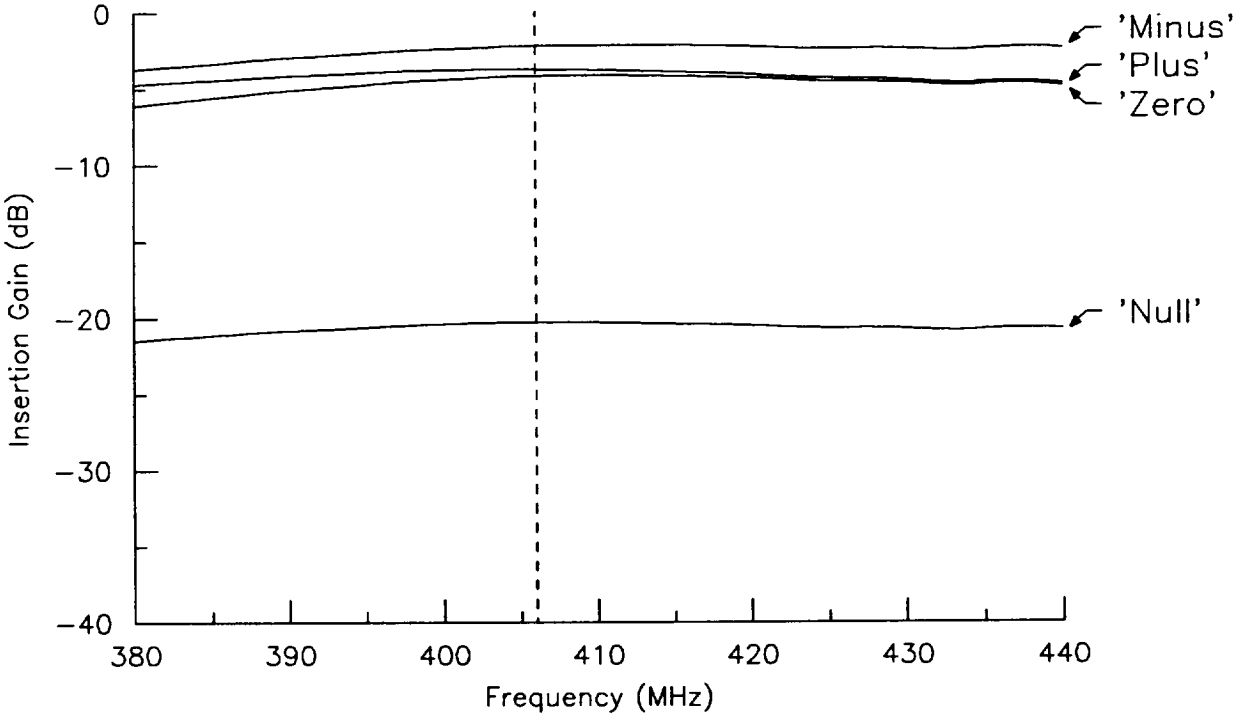


Figure 8.2-2) MEASURED INSERTION GAIN OF A SECOND ITERATION PHASE MODULATOR

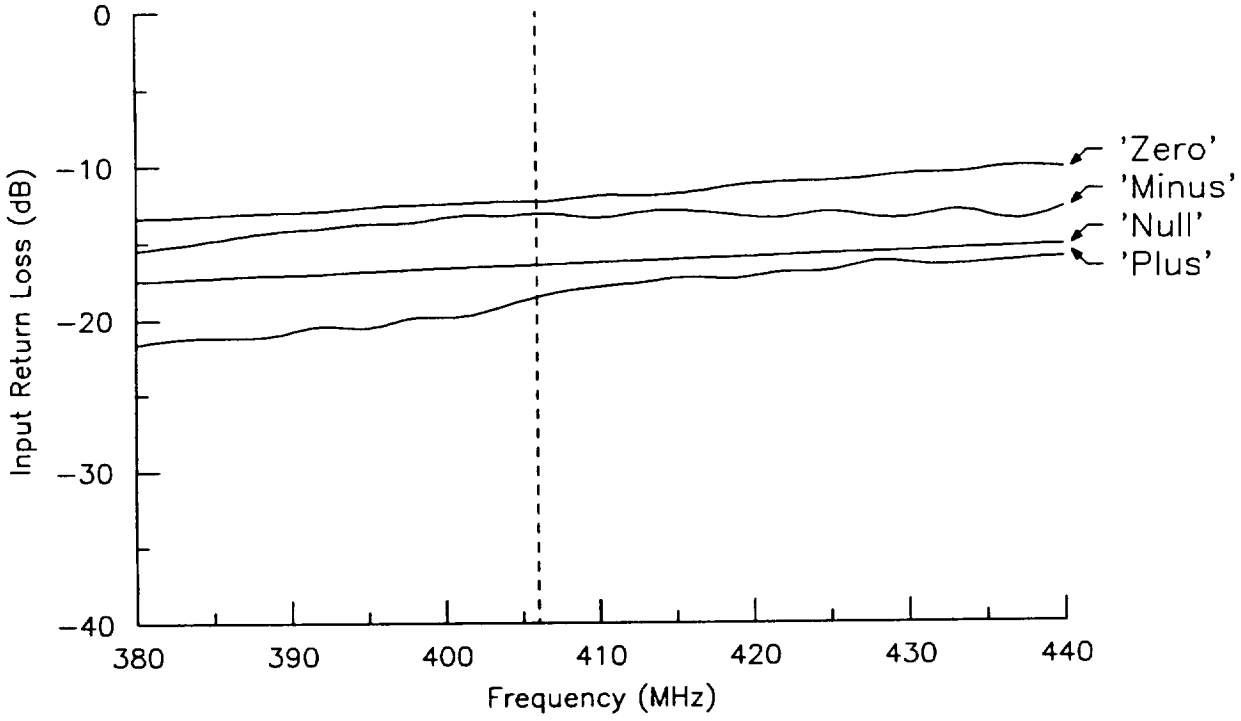


Figure 8.2-3) MEASURED INPUT RETURN LOSS OF A SECOND ITERATION PHASE MODULATOR

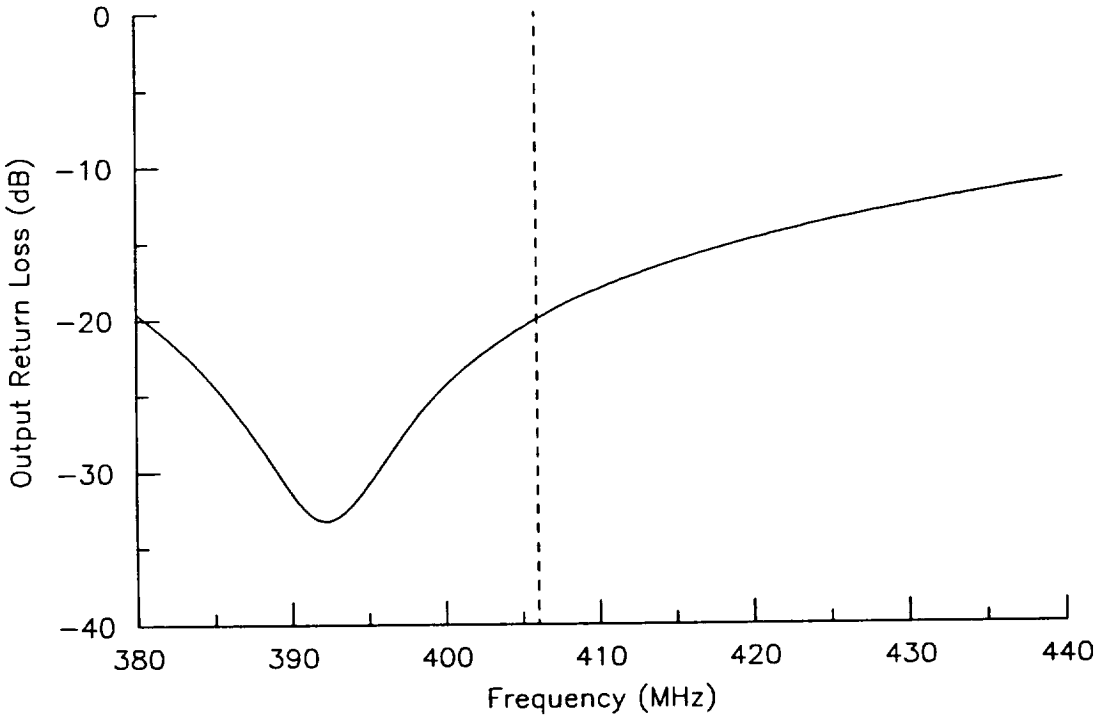


Figure 8.2-4) MEASURED OUTPUT RETURN LOSS OF A SECOND ITERATION PHASE MODULATOR

Table 8.2-1) MEASURED PERFORMANCE OF A SECOND ITERATION PHASE MODULATOR WITH INTEGRAL BUFFER AMPLIFIER

State	Gain	Phase Shift
1 (V_{c1}= 0, V_{c2} =0)	-20.2 dB	-0.15 Rad.
2 (V_{c1}=-5, V_{c2}= 0)	-2.2 dB	-1.10 Rad.
3 (V_{c1}= 0, V_{c2}=-5)	-3.8 dB	+1.16 Rad.
4 (V_{c1}=-5, V_{c2}=-5)	-4.2 dB	Reference

8.3) SUMMARY OF TEST RESULTS

An output power of over 5 watts and nearly 60 % power-added efficiency has been measured with the power amplifier operating at the lower limit of the specified drain voltage supply. The associated gain of the two-stage amplifier was in excess of 25 dB. Output powers as high as 7 watts have been observed. All the program goals have been met and in most cases exceeded. As discussed in section 3, the original program goals are for the power amplifier output stage only. MMInc. included the driver stage to make the input power level agree with established beacon architecture. All the program goals have been met.

Very accurate phase shifts have also been measured in the phase modulators. The average phase error was only 0.03 radians. All the program goals have been met.

9) PRELIMINARY PRODUCTION DESIGN & COST ESTIMATES

Many production-related issues were considered during the design of the second iteration GaAs MMIC RF module chip set. The result is a design which, is in many respects, close to a production version. The total size of the chip set, including area needed for die separation, had been reduced from 30.8 square millimeters for the first iteration design to 23.2 square millimeters for the second iteration design. This represents a 25 % reduction in wafer area consumed by the chip set. Note that the first iteration chip-set size is very close to the 30 square millimeters estimated in the phase II proposal. The GaAs MMIC RF module architecture had also evolved from the three, and possibly four, chip set for the first iteration design to the two chip set for the second iteration design. The result is an optimal partitioning in circuit functions. Separate mask tools, and indeed separate wafer fabrication lines, may be used to produce the chips. Materials and processing parameters optimized for medium power and high gain may be used to fabricate the modulator, whereas fabrication of the power amplifier can be optimized for high power and high efficiency.

Another effort towards production of these chips is packaging. As described in section 5, chips tested in this program were mounted on expansion-matched carriers made of high thermal conductivity Cu/W matrix material. This was no accident since Cu alone would suffice if thermal conductivity had been the only concern. The resulting assembly is compatible with the wide temperature range anticipated for beacon operation. Although two housings were used for convenience of characterizing the modulator and the power amplifier as separate components during this program, a single housing not too different in size from <u>one</u> of these units could conceivably be used to contain <u>both</u> monolithic circuits in the future.

The extensive cost analysis framework from program phase I remains valid. Only the input variables such as the cost of various production steps and the size of the SARSAT beacon MMICs required updating. As before, it is assumed that only the center 2.75 inches of a three inch diameter wafer will produce functional chips since the outside edge will likely be damaged by handling. Four inch GaAs wafers are emerging in digital GaAs IC fabrication; suitability of the material characteristics for high power MMICs, however, has not been well established. Based on the experience with the R&D circuits fabricated in this program as well as other efforts, it is reasonable to assume that DC probe yield in the center section of the wafer is 30 %, and that the DC to RF yield is 75 %. Visual yield is approximately 60 %. An 80 % assembly and test yield results in an overall yield of 11 % for the center section of the 3 inch GaAs wafer (5.94 square inches, or 3832 square millimeters). The size of the modulator / power amplifier chain for the second iteration design is 23 square millimeters. Thus on average 18 good chips per wafer are anticipated at the conclusion of packaging and RF testing. Chip cost in volume production can be estimated once processing cost per wafer has been determined.

The estimated wafer fabrication costs under conditions of high volume production (several million chips per year) and a production line loaded with the SARSAT beacon components and other similar high volume products is summarized in Table 9-1. Non-recurring engineering (NRE) for the chip and equipment depreciation has not been included in these calculations, which will increase the figures presented in the table. The estimated cost per yield chip (set) for such high volumes is shown in Table 9-2. An overall volume scaling factor, which has been widely used in the silicon industry, can be applied to arrive at an approximate cost for large scale production of GaAs MMIC RF modules for the beacon. Based on the industry wide experience in processing large scale silicon integrated circuits, each time the volume doubles the cost is reduced to 70 to 80 percent of its original cost. Assuming the doubling cost factor is 80%, then scale the estimated cost at 2 million units per year down to 10,000 units, the numerical scale factor is 5.5. The estimated unit price for a production level of 10,000 units is then $165.88.

TABLE 9-1) ESTIMATED MMIC PROCESSING COST PER SLICE IN VOLUME PRODUCTION (>1,000,000 UNITS/YEAR)

Ion Implantation	$ 11.17
Photolithography	$ 87.92
Vacuum Metalizations	$ 7.45
Dielectric Depositions	$ 3.02
Gold Plating	$ 1.94
Pattern Etching and Formulations	$ 7.84
Dice Sawing and Chip Separation	$ 18.62
Miscellaneous Operations and Inspections	$ 15.52
Total Processing Cost per Wafer	$153.48

Note 1: Labor costs are included.

Note 2: Costs of GaAs and gold are not included.

10) CONCLUSIONS AND RECOMMENDATIONS

In this phase II of a multi-phase program to develop a low cost high efficiency GaAs monolithic RF module for SARSAT distress beacons, MMInc. has designed, fabricated, and characterized (1) a high efficiency 406 MHz GaAs MMIC power amplifier and (2) a monolithic GaAs bi-phase modulator. The excellent measured performance of these MMIC chips and their compatibility with existing beacon architecture has clearly demonstrated proof of concept for MMInc.'s vision of low cost high performance SARSAT distress beacons. Two complete sets of RF modules have been assembled, characterized, and delivered to NASA. Each RF module component is enclosed in a hermetically sealed and connectorized custom housing for data correlation and further testing.

An output power of over 5 watts and nearly 60 % power-added efficiency has been measured from the power amplifier operating at the lower limit of the specified drain voltage supply. The associated gain of the two-stage amplifier was in excess of 25 dB. Output powers as high as 7 watts have been observed. Very accurate phase shifts have also been measured in the phase modulators. The average phase error was only 0.03 radians. All the program goals have been met and in most cases exceeded. The GaAs MMIC RF module chip set has been design for compatibility with present 406 MHz signal source and digital controller designs. A complete high performance low cost SARSAT beacon can be realized with only additional minor iteration and systems integration.

The next logical step of systems integration towards low cost high performance SARSAT distress beacon development and production is beyond the resources of the current program. However they are relatively straightforward and are thus considered low risk compared to the progress already attained by MMInc. The majority of the chip set development effort has been completed. Some issues include environmental testing and exact interface specifications with the signal source and digital controller (e.g. power levels and control sequence) remain to be addressed. Since the higher risk aspects of the design have already been overcome, a low risk Phase III program consisting of a final MMIC design iteration followed by systems integration is recommended. As originally envisioned by MMInc., this phase III program will lead to completion of a small size and light weight SARSAT distress beacon with much less demanding battery requirements. Completing development of this low cost unit will help realize the full potential of the Search and Rescue Satellite-Aided Tracking system.

REFERENCES

1) "COSPAS/SARSAT 406-MHz Emergency Beacon Digital Controller", W.D. Ivancic, July 1988.

2) "Specifications for COSPAS-SARSAT 406 MHz Distress Beacons", C/S T.001 Issue 2, January 1988.

APPENDIX A) HARDWARE DELIVERABLES

This appendix describes the hardware delivered to NASA for engineering data correlation per the contract data requirements list.

A.1) Monolithic GaAs Power Amplifiers

As described in the body of this report, the monolithic GaAs power amplifier, consisting of the driver and the output stage, is mounted on a single thermally compensated carrier which also contains the hybrid output matching network. This carrier was mounted in a test fixture/housing with SMA connectors for characterization.

The pin out configuration of this component is as shown in Figure A.1-1. Measured performance of the two delivered units is summarized in Table A.1-1. Maximum operating limits and operating procedures for the 406.025 MHz Power Amplifiers is summarized in Table A.1-2.

A.2) Monolithic GaAs Phase Modulators

The Monolithic GaAs Phase Modulator with internal buffer amplifier was mounted on a thermally compensated carrier. This carrier was mounted in a test fixture/housing with SMA connectors for characterization.

The pin out configuration of this component is as shown in Figure A.2-1. Measured performance of the two delivered units is summarized in Table A.2-1. Maximum operating limits and operating procedures for the 406.025 MHz Power Amplifiers is summarized in Table A.2-2.

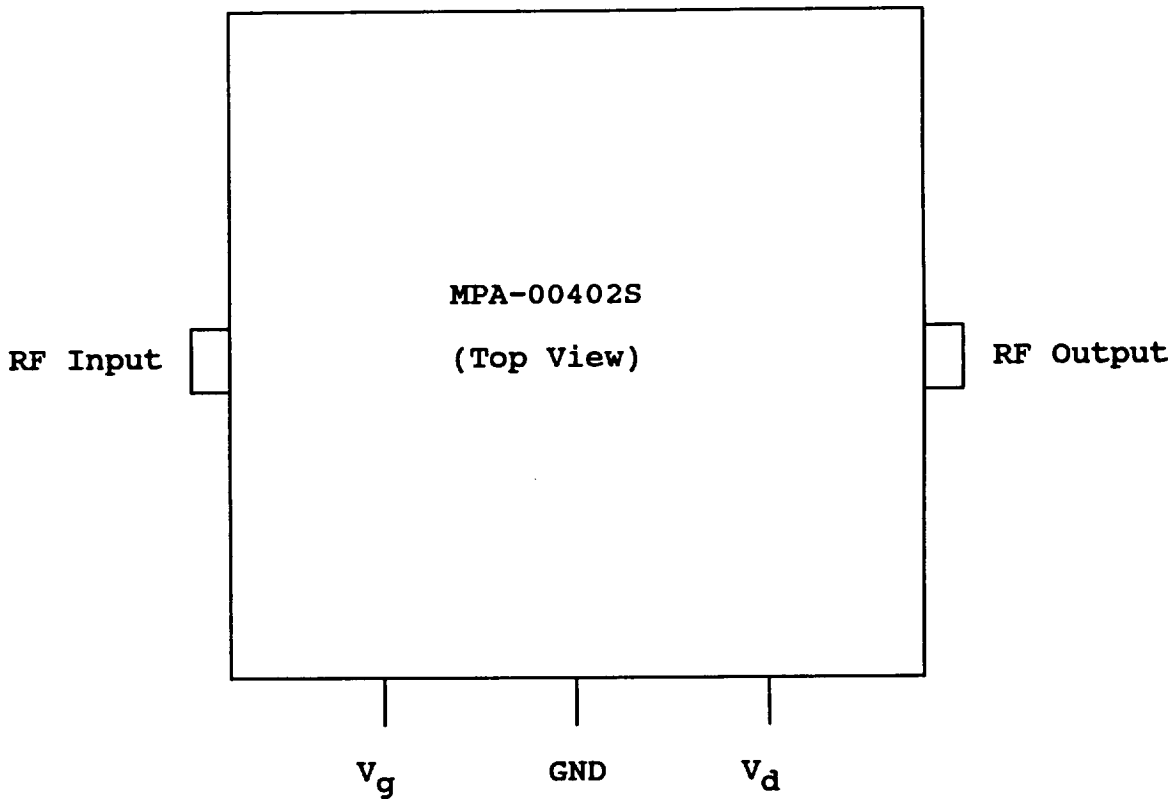


Figure A.1-1) Pin Out Configuration for the 406.025 MHz Power Amplifier.

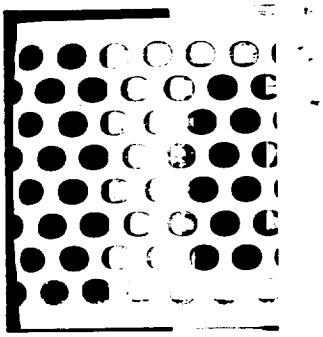
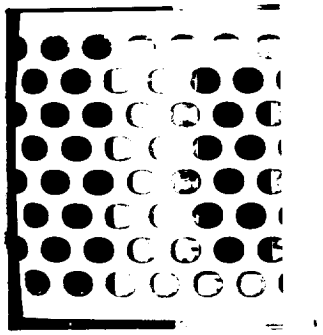


Table A.1-1) Measured Performance of the 406.025 MH
Power Amplifiers.

	MPA-00402S-098	MPA-00402
Gate Voltage, V_g	-1.0 Volts	-1.2 Vc
Drain Voltage, V_d	9.0 Volts	9.0 Vc
Drain Current, I_d	982 mA	1401 mA
Power Output	5.0 Watts	7.0 Wa
Gain	23.1 dB	28.3 dB
Power-Added Efficiency	57 %	56 %



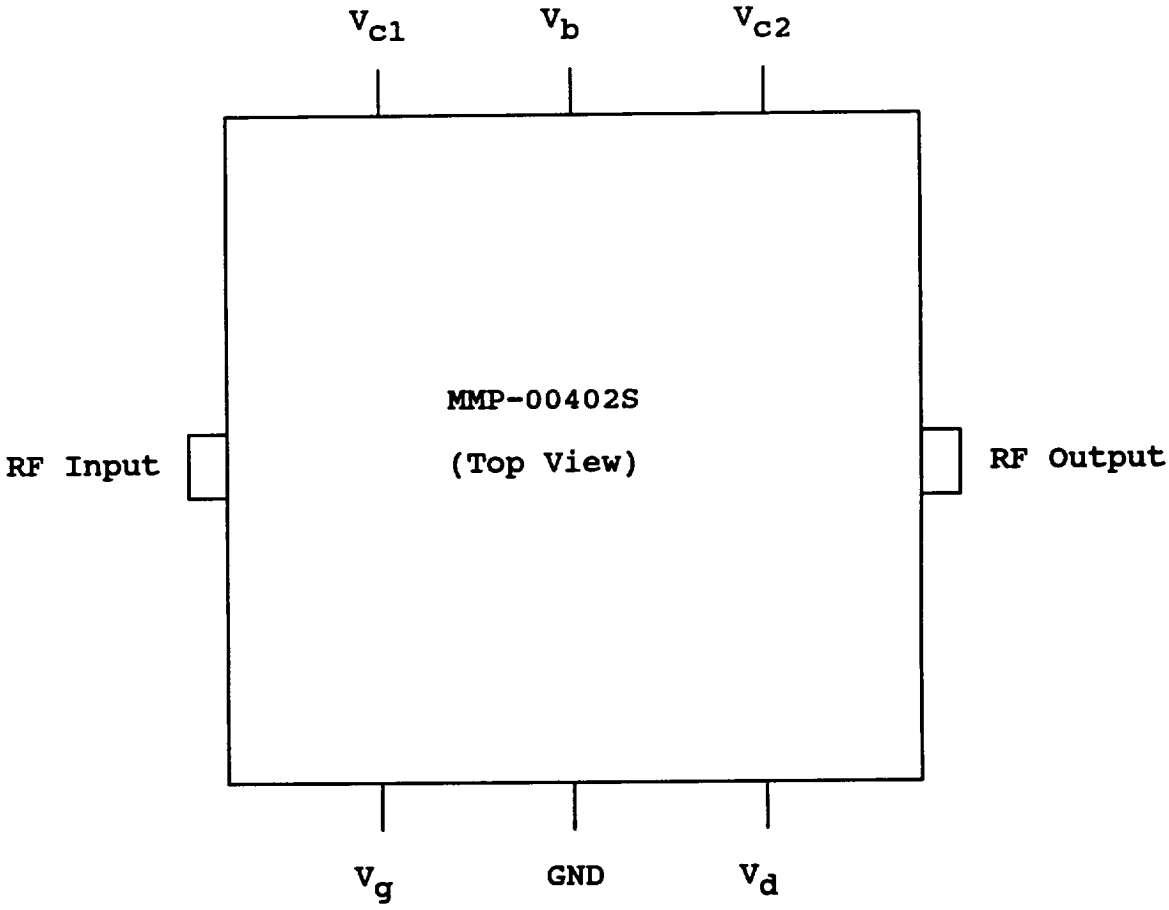


Figure A.2-1) Pin Out Configuration for the 406.025 MHz Phase Modulator with Integral Buffer Amplifier.

Table A.2-1) Measured Performance of the 406.025 MHz Phase Modulator with Integral Buffer Amplifier.

	MMP-00402S-098	MMP-00402S-099
Gate Voltage, V_g	-0.6 Volts	-0.5 Volts
Drain Voltage, V_d	5.0 Volts	5.0 Volts
Drain Current, I_d	40 mA	40 mA
State 1 (V_{c1}=0, V_{c2}=0)		
Gain	-21.8 dB	-21.7 dB
Phase Shift	-0.04 Rad.	-0.04 Rad.
State 2 (V_{c1}=-5, V_{c2}=0)		
Gain	-4.8 dB	-5.4 dB
Phase Shift	-1.08 Rad.	-1.09 Rad.
State 3 (V_{c1}=0, V_{c2}=-5)		
Gain	-5.6 dB	-6.0 dB
Phase Shift	+1.18 Rad.	+1.09 Rad.
State 4 (V_{c1}=-5, V_{c2}=-5)		
Gain	-7.4 dB	-7.3 dB
Phase Shift	Reference	Reference

Table A.2-2) Maximum Operating Limits and Operating Procedure for the 406.025 MHz Phase Modulator with Integral Buffer Amplifier.

Turn-On Sequence:

1) Set V_g to desired value:
   -2.0 Volts Min., 0.0 Volts Max.
2) Ramp V_d to the desired value:
   0.0 Volts Min., 5.0 Volts Max.
3) Apply -5 Volts to V_b.
4) Set Control line voltages to desired setting
   (0.0 or -5.0 volts)
5) Maximum RF Input Power: +17 dBm.

Turn-Off Sequence:

1) Set V_d to Zero Volts.
2) Set V_g to Zero Volts.
3) Set Phase Control Signals to Zero Volts.
4) Set V_b to 0 Volts.

Other Precautions:

1) The V_g gate bias line is connected to the gates of the power GaAs FETs and is thus susceptible to static discharge damage. An external resistor is provided for some static protection.

2) The V_b, V_{c1}, and V_{c2} phase control lines are connected to the gates of GaAs FET switches and are thus susceptible to static discharge damage.