

REVIEW

NASA Space Engineering Research Center for
VLSI Systems Design
University of Idaho
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1 Summary

1.1 Published Papers

One metric for measuring research productivity is the number of papers accepted for publication. It is usually safe to assume that experts in a field can identify quality and therefore, published papers are a good indication of research quality. Twenty one papers were published this year and are listed in Section 3.1. Also, eighteen papers were presented in this year's NASA VLSI symposium by SERC personnel.

1.2 Research Applications to NASA

A second metric deals with the practical applications of research results to projects within NASA. Several VLSI projects that are complete or nearing completion are scheduled for application in the following NASA missions:

- 200 CCSDS decoder chip sets are being delivered for use in the Deep Space Network and the CDOS ground based system.
- Lossless image compressor/decompressor chip set is scheduled for use in SOHO and HST 96.
- Radiation Hard CCSDS encoder has application in XTE and EUVE missions and potentially every CCSDS space application.

1.3 Student Involvement

The student involvement remains high:

- Three Ph.D's graduated in Electrical Engineering in the last twelve months.
- Thirteen Master of Science graduated in Electrical Engineering in the last twelve months.
- Twenty undergraduate students are currently involved in the NASA program.
- Twelve Master's students are currently pursuing advanced degrees and research in Electrical and Computer Engineering.
- Eight Ph.D students are currently pursuing advanced degrees in Electrical Engineering.

The Thesis and Dissertation titles are listed in Section 3.3.

1.4 Outside Support

\$771,000 in non-SERC funds have been raised this year to support the SERC activities. These are itemized herein.

1.5 Research Results

Research summaries and proposed research activities are described in the Section 7. A few of the significant results are summarized.

- New work on the design of Single Event Upset (SEU) immune VLSI logic is reported. This is a novel approach to realizing SEU tolerant storage cells. In addition to the theoretical breakthroughs, SEU immune cells have been implemented into a CCSDS encoder which is targeted for a number of missions. New work will develop a family of SEU immune logic with eventual applications in a standard cell library.
- New state-of-the-art CAD tools have been advanced:
 - The most important is the logic simulator called NOVA. It improves the speed relative to commercial logic simulators by a factor of 3 or 4 and contains excellent electronic transistor models. The simulator was tested in the design of at least one chip (the CCSDS encoder) and is being used to design the image compression chip set. The SERC plans to implement a hardware logic simulation accelerator making this work very attractive for the VLSI industry in general.
 - State machine compiler. Another CAD tool has been developed that can implement arbitrary state machines in CMOS VLSI. The design description is given in a general manner (easy to use) and the resulting VLSI design is produced is an artwork description that can be directly incorporated into an overall layout. This tool has been used in the design of several chips.
 - Schematic driven layout for custom VLSI. The tool needs of the custom VLSI layout environment are being virtually ignored by the CAD tool community. A set of simple, schematic driven layout tools, specified to assist a human layout designer in the custom VLSI environment, is presented in this work.
- New circuit design procedures were advanced:
 - Statistical design for microwave systems. Statistical circuit analysis has been used by the microwave engineer for the past ten years. Recently statistical circuit design has been introduced to the microwave community. However, the application of statistical design and analysis techniques to systems has not yet been discussed in the literature. This work presents, for the first time, a proposed methodology for statistical system design using the commercial simulator OMNISYS (TM). An application to a complete satellite receiver system is demonstrated to show the benefits of statistical system design.

- Statistical interpolation of FET data base measurements. This work is the result of research into valid and compact statistical FET models which extends the Truth Model proposed by Purviance and Meehan. The Truth Model proposes to simply use samples from a FET measurement data base when performing statistical analysis and design. The statistical interpolation technique developed in this work multiplies the number of points available for use in statistical circuit design and analysis by interpolating among the measurements in a statistically valid manner. The statistical interpolation technique using 179 Gallium Arsenide FET measurements supplied by TriQuint Semiconductor Inc have been developed and validated.
- Modeling and sensitivity of GaAs HEMPT transistors. In this research, the Monte Carlo technique is used to study the statistical sensitivity of the AlGaAs High Electron Mobility Transistor (HEMT). The device performance yields and the sensitivity of four different HEMTs to process parameter variations are studied.
- Digital control of magnetically levitated bearings. A digital control system to control the position of moving shafts supported by magnetically levitated bearings has been designed. A prototype controller has been implemented using an Intel 8096 microprocessor.
- Neural networks. An identification method is developed to find the strength of the connections between neurons from their behavior in small biologically-inspired neural networks. That is, given the network external inputs and the temporal firing pattern of the neurons, a solution is calculated for the strengths of the connections between neurons and the initial neuron activation's if a solution exists. The method determines directly if there is a solution to a particular neural network problem. No training of the network is required.
- New design algorithms for VLSI asynchronous sequential circuits. Most VLSI digital controllers designed today model synchronous sequential circuits. The synchronous model is facing difficult electronic problems as the integration density increases. The asynchronous model is an effective means to overcome the problems faced by the synchronous model and to produce faster circuits. New advances in asynchronous circuits by the principal investigator and associates hold promise for future generations of VLSI circuit design. This work focused on generating a new asynchronous sequential structure that will allow easy CAD generation of circuits and provide a structured architecture.
- CMOS output buffer waveshaping. This work reports a novel design technique to reduce CMOS output switching noise. The technique is based on analysis of the RLC equivalent circuit of the output driver stage. SPICE simulations verify the method's effectiveness and a test circuit is being submitted to MOSIS for fabrication.

- New results in communications includes:
 - A new architecture that can implement a SAR processor containing only three unique VLSI chips has been advanced; the total system would contain 100 chips, but only three unique chips. SEASAT data rates would be supported.
 - A new CMOS correlator was designed. It was designed as a single chip that contains 32 channels that operate at 25 MHz. This work is being extended to realize potentially 1,600 correlators that can operate at 60MHz for use in the NASA ESTAR program.
 - New extensions to the error correction capability of Reed Solomon (RS) codes. It is shown that an RS code with an symbol error correction capability of T can actually correct more than T symbols under burst error conditions.
 - Image compression. Lossless encoder and decoder chips are being designed. New research will pursue lossy image compression techniques. The unique approach will emphasize algorithms that yield efficient high performance VLSI architectures.
- New work in computer architectures includes:
 - A high performance video image processor (ACE) has been implemented which is capable of grouping contiguous pixels from a raster scan image into groups and then calculating centroid information for each object in a frame. Processing speeds are adequate for real time processing of video images having a pixel rate of up to 20 million pixels per second.
 - A general purpose hardware accelerator that can support parallel, pipelined or sequential operations. The hardware is well defined and the project is entering the software development phase.
- Advances in reliable design include the following:
 - New procedures for the design of fail-safe CMOS logic circuits. Design techniques to make CMOS logic circuits fail-safe are reported. The set of transistor stuck-on and stuck-open faults, signal lines stuck-at faults, and bridging faults is partitioned into two classes of faults. Fail-safe property is maintained for multiple faults within a class. Limited fault tolerance capability is introduced as a by-product
 - Applications of redundancy for fault tolerance in CMOS logic. The use of hardware redundancy and coding of inputs to achieve fault tolerance in CMOS logic circuits is investigated. The fault set consists of stuck-open and stuck-on faults of individual transistors and stuck-at faults on the signal lines that feed the gates of the transistors. It is shown that to tolerate stuck-open faults, at

least $2n$ devices are needed, where n is the number of devices in a *minimal non-redundant* implementation of the logic function. It is shown that single stuck-on faults can be tolerated if the function is such that there is a minimum Hamming distance of 2 between any input state that gives an output of 1 and any input that gives an output of 0.

- Optimal test set for stuck-at-faults in VLSI. This work presents two new techniques, graphical and inspection, for generating minimal test sets for combinational logic circuits. Both techniques follow the approach of first identifying a minimal multiple fault set covering all single stuck-at faults, and then finding the corresponding test vectors. Boolean simplification or K-maps are not needed, leading to easy automation of these techniques.

1.6 Outreach Program

A new experimental program was initiated in July 1990. Twenty high school teachers were invited to campus to participate in a special course. The purpose of the program was to expose the teachers to fundamentals of digital logic design. This enables the teacher to use new technology in teaching physics and provides insight into a rapidly changing scientific area. Teachers are using their new electronic skills to have their students design electronic measurement devices that are used to verify physics fundamentals.

Next year 16 more teachers will be invited to participate in another one week course. In addition, 10 of the 20 teachers from last year will be invited to return to campus for a four week class that will conclude with designing a VLSI chip that will be submitted to the NSF MOSIS program for fabrication. This is probably the only program where high school teachers have the experience of designing a VLSI chip.

2 VLSI Project Status

Chip Project	Status	Expected Date	Application
LLL ACE	Complete	Operational	Explorer
CCSDS Decoder	In Test	February 1991	DSN and CDOS
JPL Correlator	Complete		Limb Sounder
Rad Hard Encoder	In Fab	March 1991	Explorer XTE EUVE
Data Compression Encoder	In Progress	February 1991 Fab Release	SOHO HST 96 OSL
Data Compression Decoder	In Progress	February 1991 Fab Release	SOHO HST 96 OSL
ESTAR Correlator	Initial Phase		ESTAR

2.1 Project Description

- CCSDS Decoder Chip Set
 - Deep Space Network and CDOS
 - * Delivering 200 systems to GSFC in February 1991. The chip sets are being tested to commercial IC standards.
- Processors Being Developed
 - A radiation hard error correction processor is scheduled for delivery in early 1991. Two independent processors reside on each chip, where each processor performs 2,500 million operations per second with a 320 million bit per second data rate at MIL specification ranges. It is planned for use on Explorer platforms, specifically XTE and EUVE.
 - An Image Compression chip set is being developed for use on the Orbiting Solar Lab (OSL). Also scheduled for use on the Mickleleson Doppler Imager on ESA (European Space Agency) SOHO experiment. Delivery is scheduled for mid 1991. The maximum data rate is 200 million bits per second at MIL SPEC ranges.
 - Narrow Band Auto Correlator for the JPL Microwave LIMB Sounder is complete and ready for fabrication.
 - The SERC s serving an important role in designing the processor for the Electronically Scanned Thinned Array Radiometer (ESTAR) Earth Probe. The complete processor is anticipated to require 10 VLSI chips, each chip having 1,600 correlators and consuming 1 watt while operating at 60 MHz. ESTAR is an important future NASA mission to study the global hydrologic cycle which is not currently being addressed by the instruments on the proposed Earth Observing System (EOS).

3 Publications

3.1 List of Published Papers

- K. Cameron, "ACE: Automatic Centroid Extractor for Real Time Target Tracking," IEEE 1990 Northcon Symposium, Seattle, WA. October 1990.
- S. Whitaker and G. Maki, "Configurable Pipelined VLSI Processor," IEEE 1990 Northcon Symposium, Seattle, WA. October 1990.
- G. Maki, "VLSI: A Unique Technology for Aerospace High Performance for Aerospace High Performance Computing," IEEE 1990 Northcon Symposium, Seattle, WA. October 1990.
- J. Venbrux and N. Liu, "Lossless Image Compression Chip Set," IEEE 1990 Northcon Symposium, Seattle, WA. October 1990.
- S. Whitaker, K. Cameron, P. Owsley and G. Maki, "Custom CMOS Reed Solomon Coder for the Hubble Space Telescope," IEEE MILCOM Conference, September 1990.
- D. Radhakrishnan and Y. Yuan, "A Fast RNS Galois Field Multiplier," Proc. Intl. Symp. on Circuits and Systems, pp. 2909-2912, May 1990.
- D. Radhakrishnan and T. Pyon, "Fault Tolerance in RNS: An Efficient Approach," IEEE ICCD '90, October 1990.
- D. Radhakrishnan and C. Lai, "Efficient Test Generation for CMOS Circuits," IEEE 33rd Midwest Symp. on Circuits and Systems, August 1990.
- A. Premkumar and J. Purviance, "A Two-dimensional Correlation Architecture," IEEE 1990 Northcon Symposium, Seattle, WA. October 1990.
- J. Purviance and M. Meehan, "CAD for Statistical Analysis and Design of Microwave Circuits," International Journal of Monolithic and Microwave CAD, Vol. 1, No. 1. October 1990.
- Howard Demuth, Kwok-Yin Leung, Mark Beale and Joseph Hicklin, "Neural Network Identification," International Neural Network Conference, Paris, France, 1990.
- Howard Demuth, Kwok-Yin Leung, Mark Beale and Joseph Hicklin, "Identification of the Connections of Neural Networks," IASTED International Symposium Expert Systems and Neural Networks Theory and Applications, Honolulu, Hawaii, August, 1990.
- M. Fellows and M.A. Langston, "Fast Search Algorithms for Layout Permutation Problems," *International Journal of Computer-Aided VLSI Design*.

- S. Whitaker, K. Cameron, G. Maki and P. Owsley, "VLSI Reed Solomon Processor for the Hubble Space Telescope," 1990 IEEE Workshop on VLSI Signal Processors, November 1990.
- S. Gopalakrishnan and G. Maki, "VLSI Asynchronous Sequential Circuit Design," IEEE ICCD Conference, September, 1990.
- G. Maki and S. Whitaker, "Full Custom VLSI: A Technology for High Performance Computing," NASA Symposium on Health Monitoring for Space Propulsion Systems Nov 1990.
- J. Purviance, "Design Centing for Yield Improvement of an HEMT LNA," Proceedings of EESof Users' Group Meeting, IEEE MTT-S 1989, Paper No. 6
- D. Radhakrishnan and T. Pyon, "A Compact Real Time RNS Error Corrector," International Journal of Electronics, (accepted for publication)
- D. Radhakrishnan and Y. Yuan, "Fast and Highly Compact RNS Multipliers," International Journal of Electronics, (accepted for publication)
- S. Whitaker, G. Maki and M Shamanna, "Reliable VLSI Sequential Controllers," accepted for publication in International Journal of Electronics.
- S. Whitaker, M Shananna and G. Maki, "Sequence Invariant State Machines," accepted for publication in the IEEE Journal of Solid State Circuits.

3.2 NASA VLSI Symposium Papers

- Albertson, Lyle, UI NASA SERC, "CMOS Output Buffer Wave Shapper"
- Biddappa, Anita, UI NASA SERC, "Efficient Design of CMOS TSC Checker"
- Bobin, Vijayachandran, UI NASA SERC, "A Fail-Safe CMOS Logic Gate"
- Buehler, David, UI NASA SERC, "Automated Synthesis of Sequence Invariant State Machines"
- Cameron, Kelly, UI NASA SERC, "ACE: Automatic Centroid Extractor for Real Time Target Tracking"
- Canaris, John, UI NASA SERC, "High Speed CMOS Correlator"
- Chen, Jian, UI NASA SERC, "A Burst-Correcting Algorithm for Reed Solomon Codes"
- Demuth, Howard, K Leung, M. Beale and J. Hicklin, UI NASA SERC, "Identification of the Connections in Biologically Inspired Neural Networks"

- Feeley, Joe, UI NASA SERC, "Digital Control of Magnetic Bearings in a Cryogenic Cooler"
- Frenzel, Jim, UI NASA SERC, "Supply Current Diagnosis in VLSI"
- Lynn, Doug, UI NASA SERC, "Frequency Domain FIR and IIR Adaptive Filters"
- Manjunath, Shamanna, UI NASA SERC, "Minimal Test Set for Stuck-at Faults in VLSI"
- Miles, Lowell, UI NASA SERC, "NOVA - A New Multi-Level Logic Simulator"
- Purviance, John, UI NASA SERC, "A VLSI Implementation for Synthetic Aperture Radar Image Processing"
- Volkening, Larry, Moscow High School,"NASA Institute Workshop for Secondary Physics Teachers"
- Whitaker, Sterling, UI NASA SERC, "A High Speed CCSDS Encoder for Space Applications/SEU Hardening of CMOS Memory Circuits"
- Whitaker, Sterling, UI NASA SERC, "Reliable VLSI Sequential Controllers"
- Winters, Kel, Montana State University, "Application Specific Serial Arithmetic Arrays"

3.3 Thesis and Dissertation Publications

- Suresh Gopalakrishnan, "Design of Asynchronous Sequential Machines," PhD dissertation, Dec 1989, major professor G. Maki.
- Ching Yu, "Advances in Pass Transistor Design," MSEE Thesis, Dec 1989, major professor G. Maki.
- M. Shamanna, "Minimal Test Set for Stuck-at Faults in VLSI," MSEE thesis, May 1990, major professor S. Whitaker.
- Yong Yuan, "Residue Arithmetic Multipliers: Galois Field Approaches", MSEE thesis, May 1990, major professor D. Radhakrishnan.
- Taejin Pyon, "Fault Tolerance in Residue Number Systems: An Efficient Approach," MSEE Thesis, May 1990, major professor D. Radhakrishnan.
- D. Pedan, "A Comparison of Calculation Methods for Coupled Transmission Lines with Application to VLSI Circuits," MSEE thesis, May 1990, major professor J. Purviance.

- Gregory Barnes, "A VLSI Polynomial Evaluator and Integrator," MSEE Thesis, May, 1990, major professor G. Maki
- W. Guo, "Design of Elliptic Bandpass Filters Using Switched Capacitors," MSEE thesis, May 1990, major professor S. Whitaker.
- C. Lai, "Testing Stuck-open Faults in CMOS VLSI Circuits," MSEE thesis, August 1990, major professor D. Radhakrishnan.
- A. Premkumar, "Real-time SAR Processor," Ph.D dissertation, December 1990, major professor Dr. J. Purviance.
- John Canaris, "A VLSI Architecture for the Real Time Computation of Discrete Trigonometric Transforms," MS EE thesis, December 1990, major professor S. Whitaker.
- Lyle Albertson, "A Technique for the Reduction of Ringing Noise on CMOS Output Buffers," MSEE Thesis, December 1990, major professor S. Whitaker.
- David Buehler, "Sequence Invariant State Machine Compiler" MSEE Thesis, December 1990, major professor S. Whitaker.
- J. Sarkar, "A Statistical Sensitivity Study of the HEMT FET," MSEE Thesis, December 1990, major professor J. Purviance.
- Chunyu Huang, "Combined Error Correction and Source Codes," MSEE Thesis, December 1990, major professor J. Purviance.
- Krishna Parsad, "Parallel Gate Time Sorter," Ph.D dissertation, December 1990, major professor H. Demuth.

4 NASA SERC Symposium on VLSI Design

Association	First Symposium	Second Symposium
NASA	14	17
Industry	42	20
Universities	26	62
Total	82	99

Table 1: Statistics From Symposia

The second VLSI Symposium was held on November 6 at the University of Idaho. It was attended by 99 individuals from NASA, private industry and academia. Subjects such as reliability in CMOS IC processing, SEU issues, space qualification of microprocessors, GaAs VLSI for aerospace electronics, CAD tool developments, and the UI NASA SERC's summer workshop for teachers were discussed during the two featured sessions in the morning and afternoon. An additional 24 papers were presented during concurrent sessions which covered topics such as reliable circuit design, signal processing, neural networks, and VLSI telemetry, design and processors. The following papers were presented.

- Albertson, Lyle, UI NASA SERC, "CMOS Output Buffer Wave Shaper"
- Benz, Harry, NASA Langley, "Space Qualified Microprocessors"
- Biddappa, Anita, UI NASA SERC, "Efficient Design of CMOS TSC Checker"
- Bobin, Vijayachandran, UI NASA SERC, "A Fail-Safe CMOS Logic Gate"
- Buehler, Martin, Jet Propulsion Lab, "Assessing the SEU Resistance of CMOS Latches Using Alpha-Particle Sensitive Test Circuits"
- Buehler, David, UI NASA SERC, "Automated Synthesis of Sequence Invariant State Machines"
- Cameron, Kelly, UI NASA SERC, "ACE: Automatic Centroid Extractor for Real Time Target Tracking"
- Canaris, John, UI NASA SERC, "High Speed CMOS Correlator"
- Chandra, Kumar, Jet Propulsion Lab, "VLSI Correlator Chip for Space-Borne mm-wave Radiometer Spectrometers"
- Chen, Jian, UI NASA SERC, "A Burst-Correcting Algorithm for Reed Solomon Codes"
- Chesney, J., Goddard Space Flight Center, "High Performance VLSI Telemetry Data Systems"

- Demuth, Howard, UI NASA SERC, "Identification of the Connections in Biologically Inspired Neural Networks"
- Feeley, Joe, UI NASA SERC, "Digital Control of Magnetic Bearings in a Cryogenic Cooler"
- Foote, Roy, Hewlett-Packard, "Costs of Becoming a Commodity"
- Frenzel, Jim, UI NASA SERC, "Supply Current Diagnosis in VLSI"
- Katti, Romney, Jet Propulsion Lab, "Data Storage Technology Comparisons"
- Katti, Romney, Jet Propulsion Lab, "Vertical Bloch Line Memory"
- LaRue, George, Boeing Electronics, "GaAs VLSI Design for Aerospace Electronics"
- Lynn, Doug, UI NASA SERC, "Frequency Domain FIR and IIR Adaptive Filters"
- Manjunath, Shamanna, UI NASA SERC, "Minimal Test Set for Stuck-at Faults in VLSI"
- Meador, Jack, Washington State Univ., "Neural Net Diagnostics for VLSI Test"
- Meador, Jack, Washington State Univ., "Auto Programmable Impulse Neural Circuits"
- Miles, Lowell, UI NASA SERC, "NOVA - A New Multi-Level Logic Simulator"
- Peterson, Steve, Mentor, "New Directions in CAD Tools"
- Peterson, Corey, Intl. Microelectronics Prod., "High Frequency Integrated MOS Filters"
- Purviance, John, UI NASA SERC, "A VLSI Implementation for Synthetic Aperture Radar Image Processing"
- Shreeve, Robert, Hewlett-Packard, "Reliability in CMOS IC Processing"
- Taylor, Brian, Bonneville Microelectronics, "Path Programmable Logic: A Structured Design Method for Digital and/or Mixed Analog Integrated Circuits"
- Volkening, Larry, Moscow High School, "NASA Institute Workshop for Secondary Physics Teachers"
- Whitaker, Sterling, UI NASA SERC, "A High Speed CCSDS Encoder for Space Applications/SEU Hardening of CMOS Memory Circuits"
- Whitaker, Sterling, UI NASA SERC, "Reliable VLSI Sequential Controllers"

- Winters, Kel, Montana State University, "Application Specific Serial Arithmetic Arrays"
- Wu, Angus, Washington State Univ., "High Performance Pipelined Multiplier with Fast Carry-Save Adder"
- Yancy, Marvin, Gould AMI, "Characteristics of a Semicustom Library Development System"

5 Resource Support in Last 12 Months

Source	Type	Amount
State of Idaho	Center Support	100,000
University of Idaho	Center Support	151,000
GSFC NASA	CCSDS Decoder Fabrication	35,000
GSFC NASA	CCSDS Rad Hard Encoder	100,000
GSFC NASA	VLSI Architectures	50,000
LLL	ACE Processor	225,000
Hewlett Packard	Analog VLSI	60,000
AHA	RISC Processor	50,000
Total		\$771,000

6 Outreach

6.1 Undergraduate NASA Scholars

An undergraduate scholarship program is supported by NASA to help support a group of students who major in Electrical or Computer Engineering or Computer Science. Current scholars are:

- Amy Anderson, Sophomore, Computer Science, Troy, ID
- Mike Bly, Freshman, Computer Engineering, Otis Orchards, WA
- Thomas Busch, Senior, Electrical Engineering, Moscow, ID
- Eric Cameron, Sophomore, Electrical Engineering, Blackfoot, ID
- Brian Carlson, Freshman, Electrical Engineering, Troy, ID
- Jason Ficca, Sophomore, Electrical Engineering, Moscow, ID
- Michael Fisch, Sophomore, Electrical Engineering, Boise, ID
- Cade Greenup, Freshman, Computer Engineering, Hamilton, MT
- Brian Haler, Freshman, Electrical Engineering, Coeur d'Alene, ID
- Eric Hewitt, Freshman, Computer Engineering, Pocatello, ID
- Sheryl Hoene, Freshman, Computer Science, Nez Perce, ID
- Vernon Koehler, Freshman, Computer Science, Grangeville, ID
- Andrew Miller, Sophomore, Electrical Engineering, Coeur d'Alene, ID

- Alison Pabst, Freshman, Electrical Engineering, Camas, WA
- Teri Ratts, Sophomore, Computer Engineering, Boise, ID
- Brett Shelton, Sophomore, Electrical Engineering, Boise, ID
- Sarah Trask, Freshman, Electrical Engineering, Nampa, ID
- Shannon Wade, Sophomore, Computer Science, Nampa, ID
- Wendy Wahl, Freshman, Electrical Engineering, Genesee, ID
- Paul Winterrowd, Senior, Electrical Engineering, Troy, MT

6.2 Graduate Students

Following is a list of the current graduate students working on SERC related projects. Non US citizens are supported on non-SERC funds.

Student	Program	Degree
Mahmoud Alahmad	Electrical Engineering	MS
Lyle Albertson	Electrical Engineering	MS
Anitha Biddappa	Electrical Engineering	MS
Vi Jayachandran Bobin	Electrical Engineering	PhD
David Buehler	Electrical Engineering	MS
Lowell Campbell	Electrical Engineering	PhD
John Canaris	Electrical Engineering	PhD
Jian Chen	Electrical Engineering	PhD
Qian Chen	Computer Engineering	MS
Roland Cooke	Electrical Engineering	MS
Terry Fay	Electrical Engineering	MS
Jody Gambles	Electrical Engineering	MS
Guruswamy Ganesh	Electrical Engineering	MS
Seetaram Kamath	Electrical Engineering	MS
Norley Liu	Electrical Engineering	PhD
Navid Madani	Computer Engineering	MS
John Pendleton	Electrical Engineering	MS
Phil Prins	Electrical Engineering	PhD
Manjunath Shamanna	Electrical Engineering	PhD
Don Thelen	Electrical Engineering	PhD

6.3 High School Teacher Program

A new experimental program was initiated in July 1990. Twenty high school teachers were invited to campus to participate in a special course. The purpose of the program was to

expose the teachers to fundamentals of digital logic design. This enables the teacher to use new technology in teaching physics and provides insight into a rapidly changing scientific area. Teachers are using their new electronic skills to have their students design electronic measurement devices that are used to verify physics fundamentals.

The topics covered were

- Digital logic and design with SSI chips
- VLSI electronics
- Digital design with MOS electronics
- VLSI graphics editor
- Digital logic laboratory
- Electronics projects laboratory

The teachers were provided with a set of CMOS SSI digital logic. CMOS was used so teachers could power them with a 9 volt battery.

The teachers were from the following states.

State	Teachers
Idaho	5
Washington	7
Oregon	5
Nevada	1
Utah	1
Michigan	1

Next year we plan to invite 16 more teachers to participate in another one week course. In addition, 10 of the 20 teachers from last year will be invited to return to campus for a four week class that will conclude with designing a VLSI chip that will be submitted to the NSF MOSIS program for fabrication. This is probably the only program where high school teachers have the experience of designing a VLSI chip.

7 Research Report

7.1 CCSDS Encoder for Space Applications

Sterling R. Whitaker, Kathy Liu and John A. Canaris

Abstract – This $1.0\mu\text{m}$ CMOS, CCSDS standard, Reed Solomon encoder incorporates control circuitry which is immune to Single Event Upset in the space environment and performs 2,560 MOPS with a data rate of 320 Mbits/sec.

In the environment of outer space, electronic circuitry is exposed to a flux of ionized particles. If the energy level of a charged particle is high enough and that particle passes through the diffusion of a susceptible node then the contents of a MOS memory cell can be changed [1]. This is a Single Event Upset (SEU) of the integrated circuit containing the memory cell. Single Event Upset of circuitry in space is a basic limitation for space based computational systems. This work reports circuit design techniques for SEU immunity which are independent of processing and which are without serious performance degradation. Fundamental design concepts for SEU immune circuitry are reported.

A Rad Hard, SEU tolerant implementation of a CCSDS standard (255,223) Reed Solomon encoder has been designed for Goddard Space Flight Center for use on the Space Station and Explorer platforms [2]. The 5.9mm by 3.6mm full custom $1.0\mu\text{m}$ CMOS IC containing 48,000 transistors is being fabricated at Hewlett Packard's Circuit Technology Group.

The CCSDS code is defined over the finite field $GF(2^8)$. The field defining primitive polynomial is $p(x) = x^8 + x^7 + x^2 + x^1 + x^0$. The generator polynomial is given by $g(x) = \prod_{i=1}^{143} (x - \beta^i)$ where $\beta = \alpha^{11}$. The encoder represents data in the dual basis such that $[z_0, z_1, \dots, z_7] = [u_7, u_6, \dots, u_0] T$ where $[z_0, z_1, \dots, z_7]$ is the symbol represented by the dual basis, $[u_7, u_6, \dots, u_0]$ is the symbol represented by the normal basis and T is a transform matrix. Any of the code defining polynomials can be modified with a single mask layer change.

Data is input in a byte serial fashion at a constant rate, and is output in a byte serial fashion with a fixed one clock cycle latency. After the information bytes have been output, the 32 bytes of RS parity are appended to the data stream. The data rate for the chip is 40 Mbytes/sec. The operation rate is 2,560 MOPS. The encoder has a pin selectable interleave depth of from $I = 1$ to $I = 8$.

Fabricated in a CMOS process with a reported total dose radiation tolerance exceeding 1 Mrad, the chip is designed to provide protection against Single Event Upset in two ways. First, control memory cells are designed to be electronically tolerant of SEU's. Second, the control structure and data path are configured to completely reset after each message ensuring that an SEU of the data registers will effect at most one encoded message.

Proposed Work

The new efforts include:

1. Perform radiation testing of the above encoder after fabrication.
2. Investigate employing SEU immune control logic in a CCSDS decoder that could be used in a communication uplink. The decoder is much more complex than the encoder and therefore must be approached with much greater care.

7.2 SEU Hardening of CMOS Memory Circuits

S. Whitaker, J. Canaris and K. Liu

Abstract - This work reports a design technique to harden CMOS memory circuits against Single Event Upset (SEU) in the space environment. A RAM cell and Flip Flop design are presented to demonstrate the method. The Flip Flop was used in the control circuitry for a Reed Solomon encoder designed for the Space Station and Explorer missions.

Introduction

Electronic circuitry is exposed to a flux of ionized particles in the outer space environment. If the energy level of a charged particle is high enough and that particle passes through the diffusion of a susceptible node then the contents of a MOS memory cell can be changed [1]. This is known as a Single Event Upset (SEU) of the integrated circuit containing the memory cell. The consequences of the SEU depend on the system function of the memory cell. Circuit design techniques which are independent of processing and which are without serious performance degradation have been reported [16]. This work also reports a circuit design method which is process independent and maintains the performance level. With the new techniques presented here, loading on the clock signal is reduced when compared with other known techniques[16].

RAM Design

There are three fundamental concepts that can be used to design SEU immune circuitry. First, information must be stored in two different places. This provides a redundancy and maintains a source of uncorrupted data after an SEU. Second, feedback from the noncorrupted location of stored data must cause the lost data to recover after a particle strike. Finally, current induced by a particle hit flows from the n-type diffusion to the p-type diffusion. If a single type of transistor is used to create a memory cell then p-transistors storing a 1 cannot be upset and n-transistors storing a 0 cannot be upset.

The RAM cell consists of two storage structures. The top half is constructed from p-channel devices while the bottom half consists solely of n-channel devices. Some transistors

are sized to be weak and the other transistors are sized using the normal design considerations for a RAM cell to allow the cell to be written and read to meet the performance required.

The memory cell was then designed for the desired write time and read time and the cell drawn. Parasitics were extracted and SPICE simulations run to verify functionality and performance. SPICE simulations were performed under worst case speed conditions ($V_{dd} = 4.3V$, $T_j = 140C^\circ$ and 3σ parameters). Both SPICE simulations show a recovery time of only a few *nsec*. The hardness of the cell design is independent of processing and parameters. The logical feedback and ratioing of transistor strengths provides the recovery mechanism.

The circuitry added for SEU immunity doubles the number of transistors required by a RAM cell. The layout requires an increase of about 75% in area over the traditional 6 transistor RAM cell. The method described in [16] also doubled the transistor count, but will result in a more compact layout (only a 40% increase in area). The cell described in this paper does, however, have an advantage in the loading seen by the clock signal and the loading seen by the data drivers during a write cycle is less [16]. This should result in an increase in performance. Cells implemented with these two methods using the same CMOS process need to be analyzed to verify this claim.

Summary

An SEU immune RAM cell has been presented which compares favorably with others in the literature. This RAM cell design was implemented as a D flip flop in the controller for a Reed Solomon encoder to be used in a number of NASA missions. This is a preliminary report. Work needs to be performed to produce a comparison of previously reported SEU immune logic with this cell. Also when the chip fabrication is complete, a test structure will be subjected to cyclotron tests to verify the SEU immunity of this cell and results will be reported.

7.3 SEU Immune Logic Family

J. Canaris and S. Whitaker

New Research

In radiation environments such as outer space, high altitude aviation or some medical instrumentation, electronic circuitry is exposed to a flux of ionized particles. If the energy level of a charged particle is high enough and that particle passes through the diffusion region of a susceptible node then the logic state of that node is changed [1]. This is a Single Event Upset (SEU) of the integrated circuit containing the node. Single Event Upset of circuitry is a basic limitation for space based computational systems and is a cause of expensive field testing of aircraft electronics. In preliminary research, new circuit design

techniques for SEU immunity which are independent of processing and which are without serious performance degradation have been developed for memory cells [5]. The structure of these SEU immune memory cells suggests an extension to a logic family. The proposed research would develop the design techniques for this family of SEU immune or fail-safe cells. Past SEU work has been limited to the design of memory cells and has not addressed combinational or sequential logic [6,7,8,9,10,11,12,13,14,15,16]. Fail-safe design techniques have in the past been only logic level methods [17,18,19,20,21]. By designing from a completely new approach, at the transistor level, fundamental fail-safe design concepts should be advanced.

7.4 NOVA: A New Multi-Level Logic Simulator

J. Gibson, L. Miles, K. Cameron and P. Prins

Introduction

NOVA is a new logic simulator that was developed at the University of Idaho NASA Space Engineering Research Center for VLSI Design. NOVA is able to simulate simultaneously at the transistor or switch level and at behavioral levels of circuit description by the use of functional models. NOVA has been used to simulate integrated circuits designed for the NASA Space Station and the Explorer missions.

Why was NOVA developed?

Digital logic simulators make it possible to produce high quality integrated circuits without investing the effort, expense and time in building a prototype. The architecture of a prototype rarely reflects the architecture that is used in an integrated circuit version of the same design. Furthermore, logic simulators address issues that a prototype cannot effectively model, such as simulating faulty circuits, checking internal device states, modeling worst-case process parameters, and more. NOVA extends the state of the art in both simulation accuracy and performance, and in meeting the requirements of future, more complex integrated circuit designs.

Accuracy and Performance

Some digital logic simulators available today address several of the above issues less than satisfactorily. Simulation accuracy and performance varies widely, depending upon the level of circuit modeling detail. NOVA provides greater accuracy by providing more states and strengths with which to model complex CMOS circuits. Twenty-one states are supported, incorporating the levels 0, 1 and X (unknown level) and the strengths of active, resistive and floating (non-driving). Using these levels and strengths, along with unidirectional and bidirectional transistor models, a much larger range of circuits can be accurately represented in NOVA simulations. NOVA performance is very good, due to the efficient use

of workstation resources. NOVA requires an average of 35 bytes of memory per primitive (a transistor or logic gate). The range of memory required by commercially available simulators ranges from 400 to more than 1000 bytes. Simulator performance is fairly directly proportional to the amount of memory required to represent the circuit model, on a given workstation.

Another benefit of the very efficient memory usage by NOVA is the ability to handle very large circuits. The formatters and compilers that accompany NOVA have been designed to minimize the simulation turn-around-time. Designs of one million transistors will still fit within the high speed memory system of an average workstation, preserving good performance. The formatting and compile times required to prepare a circuit for simulation are very much faster than competitive simulators.

Synchronous and Asynchronous Design

NOVA is also a timing simulator, meaning that rise and fall times can be associated with all circuit elements. In fully synchronous systems, timing analysis can be greatly simplified. But as system clock speeds increase, the need for using asynchronous timing increases, which requires the use of accurate circuit delay times. NOVA has been developed to anticipate the circuit design needs of the next 5 to 10 years, with respect to both synchronous and asynchronous design. As circuit geometries decrease in size, it will be necessary to model interconnect delays in greater detail, which NOVA is capable of doing.

Proposed Research

An X11 graphics-based waveform analyzer is available for NOVA that greatly assists the designer in determining if a circuit works according to specification. Logic analyzer trigger functions are being added to the waveform analyzer to allow in depth analysis of complex events. The emphasis is on providing tools to help the designer to a better job in less time.

Research is in progress to develop behavioral modeling methodologies that are easier to use. The use of industry standard high level description languages, such as Verilog HDL and VHDL, with NOVA are being investigated. Using Verilog HDL or VHDL makes possible the use of extensive circuit libraries.

Using VHDL as the behavioral description language for the NOVA simulator is being studied. NOVA's present behavioral language is 'C' based, which produces relatively fast, compact models. The main difficulty with using a unique behavioral modeling language is that only the present NOVA user community is knowledgeable in the language. The communication of design information is more difficult between design engineers in separate design centers where non-standard languages are involved. Though difficult to learn, VHDL is very flexible and can be adapted to most design methodologies. Using VHDL as the behavioral language for NOVA would permit the mixing of behavioral descriptions at a high level with some circuit representations at the transistor level, where modeling efficiency or accuracy would benefit. It will continue to be important to allow the designer to

replace behavioral blocks with detailed circuit blocks, to prove that the behavioral blocks function correctly. A future extension of the NOVA hardware simulation accelerator could be a VHDL hardware behavioral simulation accelerator. The Verilog simulator, along with the Verilog HDL behavioral modeling language, will be installed in the NASA Space Engineering Research Center soon, as a part of comparative studies of simulators and high level description languages.

Another development is a hardware version of the central simulation algorithm of NOVA. The software version of NOVA has been structured to facilitate the design of an integrated circuit that will accelerate NOVA simulation speeds by possibly 100 to 200 times. The NOVA IC will be combined with a dedicated processor and sufficient memory to contain the data for simulation models of one to two million transistors. The hardware simulator will be connected to engineering workstations via a standard interface, such as the SCSI bus.

7.5 A Sequence Invariant State Machine Compiler

D. Buehler, S. Whitaker and J. Canaris

Abstract - A CAD tool for automatic generation of VLSI state machines based on a sequence invariant architecture is presented. The program, which is process independent, operates on a flow table input and produces a layout archive. Using an incremental approach for layout also allows subcircuits to be generated.

Summary

A VLSI state machine can be implemented as a programmable logic array (PLA) based structure or as random logic. The realization of state machines based on random logic often results in the most compact and highest performance circuits, but the logic, which is a function of the state assignment, flip flop type and flow table, does not lend itself to easy automatic synthesis. Controllers implemented as PLA structures can be generated automatically, but are less area efficient and have reduced system performance.

An architecture that retains the traditional strengths of dedicated state machines, but offers the programmability of a microcontroller, was presented in [29]. This architecture produces controllers whose logic is invariant with respect to the actual sequence desired. State machines designed using this method approach the performance and size of random logic based state machines and have a programmability superior to a PLA based design.

This work presents a CAD tool for generating dedicated VLSI controllers based on the sequence invariant architecture. The layouts are design rule independent and correct by construction. Layout generation is done on the fly, with a process rule file being the minimum input required. The software, which is a pipeline of sub-circuit generators, not only provides the layout of complete state machines, but can also generate stand alone

sub-circuits. The program performs all the logic design tasks while leaving the interesting and creative task, flow table definition, to the engineer.

The structure of the architecture lends itself to two "natural" layout approaches. First, the regularity of poly spacings vertically and metal spacings horizontally suggests a gate-matrix layout approach [22]. In this approach, horizontal poly-silicon and vertical metal pitches are calculated, then contact and diffusion areas are placed to form transistors. This approach is, however, inflexible due to the monolithic layout structure created. A second approach divides the layout into a number of tiles which can be calculated, created and then placed, allowing decomposition of the layout problem into smaller cell layout problems. The tile approach was implemented. The state machines for two data compression chips for NASA [23] and a correlator chip for JPL [24] have been implemented using sequence invariant state machines.

7.6 Schematic Driven Layout for the Custom VLSI Design Environment

J. Canaris

Abstract - The tool needs of the custom VLSI layout environment are being virtually ignored by the CAD tool community. A set of simple, schematic driven layout tools, specified to assist a human layout designer in the custom VLSI environment, is presented in this work.

New Research

Introduction

In the rush to supply the rapidly growing semi-custom/standard cell/gate array VLSI design environment, CAD tool vendors are virtually ignoring the once premier custom design environment. This is particularly true of tools, other than graphics editors, for assisting human layout designers in the complex task of physical mask generation.

This work proposes a small set of simple CAD tools, which when used in conjunction with a human layout designer, will significantly reduce the design cycle of custom VLSI circuits. The tools are based on the premise that the use of human designers is, and always will be, the most creative and cost effective method of generating complex VLSI masks. It must be remembered that even in the standard cell and gate array design environment, human layout designers still generate the base cells used in subsequent chip developments. A second basic premise for these tools is a graphical interface. Layout design is a visually oriented optimization problem, and layout tools should reflect that. Currently available code-driven module generators suffer from their non-visual nature.

A brief description of the tool set is given below.

A Smart Tiler

The layout of custom VLSI circuits frequently requires the generation of very regular, densely packed functional blocks. These blocks require extreme attention to area consumed as well as attention to local and global routing considerations. It is often appropriate to perform all routing inside the base cells of these sections. In this case, no routing channels are needed and all routing is done with *Connection by Abutment*. A schematic driven, smart tiler, coupled with a schematic capture system which allows connections by abutment, would provide a significant time savings in layout design. The tiler would require direct data base access to leaf cell layouts, which are created and optimized by human layout designers. This tool frees the layout designer from mundane tiling and net naming tasks, while allowing maximum creativity in solving routing problems.

Random Logic Layout Synthesis

One of the most time consuming tasks in layout design is the generation of random logic associated with controllers and state machines. Although much effort has been expended on PLA and ROM generators, these types of machines are often not useful in a full custom environment. It is usually more efficient to distribute control in small state machines containing fewer than two dozen random logic gates and associated storage elements. A schematic driven layout synthesis tool would be a great help to a layout designer in this case. It should be noted that this problem can be limited to small layouts. This reduces the complexity of the software solution to reasonable levels.

Interactive Channel Router

A frequent task required of custom layout designers is the routing of short interconnect channels or channels which are well defined and regular. An interactive channel router would prove quite useful in these cases. This problem can be limited in scope, again reducing the complexity of the software problem.

Conclusion

A small, simple set of CAD tools has been proposed. These tools can be designed to solve a set of limited problems, thus minimizing software complexity. When coupled with a human layout designer, however, these simple tools can provide a significant reduction in the time required to generate complex VLSI masks.

7.7 Statistical Design for Microwave Systems

R. Cooke and J. Purviance

Summary

Statistical circuit analysis has been used by the microwave engineer for the past ten years. Recently statistical circuit design has been introduced to the microwave community. Statistical circuit design is essentially the design for high manufacturing yield, rather than high performance. However, the application of these statistical design and analysis techniques to systems has not yet been discussed in the literature. This work presents, for the first time, a proposed methodology for statistical system design using the commercial simulator OMNISYS (TM) [35]. Using two examples, a simple amplifier chain and filter, and a complete satellite receiver system, the application and benefits of statistical system design are demonstrated. The nonlinear characteristics of the system amplifiers and mixers are accounted for in this work. The specification of group delay, signal to noise ratio, and power out are all considered in these statistical designs.

7.8 Statistical Interpolation of FET Data Base Measurements

L. Campbell and J. Purviance

Summary

This work is the result of research into valid and compact statistical FET models. The work develops a statistical interpolation technique which extends the Truth Model proposed by Purviance and Meehan. The Truth Model proposes to simply use samples from a FET measurement data base when performing statistical analysis and design. This is accurate when the number of measurements is large, say greater than 1000.

The statistical interpolation technique developed in this work multiplies the number of points available for use in statistical circuit design and analysis by interpolating among the measurements in a statistically valid manner. Statistical interpolation should be used when the number of data points is small, say less than 500 points. Statistical interpolation is a simple and powerful simulation tool. It lends itself easily to software implementation, and gives results better than other simulation models now available [36].

We have developed and validated the statistical interpolation technique using 179 Gallium Arsenide FET measurements supplied by TriQuint Semiconductor Inc. We show that the marginal statistics and the correlation matrix are preserved for the simulated samples.

7.9 Modeling and Sensitivity of the GaAs HEMT Transistor

J. Sarker and J. Purviance

Summary

In this research, we use the Monte Carlo technique to study the statistical sensitivity of the AlGaAs/GaAs High Electron Mobility Transistor (HEMT). We study the device perfor-

mance yields and the sensitivity of four different HEMTs to process parameter variations.

We choose one of the best, most complete analytical models available in the literature for this work. We validate this model by reproducing the I-V characteristics of four typical HEMTs.

Using numerical methods, we develop a simulation program to compute the small-signal parameters, such as transconductance, G_m , gate-to-source capacitance, C_{gs} , current gain cut-off frequency, f_T , and the optimum cut-off frequency, $f_T(\text{opt})$. These computed nominal small-signal parameter values have been used as the device specifications in the Monte Carlo analysis.

Based on the model, we develop a Monte Carlo statistical device simulation. In the simulation, we have simultaneously varied three process parameters, gate length, gate width and the carrier mobility about their nominal values and determine the yield factor histograms of each performance and its sensitivity to the process parameter variations. From this statistical sensitivity study, we observe that the current gain cut-off frequency increases as the carrier mobility increases. We also found that the drain current, transconductance and the optimum cut-off frequency increase with mobility, but the gate-to-source capacitance is independent of the carrier mobility.

From the gate length variation, we found that all the performance yields are inversely proportional to the gate length. The gate width variation tells us that the yields of drain current and transconductance increase with gate width; but the reverse happens for C_{gs} , f_T , and $f_T(\text{opt})$. In this work, we also determine the total performance yields of the four HEMTs at different bias conditions [37,38].

7.10 Real Time Synthetic Aperture Radar Imaging: A Model and Design using VLSI Correlators

A. Benjamin Premkumar and John Purviance

Summary

Synthetic Aperture Radar (SAR) is a two dimensional imaging system that processes reflected radar signals into an image of the reflecting object. SAR image processing is typically done using either frequency or time domain techniques. Different architectures in time domain, frequency domain and a combination of both have been studied and are summarized, compared and contrasted. However, most of the above techniques do not process the SAR data in real time to produce images.

In this research a simplified model for the time domain SAR imaging problem is presented. The model is based on the geometry of the SAR system. Using this model an expression for the phase history of the received signal is formulated. From the phase history it is shown that the range and the azimuth coordinates of a point target image can be obtained by processing the phase information during the intra pulse and inter pulse period

data respectively. This research also presents an algorithm for a two dimensional correlation in the time domain in order to exploit the natural parallelism to accommodate the higher computation rates necessary in time domain approaches. The algorithm requires only as many multiplier accumulators as there are non-zero elements in the correlation reference function and uses no explicit memory for its operation. It produces output at every clock cycle with a latency time of one multiply accumulate. The algorithm lends itself nicely to VLSI implementation. This research proposes a SAR architecture using these correlators to generate images in real time. A one dimensional correlator is used to process the received SAR data in the range direction and a two dimensional correlator is used to process the range correlated data in the azimuth direction. The architecture proposed has several advantages over the existing architectures such as no large memory requirements, no explicit range migration correction circuitry, efficient processing and fewer number of VLSI chips [39,40,41].

This research addresses the possibility of reducing the data rates by down sampling the received target azimuth phase history. It is shown that down sampling the phase history improves the spatial resolution between point targets. Down sampling and the time domain correlators help real time imaging of SAR data. The bit width requirement criterion for a given grey scale resolution at each of the processing blocks is also addressed. A simulator capable of imaging point targets is also developed.

7.11 Combined Error Correction and Source Codes

Chunyu Huang, Cathy French and John Purviance

Summary

An approach to combined error correction coding (ECC)/source coding is presented in this research. We create combined codes by starting with error correction block codes. Then, in contrast to conventional error correction decoding using decoding spheres of equal size, our approach to decoding is to assign decoding spheres of varying sizes, with larger decoding spheres assigned to more likely codewords. Thus, the number of errors that can be corrected depends on which codeword was sent. Sphere-packing bounds are introduced to aid in choosing codes. To compare various codes, the decoded probability of error over the binary symmetric channel is calculated as a function of the channel error probability. We show that the combined ECC/source coding has better error correction capabilities than error correction coding alone for certain input probability distributions. Finally, we also compare the combined ECC/source codes to separate source and error correction codes. Again, decoded probability of error is calculated for both cases, and the combined ECC/source coding has better error correction capabilities than the separate source and ECC coding when the channel is noisy.

7.12 Decoding Algorithms which Extend the Reed-Solomon Code

Jian Chen, Pat Owsley and John Purviance

Proposed Research

The Bose, Chaudhuri, and Hocquenghem (BCH) codes form a large class of powerful error-correcting cyclic codes. Among the non-binary BCH codes, the most important subclass is the Reed Solomon (RS) codes. Reed Solomon codes have the ability to correct random and burst errors. It is well known that an (n,k) RS code can correct up to $(n-k)/2$ random errors. When burst errors are involved, the error correcting ability of the RS code can be increased beyond $(n-k)/2$. It has previously been shown that RS codes can reliably correct burst errors of length greater than $(n-k)/2$. In this work, a new decoding algorithm is being developed which extends the error correcting ability, first for burst errors, then for combinations of burst and random errors. A VLSI architecture is being developed to implement this extended error correction algorithm.

7.13 Digital Control of Magnetically Levitated Bearings

Joe Feeley, A. Law, and J. Lind

Continued Work

A digital control system to control the position of moving shafts supported by magnetically levitated bearings has been designed [42]. A prototype controller has been implemented using an Intel 8096 microprocessor. The controller is being tested using an analog simulation of a magnetic bearing and shaft. Test results will be used to refine the control system design and recast the control algorithm in a form suitable for implementation on a special-purpose chip. The objective of the chip design will be to package as many controllers as possible on a single chip. This will greatly reduce the electronic control equipment required in magnetic bearing applications.

7.14 Neural Networks

Howard Demuth, Kwok-Yin Leung, and Mark Beale

Abstract

We developed an identification method to find the strength of the connections between neurons from their behavior in small biologically-inspired neural networks. That is, given the network external inputs and the temporal firing pattern of the neurons, we can calculate a solution for the strengths of the connections between neurons and the initial neuron activation's if a solution exists. The method determines directly if there is a solution to a particular neural network problem. No training of the network is required.

Introduction

Previous attempts by biologists to understand small (thirty neuron) biological neural (bioneural) networks have involved direct measurement of physical properties or partial destruction of networks to observe the effects of such changes. Both approaches are long and tedious procedures. Our research suggests an alternative method of solving the problem of determining the strengths of connections between neurons. An understanding of the structure of bioneural networks would let us build the electronic equivalent of biological vision or recognition systems and make it possible to design neural prosthesis. For instance, if we can understand the human heart's pacemaker structure, we might be able to design and build a pacemaker that would be responsive to level of effort.

Neural Network Models and Method of Identification

We have chosen neuron and network models that capture some of the most important aspects of the behavior of bioneural networks. Each neuron has an activation level that is the integrated sum of previous inputs from other neurons since that neuron's last "firing". If the activation potential A reaches a threshold T , the neuron "fires", sending positive (excitatory) or negative (inhibitory) signals to other neurons, and resetting its own activation level to the resting potential.

If the temporal firing pattern of a network is known, inequalities constraining the values of the strengths of the connections between the neurons can be written. in the following way. At each time step, a particular neuron either fires or does not fire. If it fires, its activation $A > T$. If it did not fire, its $A < T$. The activations at each time step are functions of the connection strengths between the neurons. Thus, we can develop sets of inequalities whose unknowns are connection strengths. These inequalities can be solved with the simplex method to find a specific solution in terms of connection strengths if any solution exists.

Summary of Results

The method described above has been enhanced to allow a variety of additional connection strength constraints to be imposed. For instance, one can specify the values of connections, one can set all connections from neurons to themselves to zero, one can specify that specific neurons are excitatory (their output connections to all other neurons are positive) or inhibitory (their output connections are negative), that some or all neurons are to be excitatory or inhibitory , etc.

We have written an Apple Macintosh program that allows easy problem specification. It can solve small problems of ten neurons and ten time steps in about a minute. We have also written a Cray X-MP program that runs much faster. We have used this program to run tens of thousands of problems to obtain statistical results of interest.

Recently we have developed a method of finding a central "robust" solution for the connection matrix. We include a common slack variable in each nonlinearity, and maximize

it through application of the second phase of the simplex procedure. The solution that is developed is maximally distant from constraint boundaries in the multidimensional connection strength space. Such a solution is much more robust than the vertex (edge)solutions produced by the first phase of the simple method.

Future

We hope to improve our neuron model to make it include even more important biological features. At a time when the model is sufficiently sophisticated, we will apply it to data from small real biological systems to see if we can help biologists unscramble the true structure of these systems. In this way, we hope to prove the validity of our approach and to know that we have a good investigative tool. Possession of such a tool would be the first step toward understanding and designing the electronic equivalent of a real biological neural system.

7.15 VLSI Asynchronous Sequential Circuit Design

Suresh K. Gopalakrishnan and Gary K. Maki

Most Very Large Scale Integrated (VLSI) digital controllers designed today model synchronous sequential circuits. The synchronous model is facing difficult electronic problems as the integration density increases. The asynchronous model is an effective means to overcome the problems faced by the synchronous model and to produce faster circuits. New advances in asynchronous circuits by the principal investigator and associates hold promise for future generations of VLSI circuit design. This work focused on generating a new asynchronous sequential structure that will allow easy CAD generation of circuits and provide a structured architecture. The approach is different than that which appears as standard in the literature.

Asynchronous Sequential Circuits Designed with Pass Transistors

Since pass transistor logic has major advantages in speed and density they are widely used in VLSI design[25]. However, they had not been applied to asynchronous sequential circuits until recently. Whitaker was the first to utilize pass transistor networks in asynchronous sequential circuits [26]. Gopalakrishnan made major improvements to Whitaker's work by advancing a new architecture and design procedure [27]. Gopalakrishnan has introduced a new design technique for the pass transistor implementation of asynchronous sequential circuits. The design procedure introduced here is based on partition algebra and generates circuits that, compared to previous procedures, use far fewer transistors. This design procedure is very simple and produces circuits that have regular structures and are faster when compared to the circuits generated by the existing procedures. The hardware bounds derived for all the examples presented by Whitaker show that the new design procedure generates circuits that use fewer transistors [26]. Table 2 gives the comparison of the transistor counts obtained with the existing and the new design procedures.

Assignment	Existing procedure	New procedure
Enable-Hold		
Unit Distance	16	
Reduced Unit Distance	12	
Enable-Disable		
Tracey	29	20
Liu	42	31
Tan	28	15
Transition Path Synthesis		
Tracey	132	
Reduced Tracey	100	
Liu	48	11
Tan	98	21

Table 2: Comparison of the transistor count of the new and existing procedures.

Proposed Research

Typically there are many state assignments that are valid for a given asynchronous sequential circuit. The question is "Given many valid state assignments, which assignment produces hardware with the fewest number of transistors or operates the fastest?" One way is to realize all statements into hardware and count the number of transistors or measure the delay. It would be better if one could determine these metrics without realizing the hardware. Therefore, the proposed work is to develop new procedures to estimate which state assignment will produce desirable characteristics.

7.16 ILA Asynchronous Sequential Circuits

Norley Liu, Sterling Whitaker and Gary Maki

New Proposed Research

The design of sequential circuits presents a major design task for most digital systems. A system normally includes modules, such as the controller, which in most cases is modeled as a sequential circuit. The system's performance will heavily rely on the performance of these sequential circuits for generating control signals and performing sequential operations.

Sequential circuits are typically classified as synchronous or asynchronous. A synchronous circuit needs a clock to synchronize all operations and to avoid the problems of

critical races and hazards. An asynchronous circuit, on the other hand, does not employ a clock and hence improves the circuit in the categories of speed, clock distribution and power distribution [58]. However, the possible presence of critical races and hazards makes asynchronous circuit far more difficult to design than synchronous circuit. The design complexity prevents asynchronous circuits from being used in the majority of sequential circuits, in spite of its better circuit performance.

When measuring the success of a sequential circuit design, apart from the logic and circuit performance, the efficiency of design itself is also an issue to be considered. As VLSI technology advances, the complexity and density of circuits also increase rapidly. In turn, the time spent on the design and verification are soaring as well. Therefore, a good design procedure must not only be able to implement the function, but also be able to minimize the cost of design and verification and in terms of time and layout area. A good architecture will bring in the efficiencies to all of the design steps, including logic/circuit design, artwork generation and verification.

Pass transistor logic structures have proved to be a significant improvement by producing great regularity and density. It also reduces DC power and delay. Pass transistor logic has been studied in both synchronous and asynchronous sequential circuits extensively in last decade. Moreover, several effective design procedures have been introduced recently [59,60].

Background

The applications of pass transistor logic to sequential circuits have been explored for years. The early applications of pass transistors to sequential circuits were primarily in the design of combinational NMOS part for next state generation of synchronous circuits. The technique was not formalized until a design procedure for NMOS pass transistor circuits was introduced by Whitaker in 1982 and formalized in 1985 [61]. The pass transistor logic was studied and applied to CMOS circuits and was proved to have definite advantage over conventional gate logic for the design of functions such as digital multipliers and binary tree structures [62,63]. Recently, the pass transistor binary tree structure has been applied to build synchronous sequential controller with real time fault detection by Whitaker and Maki [64].

Pass transistor asynchronous sequential logic was first presented by Whitaker in 1988 [60]. Design procedures for various asynchronous sequential circuits have been given in Whitaker's Ph.D dissertation [60]. Gopalakrishnan extended the procedures by using variable passing to generate faster, simpler and more regular asynchronous sequential circuits [59].

So far, the researchers on the pass logic sequential circuits have focused on the following issues:

- Architecture regularity
- Race and hazard conditions

- Safe design
- Circuit speed and layout design
- Design procedure simplification

Pass transistor sequential logic with Binary Tree Structure (BTS) has proved to have the most regular architecture so far. A unique realization for sequential circuits that has identical circuitry for all of the next state equations has been derived [26]. Valid state assignments can be generated by Single Transition Time (STT) assignment procedures [65,66,67]. Selection metrics have been proposed by Gopalakrishnan to measure the transistor count, speed and layout area of BTS sequential logic [59].

It is necessary to identify the worst case timing path in an asynchronous circuit. Inputs can not be provided at a higher rate than that governed by the delay of worst case timing path. To maximize the speed of asynchronous sequential machine, a self timed machine can be designed to allow the input being provided at varied rate, depending on the speed of active path instead of the worst case path. A normal approach is to generate a spacer input between each input transitions and the asynchronous sequential machine must be able to distinguish a spacer input from a regular input.

Proposed Work

This new effort introduces a new architecture which employs iterative logic arrays. New design procedures are proposed that realizes unique logic and circuit features to design both asynchronous and synchronous sequential circuits.

New Sequential Logic Structure: Pass Transistor Iterative Logic Array

Iterative Logic Array (ILA) has been described in the literature for quite some time [28,68]. To date, there have not been any published research attempts to utilize an ILA structure, particularly a Pass Transistor ILA (PTILA), in deriving asynchronous or synchronous sequential machines.

This work proposes to introduce the Pass Transistor Iterative Logic Array as a new structure in designing asynchronous and synchronous sequential circuits. The basic PTILA cell is a module of two pass transistors with one output Q , two inputs I_1 I_2 and two control lines. Only one PTILA cell design, artwork generation and verification need to be performed. It can be then build into a network by cascading the PTILA cell.

PTILA Design Procedure for Asynchronous Sequential Logic

A simple design procedure is proposed for generating asynchronous sequential circuits. The design procedure is based on Tan's assignment [67] and maps the flow table directly to a PTILA. A necessary and sufficient condition will also be derived to generate PTILA such that each of its inputs are tied to only one state variable.

	I_1	I_2	I_3
A	B	C	A
B	B	D	F
C	E	C	F
D	E	D	F
E	E	G	A
F	E	C	F
G	E	G	A

Table 3: An Example of Flow Table

The procedure can be illustrated by implementing an example of asynchronous flow table, as shown in Table 3. The operation of flow table can be defined as:

$$S_i = \sum_{j=1}^m f_{ij} * I_j$$

where S_i is the next state of present state s_i , and f_{ij} is a function of the present states which are under input I_j and have a next state of S_i .

For example, the operational functions corresponding to Table 3 are:

$$\begin{aligned} A &= I_1 * E + I_2 * G + I_3 * A \\ B &= I_1 * B + I_2 * 0 + I_3 * A \\ C &= I_1 * 0 + I_2 * C + I_3 * (A + F) \\ D &= I_1 * B + I_2 * D + I_3 * 0 \\ E &= I_1 * E + I_2 * (C + D + G) + I_3 * F \\ F &= I_1 * B + I_2 * (C + D) + I_3 * F \\ G &= I_1 * B + I_2 * G + I_3 * 0 \end{aligned}$$

To illustrate the above equations, state A is reached (next state) when the circuit is in state E under I_1 , state G under I_2 and state A under I_3 . Research conducted thus far has shown that the above equations can be directly implemented with a pass transistor ILA structure.

Fundamental issues to be discovered and formalized in the proposed research include:

- Critical Race Free state assignment generation
- Single Transition Time operation
- Pass Transistor ILA cell architecture
- Design Equation generation - hopefully by inspection
- Approaches to automatic artwork generation
- Hardware minimization

New PTILA Architecture

PTILA structure significantly improves the regularity of design, comparing to Binary Tree Structure (BTS) sequential circuits [60] and the pass transistor sequential logic proposed by Gopalakrishnan [59]. The work in [60] results in a BTS that wastes half of the layout area, and the work in [59] results in a pass logic network that utilizes only a square root of area unless an extra routing effort is made to condense the network. In contrast, The PTILA structure will utilize 100 percent of area without introducing extra routes.

Another advantage of PTILA structure is the low area expansion rate versus the number of input states and state variables. Layout area of PTILA for each state variable is only a linear function of the number of input state, and not a function of the number of state variables. By comparison, the layout area for each state variable in other pass transistor structures are a quadratic or exponential function of the number of input states or the number of state variables.

PTILA structure has some unique features. The proposed work will study and prove them in detail. Those properties include:

- Essential Hazard Free

An essential hazard exists if and only if a stable state reached after one change in input I_i is different from the stable state reached after three changes in input I_i [68]. For example, in Table 3, an essential hazard starts in state A when changing input I_3 to I_1 , and starts in state B when changing input I_1 to I_2 .

The key to prove that the PTILA is essential hazard free is to show that PTILA asynchronous logic design procedure guarantees that it is impossible for part of PTILA circuit to work with previous input I_i while another part of circuit to work with present input I_j . All state variables are governed by only one input line, and all paths have identical structure. Moreover, even if I_i and I_j are active at the same time (1-1 overlapping), PTILA will be controlled by only one of them while the others are ignored.

- Input Overlapping/Crossing Tolerant

Two input lines can rarely be switched at exactly the same time. Potential conflicts arise in asynchronous sequential circuit when more than one input are present at a time (1-1 overlapping), or when all inputs are zero (0-0 crossing). Most design procedures avoid such uncertainties by setting a constraint to either no 1-1 overlapping or no 0-0 crossing of input states or both. Asynchronous sequential circuits implemented by PTILA are not, however, subjected to such constraints. PTILA structures are stable against both 1-1 overlapping and 0-0 crossing. This feature is due to a property of PTILA that if one of inputs is "1", all other inputs will be disconnected from state variables; if none of inputs are "1", the all-zero path will be turned on to maintain the current states. Such an input tolerant feature makes PTILA more flexible to deal with different type of input sources.

The circuits generated by proposed procedure also immune to input bouncing. Input bouncing happens when dynamic hazard occurs. For many state machine, dropping the

input level before the state variables reach their stable levels might result in potential problems, such as metastability and malfunction. The property of input bounce tolerant of PTILA is based on the fact that each input variable only controls cells which pass partitioning variables under that input. The design procedure insures that partitioning variables are stable before the input is turned on.

- **Safe Design**

A asynchronous circuit is unsafe if it has a lock-up problem. The lock-up happens when circuit enters unspecified stable states (lock-up states) under abnormal conditions and can not re-enter a specified transition path by simply changing inputs. The asynchronous circuit design procedure proposed in this work greatly reduces probability of lock-up. In many cases, a safe circuits will be realized automatically without applying any special safe design procedure. A common situation is that if a flow table contains at least one column in which there are only two specified stable states, PTILA design procedure will automatically guarantee to come up with a safe design.

Self Timed Logic

Many Self Timed circuit solutions insert a spacer input between normal inputs to provide handshaking mechanism between input source and circuit. This scheme reduces the throughput of such circuit. The proposed approach will seek a new strategy which will always generate signals specifying that the circuit has gone from one stable state to another.

The regularity of PTILA can be used to implement the approach. Due to the PTILA structure, an identical delay for each state variable can be realized. A signature circuit using the same PTILA structure can be attached to the asynchronous sequential circuit. The signature circuit generates a signature for corresponding input state. Whenever a signature is generated, the input state has be digested by the circuit, that is the asynchronous sequential circuit has reached another stable state.

Another approach the solve the problem is to use the partitioning theory to identify the stable variable set for each input. The circuit will send a stable signal to input source when the stable variable set is decoded.

Summary

This work is centered around the theory and application of a new circuit structure – Pass Transistor Iterative Logic Array (PTILA). Design procedures for asynchronous and synchronous sequential circuits are proposed to generate PTILA with many unique features, which out-performs the state of art BTS and other sequential logic structures. Moreover, the PTILA explored a new architecture of sequential logic design. Some of its features are listed below:

- The best regularity

- The best utilization of area
- Simple and straight forward design procedures
- Essential Hazard Free implementation
- Overlapping/Crossing Tolerant input interface

The application of PTILA to Self Timed asynchronous logic is also studied in this proposal. An approach of hand shaking scheme without spacer input is obtained.

7.17 CMOS Output Buffer Waveshaping

L. Albertson, S. Whitaker and R. Merrell

Abstract – This work reports a novel design technique to reduce CMOS output switching noise. The technique is based on analysis of the RLC equivalent circuit of the output driver stage. SPICE simulations verify the method's effectiveness and a test circuit is being submitted to MOSIS for fabrication.

Summary

As switching speeds increase for CMOS integrated circuits, output switching noise is becoming a fundamental limitation in testing and design. There are two main types of output switching noise, ground bounce, which is the variation of the chip ground with respect to the external ground, and ringing (undershoot/overshoot) on the output signal lines. Ground bounce is caused by the rapid discharging of the output capacitance and is accentuated by multiple output drivers switching simultaneously. Ringing is caused by the improper damping of the inherent RLC discharge or charging loop. Both of these sources of noise are attributed to having an inherent inductance in the charging or discharging path of the output load capacitance. Noise caused by ground bounce can cause false switching of internal gates leading to incorrect logic states and reduced reliability of the integrated circuit. Ringing on signal lines is also undesirable in that it can falsely trigger an input in circuits driven by the IC resulting in incorrect data transmission.

There has been a significant amount of effort put forth in finding solutions to the problems of output switching noise. Most of these solutions are based upon three main approaches: [43,44,45,46,47,48,49,50,51,52,53], 1) reducing the inherent inductances in the ground and power paths, 2) decoupling the noise generated by the output drivers, and 3) innovative circuit designs which usually reduce di/dt . This paper first reviews these methods for noise reduction, then presents a method for the evaluation of output ringing and finally presents a solution based on waveshaping the gate voltages controlling the output devices.

The analysis presented is based upon the characterization of the RLC discharge loop in the output buffers. This analysis leads to a design which properly damps the RLC discharge

loop for low capacitances while maintaining the ability of the output to drive a wide range of capacitive loads. A one pole RC low pass filter is introduced between the predrivers and the gates of the output inverter to shape the driving voltage. The filter capacitor is the gate capacitance of the output transistors and the resistance is implemented with biased CMOS transmission gates. In addition, ground bounce is decreased by the reduced di/dt when an output switches. SPICE simulations verify the design claims and a test circuit is being submitted to MOSIS for further verification.

7.18 A Low Power CMOS Correlator

J. Canaris and S. Whitaker

Abstract – A full custom, 25 MHz, $1.6\mu\text{m}$ CMOS Correlator chip is reported. The 5.15mm by 4.23mm chip performs either autocorrelation or crosscorrelation, consuming less than 10mW per channel. The correlator, designed for a space borne spectrometer, contains 32 channels and is cascable.

Summary

A high speed, low power CMOS correlator chip is presented in this paper. The correlator, designed for a space borne spectrometer contains 32 time-lag channels, each of which contains a biasing multiplier, a 4 bit accumulator and a 24 bit counter. The sensing instruments provide the chip with two 2 bit input words, which can be either the same signal, for autocorrelation, or different signals, for crosscorrelation. The biasing multiplier does not perform binary multiplication, but implements a special function described in this paper. External control of the correlator is quite simple, requiring only a reset signal and an input to signal the end of an integration period. Simple handshaking is provided through a single output pin, which signals when data is available to be read from the output port. Output data can be read while integration is in progress, in either 8 bit bytes or 16 bit words, under the control of a user provided strobe. The correlator is capable of maintaining a 25 Megasample/second input data rate, under 3 sigma worst case speed processing and worst case temperature and supply voltage conditions. Data can be output from the chip at 10 MHz. The chip consumes less than 10mW/channel of average power. Auxiliary ports are provided for both of the data inputs.

The data path of this chip is extremely regular, the initial layout of the core required only 30 hours to complete. The controllers for the input data path and the data output section are implemented with Sequence Invariant State Machines [29], and were initially layed out with a compiler described in [54]. This chip is amongst the first VLSI designs to utilize Sequence Invariant State Machines [23,24].

The core of the device contains 31,948 transistors in an area 3.49mm by 2.52mm . The core transistors have a n-transistor to p-transistor ratio of 1.77:1, which reflects the

extensive use of n-transistor pass networks. The entire chip layout is highly structured and contains no more than 120 random transistors.

Some of the main features of the correlator chip are listed below.

- Autocorrelation or Crosscorrelation
- 25 Megasamples/second
- 32 channels
- Up to 1.78 second integration time at 25MHz
- Low Power ($\leq 10mW$ per channel)
- Cascadable
- Selectable auxiliary ports on the data inputs
- Integration can continue while data is output
- CMOS and TTL compatible inputs

7.19 Research in Support of ESTAR Earth Probe

John Canaris

The ESTAR Earth Probe Project

The Electronically Scanned Thinned Array Radiometer (ESTAR) has demonstrated promise as a new technique for microwave remote sensing, of soil moisture and salinity, from space. The NASA Instrument Concept Design Office (Code 722) developed a study team to look at possible ESTAR instrument configurations and recommend technology development programs that would enable a Phase A study to begin in the early 1990's. The scope of the study was expanded to include preliminary spacecraft power and mass budgets [74]. The University of Idaho NASA SERC for VLSI Systems Design provided preliminary design information, in regards to special purpose VLSI computers, in support of this study.

Correlator needs of ESTAR

A synthetic aperture radio antenna requires a large number of correlations to be performed in real time. The ESTAR earth probe is estimated to require 123 individual antennas and some 15,000 correlators. Scientists at GSFC have indicated they would like to have a system requiring some 800 antennas and 63,920 correlators. The correlators will have to operate at 60 Megasample/second data rates. Needless to say this is a significant computational problem.

Planned Development

Goddard Space Flight Center has asked the University of Idaho NASA SERC to investigate architectures for a Correlator VLSI to be used in the ESTAR Earth Probe. The SERC has already done preliminary work in this area and intends to continue such research in 1991.

The main focus of this research will be the following.

- Study and evaluate architectures for the ESTAR correlator chip. Provide power and size estimates to GSFC.
- Write a specification of the correlator chip and create a preliminary schedule for the correlator.

This work will be performed in conjunction with the GSFC so as to ensure that the final solution will meet the needs of the NASA engineering and scientific community.

7.20 Image Compression

Jack Venbrux

Two major tasks are planned for the next time period. The first task is to work on solving the problem of finding a lossless data compression technique that is easy to decode and extremely regular to implement in terms of chip complexity. The emphasis of the study will be on decoding, rather than encoding, because decoding is often the bottleneck in performance for a chipset. The second task involves helping to design part of a lossy compression chip for GSFC.

Proposed Research

ALGORITHM SEARCH

The first task, that of finding a compression algorithm that is easy to decode and extremely regular to implement is not readily solved by mathematicians or data compression experts. What is easy to decode on a chip often has very little to do with what a mathematician or a computer programmer considers easy or elegant. The emphasis of this study would be to analyze the ease of DECODING and estimate how REGULAR the encoder and decoder architectures may be. The present Rice Algorithm has some very strong points about it but, like most algorithms, it has some weak points also [71,72,73].

Strong points about the Rice Algorithm:

1. Performance. Adapts readily to changing entropy conditions and covers a wide entropy range.
2. Encoder architecture, with the present option set, is a highly pipelined architecture able to operate a very high speed. It performs encoding without the use of codebooks and allows for the sharing of hardware between most of the options. The decoder can also share extensive hardware between most of the options.

Weak points about serial algorithms such as the Rice Algorithm.

1. Performance. The present option set does a poor compression job at entropy levels less than about 2 bits per pixel. To add an option to cover low entropy will add more hardware complexity. It would be very desirable to have a compression algorithm in which a particular piece of chip hardware would cover all entropy ranges, without having to design something special for low entropy.
2. The decoding process is the bottleneck of performance for the chipset. As the decoder designer stated in a paper being submitted for review to the Data Compression Conference "The major bottleneck in the decoding process is that the position of a new symbol in the data stream cannot be decided until the previous sample is decoded [1]." Our present Rice Decoder is only able to operate at half of the maximum encoding speed.

Finding an algorithm that can be decoded more quickly and be even more regular in structure than the present Rice architecture would help meet future high speed compression and decompression needs. One promising coding and decoding method that will be studied is Arithmetic Coding. It offers much better compression at low entropies than a Huffman type code and performs arithmetic operations instead of extensive bit manipulations.

COSINE TRANSFORM CHIP

The other major task in view at this time could involve helping to design a portion of a lossy compression chip for Goddard Space Flight Center. This would be more in a support role, not as chief designer, and might involve designing a run-length coder for the output side of the Cosine Transform Chip.

7.21 Research in Support of Lossy Image Data Compression

John Canaris

Discrete Trigonometric Transforms

Discrete transforms play a significant role in many areas of image and signal processing. The Discrete Fourier Transform (DFT), Discrete Cosine Transform (DCT), Discrete Sine Transform (DST) and the Discrete Hartley Transform (DHT) are discrete trigonometric transforms (DTT). DTT's are used in both one and two dimensional forms to aid in the analysis of signals and systems as well as in the area of data compression.

The search for efficient algorithms for computing these transforms is an active area of research. The primary focus of this research has been to minimize the number of computations, that is, additions and multiplications. This focus has an historical background based on general purpose, sequential, stored program computing machines. The current state of Very Large Scale Integration (VLSI), however, allows many computational elements,

adders and multipliers, to be integrated on a single die. With VLSI as the implementation medium, algorithms and architectures which minimize computations are often not the most efficient solutions to a problem. In fact, in a VLSI design it is much more important to minimize interconnect, regularize data flow and simplify control structures.

John Canaris' masters thesis proposed a VLSI architecture which can fully utilize the parallelism inherent in the trigonometric transforms without wasting area on complex interconnections or special purpose buffer/data transfer circuits. This architecture, based on *Goertzel's Algorithm*, was shown to be a viable alternative to traditional fast transform algorithms for a VLSI implementation. *Goertzel's Algorithm* takes a linear digital filtering approach to the computation and provides a highly flexible, easily analyzed method for computing the DTT's. The architecture consists of identical second order filters, each of which receives the same input sequence, eliminating the need for input data buffering and allowing for real time calculation. Although the number of calculations required is greater than traditional fast transforms, the interconnect is reduced to one global input bus.

Goertzel's Algorithm is extremely flexible. The DFT, DCT, DST and DHT can all be calculated with the same processor core. If an application needs only certain frequency samples from an N point sequence, then fewer computational units are required. On the other hand, by using N units, a full N point frequency sequence can be obtained. As the algorithm is highly parallel in nature, an N point DTT can be calculated in $N + 1$ time. Additionally, N does not need to be a power of two.

Lossy Image Data Compression

The collection and transmission of images involves large amounts of data, often on the order of 14 Megabits per image. NASA realizes that it is imperative that some sort of compression be done on data generated by space borne sensors, before transmittal to earth. An image data compression system will require several components. The NASA SERC for VLSI Systems Design is currently addressing a portion of this system, with the development of an encoder/decoder chip set, which implements Rice's algorithm, for lossless data compression.

The Discrete Cosine Transform is a component of a lossy compression system. An image is first transformed by the DCT, post processed and sent through the lossless compressor, before transmittal to earth. The computational needs of the DCT are not currently addressed by any commercial vendor or university research group.

Planned Development

Goddard Space Flight Center has asked the University of Idaho NASA SERC to investigate algorithms and architectures for a Discrete Cosine Transformation VLSI. The SERC has already done preliminary work in this area and intends to continue such research in 1991.

The main focus of this research will be the following.

- Study and evaluate algorithms and architectures for a 2 Dimensional 32 point Discrete Cosine Transform VLSI.
- Write the specification and create a preliminary schedule for the DCT chip.

This work will be performed in conjunction with the GSFC so as to ensure that the final solution will meet the needs of the NASA engineering and scientific community.

7.22 ACE: Automatic Centroid Extractor for Real Time Target Tracking

Kelly Cameron, Sterling Whitaker and John Canaris

Abstract – A high performance video image processor has been implemented which is capable of grouping contiguous pixels from a raster scan image into groups and then calculating centroid information for each object in a frame. The algorithm employed to group pixels is very efficient and is guaranteed to work properly for all convex shapes as well as most concave shapes. Processing speeds are adequate for real time processing of video images having a pixel rate of up to 20 million pixels per second. Pixels may be up to 8 bits wide. The processor is designed to interface directly to a transputer serial link communications channel with no additional hardware. The full custom VLSI processor was implemented in a $1.6\mu\text{m}$ CMOS process and measures $7200\mu\text{m}$ on a side.

Summary

ACE (Auto Centroid Extractor) groups contiguous pixels whose intensities are equal to or exceed a given threshold into separate objects and calculates their centroids. Proper assignment of contiguous pixels to their respective objects is guaranteed for all convex shapes and most concave shapes. Data for a $N \times M$ pixel image is processed in raster scan format with a maximum value of 1024 for N and M . ACE can process in excess of 500 objects per frame. It serially outputs the following information for each object:

$$\sum X_i I_i \quad \sum Y_i I_i \quad \sum I_i \quad \# \text{ of Pixels} \quad (1)$$

where X_i and Y_i are the x - and y -coordinates of the i_{th} pixel in an object respectively, and I_i is the intensity of the i_{th} pixel.

Threshold intensity levels are set as instructed by a Transputer via the serial link interface. Pixels whose intensities fall below the specified level are not recognized as object pixels. Masking of pixels is also performed according to an optional external RAM, which is controlled by the ACE chip. The ACE chip updates the masking pattern as instructed by a Transputer.

ACE also provides status information for each frame processed. This information includes a frame identification count, internal memory overflow flags, and an invalid shape detection flag.

Highly efficient pixel grouping algorithms were developed for ACE. The required calculations are performed in a specially designed architecture which minimizes signal line interconnect, and maximizes data throughput and computational efficiency. All control, pattern matching, memory management, data flow, input/output, and computational operations are performed in parallel. These factors, combined with a custom designed layout, result in a very high performance centroid processor.

This processor has been delivered to LLNL and is currently operating in a prototype system.

Proposed Work

This processor is complete. New applications within NASA will be sought for use of this chip. Possible applications include

- Centroid calculation is being used to determine the exact focal length of lens used in systems that measure the distance between spacecraft as they dock. This chip could replace the current slow software.
- Once the focal length is determined, then this chip could be used in real time docking procedures where the centroids are calculated.

7.23 A General Purpose Hardware Accelerator

Gary K. Maki and Sterling R. Whitaker

Abstract

Logic designers can implement a variety of logic control structures with Field Programmable Gate Arrays (FPGA) which can implement a large set of logic circuits. Digital system designers who wish to implement various data path architectures do not have a similar generalized device that can be easily modified to produce arbitrary data path configurations.

High performance computing is a strong function of the data path. Each class of problems requires a unique data path to achieve maximum performance. This paper presents a general architecture that can be modified by the user to realize unique data paths. This work is a first attempt at providing a data path equivalent of a FPGA.

Following are the principle advantages associated with this processor:

- Capable of operating in parallel, pipelined or sequential modes of operation.
- User programmable to configure the data path.
- No instruction fetch.
- General purpose or dedicated.

- Attached or stand alone processor.

This configurable architecture combines the general purpose advantages of the stored program machine with the optimization of a fully customized architecture to achieve maximum performance for a broad class of problems. Every functional unit, data path and control structure can be individually optimized for a given algorithm.

Introduction

Field programmable gate arrays (FPGA) have given the logic designer the ability to implement a large variety of logic control structures with a single logic device. Small Scale Integrated (SSI) circuits are rapidly being replaced with FPGAs. While this provides an attractive means towards implementing control logic, a similar device is not presently available for realizing alternative data paths. Such specialized data paths are required in high performance computing. Specialized computers designed for maximum performance are called hardware accelerators.

Hardware accelerators are custom designed logic which are normally application specific as exemplified by floating point processors and logic simulators. Most hardware accelerators do not have the Von Neumann architecture of a stored program computer, but rather have logic structures specific to a given application. Most accelerators cannot be altered and hence the set of problems that can be efficiently solved by a specific accelerator is small. The data path is the architectural element that determines the data processing speed. In most hardware accelerators, the data path is fixed. This paper presents a general purpose accelerator that allows a variety of data path configurations and hence is applicable to a wide range of applications.

In general a processor is defined to operate in one of three modes:

1. Pipelined
2. Parallel
3. Sequential

The mode of operation is determined entirely by the control states, not the data path. The processor presented here can operate in each of the above modes or in any combination of the above modes by providing a data path that can be altered by the control states. The control states are user programmable and this hardware accelerator could complement a stored program computer or operate as a customized stand alone processor.

A stored program computer functions through an instruction fetch-execute cycle. This machine does not fetch instructions in the normal sense; there is no instruction decode step in the processing. Moreover, an operation can be executed every clock pulse. With a frequency of f , and m register-ALUs in the data path, the number of operations is equal to mf ; if $m = 16$ and $f = 20$ MHz, the operation rate is equal to 320 MOPS.

A fully customized architecture can achieve the maximum performance. Every functional unit in the data path and control structure can be optimized for a given algorithm.

With such an architecture, every module can be designed to be operating simultaneously thereby maximizing performance. In the traditional stored program computer, normally only one module is functioning at an instance of time thereby reducing the overall efficiency. A key element in the new processor design is to provide a mechanism where many functional units can be operational simultaneously.

The proposed processor does not operate like the traditional computer. It is not a stored program computer where instructions are fetched, decoded and executed. There is an initialization procedure where the processor is "programmed" to specify its operation. However, after the initialization phase, the processor can perform a set of simultaneous operations during each clock pulse. This corresponds to compilation of a software program and can be described as "hardware compilation" where the data path is configured.

Proposed Research

Designing a new hardware architecture is only one half of the task to produce a useful system. Software needs to be developed. The new work proposes to develop the following:

1. A software simulator that allows one to simulate the new hardware architecture. The simulator must be capable of executing parallel events since the hardware typically has many parallel operations occurring at the same time. Performance information must come from the simulator also.
2. Hardware compilation that corresponds to initialing the control store is needed. It is proposed that a high level language like C be used by the user specifying the operation of the hardware.

7.24 Arithmetic Array Processors

Kel Winters, Principal Investigator
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Overview: High Speed Systolic Serial Arithmetic Arrays

The proposed work is a continuation of research initiated last year on the design and implementation of high speed systolic serial arithmetic arrays. The goal is to develop a design methodology and a library of high-performance CMOS modules that can be used to quickly implement a wide class of massively parallel machines that operate at clock speeds approaching the ring-oscillator frequency of a given CMOS technology. A number of specific architectures under development to demonstrate this approach are described below. It is intended that this work will lead to the implementation of high performance components for space applications.

Babarc: A Babbage Polynomial Solver

Diane Mathews and Kel Winters

The Difference Engine, a recursive polynomial solver architecture proposed by Charles Babbage in the 1820s, has been adapted to a single-cell systolic architecture. This machine was chosen to provide a structurally simple example of the proposed methodology and circuit implementation. An early version of the Babarc (Babbage Array IC) architecture has been successfully prototyped in 2 micron CMOS using the Berkeley OCT standard-cell synthesis tools. The architecture has since been redesigned to greatly improve performance. A full-custom IC release is planned for January, 1990.

Two-Dimensional Integer Convolver

Diane Mathews and Kel Winters

A 2-dimensional integer convolver array under development is essentially a digital filter for 2-dimensional integer-valued data. This architecture was initially intended for Laplacian Pyramid image compaction, as proposed for the Mars Rover/Sample Return Mission, but could be easily configured for a number of image and signal processing applications. A full-custom CMOS implementation is planned for release in the spring of 1991. It may be preceded by an optional standard-cell prototype.

Systolic Finite-Field Constant Multiplier

Sanjay Mitra and Kel Winters

A row/column systolic adaptation of a finite-field constant multiplier is proposed as an example of a 2-dimensional systolic state machine. It will hopefully provide insights leading to the development of high speed error correction systems. A full-custom CMOS implementation is planned for release by the summer of 1991. It also may be preceded by an optional standard-cell prototype.

Programmable Massively Parallel Architectures

A number of general purpose massively parallel architectures have been investigated. One may be implemented in the fall and winter quarters of 1991. Alternate possibilities include a 2-D systolic neural network emulator or various image and signal processing configurations.

Work will continue in the development of hardware description language based modeling and synthesis techniques for systolic serial arithmetic arrays. This work is centered around the OCT tool suite from UC Berkeley.

Research into differential single-clock CMOS circuits will also continue, particularly aimed at performance bounds, time-area complexity, and differential lockup states.

7.25 Design of Fail-Safe CMOS Logic Circuits

V. Bobin and S. Whitaker

Abstract – Design techniques to make CMOS logic circuits fail-safe are reported. The set of transistor stuck-on and stuck-open faults, signal lines stuck-at faults, and bridging faults is partitioned into two classes of faults. Fail-safe property is maintained for multiple faults within a class. Limited fault tolerance capability is introduced as a by-product.

Summary

A fail-safe logical system is one which assumes a safe output state upon failure [30]. A 1(0)-fail-safe system can give an erroneous 1(0) output upon failure, but never an erroneous 0(1) output. Two fail-safe systems can be used together to tolerate faults in one system. Conventional fail-safe circuits do not lend themselves to integration [31]. This paper introduces a novel design procedure by approaching the problem on the transistor level rather than the gate level.

Due to faults, a CMOS logic gate may assume the wrong output logic value or an indeterminate value, when the output is neither logic 1 nor logic 0. The latter condition is intolerable in a digital system, since it can lead to unpredictable behavior. This situation is alleviated by designing the circuit with latched output. The latch uses redundant devices for fault tolerance capability. The CMOS logic gate with latched output is called the *Safe Gate* [32]. The original circuit from which it is derived is the *Basic Gate*.

Stuck-at faults on the input signal lines cause transistors to be stuck-on or stuck-open depending on the logical state of the faulty signal line and the type of transistor, nMOS or pMOS. Bridging faults within a network cause the circuit configuration to be changed from the designed configuration. In several cases, bridging faults introduce extra conduction paths to the supply rails. The fault set addressed in this paper is partitioned into two classes of faults depending on their effect on the circuit output. The effect of one class of faults is to favor an erroneous 1 at the output of the safe gate whereas the effect of the other class is to favor an erroneous 0. The safe gate described previously can be designed to be 1-fail-safe for the first class of faults and 0-fail-safe for the second class.

This technique is useful in environments where certain faults are more likely than others, such as space. An advantage of the technique is that fail-safe circuits can be interconnected to form a fail-safe system. The issues involved in the design of latched output circuits are discussed. SPICE simulations indicate that limited fault tolerance capability is obtained as a by-product.

It is shown that dynamic CMOS circuits are attractive for implementing fail-safe logic circuits. The circuit is designed so that one class of faults dominates the other. As a result, the circuit can be designed to be fail-safe irrespective of the class which the fault belongs to. Thus in this case, the distinction between the classes of faults is unnecessary.

If only a subset of the fault set consisting of transistor stuck-on faults or equivalent faults are considered, the logic functions of NAND, NOR, XOR, and NOT can be easily

implemented in static CMOS as fail-safe functions by properly sizing the transistors in the pull-down and pull-up network, thereby using the concept of *dominance* [33]. The trade-offs involved in designing complex logic functions to be fail-safe in the presence of stuck-on faults have been conducted.

7.26 Applications of Redundancy for Fault Tolerance in CMOS Logic Circuits

V. Bobin and S. Whitaker

Abstract - The use of hardware redundancy and coding of inputs to achieve fault tolerance in CMOS logic circuits is investigated. The fault set consists of stuck-open and stuck-on faults of individual transistors and stuck-at faults on the signal lines that feed the gates of the transistors. It is shown that to tolerate stuck-open faults, at least $2n$ devices are needed, where n is the number of devices in a *minimal non-redundant* implementation of the logic function. It is shown that single stuck-on faults can be tolerated if the function is such that there is a minimum Hamming distance of 2 between any input state that gives an output of 1 and any input that gives an output of 0. Assuming that individual failures are independent of each other, probability of failures of the redundant and non-redundant designs are compared to study the usefulness of applying hardware redundancy. The implications of the application of redundancy on the testability of the logic circuit are discussed.

Summary

Two of the prominent faults in CMOS technology are stuck-on and stuck-open faults of individual transistors [33]. It is easy to see that the effect of signal line stuck-at faults is to make transistors stuck-open or stuck-on. Bridging faults within a network changes the circuit configuration by introducing additional conduction paths. In several cases, this can be modeled as multiple transistor stuck-on faults. This work addresses the reliability enhancement of logic circuits in the presence of failures that can be modeled as single transistor stuck-open or stuck-on faults. In most cases, the results can be extended to the case of multiple faults affecting a single path from the power supply rails to the output node.

In order to tolerate stuck-open faults, there must be a redundant conduction path which is active for the same input state so that the effect of the stuck-open fault does not affect the circuit operation. Thus if the non-redundant design was minimal, a redundant design to tolerate all single stuck-open faults in the circuit would have twice the number of devices that the minimal design had, since there was absolutely no redundancy in the original design. Moreover, this would be the minimal single stuck-open fault tolerant design for that logic function. It is interesting to note that the area penalty paid for this redundancy can be reduced, if a performance penalty in terms of the switching speed can

be accepted. In this case, each transistor in the original design would be split into two parallel devices.

The coding of input states so that the minimum Hamming distance d between S_1 , the set of all inputs that cause an output of 1, and S_0 , the set of all inputs that cause an output of 0, is 2, has been attempted in the past to tolerate some stuck-at faults in combinational logic circuits [34]. This same principle can be used to achieve stuck-on fault tolerance capability. Since there is no 0 of the function adjacent to a 1, the logic circuit can be designed such that no single stuck-on fault can cause a conflict at the output. This means that the single stuck-on fault tolerant logic design would implement an incompletely specified function since there is a non-empty S_{dc} , the set of inputs whose output are not specified. It is well known that any completely specified switching function can be modified to satisfy the above criterion by the addition of at the most one input variable. This would be an XOR function of the other input variables. However, in general, this would yield a hardware implementation that is unattractive in terms of the number of devices. The hardware implementation of the stuck-on fault tolerant function can be improved by carefully "designing" the added Boolean variable, since the requirement is only that $d = 2$. In this case extra hardware would have to be added to generate the additional variable.

One of the major disadvantages of using hardware redundancy for fault tolerance is that, in general, it adversely affects testability. Thus hardware redundancy should be judiciously used. The benchmark for any fault tolerant scheme should be such that the probability of failure of the fault tolerant design should be acceptably smaller than the probability of failure of the original non-redundant design. Assuming that each device has the same probability of failure and the failure of one device is independent of the failure of another, the probabilities of failure of the two design methodologies can be calculated and compared to see the trade-off.

An issue that has to be investigated is the effect of the physical layout of the circuit, especially where hardware redundancy is used to achieve reliability. For example, when one transistor is "split" into two in parallel, is it advisable to lay them out as two separate entities with separate contacts, or is it better to connect them in parallel?

7.27 Optimal Test Set for Stuck-at Faults in VLSI

M. Shamanna and S. Whitaker

Abstract -This work presents two new techniques, graphical and inspection, for generating minimal test sets for combinational logic circuits. Both techniques follow the approach of first identifying a minimal multiple fault set covering all single stuck-at faults, and then finding the corresponding test vectors. Boolean simplification or K-maps are not needed, leading to easy automation of these techniques.

Summary

System and circuit design, over the years has advanced much and achieved a great deal of sophistication and reliability. Because of higher complexities and the lack of external test points, VLSI chips are becoming increasingly difficult to test. To ensure zero-defect conditions necessary in Space engineering, and other specialized fields, all system components must be comprehensively tested for defects and faults.

One of the methods available, but rarely ever used is Exhaustive testing. But these tests are very lengthy and are impractical. Moreover for most circuits, it is possible to diagnose the faults by a shorter test sequence. Hence most of the test methods available use either Boolean simplification [55,56] or K-maps to achieve minimal test sets. Often the information, provided to test engineers, consists solely of the circuit's logic schematics. Boolean equations, K-maps and state tables may be unavailable and are often tedious to derive. Very few of the test methods take this factor into account. One of the methods which uses the logic schematic as the starting data for generation of test vectors is the *Fault Folding Graph* method [57]. But this method does not generate a minimal test set. Minimal test set has to be obtained by the application of Petrick's method [28] to the test vectors obtained by the fault folding graphs. In this work, some new theorems and conjectures have been proposed using which the minimal test set is obtained directly from the fault folding graphs eliminating the need for the subsequent application of Petrick's procedure.

The second technique proposed eliminates the need for the fault folding graphs. The faults which can be tested by a single test vector are first identified to form a multiple fault. A minimal length multiple fault set is then constructed such that all the essential single stuck-at faults are covered. The test vectors derived for these minimal multiple fault set also happens to be the minimal test set. The present methods follow the concept of identifying test vectors testing more than one fault whereas the proposed method identifies all the faults which can be tested by a single test vector. By doing so, one dispenses with Boolean simplification or the need for Karnaugh maps and also the only data ever needed is the logic schematic diagram. The identification of the minimal multiple fault sets is considerably simpler and follows an algorithmic procedure. This procedure can be easily automated for programmatic generation of minimal stuck-at fault tests.

The proposed techniques has been proven to work for all kinds of irredundant combinational circuits - Non reconvergent and reconvergent (internal and primary) fanout circuits.

7.28 Fully Testable Reconfigurable Sequential Circuits

M. Alahmad and S. Whitaker

Proposed Research

A Sequence Invariant State Machine (SISM) is a programmable state machine architecture which has important properties for reliable controller design [70]. Using redundant logic paths in the forming logic, a state machine can be reconfigured to bypass failed components within the state machine or can be reprogrammed to alter the sequence of operation to bypass failed components external to the controller. Unlike many redundant logic configurations, these configurations can be fully tested.

The work currently in progress is to develop the test and design procedures to allow practical utilization of the SISM. Comparison of the testability and reliability properties of Binary Tree Structures versus fully decoded designs are being evaluated. Chip area, speed, reconfigurability and testability comparisons are being made.

7.29 Fault Tolerance and Testing

James F. Frenzel

Proposed Research

7.29.1 Supply Current Testing

Two methods of analyzing the supply current waveform for indications of circuit faults were compared, resulting in the submission of a paper to the IEEE Custom Integrated Circuits Conference. It was demonstrated that for simulated functional faults in a microprocessor, statistical signal detection yielded superior fault detection performance compared to autoregressive modeling.

An extension of this work is research into the application of current testing to GaAs integrated circuits. A literature search is underway, focusing on the typical failure mechanisms and manufacturing defects for the various GaAs logic families. Once this has been completed, experiments will be conducted using simulation to evaluate the effectiveness of supply current testing.

7.29.2 Defect/Fault Tolerant Cache Design

Work has commenced on the design of an associative cache memory that would provide graceful performance degradation in the presence of defects and/or faults. Areas affected by this research are systems with on-chip cache memories and fault-tolerant systems. Defect tolerance will provide increased yields as well as facilitate the manufacturing of larger caches. Fault tolerance would allow a performance critical system to maintain a higher level of performance in the presence of cache failures.

7.29.3 Real-time Cache Design

An extension of the aforementioned project is an investigation into potential uses of the additional logic required for defect/fault tolerance. One area that is of particular interest is the modification of cache operation for use in real-time applications.

8 High School Teacher Workshop

Larry Volkening

The NASA Institute Workshop for Secondary Physics Teachers at the University of Idaho's NASA Space Engineering Research Center (SERC) was open by application. Preference was given to secondary physics teachers where it appeared the information presented in the workshop would most directly be utilized in the classroom. All levels of teaching experience were considered and no prior knowledge of computer chip technology was necessary to apply.

The NASA Institute Workshop offered courses of instruction on logic systems technology, the chemistry of building and operating microchips, constructing and designing analog to digital projects, designing and manufacturing of microchip circuits, utilization of Boolean logic, recognizing gate functions, and developing processes for trouble shooting problems in these systems. Labs and problem solving sessions were used extensively to develop skills the teachers need to teach students theory, logic, design, and manufacturing methods of microchip driven devices. In addition, teachers were instructed in the use of the CAD - PIGLET program for the development and design of microchip hardware. Each course was organized around the theme of making the instructor feel confident enough to design lessons in the classroom and lab or units of study to become a regular part of the curriculum.

8.1 The Work

Teachers were given enough information so, by the week's end, they could begin to see how an idea could be worked into a microchip circuit and how to build a single function system or sensing device utilizing microchip logic. Several small projects were built by the teachers using logic gate, sensing, and decision functions. One of the first project goals was to design and develop a microchip device that could act as a photogate, keep time, and calculate the velocity or acceleration of a moving object. Once this level of understanding was achieved, the instructors were then asked to explore the possibilities of developing further ideas into single function microchip systems of their particular area of expertise. Example: Design a microchip system that could sense and make decisions based upon the level, color, and intensity of light passing through a plant leaf along with doing some simple calculations regarding the rate of light intensity changes. This theme of designing a system to analyze and solve a problem was carried throughout the workshop. It was done in this manner to develop and foster confidence in each teacher in order to encourage the transfer of skills and knowledge into secondary classroom activities.

8.2 Workshop Specifics

Each teacher was given a text of "Fundamental Logic Design," two sets of instructor's notes from each class, a projects kit, several microchips of various gate functions, and as

many 'take-home' goodies the institute could gather together such as a silicon wafer chip, printed layout, hat, etc Each teacher was also given the opportunity to request extra kit materials to act as 'seeds' to start student projects in the classroom. The workshop started at 8:00 am and continued through 5:00 pm for five days with the afternoon of the last day open to free investigative work. Each evening at 7:00 pm a guest speaker presented topics of concern followed with idea sharing sessions. These lasted until 10:00 pm or later.

8.3 Background

The workshop was an idea resulting from NASA SERC Director Dr. Gary Maki's interests in public education and concern that some modern technologies are not being presented in the typical physics and math classroom. Math and science curriculums are rarely updated to current technology standards and fear of not knowing enough background and/or of not having hands on training has kept many instructors from presenting new and/or modern information. For these reasons, the workshop had to be done in a friendly and non-threatening manner.

When contacted by Dr. Maki to help design and set-up the workshop it was obvious where the work had to begin. A few energetic physics teachers have been designing projects specifically along the lines of solving some of Dr. Maki's concerns. Few, however, have achieved much success. This is due mainly to the lack of experience and lack of workshops offering technology courses at this level. In addition, discoveries in physics, technology advances, and curriculum design rarely coincide which further complicates updating course content. Other obstacles such as text, equipment, curriculum standards, time to learn and time to implement changes, almost make the concept of updating course content to fit the needs of students a nearly impossible task for the teacher. If a workshop was to be given it would have to be done in a non-threatening manner to increase the probability of having teachers feel successful enough to want to take the challenge of designing and implementing new skills and technology into the classroom.

Currently, teachers using breadboards, logic gates, or computer chip technology in the classroom are labeled as 'experts' by other teachers. Yet, in many cases, these teachers are working on their own. With a little encouragement they will most likely develop better and more updated curriculums. Today's students are eager to learn modern technologies and they welcome modern course content. The secondary goal of the workshop was then to develop a feeling of confidence within the teachers to enable them to try new ideas in the classroom. As a result, a theme of keeping the learning enjoyable, yet not lacking in substance, had to be developed.

The conditions under which many physics teachers work are extremely varied yet there are some similarities that could be used in developing the NASA workshop. In most cases, funding for the secondary physics classroom is low and in many cases nonexistent in the area of capital outlay. The workshop chose to use breadboards since breadboarding is cheap, consumable and supplies are easily acquired, without putting a major dent in the school's budget (or in the student's pocket if the student try some independent work).

Student interest in taking physics sometimes remains low due to the 'antique' equipment and methods employed in the classroom. Yet, as soon as an instructor shows a device that appears as something special or computer-like the interest level in the course rises since this is the area in which they have been told over the years the next generation will be working. Robotics, logic, computer technology, math pattern recognition, etc. are all buzz words students love to use. The idea that a physics student could tell mom and dad how the laser reader at the local grocery works or that she could help her brother build a science fair project using a computer chip is astounding both for the student and the family. This gives the physics teacher a high level of credibility and also helps generate more student interest in taking the class. The workshop chose to develop teacher understanding of topics ranging from microchip manufacture and chemistry to decision making gate logic operations. This was done to encourage teacher involvement with students at the level of understanding needed to capture proper usage of the buzz words.

8.4 Workshop Results

Teachers were asked to complete questionnaires (Appendix A) about every aspect of the workshop, with the guide that their comments and criticisms would be used to help develop the next workshop. In no case was a teacher negative about the workshop, course instructors, or overall methods of presentation of the material. Several teachers commented along the lines of saying it was nice for a change to attend a workshop of some real updated value and the hands on skills acquired were excellent. Several requested that the workshop be presented in a more detailed fashion, yet others felt it was just right. Almost all the comments indicated that the teachers will most definitely develop some curriculum changes in their classrooms and that they felt much more confident in discussing microchip technology. Several teachers expressed the desire to return for more information at a more technical level and others expressed the desire to return for more practice in developing breadboarding skills. Some of the changes that seemed to be of concern were mostly directed towards administrative concerns or evening free time. In no case was a teacher negative about any of the conditions in which they did their work. And in no case did a teacher express a negative comment regarding time spent attending the workshop. Overall, the workshop could be described as a major success, especially when several teachers expressed sorrow in having to leave.

8.4.1 One outcome – my own classroom

This year, I have chosen to start the course in a non-traditional manner. Normally, physics is taught starting with Newtonian mechanics. I have always been concerned over the concept of inundating students with equations, terms, units, and math that is often just plain overwhelming, especially to the average non-excelling student. This year I chose to start with the modern physics concepts of field theory, astronomy, and Einsteinian mechanics in a very light, non-threatening discussion mode. During this time I emphasized

the need to know basic mechanics since this is what most of us see in our regular lives. Eventually, I asked about the need to have tools that can help make the small precise observations needed to understand basic and modern mechanics. As a result, the course shifts from one of transferring interesting knowledge to one of “how to build devices that can help us become good observers.” I have then set the stage for students to become scientists who are ready to learn the electronics and logic needed to develop precise timing devices, light sensing devices, decision making logic circuits, etc

With this shift the course can now use basic electronic equations and simple math and algebra skills. The course constantly utilizes electronic energy equations to show that energy is the same whether electrical or mechanical. Energy analysis just needs different equations to show various relationships. The reason for learning electronics is based on the student's desire to build a timing device and computation device in order to look closely at basic mechanical events. In addition, I have suggested that maybe some of the electronic skills used in looking at mechanics could be modified later when it becomes necessary to look at electromagnetic events closely. This I hope will set the stage for developing the desire to look closely at modern physics phenomena.

One Example

At this time we are using Ohm's law and power equations to help design simple breadboard circuits using microchips and transistor gates to sense events and drive a logic circuit that can make decisions. In order to get to this level, we have had to discuss such things as the purposes of Boolean logic, binary numbers, asserted versus non-asserted operation modes and interfacing techniques with the computer. Trouble shooting techniques are a major part of the lab work, yet they are viewed as somewhat of a challenge since each student's problems are unique to the circuit board being built. We just finished a sailcart race where carts were designed to run by the power of a window fan and timed by hand to go a specified distance. The circuit board technology to build a timing device became a very desired tool to have in helping time carts down the course. The question of building a single circuit chip device that could detect time rates and calculate acceleration is a result of student interests, not instructor's desires. The class is now ready to build devices to help detect Newtonian events and to develop logic systems that will analyze the events.

Appendix A

Comments on the logic lectures:

- Burton, Fred: Well prepared. Carefully presented. A little fast for some. Good relations with class. Enjoyable.
- Aiken, David: Good but got too deep too quickly for me.
- Taylor, John Lynn: Suggest future candidates study associated materials and send materials to participants for review and study.
- Steidley, Perry: I could follow Dr. Maki when he was discussing the topic but for me to duplicate it would be tough. Dr. Maki is very thorough.
- Foster, Douglas: Great instruction and good introductions. Good use of selected problems and solutions.
- Wagner, Charles: Another half hour of introduction would have been good.
- Gilmore, Tom: Cut back 30% and simplify. Keep the Boolean algebra, diagrams and truth tables. Topics are good, but there is too much information.
- Volkening, Larry: Need one on recap with problems, solving by singles or as groups. Excellent basic level.
- Bergstrom, Rich: Amazed that you could take us so far so quickly. Well paced, only a few times did you get over our heads.
- Gantz, Mike: Expand the lectures to four days – same amount as materials.
- Kemp, William: Excellent.
- Parker, Donald: Very good. Basic enough to use ideas in classroom and in grade school.
- Kurowski, Ed: Challenging and within the range of comprehension of the participants.
- DesArmo, Francis: Good. Very applicable in our high school geometry in our chapter on logic.

- Martell, Charles: Lecturer was very knowledgeable and organized but at times seemed to go too deeply into the material.
- Barton, Evan: I learned some concepts which will be useful in my teaching. I was impressed by Dr. Maki's concern for us.
- Weese, Jim: I liked Gary Maki's enthusiasm and excitement; but the first day was too fast. The second and third days were good.
- Hellman, Walter: An incredible amount of stuff was covered very well. It is hard to believe we could be taken from level zero to real application so quickly. Gary has a great feel for how to select what to teach, as well as what pace to teach at.
- Ovall, Larry: Good overview of logic.
- Pedlar, Craig: Presented very well, but I would have liked more "absorption" time, discussion time, and lab work time.

Comments on the electronics lectures:

- Burton, Fred: Good content. Basic transistor theory might have been helpful. Chip manufacturing process very helpful.
- Aiken, David: Good but got too deep too quickly for me.
- Taylor, John Lynn: Suggest future candidates study associated materials and send to participants for review and study. The given materials were very good and much appreciated.
- Steidley, Perry: Extremely well done!
- Foster, Douglas: Great state of the art formal presentations.
- Wagner, Charles: O. K.
- Gilmore, Tom: Good material on Hubble Space Telescope – hot topic. Cut back 20% Includes more practical examples: chips in toys, cars, appliances, etc. More real world material like telephones and communication satellites would be good.
- Volkening, Larry: Excellent basic level especially on manufacturing process.

- Bergstrom, Rich: Good ideas, the second day it got a little fast and over most of our heads. The other two days were outstanding.
- Gantz, Mike: Expand the lectures to four days – the same amount of time as materials.
- Kemp, William: A bit hard to follow at times but interesting and useful.
- Parker, Donald: Very good. I gained a basic understanding and will be able to use the concepts in my classroom.
- Kurowski, Ed: Challenging and within our range of comprehension.
- DesArmo, Francis: Very informative, although much of it was difficult for me to follow.
- Martell, Charles: Very good presentation but once again much material was too deep; it would have been better to aim a little lower but develop a better understanding.
- Barton, Evan: Appreciated being able to talk with a scientist involved in NASA programs.
- Weese, Jim: Day one was excellent. Days two and three I did not understand. Transistor graphics and overall concepts came through.
- Hellman, Walter: First lecture on transistor was the best explanation on the subject that I have seen or heard. Subsequent lecture covered too much too fast. The final lecture on fabrication was good.
- Ovall, Larry: Good presentation of circuitry and design.
- Pedlar, Craig: Presented very well. Personally, I would have been helped by more "absorption" time, discussion time, and lab work time.

Comments on the logic labs:

- Burton, Fred: Diagrams for our labs would have been helpful. Not enough time to digest theory, technical and practical.
- Aiken, David: Good hands on experience.

Taylor, John Lynn: Great.

Steidley, Perry: I was scared to death at the onset, but by the weeks end I had relaxed and learned.

Foster, Douglas: Good emphasis on topics that were covered in class.

Wagner, Charles; O. K.

Gilmore, Tom: About right.

Volkening, Larry: Need one final complete circuit diagram added after two or three days (sensor/timer/logic to yield an entire project).

Bergstrom, Rich: First day put the whole day together: outstanding! I got over my fear of electronic chips.

Gantz, Mike: I got lost at times because of a sometimes hurried pace, but overall it was very educational.

Kemp, William: Early instructions were weak – I was unsure of where we were going.

Parker, Donald: Excellent! I can use the information and procedures in my class.

Kurowski, Ed: Working in teams proved faster and more rewarding (2 per team) under the time constraints. If more time were available then maybe individual work would be best.

DesArmo, Francis: Great time. I did not think I had learned enough to apply it in lab, but I was wrong.

Martell, Charles: Well run lab which intertwined well with the lecture materials.

Barton, Evan: Good hands on experience. Projects were good! Could give a little more time to work on them.

Weese, Jim: The first two projects were easy to build; the third project was not so successful. There was good student help.

Hellman, Walter: Great hands on experience which was challenging but possible to do.

Ovall, Larry: Excellent applications of the logic circuitry and the electronics equipment.

Pedlar, Craig: Presented very well. Personally, I would have been helped by more "absorption" time, discussion time, and lab work time.

Comments on the piglet lab:

Burton, Fred: Amy Anderson (NASA scholar serving as Piglet instructor) was very helpful and related well with people older than herself: good skills.

Aiken, David: Very interesting.

Taylor, John Lynn: Great.

Steidley, Perry: This I dug! Also, Amy was wonderful, helpful and patient.

Foster, Douglas: Lots of fun – interesting to learn technologies of how everything is created and manufactured.

Wagner, Charles: Back off to smaller circuits that could be done in high school. Just lab (#2) was just great – the rest were o.k. but usable.

Gilmore, Tom: Cut back 1/3. Use one day to study the components in a personal computer. Troubleshooting.

Volkening, Larry: Helpers were excellent, knowledgeable and had the ability to relate.

Bergstrom, Rich: Good exercise. It was interesting to see how logic designers really work.

Gantz, Mike: Very well set up. Keep the one helper per two participants ratio. A listing of menu commands and what their function is (in layman's terms) would be nice.

Kemp, William: Needed more time but it was very enlightening.

Parker, Donald: Excellent. It was my first chance to use this type of computer. It was an excellent experience which we can bring back and use in the classrooms.

- Kurowski, Ed: Working in teams proved faster and more rewarding due to the time constraints. If more time had been available then individual work would have been best.
- DesArmo, Francis: Too many new commands in such a short time, but with the assistance received things went fine.
- Martell, Charles: Nice equipment to use, but perhaps a slower pace would be good.
- Barton, Evan: I enjoyed the hands on experience with computers and the insight into chip design.
- Weese, Jim: Amy is the greatest. I wish her luck in her current studies.
- Hellman, Walter: Good experience to see how this industrial and commercial application works.
- Ovall, Larry: Nice to see how the CAD program works since I had not used one before.
- Pedlar, Craig: Presented very well. Personally, I would have been helped by more "absorption" time, discussion time, and lab work time.

Comments on the projects lab:

- Burton, Fred: Good ideas that I can use immediately in class. A strong finale!
- Aiken, David: Most directly applicable to high school teaching.
- Taylor, John Lynn: Very very good – I loved the take home materials.
- Steidley, Perry: The circuits and projects were wonderful.
- Foster, Douglas: I would have added some direct interfacing designs. I will be glad to come back and help out. Probably having a IIE or IBM and showing how to actually interface them would be great help.
- Wagner, Charles: O. K.

- Gilmore, Tom: Focus on four specific devices. Make sure that each device gets tested and works.
- Volkening, Larry: Need one final complete circuit diagram added after. two or three days (sensor/timer/logic) to yield and entire project.
- Bergstrom, Rich: Very good. But need to have better equipment so it would work more often. It became frustrating when some of the projects did not work. Gained tremendous ideas to give to kids for hands on experience.
- Gantz, Mike: Excellent. Larry was superb. Materials are greatly appreciated. Very understandable.
- Kemp, William: Excellent – need more equipment so you could save something once it worked.
- Parker, Donald: Excellent. Will use for sure.
- Kurowski, Ed: Working in teams proved faster and more rewarding under the time constraints. If more time had been available then maybe individual work would have been best.
- DesArmo, Francis: Had fun. Actually had success. Nice loose atmosphere in all classes made it enjoyable.
- Martell, Charles: Great stuff. The most successful of all materials.
- Barton, Evan: Would help to have diagrams to do projects.
- Weese, Jim: I will use more of this in class than all the other presentations. A written description of each lab with expected results and possible extensions would really be appreciated – especially two months from now when memory and notes fail.
- Hellman, Walter: Not clear yet – still assembling.
- Ovall, Larry: Again, excellent use of the electronic devices talked about during the week.
- Pedlar, Craig: Presented very well. Personally, I would have been helped by more "absorption" time, discussion time, and lab work time.

Did you gain the skills you expected?

All participants answered "yes."

Suggestions/comments regarding whether or not expectations were met:

- Aiken, David: I really did not know what to expect – but I am not disappointed.
- Steidley, Perry: I saw my limitations and liabilities quickly!
- Wagner, Charles: A few more basic electronic logic setups.
- Gilmore, Tom: Guest speakers from Apple, IBM, or NASA. Trips to chip manufacturers or a video on actual chip production. Film material on NASA projects that can be used with our classes.
- Volkening, Larry: We need a group meeting to finalize each of our parts and to help each plan if to continue next year.
I gained more insight in how design engineers work and how chips are made.
- Gantz, Mike: the CAD, Logics lab and Projects lab were extremely informative.
- Kemp, William: I am not sure what I expected but it was extremely worthwhile.
- Parker, Donald: My cup runneth over.
- Kurowski, Ed: More than I expected in some cases.
- DesArmo, Francis: You are doing a great job at promoting the sciences. Your enthusiasm for your work is truly invigorating. I wish all universities put forth the effort I have witnessed at the University of Idaho.

Martell, Charles: Focus more on certain concepts or skills and allow more time to master these skills. Much went over my head, but I gained much information which will help me.

Weese, Jim: I expected more basic component use and testing using testing devices like the oscilloscope and the test probes on the bread board.

Ovall, Larry: I feel more comfortable with microelectronic technology now. Not so afraid to tackle this area alone now.

Pedlar, Craig: I would have liked to have had a two week session – with more time to absorb material presented, work on projects (to actually make them work) and really comprehend their operation and fundamentals regarding that operation: some evenings to discuss this with instructors and other participants. Some free time to use other campus facilities would be nice.

Are you going to be able to use these skills in your classroom ?
All participants answered “yes”.

Suggestions/comments regarding skills learned:

Burton, Fred: I had not had any training with IC's.

Taylor, John Lynn: Most definitely just what I wanted and needed.

Wagner, Charles: I have found two truth table labs that I can put to good use! These labs alone made the institute worthwhile but there was much more and very good.

- Volkening, Larry: I would like a classroom set of equipment as listed in hand-out.
- Bergstrom, Rich: I will use a lot of the information given here to pass on to students. But to actually create some of the circuits I really do not know.
- Gantz, Mike: I would suggest that the lectures be toned down to a high school level. More information based on electronics.
- Parker, Donald: Maybe not the specifics but the generalities.
- Kurowski, Ed: PC boards – especially if I can get 25 or so.
- Martell, Charles: Projects class has some good activities and I will do some digital work with my AP kids.
- Barton, Evan: Students have very little knowledge in the area of microelectronics. This class will help me to help eliminate this problem.
- Weese, Jim: Breadboarding, truth tables, value of Boolean algebra all helpful.
- Ovall, Larry: It will take me some time to work it in but I see plenty of places for it.

Misc. Suggestions:

- Burton, Fred: Consider a slower pace, more background, more basics, more practice, and extend to two weeks.

- Foster, Douglas: I would have liked to had some time to see what research projects are being staffed in various departments – especially the physics department. I would be glad to teach a course on digital interfacing for Apple 2E computers/MAC computers. Hands on building kits and trying them would be good.
- Gilmore, Tom: Try to incorporate local students into an Electronic Lab Day. Let the teachers work as T. A.'s one afternoon with students. Let us see if these electronic devices actually work with junior high students.
- Volkening, Larry: 1) Need more time to stream-line and allow free time. 2) Need to give each participant a formal chance to speak to others, if so desired (idea sharing/problem solving session).
- Bergstrom, Rich: I would not change much about the workshop. It was fast pace and fun. For a week long workshop this was very well done and extremely well organized.
- Gantz, Mike: Five full days instead of four and a half. I do not think the text was needed: apply the money used to some other fund.
- Kemp, William: Thursday we needed longer lab periods once we got going.
- Parker, Donald: Continue to give this type of workshop, possibly two times per year. Give a two day workshop for teachers and students during the year.
- Kurowski, Ed: Keep up the great work and try to involve some of us again next year or in a three year master's program.
- DesArmo, Francis: I would have liked just a few more minutes when attempting problems.
- Martell, Charles: Your ideas for on going activities are great. We need to encourage more summer workshops and summer training for science teachers. Keep up the good work!!!
- Barton, Evan: It would be helpful to have more information on our level. A little more time on projects. It would be nice to have time in the evenings to become somewhat familiar with the surroundings.

- Weese, Jim: More applications and uses of electronics – research edge! Money for equipment for classroom use. A slower pace. Begin projects earlier in the week (more time to do lab extensions). Additional speakers could be brought in from industry. “War stories” of design and manufacturing problems are of great interest to students and are great fill in and attention getters for teachers.
- Hellman, Walter: Maybe things will change but logic text was not use much here and I will use it much in the future. A general purpose electronics reference would be more useful.
- Ovall, Larry: It would be possible to be much stronger and better able to implement this technology if this institute were for a longer time.
- Pedlar, Craig: Possible consider a two or three stage program providing 1) a week as we had (maybe less rigorous) 2) following year – a two week session with time for comparing what was done during the year 3) the third year the “work with a scientist” month.

Additional Comments:

- Burton, Fred: It’s difficult to critique something that is done so well. Excellent choice of staff! Each related well with us. Staff and participants both wanted to learn and share expertise. All were committed to our task. Well planned and executed. Staff members complemented and supported each other’s work.
- Steidley, Perry: This workshop opened my eyes to an area of physics that I was not current on and have not used in my curriculum! I will be more aware of these areas in my future teaching.
- Foster, Douglas: I will send you a copy of PSSC Physics Chapter and labs in logic circuits. I suggest you send this and other basic material to all participants and in the future to all participants ahead of the workshop. It would have been nice to have some time to share with other physics teachers some ideas about what we are doing. Plan and announce ahead of time so that everyone can bring some ideas!

- Wagner, Charles: Instructors and helpers were really very good. Introduction - update - future. The way material has to be presented in short session. Very pleased by individuals running course.
- Gilmore, Tom: Good use of graduate students in this program! Judy, you did an excellent job - many thanks!
- Volkening, Larry: Judy and Kelli did an exceptional job of organizing, etc. the entire workshop. I can't say enough good words. Let's consider designing and making parts available for teachers and students to build a complete single function computer from sensing through computation to read-out. Make circuit diagram and piglet print-out part of the package. Example: display T; calculate a; display a from $s = 1/2 at(sq)$; as the result of four photogates being trapped.
- Bergstrom, Rich: I think Judy and her staff made the workshop a big success. My hat is off to them. This has been a great energizing time for me. Please run it a lot more times.
- Gantz, Mike: I would like to see more release time in the evening. No one really had a chance to see the area. The instructors, helper, etc., were the best I have ever had. This program is super! I have tried to introduce electronic circuits but have never gotten beyond resistors and capacitors. Now I have a knowledge that I will use a great deal in my classes.
- Kemp, William: The attitudes and interest by all the instructors, especially Gary, was tremendous. You made us feel wanted, needed and treated us as professionals. You listened and helped - thanks for the experience.
- Parker, Donald: Set up field trips for students and teachers, rural area students are not aware of the outside world. Industry as well as college campus life similar to Agriculture and Science Days at Oregon State, Science and Humanities or Science Experience Days. Each time I attend a workshop like Sir Issac Newton I stand on the shoulders of giants and see further than before. This time is no exception; however, the giants were much larger.

- DesArmo, Francis: Evenings free. The talks in the evening were very good and should not be dropped. I don't know when they would be best.
- Martell, Charles: A good week but maybe a little too much information overload. Material would be better understood over two weeks with more lab type activities.
- Weese, Jim: A second week of basic electronics using and testing basic electronic components with specific emphasis on the oscilloscope. My electricity (math oriented) was college taught - my electronics and meter use is mostly self taught. Many physics minors or less have had very little electricity.
- Hellman, Walter: I might "free" to see a little bit of the area. This is a great experience. I hope others will have the opportunity to partake of it! I wouldn't change in any major way at all - you've hit on something really good the first time.
- Ovall, Larry: This institute allowed a wide variety of physics teachers to come together for a week and share their experiences in the classroom and beyond. That is an invaluable additional result of getting together.

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