FAULT HANDLING SCHEMES IN ELECTRONIC SYSTEMS WITH SPECIFIC APPLICATION TO RADIATION TOLERANCE AND VLSI DESIGN

FINAL REPORT (NAG 9-337)

JOHN OKYERE ATTIA

(MINORITY CONSORTIUM FOR STUDY OF SPACE RADIATION ON MATERIALS, SYSTEMS AND DEVICES)

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COLLEGE OF ENGINEERING AND ARCHITECTURE
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ABSTRACT

Naturally occurring space radiation particles can produce transient and permanent changes in the electrical properties of electronic devices and systems. In this work, the transient radiation effects on DRAM and CMOS SRAM were considered. In addition, the effect of total ionizing dose radiation of the switching times of CMOS logic gates were investigated.

Effects of transient radiation on the column and cell of MOS dynamic memory cell was simulated using SPICE. It was found that the critical charge of the bitline was higher than that of the cell. In addition, the critical charge of the combined cell-bitline was found to be dependent on the gate voltage of the access transistor.

In addition, the effect of total ionizing dose radiation on the switching times of CMOS logic gate was obtained. The results of this work indicate that, the rise time of CMOS logic gates increases, while the fall time decreases with an increase in total ionizing dose radiation. Also, by increasing the size of the P-channel transistor with respect to that of the N-channel transistor, the propagation delay of CMOS logic gate can be made to decrease with, or be independent of an increase in total ionizing dose radiation.

Furthermore, and method was developed for replacing polysilicon feedback resistance of SRAMs with a switched capacitor network. A switched capacitor SRAM was implemented using MOS Technology. The critical change of the switched capacitor SRAM has a very large critical charge. The results of this work indicate that switched capacitor SRAM is a viable alternative to SRAM with polysilicon feedback resistance.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

Naturally occurring space radiation environment can produce transient and permanent changes in the electrical properties of electronic devices and systems. Some radiation particles in the space environment are electrons, protons, cosmic ions and alpha particles. These particles can cause transient changes or permanent damage in electronic ciruits. One of the aims of radiation studies is to design devices, circuits or systems whose operation is insensitive to radiation.

CMOS (Complementary metal oxide silicon) logic gates are the basic building blocks of space electronic systems, such as space vehicles and satellites. CMOS logic gates have low power dissipation and high noise margin. These two properties make the use of CMOS logic gates more desirable in space electronic systems.

As a result of radiation, logic upset can occur in a CMOS logic gate. A logic upset may change the state of a logic device. Also, an upset at a gate can be transmitted to different parts of a circuit. Single event Upset (SEU) can cause a memory cell to change its logic state. Such an upset is temporary and non-recurrent. An SEU is induced when a charges particle strikes a portion of an integrated circuit and creates a large number of electron and hole pairs along its path. In order for SEU to occur, a particle hit has to occur at a sensitive node of an integrated circuit and the circuit has to collect enough charge to cause the logic state of the circuit to change.

Total Ionization Dose (TID) radiation results in parametric changes in MOS devices. The principal TID effects on MOS transistors are negative shift in the

threshold voltage and degradation of channel mobility. Since the threshold voltage amd mobility affect the performance of MOS devices, the TID radiation will affect the operation of electronic systems built using MOS devices.

There are three objects of this work:

(1) To obtain the critical charge of memory cell and bitline of DRAM.

(2) To determine the effect total ionizing dose (TID) radiation the switching time of CMOS Logic Gates.

(3) To explore the use of switched capacitor networks for hardening CMOS SRAM against single event upsets.

In Chapter 2, the critical charge of DRAM is obtained. It will be shown that the critical charge is dependent on the gate voltage of the access transistor. A way of integrating the circuit analysis software, SPICE, and FORTRAN is shown. The latter is needed for the calculation of the critical charge.

In Chapter 3, the rise time, fall time and propagation delay of CMOS logic gates are derived. The effects of total ionizing dose radiation on the fall time and rise time of CMOS logic gates were obtained using C program calculations and PSPICE simulations. The variations of mobility and threshold voltage on MOSFET transistors when subjected to TID radiation were used to determine the dependence of switching times on TID.

In Chapter 4, a method is developed for replacing polysilicon feedback resistors by switched capacitor networks. A switched capacitor SRAM is implemented using MOS technology. Computer simulations using SPICE was performed on switched capacitor SRAM, and SRAM with and without feedback resistors.

CHAPTER 2

SINGLE EVENT UPSET SUSCEPTIBILITY OF DRAMs

2.1 DRAM

The MOS DRAM is a widely discussed integrated circuit because of the significant impact it has had on the performance and growth of all types of computers over the last two decades. MOS DRAMs are relatively faster, cheaper and smaller than SRAMs.

One configuration of the one-transistor dynamic memory cell is shown in Figure 2.1. It consists of an access transistor and a storage capacitor [1]. Logic "1" or "0" is represented by the presence or absence of charge on the storage capacitor. Because of leakage current, the charge stored on the capacitor disappears with time. DRAM must be refreshed periodically. For efficient operation of the DRAM, the leakage current must be very small, such that the refresh rate will be considerably low compared to the operating frequency of the dynamic memory.

Information is written into the memory cell by placing the data on the bitline and transferring the data on the bitline into the capacitor through an access transistor. Signal on the word line turns the access transistor on or off. A READ is performed by precharging the bitline and raising the voltage on the word line. Charge sharing between the storage cell and the bitline capacitances changes the voltage on the bit line which is detected using a sense amplifier. For each bit, the sense amplifier

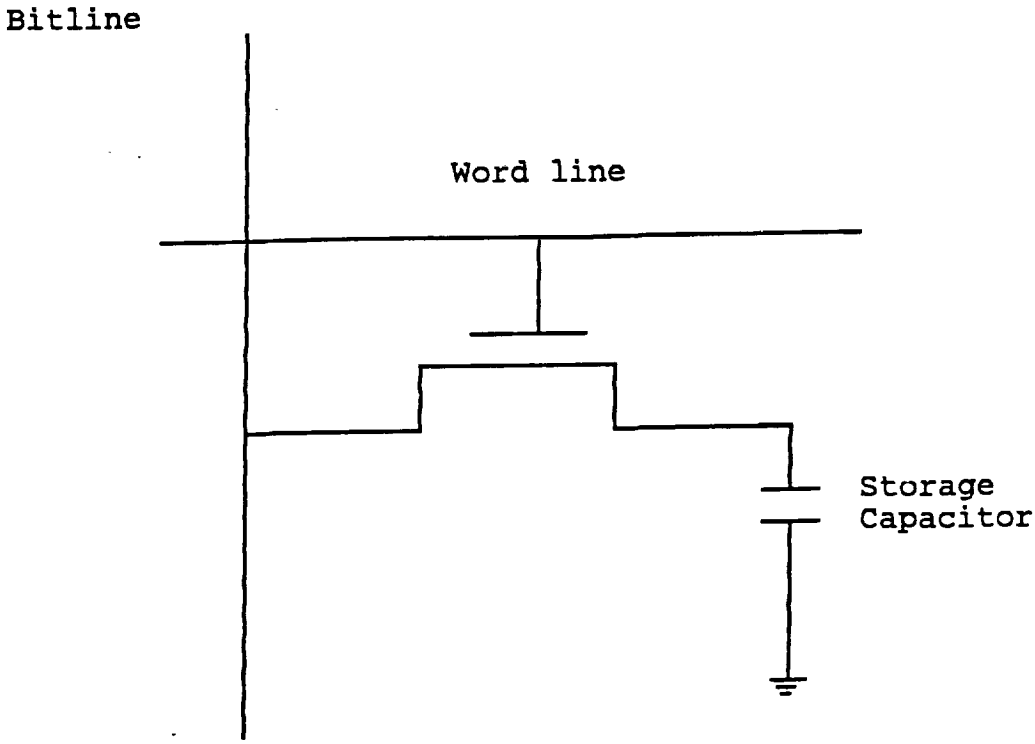


Figure 2.1 One Transistor DRAM Cell

restores the small bit line voltage swing to a full voltage level required to distinguish logic "1" from logic "0". The information on the cell is destroyed when read.

"Sense-application" circuitry must be provided for each bit line to restore the small bit line voltage swing to the full voltage levels required to distinguish a logic "1" or a logic "0".

DRAM cells can suffer single-event upset or soft errors due to ionizing radiation. Upsets are the result of free carriers created by ionizing radiation that can be collected directly by the cell's storage capacitor, upsetting the stored charge. Soft errors can also occur as a result of ionizing radiation striking bitlines or storage cells or sense amplifiers.

In this chapter, the critical charge of the DRAM will be obtained. It will be shown that the critical charge is dependent on the gate voltage on the access transistor. Integration of the circuit analysis software, SPICE, and FORTRAN is required for the critical charge computation. A batch program that allows such integration was written. This program is described in this report.

2.2 RADIATION EFFECTS ON DRAMS

Soft error was first reported by May and Woods [2] in 1979. They found that alpha particles are emitted by radioactive decay of uranium and thorium which are present in minute quantities in packaging materials. Alpha particles penetrate the die surface to create enough electron- hole pairs near a storage node to cause a random, single-bit error.

Sai-Halasz et al [3] examined the effects of scaling on the soft error rate. They found that with the reduced feature size, the critical charge is reduced and multiple errors increase. They suggested some modifications to reduce the soft error rate in DRAMS: (1) delay the arrival of excess minority carriers to circuit nodes by inducing fields in the substrate. (2) reduce the minority carrier lifetime and (3) provide regions where the excess carriers are collected and dispersed without harm to the circuits. They found that the most promising modification is the incorporation of a buried grid of opposite conductivity type from the substrate.

Two modes of upset of MOS dynamic RAM were discussed by Toyabe et al [4]: memory-cell mode and bit-line mode. In the memory-cell mode, an upset is caused by radiation-generated electrons flowing into the storage capacitor. In the bitline mode, an upset is caused by electrons flowing into the n+ diffused layer in a floating bitline in a read cycle. Since this failure mode occurs only in the read cycle, the soft error rate due to this mode is proportional to the access frequency (inversely proportional to the cycle time).

Hague et al [5] measured the soft error rates of commercially available 64K and 256K DRAM using a MC6800 microprocessor in conjunction with an Am-231 alpha source. They observed that the spread of SEUs over a particular device/manufacturer was much smaller than the differences between device families and manufacturers. In addition, they found that the devices showed widely differing rates, bit-line upsets dominate in 64K and cell upsets predominate in the 256K DRAMs.

Computer simulations of alpha bits on a 64K MOS dynamic RAM were done

using the circuit simulation program SPICE [6]. Not only were the bitline and storage cell capacitors shown to be susceptible to upset, but the sense amplifier columns were shown to upset as a result of alpha particle hit. Parasitic column capacitance and resistance were represented by a multi-stage RC delay line. An exponential decaying current source with a time constant of 1 nanosecond was used to represent the current due to the collected alpha generated charge. The soft errors were found to be dependent on the impedance of the interrupt device (device that decouples the column from the sense amplifier, allowing the low going node of the sense amplifier to pull down faster). In general, it was observed that during a sense amplifier hit, charge collected by the sense amplifier node can be dissipated to the column through the interrupt device. In addition, if a hit occurs during precharge, charge is drained from the column through the pre-charge device to a power supply, and this type of hit does not cause soft errors. However, if hit occurs just before precharge ends, enough charge may remain on the sense amplifier node to cause false latching.

A recent failure mode combined cell-bitline (CCB) of radiation-induced soft errors in dynamic memories was recently reported [7]. It occurs when the cell and the bit line each collects radiation-induced charge which is insufficient to upset the cell, but which does cause an error in combination. The study indicates that, at short cycle times, CCB failure can dominate soft error rate in high-density, high- speed dynamic memories.

2.3 CRITICAL CHARGE OF DRAMS

A high energy particle can strike the storage capacitance nodes and/or the bitline. The charged particle, penetrating the memory cell device, will produce a number of carriers determined by it initial energy. The generated carriers appear as "photo currents" within the affected nodes of a device. Cell upsets will take place if enough charge is delivered to the hit node. The charge needed to cause cell upset is termed critical charge, Q_{crit}

Critical charge is a measure of single event vulnerability of RAM cells. It can be evaluated by analysis or simulation of circuits and layouts during the design cycle [8]. The critical charge offers an advantage of preproduction assessment thereby allowing for design optimization.

In general, the critical change of sensitive nodes is expressed as:

$$Q_{crit} = \int_0^{\infty} i(t)\,dt \qquad (2.1)$$

but, the current i(t) can be approximated as:

$$i(t) = Ae^{-t/\tau} \qquad (2.2)$$

and the charge is given as:

$$Q_{crit} \approx \int_0^{5\tau} Ae^{-t/\tau} \qquad (2.3)$$

where:

A = current amplitude

τ = the falling time constant

= 250ps [Diehl et al, 1982]

Equation (2.3) simplifies to:

$$Q_{crit} = AT \qquad (2.4)$$

A is the amplitude of the exponential pulse that will cause the cell to upset. It is obtained by using both SPICE and FORTRAN programs.

SPICE [9] is one of the popular circuit simulation tool in use today. AC, DC, transient and Fourier analysis can be performed using the SPICE software. Circuit analysis using SPICE is done on a user-written program consisting of formalized statements describing the circuit elements, node connections and parameters that specify the electrical characteristics of the elements in the circuit. One of the drawbacks of SPICE is its inability to embed itself into a fortran program. Since A of equation (2.4) has to be obtained using an iterative process, a special interface program had to be written so that SPICE can be run under a "shell". The next section describes this interface program.

SPICE circuit simulator requires the device dimensions such that the program can calculate capacitances and resistances at each circuit node. Table 2.1 shows the capacitance and resistance of DRAM circuit.

TABLE 2.1

CAPACITANCE AND RESISTANCES FOR 64K DRAM CIRCUIT

Bitline capacitance per memory cell	= 32 fF
Memory cell capacitance	= 30 fF
Diffusion resistance of bit line per cell	= 275 Ohms
Gate capacitance per memory cell	= 44.16 fF
Poly resistance of the gate per cell	= 20 Ohms

2.4 INTERFACING SPICE TO FORTRAN PROGRAMS

Figure 2.2 shows an example of the program that was used to interface the SPICE software with FORTRAN program. This is a DOS batch program [10] The program was actually used to find the amplitude of an exponential decaying signal that will cause the upset of a cell when there is a hit on the memory capacitor. Similar programs were used to obtain the critical charges when hits occurred on the column, and combined cell- column hits. A simplified flowchart of the interface program is shown in Figure 2.3. The SPICE circuit file, CELL.CIR is created. The SPICE circuit file, CELL.CIR was formed by combining files "CELL-1.DAT" and "CELL-2.DAT." "CELL-1.DAT contains information about the exponential signal used for the transient analysis. The amplitude of the exponential signal was incremented at each run of the SPICE program when this batch program is running. The file "CELL-2.DAT" contains information about the memory circuit which does not change

```
REM CELL1.BAT
REM  CREATE A FILE FOR COUNTING NUMBER OF ITERATION
:REPEAT
REM TRANSIENT ANALYSIS IS PERFORMED (SPICE)
CD C:\PSPICE
PSPICE1 CELL1.CIR CELL.OUT
REM OUTPUT OF MEMORY CELL IS TESTED (FORTRAN)
CD C:\FORTRAN3
COPY C:\PSPICE\CELL.OUT C:
SWITCH
REM TEST FOR CHANGE OF STATE
IF EXIST STATECHG.DAT GOTO DONE
REM CHANGE THE AMPLITUDE OF CURRENT PULSE
VARCHG
COPY CELL-1.DAT + CELL-2.DAT CELL.CIR
COPY CELL.CIR C:\PSPICE
GOTO REPEAT
:DONE
DEL STATECHG.DAT
```

Figure 2.2 Example of a DOS batch Program for Embedding SPICE into a FORTRAN Program

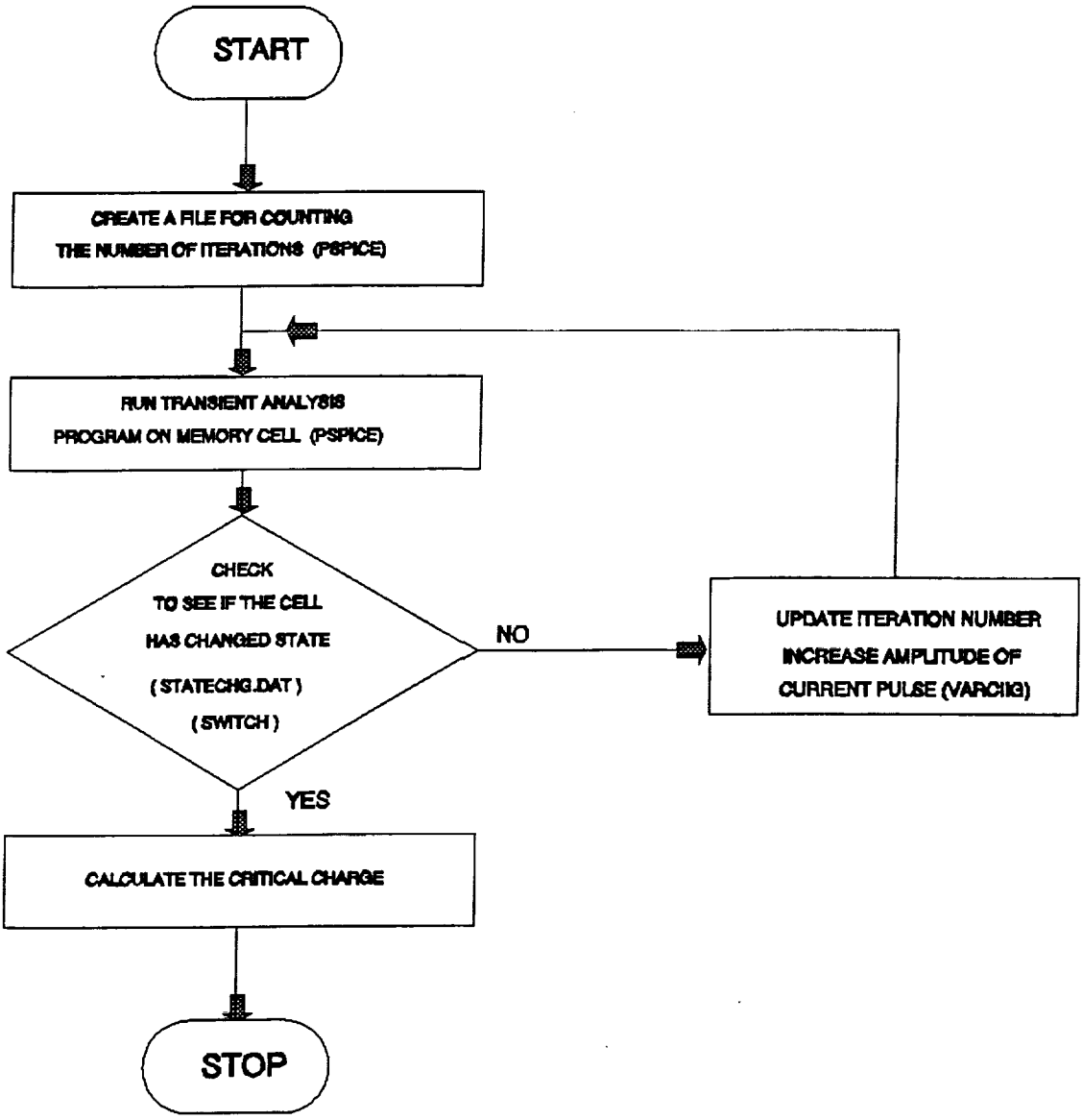


Figure 2.3 Flowchart for a Program for Embedding SPICE into a FORTRAN Program.

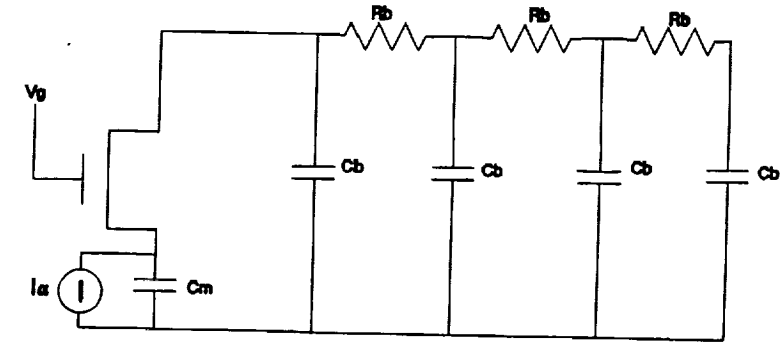
at each run of the SPICE program. In addition, a file is created for counting the number of time the SPICE program has ran. This is done using the FORTRAN program "COUNT". Transient analysis program is run. The Fortran program "SWITCH" is used to test whether the output of a cell has changed state. If there is a change of state, a file STATECHG.DAT is created. If there is no change of state, the amplitude of the current pulse is incremented using the FORTRAN program "VARCHG". The pulse information (amplitude) in the file CELL-1.DAT is changed at each run of the FORTRAN program "VARCHG." With the change in amplitude of the pulse, the transient analysis is run again.

2.5 CRITICAL CHARGE FOR SENSITIVE NODES OF DRAM

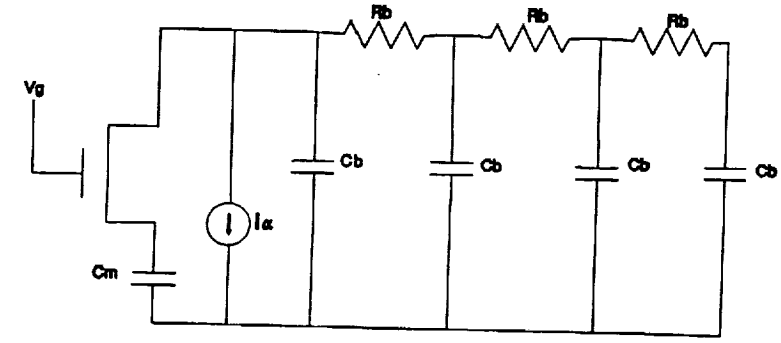
Dynamic memories have structures particularly sensitive to alpha particle bits. They are the bitline and the storage cell capacitors. Figure 2.4 shows the circuit models used for the cell, bitline and combined cell-bitline particle hit simulation. Current source is used to represent collected alpha generated electrons [6].

Because of implanted nodes associated with polysilicon columns of the bitlines, bitlines have a small effective charge collection area, therefore, the amount of charge collected at the bitline region during alpha hit is reported to be small. Unlike bitline node, the memory cells are floating during precharge. Thus a cell hit during precharge as well as after precharge but prior to latching can upset stored information.

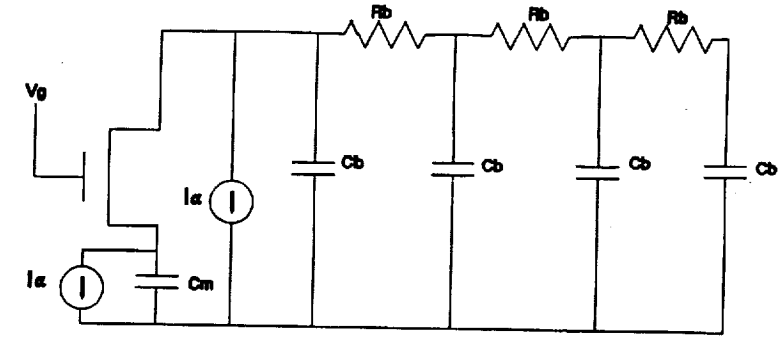
Due to the distributed RC network of the bitline, the bitline node closest in the access transistor will have the lowest critical charge compared to the critical charge at other nodes of the bitline [6]. A hit at the storage capacitor node may be able to



(a)



(b)



(c)

Figure 2.4 Circuit Models for SPICE Simulation of Alpha Particle Hits. (a) Cell hit, (b) Bitline hit and (c) Cell and Bitline hits.

discharge the charge stored on the cell capacitor. Using the DOS batch program, SPICE simulations were performed on the memory cell assuming the cell has four columns with 256 rows, the critical charges obtained for the cell and bitline are shown in Table 2.2. The amplitude values for the various sensitive nodes simulated during alpha particle hit are:

Bitline = $1.68*10^{-3}$ A

Cell capacitance = $3.8*10^{-4}$ A

Combined Cell-Bitline (0 gate voltage) = $3.7 * 10^{-4}$ A

Combined Cell-Bitline (5 gate voltage) = $1.36*10^{-3}$ A

Table 2.2 lists the major results of the critical charge on bitline, cell, and combined cell-bitline. The combined cell-bitline was compared for 0 and 5V gate voltages.

TABLE 2.2

CRITICAL CHARGES ON CIRCUIT NODES

Nodes	fC
BITLINE	425
Cell	105
Combined Cell-Bitline (0V)	105
Combined Cell-Bitline (5V)	360
Critical charge of cell	92.5
Critical charge of bitline	420

Figure 2.5 shows the voltage across the memory cell capacitor versus time, when the capacitor was bit by a source whose amplitude was large enough to cause the capacitor to lose its charge. A figure similar to figure 2.5 was obtained when the current pulse was large enough for the charge stored on the column capacitances to be lost.

Critical charge was also found when both the memory cell and the bitline were hit at the same time. The critical charge for the combined cell-bitline was obtained with respect to the gate voltage of the access transistor. Table 2.3 shows the critical charge as a function of the gate voltage of the access transistor. Figure 2.6 shows the critical charge as a function of the gate voltage.

2.6 DISCUSSION OF RESULTS

For the DRAM, the critical charge of 92.5 fC was obtained for the cell and the value of 420 fC was obtained for the bitline. The critical charge obtained in this work is similar those reported in the literature. The critical charge obtained by May and Woods [2] was between 20 to 150 fC. The range for the critical charge of DRAMs reported by Peterson et al [11] was between 20 to 180 fC.

For the DRAM cell, it was found that the critical charge of the memory cell is dependent on the gate voltage of the access transistor. This result has not been reported in the literature. The results seem to indicate that when the access transistor is turned on, the memory capacitance and the bitline capacitance form an RC network and because of charge sharing among the capacitances, the charge needed to cause the memory to change state is increased.

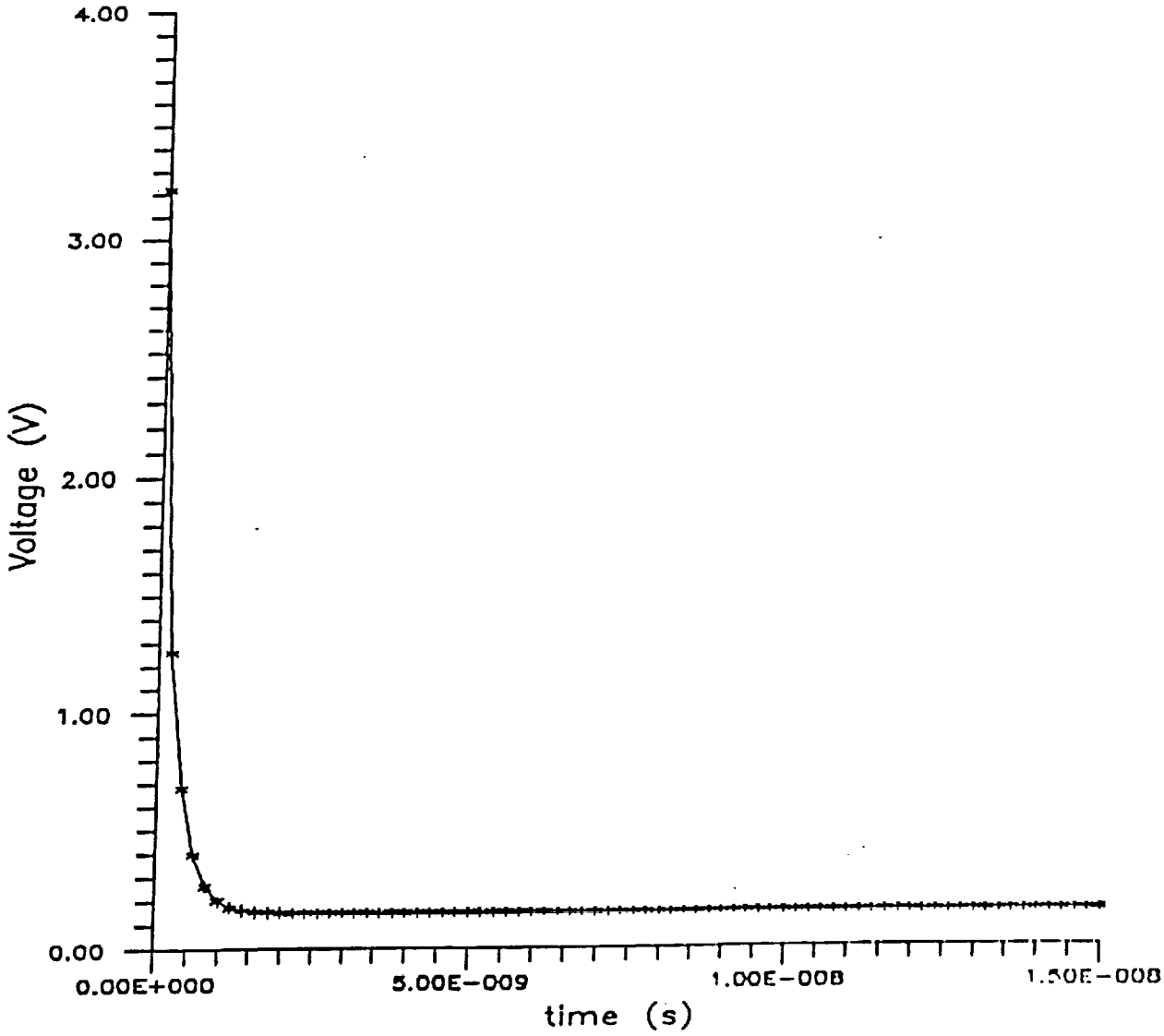


Figure 2.5 Voltage across Memory Cell Capacitor versus time.

TABLE 2.3

CRITICAL CHARGE FOR THE MEMORY CELL AS A FUNCTION OF GATE VOLTAGE OF THE ACCESS TRANSISTOR

GATE VOLTAGE (V)	AMPLITUDE OF CURRENT PULSE (A)	CRITICAL CHARGE (fC)
0	0.37E-03	92.5
1	0.38E-03	95.0
2	0.60E-03	150.0
3	0.90E-03	225.0
4	0.116E-02	290.0
5	0.136E-02	340.0

The dependence of critical charge on the access transistor gate voltage is in apparent conflict with the recently announced DRAM soft error, the combined cell-bit (CCB) failure mode of DRAMs [7]. This failure mode occurs when the cell and the bitline each collects radiation induced charge which is insufficient to upset the cell, but which does cause an error in combination. The CCB failure mode seems to dominate soft error rate in high density, high speed dynamic memories at short cycle times. In this work, short cycle times were not assumed while calculating the critical charge for the DRAM cell and bitlines. Issues related to short cycle times will be considered in future.

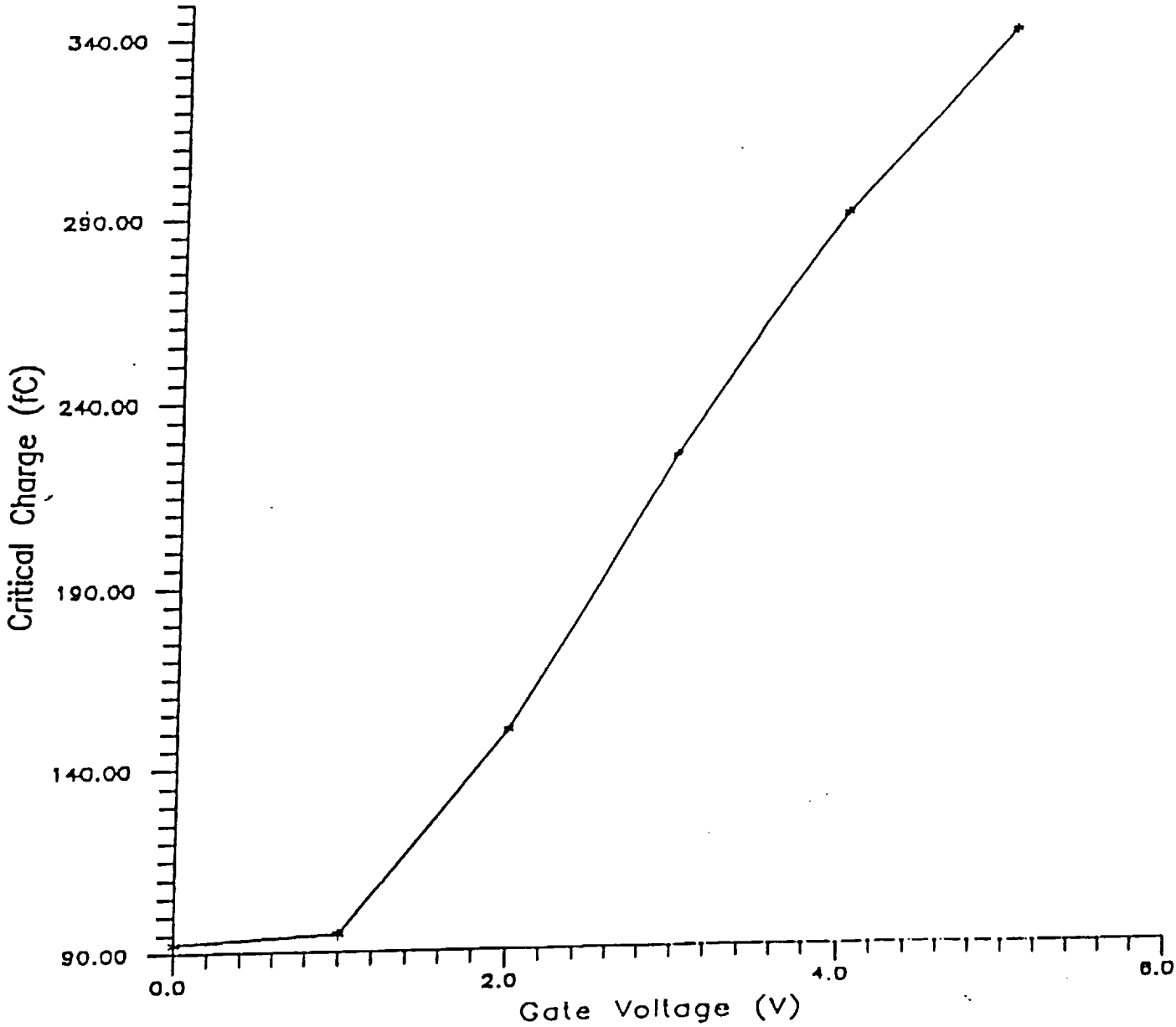


Figure 2.6 Critical Charge as a function of Gate Voltage of Access Transistor.

2.7 CONCLUSIONS

The critical charge of the DRAM memory cell and bitline were determined. The values obtained are similar to those reported in the literature. The critical charge of memory cell was found to be dependent on the gate voltage of the access transistor.

In addition, critical charge for the combined cell-bitline upset is a voltage dependent. If the bitline and cell are decoupled by having a zero gate voltage, the critical charge is lower than if the bitline is coupled to the memory cell through the access transistor.

2.8 REFERENCES

[1] Rideout, V.L. One-Transistor Cells for Dynamic Random-Access Memories: A Tutorial, IEEE Trans. Electron Devices, Vol. ED-26:839-852, 1979.

[2] May, T.C. and Woods, M.H. Alpha-Particle-Induced Soft Errors in Dynamic Memories. IEEE Trans. on Electron Devices, Vol. ED-26:3-9, 1979.

[3] Sai-Halasz, G.A., Woodeman, Mr.R. and Dennard, R.H. Alpha-Particle-Induced Soft Error Rate in VLSI Circuits. IEEE Trans. on Electron Devices: Vol. ED-29:725-731, 1982.

[4] Toyabe, T., Shinoda, T., Aoki, M., Kawamotu, H., Mitsusada, K. Masuhara, T. and Asai, S. A Soft Error Rate Model for MOS Dynamic RAMs. IEEE Trans. on Electron Devices, Vol. ED-29: 732-737, 1982.

[5] Hague, A.K.M.M., Yates, J. and Stevens D. Upset Susceptibility of 64K and 256K DRAMs to Alpha Particle Irradiation. Proc. Ist Int. Conference on Radiation Damage to Material and VLSI Circuits. Houston, Texas, Jan. 1987.

[6] McPartland, R.J. Circuit Simulations of Alpha-Particle-Induced Soft Errors in MOS Dynamic RAM's. IEEE Journal of Solid-State Circuits, Vol. SC-16: 31-34, 1981.

[7] Rajeevakumar, J.V., Lu, N.C.C., Hennkels, W.H., Hwang, W. and French, R. A New Failure Mode of Radiation-Induced Soft Errors in Dynamic Memories. IEEE Electron Device Letters. Vol. 9:644-646, 1988.

[8] Kerns, S.E., "Transient-Ionizaiton and Single Event Phenomena, In Ionizing Radiation Effects in MOS Devices and Circuits, Eds. T.P. Ma and P. V. Dressendorfer, pp.485-576, John Wiley & Sons, New York, 1989.

[9] Nagle, L.W. "Spice2: A Program to Simulate Semicouductor Circuits", University of California, Berkelely, California, ERL-MS20, May 1975.

[10] DeVoney, C. DOS Tips, Tricks and Traps, Que Corporation, Carmel Indiana, 1989.

[11] Petersen, E.L., Shapiro, P., Adams, J.H. and Burke, E.A. Calculation of Cosmic-Ray Induced Soft Upsets and Scaling in VLSI Devices, IEEE Trans. Nucl. Sci., Vol. NS-29: 2055-2063, 1982.

CHAPTER 3

THE EFFECTS OF TOTAL IONIZING DOSE RADIATION ON THE SWITCHING TIMES OF CMOS LOGIC GATES

3.1 INTRODUCTION

Space electronic systems are affected by radiation which can cause deterioration of system performance or system failure. Most space systems have MOS devices as basic building devices for computing and storage of information. MOS devices when subjected to total ionizing dose (TID) radiation experience shifts in the device parameters due to increased oxide trapped charges and interface states [1]. The principal TID effects on MOS transistors are negative shift in the threshold voltage and degradation of channel mobility [2]. The threshold voltage and mobility affect the performance of electronic circuits.

In this chapter, we investigate the effect of TID on the rise time, fall time and propagation delay of CMOS INVERTERS, NAND and NOR gates. In addition, the effect of transistor sizing on the propagation delay of CMOS logic gates under the influence of TID radiation will be explored.

3.2 SWITCHING TIME EXPRESSIONS

Figure 3.1 shows a block diagram of a generic CMOS logic gate. The node capacitance at the output represents the equivalent load capacitance due to transistor gate capacitance, metal interconnect capacitance, and diffusion capacitance [3]. The capacitor will be charged during pull-up (or rise time transition) and it will be discharged during pull down (of fall time transition). The P-channel and N-channel

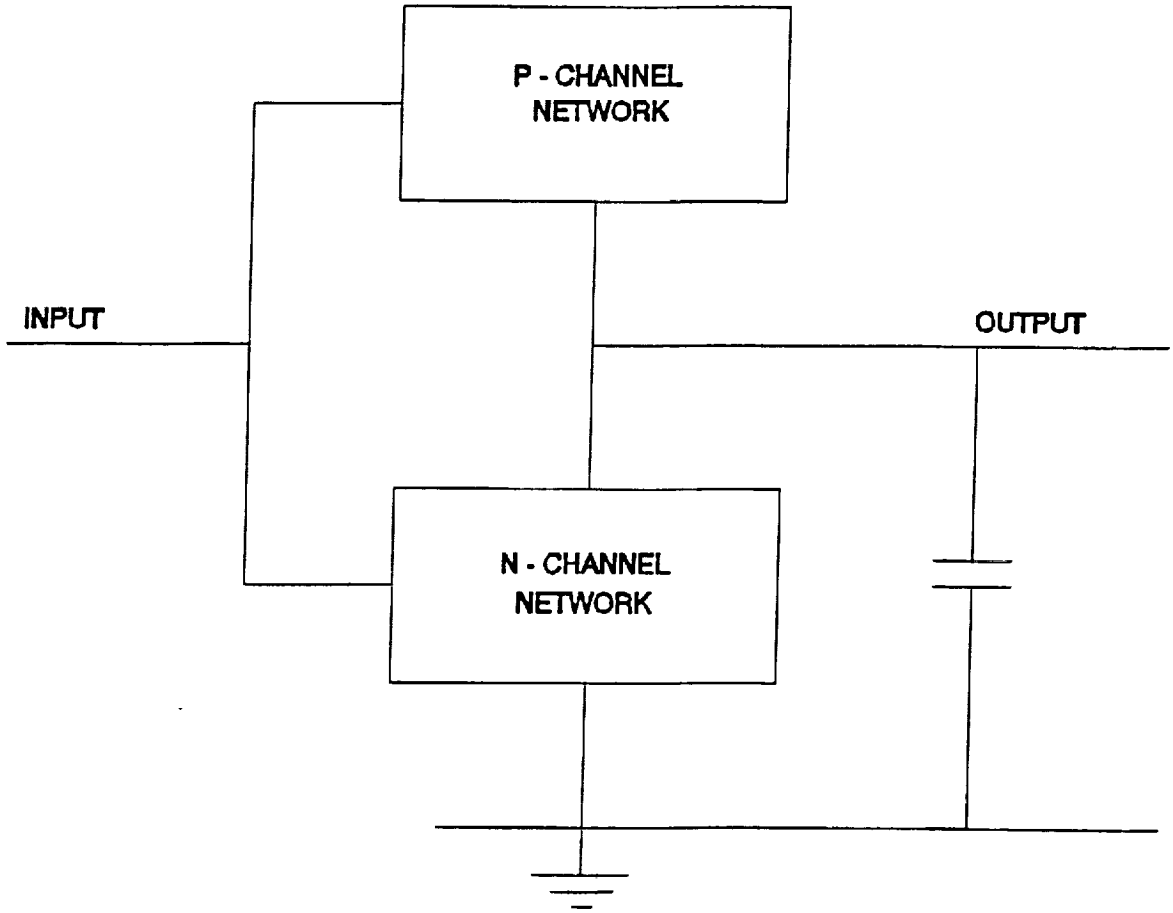


Figure 3.1 Block diagram of a generic CMOS Logic Gate

network represent N-channel and P-channel transistors, either as singles or in series or parallel combinations. CMOS inverters, nand and nor gates, shown in Figure 3.2, can be obtained from the generic network shown in figure 3.1 [3].

Switching time is a measure of the speed of operation of a logic gate. The switching times, considered in this work, are the rise time, fall time and propagation delay. The rise time is defined as the time required for logic gate output to rise to 90% of the maximum possible output, while the fall time is the time taken for the output to fall to 10% of the maximum possible output. The fall and rise time definitions are similar to those used by Taub and Schilling [4]. The propagation delay is the arithmetic mean of the rise time and fall time.

To derive the CMOS inverter fall time, assume that the capacitor is initially charged to the maximum voltage, $V_c = V_{omax}$. When the inverter output falls from high to low, the NMOS transistor conducts. Initially, the transistor will be in saturation. After a time, due to the discharge of the capacitor, the transistor conducts in the non-saturation region. The time the NMOS transistor is in saturation can be shown to be [5]:

$$t_{sat} = \frac{2L_n C_L (V_{omax} - V_{gsn} + V_{tn})}{W_n \mu_n C_{ox} (V_{gsn} - V_{tn})} \qquad (3.1)$$

where

L_n = length of n-channel device.

W_n = width of n-channel device.

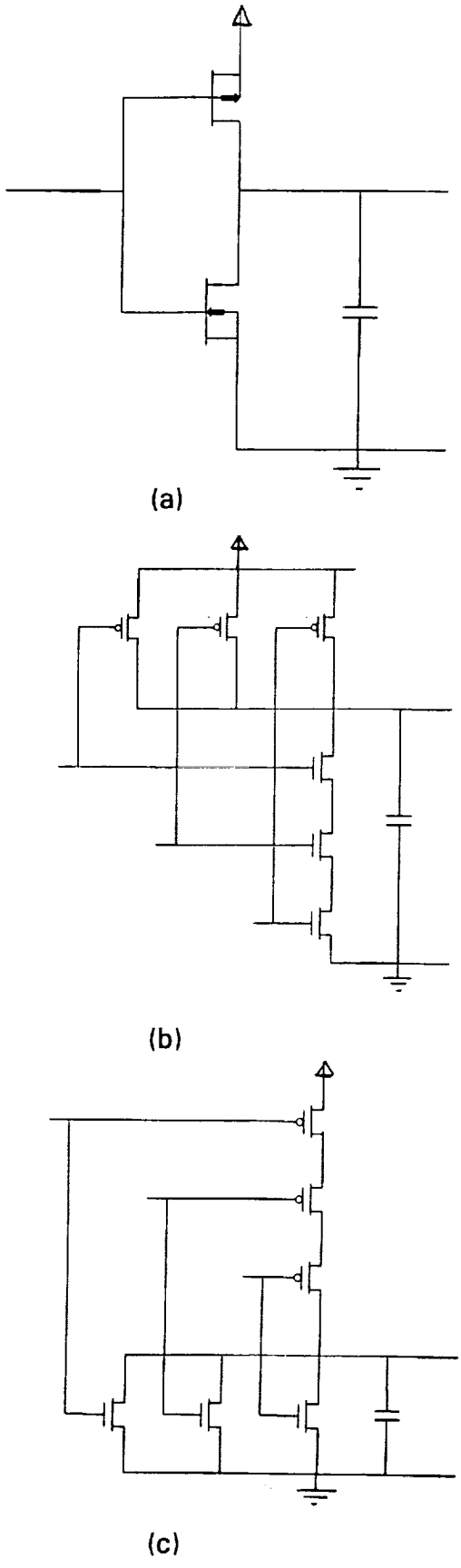


Figure 3.2 CMOS Logic Gates (a) inverter (b) 3-input NAND gate and (c) 3-input NOR gate

V_{gsn} = voltage between gate and source of n-device.

u_n = mobility of n-channel device.

C_{ox} = gate oxide capacitance.

The symbols in the equation (3.1) are similar to those in the literature [3]. The time the transistor is in non-saturation region is given as:

$$t_{nonsat} = \frac{-0.5 C_L K_n^{-1}}{(V_{gsn} - V_{tn})} \left[\ln \frac{0.1(2(V_{gsn} - V_{tn}) - V_{omax})}{(2(V_{gsn} - V_{tn}) - 0.1 V_{omax})} \right] \qquad (3.2)$$

where:

$$K_n = \frac{\mu_n C_{ox} W_n}{L_n} \qquad (3.3)$$

The fall time is the sum of t_{sat} and t_{nonsat}. Adding equations (3.1) and (3.2), the fall time becomes:

$$t_f = \frac{(V_{omax} - (1 + 0.5 \ln Y)(V_{gsn} - V_{tn}))}{0.5 C_L^{-1} K_n (V_{gsn} - V_{tn})^2} \qquad (3.4)$$

where

$$Y = \frac{0.1(2(V_{gsn} - V_{tn}) - V_{omax})}{2(V_{gsn} - V_{tn}) - 0.1 V_{omax}} \qquad (3.5)$$

Equation (3.1) is similar to that given in the literature [3, 4]. However, the expression for t_{nonsat} given in Equation (3.2) is different from that obtained by Taub and Schilling [4]. The latter obtained the following expression for t_{nonsat}:

$$t_{nonsat} = \frac{-C_L \ln[0.1]}{K_n (V_{gsn} - V_{tn})^2} \qquad (3.6)$$

It was assumed by Taub and Schilling that:

$$\frac{(V_{gsn} - V_{tn}) - V_{omax}}{(V_{gsn} - V_{tn}) - 0.1 V_{omax}} \approx 1.0 \qquad (3.7)$$

which is incorrect.

To derive the rise time equation, we assume that the load capacitance is originally discharged. The PMOS is then in the saturation region, and as the output voltage increases, the device enters into the non-saturation region. The time taken for the PMOS device to be in the saturation region is given as:

$$t_{sat} = \frac{2C_L (V_{omax} - (V_{sgp} - |V_{tp}|)}{K_p (V_{sgp} - |V_{tp}|)^2} \qquad (3.8)$$

where:

L_p = length of p-channel device.

W_p = width of p-channel device.

u_p = mobility of PMOS device.

V_{sgp} = voltage between the source and gate of p-channel device.

and

$$K_p = \frac{\mu_p C_{ox} W_p}{L_p} \qquad (3.9)$$

The time the PMOS is in the non-saturation region is given as:

$$t_{nonsat} = \frac{C_L \ln X}{K_p (V_{sgp} - |V_{tp}|)} \qquad (3.10)$$

The rise time is obtained by adding the equations (3.8) and (3.10):

$$t_r = \frac{C_L (V_{omax} - (1 - 0.5 \ln X)(V_{sgp} - |V_{tp}|))}{K_p (V_{sgp} - |V_{tp}|)^2} \qquad (3.11)$$

where

$$X = \frac{2.1 (V_{sgp} - |V_{tp}|) V_{omax} - 2 (V_{sgp} - |V_{tp}|)^2 - 0.1 V_{omax}^2}{0.1 V_{omax} (3 (V_{sgp} - |V_{tp}|) - V_{omax})} \qquad (3.12)$$

The propagation delay, t_{pd}, is the average of the rise time and fall time:

$$t_{pd} = \frac{(t_f + t_r)}{2} \qquad (3.13)$$

To obtain the switching times of the NAND and NOR gates, it should be noted that for the NAND or NOR gates, P-channel and N-channel networks contain transistors which are either in series or in parallel. If the transistors are in series, the switching time is approximately the sum of the switching time of the individual

transistors [6]. However, if the transistors are connected in parallel, then the switching time will be reduced if all the transistors are conducting [6]. Equations (3.3) and (3.9) can be modified to obtain the switching times of NAND and NOR gates.

For CMOS NAND gate, the P-channel network, of Figure 3.2, has P-Channel transistors connected in parallel, while the N-channel network will be replace by series connected N-channel transistors. For the NAND gate, the output become low only when all the series N-channel transistor conduct. Assumung each N-channel transistor has a fall time t_{fi}, the fall time of the NAND gate is approximately equal to the sum of the individual N-channel conduction time [6]. Thus

$$t_{fNAND} \approx \sum_{i=1}^{n} t_{fi} \qquad (3.14)$$

where:

n = number of input to the NAND gate.

If the NMOS transistors are identical, then the fall time for an n-input CMOS NAND gate is:

$$t_{fNAND} \approx n\ t_{fi} \qquad (3.15)$$

the fall-time t_{fi} can be approximately be given by the fall time expression of equation. (3.4)

For n-input CMOS NAND gate, the output will be high, when one or more of n-parallel connected CMOS devices conduct. The more the number of conducting P-

channel transistors, the less the rise time, due to the reduced resistance of the parallel-connected P-channel transistors. Assuming that the time taken by a single P-channel transistor to change the output to high is t_{fi}. For an n-input CMOS NAND gate, the time taken by b simultaneously conducting P-channel transistors depends on the effective parallel resistance of the conducting P-channel transistors. If the transistors have identical parameters, then the rise time for CMOS NAND gate [6] is given as:

$$t_{rNAND} = \frac{t_{ri}}{b} \qquad (3.16)$$

where:

$$1 \leq b \leq n$$

The minimum rise time is obtained when all the P-channel transistors conduct at the same time (i.e. b = n), while the maximum rise time isobtained when a single P-channel transistor conducts (i.e. b = 1). Normally, it is good to state one rise time for for the NAND gate. The worst case rise time is the maximum rise time. This occurs for b = 1. Thus, the rise time of CMOS NAND gate can be expressed by equation (3.11).

In this work, Equations (3.4) and (3.15) were used to obtain the fall time of three input NAND gate. The n in Equation (3.15) was set to 1. Equations (3.11) and (3.16) were used to obtain the rise time of the three input NAND gate. The b of Equation (3.16) was set to unity.

The CMOS NOR gate can be reconstructed from Figure 3.1 by replacing the N-

channel network by a parallel connected NMOS transistors, and replacing the P-channel network by a series connected PMOS transistors. For an N-input, NOR gate of N-channel transistors of same dimensions, the fall time is given as:

$$t_{fNOR} = \frac{t_{fi}}{b} \qquad (3.17)$$

where:

$$1 \leq b \leq n$$

and

b is the number of conducting transistors

Once again, the worst case fall time is obtained when a single N-channel transistor conducts (i.e. b = 1). Thus, equation (3.4) can be used as the worst case fall time for NOR gates.

For the CMOS NOR gate, the output will be high, provided all the series-connected transistors are conducting. If the conduction time for each transistor is t_{ri}, for an n-input CMOS NOR gate, the rise time is approximately given as the sum of the individual P-channel transistors [6]. Assuming that, all P-channel transistors have the same dimensions, then

$$t_{rNOR} \approx n\ t_{ri} \qquad (3.18)$$

In this work, Equations (3.4) and (3.17) were used to obtain the fall time of

three input NOR gate. The b in Equation (3.17) was set to unity. Equations (3.11) and (3.18) were used to obtain the rise time of three input NOR gate. The n in Equation of (3.18) was set to be 3.

3.3 C-PROGRAM CALCULATIONS AND RESULTS

To investigate the effect of TID on CMOS inverters, NAND and NOR gates, the switching time equations were employed. C programs were written to calculate the fall time, rise time and propagation delays of the logic gates. For different values of TID radiation, the corresponding values of threshold voltages and mobilities for the P-channel and N-channel transistors were obtained from available data [1,2]. This is shown in Table 3.1.

The mobility and the threshold voltage at various TID radiation were used to compute the rise and fall times of the CMOS gates. The minimum dimensions for the PMOS and NMOS devices are:

t_{ox} = 500 Angstrom,

C_{ox} = 8.0E-04 pF/um^2

$L_n = L_p$ = 2 um;

$W_n = W_p$ = 5 um;

C_L = 0.72 pF

Table 3.1

Total ionizing dose (in rads) versus mobility and threshold voltage (in volts) and calculated KP_n, and KP_p.

Dose	V_{tn}	V_{tp}	μ_n	μ_p	KP_n	KP_p
1.e4	1.42	-1.04	408	200	3.20e-4	1.60e-4
4.e4	1.37	-1.08	401	199	3.14e-4	1.59e-4
7.e4	1.24	-1.13	397	194	3.11e-4	1.55e-4
1.e5	1.19	-1.19	394	188	3.09e-4	1.50e-4
2.e5	1.02	-1.22	384	180	3.01e-4	1.44e-4
3.e5	0.92	-1.28	380	176	2.98e-4	1.41e-4
4.e5	0.82	-1.30	368	172	2.89e-4	1.38e-4
6.e5	0.68	-1.36	360	164	2.82e-4	1.31e-4
7.e5	0.60	-1.38	356	162	2.79e-4	1.30e-4
9.e5	0.49	-1.40	353	158	2.77e-4	1.20e-4

Note: The above data do not include rebound effects

Equations (3.3) and (3.9) were used to obtain the fall and rise times of CMOS inverter. Modified versions of the above mentioned equations, discussed in the previous section, were used to calculate the switching times of 3-input CMOS NAND and NOR gates.

Figures 3.3, 3.4 and 3.5 show the switching times for inverter, 3-input NAND and 3-input NOR gates, respectively. It can be seen from the figure that, the rise time increases with TID while the fall time decreases with TID.

The widths of the P-channel transistors were changed to obtain the effects of transistor sizing on the switching time. Figures 3.6, 3.7, and 3.8 show the propagation delay versus TID for inverter, 3-input NAND gate, and 3-input NOR gate, respectively. It is interesting to note that, by increasing the size of the P-channel transistor with respect to that of the N-channel transistor, the propagation delay of CMOS logic gates can be made to decrease. Furthermore, from figures 3.3 and 3.4, it can be seen that the propagation delay decreases with an increase in TID for INVERTERS and NAND gates. However, from figure 3.5, there is a slight increase in propagation delay with respect to TID for NOR gates.

3.4 PSPICE SIMULATIONS AND RESULTS

PSPICE is one version of SPICE, which is a standard program for simulation of integrated circuits. PSPICE has built in models of semiconductor devices, passive components, controlled sources and signal generators. In this work, the signal generator will be used to generate the input signal, V_m. The generated input signal has a peak voltage of 4V, a pulse width of 5 μsec, and rise time and fall time of about 0.001 nsec.

3.4.1 EFFECT OF TID ON SWITCHING TIMES OF INVERTERS

SPICE level 3 model was used to obtain more accuracy. In level 3 model, and

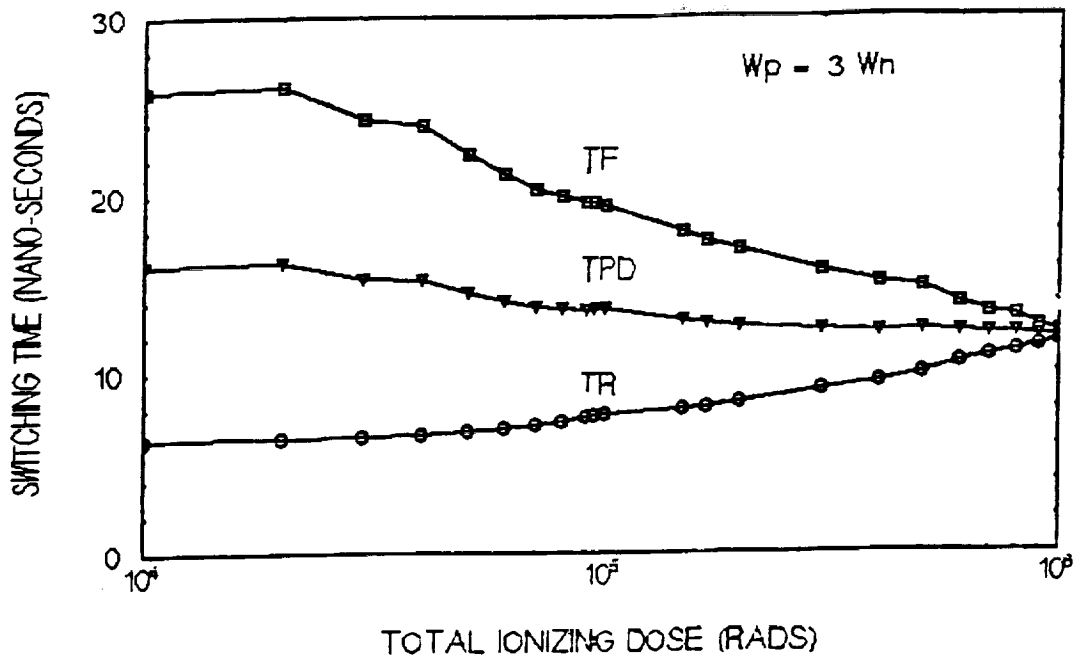


Figure 3.3 Rise time (TR), Fall time (TF) and Propagation delay (TPD) of an inverter

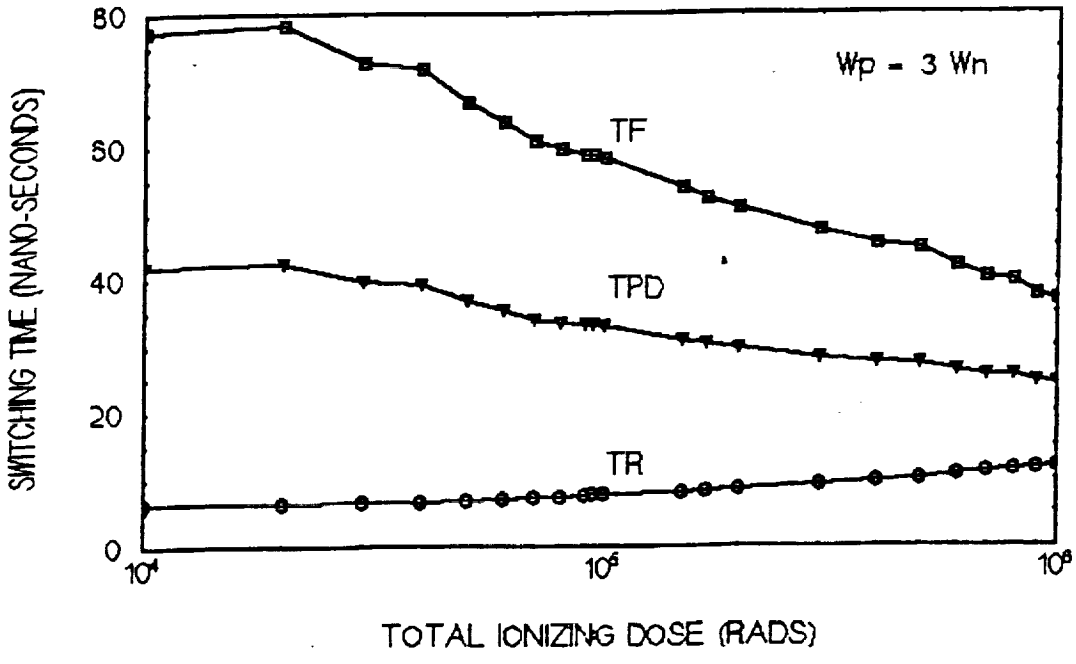


Figure 3.4 Rise time (TR), Fall time (TF) and Propagation delay (TPD) of 3-input NAND gate

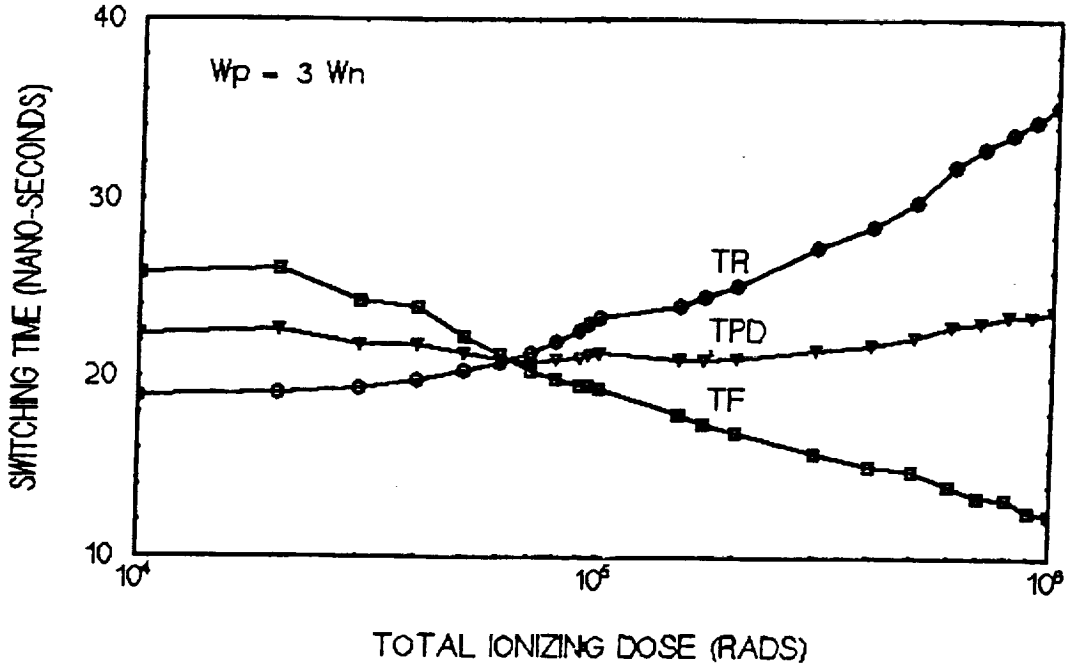


Figure 3.5 Rise time (TR), Fall time (TF) and Propagation delay (TPD) of 3-input NOR gate

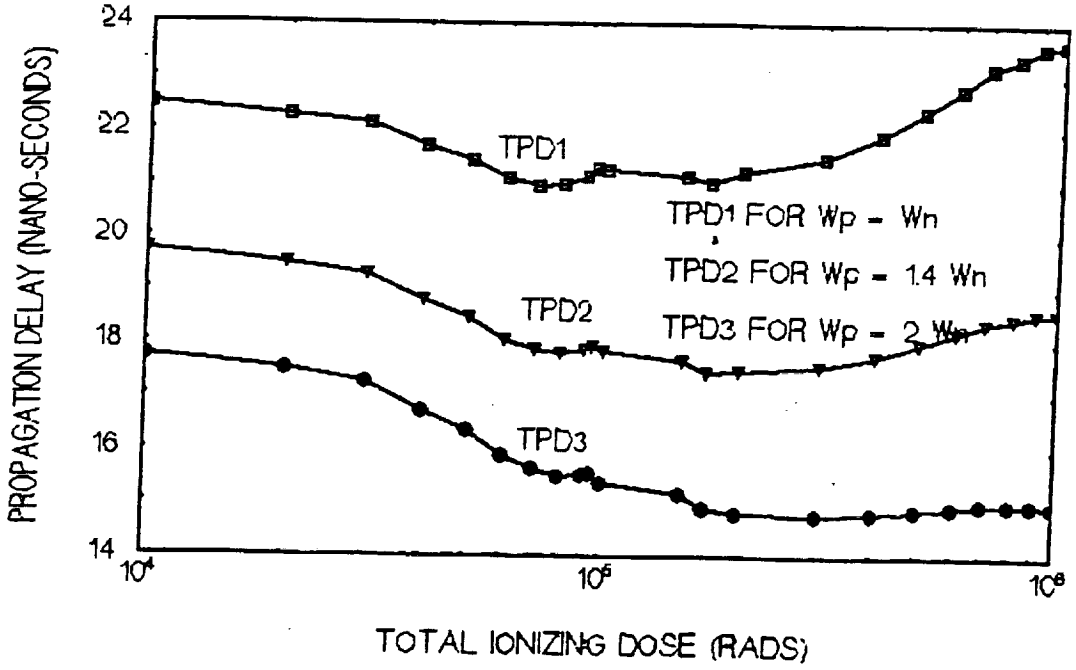


Figure 3.6 Propagation delay versus TID of inverter with various transistor sizes

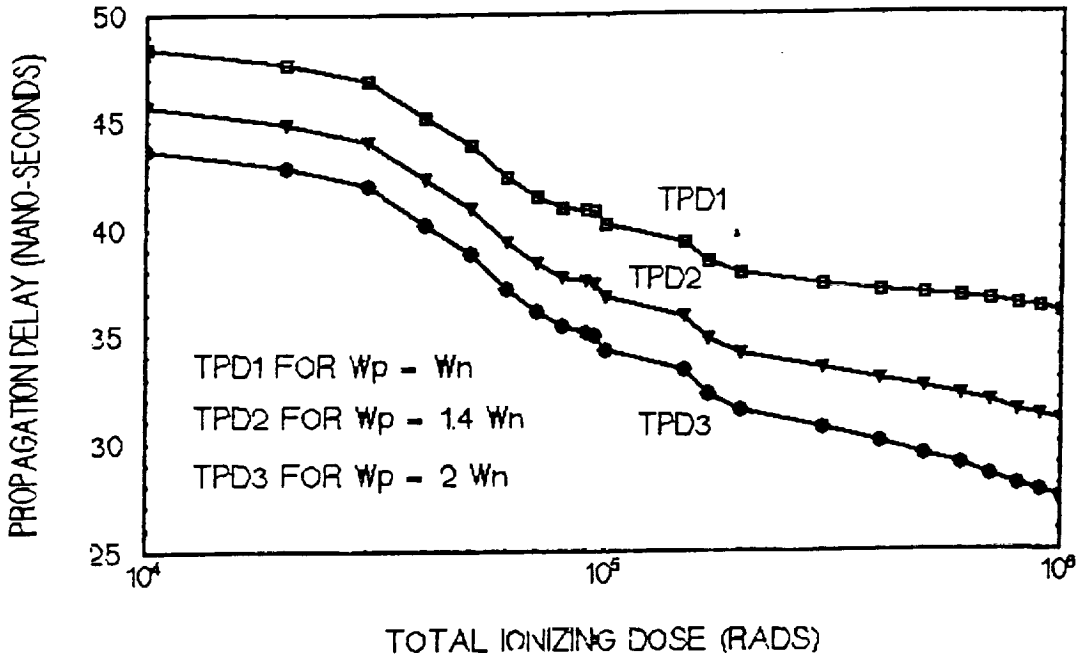


Figure 3.7 Propagation delay versus TID of 3-input NAND gates with various transistor sizes

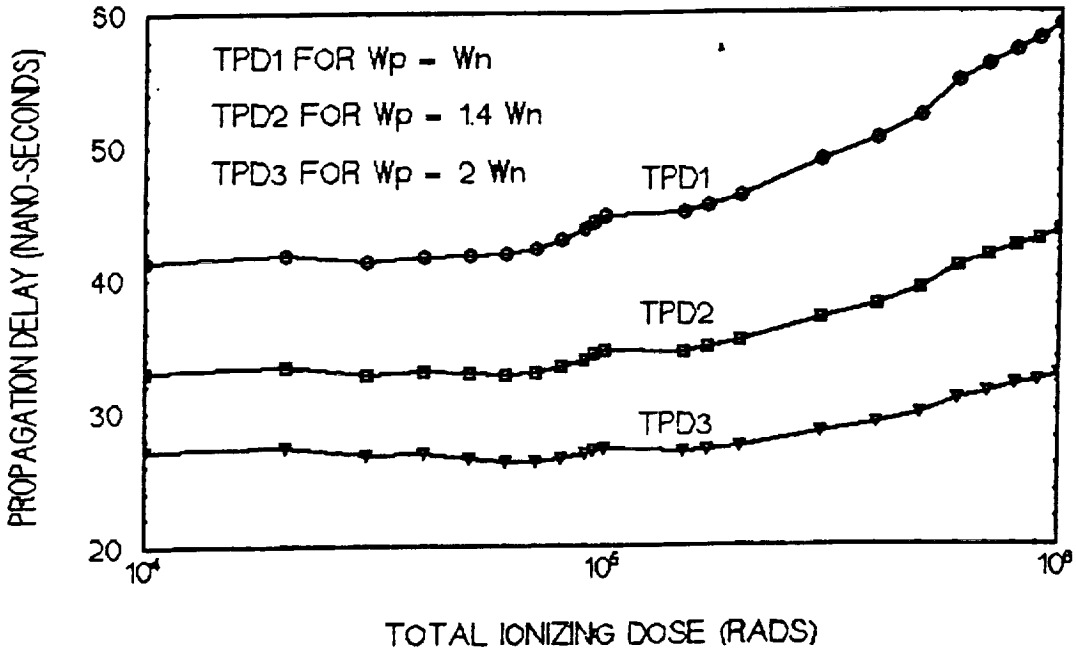


Figure 3.8 Propagation delay versus TID of 3-input NOR gates with various trnsistor sizes

additional transistor parameters are added, such as gate capacitances, THETA and KAPPA; details of which are available in the literature [6]. The effect of total ionizing dose radiation on switching time can be simulated through the threshold voltage VTO and KP parameter. The KP parameter is related to mobility as KP = μC_{ox} [6]. The values of total ionizing dose versus mobility and threshold voltage used for PSPICE simulation are shown in Table 3.1.

The width of P-channel with respect to that of N-channel was varied in turn to obtain the effect of total ionizing dose on switching time of CMOS inverter. The rise time and fall time were obtained from PSPICE .PROBE data, while the propagation delay was calculated by averaging the rise time and fall time.

Figure 3.9 shows the effect of total ionizing dose on fall time of CMOS inverter. As seen in figure 3.9, the fall time decreases with increase in total ionizing dose. The curves for TF1 ($W_p = W_n$), TF2 ($W_p = 2W_n$) and TF3 ($W_p = 3W_n$) are almost the same. This is expected since the fall time is not dependent on the width of the P-channel transistor.

The effects of total ionizing dose on the rise time of CMOS inverter is shown in figure 3.10. It can be seen from the latter figure, that the rise time increases with increase in total ionizing dose. Also, the rise time decreases as the P-channel width increases. The propagation delay is the average of rise time and fall time. The propagation delay for different total ionizing dose of the inverter is shown in figure 3.11.

Equation (3.4) shows the dependency of the fall time on mobility and threshold voltage of the N-channel transistor. Since both the mobility and threshold voltage of

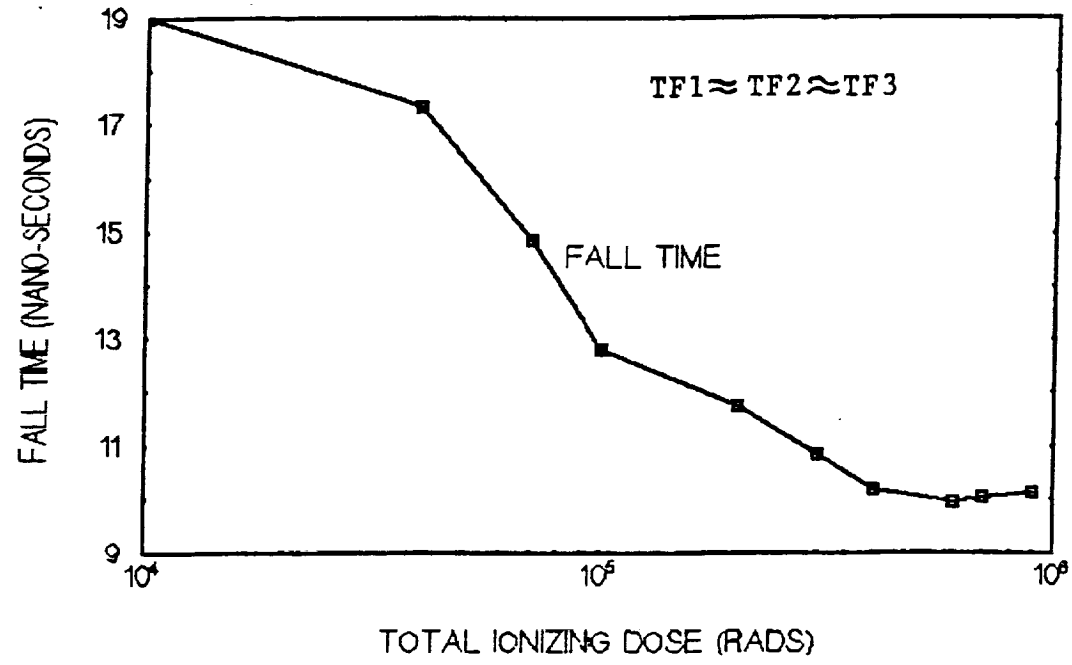


Figure 3.9 Fall Time versus TID for CMOS inverter (PSPICE RESULTS)

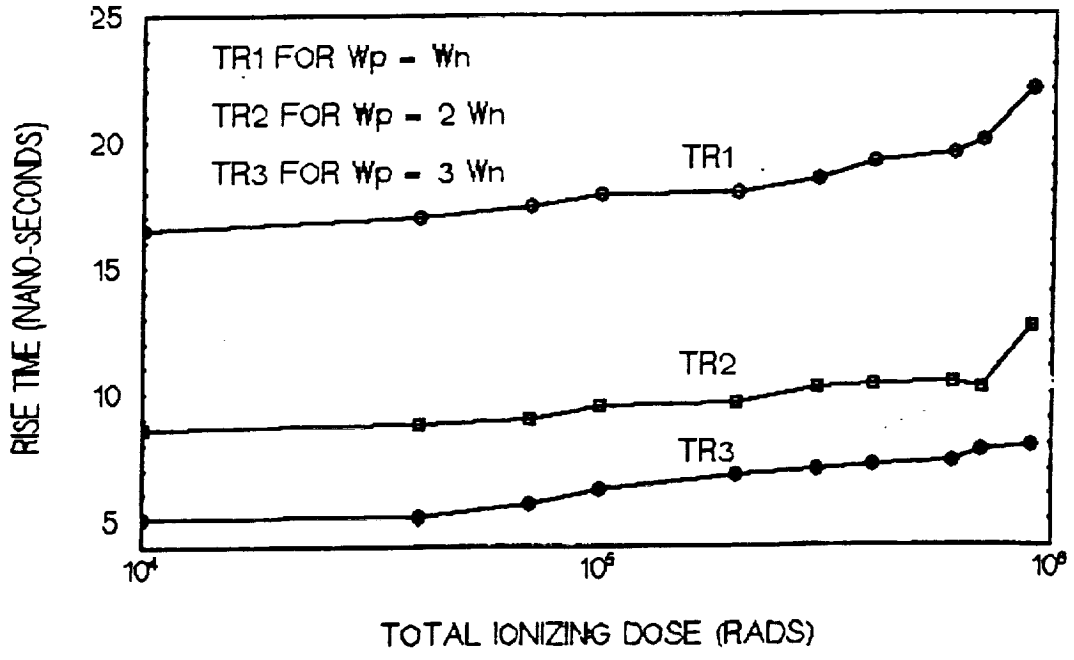


Figure 3.10 Rise Time versus TID for CMOS inverter (PSPICE RESULTS)

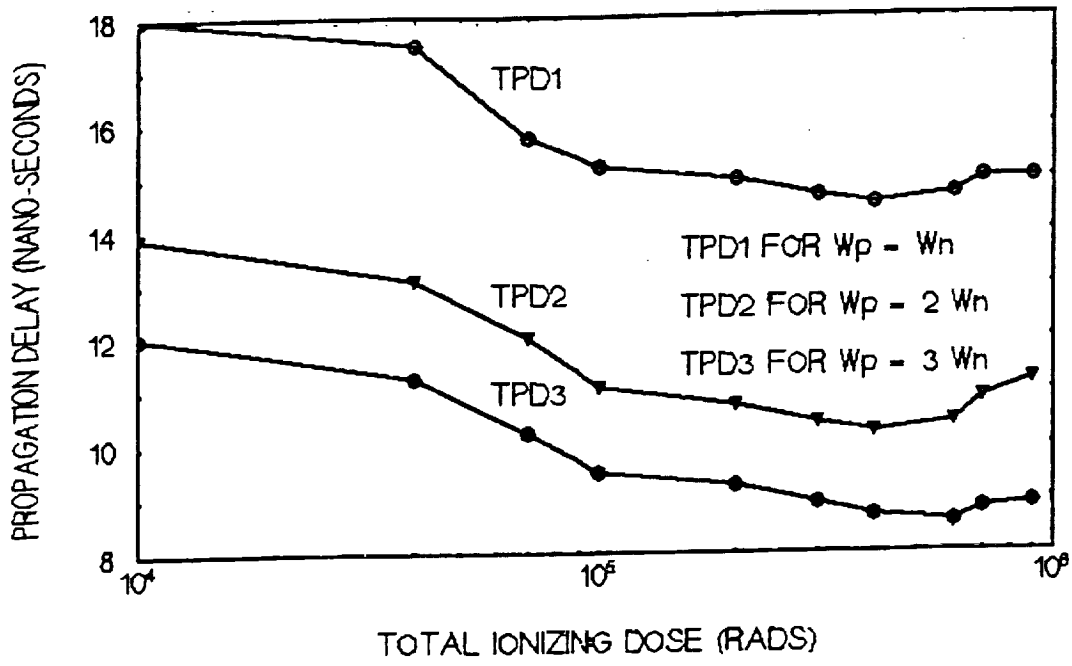


Figure 3.11 Propagation delay versus TID for CMOS inverter (PSPICE RESULTS)

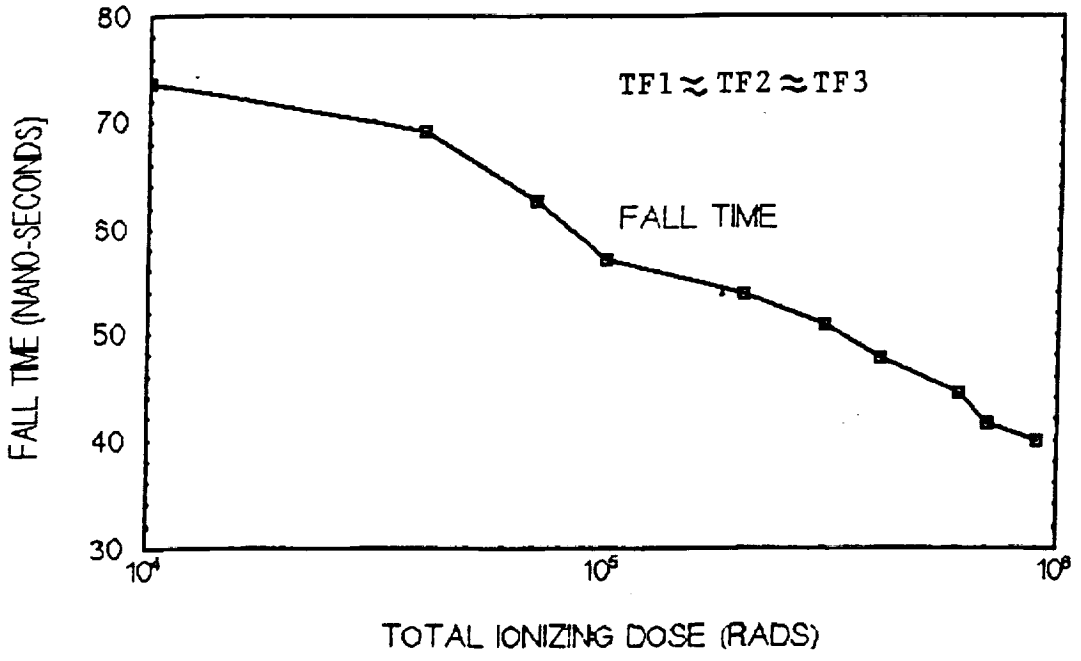


Figure 3.12 Fall Time versus TID for CMOS 3-input NAND gate (PSPICE RESULTS)

N-channel transistor decrease due to total ionizing dose, the fall time will depend on some canceling effects between the mobility and the threshold voltage. However, both the PSPICE and C program results indicate a decrease in fall time as the total ionizing dose increases. This observation suggests that the total ionizing dose effect on the fall time of CMOS inverter is dominated by the decrease in the threshold voltage as the total ionizing dose increases. This observation agrees with that reported by Kerns and Shafer [8] who reported that, for on N-channel MOSFET, the effect of total ionizing dose on the threshold voltage is more pronounced than the effect due to the corresponding mobility degradation.

Equation (3.11) shows the dependency of the rise time on mobility and threshold voltage. The increase of absolute value of threshold voltage, and the decrease in mobility of P-channel, with total ionizing dose, have resulted in increased rise time. A similar observation was reported by Hatano and Shibuya [7]. The latter related the increase in switching speed of digital circuits, with the change in the DC parameters of MOSFETS due to the effect of total ionizing dose radiation.

3.4.2 EFFECT OF TID ON SWITCHING TIME OF 3-INPUT CMOS NAND GATE.

Using Table 3.1, the effects of total ionizing dose was simulated through the variation of threshold voltage and KP (mobility) parameter. As discussed earlier, the KP parameter is related to mobility by the expression: $KP = \mu C_{ox}$ [6]. The output in the time domain in response to the input signal was determined by using the transient response of CMOS NAND gate. The transient response was obtained by the .TRAN command of SPICE. The results of the transient analysis was obtained using the

.PROBE command. The values of design parameters are the same as those used in C program calculation. The PSPICE results of the effects of total ionizing dose on the switching times of CMOS NAND gate follow:

The effects of total ionizing dose radiation on the fall time of 3-input CMOS NAND gate is shown in figure 3.12. From the latter, it can be seen that the fall time decreases with increase of total ionizing dose radiation. The maximum rise time is obtained when a signal P-channel transistor conducts, and the minimum rise time occurs when all P-channel transistors conducts. Figure 3.13 shows the maximum rise time (one P-channel transistor is on) for various transistor sizes. The latter figure shows that the rise time increases with an increase in total ionizing dose radiation. In addition, figure 3.13 shows a decrease of rise time with an increase of P-channel width with respect to N-channel width.

The maximum propagation delay (one P-channel transistor on) was drawn for various transistor sizes. This is shown in figure 3.14. As seen in figure 3.14, the propagation delay decreases with increase in total ionizing dose.

The PSPICE simulation and C program results agree on the increase in rise time with total ionizing dose. Also, the fall time and propagation delay decrease with total ionizing dose. The PSPICE results shows bigger values. The higher PSPICE results may be due to additional transistor parameters (such as gate capacitances and resistance) when MOSFET device level 3 model is used.

3.4.3 EFFECTS OF TID ON SWITCHING TIMES OF CMOS NOR GATE.

PSPICE program for CMOS NOR gate was written. The transient response was

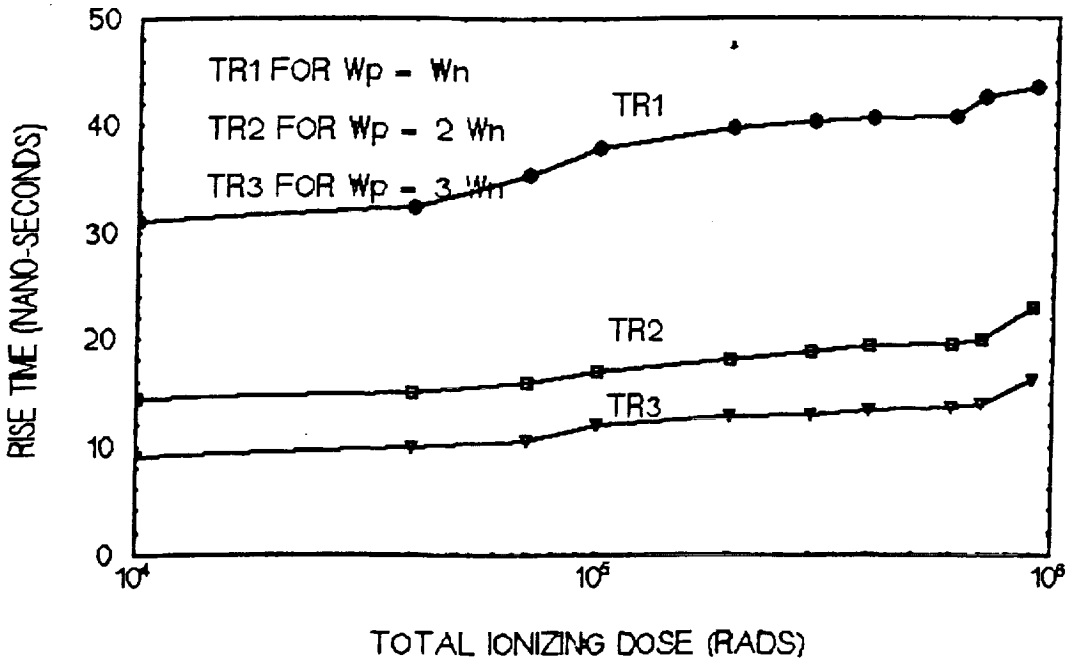


Figure 3.13 Rise Time versus TID for CMOS 3-1nput NAND gate (PSPICE RESULTS)

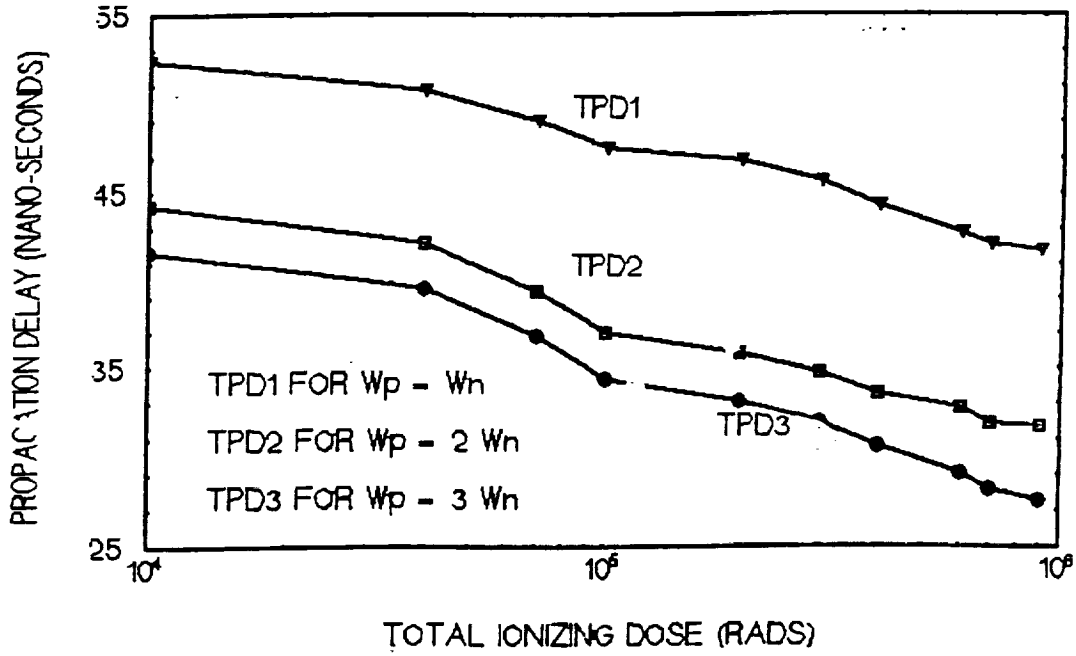


Figure 3.14 Propagation delay versus TID for CMOS 3-input NAND gate (PSPICE RESULTS)

performed by the .TRAN command. The results of the transient analysis was obtained using the .PROBE command. The effects of total ionizing dose radiation were simulated through the threshold voltage and KP parameter. The KP parameter is related to the mobility by the expression: $KP = \mu C_{ox}$ [6]. The PSPICE simulation results of the effect of total ionizing dose on 3-input CMOS NOR gate follows:

The effects of total ionizing dose radiation on the fall time of 3-input CMOS NOR gate is shown in figure 3.15. As seen from the figure, the fall time decreases with an increase in total ionizing dose radiation. The effects of total ionizing dose on the rise time of 3-input CMOS NOR gate is shown in figure 3.16. As seen from the latter figure, the rise time for CMOS NOR gate increases with total ionizing dose radiation. Also, the rise time decreases with an increase in the width of P-channel transistor with respect to that of N-channel transistor.

The propagation delay is the average of rise time and fall time, as indicated by Equation (3.13). Figure 3.17 shows the propagation delay versus TID for NOR gate. The figure was obtained for the conduction of one N-channel transistor (this implies maximum fall time). As can be seen from figure 3.17, the propagation delay of CMOS NOR gate increases with total ionizing dose. The propagation delay follows the rise time, due to the series connection of P-channel transistors. In addition, from figure 3.17, the propagation delay decreases with an increase in the width of P-channel compared with that of N-channel transistor.

The effect of increased P-channel width with respect to that of N-channel transistor was simulated using PSPICE. This is shown in figure 3.18. It can be seen from the figure that the increase in P-channel width reduces the rise time and

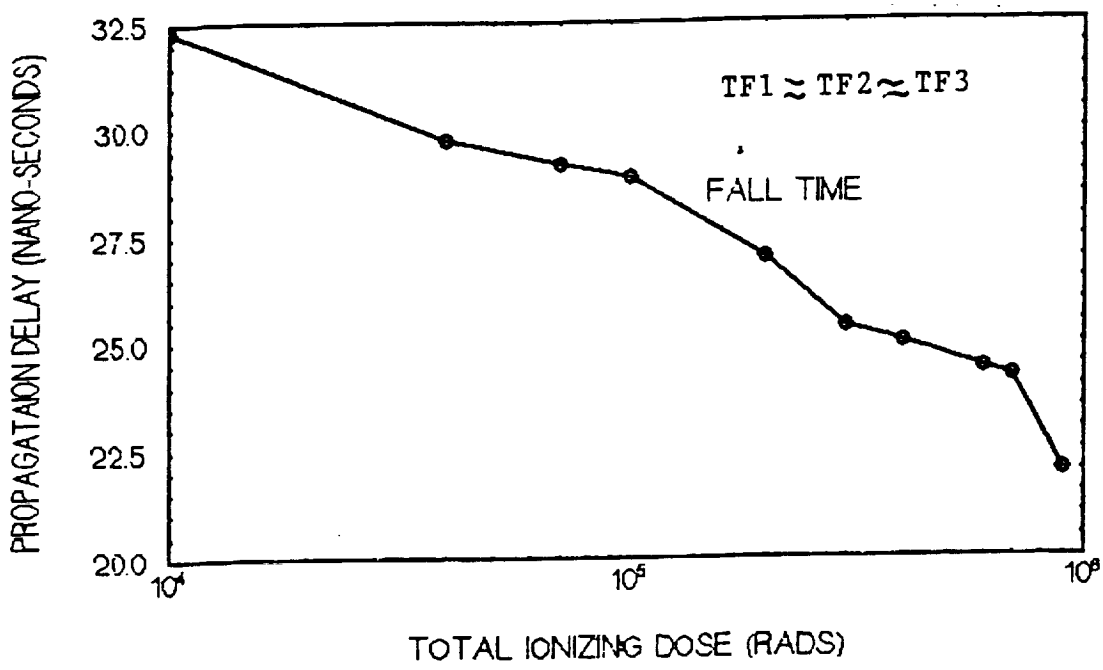


Figure 3.15 Fall time versus TID for CMOS 3-input NOR gate (PSPICE RESULTS)

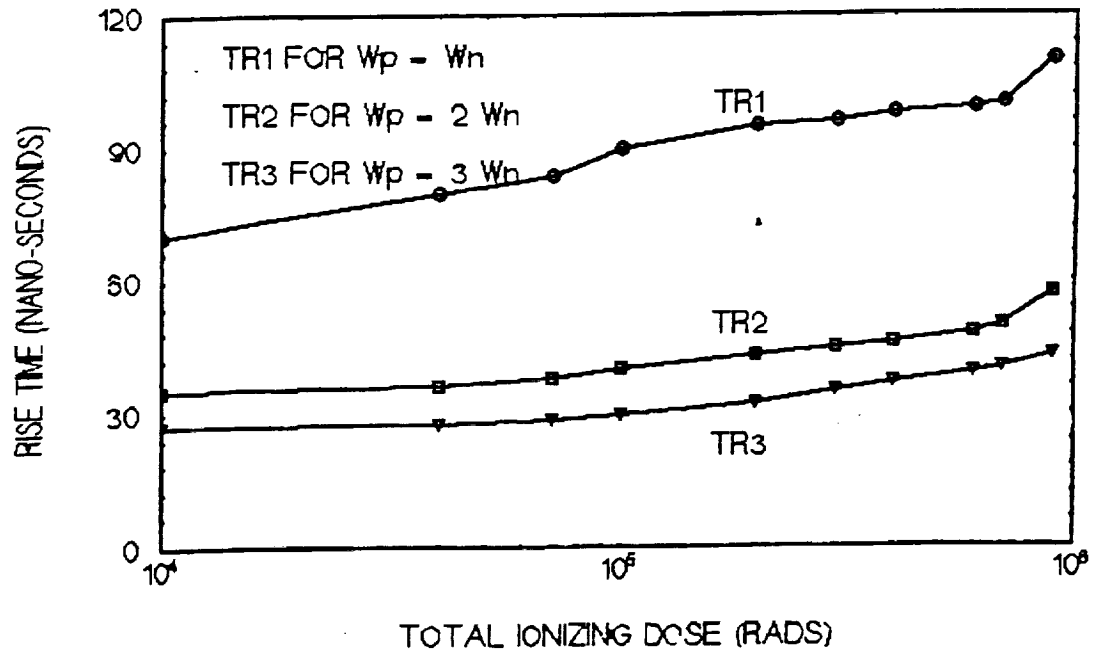


Figure 3.16 Rise Time versus TID for CMOS 3-input NOR gate (PSPICE RESULTS)

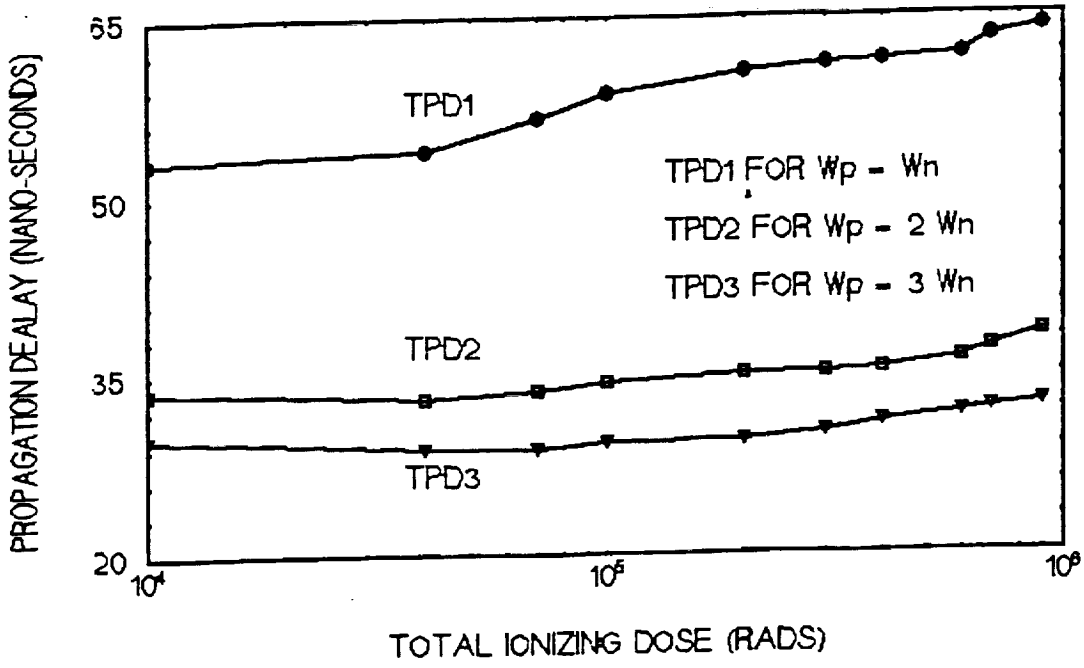


Figure 3.17 Propagation delay versus TID for CMOS 3-input NOR gate (PSPICE RESULTS)

propagation delay. As a sacrifice for using large channel width, the propagation delay can be made to decrease with an increase in total ionizing dose. Hence, the larger the transistors, the greater the radiation tolerance. This observation agrees with Kern and Shafer [8] who proposed that, the performance of CMOS electronic circuits in radiation environment can be improved by increasing the ratio of the device (P- and N- MOSFETS).

3.5 CONCLUSIONS.

The total ionizing dose effect on switching time of CMOS logic gates (INVERTER, NAND and NOR), was obtained by considering the effects to total ionizing dose radiation on the MOSFET mobility and threshold voltage. The switching time equations were derived and then used in C programs. Also, the PSPICE simulations were performed. A comparison was made of the results obtained using C and PSPICE programs.

The fall and rise time equations of CMOS INVERTER were derived. The derived equations were compared with that given by Taub and Schilling [4]. The switching time results obtained from the derived equations are very close to those obtained by Taub and Schilling [4].

The results of the effects of total ionizing dose showed that, the rise time of CMOS inverter increases with increase in total ionizing dose. The increase may be due to an increase in absolute value of the threshold voltage and a decrease in mobility of P-channel transistor with total ionizing dose radiation. The fall time of CMOS inverter decreased with an increase in total ionizing dose. The decrease may

be due to a decrease of N-channel threshold voltage with total ionizing dose. With the width of the P-channel being three times that of the N-channel, the propagation delay was found to be almost independent to of the total ionizing dose. The values of switching time obtained using PSPICE simulations were similar to those obtained using C programs.

The results on the effects of total ionizing dose on the switching time of 3-input CMOS NAND gate indicated that, the rise time increases, while the fall time and propagation delay decrease with increase in total ionizing dose radiation. The values of switching times obtained using PSPICE for simulation and C program were very close.

The effects of total ionizing dose radiation on the switching times of 3-input CMOS NOR gate indicated that, the fall time decreases while the rise time and propagation delay increase with an increase in total ionizing dose radiation. The values of switching time obtained when the derived equations for fall time and rise time were used in C program calculations, are close to those obtained from PSPICE simulations.

From the results of the effects of total ionizing dose on the switching times of the basic CMOS logic gates (the INVERTER, NAND and NOR gates), it can be concluded that:

(i) The rise time of CMOS logic gate increases with an increase of total ionizing dose radiation.

(ii) The fall time of CMOS logic gate decreases with an increase of total ionizing dose radiation.

(iii) For CMOS logic gates, the values of the rise time can be reduced by increasing the width of the P-channel transistors and the values of the fall time can be reduced by increasing the width of the N-channel transistors.

(iv) The value of the propagation delay of CMOS inverter, CMOS NAND gate and CMOS NOR gate can be reduced by increasing the width of P-channel transistors with respect to that of N-channel transistors (assuming the length of P-channel are the same to that of N-channel).

(V) The decrease of the propagation delay of CMOS NAND gate, and the increase of that of CMOS NOR gate with total ionizing dose radiation suggests an advantage of using NAND gate instead of NOR gate in the radiation environment.

(vi) By using the size of the P-channel transistor equal to three times that of the N-channel transistor (i.e $W_p = 3W_n$), the propagation delay of CMOS inverter, 3-input NAND and NOR gates can be made to decrease with or be independent of the increase in total ionizing dose.

3.6 REFERENCES

[1] Winokur,P.S., Schwank,J.R., WcWhorter,P.J, Dressendorfer P.V. and Turpin,D.C. "Correlating the Radiation Response of MOS Capacitors and Transistors," IEEE Trans. on Nucl. Sci., Vol. NS-31, pp. 1453 - 1460, 1984.

[2] Dressendorfer,P.V, Soden,J.M, Harrington J.J. and Nordstrom, T.V, "The Effects of Test Conditions on MOS Radiation-Hardened results," IEEE Trans. on Nucl. Sci. Vol. NS-28, pp. 4281 - 4287, 1981.

[3] Uyemura,J.P "Circuit Design for CMOS VLSI," Kluwer Academic Publishers, 1992.

[4] Taub, H. and D. Schilling, D, "Digital Integrated Electronics," McGraw Hill, 1977.

[5] Sasabo, M., "Effects of Total Ionizing Dose on Switching Times of CMOS Logic Gates", M.S. Thesis, Prairie View A&M University, Prairie View, Texas, August 1992.

[6] Geiger, R.L., Allen, P.E. and Strader, N.R., "VLSI Design Techniques for Analog and Digital Circuits," McGraw Hill, 1990.

[7] Hatano, H. and Shibuya, H. "Design of CMOS Logic Gate Radiation Tolerance." Electronic Letters, Vol. 19, No. 23, pp. 977 - 978, Nov. 1983.

[8] Kern, S.E. and Schafer, B.D. "Design of Radiation Hardened Integrated Circuits for Space: A Compendium of Approaches", Proc. of IEEE, Vol. 76, No. 11, pp. 1470 - 1487, Nov. 1988.

CHAPTER 4

RADIATION HARDENING OF CMOS SRAM USING SWITCHED CAPACITOR NETWORKS

4.1 INTRODUCTION

Memory elements, such as SRAM, are employed for computing and storage of information. A change of logic state, due to radiation, can cause computational errors and propagation of errors through a system. Upset of the above type can take place when a charge particle, such as cosmic ray, strikes a sensitive part of a memory cell and sufficient charge is generated to cause a change in the logic state of the cell. In the case of CMOS SRAM, a charged particle striking the drain diffusion of either the p-channel or n-channel device can cause cell upset if enough charge is deposited or removed at specific nodes of the cell [1].

One method that is used to harden CMOS SRAM cell against single event upset is the use of feedback resistors [1]. The circuit is shown in Figure 4.1. The feedback resistors tend to increase the time constants of the feedback path between the inverter pairs of the CMOS SRAM cell, and make the cell less susceptible to single event upset. However, the negative temperature coefficient of the feedback polysilicon resistance makes CMOS SRAM cell more susceptible to single event upset at high temperatures. In addition, the polysilicon resistors normally used as a feedback resistance increase the size of hardened SRAM cells. In this chapter, a method is developed for replacing polysilicon feedback resistance of SRAM cell with switched capacitor networks.

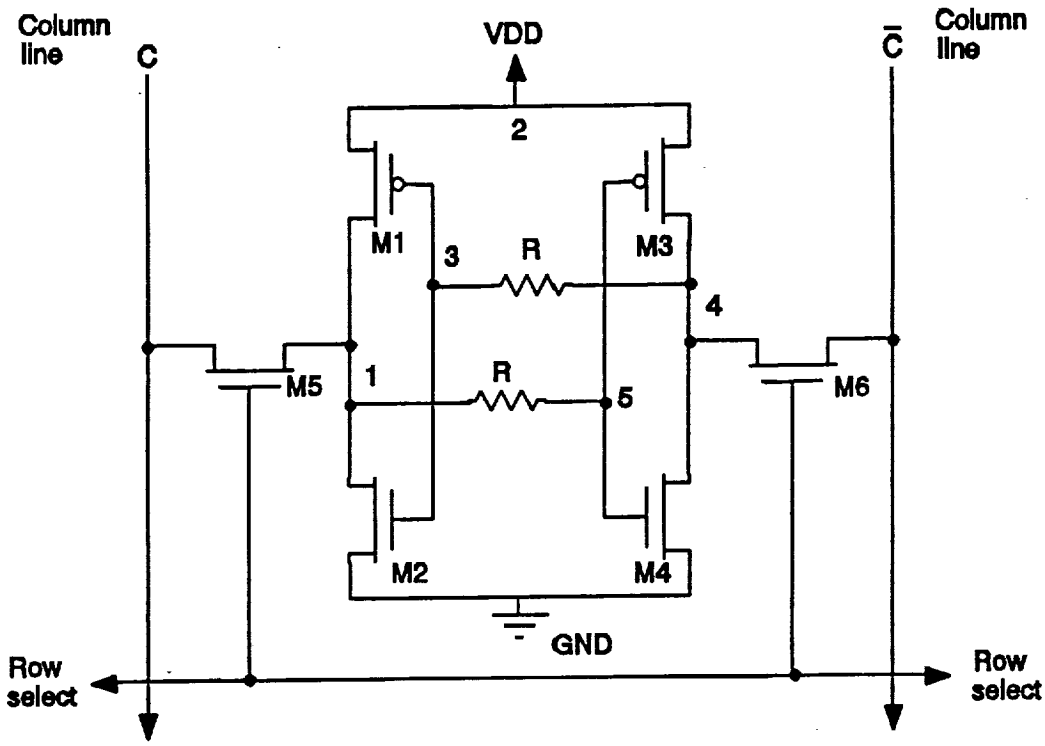


Figure 4.1 CMOS SRAM with Feedback Resistors.

4.2 SWITCHED CAPACITOR NETWORKS

It can be shown that if clock frequency is high enough, a combination of switches and capacitor can replace a resistor that is dependent only on the clock frequency and capacitor [2].

The switched capacitor network, employed in this work, is a single-phase grounded switched capacitor shown in Figure 4.2. It consists of two switches and a capacitor. Assuming that at odd time n, the left and the right switches are closed, and applying the charge equation to the network, the charge equations become:

For odd time n:

$$i_1(n) = CV_1(n) - CV_2(n-1) \qquad (4.1)$$

$$i_2(n) = CV_2(n) - CV_1(n-1) \qquad (4.2)$$

For even time n:

$$i_1(n) = 0 \qquad (4.3)$$

$$i_2(n) = 0 \qquad (4.4)$$

Equations (4.1) to (4.4) can be combined such that the resulting equations are valid for both even and odd times. This is done by using "switching function" [3] to obtain the following equations:

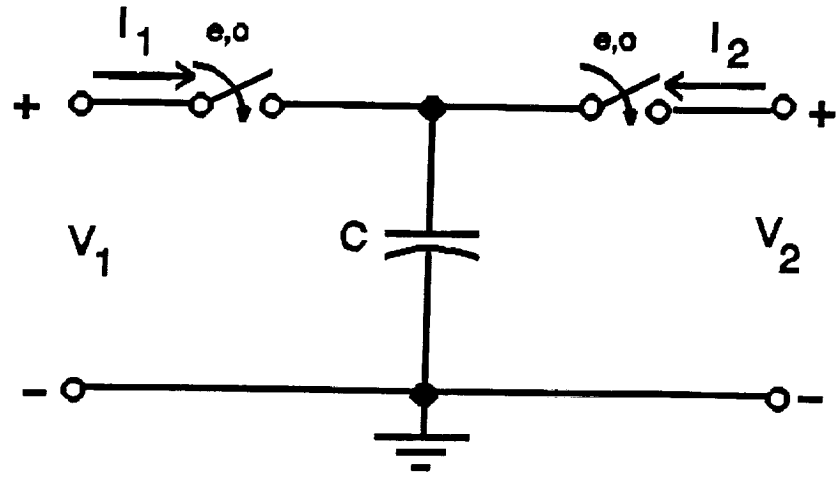


Figure 4.2 Single Phase Grounded Switched Capacitor Network.

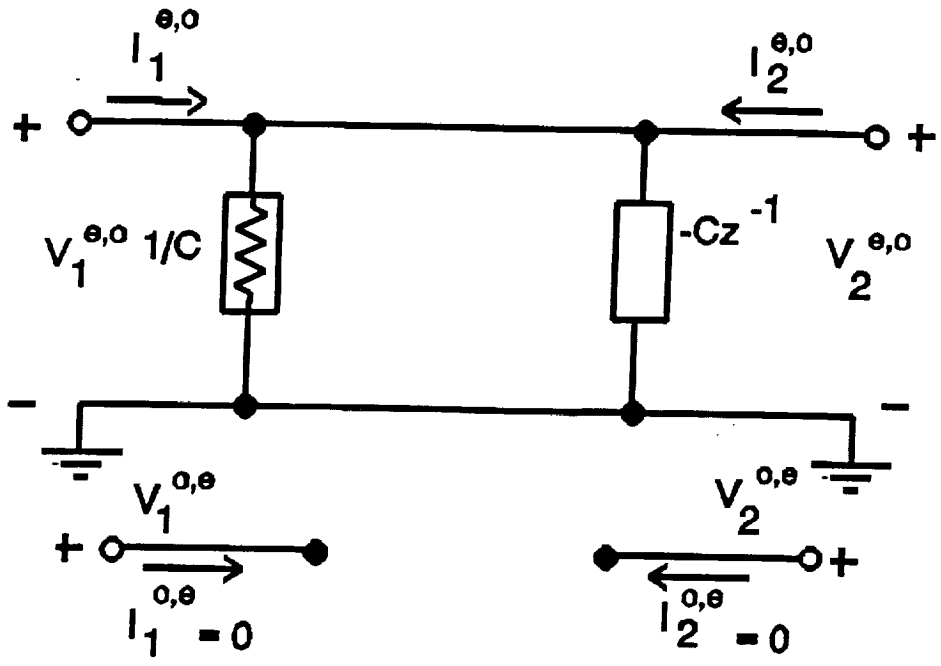


Figure 4.3 Z-domain Equivalent Circuit of Single Phase Grounded Switched Capacitor Network.

$$i_1(n) = A^o(n)\,CV_1(n) - A^o(n-1)\,CV_2(n-1) \qquad (4.5)$$

$$i_2(n) = A^o(n)\,CV_2(n) - A^o(n-1)\,CV_1(n-1) \qquad (4.6)$$

where:

$$A^e(n) = \frac{1+(-1)^n}{2}$$

and

$$A^o(n) = \frac{1-(-1)^n}{2}$$

Equation (4.5) and (4.6) are time-variant equations required to describe Figure 4.2.

For design purposes, it is desirable to describe switched capacitor networks as two-port network in the frequency domain. For the sampled-data system, the link to the frequency domain can be established with the z-Transformation. To obtain z-transform of the nodal charge equations (4.5) and (4.6), some basic z-transforms, listed in Table 4.1 [3], are required. By using formulas (2), (4), (7), (8) and (9) of Table 4.1, equations (4.5) and (4.6) become:

$$I_1^e(z) + I_1^o(z) = CV_1^o(z) - CV_2^o(z)\,z^{-1} \qquad (4.7)$$

$$I_2^e(z) + I_2^o(z) = CV_2^o(z) - CV_1^o(z)\,z^{-1} \qquad (4.8)$$

Equations (4.7) and (4.8) can be rewritten as:

Table 4.1

Some Useful Relations For The Analysis of SC Network

1. $A^{e}(n)f(n) \xrightarrow{z} \frac{F(z)+F(-z)}{2} = F^{e}(z)$

2. $A^{o}(n)f(n) \xrightarrow{z} \frac{F(z)-F(-z)}{2} = F^{o}(z)$

3. $A^{e}(n-1)f(n-1) \xrightarrow{z} z^{-1}F^{e}(z)$

4. $A^{o}(n-1)f(n-1) \xrightarrow{z} z^{-1}F^{o}(z)$

5. $A^{e}(n)f(n-1) = A^{o}(n-1)f(n-1) \xrightarrow{z} z^{-1}F^{o}(z)$

6. $A^{o}(n)f(n-1) = A^{e}(n-1)f(n-1) \xrightarrow{z} z^{-1}F^{e}(z)$

7. $A^{e}(n)+A^{o}(n)=1 \xrightarrow{z} A^{e}(z)+A^{o}(z) = \frac{1}{1-z^{-1}}$

8. $A^{e}(n)f(n)+A^{o}(n)f(n) = f^{e}(n)+f^{o}(n) = f(n)$

9. $f^{e}(n)+f^{o}(n) = f(n) \xrightarrow{z} F^{e}(z)+F^{o}(z) = F(z)$

$$I_1^{e,o}(z) = CV_1^{e,o}(z) - CV_2^{e,o}(z)\,z^{-1} \qquad (4.9)$$

$$I_1^{o,e}(z) = 0 \qquad (4.10)$$

$$I_2^{e,o}(z) = CV_2^{e,o}(z) - CV_1^{e,o}(z)\,z^{-1} \qquad (4.11)$$

$$I_2^{e,o}(z) = 0 \qquad (4.12)$$

Note that the elements in equations (4.7) and (4.8) consist of terms C which correspond to resistance, $R_{eq} = 1/C$ and Cz^{-1} which correspond to a resistors with delay (or storage) properties. The equivalent circuit of equations (4.7) and (4.8) is shown in Figure 4.3, and this z-domain equivalent circuit contains voltage sources, capacitor, resistor and storage element (storistor refers to a one-port storage element in which the current through it is proportional to a delayed version of the voltage across it [4]).

To implement the storistor on a general purpose circuit simulation program, the program has to allow time-delay elements. SPICE has such an element in a lossless transmission line, properly terminated by its characteristic impedance. The lossless transmission line realizes the pure time-delay necessary for the proper simulation of sampled-data system [4]. Figure 4.4 shows the schematic symbol in the z-domain for a storister having a delay equal to T (full switching period). The relationship between the current I(z) and the nodal voltages $V_1(z)$ and $V_2(z)$ of the storister is defined by:

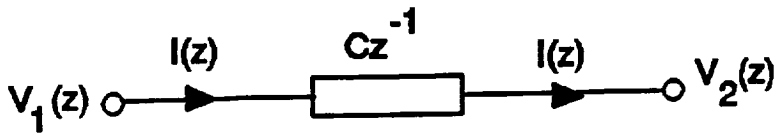


Figure 4.4 Z-domain Equivalent Circuit of Storister having a Delay of a Full Switching Period.

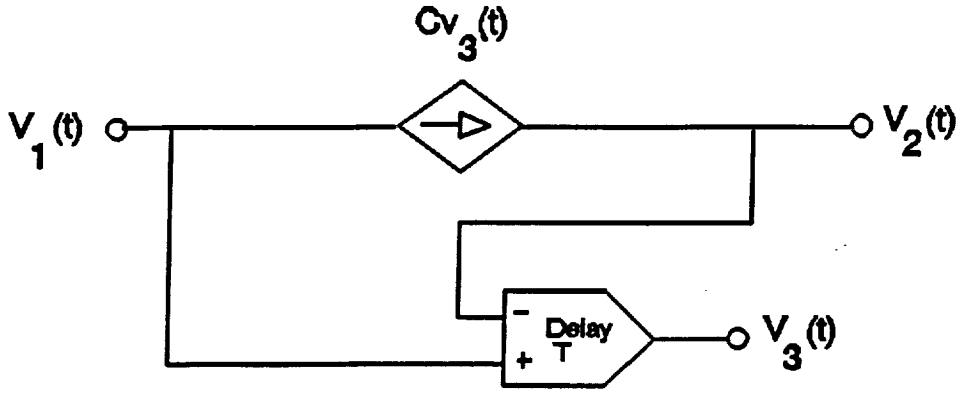


Figure 4.5 Continuous Time Model of a Storister.

$$I(z) = Cz^{-1}[V_1(z) - V_2(z)] \qquad (4.13)$$

In the s-domain, equation (4.13) becomes:

$$I(s) = Ce^{sT}[V_1(s) - V_2(s)] \qquad (4.14)$$

and in the continuous-time domain, equation (4.14) becomes

$$i(t) = C[v_1(t-T) - v_2(t-T)] \qquad (4.15)$$

Equation (4.15) can be rewritten as:

$$v_3(t) = V_1(t-T) - v_2(t-T) \qquad (4.16)$$

$$i(t) = Cv_3(t) \qquad (4.17)$$

Thus, equation (4.15) yields the continuous-time domain equivalent circuit of the storister shown in Figure 4.5. The differential input delay unit can be implemented by lossless transmission line element (available in the SPICE program). This is shown in Figure 4.6. Inserting the continuous time domain model of the storister (Figure 4.5) into Figure 4.3, we obtain Figure 4.7, which the continuous time domain equivalent circuit of the single phase grounded switched capacitor (SPGSC) with storister implemented using a lossless transmission line. SRAM with single phase grounded switched capacitor is shown in Figure 4.8.

4.3 MOS IMPLEMENTATION OF SC SRAM

The single phase grounded switched capacitor SRAM, implemented using MOS technology, is shown in figure 4.9. It consists of ten MOS transistors. M1, M2, M3

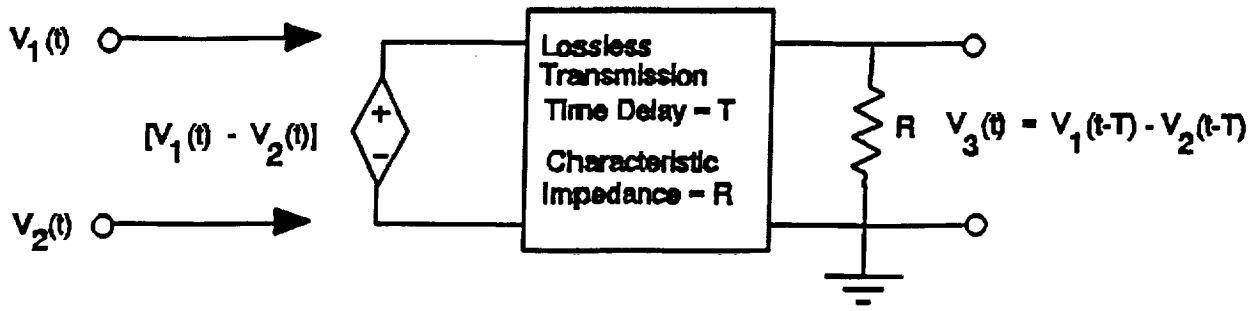


Figure 4.6 Model of SPICE Implementation of a Storister.

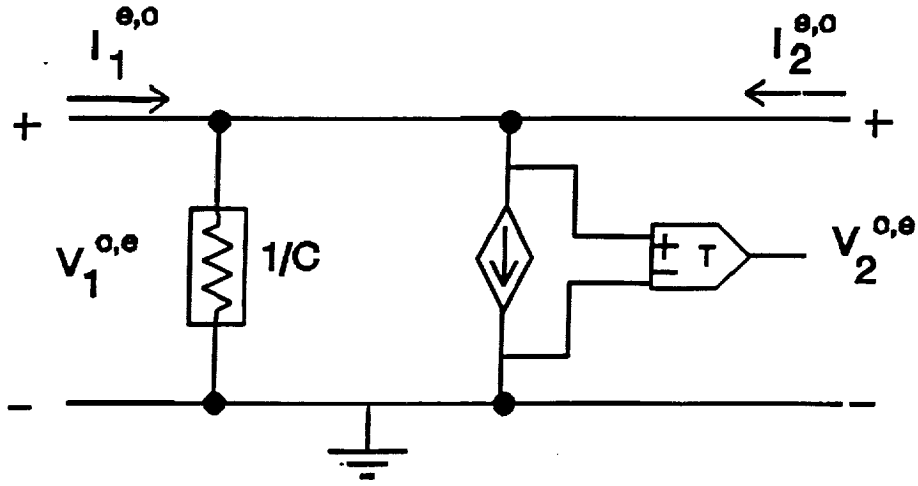


Figure 4.7 Continuous-Time Domain Equivalent Circuit of Single Phase Grounded Switched Capacitor (SC) Network.

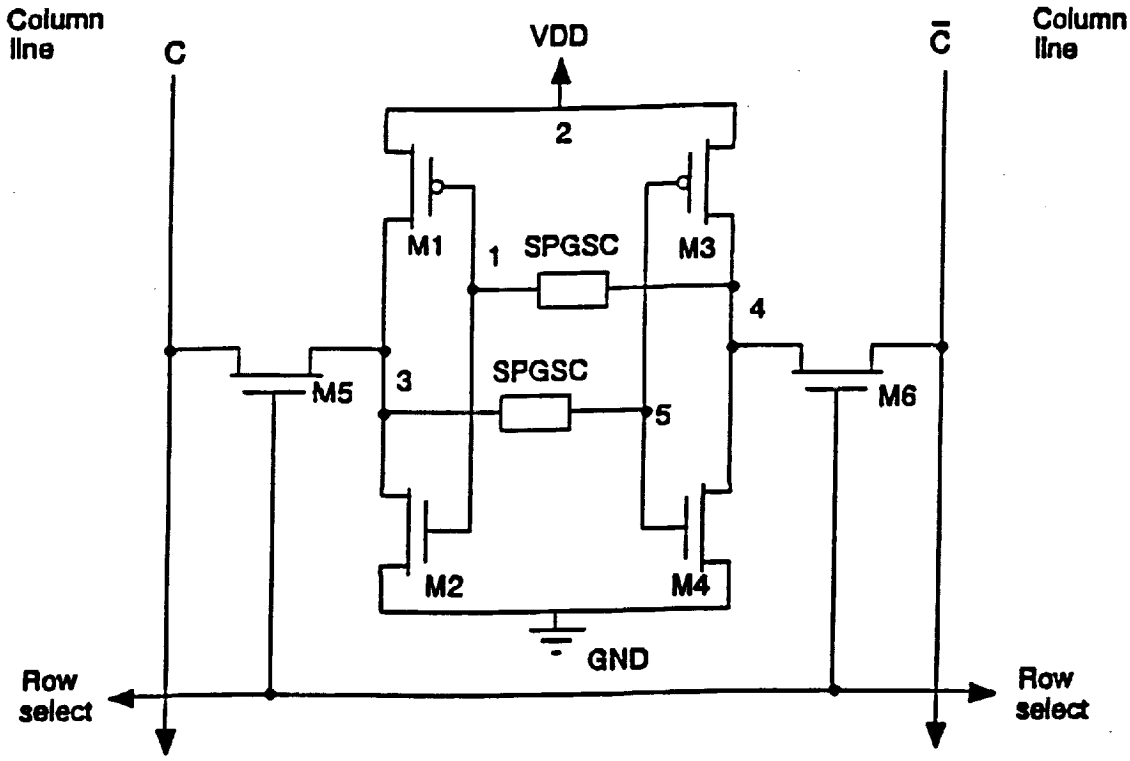


Figure 4.8 CMOS SRAM Cell with Single Phase Grounded SC Network.

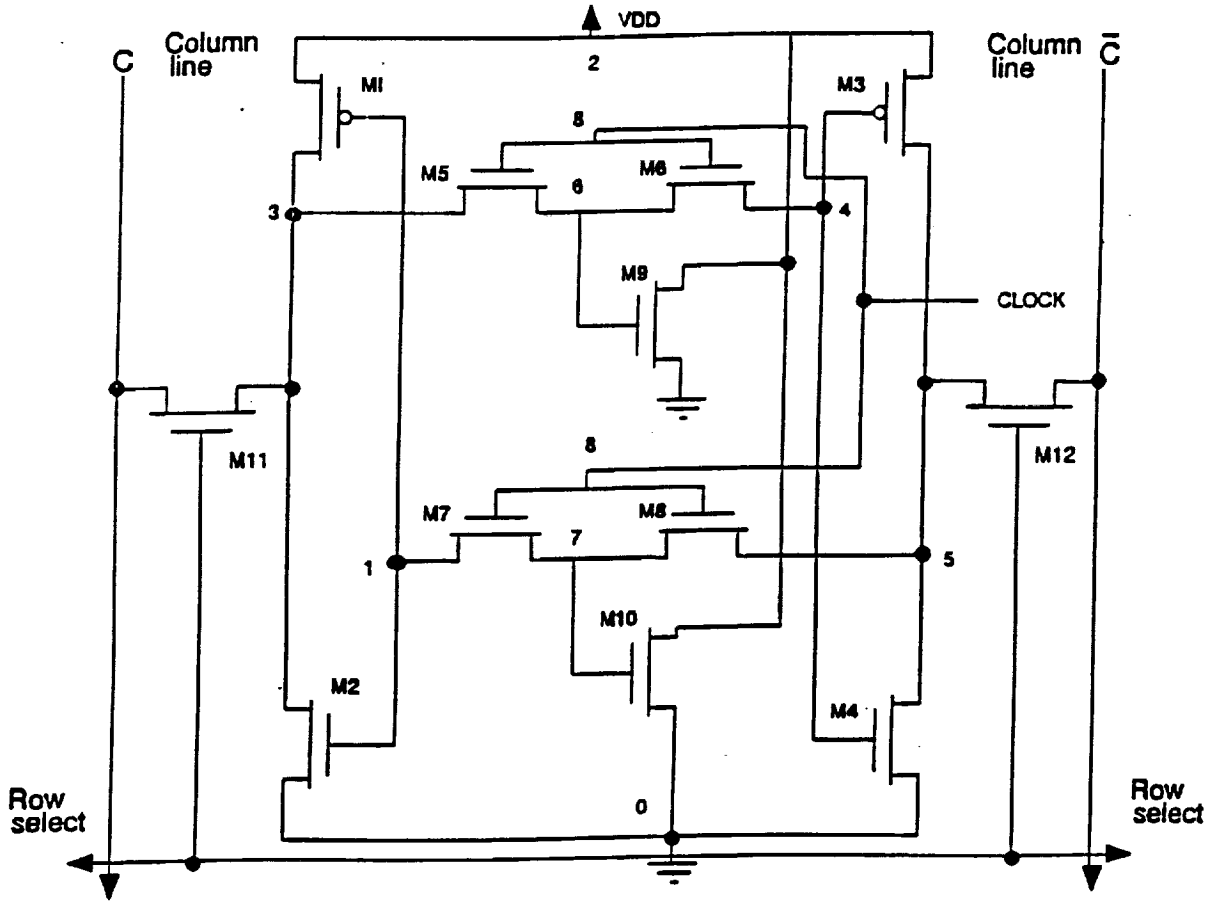


Figure 4.9 Switched Capacitor CMOS SRAM.

and M4 constitute the basic configuration of the SRAM cell and M5, M6, M7, M8, M9 and M10 constitute the SC network. The SC network operation is as follows. M5, M6, M7 and M8 are used in Figure 4.9 as switches, M9 and M10 are used as storage element (capacitors) and the clock generate the pulse to turn the switched capacitor ON and OFF. The resistance of the SC network depends on the clock frequency and storage elements. The SC networks provide the resistance needed for increasing the critical charge of the cell and also introduce additional capacitance to the sensitive nodes and the feedback paths of the cell, which can effectively increase SEU immunity of the cell. The SC SRAM operates in two modes, when clock pulse is ON and when clock pulse in OFF. In the following sections, we will compare the performance SC SRAM, SRAM without feedback and SRAM with feedback resistance.

4.4 SWITCHING TIMES OF SRAM CELLS

The switched capacitor CMOS SRAM cell, shown in Figure 4.9, was simulated when the pulse clock is ON and OFF and the results are compared with SRAM without feedback resistor (Figure 4.10) and SRAM with feedback resistor (Figure 4.1). Transient analysis on the various SRAM cells were performed. A rectangular pulse, with amplitude of 5V, pulse duration of 5ns, and period of 10ns, was connected at one input of the SRAM. Both the input and output were observed. The transient analysis output of switched capacitor SRAM cell with clock pulse ON or OFF are shown in Figure 4.11 and 4.12, respectively. From the results of the transient analysis the rise time, fall time, propagation delay and time-shift of the SRAM cells

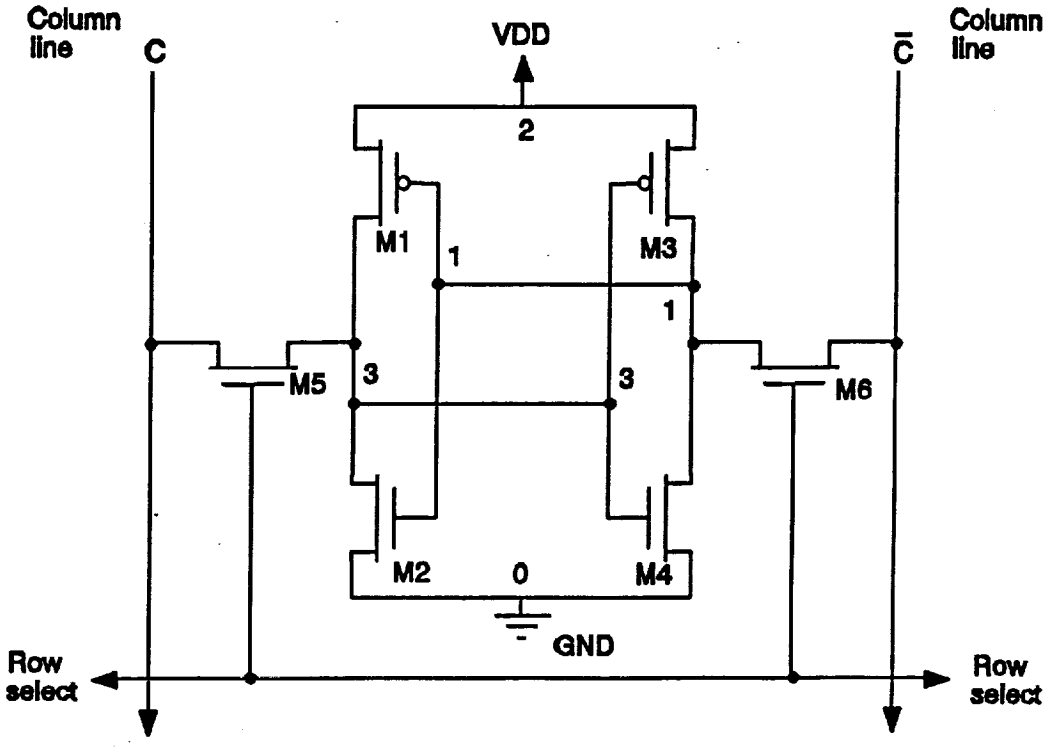


Figure 4.10 CMOS SRAM without Feedback Resistances.

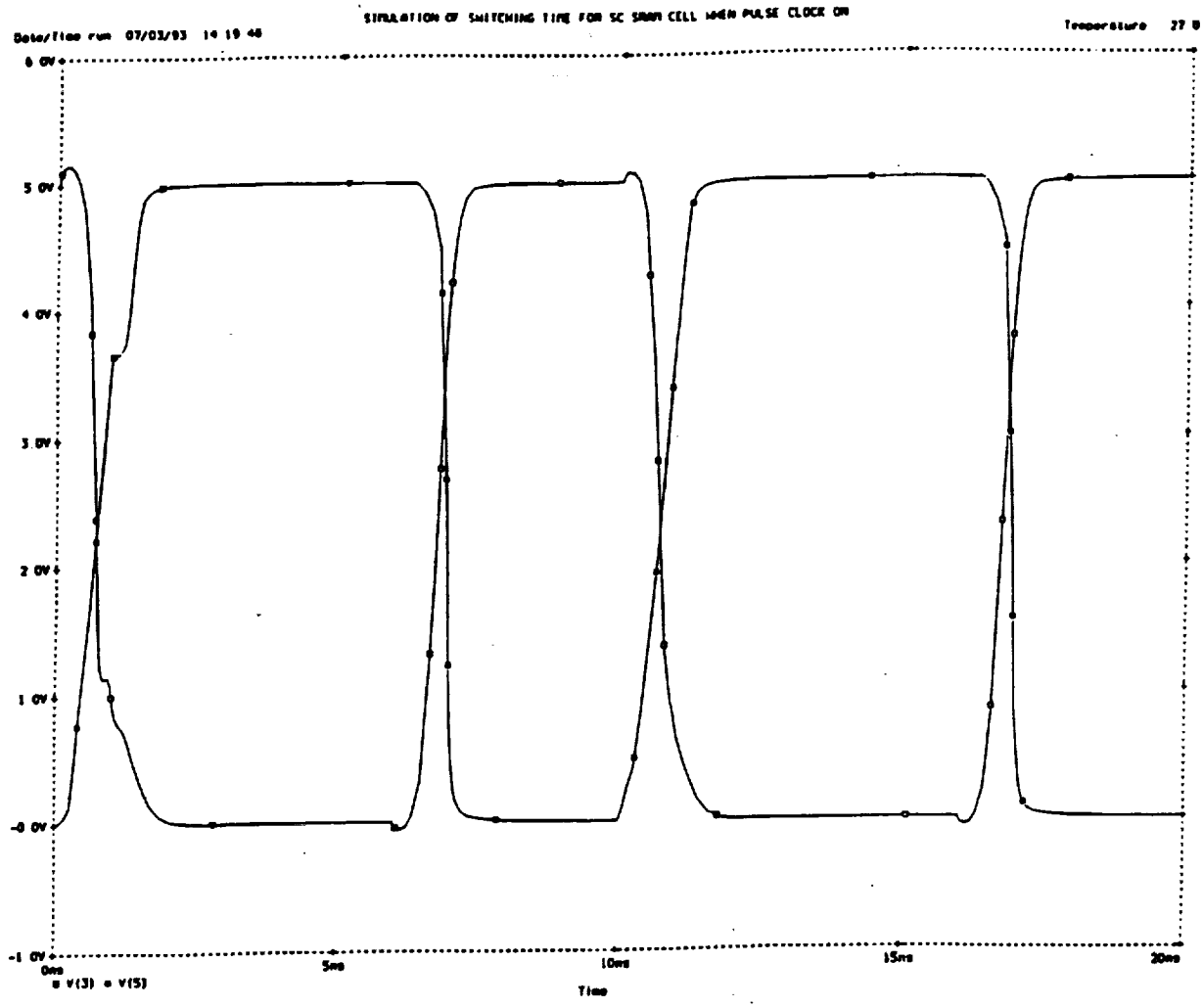


Figure 4.11 Transient Analysis of Switched Capacitor SRAM with the Clock Pulse ON. V(3) is input and V(5) is output.

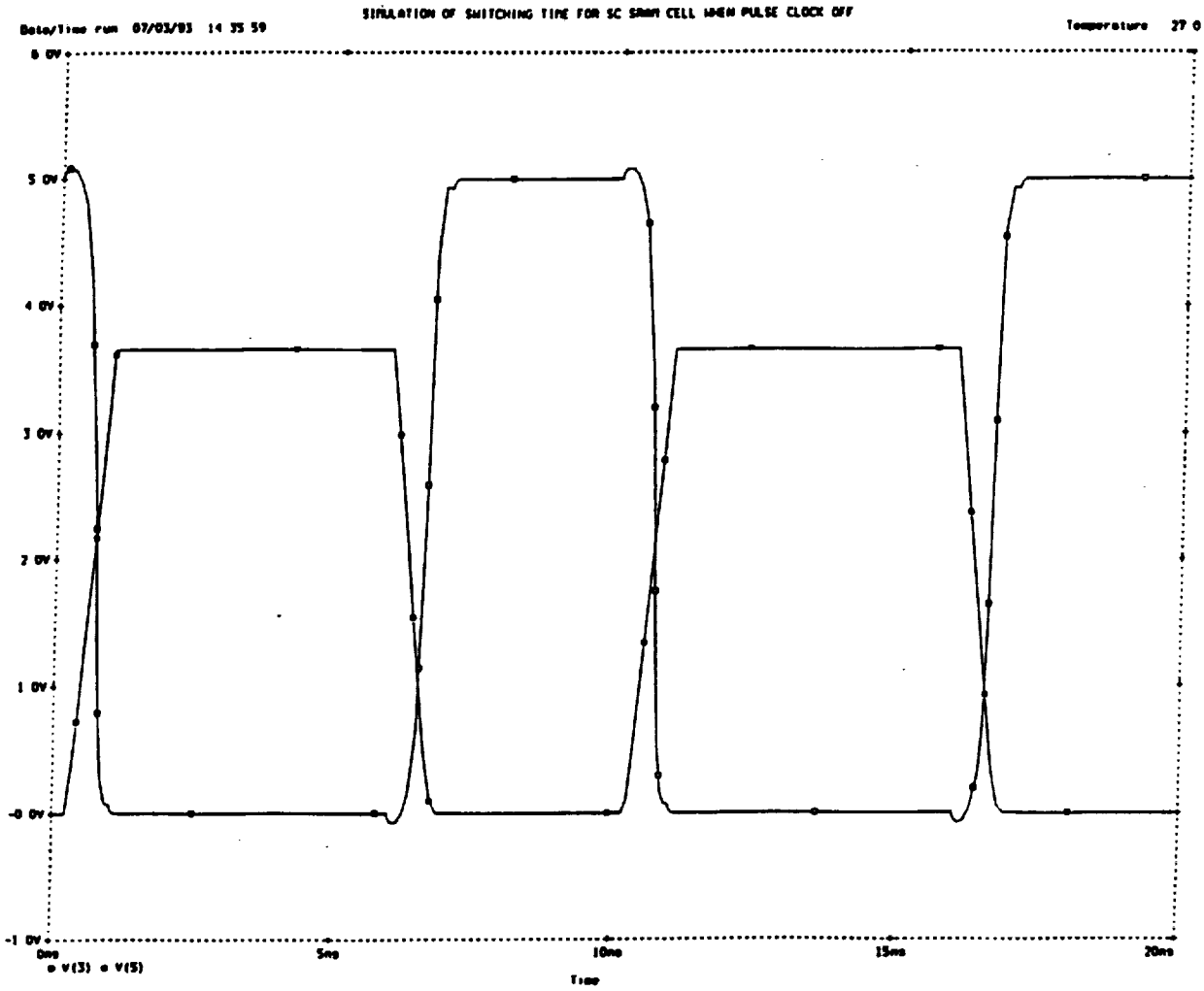


Figure 4.12 Transient Analysis of Switched Capacitor SRAM with the clock pulse OFF. V(3) is input and V(5) is output.

were obtained. The switching times are defined as follows:

Rise time: Time taken by amplitude of the output voltage to increase from 10% to 90% of the final value.

Fall time: Time during which the amplitude of the output voltage to fall from 90% to 10% of the maximum value.

Propagation delay: The average of rise time and fall time.

Time Shift: Time required for the output to occur when the input signal is applied.

Table 4.2 show the switching times of the SRAM cells. From Table 4.2, it can be seen that the rise time, fall time propagation delay and time shift of the switched capacitor SRAM with the clock pulse ON or OFF, and SRAM without feedback resistance are small compared to those of SRAM with feedback resistor. In addition, the rise time, fall time, propagation delay and time shift of the switched capacitor SRAM with clock pulse ON or OFF are similar to those of SRAM without feedback resistors.

The local write time is the minimum time required to change the logic state of SRAM via an access transistor. The local write time of the SRAM cells were determined. The circuits used to obtain the write time are Figure 4.10 (for SRAM without feedback resistance), Figure 4.1 (for SRAM with feedback resistance) and Figure 4.9 (for SC SCRAM with the clock pulse ON or OFF). To obtain the write times, 5V and 0V were connected to SRAM cells through access transistors. The pulse was placed on the gate of the access transistor, and SRAM output was

Table 4.2

Switching Times of SRAM Cells.

Feedback Resistance Value	Fall Time *E-9 S	Rise Time *E-9 S	Propaga-tion Delay *E-9 S	Time Shift *E-9 S
20k	0.90	0.891	0.895	1.497
40k	1.70	1.581	1.64	2.296
60k	2.49	2.378	2.434	3.201
80k	3.15	3.121	3.315	4.019
100k	4.00	3.750	3.870	4.830
120k	4.63	4.476	4.695	5.706
150k	5.73	5.503	5.616	6.972
200k	7.59	7.248	7.420	9.112
SRAM without feedback resistance	0.4087	0.380	0.645	0.765
SC SRAM when clock ON	0.280	1.029	0.654	0.7696
SC SRAM when clock OFF	0.610	0.5995	0.60475	0.6282

observed. The time taken for the output to reach 90% and 99% of the maximum output voltage was observed. Table 4.3 shows the write time of the memory cells, for the case where the output reaches 90% of the maximum output voltage. Table 4.4 is the local write time for the case where the SRAM output attains 99% of the maximum output voltage.

As seen from Table 4.3 and Table 4.4, the write time is increased with an increase in feedback resistance for SRAM. Figure 4.13 shows the write time versus resistance for the SRAM with feedback resistors. The figure was drawn using Table 4.3. It is obvious from the figure that, the write time increases as the feedback resistance increases. Note that the write time of SRAM without feedback resistor and SC SRAM with clock pulse ON are small compared to those of SRAM with feedback resistors. However, the SC SRAM with the clock pulse OFF has a higher value of write time.

4.5 CRITICAL CHARGE OF SRAM CELLS

A high energy particle can strike a sensitive node of SRAM. The charged particle, penetrating the memory cell device, will produce a number of carriers determined by the initial energy. The generated carriers appear as "photocurrent" within the affected node of a device. Cell upsets will take place if enough charge is delivered to the hit node. The charge needed to cause cell upset is termed critical charge, Q_{crit}. Critical charge is a measure of single event vulnerability of RAM cells. It can be evaluated by analysis of simulation of circuits and layouts during a design cycle, thereby allowing for design optimization.

Table 4.3

Local Write Times of SRAM when the SRAM Output Voltage is 90% of the Maximum Output Voltage.

Feedback resistance values	Write time *E-9 S
20k	3.9895
40k	7.1053
60k	10.30
80k	13.439
100k	16.63
120k	19.737
150k	24.526
200k	29.79
SRAM without feedback	0.622807
SC SRAM when the clock pulse ON	1.8947
SC SRAM when the clock pulse OFF	8.068

Table 4.4

Local Write Times of SRAM when the SRAM Output Voltage is 99% of the Maximum Output Voltage.

Feedback resistance values	Write time *E-9 S
20k	5.1158
40k	8.543
60k	11.030
80k	15.614
100k	17.790
120k	22.737
150k	28.211
200k	32.110
SRAM without feedback	0.712281
SC SRAM when the clock pulse ON	2.2456
SC SRAM when the clock pulse OFF	10.540

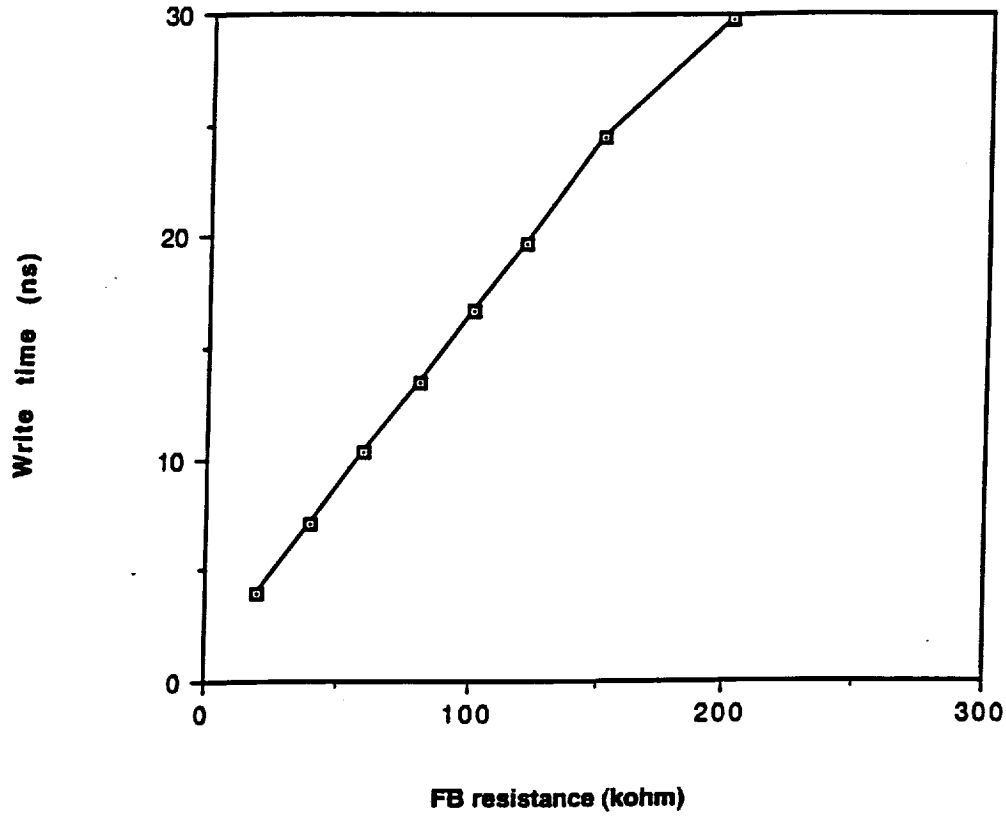


Figure 4.13 Write Time versus Feedback Resistance of CMOS SRAM.

To model the effect of p-hit for SC SRAM cell, SRAM without feedback resistance and SRAM with feedback resistance, an exponential current pulse was inserted between ground and node 5, (of Figure 4.9) between ground and node 3 (of Figure 4.10) and between ground and node 5 (of Figure 4.1), respectively. Similarly, to model the effect of n-hit, and exponential current pulse was inserted between node 3 and ground for SC SRAM (Figure 4.9), between node 1 and ground for SRAM without feedback (Figure 4.10) and between node 3 and ground for SRAM with feedback resistance (Figure 4.1). The analytical approximation of the current pulse due to transient radiation is shown by Messenger [5] as:

$$i(t) = I_o(e^{-t/\alpha} - e^{-t/\beta}) \qquad (4.18)$$

where:

Io is approximately the maximum current.

α is a collection time constant of the junction and

β is the time constant for initially establishing the ion track.

In this work, we used the modified version of equation (4.18). The waveform used is shown in Figure 4.14. The rise time and fall time constants of the exponential pulse were set equal to 0.01ns and 0.25ns, respectively [6].

During the computer simulations for the critical charge, we set the exponential current pulse width to be 2ns [6,7,8]. The critical charge was obtained by varying the amplitude of the exponential current pulse until the output of the SRAM cell changes state. Figure 4.15 and Figure 4.16 are P-hit simulations of SEU when the input and

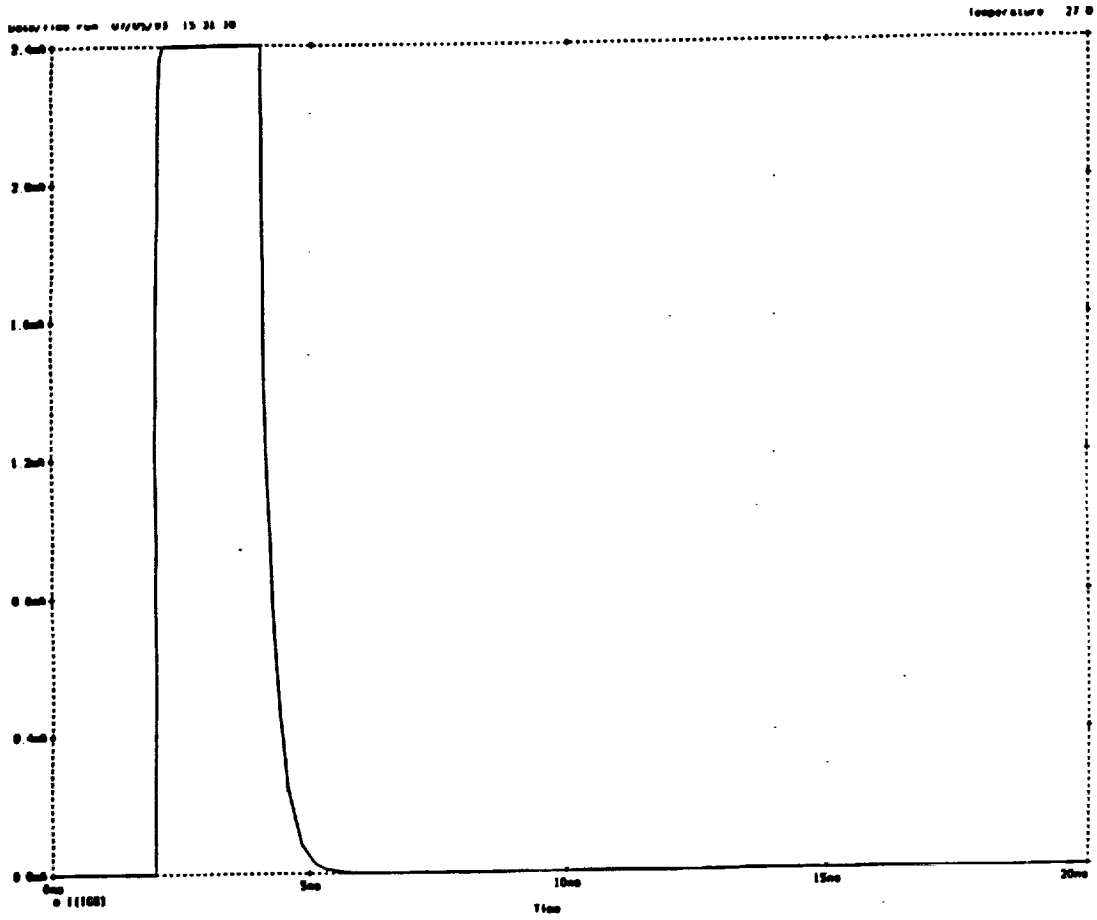


Figure 4.14 Waveform for the Exponential Current Pulse.

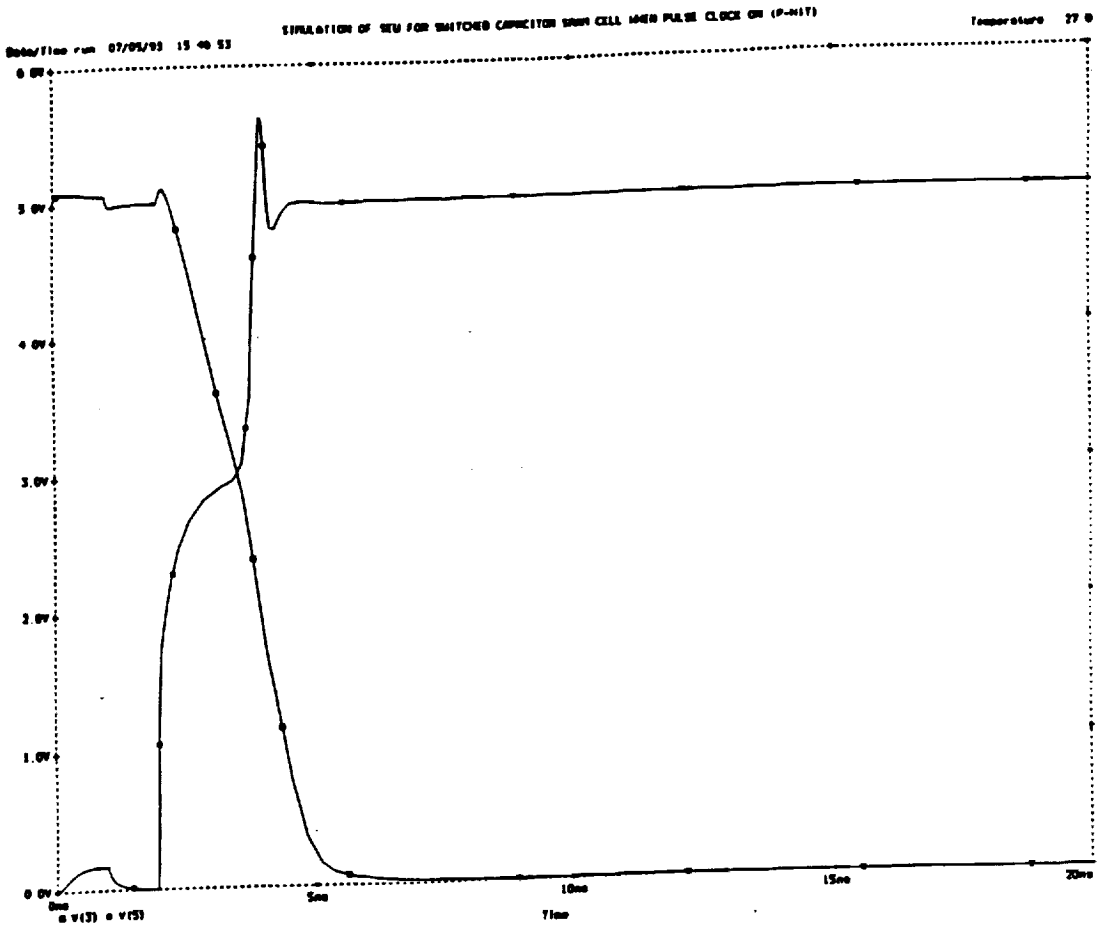


Figure 4.15 P-hit Simulation for SC SRAM with the Clock Pulse ON. V(3) and V(5) change states.

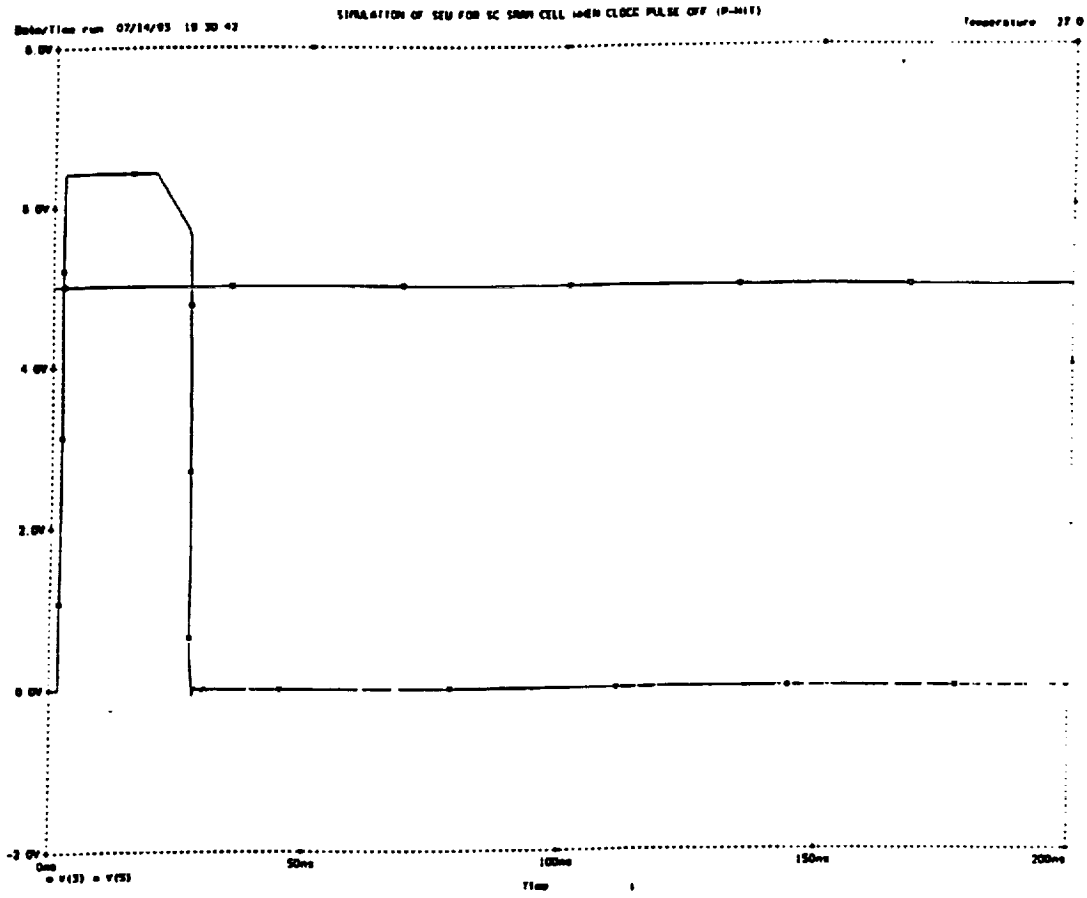


Figure 4.16 P-hit Simulation for SC SRAM with the Clock Pulse OFF. V(3) and V(5) change states.

output waveforms change states for SC SRAM when the clock pulse ON and OFF, respectively. Figures 4.17 and 4.18 are the p-hit simulations for SRAM without feedback and SRAM with feedback resistance of 80 kilohoms, respectively.

By knowing the amplitude and duration of the exponential current pulse required to change the state of the SRAM cells, the critical charge can be calculated by the expression:

$$Q_{crit} = \int_{o}^{\infty} i(t)\,dt \qquad (4.19)$$

The current pulse used in this work (show in Figure 4.15) can be expressed as:

$$i(t) = I_o(1-e^{-t/\tau_r}) \qquad 0 \le t \le 5\tau_r \qquad (4.20)$$

$$i(t) = I_o \qquad 5\tau_r \le t \le 2000\ ps \qquad (4.21)$$

$$i(t) = I_o(e^{-t/\tau_f}) \qquad 2000\ ps \le t \le 2000\ ps + 5\tau_f \qquad (4.22)$$

where:

τ_r is the rise time constant (10 ps).

τ_f is the fall time constant (250 ps).

2000 ps is the width of the exponential pulse and

I_o is the maximum value of the current pulse.

therefore,

$$Q_{crit} = I_o\left(\int_{0}^{5\tau_r}(1-e^{-t/\tau_f})\,dt + \int_{5\tau_r}^{2000ps} dt + \int_{2000ps}^{2000ps+5\tau_f} e^{-t/\tau_f}dt\right) \qquad (4.23)$$

The above equation simplifies to

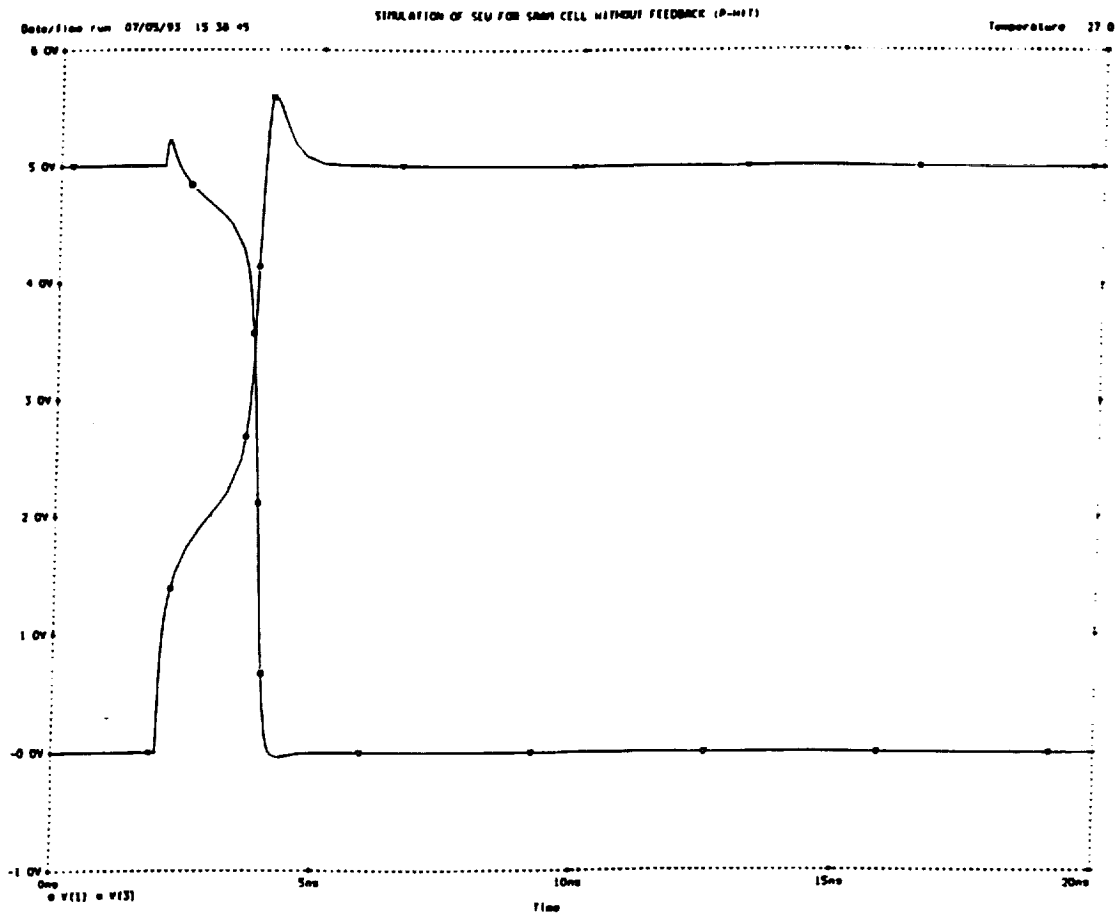


Figure 4.17 P-hit Simulation for SRAM without Feedback Resistor. V(1) and V(3) change states.

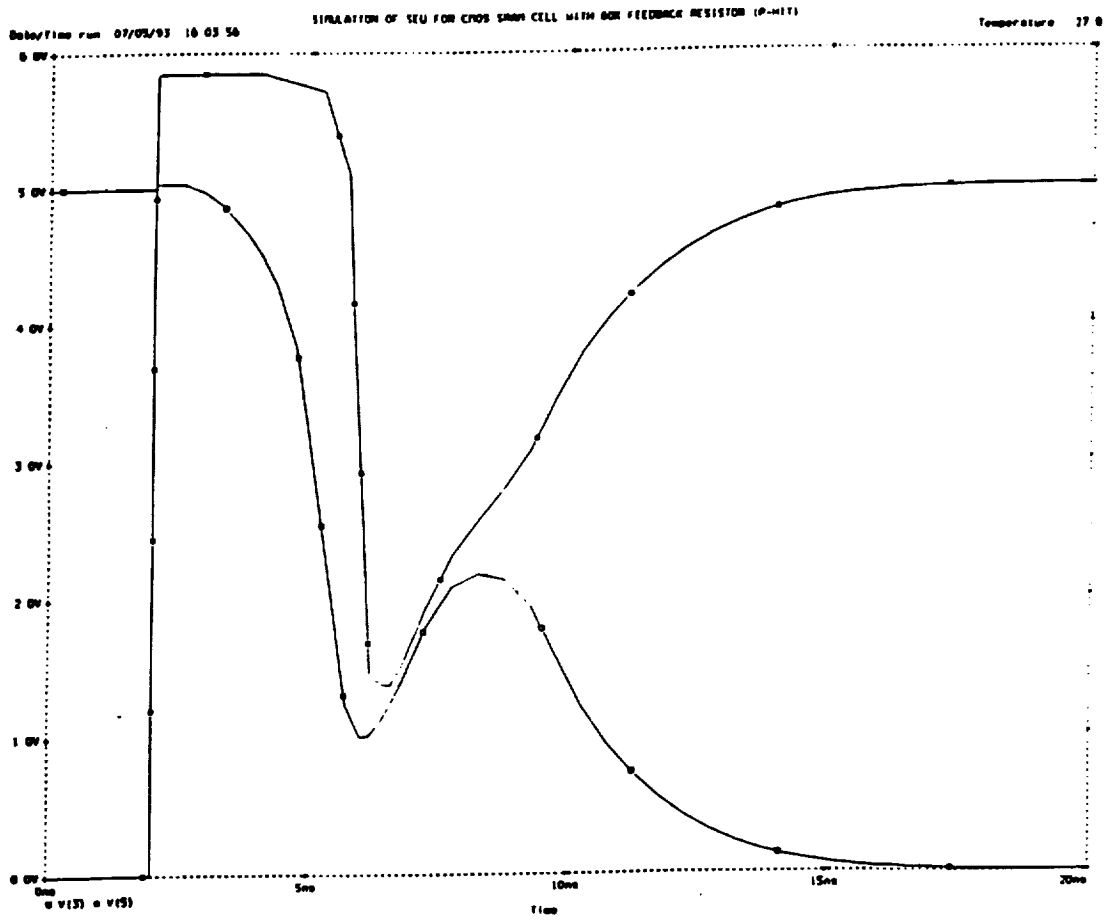


Figure 4.18 P-hit Simulation for SRAM with Feedback Resistance of 80 Kilohms. V(3) and V(5) change states.

$$Q_{crit} \approx I_o(2000ps) - \tau_r I_o \qquad (4.24)$$

$$Q_{crit} = 1990 I_o \ pC \qquad (4.25)$$

Table 4.5 shows the current amplitude needed to cause cell upset and critical charge of the p-hit simulations of the SRAM cells.

N-hit simulation for critical charge for the SC SRAM with the clock pulse ON and OFF were done. In addition, N-hit simulation for SRAM without feedback resistance and SRAM with 80 kilohms feedback resistance were performed. The waveforms are similar to those obtained for the P-hit simulations. The current pulse, described by equations (4.20) to (4.22), was used for the N-hit simulations. The critical charge was calculated using equations (4.19) and (4.24). Table 4.6 shows the current amplitude needed to cause cell upset and critical charge of the n-hit simulation of SRAM cells.

4.6 DISCUSSION OF RESULTS

From Table 4.2, it can be seen that the switching times of the switched capacitor SRAM are similar to those of SRAM without feedback resistors. Also, from Table 4.2, the switching times of the switched capacitor SRAM are similar to those of SRAM without feedback resistance. Thus, in terms of switching times, the switched capacitor SRAM is superior than resistive hardened SRAM.

From Figure 4.12, it can be seen that the output of the SC SRAM with the clock OFF is approximately 3.7 V. There is a potential drop across the large resistive value of the switched capacitor network. The voltage can be increased to 4.15 V if

Table 4.5

Critical Charge of CMOS SRAM Cells for P-hit Simulation of SEU.

Feedback resistance values	Current amplitude (A)	Critical charge (pC)
20k	1.9E-3	3.781
40k	2.3E-3	4.577
60k	49.4E-3	98.306
80k	1.5E1	29.850E3
100k	76.2E1	151.638E3
120k	3.0E3	5.97E6
150k	7.1E5	1.413E9
200k	73.8E6	146.862E9
CMOS SRAM without feedback resistance	1.3E-3	2.58
SC SRAM cell when pulse clock ON	2.4E-3	4.776
SC SRAM cell when pulse clock OFF	Greater than 1E9	1.99E12

Table 4.6

Critical Charge of CMOS SRAM Cells for N-hit Simulation of SEU.

Feedback resistance values	Current amplitude (A)	Critical charge (pC)
20k	2.3E-3	4.577
40k	3.0E-3	5.970
60k	35.9E-3	71.441
80k	1.6E1	3.184E3
100k	45.9E1	91.341 E3
120k	1.3E3	2.587E6
150k	2.8E5	557.20E6
200k	73.8E6	146.862E9
CMOS SRAM without feedback resistance	1.6E-3	3.184
SC SRAM cell when pulse clock ON	2.0E-3	3.980
SC SRAM cell when pulse clock OFF	Greater than 1E9	1.990E12

the input is 5.5 V; and also to 4.65 V if the input is 6.0 V.

From Figure 4.13 and Table 4.3, it is obvious that there is an linear relationship between the write time and the feedback resistance. This observation is similar to that observed by Fogarty and co-workers [9], who observed that for 32K x 8 SRAM (1.25μ process) the cell write time is approximately 1.48ns per 100 kilohms.

From Table 4.3, it can be seen that the write time of the SC SRAM is low when the clock pulse ON, but it is considerably higher when the pulse clock is OFF. When the clock pulse is ON, the equivalent resistance of the switched capacitor is low. However, the equivalent resistance of the switched capacitor is very high when the clock pulse is OFF. This will account for the differences in the write times of the switched capacitor SRAM for clock pulse being ON or OFF. The write-time the SC SRAM with clock pulse OFF is comparable to SRAM with feedback resistance of 60 kilohms.

From Tables 4.5 and 4.6, it can be seen that as the feedback resistance increases, the critical charge increases. This is expected, since the higher the value of the feedback resistance the more the SRAM will be hardened against single event upsets. There is no trend in terms of whether the critical charges for N-hit are higher than those of P-hit. In addition, Tables 4.5 and 4.6, shows that when the clock pulse of the SC SRAM is ON, the critical charge of the SC SRAM is small. However, when the clock pulse of the SC SRAM is OFF, the critical charge of the SC SRAM is extremely large.

The SC networks provide the resistance needed for increasing critical charge of the cell and also introduce additional capacitance to the sensitive nodes and the feedback paths of the cell, which can effectively increase SEU immunity of the cell.

The switched capacitor SRAM seems to be a viable alternative to SRAM with

polysilicon feedback resistors. The switching times of the SC SRAM are smaller than those of SRAM with feedback resistors. The write time of SC SRAM (clock pulse OFF) is better than that of SRAM with feedback resistance of 60 kilohms. In addition, the critical charge of SC SRAM (with clock pulse OFF) is far greater than that of SRAM with feedback resistance of 200 kilohms.

4.7 CONCLUSIONS AND FUTURE WORK

One method that is used to harden CMOS SRAM cells against single event upsets is the use of feedback resistors. However, the feedback resistors normally used to hardened CMOS SRAM cells increases the write time and the size of SRAM cells. In addition, because of negative temperature coefficient of the polysilicon resistor, the SRAM becomes more susceptible to radiation at high temperatures. In this chapter, a method is developed for replacing polysilicon feedback resistors with switched capacitors.

The equivalent circuit of the switched capacitor networks, suitable for SPICE simulations was developed. SRAM, with the above switched capacitor network was simulated using SPICE. SRAM with single-phase grounded switched capacitor had functional characteristics similar to classical SRAM.

The single phase grounded switched capacitor SRAM was implemented using MOS technology. Computer Simulations using SPICE were performed on switched capacitor SRAM, SRAM without feedback resistors and SRAM with feedback resistors. It was found that the rise time, fall time, propagation delay and the time shift of the switched capacitor SRAM, and SRAM without feedback resistors were

small compared to those of SRAM with feedback resistors. In addition, the switching times of the switched capacitor SRAM were found to be superior than those of SRAM cells with feedback resistors.

The write times of the SRAM without feedback resistor and switched capacitor SRAM with the clock pulse ON are small compared to those of SRAM with feedback resistors. However, the switched capacitor SRAM with the clock pulse OFF has a write time comparable to that of SRAM with 60 kilohms feedback resistance.

As expected, the critical charge of SRAM was found to increase with feedback resistance. In addition, it was found that, when the pulse clock of the switched capacitor is ON, the critical charge of the switched capacitor SRAM is small. However, when the clock pulse of the switched capacitor is OFF, the critical charge of the switched capacitor is extremely large.

The switched capacitor SRAM seems to be a viable alternative to SRAM with polysilicon feedback resistors. The switching times of the SC SRAM are smaller than those of SRAM with feedback resistors. The write time of SC SRAM (clock pulse OFF) is better than that of SRAM with feedback resistors of 60 kilohms. However, the critical charge of SC SRAM (with clock pulse OFF) is far greater than SRAM with feedback resistance of 200 kilohms.

The switched capacitor SRAM seems to be a viable alternative to SRAM with polysilicon feedback resistance. However, the results and the conclusions of this work were obtained from SPICE simulations. The conclusions need to be checked with fabricated versions of the switched capacitor SRAM.

This work did not consider the effect of total ionizing dose (TID) radiation on

the functional performance of switched capacitor SRAM. It is well known that TID radiation on MOS device, causes threshold voltage shift, mobility degradation and increases in leakage current. The double effects of TID and SEU need to be considered for SC SRAM and other memory cells.

The write time of the SC SRAM, when the clock pulse is OFF is large. Circuit design approaches should be considered with the view of reducing the write time. One approach will be to explore the sizing of the inverter transistors of the SRAM and also the transistors of the switched capacitor network.

4.8 REFERENCES

[1] Andrews, J.L., Schroeder, J.E., Gingerich, B., Kolasinski, W.A., Koga, R. and Diehl, S.E. "Single Event Error Immune CMOS RAM" IEEE Trans. on Nuclear Sci., Vol. NS-29, No. 6, Dec. 1992

[2] Sedra, A.S. and Smith, K.C. "Microelectronic Circuits", 3rd Edition, Saunders College Publishing, 1990.

[3] Kurth, C.F. and Moschytz, G.S. "Nodal Analysis of Switch Capacitor Networks" IEEE Trans. on Circuits and Systems, Vol. CAS 26, No. 2, pp. 93-104, Feb. 1979.

[4] Nelin, D.B. "Analysis of Switched-Capacitor Networks Using General Purpose Simulation Programs", IEEE Trans on Circuits and Systems, Vol. CAS-30, No. 1, pp. 43 - 48, Jan. 1983.

[5] Messenger, C.G. and Ash, S.M. "The Effects of Radiation of Electronic Systems", Van Nostrand Reinhold, 1992.

[6] Jaeger, R.G., Fox, R.M. and Diehl, S.E. "Analytic Expressions for the Critical Charge in CMOS Static RAM cells", IEEE Trans. on Nuclear Sci., Vol. NS 30, No. 6, pp. 4616 - 4619, 1983.

[7] Diehl, S.E., Ochoa Jr., A., Dressendorfer, P.V., Koga, R. and Kolasinski, W.A. Error Analysis and Prevention of Cosmic Ion-Induced Soft Error in Static CMOS RAM", IEEE Tran. on Nuclear Sci., Vol. NS-29, No. 6, pp. 2032 - 2039, Dec. 1982.

[8] Linder, J.S., Kahn, M.H. and Tang, T. "Capacitive Radiation Hardening Approach for SEUs of SRAM cell" Engineering and Architecture Symposium,

Prairie View, Texas, Vol. 1, pp. 290 - 294, March 1993.

[9] Fogarty, T.N., Okyere-Attia, J., Kumar, A.A., Tang, T.S. and Linder, J.S. "Modeling and Experimental Verification of Single Event Upset", In Selected Topics in Robotics for Space Exploration (Ed. R.C.Montgomery), NASA Langley Research Center, March 1993.

CHAPTER 5

SUMMARY

Alpha-particle induced soft errors in dynamic memories were investigated in this report. Column and cell alpha particle hits were simulated for MOS dynamic memory cell using SPICE. Simulations were performed to obtain the critical charge of bitline, memory cell, and combined cell-bitline during an alpha particle hit.

The row and column capacitances and resistances were calculated from circuit layout using 2 micron design rules. It was found that the critical charge of the bitline was far higher than that of the cell. In addition, the critical charge for the combined cell-bitline was found to be dependent on the gate voltage of the access transistor

In addition, the effect of total ionizing dose radiation on the switching times of CMOS logic gate was obtained by considering the effects of radiation on mobility and threshold voltage on MOSFET transistors. The rise time and fall time equations of CMOS logic gates were derived. The results from the derived equations were compared with an approximate equations for switching time found in the literature. The effects of total ionizing dose on the switching times of CMOS logic gates were obtained by the use of C and SPICE programs.

The results of this work indicate that, the rise time of CMOS logic gates increases, while the fall time decreases with an increase in total ionizing dose. Also, by increasing the size of the P-channel transistor, the propagation delay of CMOS logic gate can be made to decrease with, or be independent of an increase in total

ionizing dose radiation. The result from the C program calculations and SPICE simulations show similar trends.

Furthermore, a method was developed for replacing polysilicon feedback resistance of SRAMs with a switched capacitor network. For the purpose of computer simulations, the equivalent circuit of switched capacitor was developed in the continuous time domain using storister. Computer simulations show that SRAM with single phase grounded switched capacitor has functional characteristics similar to those of standard SRAM.

A single phase grounded switched capacitor SRAM was implemented using MOS technology. The characteristics of switched capacitor SRAM were compared with those of SRAMs with feedback resistance. It was found that the rise time, fall time and propagation delay of the switched capacitor SRAM is superior to those of SRAM with feedback resistance. The switched capacitor method has a write time similar to or better than SRAM with passive feedback resistance. In addition, the switched capacitor SRAM, when the clock pulse is off, has a very large critical charge. The results of this work indicate that switched capacitor SRAM is a viable alternative to SRAM with polysilicon feedback resistance.

APPENDIX A

RESEARCH STAFF

Persons who did various aspects of this work are:

(A) Principal Investigator

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APPENDIX B

PUBLICATIONS

The following papers, thesis and design project reports were published from this work

(A) PAPERS

1. Okyere-Attia, J and Sasabo, M.L. "Design of CMOS Logic Gates for TID Radiation", Proceedings of Fifth NASA Symposium on VLSI Design", Albuquerque, New Mexico, Nov. 1993.

2. Eshete, F. and Okyere-Attia, J. "Radiation Hardening of CMOS SRAM Using Switched Capacitor Networks." Proc. of 1993 Engineering and Architecture Symposium, Prairie View, Texas, pp. 306 - 311, March 1993.

3. Okyere-Attia J. and Sasabo, M.L. "Prediction of the Effects of Total Ionization Dose Radiation on the Switching Times of CMOS Logic Gates." Proc. of 1993 Engineering and Architecture Symposium, Prairie View, Texas pp. 93 - 103, March 1993.

4. Fogarty, T.N., Okyere-Attia, J., Kumar, A.A., Tang, T.S. and Linder, J.S. "Modeling and Experimental Verification of Single Event Upsets" In Selected Topics in Robotics for Space Exploration, (Ed. R.C. Montgomery) Published by NASA Langley Research Center, March 1993.

5. Okyere, J.G. and Abbey, J. "Single Event Upset Susceptibility of DRAMs" Proc. of 2nd Consortium Conference on Space Radiation on Materials, VLSI and Biosystems, Hampton, 1991

(B) M.S. THESIS

1. Sasabo, M.L. "Effects of Total Ionizing Dose on Switching Times of CMOS Logic Gates" M.S. Thesis, Prairie View A&M University, Prairie View, Texas, August 1992

2. Eshete, F. "Radiation Hardening of CMOS SRAM Using Switched Capacitor Networks", M.S. Thesis, Prairie View A&M University, Prairie View, Texas, August, 1993.

(C) UNDERGRADUATE SENIORS DESIGN PROJECT REPORTS

1. Bonner, J., Reed, R. and Simmons, R. "Design of SR Flip-Flop Circuits with Active Transmission Gates" Senior Design Project Report, Electrical Engineering Dept, Prairie View A&M University, Dec. 1992.

2. Blackshire, M., People, E. and Rahman, A. " Design Considerations for Non-Radiation Hardened and Radiation Hardened CMOS SR Flip-flop" Senior Design Project Report, Electrical Engineering Dept, Prairie View A&M University, Dec. 1991.

3. Abbey, J. 'Dynamic Memories Using Deep-Depletion MOS Capacitors" Senior Design Project Report, Electrical Engineering, Prairie View A&M University, August 1990.

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