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PRINT FIG. 4

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AWARDS DIGEST

Forback DC-To-DC Converter

As shown in Figures 4 and 5, a pulse-width modulated DC-to-DC power converter in accordance with this invention includes a first inductor, i.e. a transformer 14 (Figure 4) or an equivalent fixed inductor 21 (Figure 5) equal to the inductance of the secondary winding 20 of the transformer 14, coupled across a source of DC input voltage 10 via a transistor switch 16 which is rendered alternately conductive (ON) and non-conductive (OFF) in accordance with a signal from a feedback control circuit 18. A first capacitor 42 capacitively couples one side of the first inductor 14, 21 to a second inductor 22 which is connected to a second capacitor 24 which is coupled to the other side of the first inductor 14, 21. A circuit load 26 shunts the second capacitor 24. A semi-conductor diode 30 is additionally coupled from a common circuit connection between the first capacitor 42 and the second inductor 22 to the other side of the first inductor 14, 21. A current sense transformer 52 generating a current feedback signal for the switch control circuit is directly coupled in series with the other side of the first inductor 14, 21 so that the first capacitor 42, the second inductor 22 and the current sense transformer 52 are connected in series through the first inductor 14, 21.

Invention is believed to reside in the specific location of the current sense transformer and the equal inductance values of the first and second inductors. Such a converter topology results in a simultaneous volt-second balance in the first inductance and ampere-second balance in the current sense transformer.

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FORBACK DC-TO-DC CONVERTER

Origin of the Invention

This invention was made by an employee of the United States Government and therefore may be made and used by the U.S. Government for governmental purposes without the payment of any royalties thereon or therefor.

Background of the Invention

This invention relates generally to DC-to-DC converters and more particularly to a pulse-width modulated switching converter.

DC-to-DC power converters utilizing a switching device in a combination of inductors and capacitors to derive power from one source of DC voltage and then deliver that power to a load at the same or a different DC voltage are well known. Many different types of topologies exist for implementing such power converters. The number of different possible combinations using but a relatively few components has resulted in several standard topology types which include, among others, the buck, boost, buck-boost, forward, flyback, and CUK converters. With what initially appears to be only a simple change or a modification in the particular converter implementation, an extremely significant performance variation can result.

While many different topologies could be described, each with its own advantages and disadvantages, the configurations shown in Figures 1-3 best represent prior art topologies which exhibit the closest similarity to that of the subject invention to be hereinafter described.

Figure 1, for example, discloses what might be termed a forward converter topology and comprises an isolated or transformer version of a buck converter which, without an input filter, is typically characterized by a converter which displays discontinuous input current while providing a continuous output current. Such an arrangement offers an efficient power conversion technique; however, it almost always requires the use of a reset winding on the power transformer in order to reset the transformer core by returning its stored energy to the primary side. This requirement, while not being difficult to implement, creates some additional design considerations associated with the reset circuitry.

With respect to the circuitry shown in Figure 2, it exemplifies what is termed flyback converter topology and comprise what might be referred to as an isolated or transformer version of a boost converter which, without an input filter, is characterized by discontinuous input

current while also providing discontinuous output current and where the required inductor is incorporated into the transformer which comprises a flyback transformer. It typically offers the smallest number of components for DC-to-DC power conversion.

The third configuration comprises topology which is illustrative of an isolated or transformer version of the CUK converter. An isolated CUK converter utilizes a transformer which is capacitively coupled both on the primary and secondary sides.

While each of the above-referenced power converters as well as other known converter topologies have known utility, inherent limitations and certain disadvantages nevertheless exist.

Summary

Accordingly, it becomes a primary object of this invention to provide an improvement in DC-to-DC power converters.

It is another object of the invention to provide an improvement in pulse-width modulated DC-to-DC power converters.

It is still another object of the invention to provide a pulse-width modulated DC-to-DC power converter having current mode control.

And it is yet another object of the invention to provide a DC-to-DC converter which provides both volt-second balance of the power transformer and ampere-second balance of the current sensing transformer simultaneously.

Briefly, the foregoing and other objects of the invention are achieved by a current-mode controlled pulse-width modulated DC-to-DC power converter including both isolated and non-isolated implementations comprised of a first inductor, i.e. a transformer or an equivalent fixed inductor equal to the inductance of the secondary winding of the transformer, coupled across a source of DC input voltage via a controlled switch device, e.g. a transistor, and which is rendered alternately conductive (ON) and non-conductive (OFF) in accordance with a signal from a feedback control circuit which continuously controls the duty cycle of the transistor switch in relation to a complete cycle of operation. A first capacitor capacitively couples one side of the first inductor to an output filter circuit including a second inductor coupled to a second capacitor which in turn is coupled to the other side of the first inductor, with the circuit load being coupled across the second capacitor. A semiconductor diode is additionally coupled from a common circuit connection between the first capacitor and

the second inductor to the other side of the first inductor. A current sense transformer generating a current feedback signal for the switch control circuit is directly coupled in series with the other side of the first inductor so that the first capacitor, the second inductor and the current sense transformer are connected in series through the first inductor. This enables the current of the first and second inductors to be alternately sensed during both portions of an operational cycle. The inductance values of the first and second inductors, moreover, are made identical. The location of the current sense transformer and the use of equal valued first and second inductors result in a relatively simple DC-to-DC converter topology wherein volt-second balance in the first inductor and ampere-second balance in the current sense transformer are achieved simultaneously while at the same time reducing undesired stresses on the switching transistor.

Brief Description of the Drawing

The following detailed description of the invention will be more readily understood when considered together with the accompanying drawings wherein:

Figure 1 is an electrical schematic diagram illustrative of a known prior art forward type of converter topology;

Figure 2 is an electric schematic diagram illustrative of a flyback type converter topology;

Figure 3 is an electrical schematic diagram illustrative of an isolated version of a known prior art CUK type converter topology;

Figure 4 is an electrical schematic diagram illustrative of an isolated or transformer version of the preferred embodiment of the invention;

Figure 5 is an electrical schematic diagram illustrative of a non-isolated version of the preferred embodiment of the invention shown in Figure 4;

Figure 6 is an electrical schematic diagram illustrative of the topology shown in Figure 5 during a first portion of a circuit operating time period;

Figure 7 is an electrical circuit diagram illustrative of the circuit shown in Figure 5 during a second portion of the operational time period;

Figure 8 is a set of time related waveforms illustrative of the current and voltage relationships provided by the non-isolated embodiment shown in Figure 5; and

Figure 9 is a waveform diagram illustrative of the current flow through the current sensing transformer shown in Figure 5 during both portions and of the operational time period.

Detailed Description of the Invention

Prior Art

Before considering the details of the invention, reference will first be made back to the prior art converter topologies referred to above and illustrated in Figures 1-3.

As shown in Figure 1, the isolated forward topology depicted thereat includes a DC voltage input source 10 which applies energy to the primary winding 12 of a power transformer 14 under the control of a transistor switch 16, rendered alternately conductive (ON) and non-conductive (OFF) during each cycle T_s of operation by a feedback control circuit 18 coupled to the primary winding 12 and which controls the ON and OFF time dT_s and $\bar{d}T_s$, respectively, of the transistor 16, where d designates the duty cycle, and accordingly that of the converter itself. The secondary winding 20 couples energy to an inductor-capacitor output filter including an inductor 22 and capacitor 24, with the load comprising a resistance element shown by reference numeral 26 coupled across or shunting capacitor 24.

Furthermore, a diode 28 is connected in series from one (·) polarity end of the secondary winding 20 to the inductor 22, while a second diode 30 shunts both the inductor 22 and the capacitor 24 while being coupled to

the other or opposite end of the secondary winding 20 along with the one side of the capacitor 24 and load 26 The primary side of the transformer 14 also includes a reset circuit including a reset winding 32 having its (·) polarity end connected to ground. However, it also requires an additional diode 34 and a capacitor 36 which forms part of an input filter including an inductor 38 connected in series with voltage source 10. The input filter acts to filter out voltage and current noise on the input voltage V_{in}, and primarily to filter converter induced current pulses from the DC power source 10.

The forward converter topology illustrated in Figure 1 offers an efficient power conversion technique; however, it typically requires the use of a reset winding such as the winding 32 to reset the transformer core of the power transformer 14 by returning its stored energy to the primary side. This requirement, although not difficult to implement, causes certain design problems for some applications, such as requiring the additional diode 34 and a relatively large capacitance value for the capacitor 36.

With respect to the flyback topology as depicted in Figure 2, it intentionally stores energy in the inductance of the power transformer 14 during the on-time interval dT_s of the transistor power switch 16 and then

releases the energy to the secondary side of the transformer 14 during its off-time $\bar{d}T_S$ and where for continuous mode operation $dT_S + \bar{d}T_S = T_S$, the time period for one operational cycle. The energy delivered to the load side of the transformer 14 is out of phase with the reenergizing process of the inductance which is incorporated into the transformer 14. If operated in the continuous inductor current mode, this characteristic produces inherent problems in the stability in the duty cycle control circuit 18 which generally results in compromised dynamic performance and when operated in the discontinuous inductor current mode, the switching transistor 16 and the diode 28 can be subjected to undesirable relatively high peak current stresses.

As to the CUK topology illustrated in Figure 3, in addition to capacitively coupling the primary and secondary windings 12 and 20 of the power transformer 14 to their respective input and output circuit components, the grounded capacitor 36 of the forward and flyback topologies (Figures 1 and 2) forming part of the input filter is deleted and the control switch device 16 is no longer directly connected to the primary winding 12, but is now connected to a circuit node 39 common to both the inductor 38 and the coupling capacitor 40. Additionally, damping circuits comprised of respective series circuits

including capacitor 44, resistor 46 and capacitor 48, resistor 50 must be utilized and shunt the coupling capacitors 40 and 42.

The coupling capacitor arrangement of the CUK topology operates to continuously maintain volt-second balance on the core of the transformer 14 in addition to developing a push-pull driving voltage for improved flux utilization. In so doing, the front end inductor 38 now operates as a current source which drives energy into the transformer 14 and the coupling capacitors 40 and 42. One major disadvantage of the CUK topology, however, is that this current source typically produces voltage spikes across the switching transistor 16, which are often times extremely difficult to reduce. Furthermore, both the switching device 16 and the output diode 30 must carry significantly higher currents than typically encountered in other topologies. The potential voltage and current stresses imposed on both the switching device 16 and the diode 30 force the circuit designer to select components rated for relatively high power levels.

In addition to the potential switching component stresses and other additionally required protection circuitry, not shown, the biggest inherent disadvantage of the CUK topology is the necessary presence of relatively large damping components across both the

primary and secondary coupling capacitors 40 and 42 which are shown comprising capacitor 44, resistor 46, and capacitor 48, resistor 50. The damping components are required to shape the AC behavior of the control circuitry 18 being generally large in bulk make size and weight an important and undesirable concern for many applications.

Description of the Preferred Embodiments

Considering now the preferred embodiments of the subject invention which are shown in Figures 4 and 5, this invention overcomes the inherent deficiencies of the prior art converter topologies shown in Figures 1-3 by combining the characteristics of both the forward and flyback topologies shown in Figures 1 and 2, while resembling the topology of the CUK topology of Figure 3. However, subtle differences are now present in the subject invention which at first may not appear apparent but nevertheless are present and necessary for achieving an improved operation.

The subject invention does not utilize a capacitively coupled primary winding of the power transformer 14, but instead now employs a driving arrangement similar to that of a forward topology wherein energy is delivered to the output filter and transformer inductance or an equivalent inductor 21 (Figure 5)

thereof during the on-time (dT_S) of the switching transistor 16. The inductor 21 in effect comprises the transformer primary winding 12 reflected to the secondary side by the transformer turns ratio $N_1:N_2$.

The energy which is stored in the inductance L_1 of the transformer 14 or the inductor 21, however, is not dumped back to the input side, but instead is released to the secondary coupling capacitor (C_1) 42 during the off-time ($\bar{d}T_S$) of the transistor 16 and which is similar to the operation of a flyback topology. The topology of the subject invention is therefore termed a "forback" topology converter since it exhibits behavior of both the forward and flyback topologies alternately with dT_S and $\bar{d}T_S$ of the transistor switching period T_S.

A current sensing transformer 52 is connected in the secondary circuit as shown in Figures 4 and 5 to sense the current I_S flowing in the secondary circuit for controlling the duty cycle (d) of the switching transistor 16 in conjunction with the output voltage V_O across the load 26. The current sensing transformer 52 includes a primary winding 54 directly connected to the end of secondary winding 20 or inductor 21 opposite from the end which is directly connected to the capacitor (C_1) 42 so that the inductor currents flowing in the secondary circuit during the respective time intervals of dT_S and

$\bar{d}T_s$ can be detected. The secondary winding 56 of the sensing transformer 52 is connected to the duty cycle control circuit 18 for providing a feedback signal voltage V_s proportional to the secondary current I_s. The feedback control circuit 18 controls the duty cycle d of the transistor switch 16.

In addition to the specific location of the current sensing transformer 52, the methodology employed in the circuit design and hereinafter described, results in the inductance values of L_1 and L_2 being substantially equal.

These two last mentioned features result in a converter topology wherein a volt-second balance of the power transformer 14 and an amp-second balance of the current transformer 52 are achieved simultaneously. This will be more readily appreciated as the following detailed description of operation is considered.

Description of Operation

Referring now Figures 6-9, for the sake of simplicity Figure 6 is illustrative of the equivalent circuit for the non-isolated converter topology shown in Figure 5 during the on-time interval dT_s where the transistor switch 16 is conductive. Figure 7, on the other hand, is the equivalent circuit for Figure 5 during the off-time interval $\bar{d}T_s$ where the switch 16 is non-conductive.

The following operational conditions exist:

$$V_g = (N_2/N_1) \times V_{in} \quad (1)$$

$$V_o = V_{C1} = V_{C2} = (d/\bar{d}) \times V_g = (d/\bar{d}) \times (N_2/N_1) \times V_{in} \quad (2)$$

$$I_{L2}(avg) = I_o = V_{C2}/R_L = (d/\bar{d}) \times (N2/N1) \times (V_{in}/R_L) \quad (3)$$

$$I_{L2}(peak) = I_o + (V_o \times \bar{d} \times T_s)/2L_2 \quad (4)$$

$$I_{L1}(avg) = (d/\bar{d}) \times I_{L2}(avg) = (d/\bar{d})^2 \times (N_2/N_1) \times (V_{in}/R_L) \quad (5)$$

and

$$I_{L1}(peak) = (I_o/\bar{d}) - I_o + (V_o \times \bar{d} \times T_s)/2L_1 \quad (6)$$

It can be seen with reference to Figure 6 that during the on-time interval dT_s, wherein the semiconductor switch 16 is closed, the diode (D_1) 40, becomes reverse biased and is therefore considered an open circuit resulting in the equivalent circuit as shown. During this time, energy flows from V_g i.e. source 10' to inductor (L_1) 21, inductor (L_2) 22, and

capacitor (C_2) 24 and from capacitor (C_1) 42 to load resistor (R_L) 26.

Two currents flow during the dT_s interval, namely, I_{L1} and I_{L2}. The energy (E_{L1}) stored in the inductance (L_1) 21 increases from a minimum value to a maximum value according to the expressions:

$$E_{L1}(min) = 1/2\ L_1 \times I_{L1}^2(min) \qquad (7)$$

and,

$$E_{L1}(max) = 1/2\ L_1 \times I_{L1}^2(max) \qquad (8)$$

whereupon an increase in energy, ΔE_1, stored in inductor (L_1) 21 which can be expressed as:

$$\uparrow\Delta E_1 = 1/2\ L_1 \times [I_{L1}^2(max) - I_{L1}^2(min)] \qquad (9)$$

Accordingly, the current in inductor (L_1) 21 increases linearly from a minimum value to a maximum value as shown in Figure 8(a) by reference numeral 58.

The voltage applied to inductor (L_2) 22 is equal to $V_g + V_{C1} - V_{C2}$ or simply V_g whereupon the stored energy increases from a minimum value to a maximum value according to the expressions:

$$E_{L2}(min) = 1/2\ L_2 \times I_{L2}^2(min) \qquad (10)$$

and

$$E_{L2}(max) = 1/2\ L_2 \times I_{L2}^2(max) \qquad (11)$$

causing an increase in energy, ΔE_2, which can be expressed as:

$$\uparrow\Delta E_2 = 1/2\ L_2 \times [I_{L2}^2(max) - I_{L2}^2(min)] \qquad (12)$$

As a consequence, the current I_{L2} in the inductor 22 increases linearly from a minimum value to a maximum value as shown by reference numeral 60 in Figure 8(b).

With respect to the capacitor currents flowing during dT_s, the current out of capacitor (C_1) 42 is equal to I_{L2} and decreases from a maximum value to a minimum value as shown by reference numeral 62 of Figure 8(c) and is 180° out of phase with I_{L2} of Figure 8(b). The energy stored in capacitor (C_1) 42 also decreases from a maximum value to a minimum value according to the expressions:

$$E_{C1}(max) = 1/2\ C_1 \times V_{C1}^2(max) \qquad (13)$$

and

$$E_{C1}(min) = 1/2\ C_1 \times V_{C1}^2(min) \qquad (14)$$

whereupon the energy change, ΔE_3, stored in capacitor (C_1) 42 can be expressed as:

$$\downarrow\Delta E_3 = 1/2\ C_1 \times [V_{C1}^2(max) - V_{C1}^2(min)] \qquad (15)$$

The current entering the + terminal of capacitor (C_2) 24 is $I_{L2} - I_o$. An energy change, ΔE_4, which can be expressed as:

$$\uparrow\Delta E_4 = 1/2\ C_2\ [V_{C2}^2(max) - V_{C2}^2(min)] \qquad (16)$$

V_{C2} appears as the sinusoidal curve portion 64 shown in Figure 8(d) and changes from a minimum value to a maximum value as shown but is out of phase with I_{L1} and I_{L2} by an angle ϕ which is determined by the relative values of L_2, C_2 and R_L.

As a result of these interrelationships, the current I_S flowing through the primary winding 54 of the current sense transformer 52, is equal to I_{L2} and appears identical to the linear curve portion 60 of Fig. 8(b) as shown in Figure 9 by reference numeral 66.

Turning attention now to the off-time interval $\bar{d}T_S$, when the transistor switch 16 is non-conductive, the diode (D_1) 30 in Figure 5 becomes forward biased and can be considered a short circuit, resulting in an equivalent circuit as shown in Figure 7. While two loops are shown, it is done for purposes of illustration only, since the two conductors 68_a and 68_b shown thereat are in actuality a single current conducting path.

During the $\bar{d}T_S$ interval, energy flows from the inductor (L_1) 21 to the capacitor (C_1) 42. Simultaneously, energy is delivered to the load resistance (R_L) 26 from the inductor (L_2) 22 and the capacitor (C_2) 24. The current I_{L1} in the inductor (L_1) 21 decreases linearly from a maximum value to a minimum value as shown by reference numeral 70 in Figure 8(a). This results in a decrease in energy, ΔE_1, stored in inductor 21 (L_1) which can be expressed as:

$$\downarrow\Delta E_1 = E_{L1(max)} - E_{L1(min)} = 1/2\ L_1 \times [I_{L1}^2(max) - I_{L1}^2(min)] \qquad (17)$$

In a like manner, the current I_{L2} in the inductor

(L_2) 22 decreases linearly from a maximum value to a minimum value as shown by reference numeral 72 of Figure 8(b). A decrease in energy, ΔE_2, stored in inductor 22 (L_2) occurs which can be expressed as:

$$\downarrow \Delta E_2 = E_{L2}(max) - E_{L2}(min)$$
$$= 1/2\ L_2 \times [I_{L2}^2(max) - I_{L2}^2(min)] \qquad (18)$$

The current flow into capacitor (C_1) 42 increases non-linearly as shown by waveform 74 of Fig. 8(c) with an increase in energy storage, ΔE_3, which can be expressed as:

$$\uparrow \Delta E_3 = E_{C1}(max) - E_{C1}(min)$$
$$= 1/2\ C1 \times [V_{C1}^2(max) - V_{C1}^2(min)] \qquad (19)$$

The current flow out of capacitor (C_2) 24 is equal to $I_o - I_{L2}$ which produces the corresponding voltage waveform as shown in Fig. 8(d). The voltage V_{C2} lags the current, $I_o - I_{L2}$, by the phase angle ϕ as shown by reference numeral 76 of Figure 8(d). The corresponding change in energy storage may be expressed as:

$$\downarrow \Delta E_4 = E_2(max) - E_2(min)$$
$$= 1/2\ C_2\ [V_{C2}^2(max) - V_{C2}^2(min)] \qquad (20)$$

With respect to the current I_s in the primary winding 54 of the current sensing transformer 52, it comprises a current $-I_{L1}$ as indicated by reference numeral 78 of Figure 9.

Design Methodology

Regarding a physical implementation of the subject invention, the following method of circuit design would be followed so that among other things, but most importantly, $L_1=L_2$. Typically, a circuit designer would establish or would be provided with a set of initial or desired operational parameters, namely: output voltage V_o, switching frequency f_s, minimal input voltage $V_{in(min)}$, nominal input voltage $V_{in(nom)}$, maximum input voltage $V_{in(max)}$, minimum output load $R_{L(min)}$, nominal output load $R_{L(nom)}$ and maximum output load $R_{L(max)}$. For purposes of explanation, it should be noted that $R_{L(min)}$, for example, stands for maximum resistance in ohms, whereas $R_{L(max)}$ stands for minimum resistance in ohms.

One would then proceed to determine the turns ratio $N_1:N_2$ of power transformer 20, including the value of the inductance L_1, the inductance L_2, the capacitance C_1 and the capacitance C_2. This would then be followed by the design of the power transformer if necessary.

The first step involved is determining an acceptable duty cycle d, given the output voltage V_o, the range of the three input voltages V_{in} mentioned above, and by selecting the appropriate turns ratio $N_1:N_2$ for the transformer. The turns ratio $N_1:N_2$ should be selected such that the maximum duty cycle d_{max} should not exceed

a specified upper limit, typically 50% i.e. 0.5 T_s and should typically be in the range between 20% and 40% and from which the duty cycle d can be determined from aforementioned equation (2) as:

$$d = N_1V_o/(N_2V_{in} + N_1 \times V_o) \quad (21)$$

From this, the average current $I_{L2(avg)}$ in the output inductor 22, and in the transformer secondary $I_{L1(avg)}$, as shown in equations (3) and (5), can be calculated from the initial parameters established and equation (21) for minimum, nominal and maximum conditions.

Noting that one of the inventive features comprises a DC-to-DC converter where the values of L_1 and L_2 are equal, the value for L_2, i.e. the inductance value of the inductor 22, is determined first. This is based on three considerations: (1) the filter requirements of the output filter consisting of inductance (L_2) 22 and capacitor (C_2) 24; (2) the desirability of maintaining a continuous current conduction mode in L_2; and (3) the allowable current variation Δi of I_{L2} in the inductance (L_2) 22.

As to the output filter requirements, the voltage input to the LC filter comprised of inductor 22 and capacitor 24 is basically a square wave with a magnitude of:

$$V_{filt} = (N_2/N_1) \times V_{in} + V_{C1} \quad (22)$$

The worst case scenario exists when the largest peak-to-peak output ripple voltage across the load resistance (R_L) 26 occurs at $V_{in(max)}$, $d_{(min)}$, and $R_{L(max)}$. Thus,

$$V_{filt} = (N_2/N_1) \times V_{in(max)} + V_o \quad (23)$$

Accordingly, the attenuation in dB necessary to meet the ripple requirement is equal to:

$$20 \times \log [V_{o(ripple)}/V_{filt}] \quad (24)$$

The LC filter in this invention will have a -40dB/dec slope. Knowing this and the required attenuation at the switching frequency f_s, the filter corner frequency f_c is determined from the expression:

$$f_c = 1/(2\pi \sqrt{L_2C_2}) \quad (25)$$

Rearranging equation (24) yields:

$$L_2 = 1/[(2\pi f_c)^2 \times C_2] \quad (26)$$

Selection of a few trial values for C_2 is now made to allow one to determine one or more candidate values for L_2 which will satisfy the output filter requirements of equation (25). However, the actual value of L_2 will also depend on the other two considerations of maintaining continuous conduction mode and the allowable Δi percentage referred to above.

Since it is desirable to maintain a continuous conduction mode, then a critical minimum value of L_2 can be determined for which continuous conduction is maintained under the conditions of lightest load $R_{L(min)}$

and maximum input voltage $V_{in(max)}$. It can be shown that the minimum value of L_2 necessary to maintain continuous conduction mode under the lightest load and maximum input voltage condition exists where:

$$L_{2(min)} = [\bar{d}_{max} \times T_s \times R_{L(min)}] + 2 \qquad (27)$$

The value of the inductor (L_2) 22 dictates the slope of the current ramp as shown by the waveform segments 60 and 72 of Fig. 8(b). As a general rule, under a nominal input voltage $V_{in(nom)}$ and nominal output load $R_{L(nom)}$, Δi should remain no more than 25% of $I_{L2(Avg)}$.

In solving for L_2, it can be shown that the voltage across inductor 22 L_2 can be expressed as:

$$V_{L2} = L_2 \times \Delta i/\Delta t \qquad (28)$$

where $\Delta t = d_{nom} \times T_s$. Rearranging equation (28) results in L_2 being expressed as:

$$L_2 = (V_{L2} \times \Delta t)/\Delta i \qquad (29)$$

or

$$L_2 = (N_2 \times V_{in(nom)} \times d_{nom} \times T_s)/ (N_1 \times .25 \times I_{L2}) \qquad (30)$$

Accordingly, L_2 is selected on the basis of equations (26), equation (27) and equation (30). Having selected a value of L_2, the value of L_1 is now also determined. The appropriate value of capacitor 24 (C_2) is next determined from equation (26). The only

component left to be selected is the value for the capacitor 42 (C_1).

In the determination of the capacitance value for capacitor 42 (C_1), the value of C_1 is not as critical as the value of the other components. Preferably, capacitor 24 should be a polycarbonate or polystyrene low ESR capacitor. A 1μF polycarbonate capacitor, for example, is adequate for 100kHz designs where load currents are less than one ampere(amp).

As a general rule under nominal input voltage $V_{in(nom)}$ and load conditions $R_{L(nom)}$, the change of voltage Δv across C_1 should remain no more than 25% of V_o. During the on-time dT_s of the transistor switch 16 where Δv is selected to be 25% of V_o, C_1 can be calculated from the expression:

$$C_1 = (I_{L2(avg)} \times d_{nom} \times T_s)/(.25 \times V_o) \quad (31)$$

With the values for L_1, L_2, C_1 and C_2 being selected, it now becomes necessary to calculate the peak currents in both inductors (L_1) 21 and (L_2) 22 which can be achieved by use of equations (4) and (6), supra.

A knowledge of the values of L_1, $I_{L1(peak)}$, L_2, and $I_{L2(peak)}$ now provides all the information required for an actual design of the power transformer 14 when an embodiment such as shown in Figure 4 is desired. In designing the power transformer, the designer first

selects a trial core, then determines the minimum number of turns on the secondary winding (N_2) 20 followed by determining the required air gap.

In selecting a trial core, one makes a selection based upon the maximum desired flux density limit (B_m) under the worst case operating conditions, the effective area (A_e), relative permeability (μ_R) and effective core lengths (l_e).

The total reluctance (R_T) of both the core (R_c) and the air gap (R_g) can be determined from the expression:

$$R_T = (l_c + l_g \times \mu_R)/\mu_R A_e \quad (32)$$

from which the inductance L_1 in milliHenries can be determined from the expression:

$$L_{1(mH)} = (4\pi/R_T) \times (N_2/1000)^2 \quad (33)$$

From equation (33) the total reluctance R_T can be stated as:

$$R_T = (4\pi/L_{1mH}) \times (N_2/1000)^2 \quad (34)$$

It can be shown that the maximum flux density B_m can be expressed as:

$$B_m = I_{L1(peak)} \times L_{1(mH)} \times 1 \times 10^5 (A_e \times N_2) \quad (35)$$

from which N_2 can be obtained by rearranging equation (35) as:

$$N_{2(min)} = I_{L1(peak)} \times L_{1(mH)} \times 1 \times 10^5/(A_e \times B_m) \quad (36)$$

It is to be noted that N_2, the secondary winding 20 on the transformer 14, is the inductance L_1 in the equivalent circuit shown in Figure 5. Thus, equation 36 provides the minimum number of turns needed on the secondary winding 20 of the transformer 14 in order to keep from exceeding B_m at a value of $I_{L1(peak)}$. When desirable, larger values of N_2 are permissible, which results in a corresponding reduction in B_m.

Now that both N_2 and L_1 are known, an air gap is determined such that the required relationship between these two parameters N_2 and L_1 for a given core is achieved. Keeping in mind equations (32)-(34), the combined length l_g of the air gap and the length l_c of the core can be expressed as:

$$l_c + l_g \times \mu_R = R_T \times \mu_R \times A_e = (4\pi \times \mu_R \times A_e)/L_1(mH) \times (N_2/1000)^2 \quad (37)$$

At this point, the relationship between the effective length l_e, the length of the core l_c and the length of the air gap l_g must be specified according to the geometry of the core. For example, for a torroid, this can be expressed in centimeters(cm) as:

$$l_g(cm) = X/Y \quad (38)$$

where,

$X = [4\pi \times \mu_R \times A_e \times N_2^2]/[10^5 \times L_1(mH)] - l_e$, and

$Y = \mu_R - 1$

Following the resolution of an acceptable value of N_2, the value of N_1 is known from above where the selection of N_1:N_2 turns ratio is selected to provide an acceptable duty cycle.

Due to the flyback characteristic of this topology, it is essential to optimize the coupling between the primary and secondary windings 12 and 20 of the transformer 14 and therefore in addition to minimizing the number of turns for both N_1 and N_2, the winding should be bifilar wound if possible.

Thus what has been shown and described is an improved topology and methodology for the implementation of a current mode control pulse-width modulated DC-to-DC converter which automatically provides simultaneous volt-second balance of the power transformer and amp-second balance of the current sensing transformer simply and expeditiously.

Having thus shown and described what is at present considered to be the preferred embodiments of the invention, it should be noted that the same has been made by way of illustration and not limitation. Accordingly, all modifications, alterations and changes coming within the spirit and scope of the invention as defined by the appended claims are herein meant to be included.

ABSTRACT

A pulse-width modulated DC-to-DC power converter including a first inductor, i.e. a transformer or an equivalent fixed inductor equal to the inductance of the secondary winding of the transformer, coupled across a source of DC input voltage via a transistor switch which is rendered alternately conductive (ON) and non-conductive (OFF) in accordance with a signal from a feedback control circuit. A first capacitor capacitively couples one side of the first inductor to a second inductor which is connected to a second capacitor which is coupled to the other side of the first inductor. A circuit load shunts the second capacitor. A semi-conductor diode is additionally coupled from a common circuit connection between the first capacitor and the second inductor to the other side of the first inductor. A current sense transformer generating a current feedback signal for the switch control circuit is directly coupled in series with the other side of the first inductor so that the first capacitor, the second inductor and the current sense transformer are connected in series through the first inductor. The inductance values of the first and second inductors, moreover, are made identical. Such a converter topology results in a simultaneous volt-second balance in the first inductance and ampere-second balance in the current sense transformer.

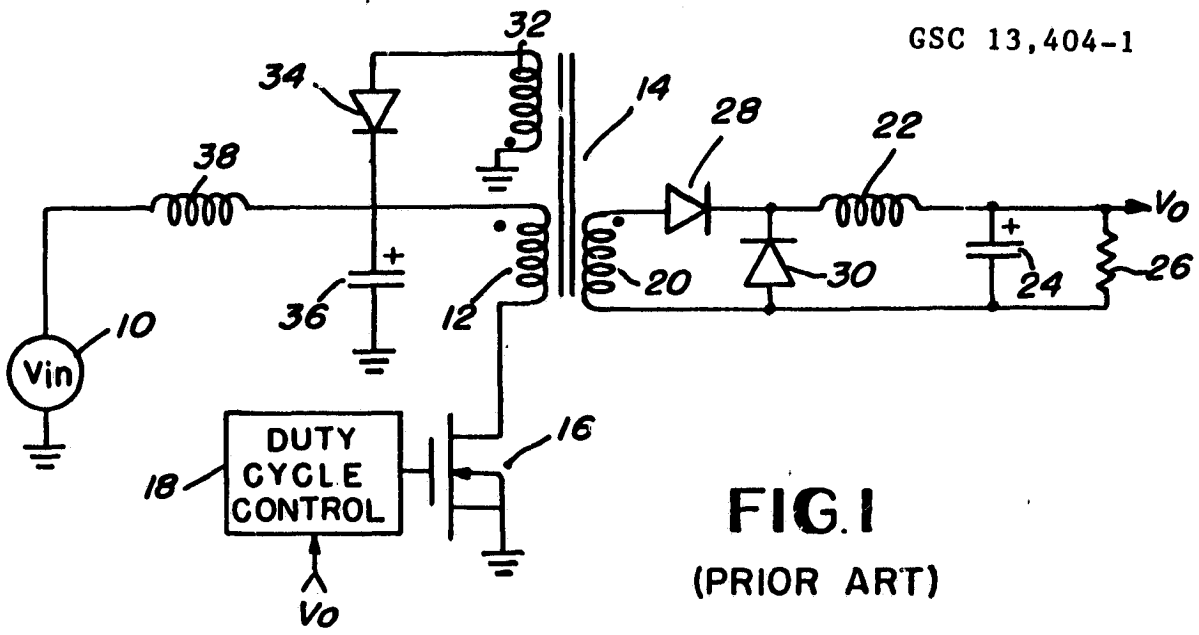

FIG. 1
(PRIOR ART)

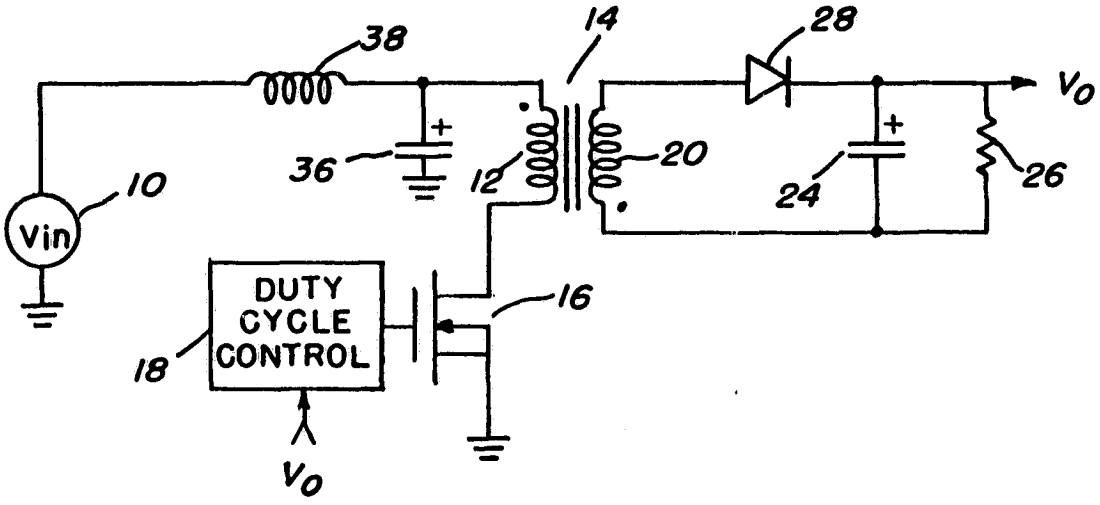

FIG. 2
(PRIOR ART)

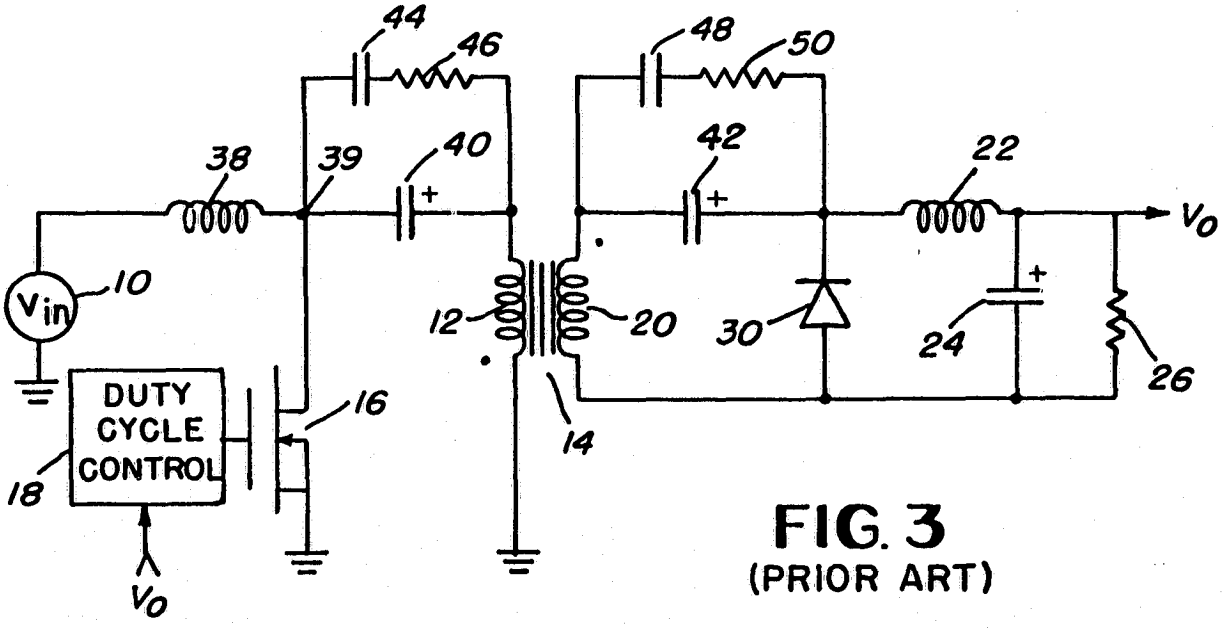

FIG. 3
(PRIOR ART)

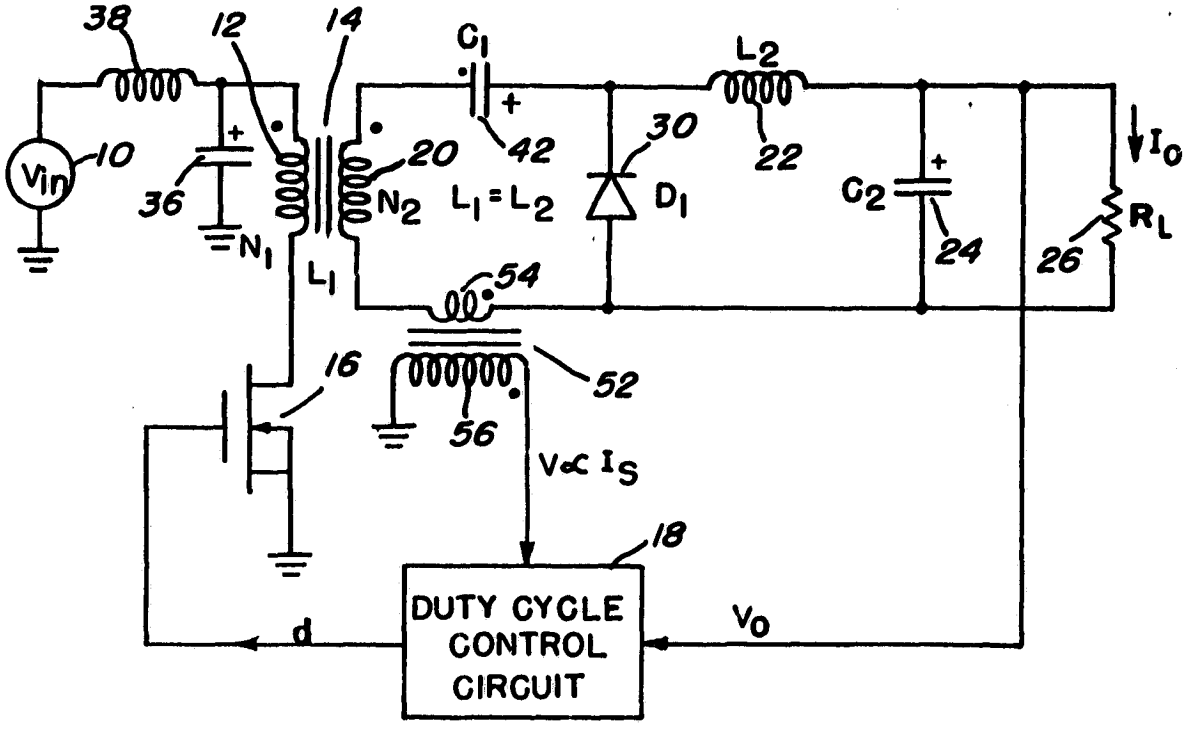
38
12
14
C1
L2
Vin
10
36
N1
20
N2
L1=L2
D1
30
22
C2
24
26
RL
Io
L1
54
16
52
56
V∝Is
18
DUTY CYCLE CONTROL CIRCUIT
d
Vo

FIG. 4

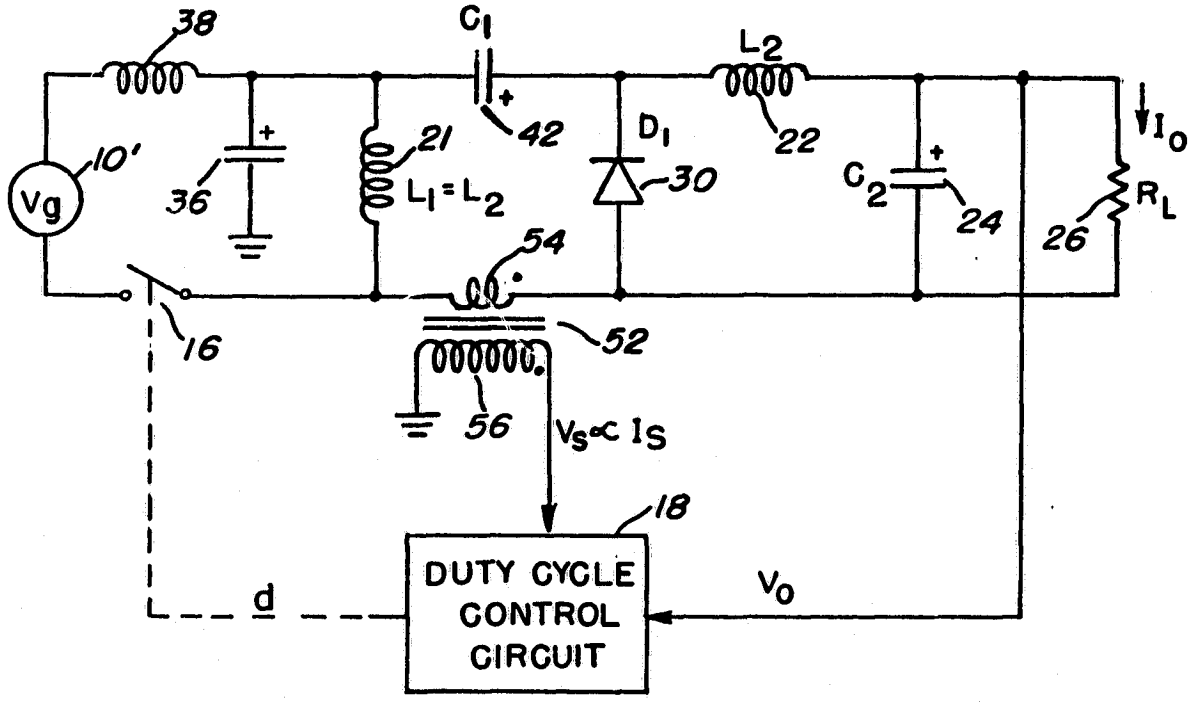
38
C1
L2
10'
Vg
36
21
L1=L2
42
D1
30
22
C2
24
26
RL
Io
54
16
52
56
Vs∝Is
18
DUTY CYCLE CONTROL CIRCUIT
d
Vo

FIG. 5

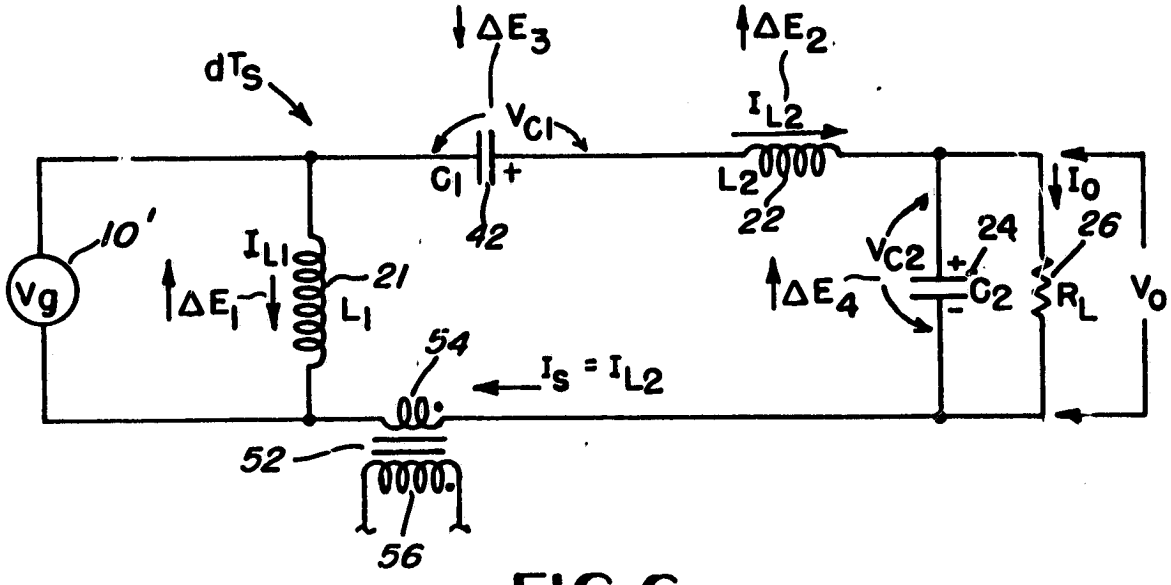

FIG. 6

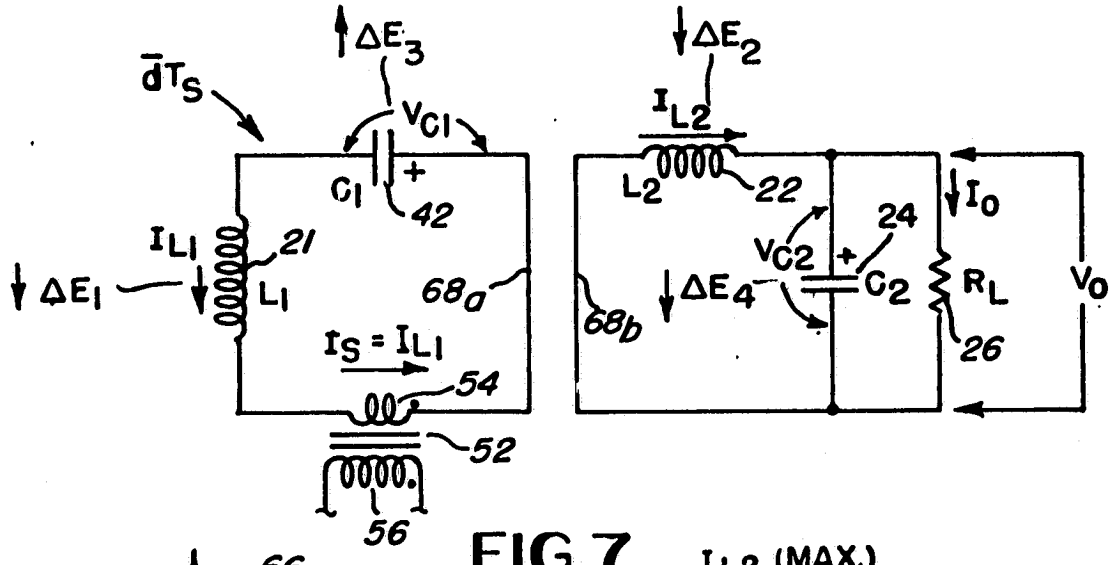

FIG. 7

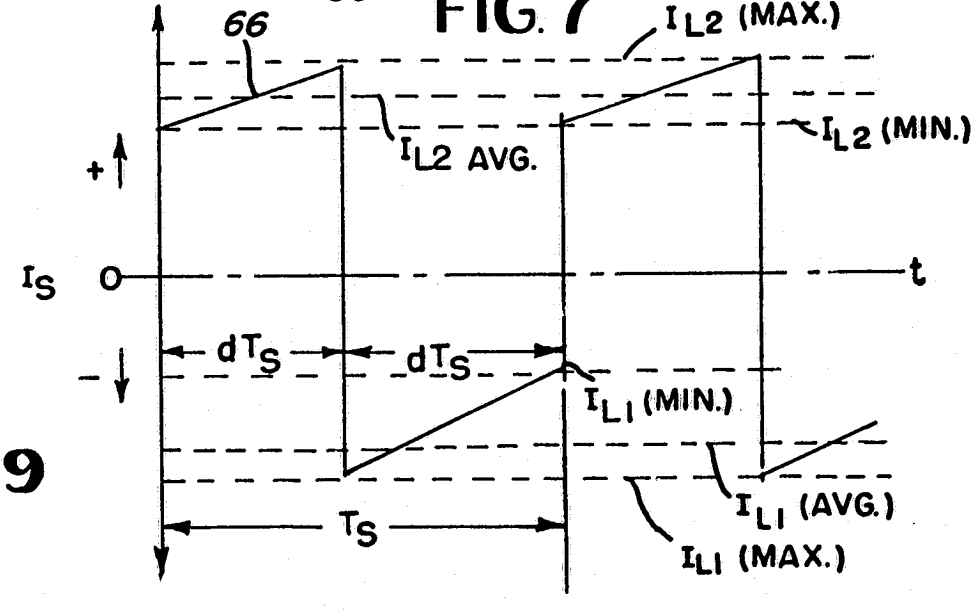

FIG. 9

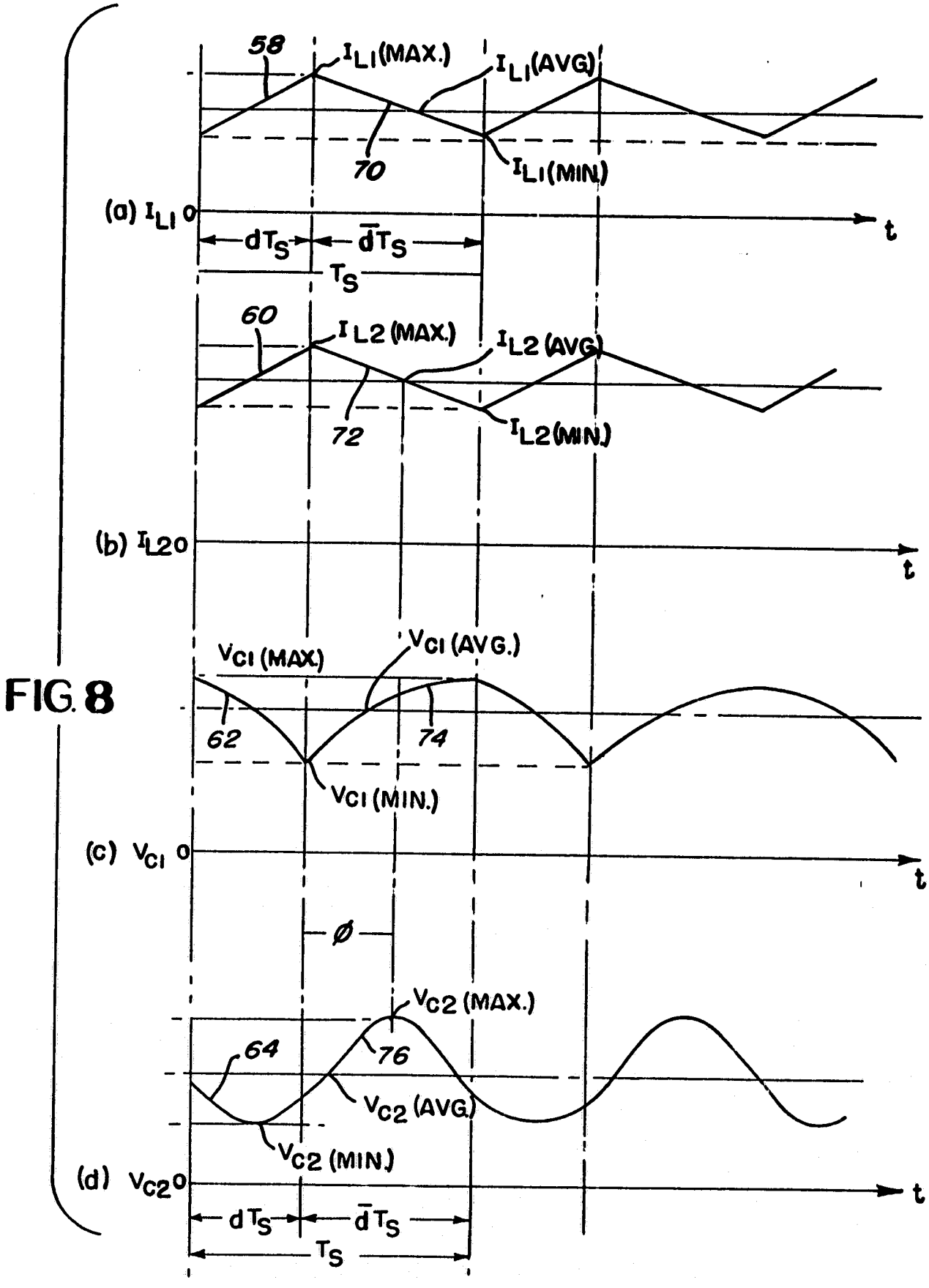
58
$I_{L1(MAX.)}$
$I_{L1(AVG)}$
70
$I_{L1(MIN)}$
(a) I_{L1} 0
t
dT_S
$\bar{d}T_S$
T_S
60
$I_{L2(MAX.)}$
$I_{L2(AVG)}$
72
$I_{L2(MIN.)}$
(b) I_{L2} 0
t
$V_{C1(MAX.)}$
$V_{C1(AVG.)}$
62
74
$V_{C1(MIN.)}$
(c) V_{C1} 0
t
ø
$V_{C2(MAX.)}$
64
76
$V_{C2(AVG)}$
$V_{C2(MIN.)}$
(d) V_{C2} 0
t
dT_S
$\bar{d}T_S$
T_S

FIG. 8