Single Phase Dynamic CMOS PLA Using Charge Sharing Technique

Y.B Dhong and C.P Tsang

The Department of Computer Science
The University of Western Australia
Nedlands, WA 6009, Australia

Abstract: **This paper presents single phase dynamic CMOS *NOR-NOR* PLA using triggered decoders and charge sharing techniques for high speed and low power. By using the triggered decoder technique, the ground switches are eliminated, thereby making this new design much faster and lower power dissipation than conventional PLAs. By using the charge-sharing technique in a dynamic CMOS NOR structure, a cascading AND gate can be implemented. The proposed PLAs are presented with a delay-time of 15.95 and 18.05 nsec, respectively, which compare with a conventional single phase PLA with 35.5 nsec delay-time. For a typical example of PLA like the Signetics 82S100 with 16 inputs, 48 input minterms (m) and 8 output minterms (n), the 2-SOP PLA using the triggered 2-bit decoder is 2.23 times faster and has 2.1 times less power dissipation than the conventional PLA. These results are simulated using maximum drain current of 600 μA, gate length of 2.0 μm, V_{DD} of 5 V, the capacitance of an input minterm of 1500 fF, and the capacitance of an output minterm of 1500 fF.**

1 Introduction

CMOS technology has become a vital technology for VLSI because of its high density and low power dissipation. However, it suffers from low speed due to its inherent parasitic capacitance. Thus high-speed CMOS techniques have been vigorously researched. With high speed CMOS it would be possible to implement real-time digital signal-processing applications. As a result, an advanced CMOS technology is expected to remain at the forefront of VLSI technology for many years to come. The problem in designing VLSI systems is of enormous complexity. This problem can be partially simplified by using the more general design principle of a PLA which provides a regular structure. PLAs are also attractive to the VLSI designer because their structure requires a minimum number of separate cell designs, and allows for ease in testing while offering the opportunity for simple, rapid expandability [2].

The delay-time of a dynamic CMOS NOR gate increases very slowly with increasing number of inputs [7]. By cascading two stages of multi-input NOR gates, any desired Boolean function of the input variables can be generated. A CMOS dynamic PLA makes use of these two properties. In CMOS technology the use of PLAs has continued, mainly for regularity of layout and ease of code modification [6]. PLA-based nMOS processors

are superior in power dissipation to random-logic based machines by a significant margin, although they are slightly larger in area [1]. Dynamic CMOS PLAs are often used to generate state vectors for lower power microprocessors rather than nMOS PLAs. However, the use of ground switches and multiple phases reduces the speed of PLA using conventional dynamic CMOS technology [7,8].

The fastest conventional single phase dynamic CMOS *NOT-NOR-NOR-NOT* PLA has large noise spikes at the floating nodes [3,4]. Hence, a four phase dynamic CMOS *NOT-NOR-NOR-NOT* PLA [8] is commonly adopted. The problem of this four phase scheme is that complex clocks must be generated to drive the dynamic logic circuits. This also reduces speed and requires larger interconnection area. A low-power *NAND-NOT-NOR-NOT* PLA using a simplified addressing scheme is proposed with 244 ns per instruction for a signal processor in paper [4].

In this paper, a family of PLAs using triggered decoders and charge sharing techniques is proposed. They are single phase dynamic CMOS *NOT-NOR-NOR-NOT* PLAs in a sum of products (SOP), called SOP PLA, using 1-bit and 2-bit triggered decoders, respectively. By using the charge sharing technique for the implementation of cascaded AND array in NOR structures, and the triggered input technique for the deletion of ground switches, these PLAs are faster and require lower power dissipation than the conventional single phase dynamic CMOS *NOT-NOR-NOR-NOT* PLA. By using triggered 2-bit decoders on the input during the precharge time, the capacitances of an input minterm of a PLA can be minimized to reduce power [5,6]. Therefore, it is possible to make a faster PLA employing the triggered input decoder circuits and the charge sharing technique.

2 Dynamic Single Phase CMOS PLA

CMOS PLA operations may be divided into two classes: pseudo-nMOS and dynamic CMOS. Advantages of the pseudo-nMOS PLAs include simplicity and small area. Disadvantages are due to the static power dissipation. The dynamic CMOS PLAs generate less power and ground noise than the pseudo-nMOS PLAs. The pseudo-nMOS PLAs are faster than dynamic CMOS PLAs, but for large PLA layouts the power dissipation is excessive, thus forcing the designer to go to dynamic CMOS.

A modified schematic of a conventional single phase dynamic CMOS *NOT-NOR-NOR-NOT* PLA [3] is shown in Figure 1. This PLA is known to be the fastest [4], but at the expense of the cost of wasted power. The ground switches are charged and discharged every cycle. They connect the sources of all the AND array input transistors, and for layout compactness are built in diffusion. This results in a high capacitance of the order of tens of picofarads. For larger minterms, the additional capacitance of the ground switches is significant.

2.1 Triggered Input Logic for Dynamic CMOS Logic

Dynamic CMOS circuits have higher speed and lower chip area than the conventional

static CMOS logic. However, it can only implement noninverting functions. This is because every Domino CMOS gate has to be followed by an inverter and the output of any dynamic CMOS gate cannot be fed directly to another gate. It is possible to avoid this problem by using a triggered 1-bit decoder.

Let us assume that every dynamic triggered 1-bit signal (a, a') is reset to (0,0) during the precharge period. A triggered 1-bit decoder signal as a two-valued "one" signal A is represented as $(1,0)$, and the corresponding two-valued "zero" signal A as $(0,1)$ during the evaluate period. For example, a two-valued static signal A can be represented as a triggered 1-bit decoder signal (a, a') using a two-variable two-valued signal with three states, as shown in Table 1.

Figure 2 shows a triggered 1-bit decoder for dynamic CMOS logic circuits. It consists essentially of a general signal a and its complementary signal a'. During the precharge time ($\bar{\phi} = 1$), n-devices (2,6) are on to be precharged to low at the outputs (a and a'), and p-devices (1,5) are off, so the output signals are low, and p-device (3) and n-device (4) together run as an inverter. During the evaluate time ($\bar{\phi} = 0$), when n-devices (2,6) are off and p-devices (1,5) are on, the values of drains of p-devices (1,5) can be transferred at the outputs a and a'. Only the logic values of drains in p-devices (1,5) can be transferred to the outputs respectively, because the outputs a and a' are low initially during the evaluate time ($\bar{\phi} = 0$). In order to make the same rise time of both a complementary signal a' and a general signal a of any input signal, the channel width of p-device 3 must be designed to be larger than that of n-device 4. This decreases the delay-time of input signals at the beginning of the evaluation time.

Figure 3 shows a triggered 2-bit decoder for input signals of a dynamic CMOS PLA. A 2-bit decoder decodes a 2-bit number into 4 output signals. In our case, during precharge time the decoder output signals are set to all "one" or all "zero" depending on the SOP or POS types, respectively. The n-device (14) and the p-device (6) together run as $\bar{A}B$ gate. This saves power dissipation and improves speed in dynamic CMOS PLA. This is because the number of input nodes is reduced by half leading to reduction of the the capacitance of input nodes. If the node N_1 is high, the node N_2 is low, the node N_3 of the drain of p-device (4) is low, and the node N_4 of the gate of n-device (4) is low during precharge time, then the node N_1 becomes low with threshold voltage and slow speed. However, because the node N_2 is low during the precharge time, the transfer of logic "1" only occurs through p-devices (4,5) to the node N_2 with high speed during the evaluation time. During the precharge time the n-devices (13,15,17,19) work as the ground switches in the front array part of PLAs, because they set all input signals of the front array part to "zero". In the case of SOP PLA (see next section), all input signals in the front array part are set to "one" during the precharge time. In this way, these triggered decoder circuits allow the input of static CMOS signals in a dynamic CMOS PLA.

2.2 Design of a Single Phase Dynamic CMOS SOP PLA

The schematic of a single phase dynamic CMOS *NOT-NOR-NOR-NOT* sum of product (SOP) PLA using triggered 1-bit decoders is shown in Figure 4. This SOP PLA consists

of triggered 1-bit decoders, the AND array, buffers, and the OR array.

The triggered 1-bit decoder consists of inverters (such as 1), the p-devices loads (such as 4,6) as the ground switches in the AND (front part) array, and functional n-device switches (such as 3,5). The n-device (3) acts as the switch for a general signal and the n-device (5) acts as the switch for a complementary signal.

The AND array consists of loads (such as p-device 11,12), switches (such as n-device 15,16) as the ground switches in the OR (next part) array, and functional switches (such as n-device 19,20) with no ground switch. A conventional dynamic CMOS logic system in two-valued logic using two-variable two-valued logic must use ground switches to prevent a discharge path during precharge time. However, by using triggered 1-bit decoder logic, ground switches are not needed. Thus this reduces power dissipation and improves speed through the omission of the ground switch. Furthermore, the triggered 1-bit decoders set all input signals in the AND array to high and all input signals in the OR array to low during precharge time. In this way, the triggered decoder concept is suitable for a dynamic CMOS PLA system.

Charge sharing is usually a problem in the design of dynamic CMOS AND gates. However, the proposed NOR gates which use charge sharing techniques are suitable for the implementation of the AND array. This charge sharing technique in the AND array overcomes the difficulty of cascading single phase dynamic CMOS gates without the ground switches. All inputs are assumed stable before the evaluation time. During precharge time, when the loads (such as 11,12) are precharged, the input load nodes (such as N_1) are charged to high, and all of minterm nodes (such as N_2) in AND array are discharged to low because all triggered 1-bit decoder signals are high. When the clock goes high for the evaluation, all loads of input minterms are turned off and the minterm switches n-device (such as 15,16) are turned on. Evaluation paths will exist through the AND array input devices according to the state of the inputs. During evaluation time, the output of the AND array will conditionally charge to high if only all inputs in the minterm of the AND array are high. This keeps all minterm lines to virtual ground except the selected ones, which have all input transistors connected to them turned off with all existing charges remaining shared. These AND gates work as *NOT-NOR* gates. Also, a minimum capacitance ratio value of C_{N_1}/C_{N_2} of 2:1 is required, where C_{N_1} is the capacitance of the node N_1 and C_{N_2} is the capacitance of the node N_2.

The speed of the AND array depends on the minterm switches (such as 15,16), and their maximum drain current depends on the n-device (such as 19,20) and the n-device (such as 15,16). Thus in the range of the maximum drain current (600 μA) we can increase slightly more the width of the n-devices (15,19) to 6.5 μm, to improve speed over that of a conventional CMOS PLA of 4 μm. Figure 5 shows the simulated waveforms of internal nodes. If A and B are low, V_4 is ϕ signal as the input trigger voltage, V_{12} is the voltage of NOR gate using charge sharing at the selected node N_3, and V_{13} is the pumping voltage at the unselected node N_2.

Figure 6 shows the simulated waveforms of selected internal nodes. V_2 is the selected output voltage at O', V_4 is ϕ signal as the input trigger voltage, V_{12} is the voltage at the

selected AND array node N_3 and its steady state voltage is the same as $C_{N_1}V_{DD}/(C_{N_1} + C_{N_2})$, and V_{16} is the voltage at the selected OR array node N_5 if A and B are low.

Figure 7 shows the relationship between the pumping voltage and the width ratio. This PLA was simulated using SPICE3d1 based on the channel width of the n-device 15 (W_{15}) at 6.5 μm, and that of the n-device (19) (W_{19}) at 6.5 μm. Although the channel width ratio w increases linearly with speed, it demands the increase of the pumping voltage with a decrease in the noise margin. Thus in order to prevent the incorrect operation resulted from pumping phenomena (*i.e.*, a reduction of the noise margin) at the nodes (such as N_2) during the evaluation time, and to keep the virtual ground, an optimal channel width ratio W_{15}/W_{19} of 1:1 can be used. Therefore, to make a minimum pumping voltage, the optimal width ratio w has "one" and in the worst case only, one input of the multi-input AND gate is high.

Figure 8 shows a dynamic CMOS buffer using a one-way NOR gate.. The width of the n-device (1) must be designed to be shorter (5 μm) to prevent the discharge by the pumping voltage relative to the ground switch (15 μm). In buffers, the first NOR buffers (such as 35,36) should be designed so that the logic threshold value of the NOR buffer is a lower value than $V_{DD}/2$. This measure improves the speed. These buffers can be used to improve speed because the node N_2 has larger capacitance due to many input variables. The rising time of an input minterm depends predominantly on the resistance of the n-device (15). Some delay will be incurred due to the finite pull-up time. The inverters (43,44) are used for synchronizing the load signal with the triggered decoder signals in input minterms. This AND array using the charge sharing technique does not require the input tracking lines in the SOP PLA.

The OR array consists of loads (such as p-device 31,32), inverters (such as 33,34), and functional switches (such as n-device 27,28) with no ground switch. Charge is dissipated only in the selected output lines themselves. The power dissipation in the OR array is minor compared to the AND array.

By using triggered 2-bit decoders on the input during the precharge time, a number of input minterms of a PLA can be minimized to reduce power and to improve speed. Therefore, it is possible to make a faster PLA with no ground switch. This SOP PLA is suitable for the implementation of the dynamic CMOS PLA which has a lower number of the AND array minterms and a greater number of the OR array minterms.

3 Simulation Results and Conclusions

To compare the performance of the single phase dynamic CMOS PLAs, each of the PLAs described in previous sections was simulated using SPICE3d1. The simulated waveforms of the various single phase dynamic CMOS PLA are shown in Figure 9 and 10. The input waveforms are V(35) and V(4), and the output waveforms of the front array are V(26) and V(16). the output waveforms are V(3) and V(2) in Figure 9 and Figure 10, respectively. In simulation, the drain maximum current of 600 μA in the input functional n-device is used, the gate length is 2.0 μm, the V_{TO} of n-device is 0.71 V, the V_{TO} of

p-device is 0.80 V, the drain capacitance C_D in the n-device is assumed 11.43 fF, the gate capacitance C_G in the n-device is assumed 2.9 fF, V_{DD} is 5 V, the node number of an input minterm is 130 with 1.5 pF capacitances, and the node number of an output minterm is 130 with 1.5 pF capacitances.

Table 2 shows a comparison of simulation results for various single phase CMOS PLA types, where both the input minterm and the output minterm are assumed to have the same capacitance, the number of input minterms is m and the number of output minterms is n. T_f is the delay-time of the front array of a PLA and P_f is the normalized average power of the front array of a PLA. T_b is the delay-time of the back array of a PLA and P_b is the normalized average power of the back array of a PLA. T_t is the total delay-time of a PLA and P_t is the total normalized average power of a PLA. The worst case total delay time of a conventional single phase dynamic CMOS PLA is 35.5 ns. The SOP PLA using the triggered 1-bit decoder and the 2-SOP PLA using the triggered 2-bit decoder are 2 and 2.23 times faster, respectively, than the conventional CMOS PLA.

The normalized average power can be considered as the total charges in a minterm. The front array in the conventional PLA has the number of average selected minterms of $\frac{m}{2}+1$, where the "1" is the input tracking line. The back array has the number of average selected minterms of $\frac{n}{2}$. The "5" is the charge of a minterm and the "4" is the charge of a ground switch. The proposed AND array using charge sharing technique in the SOP PLA has the number of average selected minterms of $\frac{m}{2}$ and $\frac{n}{2}$, respectively. The selected minterm has wasted $\frac{10}{3}$ normalized charge and the unselected minterm has wasted 10 normalized charge. The charge of the front array in the 2-SOP PLA is a half charge of that in the SOP PLA because of using the triggered 2-bit decoders. Thus the proposed PLA structures are faster and require lower power dissipation than the conventional single phase dynamic CMOS *NOT-NOR-NOR-NOT* PLA, because of the elimination of the ground switch. For a typical example of PLA like the Signetics 82S100 with 16 inputs, 48 input minterms (m) and 8 output minterms (n), the 2-SOP PLA using the triggered 2-bit decoder is 2.23 times faster and has 2.1 times less power dissipation than the conventional PLA. Therefore, the proposed 2-SOP PLA using the triggered 2-bit decoder is a faster dynamic CMOS PLA, and this PLA has no input tracking line.

References

[1] P. Cook, C.W. Ho, and S. Schuster. A study in the use of PLA based macros. *IEEE Journal Solid-State Circuits*, SC-14:833–840, October 1979.

[2] Eugene D. Fabricius. *Introduction to VLSI Design.* McGraw-Hill in Electrical Engineering:New York, 1990.

[3] D. Hodges and H. Jackson. *Analysis and Design of Digital Integrated Circuits.* McGraw-Hill: New York, 1983.

[4] Alfredo R. Linz. A low-power PLA for a signal processor. *IEEE Journal of Solid-State Circuits*, 26(2):107–115, February 1991.

[5] F.J. Pelayo, A. Prieto, A.Lloris, and J. Ortega. CMOS current-mode multivalued PLA's. *IEEE Trans. on Circuits and Systems*, 38(4):434–441, April 1991.

[6] Tsutomu Sasao. On the optimal design of multiple-valued PLA's. *IEEE Trans. on Comp.*, 38(4):582–592, April 1989.

[7] Masakazu Shoji. *CMOS Digital Circuit Technology.* Computer System. Prentice Hall, Englewood Cliffs, New Jersey, Computing Science Research Center AT&T Bell Laboratories, 1988.

[8] Neil Weste and Kamran Eshraghian. *Principles of CMOS VLSI Design A Systems Perspective.* The VLSI Systems Series. Addison-Wesley, Massachusetts, 1985.

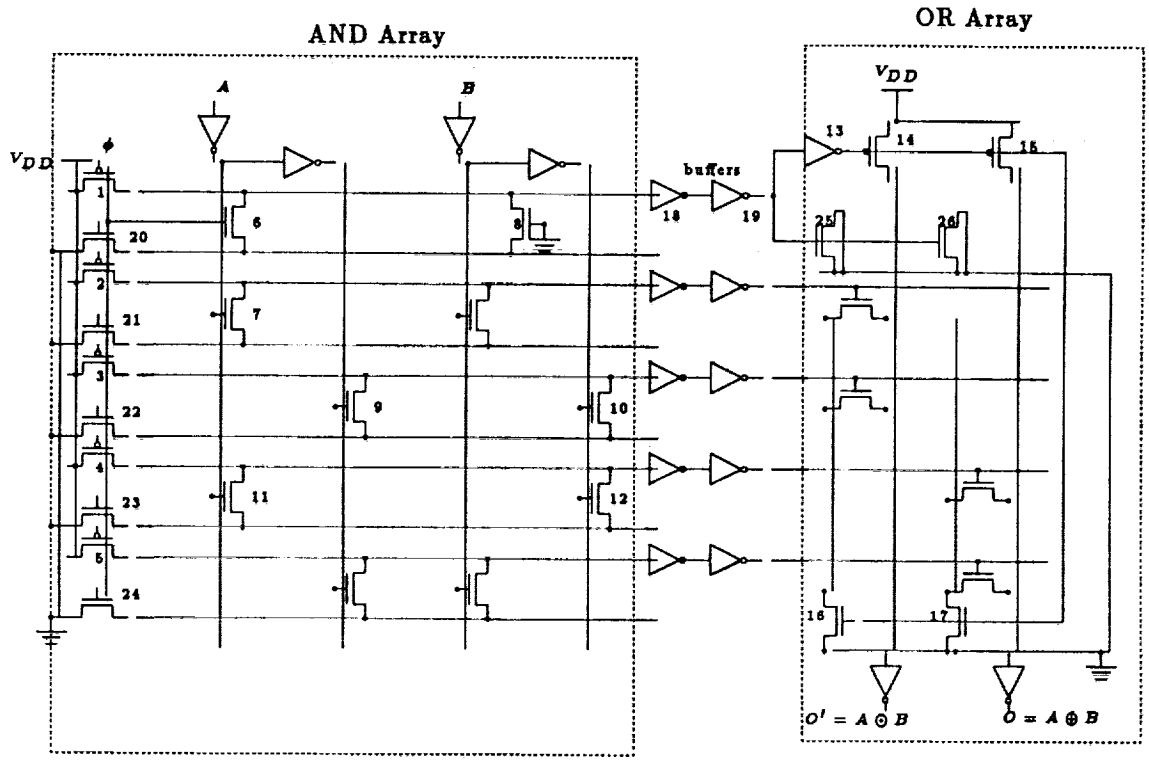

Figure 1: Conventional single phase *(NOT-NOR)-(NOT-NOT)-(NOR-NOT)* PLA

Time	*1-bit signal*	*triggered 1-bit decoder signal*			
	A	a	a'	$\bar{a}$	$\bar{a}'$
precharge	*	0	0	1	1
evaluate	0	0	1	1	0
	1	1	0	0	1

Table 1: Encoding a 1-bit signal into a triggered 1-bit decoder signal using a two-variable two-valued signal in a dynamic CMOS logic system

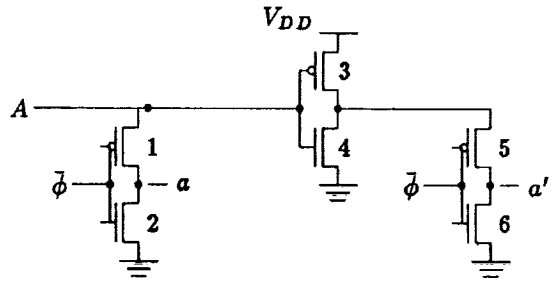

Figure 2: CMOS implementation of a triggered 1-bit decoder for dynamic CMOS logic circuits

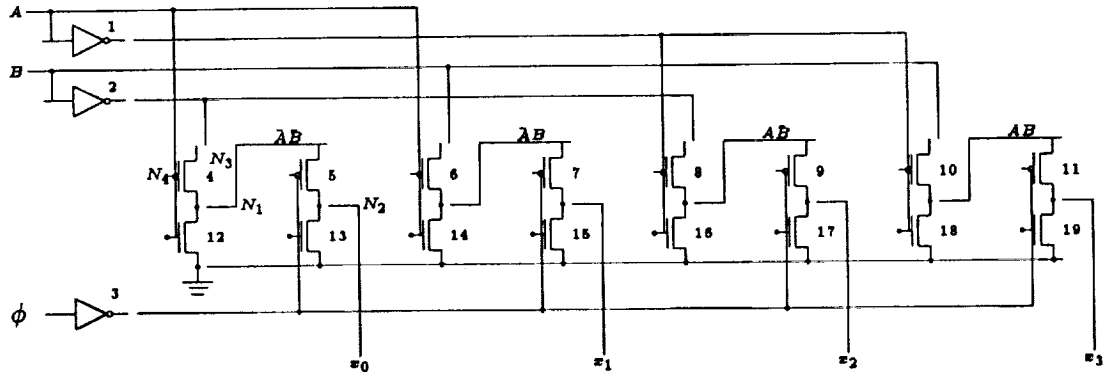

Figure 3: Static CMOS implementation of a triggered 2-bit decoder

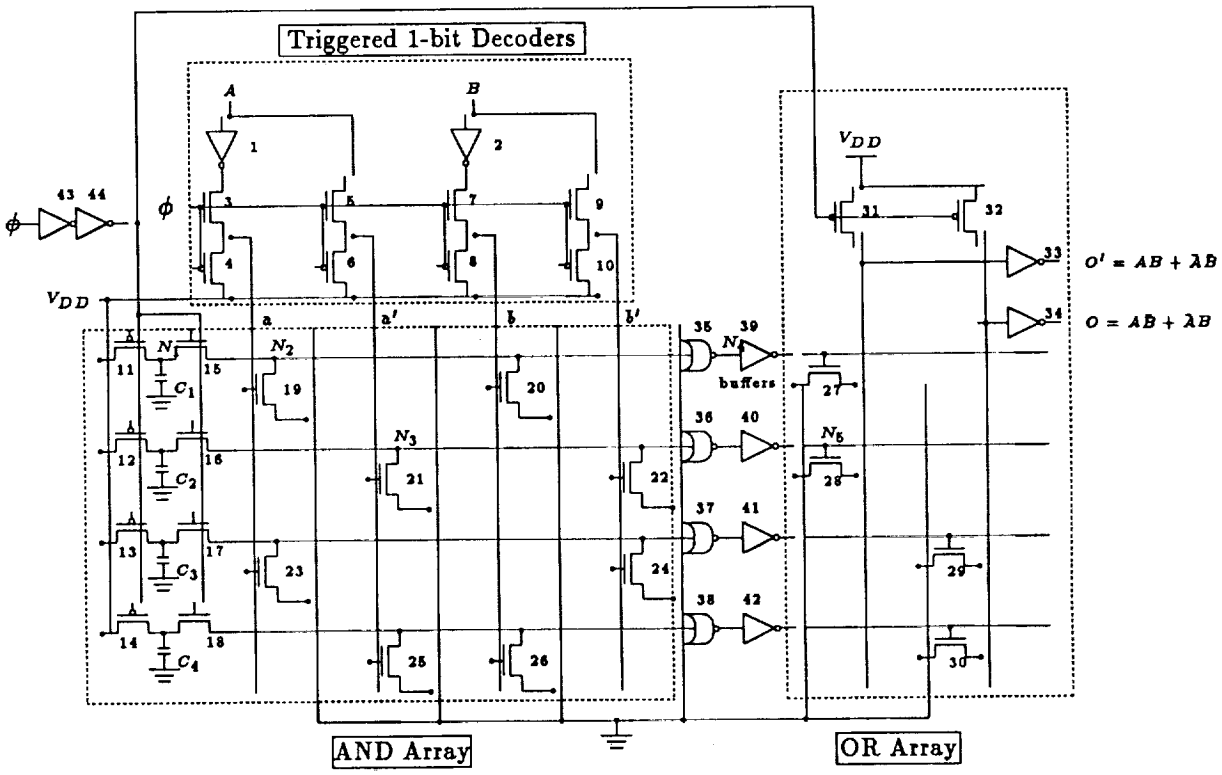

Figure 4: Single phase dynamic CMOS *(NOT-NOR)-(NOT-NOT)-(NOR-NOT)* PLA in a sum of products (SOP) using triggered 1-bit decoders

Techniques	$T_f(ns)$	P_f	$T_b(ns)$	P_b	$T_t(ns)$	P_t
Conventional	17.75	$(\frac{m}{2}+1)5+(m+1)4.3$	17.75	$\frac{n}{2}\cdot 5+4.3n$	35.5	$6.8m+6.8n+9.3$
SOP	10.55	$\frac{m}{2}10+\frac{m}{2}\cdot\frac{10}{3}$	7.5	$\frac{n}{2}\cdot 5$	18.05	$6.7m+2.5n$
2-SOP	8.45	$\frac{m}{2}5+\frac{m}{2}\cdot\frac{5}{3}$	7.5	$\frac{n}{2}\cdot 5$	15.95	$3.3m+2.5n$

Table 2: Comparison of simulation results for various single phase CMOS PLA types

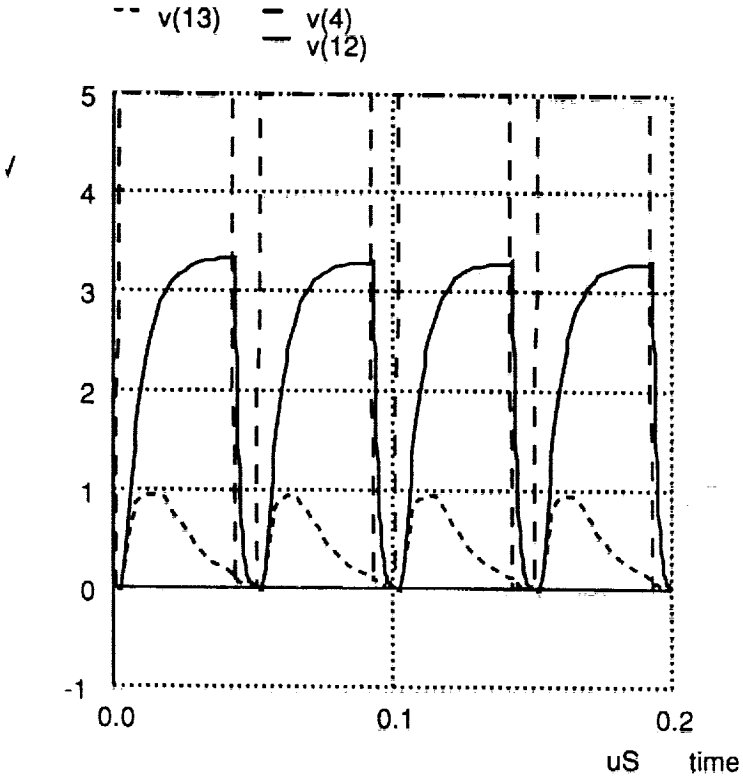

Figure 5: Simulated waveforms of internal nodes

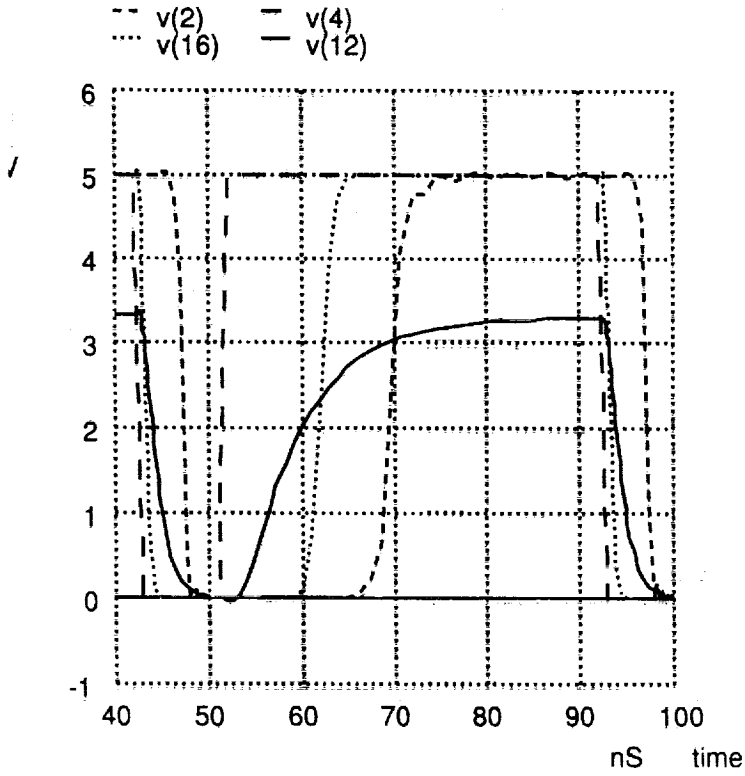

Figure 6: Simulated waveforms of internal selected nodes in a single phase dynamic CMOS SOP PLA using the triggered 1-bit decoder

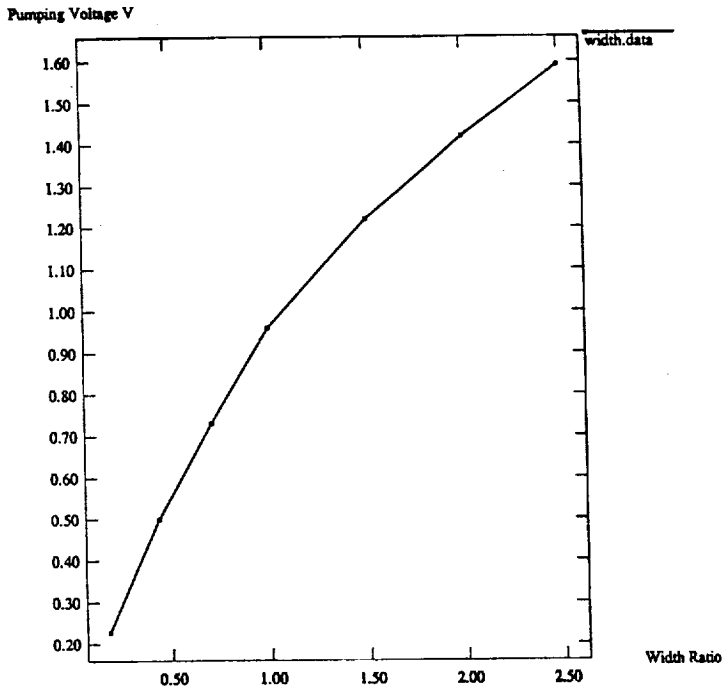

Figure 7: Simulated pumping voltage versus channel width ratio $w = W_p/W_n$

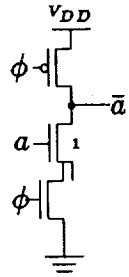

Figure 8: Dynamic CMOS buffer using an one-way NOR gate

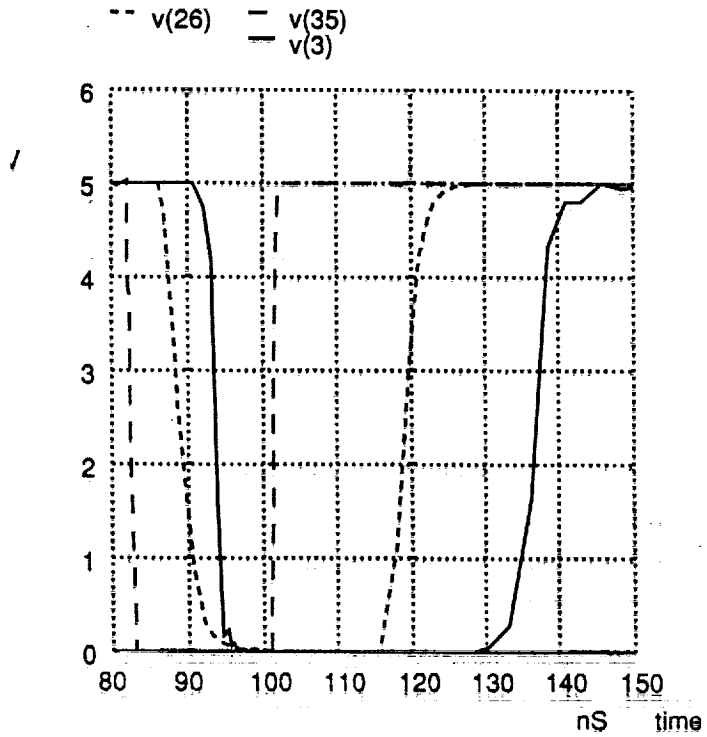

Figure 9: Simulated waveforms of a conventional single phase dynamic CMOS PLA. V_{35} is the triggered voltage of ϕ, V_3 is the output voltage at the node O', and V_{26} is the output voltage of the AND array at the gate of p-device (14)

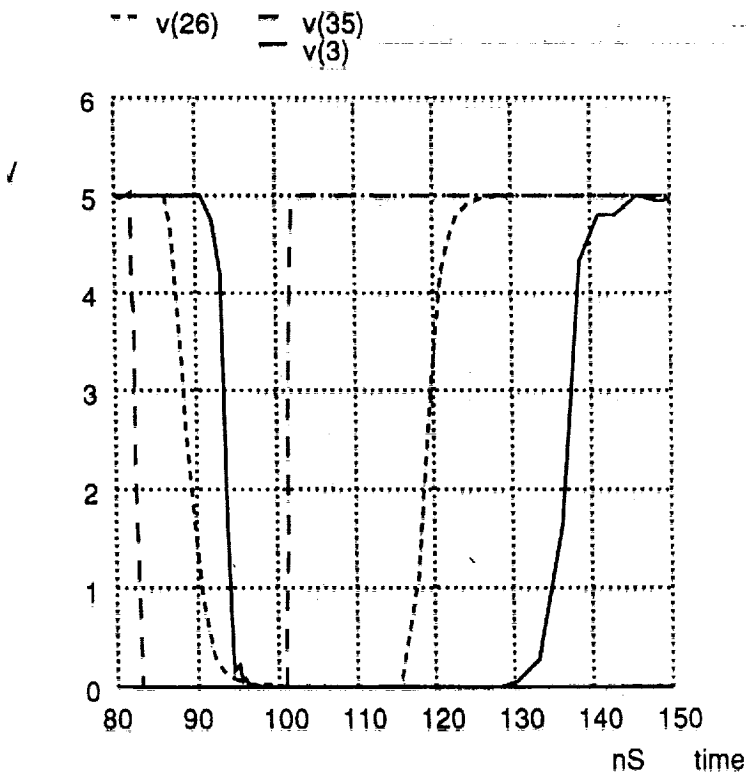

Figure 10: Simulated waveforms of a single phase dynamic CMOS SOP PLA using the triggered 2-bit decoder. All voltage numbers are the same as SOP PLA using the triggered 1-bit decoder.