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High Accuracy Switched-Current Circuits Using an Improved Dynamic Mirror

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[1] *Abstract* - **The switched-current technique, a recently developed circuit approach to analog signal processing, has emerged as an alternative/compliment to the well established switched-capacitor circuit technique. High speed switched-current circuits offer potential cost and power savings over slower switched-capacitor circuits. Accuracy improvements are a primary concern at this stage in the development of the switched-current technique. Use of the dynamic current mirror has produced circuits that are insensitive to transistor matching errors [1]. The dynamic current mirror has been limited by other sources of error including clock-feedthrough and voltage transient errors. In this paper we present an improved switched-current building block using the dynamic current mirror. Utilizing current feedback the errors due to current imbalance in the dynamic current mirror are reduced. Simulations indicate that this feedback can reduce total harmonic distortion by as much as 9dB. Additionally, we have developed a clock-feedthrough reduction scheme for which simulations reveal a potential 10dB total harmonic distortion improvement. The clock-feedthrough reduction scheme also significantly reduces offset errors and allows for cancellation with a constant current source. Experimental results confirm the simulated improvements.**

1 Introduction

The switched-current (SI) sampled-data signal processing technique is becoming a viable alternative to the switched-capacitor (SC) technique. Unlike SC circuits, which require additional processing steps to fabricate precision linear capacitors, SI circuits can be integrated in a standard digital CMOS process. In addition, SI circuits can operate with low power supply voltages, they can operate at high speeds, and they are very area efficient. The drawback of SI circuits at this time is their limited accuracy. This problem must be overcome in order for switched-current circuits to gain the wide acceptance switched-capacitor circuits have attained. In this paper, an SI circuit is presented that significantly improves the accuracy of the current-mode system.

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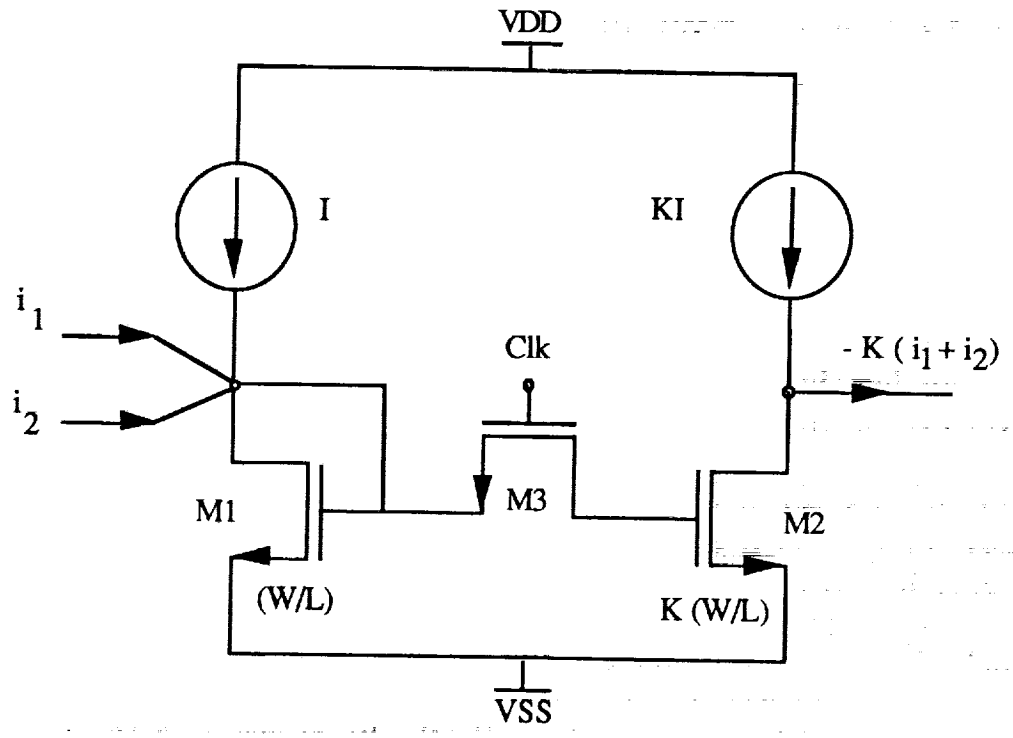

Figure 1: Switched-current track-and-hold circuit.

2 Switched-Current Circuit Operation

2.1 Current Track-and-Hold

The current track-and-hold (T/H) is a basic building block of switched-current circuits, Fig. 1. Transistors M1 and M2 are biased in saturation by the current sources, indicated as I, and the track-and-hold operation is controlled by switch transistor M3. When the clock is high, the input current is mirrored to the output. The parasitic gate capacitance of transistor M2 stores a voltage corresponding to the value of the input current. When the clock is low and transistor M3 is turned off, the drain current of M2 is held at a value corresponding to the voltage stored on the gate of M2.

The current track-and-hold performs the four signal processing operations of inversion, summation, scaling, and delay. Consider initially that the clock is high and the gates of M1 and M2 are shorted. When a signal i1 is input to the diode connected transistor M1, it is mirrored to transistor M2. The drain current of M2 is $I + i_1$. The output current is $-i_1$. This stage inverts the current. The output current is a sum of two input currents by simply connecting wires. Scaled current output is obtained by scaling the aspect ratio of M2 to M1. Finally, signal delay is controlled by switching transistor M3 on and off.

By using these basic signal processing operations, current track-and-hold circuits can be combined to perform more complicated operations. One of these, the integrator, is realized by cascading two current track-and-holds with feedback as shown in Figure 2.

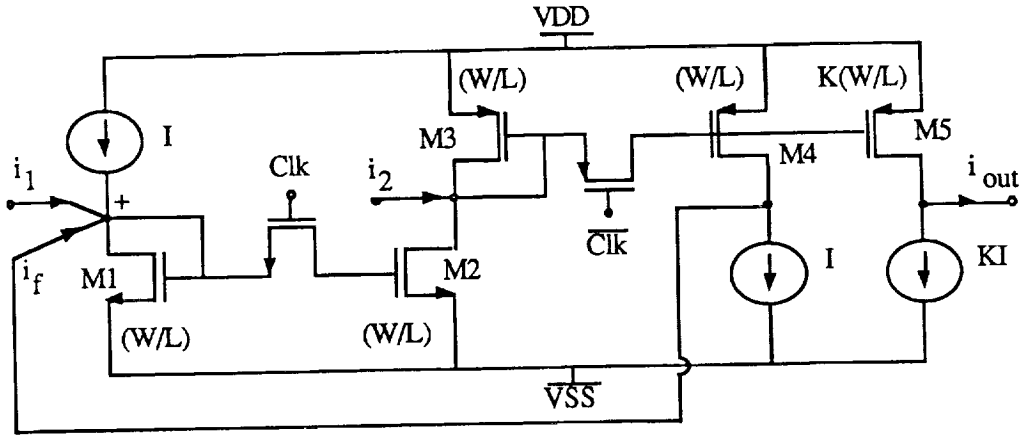

Figure 2: A switched-current differential integrator.

The transfer function of this circuit is

$$i_{out}(z) = \frac{(K(i_1 z^{-1} - i_2 z^{-0.5})}{(1 - z^{-1})}. \quad (1)$$

The non-inverting integrator input is at the input of the first T/H and the inverting integrator input is at the input of the second T/H. The switched-current integrator has been shown to be directly analogous to the switched-capacitor integrator [2]. Note that, as with the SC integrator, the two switches of the SI integrator are controlled by two phase non-overlapping clocks. Additionally, the integrator coefficient K is determined by the aspect ratio of transistor M5 to transistor M3. In the SC integrator a capacitor ratio determines this factor. The reliance of this switched-current circuit on transistor matching has contributed to its limited accuracy.

2.2 Dynamic Current Mirror

The dynamic current mirror eliminates matching errors present in simple current track-and-holds by mirroring current in time rather than space, Figure 3. Operation of the dynamic mirror is controlled by switches MC1, MC2, and MC3. These switches require a two phase non-overlapping clock, similar to the current track-and-hold integrator. It has been shown that an integrator composed of the dynamic mirror cell does

not require any more clocks that the SI integrator presented previously [3]. Transistor M1 is biased by the DC current source I. Initially the switches MC1 and MC2 are closed. The signal current is read into the diode connected transistor M1, producing a voltage on its gate. This voltage is proportional to the square root of the input current for saturated operation. The current is then read out by opening switches MC1 and MC2 while switch MC3 is closed. The stored voltage produces an output current that is an inverted replica of the input current. The dynamic mirror differs from the simple track-and-hold by using switches to time multiplex one transistor, resulting in a float-and-hold operation. Unlike the simple current mirror track-and-hold, where the switch transistor passes nearly zero current, the controlling switches MC2 and MC3 of the dynamic mirror must pass the signal

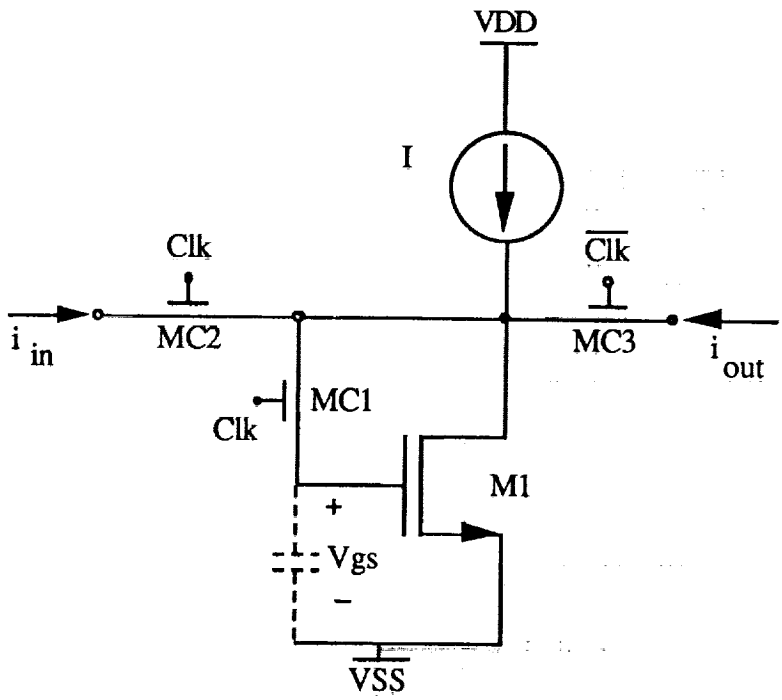

Figure 3: Dynamic current mirror float-and-hold cell.

current. Also, since the same transistor is used to both mirror in and out the signal current, the method of scaling currents by scaling transistor aspect ratios is not possible using the dynamic mirror. To perform signal scaling additional dynamic mirrors are multiplexed in time [4].

3 Dynamic Current Mirror Error Sources

Although SI circuits have been shown to be a viable signal processing circuit technique, the poor accuracy limits system performance. Sources of this inaccuracy for the dynamic mirror are finite output impedance effects, clock-feedthrough effects, and voltage spikes. While these effects can be reduced by using large current mirror devices, this solution is not optimum because increasing device size increases area requirements and reduces speed capabilities. The finite output impedance of a dynamic current mirror results in current division between stages. This division of the signal current becomes an AC gain error with magnitude

$$\Delta i = (Z_{in}/Z_{out} i. \tag{2}$$

Ideally the output impedance of the dynamic mirror would be infinite and the input impedance zero. Because these conditions are not met in real implementations, errors are introduced in the output current. The output impedance of a dynamic current mirror can be increased with the use of a cascade circuit. Because of its extremely high output impedance and special feedback properties the regulated gate cascade [5] was employed

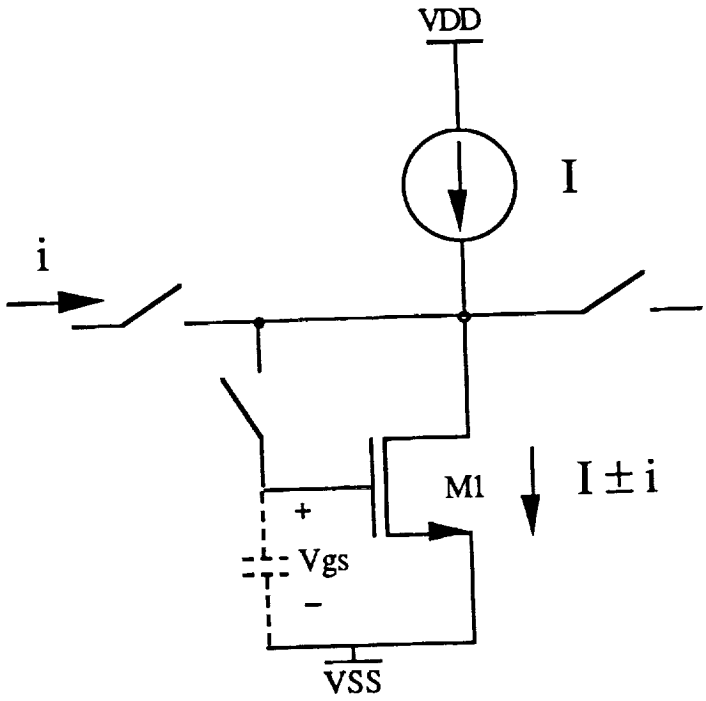

Figure 4: Current mismatch in the dynamic current mirror at the switching interval.

for reducing the AC gain errors. Clock-feedthrough effects in switched-current circuits are more severe than in switched-capacitor circuits [6]. This is because the parasitic gate capacitances of SI circuits are smaller than the linear capacitors implemented in SC circuits. By using larger capacitors to hold the signal, SC circuits reduce the effect of small clock-feedthrough charges. In SI circuits clock-feedthrough results in offset errors and increases total harmonic distortion. Several methods of reducing this injected charge in SI circuits have been studied to date. These include capacitive feedback [7], the use of dummy switches [8], current difference cells [9], and an adaptive clock [7,9]. In this paper a scheme is presented for reducing clock-feedthrough in the dynamic mirror with an improved adaptive clock. Finally, voltage spike errors are introduced in the dynamic mirror by the operation of the two phase nonoverlapping clocks. During the switching of transistors MC2 and MC3 there will be a nonzero interval of time when all of the switches are in the OFF state. During this time period the data holding transistor M1 and the current source will be attempting to draw two different currents. This can be seen in Figure 4. Transistor M1 will have a gate-source voltage set by the input current which will give a drain current of I i. The current mirror will be delivering current I. As a result, the voltage at the drain of transistor M1 will have to move to counter the current imbalance. For negative input currents, the voltage will increase in an attempt to shut off the current source and make transistor M1 draw more current. For positive input currents the voltage will decrease, attempting to draw more current from the current source and less from transistor M1.

There are two paths that these voltage transitions can couple through to the data holding node. One is through switch transistor MC1 as it turns off with switch transistor

MC2. The other is through the drain-gate capacitance of transistor M1. Although it may seem that a cascade could be used to buffer the drain of transistor M1 from the spikes, this circuit will only be useful when functioning as designed. For positive input currents negative spikes will cause the cascade to leave its proper operating point. Subsequent to this, the drain of M1 will no longer be protected and the spike will couple through C_{gs1}. The resulting error from the voltage spikes is signal dependent in both magnitude and polarity, difficult to predict, and sometimes worse than switch charge injection effects. The voltage spike error must be eliminated before clock-feedthrough cancellation schemes can be effective.

4 Voltage Spike Error Reduction

Two solutions to reducing voltage spike errors have been developed. The first involves modifying the clock phasing of the dynamic mirror. By turning switch transistor MC1 off slightly before turning switch transistor MC2 off, the path of the voltage spike through transistor MC1 is eliminated. The new clocking scheme presented here does not add another clock phase to the circuit, only a delay is needed. Transients occurring when the transistor goes from the hold mode to the output float mode are irrelevant because a new current value will be read into the diode connected transistor at this time. The delay only needs to be as long as the turn off time of transistor MC1. It can be implemented on chip with an even number of cascaded inverters. The other solution to voltage spike errors must eliminate the voltage spike from coupling through the drain-gate capacitance of transistor M1. This is accomplished by using current feedback around a regulated gate cascade dynamic current mirror, Fig. 5. The regulated gate cascade is used to increase the output impedance of the dynamic mirror and the current feedback is used to keep the cascade in its proper operating region for positive input currents. The circuit operates as follows. Transistor M3 senses variations in the drain-source voltage of transistor M1. Since a constant current biases M3, these variations will be amplified by the loop gain of transistors M3 and follower M2. Differences between the drain-source voltage of transistor M1 and the gate voltage of transistor M3 required to supply constant current J will be amplified, stabilizing the drain voltage of M1. When the current in the current source, M6, is smaller than the current in the drain of transistor M2, the voltage on the drain of transistor M2 decreases because of the current mismatch. This increases the gate voltage of transistor M4 due to the voltage feedback of transistor M3. Transistor M4 subsequently sources additional current through current mirror transistors M5 and M6 to cancel the current imbalance. When the current imbalance is corrected, the voltage on the gate of transistor M4 returns to its original DC value. The current feedback, in the meantime, keeps the voltage on the drain of transistor M2 more stable which keeps the cascade in its proper operating region. With the cascade functioning throughout the switching interval, the drain of transistor M1 was buffered from the transients and the voltage stored on its gate remained unaffected.

In order to verify the improvement in circuit performance with the current feedback

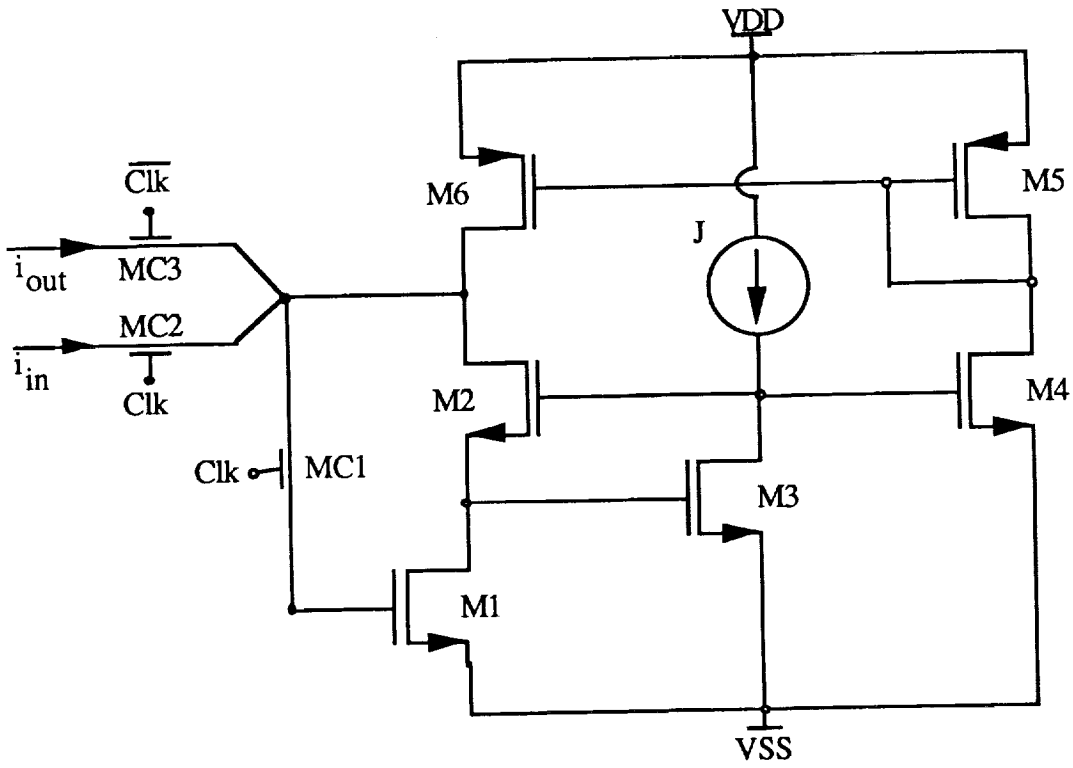

Figure 5: Regulated gate cascade with current feedback.

scheme, simulations were performed for a dynamic current mirror biased with 100uA using a 5kHz sinusodial 50uA input signal. The circuit was clocked at 100kHz. By eliminating errors due to voltage spiking, the harmonic distortion was improved by almost 9dB over the cascade without current feedback.

5 Clock-Feedthrough Error Reduction

Clock-feedthrough has been extensively analyzed in the literature [8,10]. Analysis shows that clock-feedthrough is dependent on the aspect ratio of the switch transistor with respect to the data holding transistor, the clock slope, and the magnitude of the input signal. The signal dependence of clock-feedthrough leads to difficulties in predicting the error, a necessary condition for cancellation. The adaptive clock is a technique for reducing clock-feedthrough through control of the ON conductance of the switch. This control simultaneously reduces the clock swing on the switch and causes the gate-source voltage of the switch to remain constant for varying input signals. With a constant gate-source voltage, the charge injected by the switch becomes constant. This results in the possibility of canceling the error current with a constant current source. In order to use such a system, the nonsaturated region of operation must be used for the data holding transistor. For saturated operation nonlinear transformations between voltage and current result in harmonic distortion even if a constant clock-feedthrough voltage can be generated. For

the nonsaturated region of operation the transformations are linear. A simplified equation for the drain current of a transistor operating in the nonsaturated region is given in Eqn. 3. Added to the gate-source voltage is the constant clock-feedthrough voltage, V_{cf}.

$$i_{ds} = \beta V_{ds}(V_{gs} + V_{cf} - VT - 1/2V_{ds}. \tag{3}$$

Keeping only the clock-feedthrough term, it can be seen that the error output current is given simply by,

$$i_{cf} = \beta V_{ds} V_{cf}. \tag{4}$$

The clock-feedthrough voltage contributes a DC offset. If constant, no harmonics are generated. A new adaptive clock scheme, applied to the dynamic mirror, is shown in Figure 6. When the clock signal is high, the inverter output is low and the gate-source voltage of switch MC1 is set by the gate-source voltage of transistor M2, regardless of the voltage at the source of MC1. When the clock signal goes low, the inverter turns on which shorts the gate and source of MC1 together. This turns off the transistor and the input signal is held on the gate of M1. By using this control, the gate-source voltage of the switch when on is always equal to the constant gate-source voltage of transistor M2. In order to cancel the constant clock-feedthrough generated by the adaptive clock a constant current that is equivalent to the error current needs to be generated. It has been shown that the integrator circuit presented earlier will perform such a task, [3]. The adaptive clock is also useful as a clock swing limiter. Simulations show that for a data holding transistor (M1 in Figure 6) width to length ratio of 7/5 , which gives a transistor area of 35×10^{-12} square meters, the use of an adaptive clock without cancellation reduces total harmonic distortion by 10 dB. The DC offset is reduced by an order of magnitude. As the data holding transistor size is increased, the adaptive clock's effect on total harmonic distortion decreases due to an increase in the data holding capacitance. This limits the influence of clock swing reduction. However, even for larger transistor sizes, 28/20, the use of an adaptive clock without cancellation continues to improve the DC offset and for all device sizes the error is kept constant. The adaptive clock circuit of Figure 6 was fabricated through MOSIS in a two micron CMOS p-well process. The dynamic mirror used the regulated gate current feedback circuit presented earlier as a cascade. Initial experimental results verify the improvements indicated by simulations. For a large data holding transistor size of 28/20 the DC offset error was reduced by 40

6 Conclusion

The dynamic current mirror is a useful circuit to reduce reliance on transistor matching. In order to effectively use the dynamic current mirror, consideration has to be given to the effects of transients when switching currents. Clock delays and current feedback were used to reduce distortion due to voltage spikes that occur during intervals of current mismatch. Clock-feedthrough is a source of distortion that effects all methods of sampled-data signal

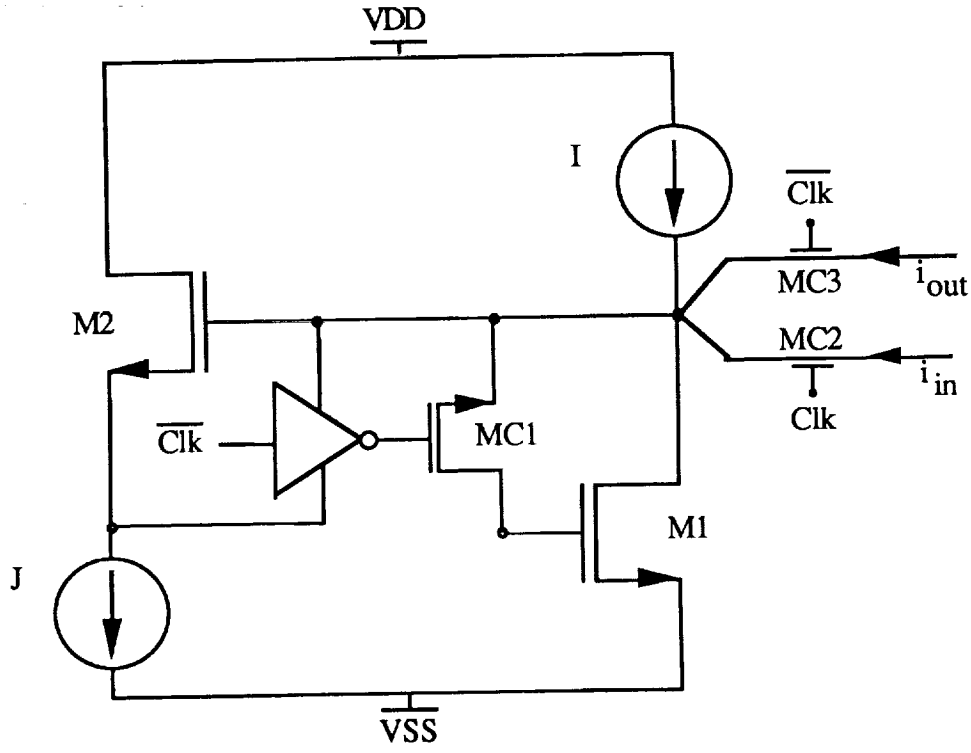

Figure 6: Adaptive clock applied to the dynamic mirror.

processing. For the dynamic mirror an adaptive clock was developed that was shown to both reduce and make constant charge injected by the switch.

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