A Tunable CMOS Constant Current Source

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Abstract - **A constant current source has been designed which makes use of on chip electrically erasable memory to adjust the magnitude and temperature coefficient of the output current. The current source includes a voltage reference based on the difference between enhancement and depletion transistor threshold voltages. Accuracy is ± 3% over the full range of power supply, process variations, and temperature using eight bits for tuning.**

1 Introduction

The lack of precision components in CMOS integrated circuits has traditionally forced design engineers to depend upon external components and matching of on chip components to realize precision functions. For example, switched capacitor filters [1] realize precise transfer functions only when supplied with an accurate clock frequency, which is usually generated by an external crystal oscillator. The locations of poles and zeros are relative to the clock frequency, and are determined by accurate on chip capacitor ratios. Switched current [2], Transconductor C [3], and MOSFET C [4] filters also depend on an external frequency reference, and matching of transistors to realize their transfer functions. In cases where external components are unacceptable, some kind of tuning of the non-ideal components must be accomplished to realize precision functions. Laser trimming is one method which works well, but requires expensive equipment, and a special process. Blowing poly-silicon fuses is inexpensive, but sometimes unreliable, and some types of tuning are difficult to achieve with fuse blowing. Neither laser trimming, nor fuse blowing is reversible, a distinct hindrance if a tuning operation requires more than one iteration. If the circuit to be tuned is fabricated in a process which includes nonvolatile electrically erasable memory, floating gate transistors can be programmed to trim analog performance. Two different methods may be used to employ the floating gate transistor to tune an analog circuit. First, an analog voltage can be stored on the floating gate to change the current or resistance from source to drain [5,6]. The current or resistance will be a function of temperature, and possibly power supply voltage. The second method is to use nonvolatile digital memory to select how much resistance or capacitance is connected to a node, or which tap of a resistor will be connected in a circuit. The second method has the advantage of insensitivity to temperature and power supply voltage, assuming the resistance of the analog switch is low, while it has the disadvantage of requiring more circuitry to do the tuning. In this paper, a circuit is described which uses the later method to tune the magnitude and temperature coefficient of a current source.

2 Application

The tunable current source described in this paper, is a part of a larger circuit which emits a constant frequency square wave, independent of temperature, processing, and power supply voltage. The circuit consists of a voltage controlled oscillator (VCO), a frequency to current converter, and an integrator connected in a feedback loop as shown in figure 1.

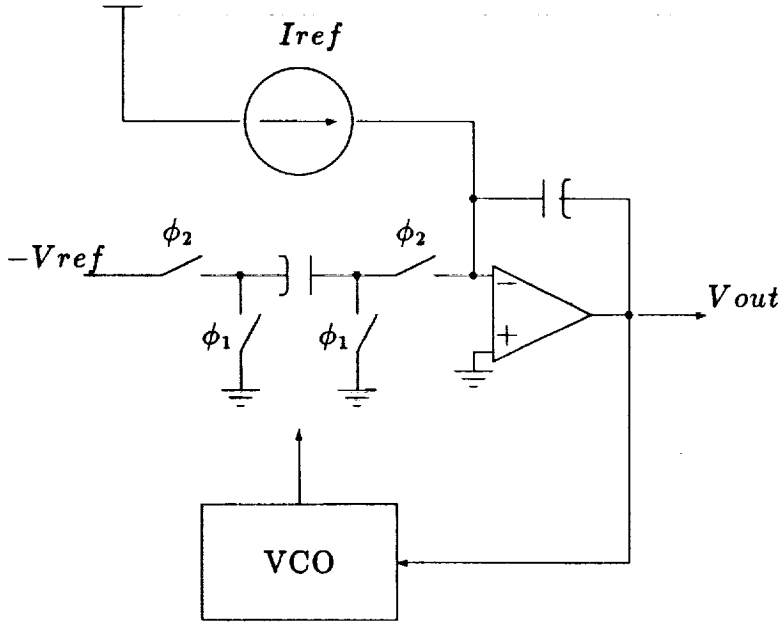

Figure 1: Constant frequency circuit.

The control voltage for the VCO is used in other cells on the chip. The frequency to current converter is based on a switched capacitor network whose average current is given by equation 1 [7]:

$$I_{ave} = f * V * C \tag{1}$$

where f is frequency, V is the voltage across the switched capacitor network, and C is the value of the switched capacitor. At a fixed temperature, both V, and C are constants in this circuit, which makes the average current proportional to frequency. The difference between the constant current and the switched capacitor current is integrated, and used to control the VCO. The high gain of the feedback loop ensures that the VCO emits a frequency which causes the current in the switched capacitor network to exactly cancel the constant current. Since the capacitor has a non-zero temperature coefficient, the constant current source must have a temperature coefficient which cancels that of the capacitor. The current source must also compensate for variations in reference voltage and capacitance due to processing.

3 Voltage Reference

In this circuit, a constant current will be derived from a constant voltage as shown in figure 2.

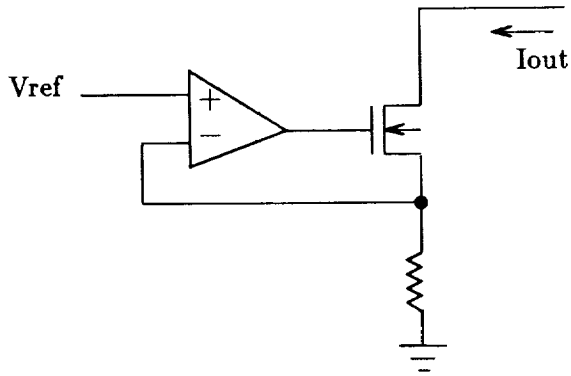

Figure 2: Voltage to current converter.

The performance of the current source will only be as good as the performance of the voltage reference, so the voltage reference must have good rejection of power supply variations and temperature. Three possibilities come to mind to generate a reference voltage on a chip. A power supply voltage divider is the most simple reference available, but since the specification for the current is tighter than the variation of the power supply, the voltage divider can not be used to generate the reference voltage. The bandgap reference [8] is probably the most accurate voltage reference which can be built on a CMOS chip, but it can not be used on this chip because substrate currents, caused by the bipolar transistors, are unacceptable. A threshold voltage reference [9] is based on the difference between the threshold voltages of depletion and an enhancement MOSFET's.

$$V_{ref} \approx V_{te}(1 - \alpha_1 T) - V_{td}(1 - \alpha_2 T) \tag{2}$$

Where V_{te} is the n-channel enhancement threshold voltage, V_{td} is the n-channel depletion threshold voltage, α_1 is the temperature coefficient of V_{te}, α_2 is the temperature coefficient of V_{td}, and T is temperature. Since α_1, and α_2 are approximately equal, V_{ref} has a very small temperature coefficient.

The mobility temperature coefficient can be ignored by making the width to length ratio of the transistors large for the amount of current flowing through them, and by making the width to length ratio, and drain to source current equal for both transistors. This makes the gate to source voltage mostly V_t, and the gate to source voltage above V_t is approximately equal for both transistors. The threshold voltage of both transistors is also dependent on the source to bulk voltage. Depletion and enhancement transistors have approximately the same body effect factor, so if the transistors have the same source to bulk voltage, the body effect will change both threshold voltages equally. This gets canceled by the subtraction as shown in equation 2. One circuit which implements the

reference with equal current, and source to bulk voltage in both transistors is shown in figure 3.

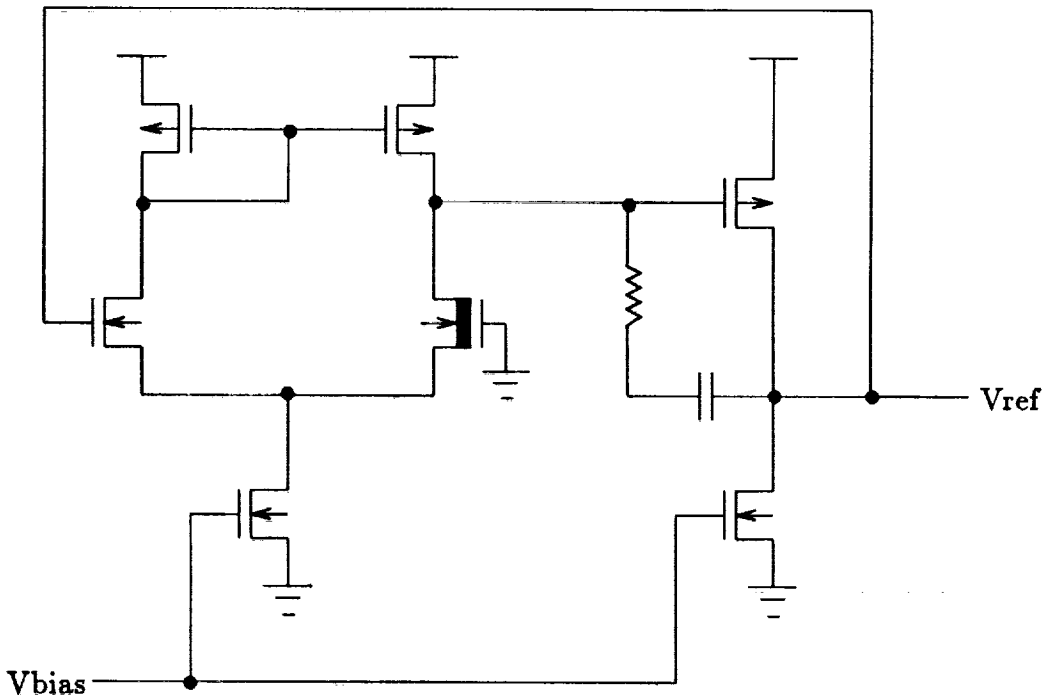

Figure 3: Enhancement-Depletion voltage reference.

Unfortunately, the reference voltage is larger than the power supply in some cases, rendering the circuit useless for this application. To rectify this situation, the circuit in figure 4 was designed which sums half of the two threshold voltages. The body effect is no longer equal for the two transistor, so the output voltage will be sensitive to the bulk voltage. Equal current flows through the two transistors, and the width to length ratios are large compared to the current, so mobility temperature coefficients are negligible.

4 Voltage to Current Conversion

Voltage to current conversion will be accomplished by maintaining the reference voltage across a resistor using an opamp as shown in figure 2. This circuit will be independent of temperature only if the resistor and the voltage reference have a zero temperature coefficient. This is far from true on silicon, where the best resistor available has a temperature coefficient of approximately $0.1\%/°C$. In addition to the temperature coefficient, the value of the resistor and voltage reference are dependent on processing. To tune the magnitude of the resistor to account for processing, taps can be programmed as shown in figure 5. The resistance of the switchs must be made small compared to the linear resistor.

In order to produce a current with a small temperature coefficient, the voltage across

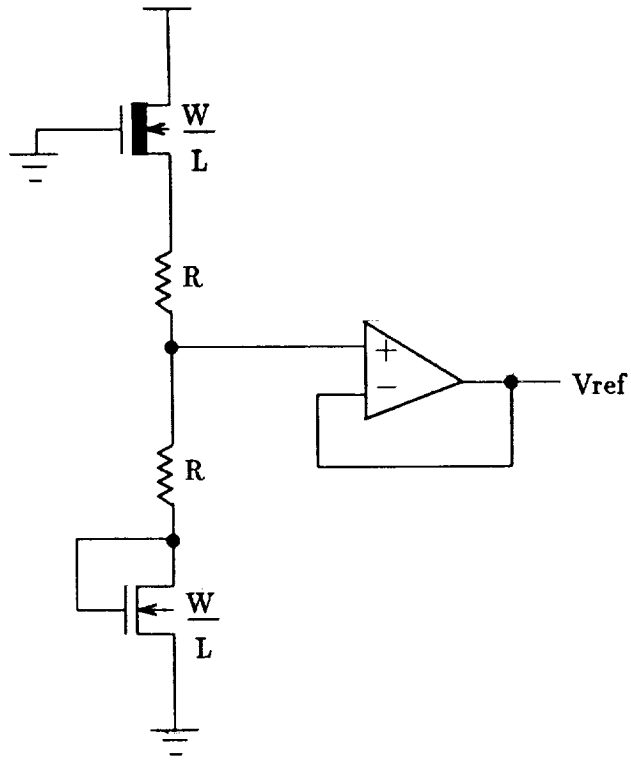

Figure 4: Enhancement-Depletion reference for low power supply voltage.

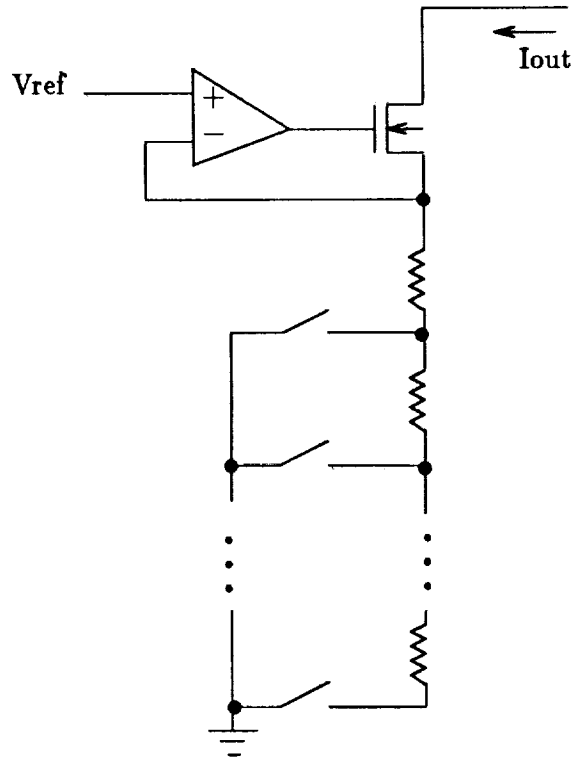

Figure 5: Tuning Scheme for the Magnitude of I_{out}.

the resistor must have a positive temperature coefficient to cancel the positive temperature coefficient of the resistor. One way to generate a voltage with a positive temperature coefficient is to subtract a voltage with a negative temperature coefficient from a constant voltage. The threshold voltage of an enhancement transistor has a linear negative temperature coefficient suitable for subtraction from V_{ref}. To make the threshold voltage independent of power supply voltages, a p-channel transistor can be used with its source connected to the bulk to get rid of the body effect. The circuit in figure 6 shows this temperature coefficient cancellation.

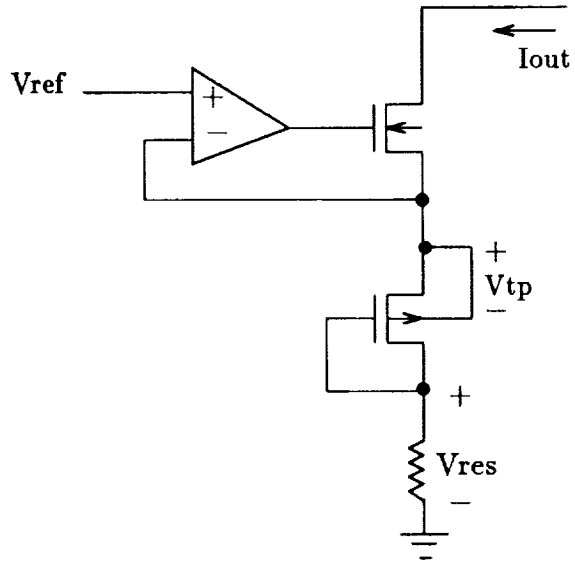

Figure 6: Temperature Coefficient cancellation for I_{out}.

To tune the temperature coefficient of the current to zero, the magnitude of the reference voltage can be adjusted. This makes the negative temperature coefficient voltage a larger or smaller portion of the reference voltage, which adjusts the overall temperature coefficient. This temperature coefficient cancellation can be expressed as follows:

$$I_{out} \approx \frac{K_1 V_{ref} - V_{tp}(1 - \alpha_1 T)}{K_2 R_{ref}(1 + \alpha_2 T)} \tag{3}$$

where V_{tp} is the threshold voltage of a p-channel enhancement transistor, α_1 is the temperature coefficient of V_{tp}, and α_2 is the temperature coefficient of R_{ref}. K_1 is the fraction of the reference voltage chosen by the first tapped resistor, K_2 is the portion of R_{ref} chosen by the second tapped resistor. K_1 and K_2 range from zero to one. If we define two new terms:

$$V_{tune} = K_1 V_{ref} - V_{tp} \tag{4}$$

and

$$\beta = V_{tp}\alpha_1 / V_{tune} \tag{5}$$

then equation 3 can be rewritten as:

$$I_{out} \approx \frac{V_{tune}(1+\beta T)}{K_2 R_{ref}(1+\alpha_2 T)} \tag{6}$$

When β equals α_2, I_{out} has a zero temperature coefficient.

The key to all this temperature coefficient cancellation is that all the components have only first order temperature coefficients. Measurements from silicon indicate that poly-silicon resistors have linear temperature coefficients, as well as the smallest temperature coefficient of any resistor available on chip. The poly-silicon resistor also has no voltage coefficient, since there is no reverse bias junction which could change the dimension of the resistor. The threshold voltages of n-channel and p-channel transistors have negligible higher order temperature coefficient terms. Threshold voltages of n-channel enhancement and depletion transistors were found to track well over temperature. A simplified schematic of the entire circuit is presented in figure 7.

5 Tuning Strategy

Equation 3 shows that K_1 adjusts the magnitude of the current as well as the temperature coefficient, so K_1 must be adjusted first, then K_2 can calibrate the current to the desired value. Tuning the temperature coefficient of this circuit in a production test environment without non-volatile memory would be a logistic nightmare. Somehow the result of the first temperature measurement would have to be stored with a serial number for each die for use during the second temperature test. No such serial numbers are available for each die, and moreover, testing at two temperatures is usually done before and after packaging; one temperature during wafer sort, and the other temperature during final assembly test. Fortunately, with non-volatile memory the results of the first temperature measurement can be written to memory then simply read during the second temperature test. After the temperature coefficient is tuned, the magnitude can be adjusted in one step, since the magnitude adjust (K_2) should have almost no effect on the overall temperature coefficient.

6 Results

The circuit was simulated with various extremes of power supply voltage, processing, mismatch of threshold voltage temperature coefficients, and temperature. HSpice [10] simulations show the error to be less than 3%. Error can be attributed to non-zero step size in tuning, and finite power supply rejection, especially to the substrate power supply. The chip is presently in layout.

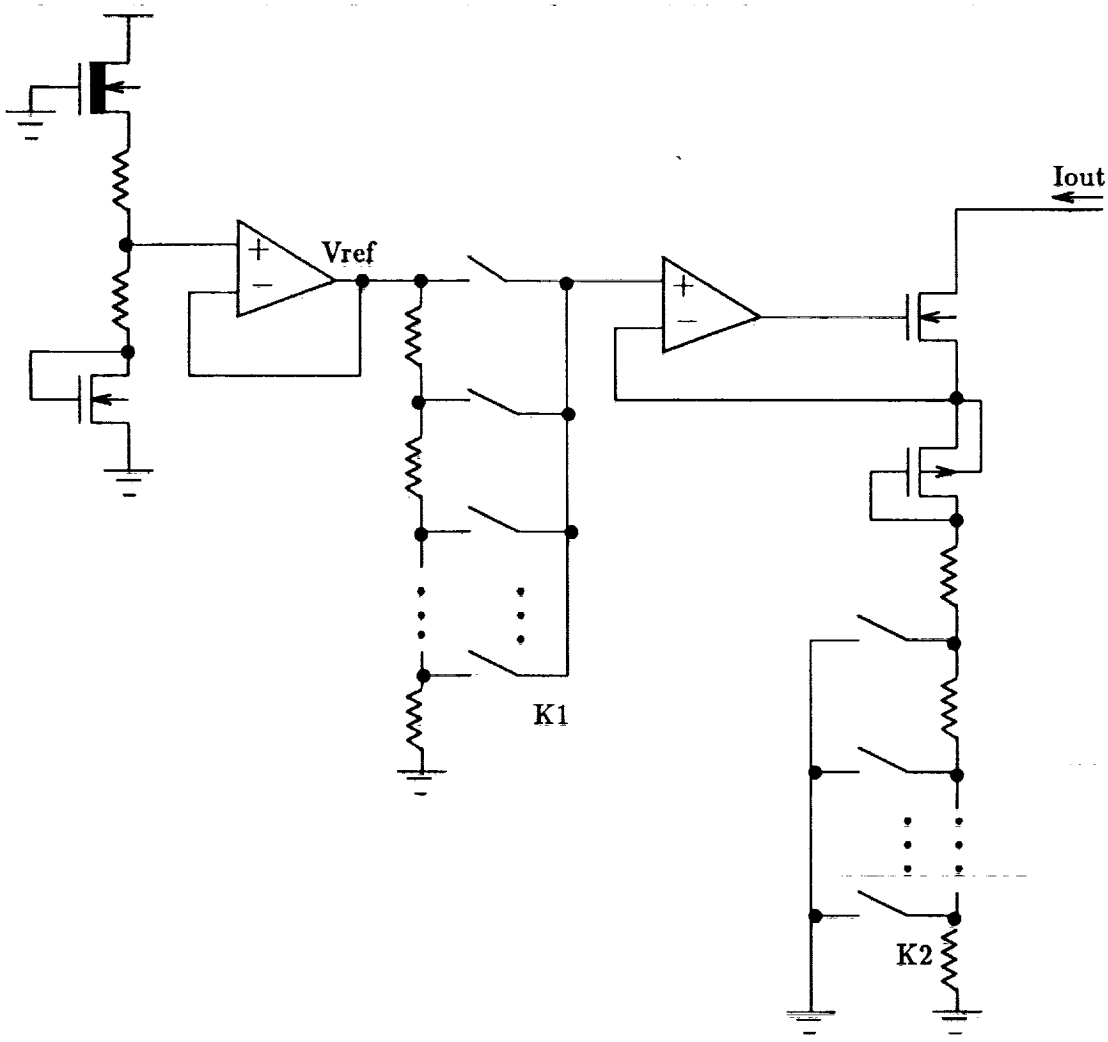

Figure 7: Simplified Schematic.

7 Conclusion

Tuning analog circuits with nonvolatile memory provides a very powerful and linear way to overcome the wide tolerances intrinsic in semiconductor processing. The disadvantage of using digital memory to tune analog circuits as opposed to using the floating gate transistors in an analog fashion is the increased number of transistors necessary to do the tuning. The advantage is that the nonlinear characteristics of programming the floating gate transistors can be ignored.

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