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Multichannel Error Correction Code Decoder

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Abstract

This paper provides a brief overview of a processing satellite for a mesh very-small-aperture (VSAT) communications network; describes the multichannel error correction code (ECC) decoder system, the uplink signal generation and link simulation equipment, and the time-shared decoder; discusses the testing; and recommends applications of the time-shared decoder.

Introduction

The Digital Systems Technology Branch of NASA's Lewis Research Center has an ongoing program in modulation, coding, onboard processing, and switching. Since 1990 the branch has been investigating various mesh very-small-aperture (VSAT) architectures that utilize onboard processing technology.¹⁻⁵ Multichannel demultiplexers, time-shared multirate demodulators, and high-speed codecs have been developed under contract in support of the mesh VSAT architectures (Fig. 1). A key element of this regenerative satellite architecture that has been neglected to date is the development of a time-shared decoder. Time sharing the decoder is necessary because the satellite architectures envisioned are multibeam systems with each beam capable of receiving 1000 individual, simultaneous transmissions.

Presently, NASA is proceeding with a project to incorporate a time-shared decoder into the mesh VSAT onboard-processing (OBP) architecture. The primary goal is to demonstrate a time-shared decoder for a regenerative satellite using asynchronous, frequency-division multiple access (FDMA) uplink channels, thereby identifying hardware and power requirements and fault-tolerant issues that must be addressed in a operational system. A secondary goal is to integrate and test, in a system environment, two NASA-sponsored, proof-of-concept hardware deliverables: the Harris Corp. high-speed Bose Chaudhuri-Hocquenghem (BCH) codec⁶ and the TRW multichannel demultiplexer/demodulator.⁷ A beneficial byproduct of this project is the development of flexible multichannel uplink signal generation equipment.

Error Correction Code Coding Formats

Convolutional, linear block, and concatenated codes were all considered for the time-shared decoder. Also considered in the design tradeoffs was whether or not to use a "unique word." Although adding a unique word adds overhead, the processing otherwise involved to resolve encoder word ambiguity was considered impractical for all coding formats—particularly when considering the number of channels in an operational system. Therefore, we chose to use a unique word to simplify the overall processing.

A convolutional codec does not require unique words and tends to work well for dedicated channels. However, a convolutional codec, by architecture, is rather difficult to time share. In fact, one of the strengths of the convolutional codec is that, for a dedicated channel, one can begin decoding in midstream and after some degradation in the first few decoded bits the codec stabilizes and performs as expected. However, to time share a convolutional codec, the state of the codec must be saved for each channel. The codec is restored to the specified channel's previous state every time that channel's data are to be processed. The processing and switching can get quite involved—particularly as the size of the data packets decreases. Conversely, attempting to simplify the codec by increasing the packet sizes inadvertently increases the data memory storage requirements. Therefore, the concept of implementing a time-shared convolutional decoder was discarded.

A linear block code requires a unique word to resolve encoder word ambiguity because of the complexity of the code word search algorithm if a unique word is not used. Using a unique word makes time sharing of a block codec relatively straightforward as the encoder word ambiguity disappears. Data blocks from individual channels can be decoded on a block-by-block basis. In addition, linear block codes can provide a wide range of code rates. Therefore, the linear block code format was chosen for implementation in a time-shared decoder.

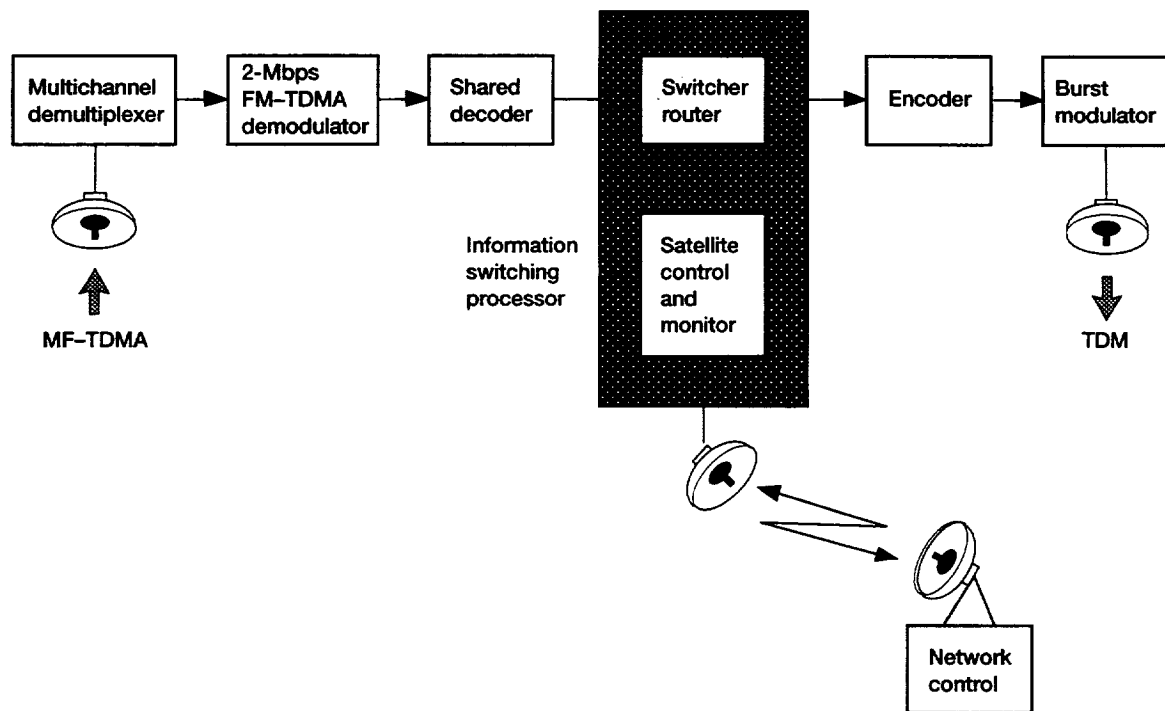


Figure 1.—Mesh VSAT processing satellite.

A concatenated code was considered overly complex to implement relative to a linear block code; therefore the concept was discarded.

Multichannel Error Correction Code System

The multichannel error correction code system consists of a bit-error-rate test set, uplink signal generation equipment, a multichannel demultiplexer/demodulator (MCDD) including radiofrequency link simulation equipment, and the time-shared decoder (Fig. 2).

Bit-Error-Rate Test Set

The bit-error-rate test set is an off-the-shelf test set capable of generating pseudo-random data at approximately 64 kbps.

Uplink Signal Generation Equipment

The uplink signal generation equipment consists of a multichannel error correction code (ECC) encoder card, four digital modulator cards, a digital combiner/upconverter unit, and clock and mixing signal generation cards.

Computer Control

The entire system is controlled by a personal computer that interfaces to the multichannel ECC decoder hardware through a parallel printer port. Control is based on the serial protocol channel (SPC) principle.⁸ Major functions are controlled through a three-line serial interface consisting of clock, data, and mode

using 818 double-buffered, serial-to-parallel, eight-bit shift registers. These registers may be cascaded to create various-length control words. Three of the eight printer port lines are assigned as clock, data, and mode select. The other five lines are used for addressing, providing up to 32 possible control addresses.

Control Distribution Card

The control distribution card serves as an interface between individual multichannel ECC decoder cards and a personal computer through the parallel printer port. The card decodes the five-bit address lines from the parallel port and transmits the three SPC lines to the proper card. In addition, the control distribution card sends power-on and computer-generated reset signals to individual cards. This procedure is necessary because much of the multichannel ECC decoder logic is implemented by microcoded state machines that must be initialized.

Clock Distribution Card

The clock distribution card (CDC) buffers and distributes various clocks throughout the multichannel ECC decoder hardware. For the uplink signal generation equipment the CDC generates four 67.108864-MHz (2^{26} Hz) clocks that are used by the encoder/modulator timing cards and the quadrature oscillator card. The 67.108864-MHz clocks are derived from a 268.435456-MHz (2^{28} Hz) voltage-controlled ovenized oscillator. For the time-shared decoder hardware the CDC generates an 11.52-MHz clock that is used by the unique-word detector card, the encoder block-builder card, and the time-shared decoder. The 11.52-MHz clock is derived from a 46.08-MHz clock provided by the TRW MCDD special test equipment.

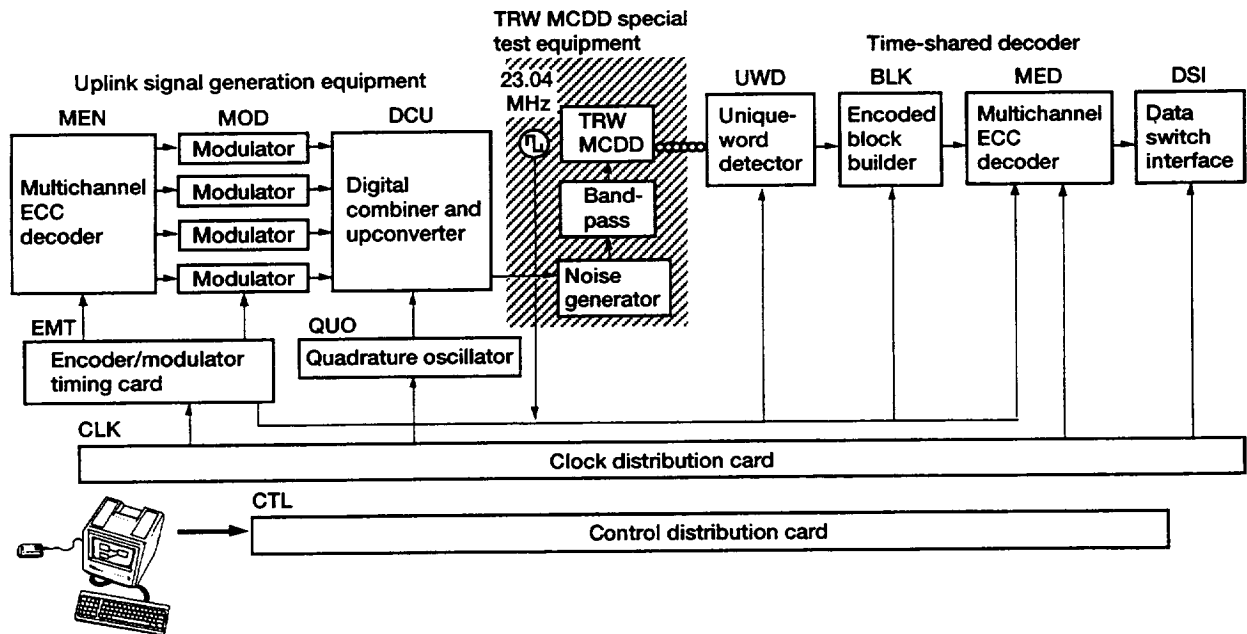


Figure 2.—Uplink signal generation equipment and time-shared decoder.

Encoder/Modulator Timing Cards

There are two pairs of identical encoder/modulator timing cards (EMT's). One EMT provides the clock at the uncoded data rate to the multichannel time-shared encoder and decoder cards. The second EMT provides a 16.384-MHz clock to the time-shared encoder card, four modulators, the digital combiner/upconverter (DCU), digital-to-analog (D/A) converters, and the time-shared decoder.

An EMT consists of two sets of SPC interfaces, a Stanford Telecommunications Incorporated (STEL) 1275 numerically controlled oscillator (NCO) evaluation card, and two programmable clock generation circuits. One SPC interface in both EMT's controls the STEL-1275 NCO, which is programmed to generate a 16.384-MHz sine wave from a 67.108864-MHz reference clock. Within the first EMT the 16.384-MHz frequency is used to generate clocks at the uncoded and coded data rates. These rates are programmed by the second of two SPC interfaces. Each clock (encode rate or decode rate) is generated by preloading a countdown counter circuit with a 16-bit value held in the SPC buffer. The outputs of the counters are compared with the high 15 bits of the SPC buffer to create a near 50-percent-duty-cycle clock. The countdown counters are reloaded after reaching a count of zero. Within the second EMT the 16.386-MHz clock is simply buffered and distributed across the back plane (Fig. 3).

Quadrature Oscillator

The quadrature oscillator card provides sine and cosine signals to the DCU card. These signals are used to upconvert a 1.44-MHz composite signal to an intermediate-frequency signal between

10 and 20 MHz. For use with the TRW MCDD the composite signal will be upconverted to 17.28 MHz.

The quadrature oscillator board has been designed to create two high-purity tones in 90° phase quadrature with individually adjustable center frequencies. The tones are generated by a commercially available NCO hybrid module (STEL-1377Q/CE) with integral D/A converters. A 67.108864-MHz reference clock signal from the CDC drives the NCO. Because the NCO has a 32-bit phase accumulator, the frequency resolution of the NCO outputs is 1/64 hertz per step ($2^{26}/2^{32} = 1/64$) or 64 steps per hertz. This frequency resolution allows highly accurate output frequency values to be synthesized. Each tone output is filtered by a pair of 21.4-MHz low-pass filters in cascade, to reject aliases of the digitally implemented synthesis process. There is a computer control interface to the hybrid module through the SPC (Fig. 4).

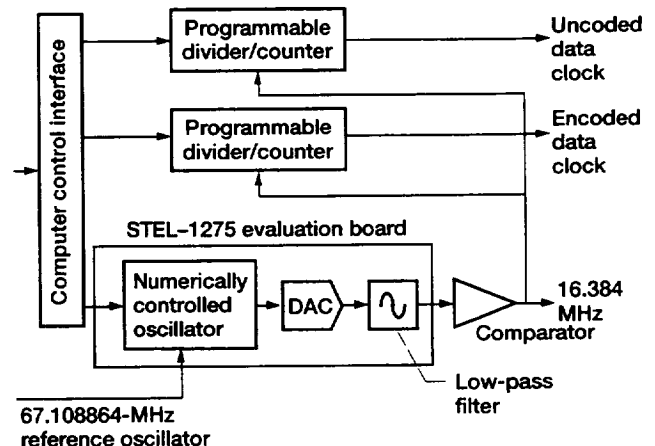


Figure 3.—Encoder/modulator timing card.

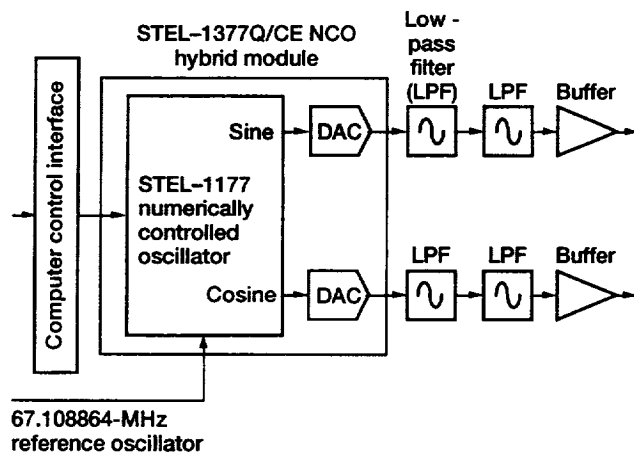


Figure 4.—Quadrature oscillator.

Multichannel ECC Encoder

The multichannel ECC encoder generates four channels of pseudorandom data, block encodes the data, prefates a unique word to the encoded block, and passes the data on to the modulator cards. One of four channels can be selected to originate from a commercial bit-error-rate test set; the other three channels are generated on the card. The pseudorandom generators operate at a rate of k/n , where k is the uncoded data rate and n is the coded data rate. To operate with the TRW MCDD, n is always 64 kbps. The four serial data sources are built into data blocks of 224 to 480 uncoded data bits using one uncoded data first in-first out (UC-FIFO) per channel. As soon as a full data block is available from any of the channels, the control circuitry is notified. Once notified that a full uncoded block is available, the control circuitry stores a unique word into the encoded data FIFO (ED-FIFO). The uncoded data block is then encoded and stored in that same ED-FIFO. The data are encoded by using a BCH codec chip developed by Harris Corp.⁶ The codec chip is clocked at 16.384 MHz and can easily be time shared among 32 channels operating at approximately 64 kbps. Just as in the uncoded case there is one FIFO per channel. The encoded data are passed on to the modulator

card as a two-bit differentially encoded symbol at the symbol rate of 32 ksps. For debugging and link evaluation purposes a no-code option is available. The no-code option and the block lengths are computer controlled through the SPC interface (Fig. 5).

Modulator

The digital modulator board has been designed to create a wide variety of continuous and burst-formatted, modulated digital signal types, including spectral shaping. The modulator can also digitally offset the center frequency of the signal. This function supports direct digital translation to low intermediate frequencies, FDMA simulation (with multiple modulators), and adjacent-channel interference testing.

The modulator consists of an input-interface section, a serial-to-parallel (S/P) and interpolation section, a pulse-shaping filter, and a digital baseband upconverter section (Fig. 6). System timing on this card is derived from a 16.384-MHz clock.

The modulator's input-interface section will accept symbol inputs as a continuous stream or in bursts of up to 512 symbols in length. The input source must ensure that the average symbol creation rate equals the production rate. The modulator provides a 50-percent-duty-cycle symbol clock whose frequency equals the sample rate divided by the interpolation factor. This symbol clock is available for use by the input source if desired. The programmable read-only memory (PROM) following the synchronous FIFO maps the symbol input value into codes representing the desired I and Q amplitudes.

Two S/P and interpolation-section hardware paths (one for I signals and one for Q signals) each accept amplitude codes up to four bits wide and perform a serial-to-parallel register function on them. This action forms a finite-width data aperture for input to the spectral shaping operation. The programmable array logic (PAL) in each path creates the S/P registers and a cyclic counter that sequences from zero to one less than the desired interpolation

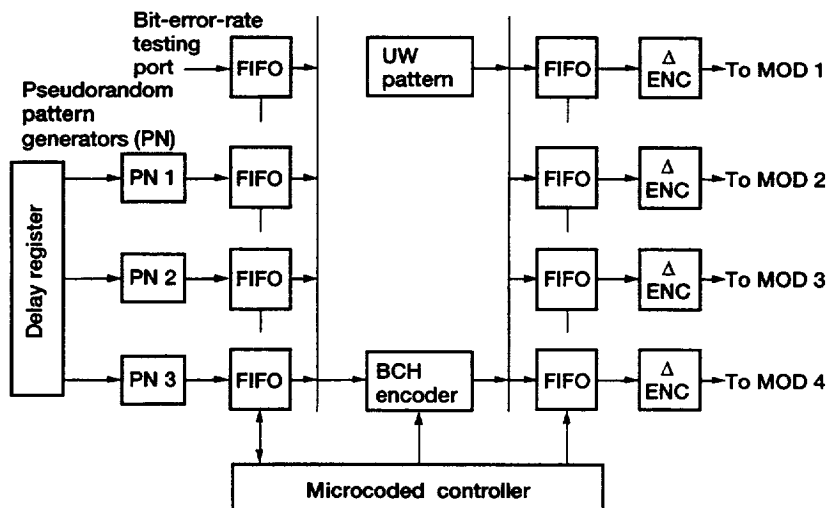


Figure 5.—Multichannel ECC encoder.

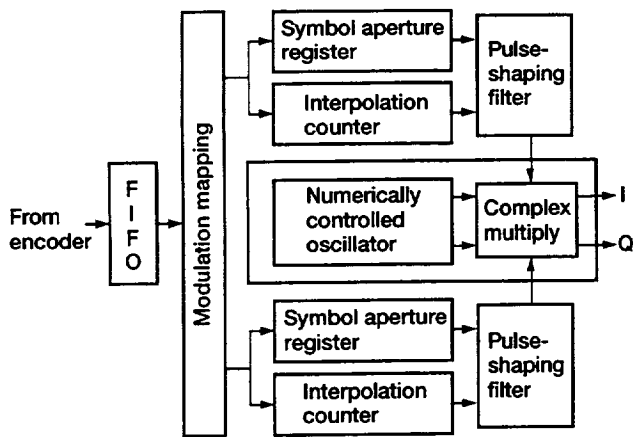


Figure 6.—Digital modulator.

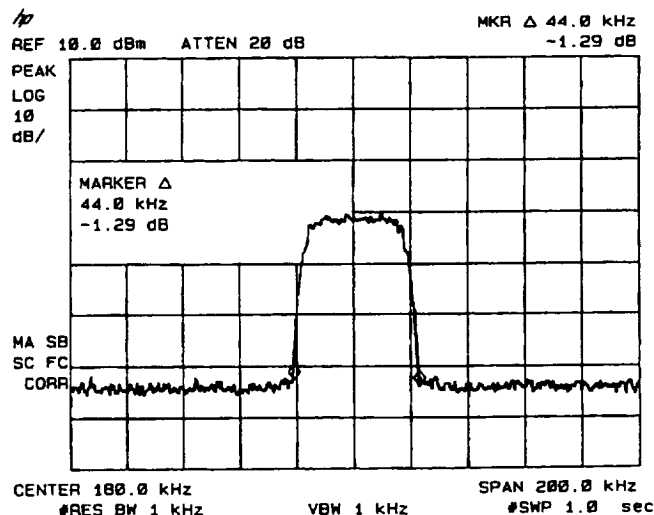


Figure 7.—Thirty percent raised cosine offset QPSK spectrum.

factor. A common PROM decodes specific I counter output values to create control signals for both the I and Q channels' S/P and interpolation functions. The PROM also controls the reading of the FIFO contents to account for the FIFO and mapping PROM pipeline latency.

The pulse-shaping filter's action is implemented by PROM lookup tables, which are addressed by a concatenation of S/P-converted amplitude codes and interpolation sequence counting as built by the S/P and interpolation functions. The pulse-shaping PROM outputs are added together so that two smaller memories can act as one larger memory in terms of available aperture size and degree of interpolation.

The digital baseband upconverter function is a combination of a numerically controlled oscillator and a complex multiplier. This operation shifts the center frequency of the filter outputs' spectral content from zero frequency to any desired frequency up to about 40 percent of the sample rate (as constrained by practical anti-alias filter realization). The center frequency is controlled through the SPC interface.

For integration with the TRW MCDD the modulator is configured as an 64-kbps differentially encoded, offset quadrature phase-shift keyed (DE-OQPSK) modulator with 30 percent raised cosine shaping, 512 samples per symbol, and an aperture size of 12 (Fig. 7).

Digital Combiner/Upconverter

There are two digital combiner/upconverter (DCU) cards. One DCU processes the I channel data; the other processes the Q channel data. Each card applies gain factors to the digital I or Q outputs of as many as four modulator cards and adds them together. The DCU also anti-alias filters the analog version of this composite signal created by a companion digital-to-analog converter (DAC) card and upconverts it with a carrier provided by the quadrature oscillator board to an intermediate frequency compatible with the TRW MCDD input. A passive two-way combiner adds the two DCU outputs together to yield an $I \cos \omega t + Q \sin \omega t$ output signal structure (Fig. 8), where ω denotes frequency and t denotes time.

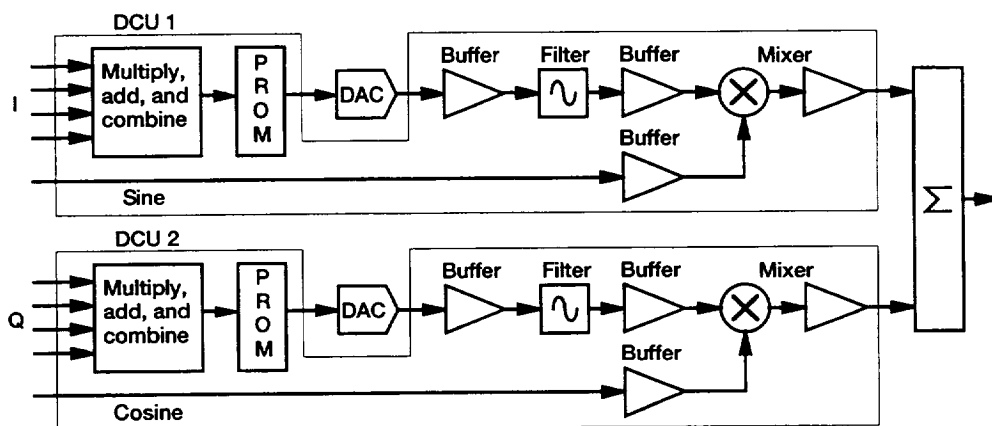


Figure 8.—Digital combiner/upconverter.

The digital weight and combined processing is implemented by a single digital four-port, multiply-and-add device. Each port of the device accepts a data stream from one of the modulator cards and a gain coefficient from one of the DCU card's computer control interface ports. The coefficients allow each port's gain to be adjusted by ± 3 dB relative to a 0-dB reference value. Each modulator output channel can be disabled by programming its associated gain coefficient to zero. In addition, a gain correction PROM allows corrections to be implemented for small variations in gain due to analog circuit resistor tolerances, differences between the two DCU cards, amplitude imbalance of the two-way combiner paths, and other factors. The two most significant bits of the PROM are established through computer control by using the SPC interface, thus allowing as many as four different gain adjustment tables to be applied to the digital data prior to analog reconstruction.

The analog input buffer ensures that the DAC board's output driver circuit and transmission line path are properly terminated. It also provides matching and input gain adjustment for the reconstruction filtering circuit.

The reconstruction filter ensures that spectral aliases of the D/A conversion process are rejected prior to intermediate-frequency upconversion. Three identical stages of linear group delay filtering are cascaded to yield good alias rejection without distorting the digital waveshapes of the DCU card outputs.

The mixer circuit accepts the reconstruction filter's output and one of the quadrature oscillator card's outputs as inputs. A state-of-the-art device is used to perform a high-fidelity, four-quadrant multiplication of the two input signals, in contrast to the conventional distortion-prone, diode-mixer-based approaches.

Composite Radiofrequency Signal

The composite radiofrequency signal is created in a three-stage process. First, the modulator cards create individual 45-kHz offset

quaternary phase-shift keying (QPSK) signals with center frequencies between 0 and 1.44 MHz. With four modulator cards adjacent-channel signals can be generated. The four QPSK signals are digitally combined in the DCU card and D/A converted. At this point the I and Q signals are a composite of the four I and Q modulator signals and are stacked in frequency between 0 and 1.44 MHz. These composite I and Q signals are then upconverted through a mixer and combined by using a passive two-way combiner, thus forming the composite radiofrequency signal (Fig. 9).

Radiofrequency Link Simulation Equipment and Multichannel Demultiplexer/Demodulator

The radiofrequency link simulation equipment and MCDD were developed under a contract with TRW.7

Radiofrequency link simulation provides the calibrated noise generation by using an MDF Products model 8151 noise generator with a bandwidth of 10 Hz to 40 MHz. The signal-to-noise ratio can be adjusted in 1-dB steps. The intermediate-frequency signal from the DCU is input to the noise generation unit. The output of the noise generation unit is bandpass filtered, amplified, and input to an analog-to-digital (A/D) converter that feeds the digitally implemented MCDD. The A/D converter is sampled at 23.04 MHz, which corresponds to the wideband channel spacing of 1.44 MHz multiplied by the number of wideband channels (eight) sampled at the Nyquist rate (1.44 MHz per wideband channel times eight times two).

The MCDD channelizes and demodulates either 2.084-Mbps or 64-kbps spectrally shaped QPSK signals. The channelizer portion of the MCDD first decomposes a composite intermediate-frequency signal into individual 1.44-MHz wideband channels. For our purposes these wideband channels are further demultiplexed into thirty-two 45-kHz narrowband channels. Either one wideband or 32 narrowband channels can be demodulated in the time-shared, multirate demodulator. Presently the demodulator

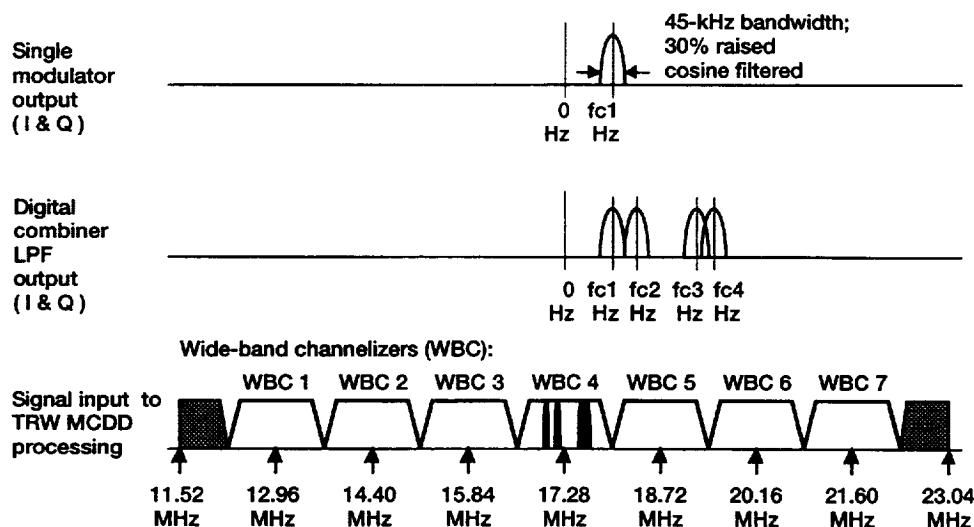


Figure 9.—Composite radiofrequency signal.

is configured to operate on a DE-QPSK signal. The demodulator outputs the following signals to the time-shared decoder: a 11.52-MHz clock, serial data (one bit indicating that valid data is available), and five bits of channel identification indicating which of 32 channels the data are associated with (Fig. 10).

Time-Shared Decoder

The time-shared decoder consists of a unique-word detector card, an encoder block-builder card, a multichannel ECC time-shared decoder card, and a data switch interface card.

Unique-Word Detector

The unique-word detector (UWD) card has been designed to detect the presence of a unique word concurrently in as many as 32 data channels. The UWD identifies the beginning of data packets for each of 32 channels and notifies the encoder block-builder card when a block has been identified and in which channel that block resides. The UWD board outputs feed the encoder block-builder card and are a delayed version of the demodulator outputs with an additional "valid correlation" signal (Fig. 11).

The UWD board's input interface section receives differential line signals from one of the TRW MCDD's demodulator output boards. The line receiver outputs are clocked into a synchronous interface FIFO, which absorbs any potential timing skew between the TRW MCDD output clock signal and the time-shared decoder system's clocks. The UWD clocks operate at 11.52 MHz.

The signal retiming function alters the received MCDD output signals with synchronous logic to create versions that are more suited to the UWD board's processing and control needs.

The retimed MCDD signals are then passed to a microcode-controlled processor that performs a multichannel unique-word

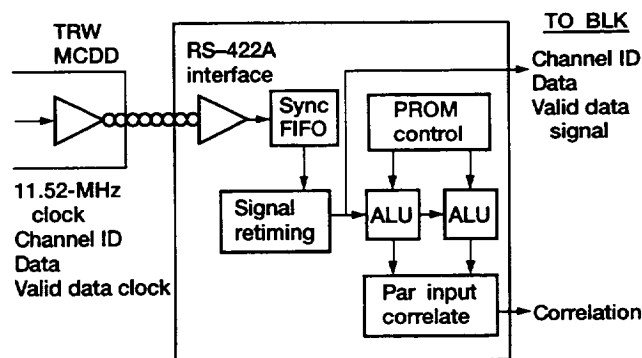


Figure 11.—Unique-word detector.

comparison function using two cascaded 6416-bit arithmetic logic units (ALU's). The ALU's internal register files are used as a set of 32 individually addressable, 32-bit serial shift registers. Each time the MCDD time-division multiplexed (TDM) canal identifies a given channel, either zero or two bits of demodulated data (i.e., one QPSK symbol's worth) are being output. When data are available, they are clocked into their assigned ALU storage register, exclusive NORed with a programmable unique-word value, and ANDed with a length selection pattern. The results of these operations are then output from the ALU.

The total number of active ALU output bits is calculated by three 11-bit registered recoders and a final sum PAL. If this number is greater than a five-bit programmable threshold value, the threshold detection circuit will create a "valid correlation" flag. This flag informs the encoder block-builder board that the unique word in a certain channel has been detected and therefore storage of an ECC block length of data from that channel should commence.

The UWD contains two SPC interfaces. One SPC register loads the unique-word value and unique-word length into the ALU's. The second SPC register holds the threshold value. The threshold

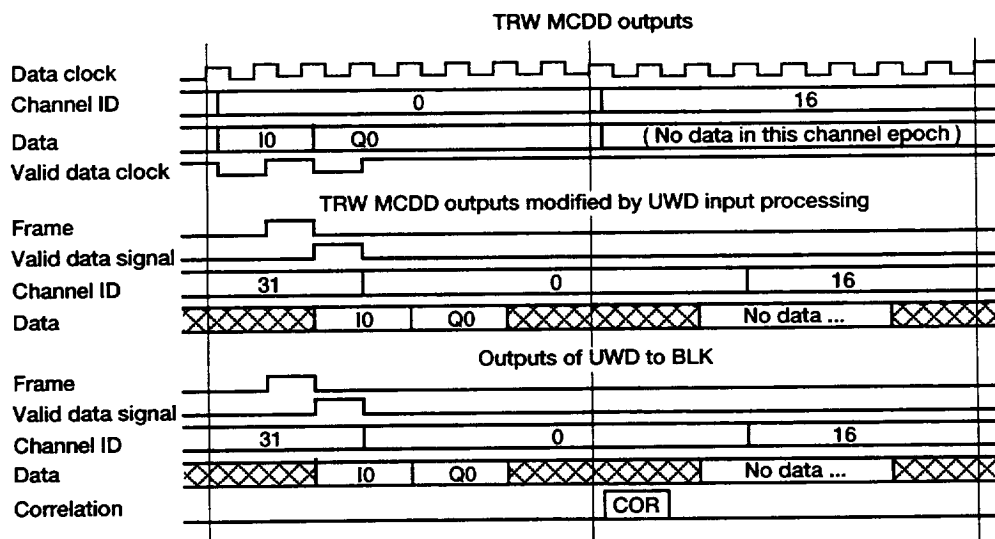


Figure 10.—Outputs of unique-word detector and multichannel demultiplexer/demodulator.

value is used to determine how many correct bits of a unique word must be received before a "valid correlation" occurs. The threshold may be set from 1 to 31 bits.

Encoder Block Builder

The encoder block builder (BLK) concurrently builds up each block for 32 separate channels and notifies the multichannel ECC decoder when a full block of data is available for decoding and in which channel it resides (Fig. 12).

Upon initialization the address ALU, the dual-port random-access memory (RAM), and block identification FIFO are cleared. The BLK waits for a valid correlation signal from the UWD. The next time that channel has data available the BLK begins building up a data block. Two microcode-controlled ALU's, a dual-port RAM, and a FIFO perform the block building. One ALU, the data ALU, is used to build up eight-bit bytes of data, two bits at a time, using the S/P function of the ALU. This data ALU builds and stores eight-bit bytes for all 32 channels concurrently. Once a byte of data has been built, those data are stored in the dual-port RAM. The second ALU, the address ALU, is used to keep track of how many bits have been stored in the data ALU and to manage the memory addressing for the dual-port RAM. A count of one is added to the address ALU every time two bits of data are stored in the data ALU. The two least significant bits out of the address ALU indicate how many bits are stored in the data ALU; the remaining bits are used as addresses to the dual-port RAM. The dual-port RAM acts as 32 individual ping-pong memories, one for each channel. While one-half of any channel's RAM is being written to, the other half is available for the multichannel ECC encoder to read (Fig. 13). The FIFO is used to indicate when a full block of data is available. Upon initialization the FIFO is cleared and its "empty flag" is reset. As soon as a block has been built, the five channel identification bits along with an additional address bit are written into the FIFO, and its empty flag is set. The additional bit is used to indicate which half of the virtual ping-pong memory should be read by the multichannel ECC decoder. The block length is controlled through the SPC interface.

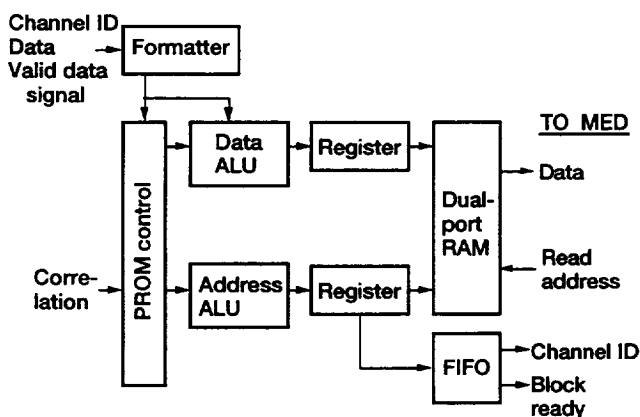


Figure 12.—Encoder block builder.

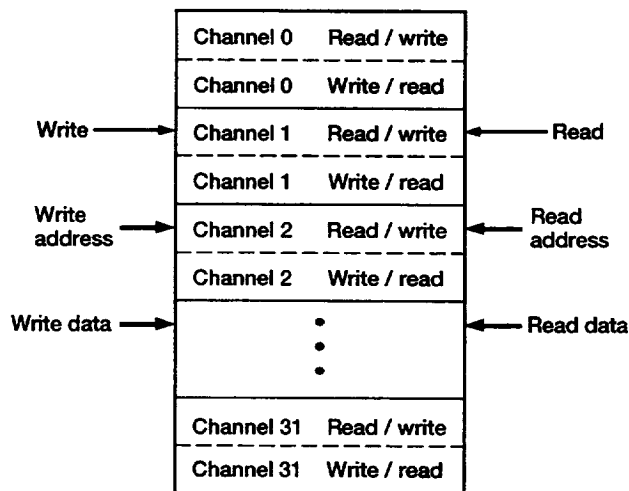


Figure 13.—Dual-port ram configuration.

Multichannel ECC Decoder

The multichannel ECC decoder (MED) decodes individual data blocks in a time-shared manner, stores the decoded blocks and channel identifiers, and notifies the data switch interface of available channels.

The MED utilizes the decoder portion of the Harris BCH codec chip. The codec chip operates at 10.52 MHz and can easily be time shared among 32 channels operating at approximately 64 kbps. Once notified by the BLK that a full data block is available, the encoded block is read from the BLK, decoded, and stored in a dual-port RAM. The DSI is then notified that a decoded block of data is available. Storage of the decoded data in the MED is similar to storage of the encoded data in the BLK. A dual-port RAM is used to store the block, and a FIFO is used to pass the channel identifier bits along, with an additional bit indicating which half of the virtual ping-pong memory is to be read. For debug and link evaluation purposes a no-code option is available. The no-code option and the block lengths are computer controlled through the SPC interface (Fig. 14).

Data Switch Interface

The data switch interface (DSI) converts the stored data in the MED to a format that can be used by either bit-error-rate test equipment or, in an operational system, by a circuit or packet switch. To interface the MED card with a bit-error-rate test set, an eight-bit parallel word from a specified channel is read from the MED and is parallel-to-serial (P/S) converted. The serial data and the uncoded data clock are passed on to the commercial bit-error-rate test set. To interface to a circuit switch, the DSI is configured as a bank of 32 P/S converters. To interface to a packet switch, the DSI has to synchronize all 32 data blocks so that the beginning of all the blocks would align. This procedure is memory intensive for an operational OBP system with as many as 1000 channels per uplink beam.

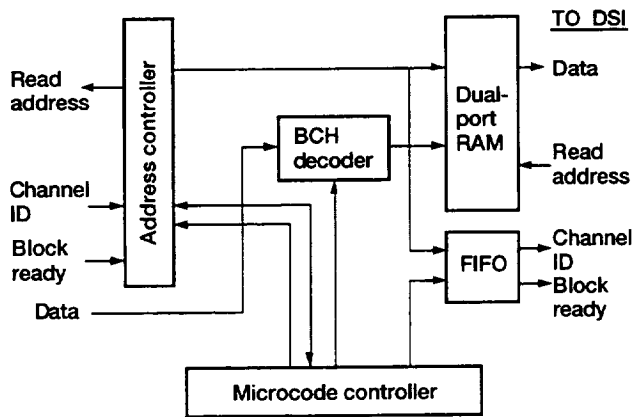


Figure 14.—Multichannel ECC decoder.

Testing

Testing will be performed to characterize the information channels through the MCDD at various signal-to-noise levels. In addition, the MCDD has degraded guard channels that may be used for transmission with inferior performance. Therefore, the guard channels will also be characterized. Some parameters to be investigated included coding block length and adjacent-channel interference.

Recommendations

The time-shared decoder described in this paper was optimized for an asynchronous mesh, very-small-aperture network where individual Earth terminals access the satellite in a frequency-division multiple access (FDMA) format and channels are not aligned at the satellite. This time-shared decoder has very good potential for application in an onboard-processing circuit switch environment because individual blocks of data can be processed and routed as soon as a full data block is available. Thus, the amount of storage memory required onboard is reduced. For applications to a packet switch in an asynchronous FDMA environment, the time-shared decoder system would have to be modified to align packets. This procedure would be prohibitively memory intensive and is not recommended. The problem, however, does not reside in the time-shared decoder but in the asynchronous uplink access scheme, which requires the onboard processing circuitry to align packets (refs. 1 to 3).

The time-shared decoder was implemented by using commercial parts—particularly, registered programmable read-only memories as the microcode controllers, programmed logic for control circuitry, dual-port random-access memories (RAM's), and 49C402 arithmetic logic units (ALU's). Many of the functions on the ALU's were not used, and many of the memories could be optimized. In conclusion, a shared decoder capable of decoding

32 simultaneous asynchronous FDMA channels could be implemented with a custom application-specific integrated circuit, two small dual-port RAM's, and a codec chip residing in a multichip module.

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