FINAL REPORT

for

DESIGN OF POWER ELECTRONICS FOR TVC EMA SYSTEMS

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TABLE OF CONTENTS

	Page
Chapter 1 - INTRODUCTION	1
Chapter 2 - PULSE DENSITY MODULATION AND THE RESONANT DC LINK INVERTER	4
Pulse Width Modulation (PWM)	4
Pulse Density Modulation (PDM)	6
The Resonant DC Link Inverter (RDCLI)	8
Chapter 3 - MOS-CONTROLLED THYRISTORS (MCT)	17
The MOS-Controlled Thyristor (MCT)	18
Inductive Switching Test	21
Chapter 4 - EXPERIMENTAL SETUP	26
The Resonant DC Link Inverter	26
The Inverter Bridge	29
Brushless DC Motor	32
Speed Control Loop Using Pulse-density Modulation	36
Chapter 5 - EXPERIMENTAL RESULTS	42
Chapter 6 - SUMMARY AND SUGGESTIONS FOR FUTURE WORK	48
Suggestions for Future Work	49
REFERENCES	51
APPENDIX	54

LIST OF FIGURES

Figure		Page
2.1	Three-phase inverter	5
2.2	Line-to-line inverter voltage for PWM operation	6
2.3	Three-phase inverter with oscillatory input voltage	7
2.4	Line-to-line voltage for PDM operation	8
2.5	Resonant dc link inverter	9
2.6	Link equivalent circuit	11
2.7	Equivalent circuits for two modes of link operation: (a) switch S open and (b) switch S closed	11
2.8	Plot of normalized capacitor voltage versus ωt	12
2.9	Plot of the normalized maximum and minimum capacitor voltages as a function of the normalized initial inductor current I_{LO}	13
2.10	Resonant dc link inverter with active clamp circuit	15
2.11	Buck output resonant dc link inverter	16
3.1	P-MCT symbol	18
3.2	P-MCT analog circuit	19
3.3	P-MCT SPICE subcircuit and +150°C device constants [8]	20
3.4	Inductive switching test circuit	21
3.5	MCT gate drive circuit	23
3.6	MCT inductive switching waveforms. Top trace: Gate-to-anode voltage. Bottom trace: Anode-to-cathode voltage	24
3.7	MCT inductive switching waveforms at turn off. Top trace: Gate-to-anode voltage. Bottom trace: Anode-to-cathode voltage	24
3.8	MCT inductive switching waveforms at turn on. Top trace: Gate-to-anode voltage. Bottom trace: Anode-to-cathode voltage	25
3.9	MCT inductive switching waveforms. Top trace: Cathode-to-anode voltage. Bottom trace: Device current	25
4.1	Circuit diagram of the resonant dc link	27

4.2 Circuit diagram of the resonant dc link with electronic components..... 28

4.3 Drive circuit for the resonant switch S and the synchronizing switch S7..... 29

4.4 Circuit diagram of the inverter bridge with IGBT's..... 30

4.5 Drive circuit for one leg of the IGBT inverter..... 31

4.6 The drive circuit for the MCT..... 32

4.7 Open loop resonant dc link inverter driven brushless dc motor system..... 32

4.8 Brushless dc motor hall effect signals with corresponding phase currents..... 34

4.9 Brushless dc motor hall effect signals with corresponding switching signals..... 34

4.10 Stator voltage applied when pairs of switches are conducting..... 35

4.11 Hall effect signal decoder for the brushless dc motor..... 35

4.12 PDM control system for a brushless dc motor..... 36

4.13 Circuit diagram of the summer and PI controller for the PDM control system..... 37

4.14 Circuit diagram of the current loops of the PDM control system..... 40

4.15 Circuit diagram of the brushless dc motor hall effect decoder and the PDM signals, which create the drive signals for the inverter switches..... 41

5.1 Resonant dc link voltage waveform..... 42

5.2 Brushless dc motor hall effect signals and corresponding phase currents..... 43

5.3 One phase of the brushless dc motor hall effect signals and its corresponding phase current..... 43

5.4 Oscilloscope plot of the phase current under loaded conditions with the IGBT inverter..... 44

5.5 Oscilloscope plot of the phase current under loaded conditions with the MCT inverter..... 44

5.6 Inverter drive signals: (Top: Open loop operation; Bottom: PDM operation)..... 45

5.7 PDM regulated current of the brushless dc motor..... 46

5.8 Brushless dc motor hall effect signal and current of 2 amperes..... 46

5.9 Brushless dc motor hall effect signal and current of 4 amperes..... 47

5.10 Brushless dc motor hall effect signal and current of 5 amperes..... 47

Chapter 1

INTRODUCTION

Hydraulic and pneumatic actuation systems are currently utilized in many aerospace vehicles. These systems have many drawbacks. Their weight is often quite high because they require a central pump and a tank with sufficient capacity for fluid storage. Safety issues are related to the presence of high pressures in these systems and to leaks of potentially hazardous fluids. These concerns may be amplified in space where outgassing may decrease seal lifetime. In addition, outgassing and leakage may not be acceptable in sensitive environments. Hydraulic systems also present problems in the area of reliability and robustness (a leak at one point in the system can degrade the performance of the entire system). Electrohydraulic systems are a decentralized approach for hydraulic systems. The central pumping system is eliminated in favor of local hydraulic systems pressurized by smaller pumps, which in turn are driven by electric motors. However, problems with leaks and outgassing still exist.

Electromechanical actuation systems offer many improvements over these systems. System reliability and efficiency are increased. The weight of the system can be reduced through the elimination of the central pump and fluid storage tank. Safety improvements are possible through the elimination of hazardous fluids and high pressures. Maintenance and operating costs are reduced as well as check-out and replacement times. Other benefits of the electromechanical approach are higher bandwidth for servo control, high stiffness, reduced dynamics between the flight computer and load, and easier redundancy management.

The Component Development Division of the Propulsion Laboratory at Marshall Space Flight Center (MSFC) is currently developing a class of Electromechanical Actuators (EMAs) for use in space transportation applications such as Thrust Vector Control (TVC)

and Propellant Control Valves (PCV). These high power servomechanisms will require rugged, reliable, and compact power electronic modules capable of modulating several hundred amperes of current at up to 270 volts. MSFC has selected the brushless dc motor for implementation in EMAs. This report presents the results of an investigation into the applicability of two new technologies, MOS-Controlled Thyristors (MCTs) and Pulse Density Modulation (PDM), to the control of brushless dc motors in EMA systems.

MCTs are new power semiconductor devices, which combine the high voltage and current capabilities of conventional thyristors and the low gate drive requirements of metal-oxide-semiconductor-field-effect transistors (MOSFETs) [8]. Conventional thyristors are turned on by applying a current pulse to their gate; however, it may not be turned off by applying a current pulse of the opposite polarity to the gate. Gate-turnoff thyristors (GTOs) are available which can be turned off by applying a negative current pulse to the gate. However, the amplitude of this current pulse typically might be 1/5 of the current flowing through the device. As a result, a GTO carrying 200 A might require a 40 A gate pulse to turn it off. The gate drive requirements of the MCT are much less than the GTO since only a small current is required to turn it off. The combination of low gate drive requirements and high current ratings make the MCT attractive for this application.

Compared to pulse width modulation (PWM), PDM has only recently been applied to the control of induction motors [14]. The commanded signals in a PDM system are synthesized using a series of sinusoidal pulses instead of a series of square pulses as in a PWM system. A resonant dc link inverter is employed to generate the sinusoidal pulses in the PDM system. This inverter permits zero-voltage switching of all semiconductors which reduces switching losses and switching stresses [1,2,6,7].

The objectives of this project were as follows:

1. Develop and validate an analytical model (e.g., a SPICE hybrid parameter model) of the MCT device when used in high power motor control applications.

2. Design, fabricate, and test a prototype electronic circuit employing both MCT and PDM technology for controlling a brushless DC motor.

This report is organized as follows. The next chapter compares PWM and PDM. Then the resonant dc link inverter is presented and its operation discussed. Chapter 3 presents the MCT and its operation. An equivalent circuit and results from inductive switching tests are presented in this chapter. The brushless dc motor speed servo which was constructed to test PDM and MCTs is described in chapter 4. The experimental results obtained from the speed servo are presented in chapter 5. The final chapter summarizes the project and gives suggestions for future work.

Chapter 2

PULSE DENSITY MODULATION AND THE RESONANT DC LINK INVERTER

One of the objectives of this project was an investigation into the application of PDM to the control of brushless dc motors. This chapter will begin with a brief comparison of PWM and PDM. Implementation of a PDM scheme requires a resonant dc link inverter, which is derived from a standard three-phase inverter by the addition of a waveshaping circuit. Analysis and operation of the resonant dc link inverter will also be described

Pulse Width Modulation (PWM)

Since PWM has been employed for the control of electric motors for many years [15], it is very well understood but remains an active research area. A brief description of PWM will be given with the help of Figure 2.1 which shows a three-phase inverter. This circuit utilizes insulated gate bipolar transistors (IGBTs) as the switching devices. Note that the input to this circuit is a "hard" dc source. With this type of source, it is imperative that the two switches in each leg of the inverter are not turned on together. This condition is referred to as inverter shoot-through and results in destruction of the semiconductor switches and is easily prevented by adding delay to the control signals which turn on and off these switches.

Figure 2.2 shows the type of waveform that is typically produced by the circuit of Figure 2.1. The voltage V_{ab}, which is plotted in Figure 2.2, is a series of square pulses of equal height but varying width. Many different schemes have been developed to determine the switching instants for the pulses [15]. An infinite number of switching instants exist with this scheme. As a result, both the frequency and magnitude of the voltage V_{ab} may be controlled very accurately.

The main disadvantages of PWM are high switching stresses and high switching losses, particularly in high power applications. The semiconductor switches have two types of losses: switching and conduction. The latter are ohmic losses due to the resistance of the devices. Switching losses occur when a device transitions from the on state to the off state and vice versa. When driving an inductive load such as an electric motor, the inverter switches have to turn on or off large currents. During turn on, the voltage across the inverter switch changes from the bus voltage V_s to a small on-state voltage. The reverse occurs during turn off - the voltage begins at a small value and ends up at the bus voltage. The power loss associated with these transitions are the switching losses. These losses, of course, will increase with switching frequency. Another problem associated with switching an inductive load are voltage spikes. Snubbers may be added to the circuit of Figure 2.1 to help reduce the switching stresses. The switching losses in the inverter switches may be reduced by the snubbers, but the overall efficiency remains the same because the power loss has been transferred from the inverter switches to the snubbers.

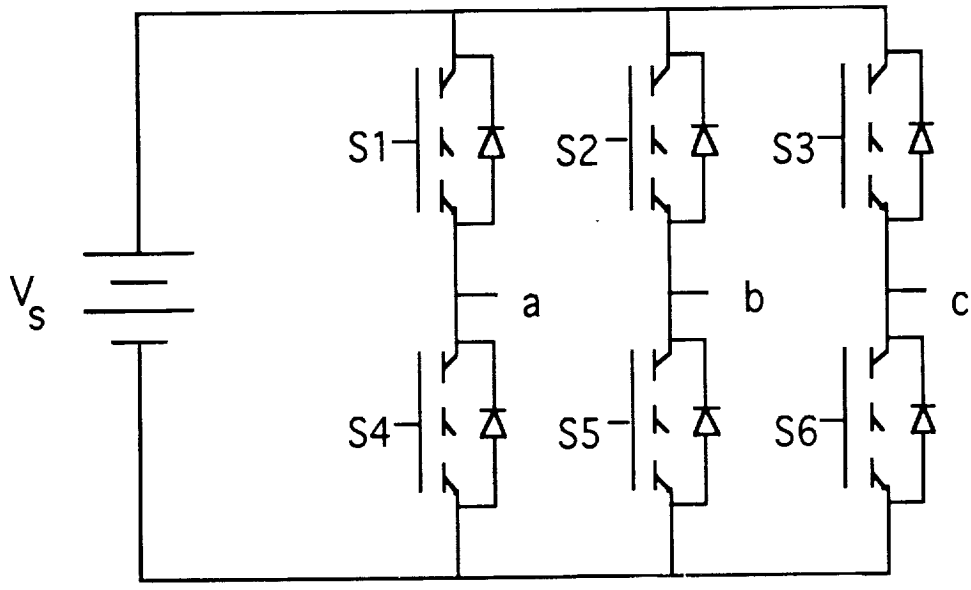


Figure 2.1. Three-phase inverter.

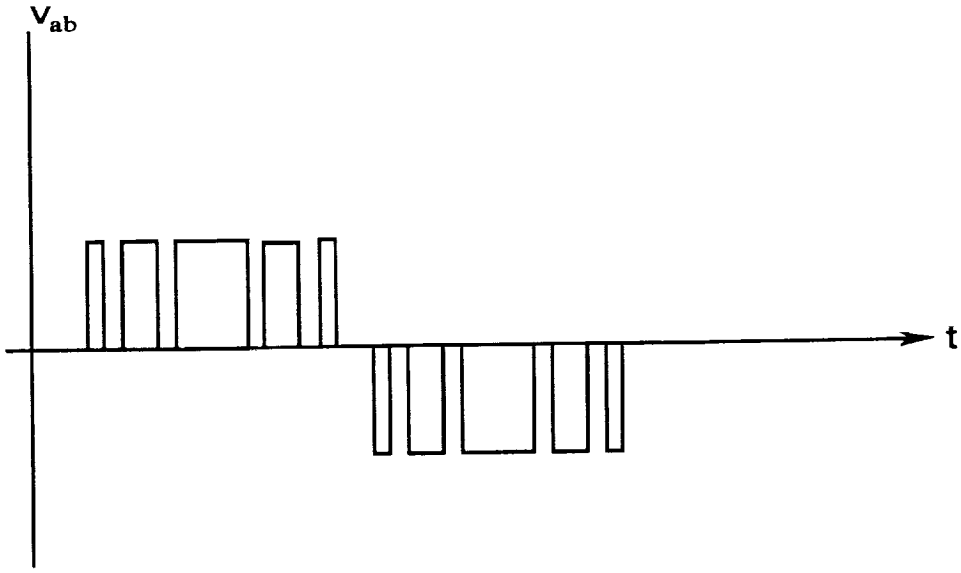


Figure 2.2. Line-to-line inverter voltage for PWM operation.

Pulse Density Modulation (PDM)

The inverter in a PWM system has a fixed dc input voltage as seen in Figure 2.1. In a PDM system, the inverter input voltage is not constant but oscillatory, resonating to zero periodically [1,2] as seen in Figure 2.3. All switching of inverter switches takes place when the input voltage is at zero; as a result, the switching losses are zero. Since the switching losses are now zero, the switching frequency of the inverter can be increased for improved circuit performance. In addition, the inverter switches are not subjected to switching stresses so snubbers are not needed.

The PDM system is not without its problems. The inverter must be controlled such that its input voltage oscillates to zero each cycle. For the input voltage to return to zero may require that its peak value be 2.5 to 3 times higher than the bus voltage. The control of the inverter is more complicated because all switching is synchronized to the zero crossings of the input voltage, which requires sensing of the input voltage. The number of switching instants in the PDM system is less than those in the PWM system. As a result, the control of the desired system variables may not be as accurate as that obtained with a PWM

system. This may be offset by the higher switching frequency which can be obtained with the PDM system.

Recall that the voltage V_{ab} for the PWM system is a series of square pulses of the equal height but different widths as shown in Figure 2.2. The input voltage to the inverter in the PDM system is a series of sinusoidal pulses. Figure 2.4 shows that the voltage V_{ab} in the PDM system is also a series of sinusoidal pulses. The desired system variables are now regulated by the density of pulses in V_{ab}. For example, if the current flowing in the motor is below the desired value, the density of pulses will be increased. Likewise, if the current is too large, the density of pulses will be decreased.

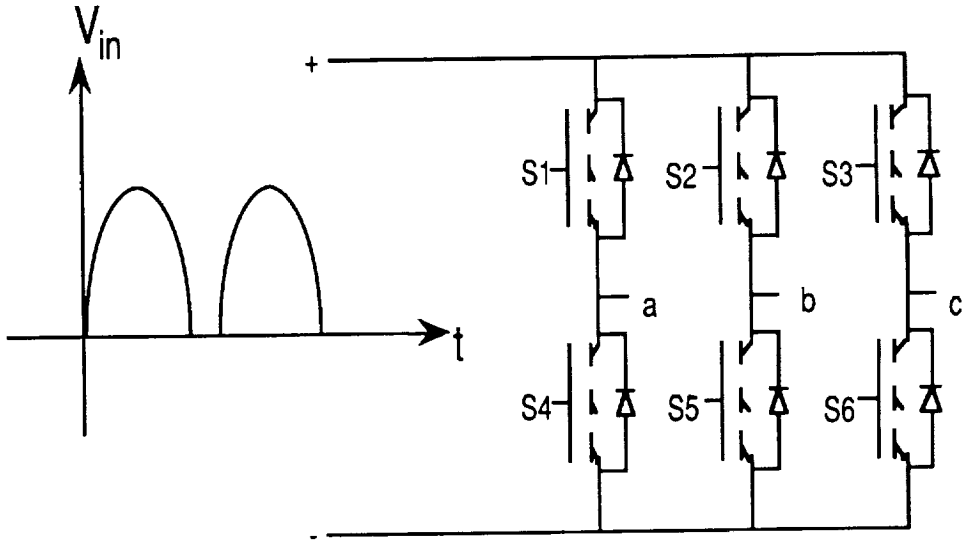


Figure 2.3. Three-phase inverter with oscillatory input voltage.

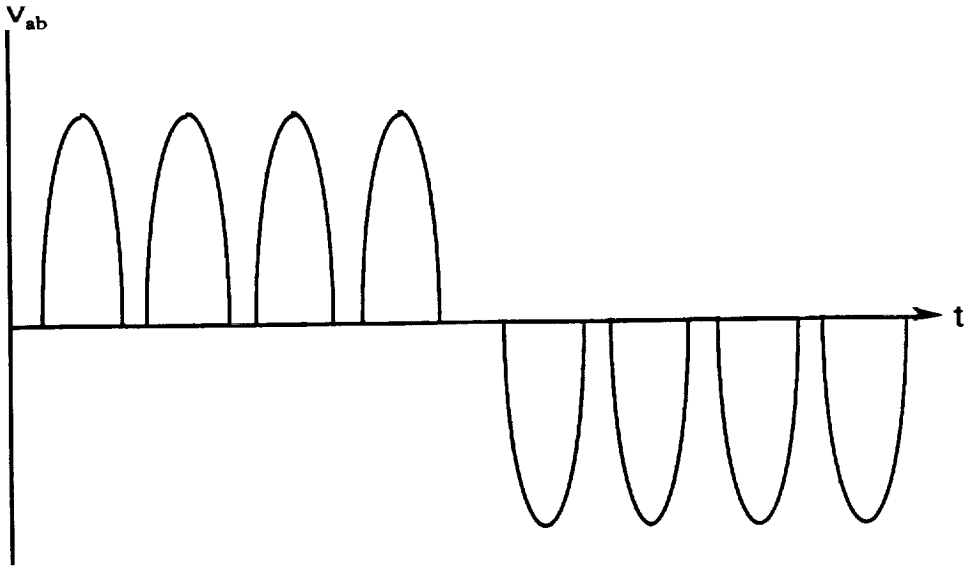


Figure 2.4. Line-to-line voltage for PDM operation.

The Resonant DC Link Inverter (RDCLI) [1,2,5,6,7]

The voltage source inverter of Figure 2.1 must be modified to produce sinusoidal voltage pulses. This can be accomplished with the addition of 4 components as shown in Figure 2.5. The inductor, capacitor, diode, and switch form a waveshaping network to produce the sinusoidal voltage pulses at the input to the inverter. The circuit in Figure 2.5 is referred to as a resonant dc link inverter (RDCLI).

The operation of the RDCLI will now be described. Assume that switches S1-S6 are open and that the voltage across the capacitor C is zero. Switch S is now closed and current begins to increase in the inductor. After a certain time period, switch S is now opened. The dc source, inductor, and capacitor form a resonant circuit. The voltage across the capacitor now begins to increase sinusoidally, reaches a peak value, and then returns to zero. When the voltage across the capacitor tries to go negative, the diode in parallel with switch S turns on clamping the inverter input voltage to zero. At this point, switch S is again turned on holding the inverter input voltage at zero while the current in the inductor builds up again. Switches S1-S6 change states during the interval that the inverter input

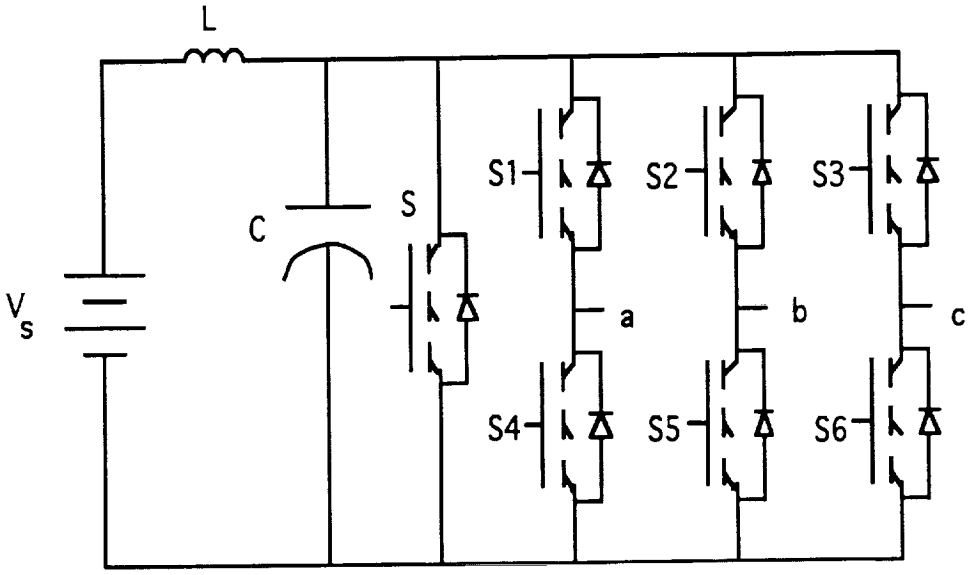


Figure 2.5. Resonant dc link inverter.

voltage is clamped at zero. Switch S is switched at zero voltage except for the first time it is opened.

The section of the circuit between the dc voltage source V_S and the inverter is referred to as the link. The characteristics of the link will now be described using the equivalent circuit of Figure 2.6. In this circuit, the load is treated as a constant current source for analysis purposes. This is a valid approximation because the frequency of the link quantities is much faster than the frequency of the motor current. The assumed positive direction of the current source I_x is as indicated in this figure. Note that it is possible that the numerical value of this source could be negative depending on the status of switches S1-S6.

The equivalent circuit of Figure 2.6 can be described by two modes of operation. The first mode corresponds to switch S being closed and is described by the circuit of Figure 2.7a. An open switch S characterizes the second mode, which is represented by the circuit of Figure 2.7b. For mode 1, assume that the inductor current i_L has an initial value of I_{LA}. Equation (2.1) gives the solution for the inductor current in mode 1. The capacitor

voltage v_C is zero during this mode because switch S is closed. The value of the inductor current at the end of this mode will be designated I_{L0} and depends on T_{on}, the on time for switch S.

$$i_L(t) = \frac{V_s}{L} t + I_{LA} \tag{2.1}$$

Analysis of Figure 2.7b yields the following equations for the inductor current i_L and the capacitor voltage v_C [3,4]. The parameters in these equations are described below.

$$i_L(t) = I_x + e^{-\alpha t}\left[[I_{L0} - I_x]\cos\omega t + \frac{2V_S - (I_x + I_{L0})R}{2\omega L}\sin\omega t\right] \tag{2.2}$$

$$v_C(t) = (V_s - I_x R)\left[1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\alpha t}\sin(\omega t + \theta)\right] + \frac{(I_{L0} - I_x)Z_r}{\sqrt{1-\xi^2}} e^{-\alpha t}\sin\omega t \tag{2.3}$$

$$Z_r = \sqrt{L/C} \qquad \alpha = R/2L \qquad \xi = R/2Z_r$$

$$\theta = \cos^{-1}(\xi) \quad \omega_r = 1/\sqrt{LC} \quad \omega = \omega_r\sqrt{1-\xi^2}$$

A plot of the normalized capacitor voltage for a given set of parameters is given in Figure 2.8. Equation (2.3) is normalized by the source voltage V_S for this plot. Note that the positive peak voltage reaches approximately twice the source voltage. Recall that to achieve zero-voltage switching the capacitor voltage must go negative so that the diode will clamp it at zero. The normalized capacitor voltage of Figure 2.8 does go negative for this example indicating that the link will operate properly.

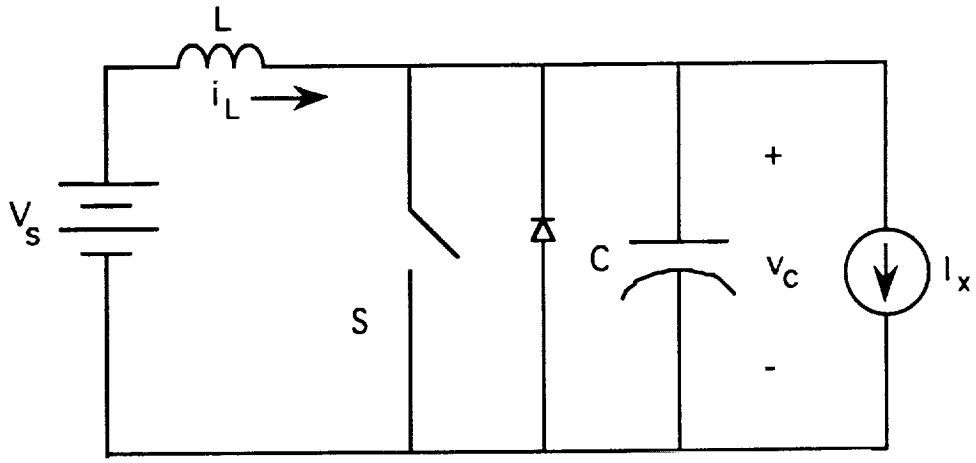
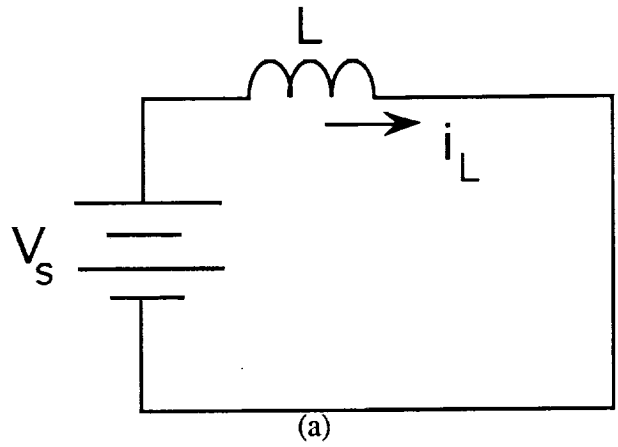
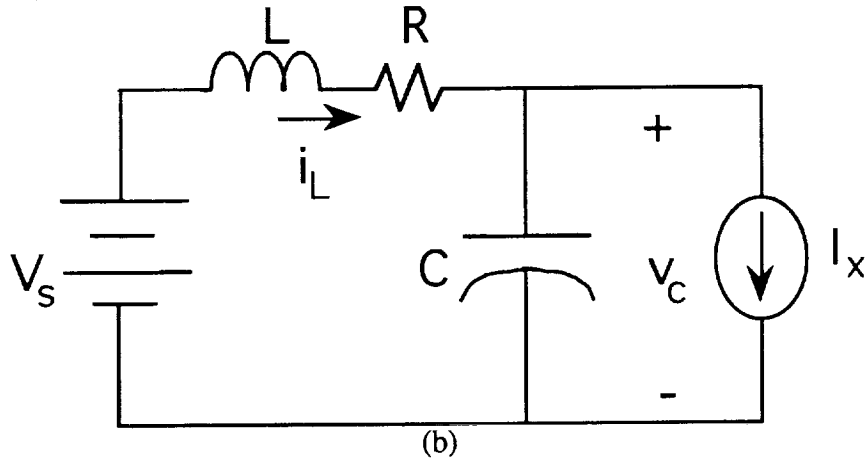


Figure 2.6. Link equivalent circuit.



(a)



(b)

Figure 2.7. Equivalent circuits for two modes of link operation: (a) switch S open and (b) switch S closed.

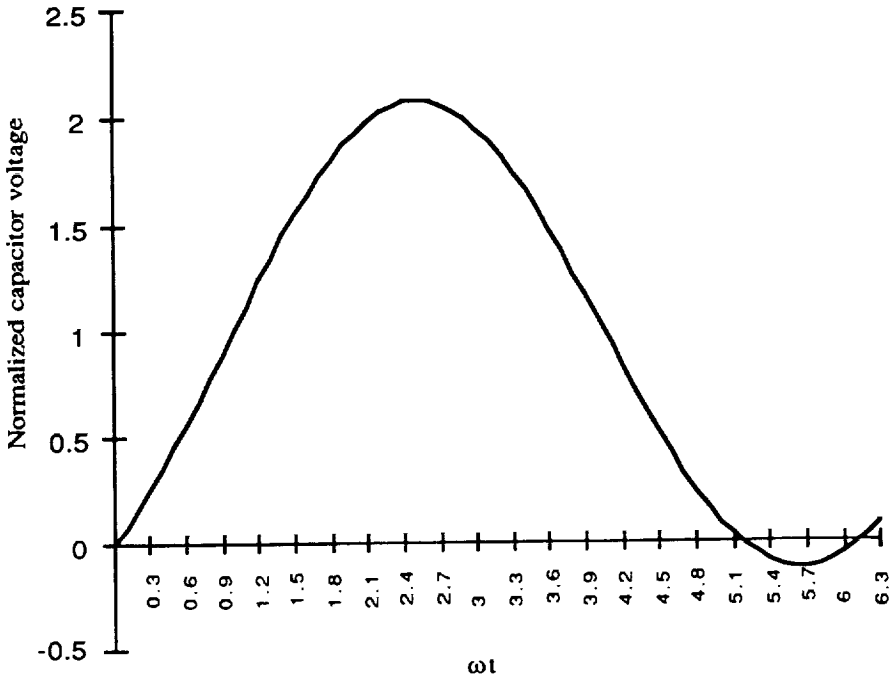


Figure 2.8. Plot of normalized capacitor voltage versus ωt.

Two parameters of interest for the capacitor voltage are the positive and negative peak voltages. The positive peak voltage is of interest because it determines the voltage rating of the motor supplied by the RDCLI. Of more importance is the negative peak voltage because it indicates that zero-voltage switching is occurring. Using calculus, equation (2.3) may be solved for the times at which the positive and negative peak voltages occur. These times are given in equations (2.4) and (2.5) [3,4].

$$\omega t_{max} = \pi + \tan^{-1}\frac{2\sqrt{1-\xi^2}(I_x - I_{LO})Z_r}{2V_s - (I_x + I_{LO})R} \tag{2.4}$$

$$\omega t_{min} = 2\pi + \tan^{-1}\frac{2\sqrt{1-\xi^2}(I_x - I_{LO})Z_r}{2V_s - (I_x + I_{LO})R} \tag{2.5}$$

The normalized positive and negative peak capacitor voltages can be calculated by substituting the times obtained from equations (2.4) and (2.5) into equation (2.3). Figure 2.9 shows a plot of these normalized peak values as a function of the normalized value of the initial inductor current I_{LO}. The circuit parameters used for this plot are the following:

$V_S = 1.0$ $L = 3.0$ $C = 1.0$ $R = 0.05$ $I_X = 1.0$

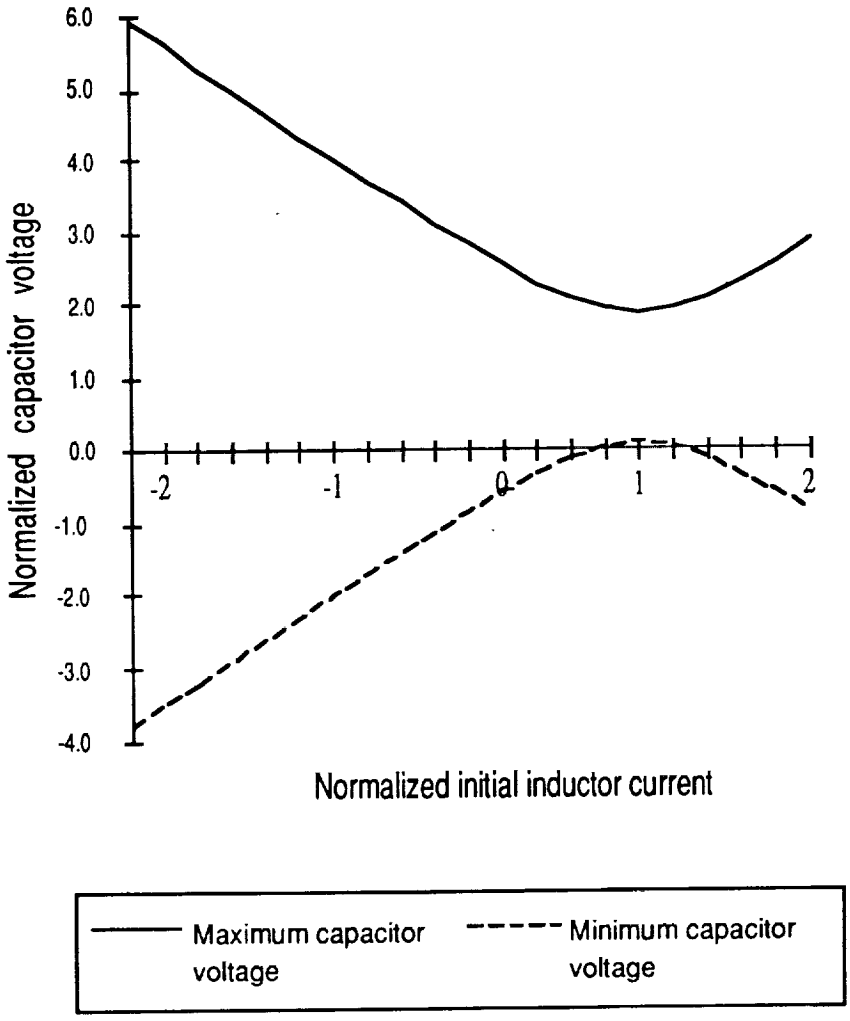


Figure 2.9. Plot of the normalized maximum and minimum capacitor voltages as a function of the normalized initial inductor current I_{LO}.

The positive peak or maximum capacitor voltage has a minimum value of approximately 2.0 when $I_x=I_{L0}$. This can also be determined by inspection from equation (2.3). The maximum voltage increases as the difference between I_x and I_{L0} and can become quite large. Referring to the circuit of Figure 2.6, the difference between the two currents flows into the capacitor; the amount of energy stored in the capacitor and thus the capacitor voltage increases with this current difference. A more important result is demonstrated by the plot of the negative peak or minimum capacitor voltage. For values of current difference (I_x-I_{L0}) very small, the normalized capacitor is not negative but positive which indicates that zero-voltage switching is lost.

One circuit adjustment to ensure that the capacitor voltage will go negative is through the on time of the switch S. As stated previously, the value of the inductor current at the end of mode 1, I_{L0}, depends on the on time T_{on}. The current difference depends on both the load current and the inductor current; therefore, a particular on time may not provide zero-voltage switching over a wide range of load currents. It is possible through experimentation to select an on time which does permit zero-voltage switching.

Figure 2.9 illustrates one problem for this circuit as a component in the EMA system. This system will operate from a 270 Vdc bus. Depending on the load current, the peak value of the capacitor voltage may reach values on the order of 550 V. The power system for the EMA is not allowed to have this type of overvoltage. One possible solution to this problem is to somehow clamp the capacitor voltage at some prescribed level. This can be accomplished with the addition of an active clamp circuit to the RDCLI [2] as shown in Figure 2.10. The switch S, which was shown in an earlier circuit, is not included in this figure. Its function of charging the inductor and holding the inverter input voltage at zero may be performed by switch pairs S1-S4, S2-S5, and S3-S6. Recall that this was not permitted in the PWM inverter; it is permissible here because of the inductor L.

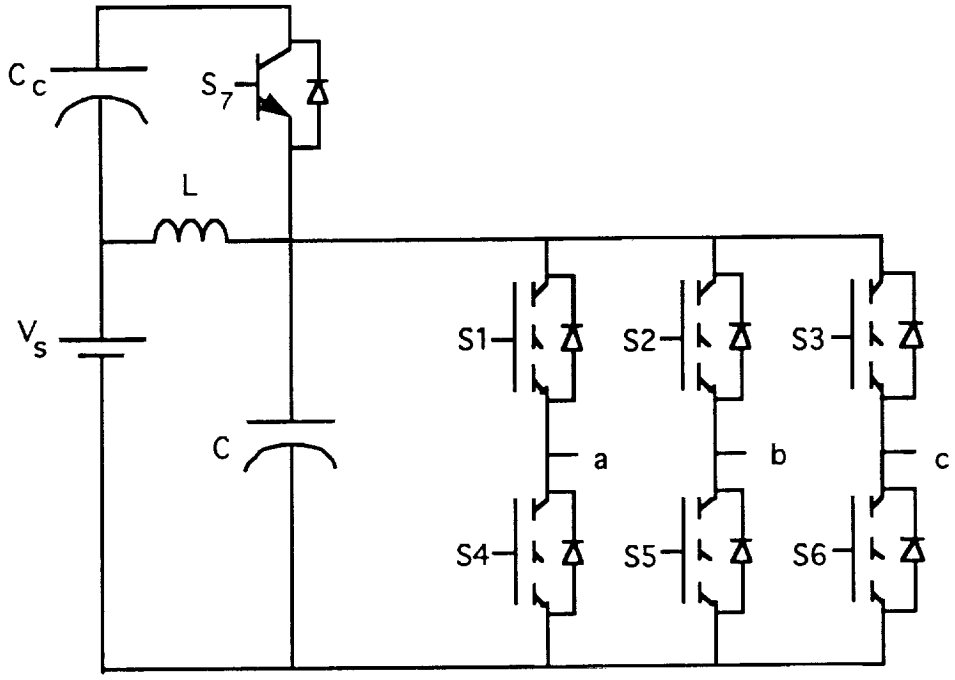


Figure 2.10. Resonant dc link inverter with active clamp circuit.

The RDCLI with active clamp circuit works as follows. Assume that the capacitor C_c is charged some value $(k-1)V_s$ where $k > 1$. Charging of the inductor is initiated with the closing of one of the three switch pairs: S1-S4, S2-S5, or S3-S6. After the inductor current has increased to the desired value, one of the switches in the pair is opened and the capacitor voltage begins to increase as before. When this voltage reaches kV_s, the diode in anti-parallel with switch S7 turns on clamping the capacitor voltage at kV_s. Energy is now transferred from capacitor C to capacitor C_c. While current is flowing through this diode, switch S7 can be turned on at zero voltage. Current will flow from C to C_c and then reverse and flow through S7. Switch S7 is held on until the amount of energy transferred from C_c to C equals that transferred from C to C_c. Switch S7 is turned off under current but at zero voltage so that the switching losses are zero. Since the same amount of energy taken out of the dc link is returned from C_c to the link, the capacitor voltage will continue to decrease until it reaches zero at which time the diodes in the inverter will clamp.

The capability of clamping the dc link voltage has not been achieved without a penalty. Additional circuit components have been added which will decrease the efficiency. Circuit operation is now more complex because of the extra switch. Since k cannot be less than 1.3 [2], the link voltage may not fall within the voltage restrictions for the EMA.

An alternative circuit for clamping the link voltage at the input voltage value is given in Figure 2.11. This circuit is referred to as the buck output RDCLI [2]. The constant k is less than 1 for this circuit. The operation of this circuit was not investigated in this project.

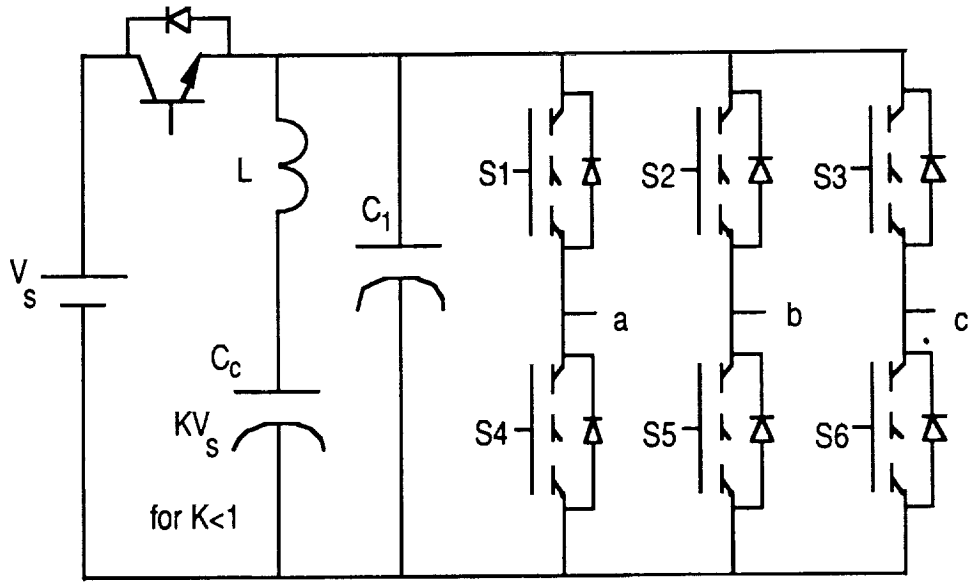


Figure 2.11. Buck output resonant dc link inverter.

Chapter 3

MOS-CONTROLLED THYRISTORS (MCT) [8]

The thyristor or SCR (silicon-controlled rectifier) was developed by General Electric Research Laboratories in 1957 [15]. It is one of the oldest power semiconductor devices and was one of the key elements in the evolution of the power electronics field. Even though many power semiconductor devices have been developed since 1957, the thyristor still has the highest power-handling capability. The thyristor is turned on by applying a pulse of current to the gate of the device at which time it latches on. It cannot be turned off by applying a current pulse of opposite polarity to the gate; the current flowing through the device must be reduced below a minimum level or the device must be reverse biased to cause it to turn off. Gate-turnoff thyristors (GTO) are available which can be turned off by applying a negative current pulse to the gate. The amplitude of this current pulse, however, typically might be 1/5 of the current flowing through the device. For example, a GTO carrying 200 A might require a 40 A gate pulse to turn it off.

The desire to have a power semiconductor device which has the power-handling capability of the thyristor and can be turned on and off quite easily led to the development of the MOS-Controlled thyristor (MCT) by Harris Semiconductor [8]. The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a semiconductor device which has extremely low gating requirements. The gate structure of the MOSFET has been integrated with a bipolar device to produce the Insulated Gate Bipolar Transistor (IGBT). The same concept has been employed in the MCT - a MOSFET gate structure has been integrated with a conventional thryristor. As a result, the MCT retains the high voltage and current capabilities of the thyristor while its turn on and turn off are easily controlled by the application of a small positive or negative current pulse to its gate. These characteristics make the MCT attractive for high power applications.

This chapter discusses some of the characteristics of the MCT. A four transistor analog circuit is used to descibe its operation. A SPICE model developed by Harris for this analog circuit is given. The MCT has been tested in an inductive switching test and the results are presented. The gate drive circuit used in the testing is also given in this chapter.

The MOS-Controlled Thyristor (MCT)

Figure 3.1 shows the symbol for the MCT with gate, cathode, and anode terminals labelled. This symbol is for a P-MCT - a device which has a blocking region that is P-type. The first devices produced by Harris are P-MCTs because an N-channel Off-FET can turn off 2 - 3 times the current density than a P-channel Off-FET [8]. Even though P-type devices are currently the only devices available, Harris is in the process of developing N-type devices designated as N-MCT's.

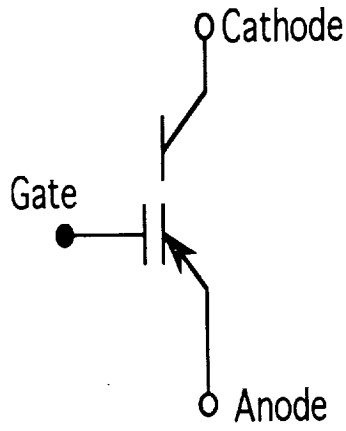


Figure 3.1. P-MCT symbol.

The operation of conventional thyristors has often been described in terms of a two transistor analog circuit [15]. The addition of two MOSFET transistors to this analog circuit yields a circuit which can be used as an aid in describing the operation of the MCT. This MCT analog circuit is shown in Figure 3.2. The NPN and PNP bipolar transistors are the components in the analog circuit for the conventional thyristor. The circuit of

Figure 3.2 contains a P-channel and a N-channel MOSFET. The application of a negative gate-to-anode voltage turns on the P-channel MOSFET which causes the MCT to turn on. This is equivalent to the application of a gate pulse to the gate of a conventional thyristor. The P-channel MOSFET is often referred to as the ON FET. MCT turn off is accomplished by the application of a positive gate-to-anode voltage, which turns the N-channel MOSFET on. With the N-channel MOSFET on, base current is shunted away from the PNP bipolar transistor turning it off. This N-channel MOSFET is referred to as the OFF FET. Operation without a gate-to-anode voltage is not recommended because the input terminals of the conventional thyristor structure are not terminated.

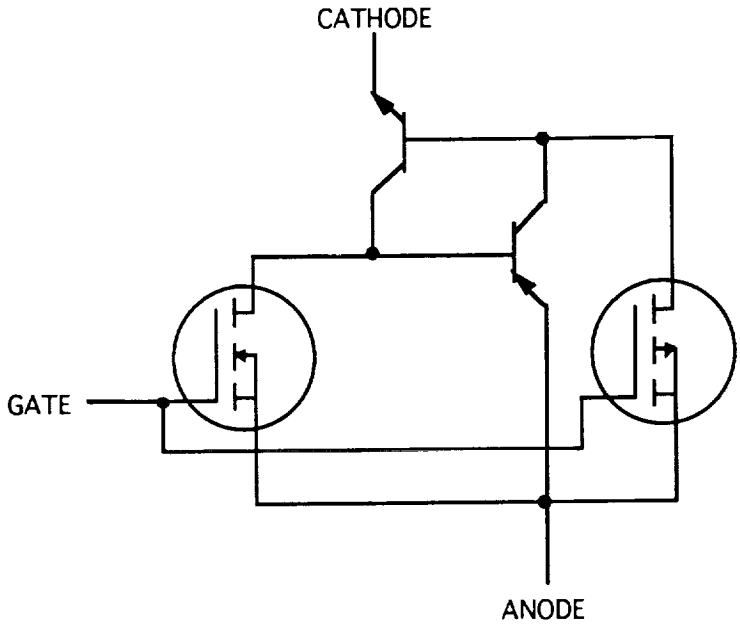


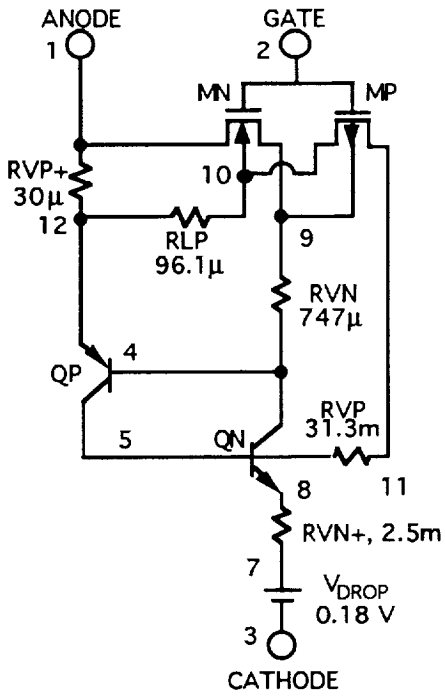
Figure 3.2. P-MCT analog circuit.

Appendix A contains a data sheet for an MCTA75P60 MCT. This device is a P-channel MCT which has a continuous current rating of 75 A and a rated blocking voltage of 600 V. Two points of interest from this data sheet are the peak reverse voltage and the peak controllable current. Since the MCT is not designed to be a reverse blocking device, the peak reverse voltage for the MCTA75P60 is only 10 V. Utilization of these devices in

an ac application will require that a diode be connected in series with the device. The peak controllable current for the MCTA75P60 is 120 A. Attempts to turn off more current than this will possibly destroy the device.

One of the objectives of this work was to develop and validate an analytical model for the MCT. Validation of the MCT model has not been possible due to the limited number of devices which could be obtained. Approximately eight devices were obtained from NASA/MSFC and another eight were left over from a previous research project at Auburn University on high temperature characterization of MCT's. Since six devices are needed for a three-phase inverter, only a small number of the sixteen total devices were available for testing. As a result, it was not possible to perform detail device testing in order to validate a device model.

Other researchers [9-13, 16] have studied the MCT and proposed models for it. The SPICE model presented here was developed by Harris Semiconductor. The reader is referred to Section 3 of [8] for more detail.



	QP	QN
BF	9.1	2.75
VAF	2000	2000
IKF	600	600
IS	1.14E-10	1.14E-10
TF	42.9ns	207ns
CJE	9.47nF	1.25nF
VJE	1.0	0.66
CJC	362pF	362pF
MJC	0.5	0.5
VJC	0.64	0.64

	MN	MP
L	0.5	5.0
W	5.63	0.715
NSUB	1E18	8E13
U	500	200

Figure 3.3. P-MCT SPICE Subcircuit and +150°C Device Constants [8].

Inductive Switching Test

One test which was performed on the MCT's was the inductive switching test. This test allows examination of MCT performance under hard switching conditions. The test setup is shown in Figure 3.4. The input voltage is shown as negative since the MCT is P-type. For this test, the MCT is switched at different frequencies with different resistances and inductances, and the device voltages and current are monitored with an oscilloscope.

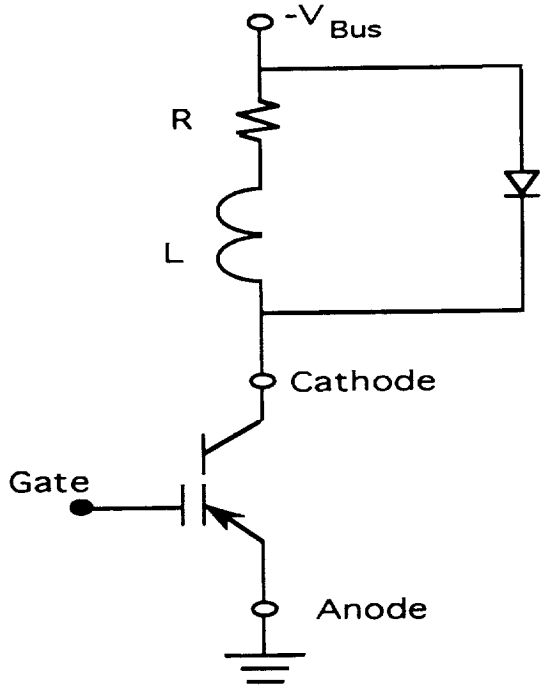


Figure 3.4. Inductive switching test circuit.

The gate-to-anode voltage for the MCT is provided by the drive circuit of Figure 3.5. The 555 timer is connected in the astable mode with two potentiometers so that the frequency and duty cycle of the drive signal may be varied. The 1 Ω resistor connected to the gate of the MCT influences its turn-on and turn-off times. The 10 kΩ resistor provides a continuous connection between gate and anode of the device. The 2222 and 2907 transistors act as a buffer to provide current to turn the MCT on and off rapidly. When the output of the 555 timer is high, the 3904 is turned on which pulls the base of the 3906 low turning it on. With the 3906 on, +V is tied to the 2222 turning it on and supplying a positive voltage between the gate and anode of the MCT turning it off. For a low 555 timer output, the 3904 is turned off which supplies a positive voltage to the base of the 3906 turning it off. A negative voltage is then applied to the base of the 2222/2907 combination turning on the 2907 and applying a negative voltage to the gate of the MCT turning it on. The 2.2 kΩ resistor slows down the turn on of the MCT because it slows down the turn on of the 2907. The 0.001 μF capacitor in the base circuit of the 3906 increases the switching speed of this device.

Figure 3.6 shows the gate-to-anode and anode-to-cathode voltage for the circuit of Figure 3.4. The top trace shows the gate-to-anode voltage which alternates between +15 V and -15 V at a frequency of approximately 20 kHz. When the gate-to-anode is negative, the device is on as indicated by an anode-to-cathode voltage of appoximately 0 V. A positive gate-to-anode voltage yields an anode-to-cathode voltage of approximately 70 V, which is the value of V_{BUS} for this test. Note that there is a voltage spike on the anode-to-cathode voltage at turn off due to the inductive load.

Figure 3.7 gives a more detailed waveform for the turn-off conditions. The MCT turns off in approximately 1μs as measured from the point where the gate-to-anode voltage goes positive. Note that the voltage spike on the anode-to-cathode voltage reaches about 110 V for this case. Figure 3.8 shows the turn-on waveforms for the same operating conditons as Figures 3.6 and 3.7. Note that the MCT turns on very rapidly once the gate-

to-anode voltage reaches zero, which happens in about 450 ns after the gate-to-anode voltage begins to decrease.

Figure 3.9 contains a plot of the cathode-to-anode voltage and the current flowing through the MCT for a different load level than used for Figures 3.6-3.8. V_{BUS} for this test was 75 V and the load resistance was 15 Ω; the switching frequency was approximately 25 kHz. Note that the device turns off with about 15 A flowing through it. A voltage spike of about 50 V is generated at turn off.

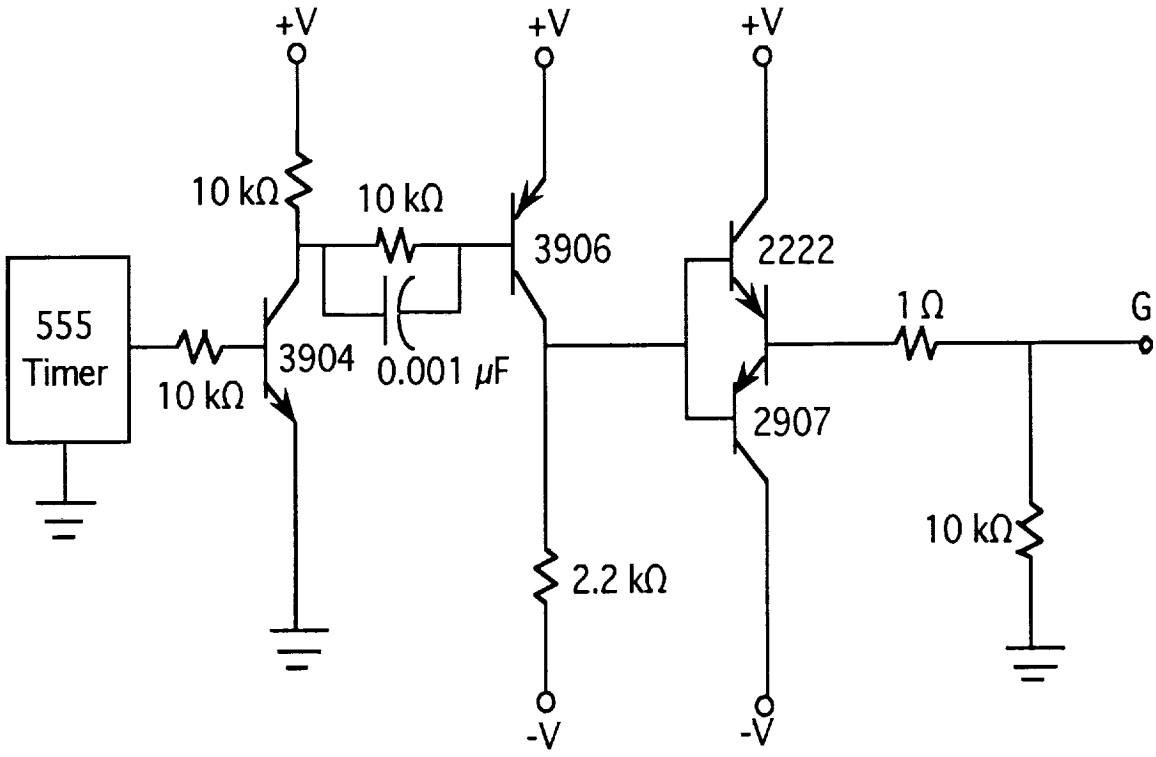


Figure 3.5. MCT gate drive circuit.

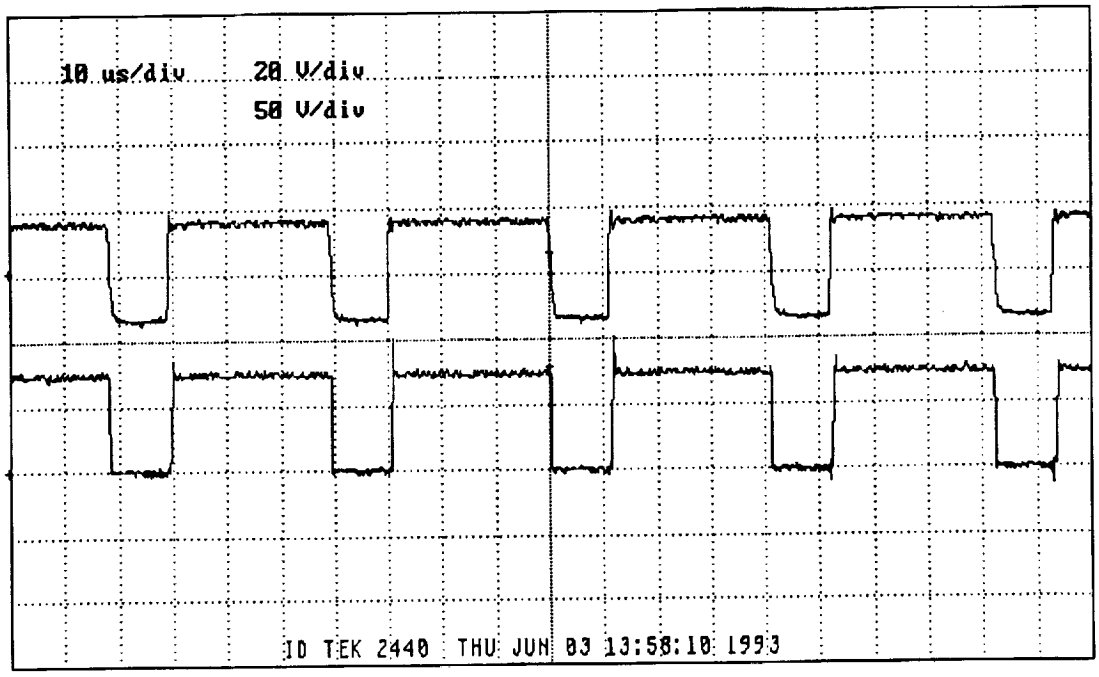


Figure 3.6. MCT inductive switching waveforms
Top trace: Gate-to-anode voltage
Bottom trace: Anode-to-cathode voltage

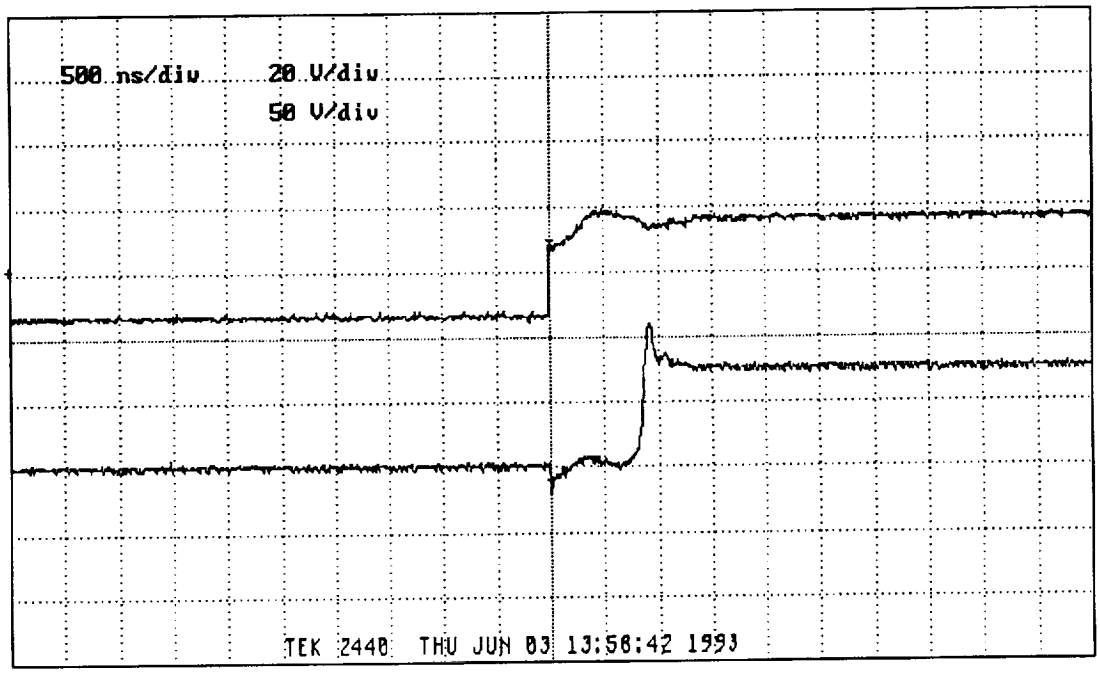


Figure 3.7. MCT inductive switching waveforms at turn off.
Top trace: Gate-to-anode voltage
Bottom trace: Anode-to-cathode voltage

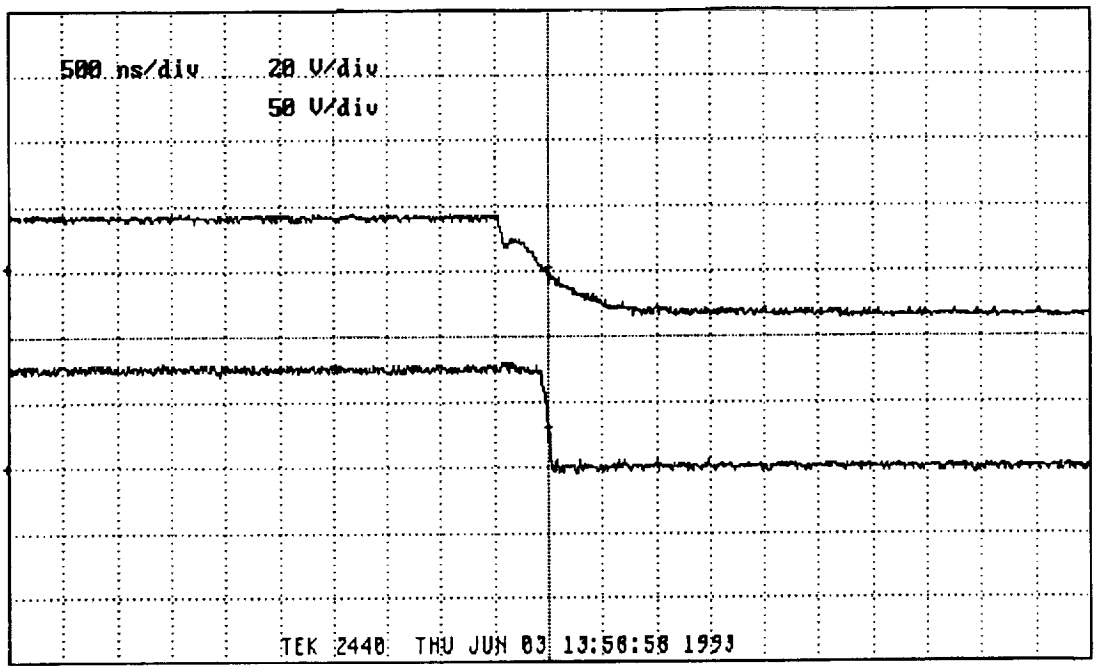


Figure 3.8. MCT inductive switching waveforms at turn on.
Top trace: Gate-to-anode voltage
Bottom trace: Anode-to-cathode voltage

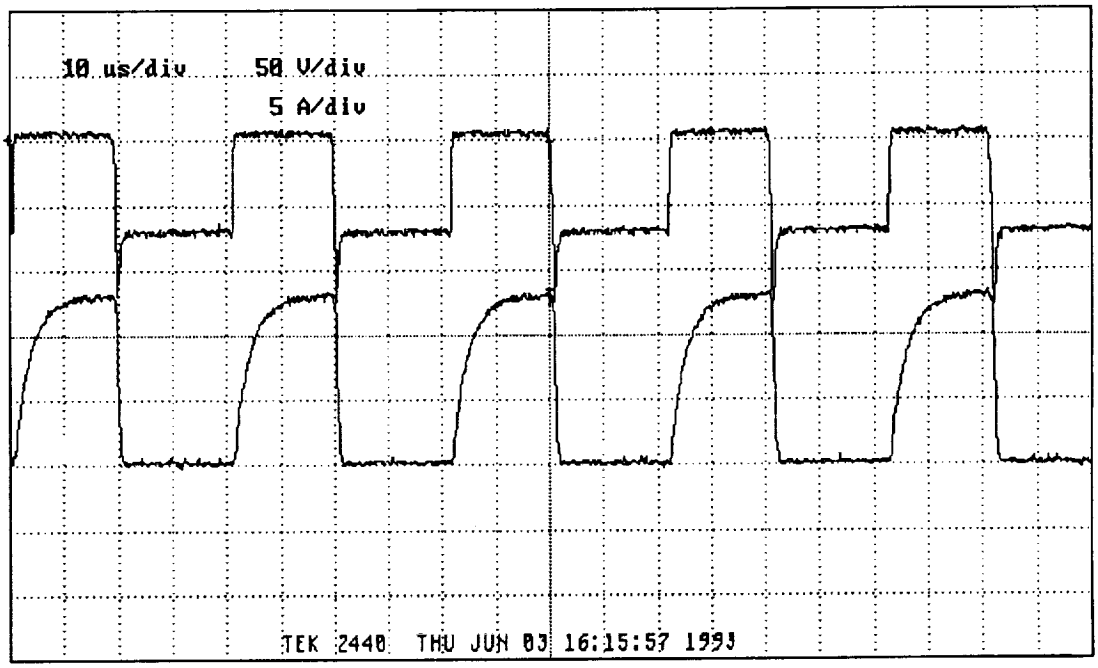


Figure 3.9. MCT inductive switching waveforms.
Top trace: Cathode-to-anode voltage
Bottom trace: Device current

Chapter 4

EXPERIMENTAL SETUP

This section of the report discusses the experimental setup of the project. First a resonant dc link inverter was built. This inverter was then used to drive a brushless dc motor in an open loop system. A control loop was then added to the system implementing pulse-density modulation (PDM) to control the speed of the motor.

The Resonant DC Link Inverter

The purpose of the resonant dc link is to provide an input voltage that periodically resonates to zero volts for the three-phase inverter bridge. The circuit diagram of the resonant dc link is shown in Figure 4.1 with the control electronics in block diagram form. The primary components of the resonant dc link are a dc voltage bus, an inductor, a capacitor, and a shunt switch. The dc bus is produced by rectifying a three-phase source and using a large filter capacitor to hold the voltage as constant as possible. Two 1 μF, oil-filled GE capacitors were connected in series to produce a resonant capacitance of 0.5 μF. A 45.5 μH, 0.29 Ω air-core inductor was used as the resonant inductor. The shunt switch S is an IRGPC40U 600V/40A IGBT with a 1N3913 diode in anti-parallel. Switch S7 is an IRF250 MOSFET that is used to initialize the start-up of the resonant dc link.

As mentioned in chapter 2, the resonant link provides an oscillatory input for the inverter to allow for zero voltage switching. The circuit in Figure 4.1 accomplishes this task in the following manner. When the manual switch ST is turned on, the output Q of the latch goes from low to high (0V to +15V) to turn the switch S7 on. Simultaneously, the output Q' of the latch goes from high to low (+15V to 0V). This signal is differentiated to give the 555 timer the proper trigger signal. When triggered, the 555 timer turns the shunt switch S on for a set amount of time. With switch S on, the capacitor is shorted and the current in the inductor increases linearly. When switch S is turned off, the voltage across

the capacitor rings up to about $2V_s$ and back to zero. This voltage is sensed by the voltage dividing resistors and fed back to the zero-voltage detector. When the input to the zero-voltage detector reaches zero volts the output goes from high to low (+15V to 0V). This signal is differentiated and sent to the 555 timer to turn switch S on and the process repeats.

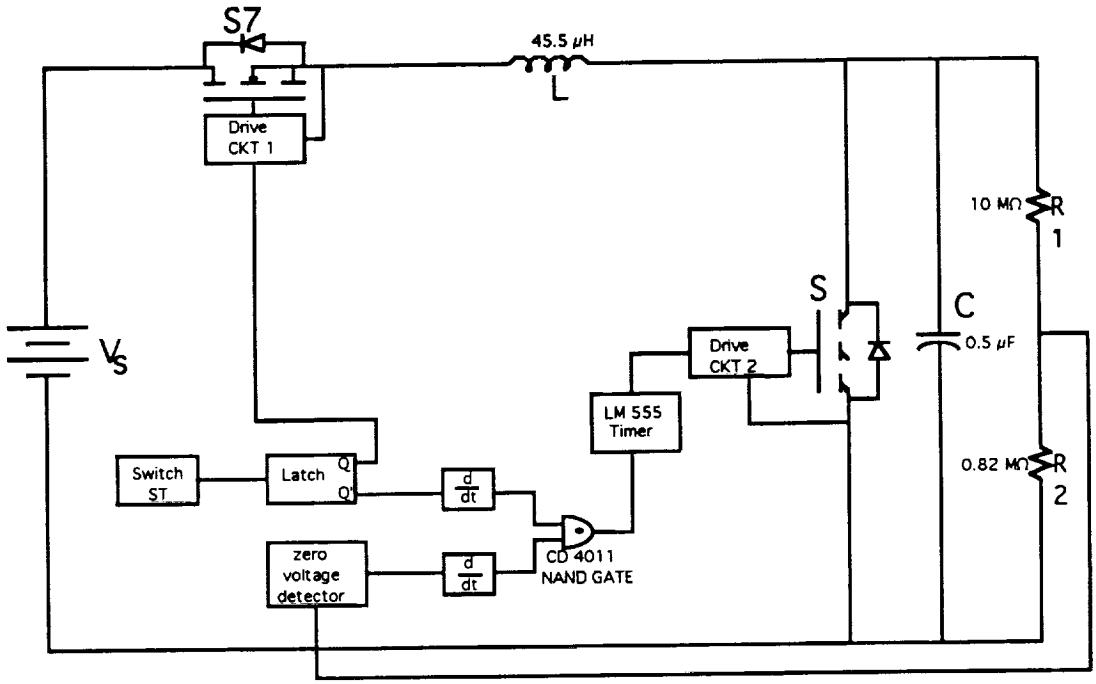


Figure 4.1 Circuit diagram of the Resonant DC Link.

Figure 4.2 shows the circuit diagram of the resonant dc link with the electronic components pictured in detail. An LM555 timer, connected in the monostable mode, was used to control the switching of the shunt switch S. In the monostable mode, the LM555 timer requires a trigger signal that goes from Vcc to less than 1/3 Vcc in a time span less than that of the on time of the output signal. In this circuit, the LM555 timer is triggered by the Q' output of the latch on start-up and by the output of the zero-voltage detector thereafter. These signals are not fast enough to trigger the LM555 timer properly; therefore, the differentiators are needed to process these signals to the proper form for the LM555 timer. The zero-voltage detector was constructed using an LM311 operational amplifier comparator. The output of the zero-voltage detector is Vcc when its input is greater than

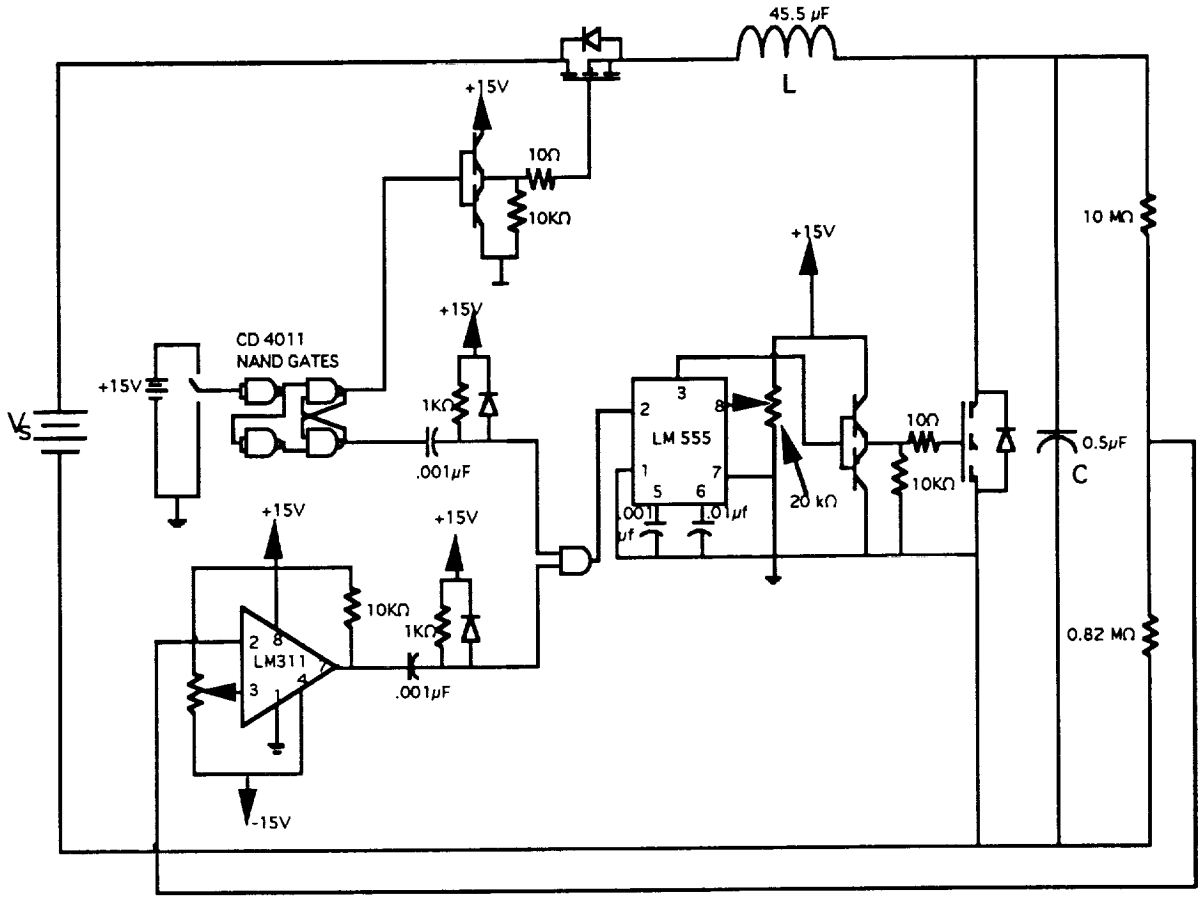


Figure 4.2 Circuit diagram of the resonant dc link with electronic components.

zero and 0 when its input is less than zero, thus triggering the LM555 timer when the resonant dc link reaches zero volts.

The drive circuit used for both the MOSFET and the IGBT shunt switch is seen in Figure 4.3. The drive circuit consists of a complementary pair of bipolar transistors (PNP=2N2907 and NPN=2N2222), that creates a current amplifier to drive the power switch. A 10 Ω 1/4 watt resistor is placed in series with the gate of the power switch to limit the rise of the gate to source signal. A 10 kΩ 1/4 watt resistor is connected from the drive output to ground to provide a current discharge path.

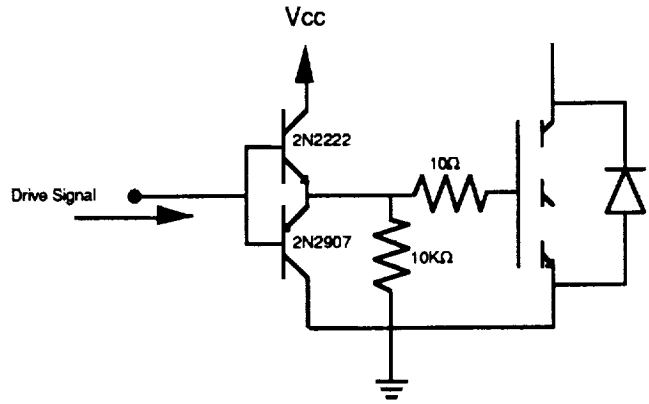


Figure 4.3 Drive circuit for the resonant switch S and the synchronizing switch S7.

The Inverter Bridge

One of the main objectives of this project was to study the performance of MOS-controlled thyristors (MCT's) in 3-phase inverter operation. MCT's were found to be much more expensive and more difficult to obtain than IGBT's. Because of this, two inverter bridges were constructed; one with IRGPC40U 600V/40A IGBT's and 1N3913 diodes in anti-parrallel and another with MCTA75P60 600V/75A MCT's and MUR 3040PT diodes in anti-parrallel. The complete system was first designed and constructed using the IGBT inverter bridge. When this system was completed successfully, the MCT inverter bridge was then added to study the system operation using the MCT inverter bridge. Figure 4.4 shows the circuit diagram of the inverter bridge with IGBT's as the power semiconductor devices.

For the circuit configuration of that seen in Figure 4.4, special design considerations are required for the drive circuits for the power switching devices. The drive circuit for one leg of the IGBT inverter is shown in Figure 4.5. The IGBT's used are N-channel devices which require a positive gate-to-emitter signal to turn the switch on. The emitters of the bottom switches S4, S5, and S6 are connected to ground in the circuit, so the drive circuit for these switches is straightforward. However, the emitters of the top switches S1, S2, and S3 are not at the same potential. For the bottom switches, drive

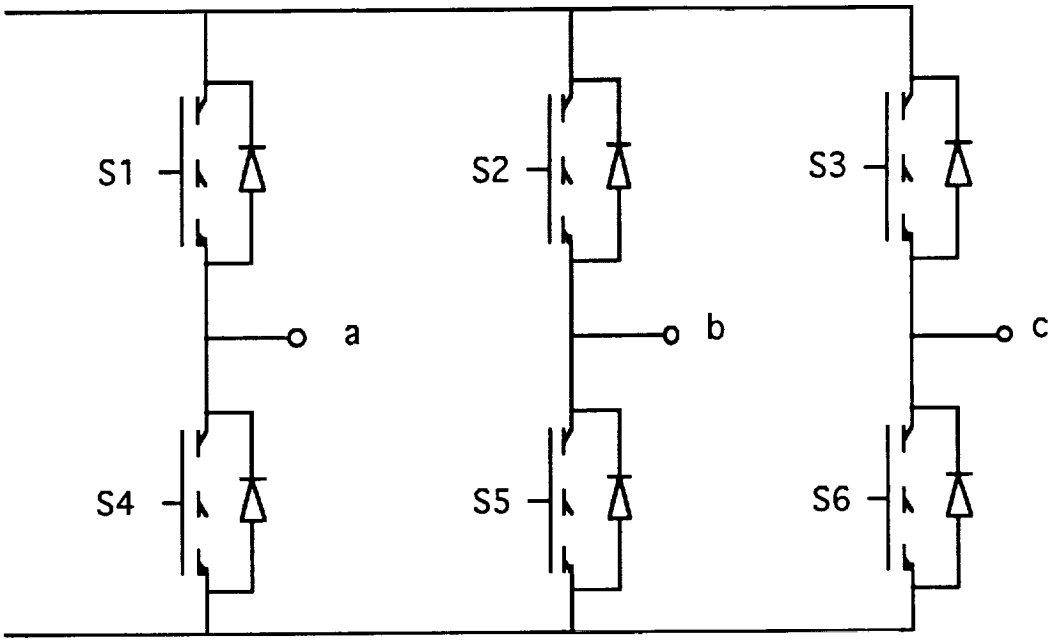


Figure 4.4. Circuit diagram of the inverter bridge with IGBT's.

circuits similar to that seen in Figure 4.3 with the addition of an optocoupler are used. Bootstrap drive circuits are needed for the top switches to solve the problem of the floating emitters. The bootstrap capacitor charges up to the voltage of the emitter of that particular switch plus 15V. When the control signal is sent to the drive circuit of one of the top switches, the gate-to-emitter signal will always be 15V. HP2211 optocouplers are used in the drive circuits to isolate the control circuitry from the high power elctronics.

The MCT's are P-channel devices which requires a -15V gate-to-cathode signal to turn them on and a +15V signal to turn them off. For the MCT's the cathodes of the top three switches share a common point in the circuit while the cathodes for the bottom three switches do not. A bootstrap circuit that would provide the positive and negative voltage needed to drive the MCT would be very complicated so isolated power supplies were used here. The drive circuit used for the MCT is seen in Figure 4.6.

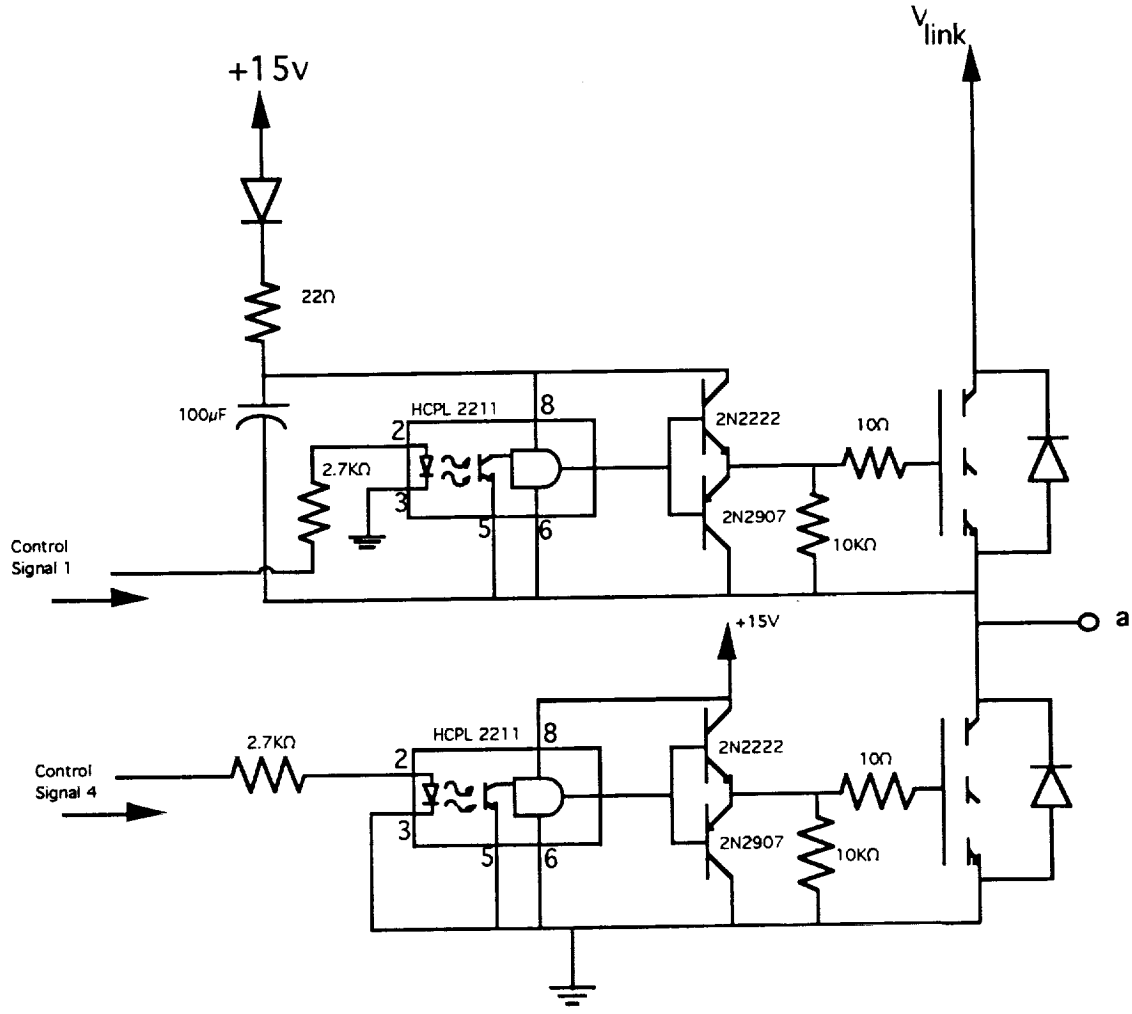


Figure 4.5. Drive circuit for one leg of the IGBT inverter.

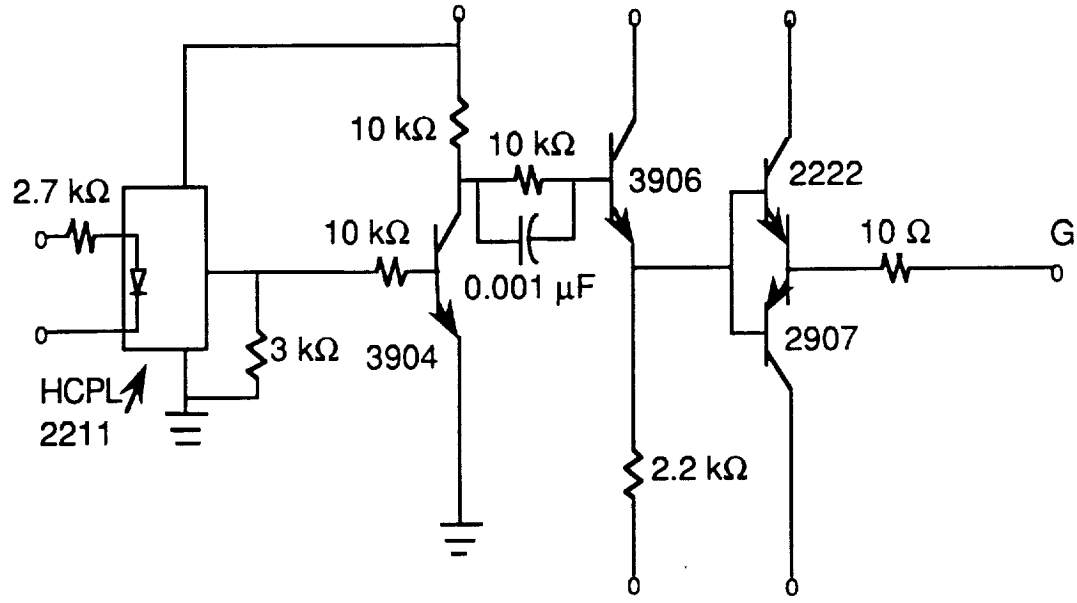


Figure 4.6. The drive circuit for the MCT.

Brushless DC Motor

A Reliance 5 Hp, 4000 RPM, 30A, 290V brushless dc motor was used in this experimental system. First, an open loop system was constructed where the resonant dc link inverter provided the input voltage to stator of the brushless dc motor. Figure 4.7 shows the open loop system for the resonant dc inverter driven brushless dc motor.

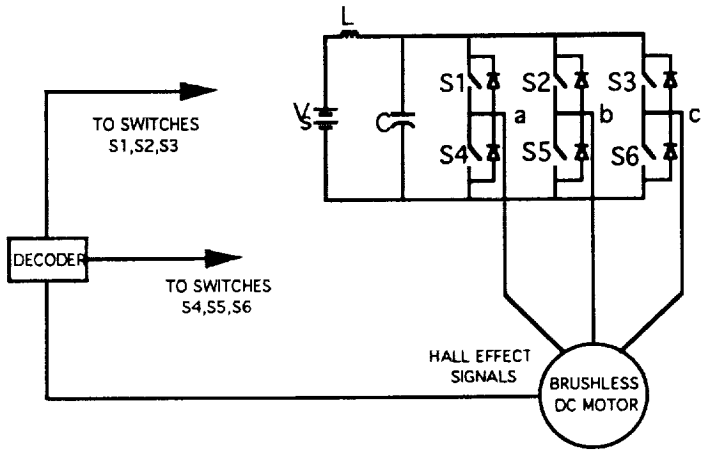


Figure 4.7. Open loop resonant dc link inverter driven brushless dc motor system.

A brushless dc motor has a stator similar to that of a three-phase induction motor and the rotor contains permanent magnets. The rotor also contains hall effect sensors that feed back signals to the control sytem. These signals are decoded to control the inverter to provide the proper phase sequence for the input stator voltage. Figure 4.8 shows the hall effect signals and the corresponding phase currents for this brushless dc motor.

The decoded hall effect signals provide the control signals for the inverter switches. Figure 4.9 shows the hall effect signals with the corresponding inverter switching signal. It can be noticed from Figure 4.9 that at any time only two of the inverter switches are conducting. Figure 4.10 shows the applied stator voltage when the corresponding pair of inverter switches are conducting.

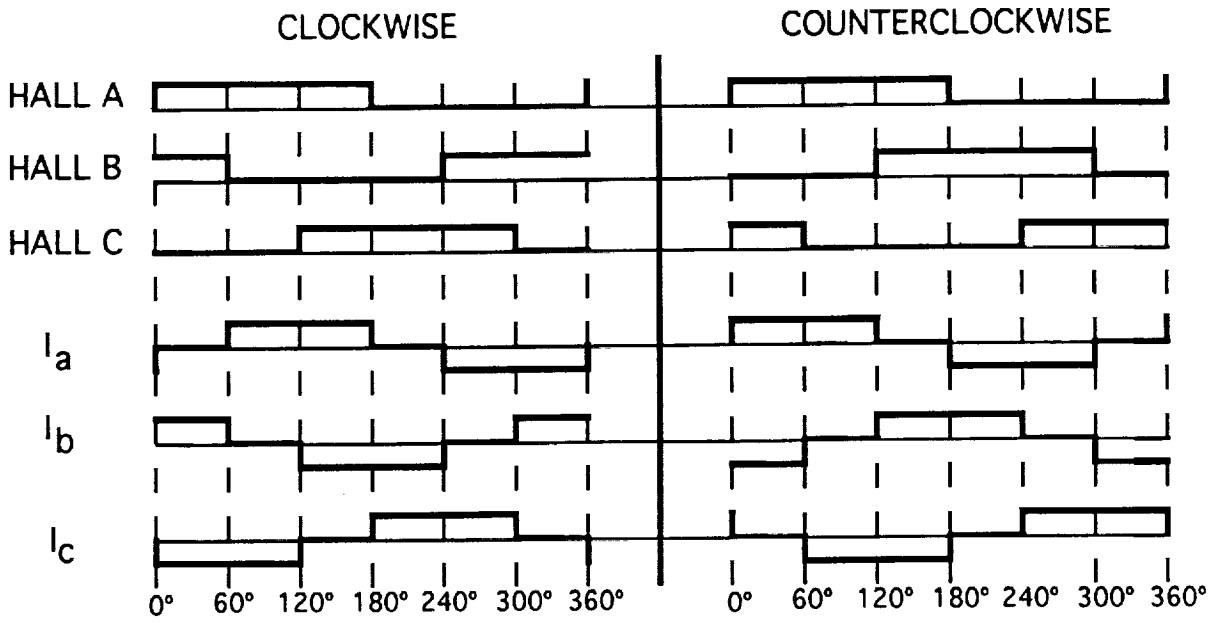


Figure 4.8. Brushless dc motor hall effect signals with corresponding phase currents.

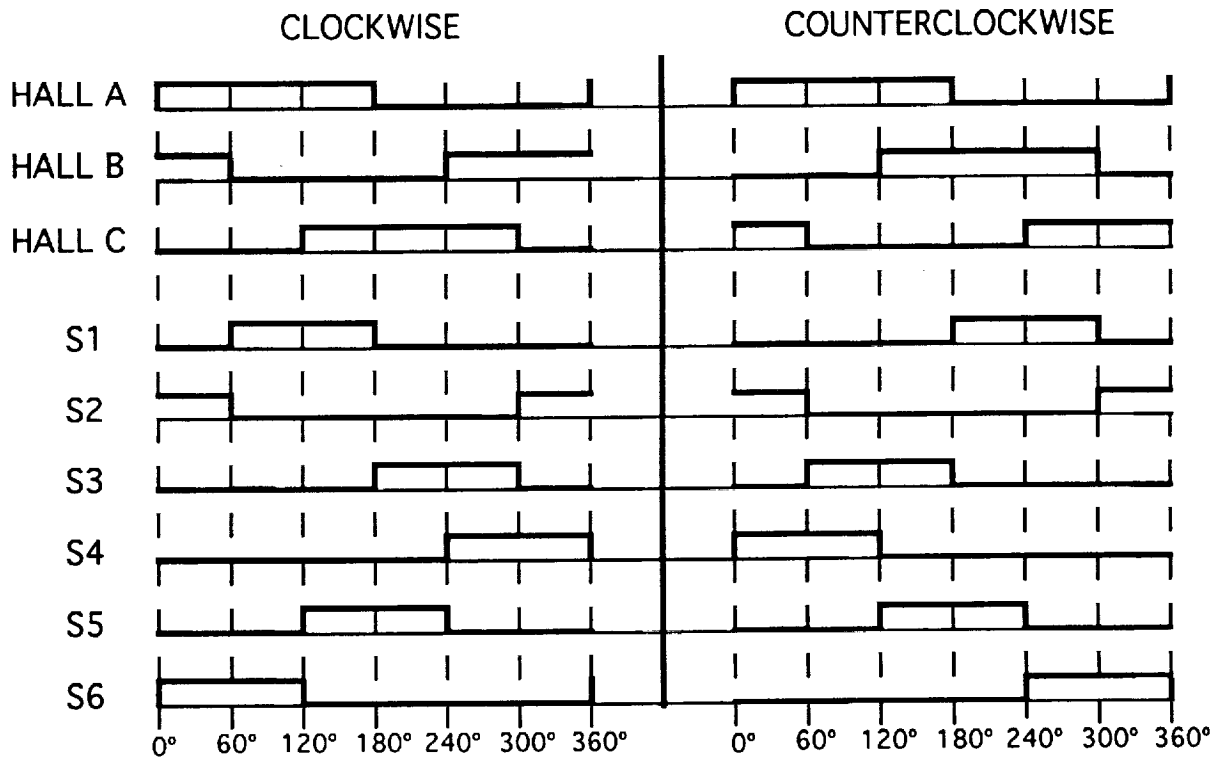


Figure 4.9. Brushless dc motor hall effect signals with corresponding switching signals.

SWITCHES CONDUCTING	PHASE VOLTAGE
S1 & S5	+ Vab
S1 & S6	- Vca
S2 & S4	- Vab
S2 & S6	+ Vbc
S3 & S4	+ Vca
S3 & S5	- Vbc

Figure 4.10. Stator voltage applied when pairs of switches are conducting.

The hall effect signals were decoded using a CD4028 BCD chip and logic gates. The brushless dc motor hall effect signal decoder is shown in Figure 4.11. The hall effect signals are first run through a D flip-flop whose clock signal is the drive signal for the shunt switch of the resonant dc link. This ensures that all switching takes place at zero volts. In other words, when the hall effect signals change states, the control circuitry waits until the next zero voltage crossing before any switching is performed.

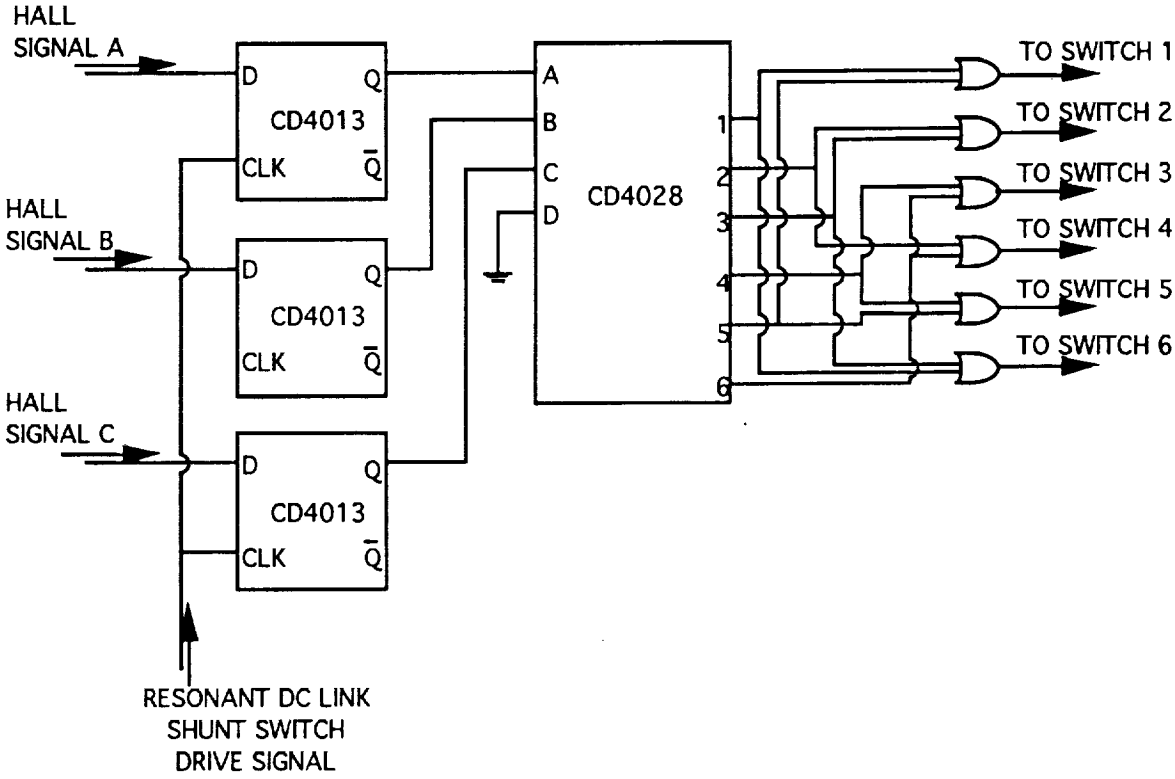


Figure 4.11. Hall effect signal decoder for the brushless dc motor.

Speed Control Loop Using Pulse-density Modulation

The speed of the brushless dc motor is dependent on the applied input stator voltage. Speed control of the brushless dc motor was accomplished with the implementation of pulse-density modulation (PDM). PDM produces the switching signals for the power semiconductor devices of the three-phase inverter bridge to control the stator voltage of the brushless dc motor, thus controlling the speed of the motor. The block diagram of the PDM control system for the brushless dc motor is shown in Figure 4.12. This system is simply the open loop system as seen in Figure 4.7 with the addition of three current loops and one speed loop that performs the PDM to control the speed of the motor.

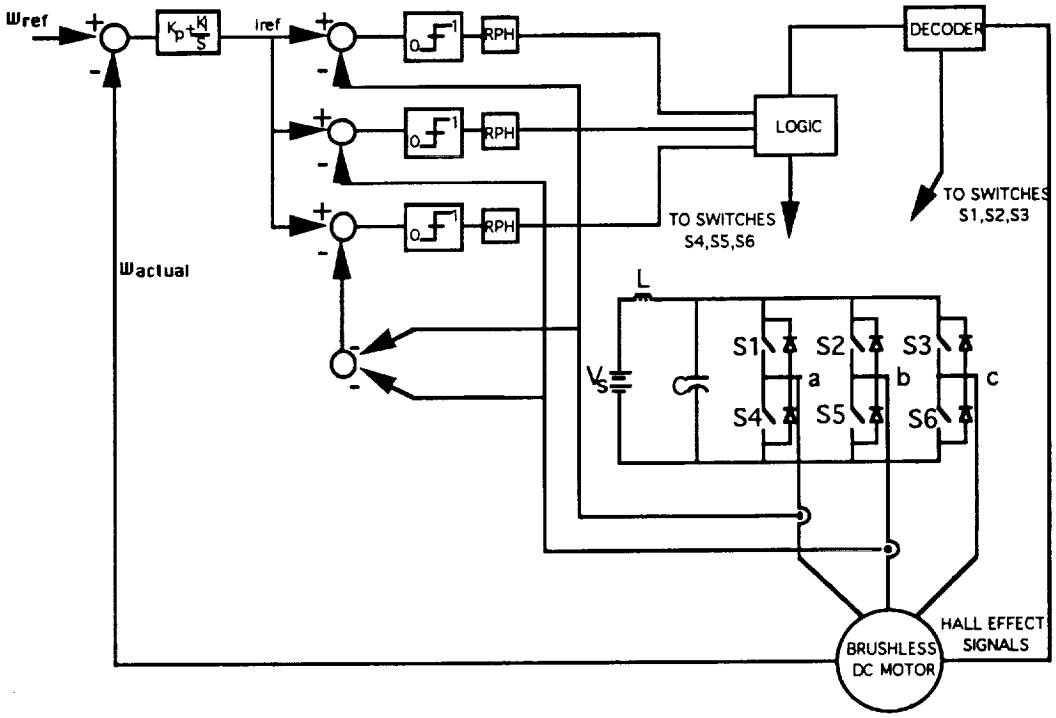


Figure 4.12. PDM control system for a brushless dc motor.

Pulse-density modulation controls the input stator voltage of the brushless dc motor by controlling the switching of the three-phase inverter bridge. From Figure 4.10, it can be seen for the open loop system that at any time only two inverter switches are conducting. PDM is implemented to further control the inverter switching to not only control which

phase voltage is applied but also the amount of voltage applied to the stator of the brushless dc motor. To illustrate, consider when switch S1 and S5 are conducting and a positive V_{ab} is applied to the stator of the motor. If during this 1/6th of the cycle, switch S5 is turned off, the applied voltage V_{ab} would be zero. Likewise, if during the period when switches S1 and S6 are conducting, switch S6 is turned off, the voltage applied would be zero. Similarly, for all switching combinations seen in Figure 4.10, the voltage applied can be controlled by switching the corresponding bottom switch, switch S4, S5, or S6, on or off. Thus, by "toggling" the proper bottom switch of the inverter the speed of the brushless dc motor can be controlled.

The control system seen in Figure 4.12 compares the actual speed of the motor to a speed reference to produce an error signal. This error signal is applied to a PI controller to create a current reference. This current reference is compared to each of the three phase currents and the difference is a current error signal for each phase. If the current error signal is above zero, the digitizer outputs a logical one, and if the current error signal is below zero the digitizer outputs a logical zero. The resonant pulse hold (RPH) is simply a D flip-flop that is clocked by the drive signal of the shunt switch to ensure zero voltage switching. The RPH output and the open loop drive signals for the bottom switches are combined with logic gates to produce the PDM drive signals for the inverter switches S4, S5, and S6. This produces the "toggling" effect for the bottom switches as mentioned above. Switches S1, S2, and S3 are driven directly by the decoded hall effect signals from the brushless dc motor.

Figure 4.13 is the circuit diagram for the summing op-amp and the PI controller of the PDM controller. A 500 kΩ potentiometer connected between +15V and ground creates the speed reference voltage ω_{ref}. The summing op-amp was constructed using an LF351 operational amplifier. The summer takes the difference of the speed reference, ω_{ref}, and the actual speed fed back from the motor's tachometer. The PI controller was also constructed with LF351 operational amplifiers. The PI controller consists of an LF351

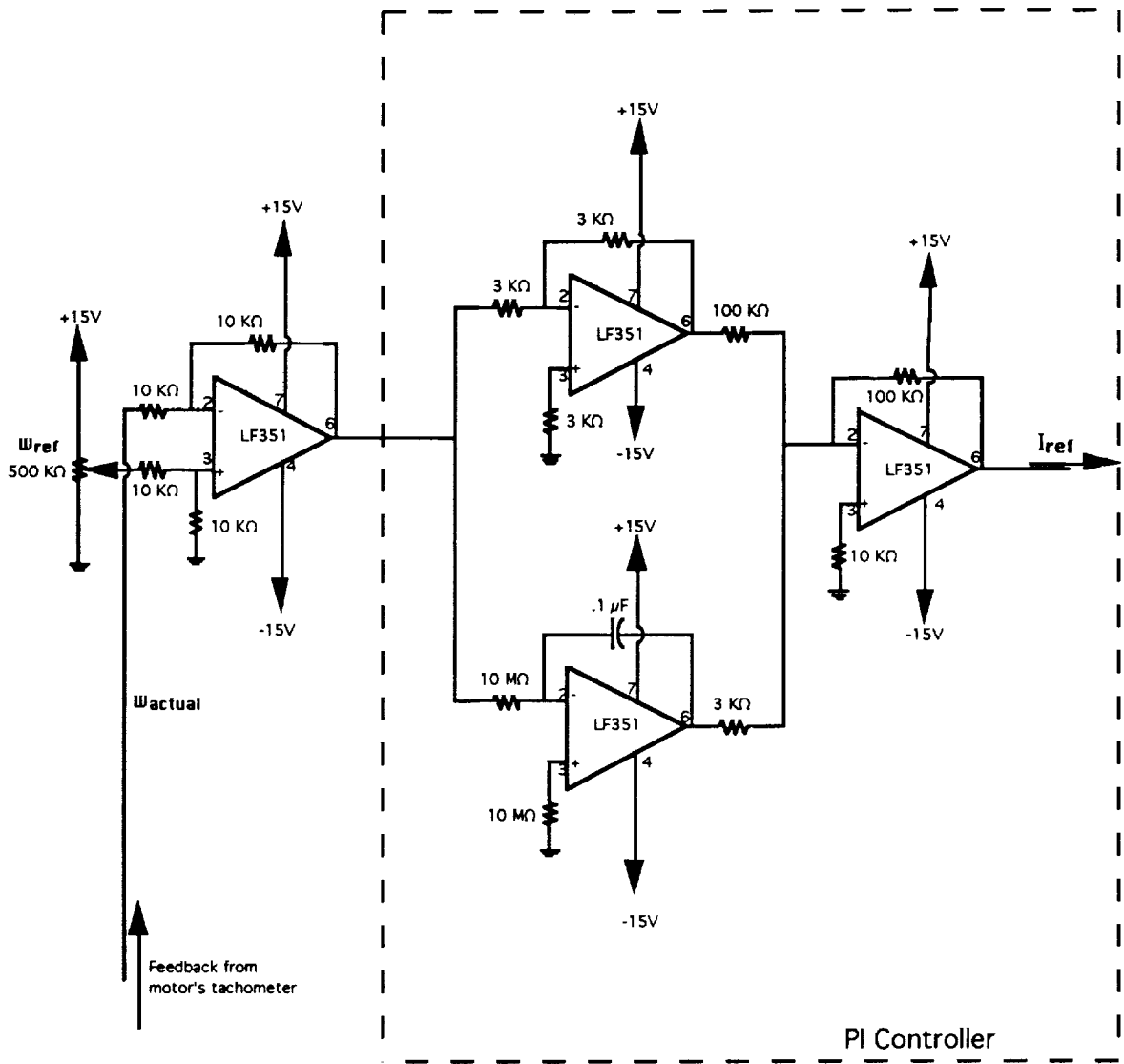


Figure 4.13. Circuit diagram of the summer and PI Controller for the PDM control system.

op-amp connected as an integrator in parallel with an LF351 op-amp connected as a constant gain. Since both the integrator and gain are connected with an inverted output, a third op-amp is needed to invert the combination of these two signals. The output of this op-amp is the current reference I_{ref}, which feeds into the individual phase current loops of the control system as seen in Figure 4.14.

The three summing op-amps for the phase current control loops seen in Figure 4.14 were also constructed using LF351 op-amps. These summers take the difference of the

current reference, I_{ref}, and the actual current. Micro Switch CSLA1CD linear current sensors were used to measure the actual current for each phase. Since this is a balanced three-phase system, the actual current for phase c can be calculated from the phase a and b currents. However, we used current sensors for each phase for simplicity. The difference of these signals creates the inputs for the digitizers. The digitizers were constructed using LM311 operational amplifier comparators. These are connected to give an output of 15V when the input from the summers are above 0 V and an output of 0 V when the input is below 0 V. The resonant pulse hold (RPH) was accomplished using a D flip-flop. The clock input to the D flip-flop is the drive signal to the resonant link shunt switch. This ensures that the output will change states only at a zero voltage crossing, thus creating zero-voltage switching. The output of the three RPH circuits creates the Phase A, B, and C PDM signals.

Figure 4.15 shows how the brushless dc motor hall effect signal decoder seen in Figure 4.11 is modified to accompany the PDM control loop system. The A, B, and C phase PDM signals are combined with the outputs of the hall effect decoder to create the PDM drive signals for the inverter signals.

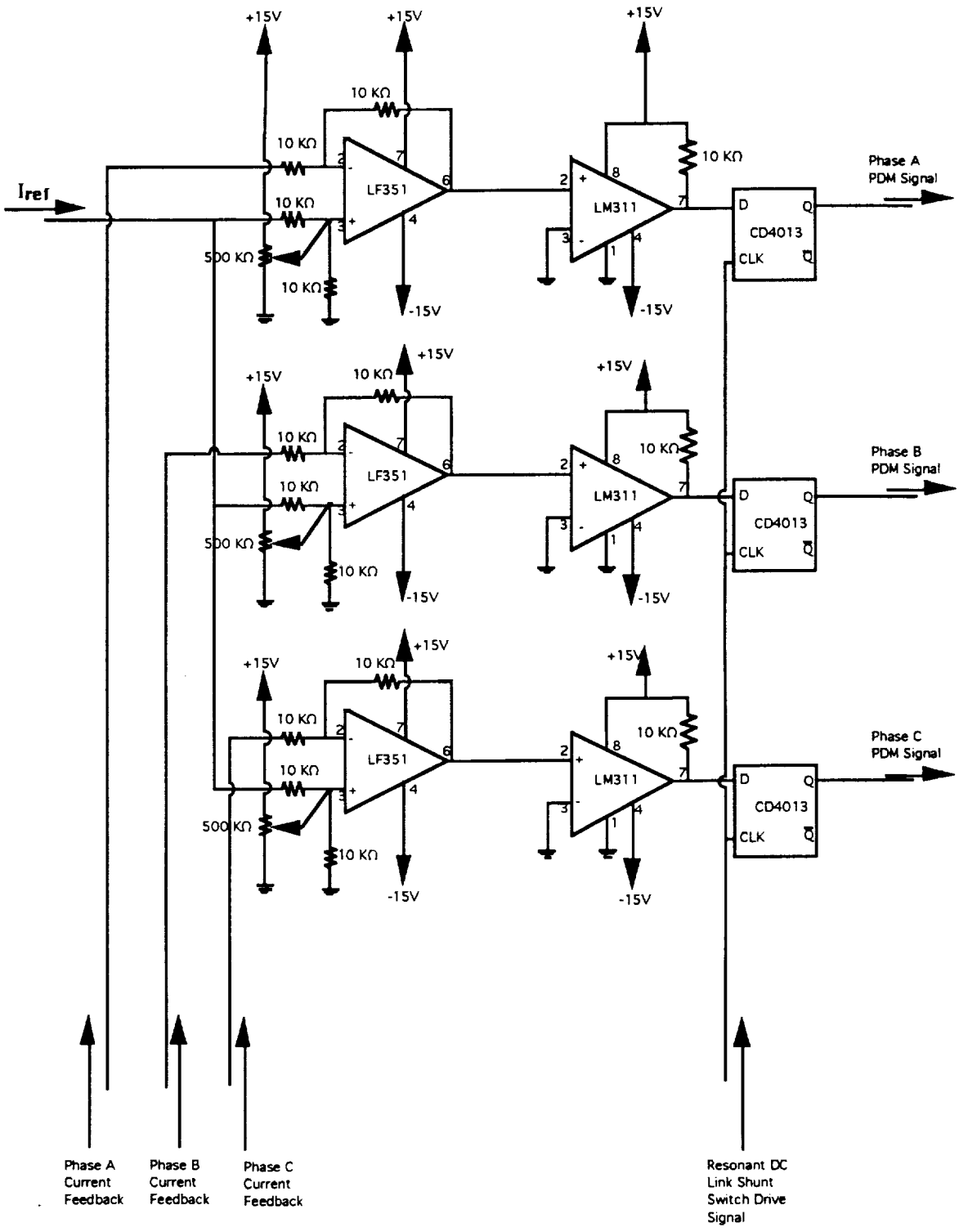


Figure 4.14. Circuit diagram of the current loops of the PDM control system.

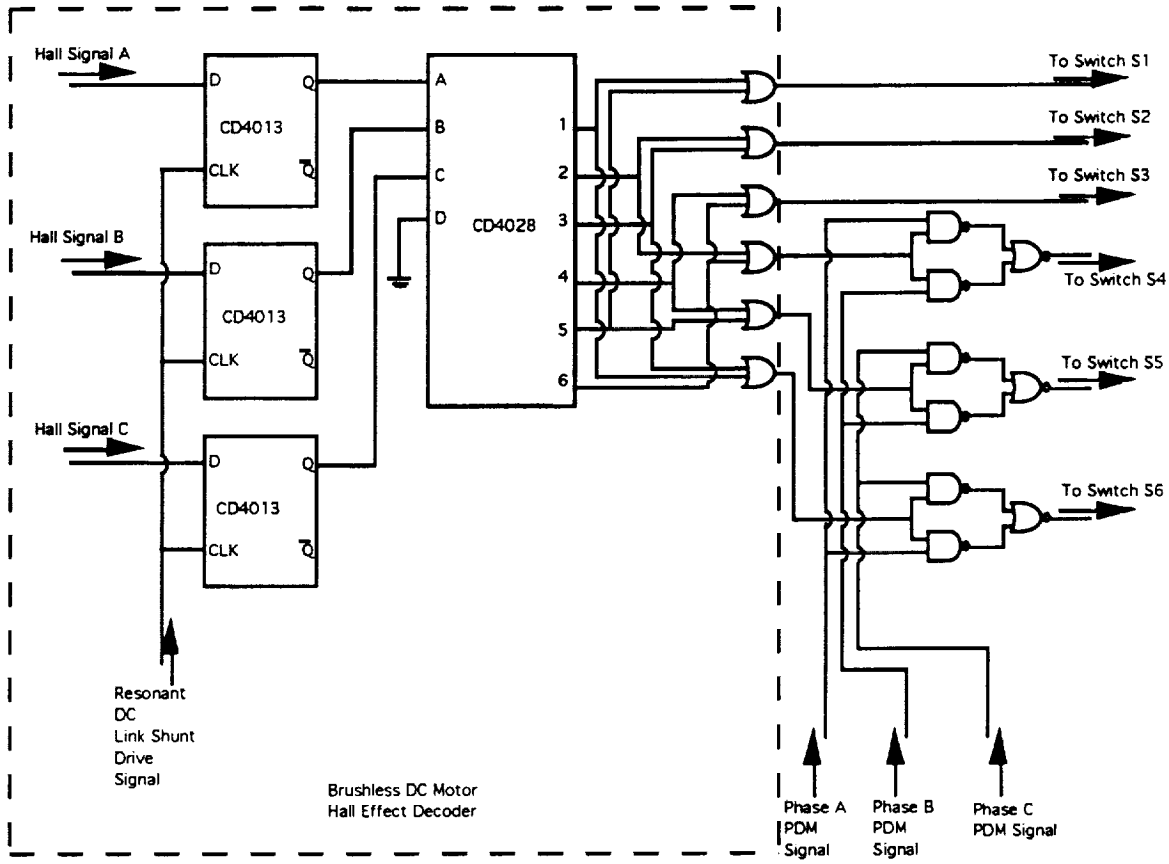


Figure 4.15. Circuit diagram of the brushless dc motor hall effect decoder and the PDM signals, which create the drive signals for the inverter switches.

Chapter 5

EXPERIMENTAL RESULTS

This chapter presents experimental results for the pulse-density modulated brushless dc motor speed regulated system. The results are presented in the form of oscilloscope traces. The output of the resonant link is first shown. The results of the brushless dc motor running in both open-loop operation and closed-loop PDM operation are also presented. Inverter power switch drive signals are shown to illustrate the PDM operation that is discussed in Chapter 4.

Figure 5.1 shows an oscilloscope plot of the output of the resonant dc link with the input dc voltage, V_s, at 100 Volts. The peak link voltage is about 220 Volts, which is as expected, a little above $2V_s$. The resonant frequency, which is determined by the values of the resonant inductor and the resonant capacitor, is 30 kHz with the 45.5μH inductor and the 0.5 μ F capacitor.

It can be seen in Figure 5.1 that the link voltage periodically resonates to zero volts and remains at zero for a period of time sufficient enough to allow all switching to be performed, thus creating zero-voltage switching.

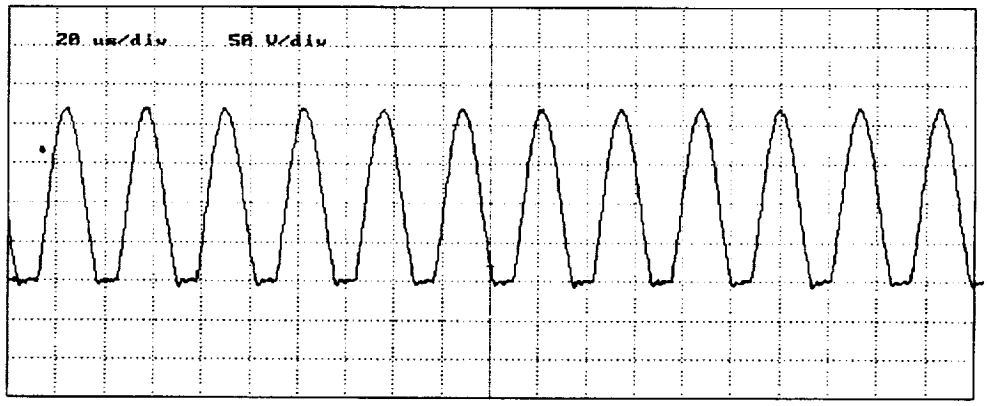


Figure 5.1. Resonant DC Link voltage waveform.

Figure 5.2 shows the hall effect signals, HA, HB, and HC from the brushless dc motor and their corresponding phase currents, IA, IB, and IC. The frequency of the hall effect signals and the phase currents are the same and are proportional to the speed of the motor. These hall effect signals are decoded to produce the switching signals for the inverter switches.

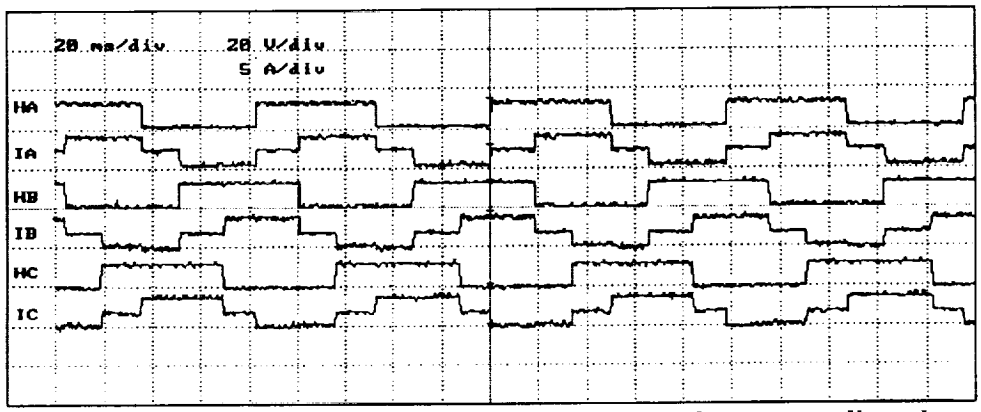


Figure 5.2. Brushless dc motor hall effect signals and corresponding phase currents.

Figure 5.3 is an oscilloscope plot of one of the hall effect signals and its corresponding phase current under no load conditions. The commutation of the inverter switches can be noticed by the dips in the current waveforms half way through the maximum and minimum points of the waveform. This is a typical brushless dc motor current waveform for the open loop system.

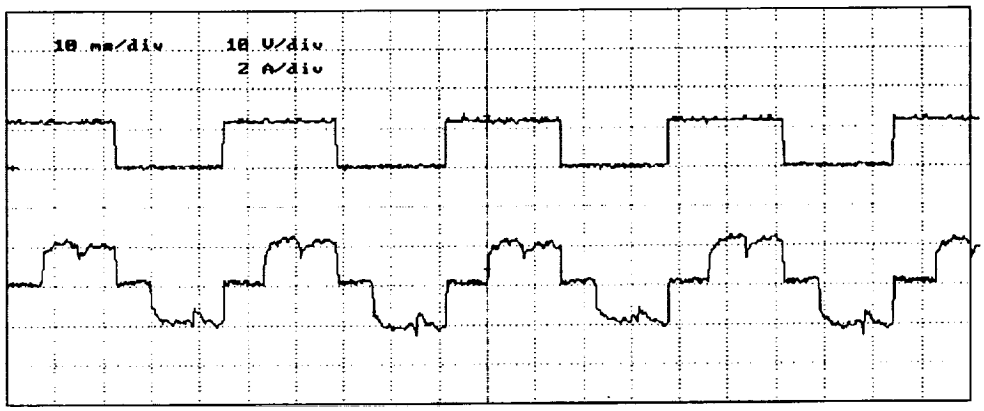


Figure 5.3. One phase of the brushless dc motor hall effect signals and its corresponding phase current.

Figure 5.4 shows a current waveform of the open-loop system under loaded conditions with the IGBT inverter bridge. As you can see, the peak current is near 15 amps which is significantly larger than the no load current of 2 amperes seen in Figure 5.3

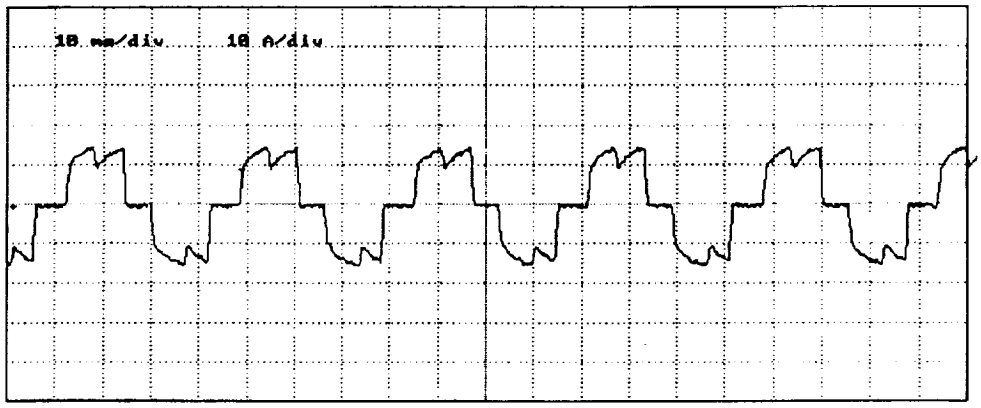


Figure 5.4. Oscilloscope plot of the phase current under loaded conditions with the IGBT inverter.

Figure 5.5 shows the current waveform of the loaded brushless dc motor system with the MCT inverter bridge. No difference in motor performance was noticed between the IGBT inverter and the MCT inverter.

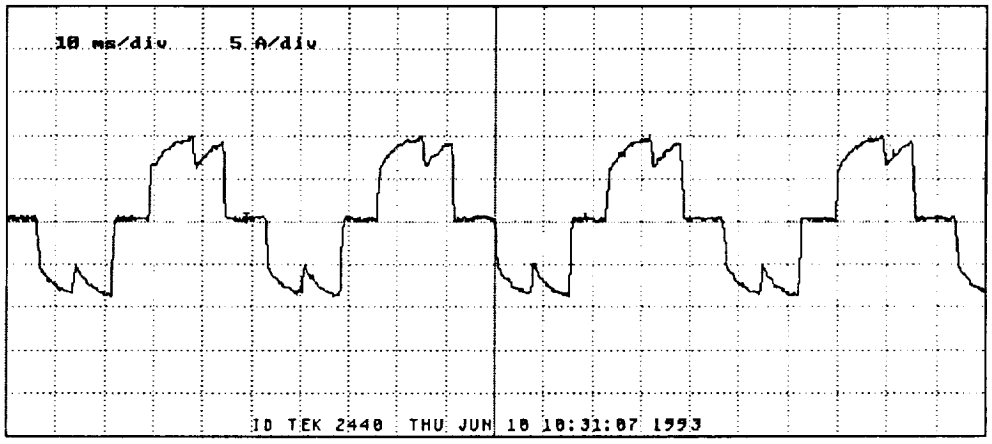


Figure 5.5. Oscilloscope plot of the phase current under loaded conditions with the MCT inverter.

Figure 5.6 depicts a comparison of inverter switching signals. The top waveform is a switching signal for an inverter switch under open-loop conditions, or with no current regulation. The bottom waveform shows the switching signal for a bottom inverter switch under PDM operation. The PDM current loop seen in Figure 4.14 creates signals that turn each bottom switch off when the current reference is exceeded and allows the switch to be turned on when the current falls below the reference. It can be noticed that this switch is turned on and off quickly creating the "toggling' effect as mentioned previously that controls the inverter output voltage.

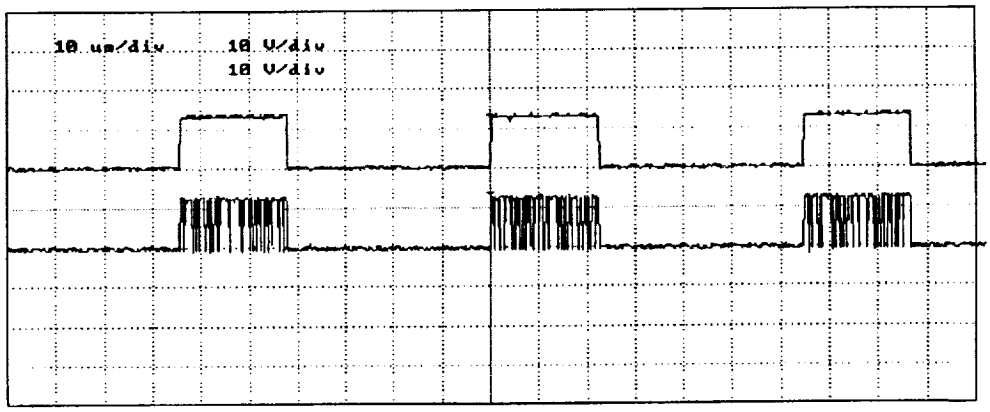


Figure 5.6. Inverter drive signals: (top: open loop operation; bottom: PDM operation)

Figure 5.7 shows a brushless dc motor phase current during PDM operation. The control system contains a current regulator loop to produce the PDM which flattens the current waveform as seen in this figure.

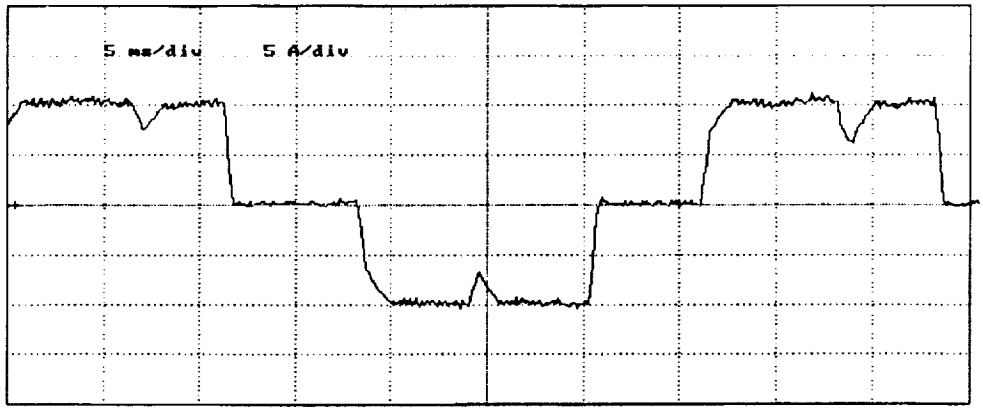


Figure 5.7. PDM regulated current of the brushless dc motor.

As mentioned above, the speed of the brushless dc motor is proportional to the frequency of the hall effect signals. Figures 5.8, 5.9, and 5.10 demonstrate the speed regulation of the system when the mechanical load is increased. It can be noticed that for the following waveforms the current level increases, showing the increase in load, while the frequency remains constant, showing constant speed, thus speed regulation is maintained.

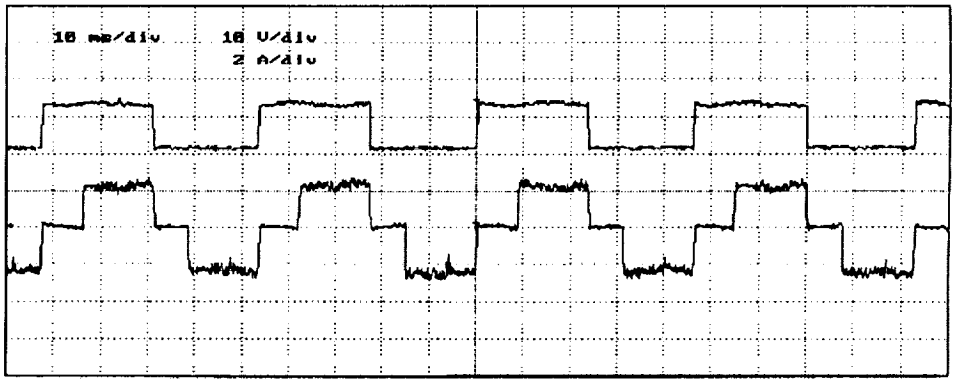


Figure 5.8. Brushless dc motor hall effect signal and current of 2 amperes.

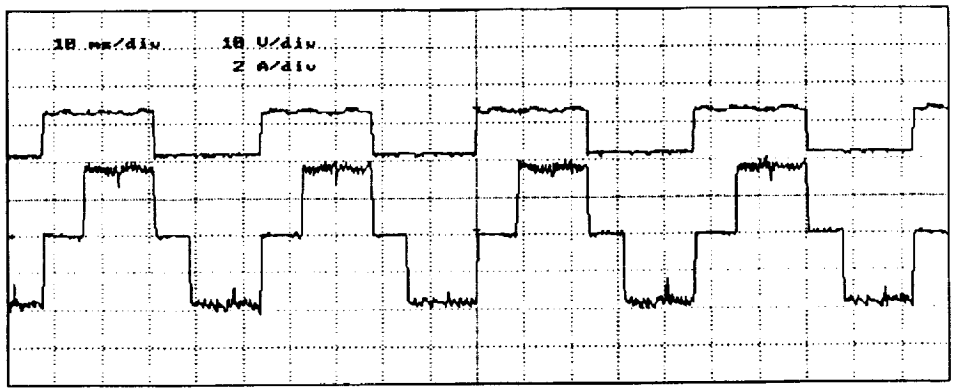


Figure 5.9. Brushless dc motor hall effect signal and current of 4 amperes.

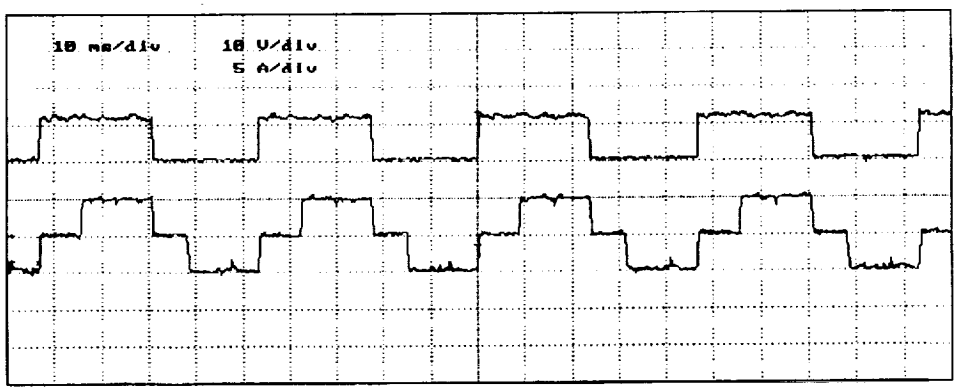


Figure 5.10. Brushless dc motor hall effect signal and current of 5 amperes.

Chapter 6

SUMMARY AND SUGGESTIONS FOR FUTURE WORK

The objectives of this research project were to develop and validate an analytical model of the MCT device when used in high power motor control applications and to investigate the use of MCTs and pulse-density modulation concepts in the control of brushless dc motors. The unavailability of MCTs prevented satisfactory completion of the first objective. The researchers made many calls to Harris representatives to obtain MCTs. It was not until the end of this project that the researchers were able to obtain any MCTs from Harris through an electronics distributor at a cost of $46.50 each with a minimum order of 30 pieces. A total of sixteen devices were used in this investigation: eight were obtained from NASA/MSFC and another eight were found at Auburn University as surplus parts from another project related to high temperature characterization of MCTs. Since a three-phase inverter requires six power devices, only a small number of devices were available for testing so that a device model could not be validated. As a result, the device model presented in this report was developed by Harris Semiconductor [8] and was not validated in the laboratory. The inductive switching tests performed with the MCTs were used to test the drive circuit which was designed for the MCTs and also briefly examine the "hard" switching characteristics of the MCT.

The second objective of this project was the design, fabrication, and testing of a three-phase inverter system which utilized pulse-density modulation concepts in the control of a brushless dc motor. This objective was successfully completed in the laboratory and the test results are included in this report. Two inverter systems were constructed in the laboratory: one used IGBTs and the other used MCTs. Because of the limited availability of MCTs, all of the development was done with IGBTs. The control system for the brushless dc motor has a speed loop for speed regulation and a current loop for current

regulation. Both of these quantities are regulated with pulse-density modulation. The experimental results included in this report demonstrate the applicability of pulse-density modulation concepts to the control of brushless dc motors. From a system viewpoint, the IGBTs and the MCTs performed the same. The system with the MCTs is more complex because of the requirements of two power supply voltages. One observation is that the MCTs do not seem to be as reliable as the IGBTs at this point in time.

Suggestions for Future Work

Even though this project has successfully demonstrated the use of the MCTs and pulse-density modulation to the control of brushless dc motors, several areas of future investigation still exist. The first of these is more MCT testing. Since it appears that MCTs are available at high prices and in small quantities, devices could be purchased so that thorough testing and evaluation could be performed to develop and validate some type of device model.

The current control system developed in the laboratory at Auburn University regulates the speed of the brushless dc motor. The electromechanical actuators for TVC and PCV applications are position servomechanisms. One area of investigation that should be pursued is the development of a position control system which uses pulse-density modulation concepts and brushless dc motors.

The spacecraft power system for the EMA system has very strict voltage requirements due to the corona effect. The nominal bus voltage of this system is 270 Vdc and cannot exceed 270-300 Vdc during assent into orbit. As discussed in chapter 2 and presented in chapter 5, the dc link voltage in the current PDM system reaches about twice the input voltage. As a result, a method for clamping the voltage at the desired level should be investigated. This may require the addition of some type of voltage clamp circuit to the current PDM system or the use of a different type of inverter topology.

The final two areas of investigation are the use of microprocessor technology in the control of the brushless dc motor and the application of advanced control algorithms to the position servomechanism. These might allow improved system performance and better integration into existing computer systems on the spacecraft.

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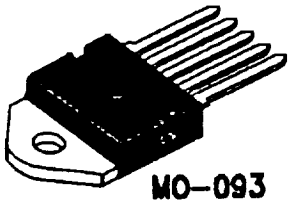
APPENDIX



MO-093

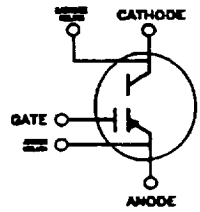
P-CHANNEL MOS CONTROLLED THYRISTOR (MCT)

75 Amp 600 Volt

Features:
- MOS Insulated Gate Input
- Gate Turn-Off Capability
- 1000 Amp Peak Current Capability
- 120 Amp turn-Off Capability
- Vtm=1.3 V @ I=75 A

The MCTA75P60 is an MOS Controlled SCR designed for switching currents on and off by negative and positive pulsed control of an insulated MOS gate. It is designed for use in motor controls, inverters, line switches and other power switching applications.

MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperatures of 150°C with active switching.



SYMBOL

Developmental type devices or materials are intended for engineering evaluation. The type designation and data are subject to change unless otherwise arranged. No obligations are assumed for notice of change or manufacture of these devices or materials.

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C)

Peak Off-State Voltage	V_{DRM}	-600	V
Peak Reverse Voltage	V_{RRM}	+10	V
Cathode Current Continuous@T_C=25°C	I_{C25}	120	A
@T_C=90°C.	I_{C90}	75	A
Nonrepetitive Peak Cathode Current	I_{TSM}	1000	A
Peak Controlable Current	I_{TC}	120	A
Gate-Anode Voltage Continuous	V_{GA}	±20	V
Rate of Change of Voltage (Vga = +15V)	dV/dT	10000	V/μS
Rate of Change of Current(Vga = -10V)	dI/dT	1000	A/μS
Power Dissipation Total @T_C=25°C	P_T	208	W
Power Dissipation Derating T_C>25°C		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C unless otherwise specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Peak Off-State Blocking Current	I_{DRM}	V_{AK} = -600V, V_{GA} = +15V	T_C = 150°C	---		3	mA
			T_C = 25°C	---		100	μA
Peak Reverse Blocking Current	I_{RRM}	V_{AK} = +5V V_{GA} = +15V	T_C = 150°C	---		4	mA
			T_C = 25°C	---		100	μA
On-State Voltage	V_{TM}	I_C = I_{C90}, V_{GA} = -10V	T_C = 150°C	---		1.3	V
			T_C = 25°C	---		1.4	
Gate-Anode Leakage Current	I_{GAS}	V_{GA} = ±20V		---		200	nA
Input capacitance	C_{is}	V_{AK} = -20 V V_{GA} = +15 V	T_j = 25°C	---	---	11	nF
Output Capacitance	C_{os}					TBD	nF
Current Turn-on Delay Time	$t_{d(on)i}$	L = 50μH, I_C = I_{C90}		---	---	400	ns
Current Rise Time	t_{ri}	R_g = 1Ω, V_{GA} = +15V,-10V		---	---	500	ns
Minimum on time	$t_{(\alpha)}$			TBD	---	---	μS
Current Turn-off Delay Time	$t_{d(off)i}$	T_J = 125°C		---	---	700	ns
Current Fall Time	t_{fi}	V_{AK} = -300 V		---	---	1.4	μS
Turn-off Energy	E_{off}			---	---	15	mJ
Thermal Resistance	$R_{\theta JC}$			---	.5	.6	°C/W

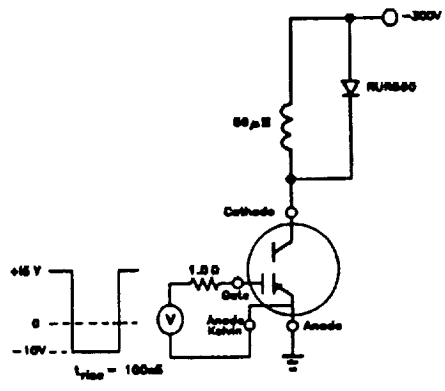


Figure 1 - Switching Circuit.

Handling Precautions for MCT's

Mos Controlled Thyristors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. MCT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORB LD26" or equivalent.

2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.

3. Tips of soldering irons should be grounded.

4. Devices should never be inserted into or removed from circuits with power on.

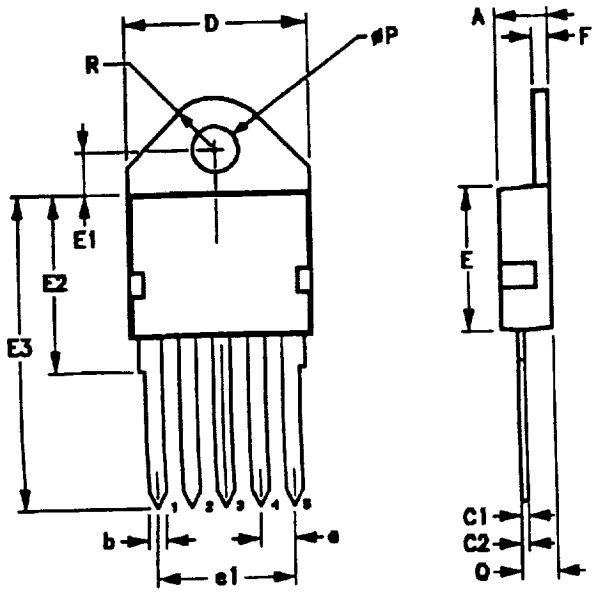
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GA}. Exceeding the rated V_{GA} can result in permanent damage to the oxide layer in the gate region.

6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.

7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

* Trademark Emerson and Cumming, Inc.

MO-093 Plastic Package



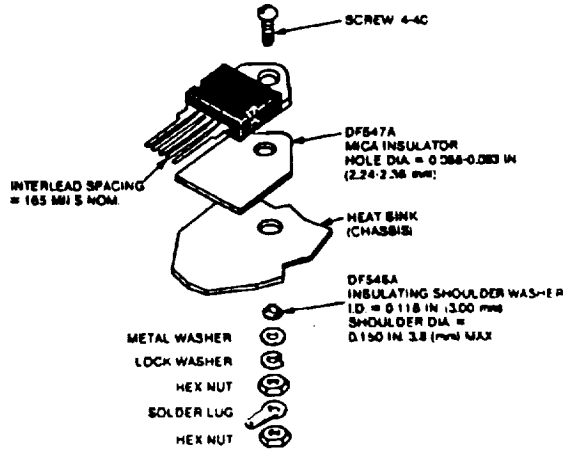
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.180	0.200	4.58	5.08	
b	0.048	0.054	1.22	1.37	6
C1	0.018	0.022	0.458	0.558	6,8
C2	–	0.028	–	0.711	6,7
D	0.615	0.625	15.62	15.87	
e	0.1095BSC		2.7813BSC		
e1	0.438REF		11.125REF		
E	0.480	0.490	12.20	12.44	
E1	0.135	0.155	3.43	3.93	
E2	–	0.750	–	19.05	
E3	1.204	1.224	30.59	31.09	
F	0.057	0.063	1.448	1.600	
ϕP	0.159	0.163	4.039	4.140	
Q	0.110	0.130	2.80	3.30	
R	0.176	0.186	4.47	4.72	

NOTES:

1. This package is similar to TO-218
2. Maximum radius 0.050" on all body edges and corners.
3. Tab outline optional within boundaries of Dimensions D and R.
4. Controlling dimension: Inch.
5. Details of Hold-Down Clamp Notch are optional.
6. Lead dimensions and tolerances apply over entire lead length beyond E2.
7. Includes lead finish.
8. Lead base material thickness only.

TERMINAL CONNECTIONS

Lead #1 - Gate
Lead #2 - Anode Kelvin
Lead #3 - Cathode Kelvin
Lead #4 - Anode Current
Lead #5 - Anode Current
Mounting Flange - Cathode Current



92CS-39588

Suggested mounting hardware for JEDEC TO-218AC.