Characteristics of 0.8- and 0.2-μm Gate Length $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As/InP$ ($0.53 \leq x \leq 0.70$) Modulation-Doped Field-Effect Transistors at Cryogenic Temperatures

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***Abstract*—We have investigated analytically and experimentally the performance characteristics of InP-based $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ ($0.53 \leq x \leq 0.70$) pseudomorphic modulation-doped field-effect transistors (MODFET's) as a function of strain in the channel, gate, length, and temperature. The strain in the channel was varied by varying the In composition x. The temperature was varied in the range of 40–300 K and the devices have gate lengths L_g of 0.8 and 0.2 μm. Analysis of the device was done using a one-dimensional self-consistent solution of the Poisson and Schrödinger equations in the channel, a two-dimensional Poisson solver to obtain the channel electric field, and a Monte Carlo simulation to estimate the carrier transit times in the channel. An increase in the value of the cutoff frequency is predicted for an increase in In composition, a decrease in temperature, and a decrease in gate length. The improvements seen with decreasing temperature, decreasing gate length, and increased In composition were smaller than those predicted by analysis. The experimental results on pseudomorphic InGaAs/InAlAs MODFET's have shown that there is a 15–30% improvement in cutoff frequency in both the 0.8- and 0.2-μm gate length devices when the temperature is lowered from 300 to 40 K.**

I. Introduction

INDIUM PHOSPHATE-based pseudomorphic modulation-doped field-effect transistors (MODFET's) have demonstrated high-frequency and low-noise performance superior to that of any other field-effect transistors [1], [2]. In exploring the properties of high-performance pseudomorphic MODFET's, there are several important and critical issues. The transport properties of the channel and ultimately the device performance depend on the nature of the heterointerface across which electron transfer takes place. This, in turn, depends on the amount of strain in the channel, the growth parameters, and the growth modes. The question is, how much strain should be accommodated in the channel before the advantages listed above are outweighed by growth-related factors which ultimately degrade the transistor performance? Another important issue is the improvement in the performance of pseudomorphic MODFET's as the gate length is reduced. In other words, it is important to determine if the performance of submicrometer-gate pseudomorphic MODFET's is significantly better than that of lattice-matched submicrometer devices. Finally, cryogenic operation of MODFET receivers and amplifiers has shown improved gain characteristics and lower noise figures compared to operation at room temperature [3], [4]. Other potential benefits such as greater reliability, lower metal resistance, and integration with high-temperature superconductors have further increased the interest in MODFET operation at cryogenic temperatures [5].

In the work reported here, we have investigated some of these issues in the context of understanding the performance characteristics of 0.8- and 0.2-μm gate length $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ heterostructure ($x = 0.53$, 0.60, and 0.70) pseudomorphic MODFET's at cryogenic temperatures.

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II. Numerical Analysis of Device Performance

We have analyzed the microwave performance of both the 0.8- and 0.2-μm devices in order to understand the characteristics of pseudomorphic InGaAs/InAlAs MODFET's. The schematic of a typical structure is shown in Fig. 1. The source-to-drain spacing is 3.5 and 2.0 μm for the 0.8- and 0.2-μm gate-length devices, respectively. The unintentional background doping for the InGaAs and InAlAs layers is assumed to be 2.0×10^{15} cm^{-3}. The simulation was carried out as follows: first, the charge distribution in the growth direction (z direction) was obtained by self-consistently solving one-dimensional Poisson's equation and Schrödinger equation; next the two-dimensional Poisson's equation was solved for the device by a finite difference technique and the electric field along

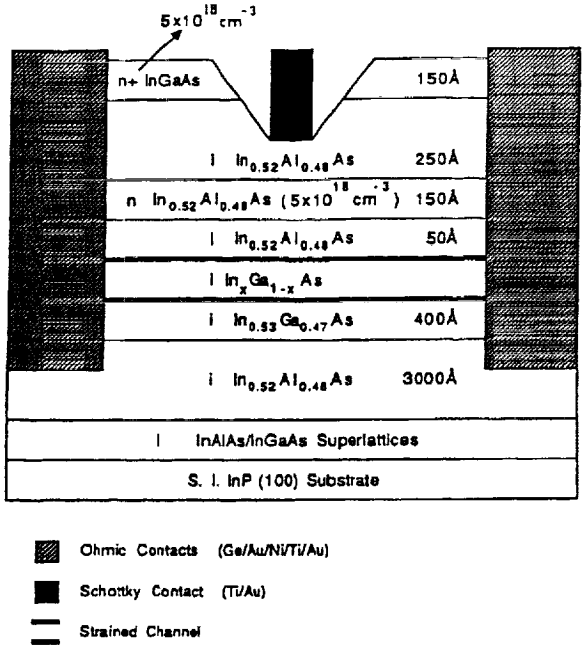

Fig. 1. Layer schematic of pseudomorphic $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ (x = 0.53, 0.60, and 0.70) channel MODFET's on InP substrates.

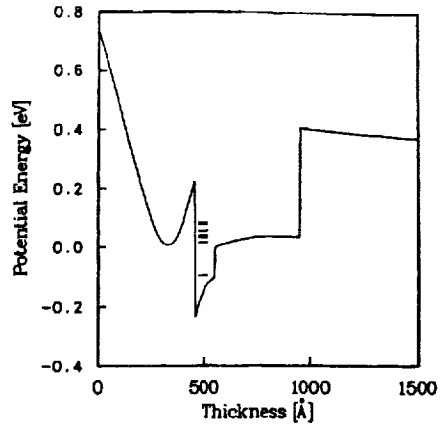

Fig. 2. Calculated conduction band profile and subband energies of strained-channel $In_{0.6}Ga_{0.4}As/In_{0.52}Al_{0.48}As/InGaAs$ MODFET (V_{gs} = V_{ds} = 0 V, T = 300 K).

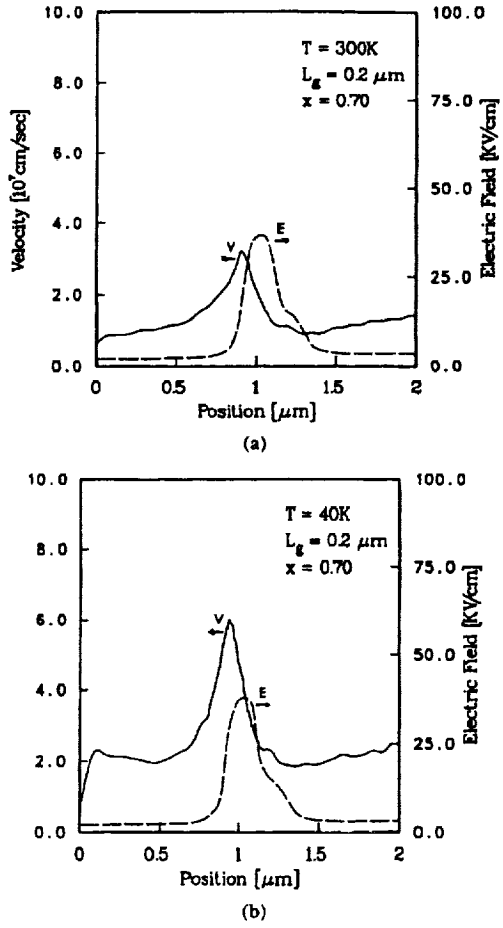

Fig. 3. Calculated electron velocity and electric field versus position in the source–drain region of an $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ MODFET having a 0.2-μm gate-length and 2.0-μm source–drain spacing with V_{gs} = 0.2 V and V_{ds} = 1.5 V at a temperature of (a) 300 K and (b) 40 K.

the channel (x direction) was found; finally, the Monte Carlo technique [6], [7] was used for transient analysis of electron transport in the pseudomorphic InGaAs channel. A typical calculated band profile is shown in Fig. 2. The electric field profiles for a 0.2-μm device with In composition x = 0.70 are shown in Fig. 3(a) and (b). The gate is located in the middle of the plot, i.e., from 0.9 to 1.1 μm in position.

Self-consistent solutions of Poisson and Schrödinger equations show that as the In content in the pseudomorphic channel increases, the sheet charge carrier density n_s also increases. This is expected and has been also observed experimentally. It arises mainly due to the increase in the band offset at the heterointerface ΔE_c with increasing indium in the channel. Note that in order to improve the quality of the active heterojunction, a 400-Å smoothing layer of lattice-matched InGaAs is incorporated below the channel layer. The electron wave function actually extends into this buffer layer, which can lead to inferior charge control with gate bias. Higher indium composition in the channel layer can lead to better charge confinement so that most of the conduction electrons will have smaller effective mass.

The electric field obtained from the solution of two-dimensional Poisson equation shows that most of the channel, except the region below the gate, is under low electric field. At the drain side of the gate, the electric field increases due to a pinch-off effect. As the gate length decreases from 0.8 to 0.2 μm, the electric field under the gate changes abruptly (Figs. 3(a) and (b)) due to the small dimension of the Schottky gate.

The Monte Carlo analysis gives insight to the electron transport properties in the channel. For both 0.8- and 0.2-μm gate-length devices, a small fraction of the electrons traveling in the high-field region of the channel are scattered into the L valley. They gradually relax back into the Γ valley as they travel through the gate–drain section. This is shown, as an example, in Fig. 4 for a 0.2-μm gate-

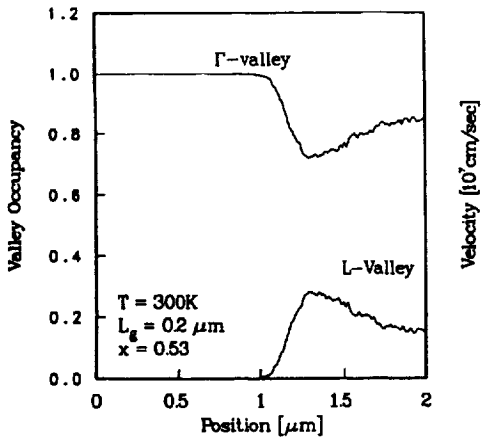

Fig. 4. Calculated Γ- and L-valley occupancy versus position in the source-drain region of an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ MODFET with 0.2-μm gate-length and 2.0-μm source-drain spacing. V_{gs} = 0.2 V and V_{ds} = 1.5 V for this calculation.

length device with the In composition in the channel x = 0.53. As x increases, the transfer to the L valleys decreases due to the larger Γ–L separation.

For the 0.8-μm gate-length device, the electron velocity in the channel increases with increasing In composition and decreasing temperature. For the 0.2-μm gate-length device, the abrupt change of the electric field under the gate leads to nonstationary transport [8]. Electron transport under the gate in these devices is dominated by velocity overshoot effects. Calculated 300 K velocities and electric fields in the channel for a 0.2-μm gate-length device with x = 0.7 are shown in Fig. 3(a). As the temperature is reduced to 40 K, phonon scattering is greatly reduced and the overshoot increases as seen in Fig. 3(b). The average channel velocities for the different samples at 300 and 40 K are listed in Table I.

The time required for electrons to transit the channel under the gate is obtained from a transient Monte Carlo analysis. The intrinsic cutoff frequency without considering the gate-drain transit time is then obtained from

$$f_{T,\text{int}} = \frac{1}{2\pi\tau} \tag{1}$$

where τ is the gate delay time. The calculated delay times for 0.8- and 0.2-μm gate-length device with channels of different composition and at temperatures of 40 and 300 K are shown in Fig. 5(a) and (b). The values of $f_{T,\text{int}}$ obtained from (1) are listed in Table II.

The trends in the calculated cutoff frequency values show the general improvement in values when increasing the In composition in the channel, decreasing the temperature, and decreasing the gate length. Indeed, we have observed experimentally the improvement in the average velocity for $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ ($0.53 \le x \le 0.65$) MODFET structures both with increasing In composition and decreasing temperature [9]. The improvement with increasing In composition can be attributed mainly to a smaller effective mass, a larger ΔE_c, and a decrease in alloy scattering. The improvement with decreasing temperature can be mainly attributed to a decrease in phonon scattering as well as other scattering rates. At the lower temperatures, polar optical phonon emission, ionized im-

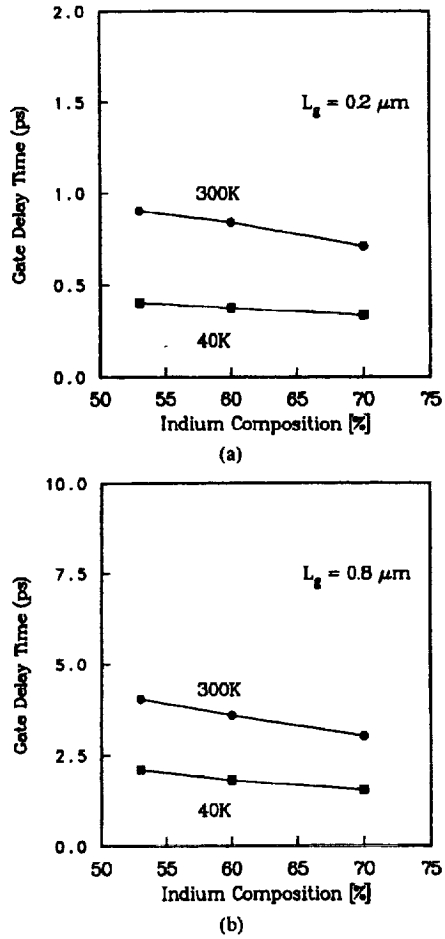

Fig. 5. Calculated gate delay times versus In composition at 300 and 40 K in pseudomorphic $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ (x = 0.53, 0.60, and 0.70) channel MODFET's with (a) a 0.2-μm gate-length device and (b) a 0.8-μm gate-length device with V_{gs} = 0.2 V and V_{ds} = 1.5 V.

TABLE I
AVERAGE CALCULATED CHANNEL VELOCITIES (10^7 cm/s) IN 0.2- AND 0.8-μm GATE PSEUDOMORPHIC $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ MODFET'S

V_{av} / x/L_g	300 K 0.8 μm	40 K 0.8 μm	300 K 0.2 μm	40 K 0.2 μm
0.53	0.98	1.96	1.08	2.13
0.60	1.06	2.17	1.17	2.20
0.70	1.20	2.42	1.35	2.50

TABLE II
ROOM AND LOW-TEMPERATURE INTRINSIC CUTOFF FREQUENCIES $f_{T,\text{int}}$ (GHz), OF 0.8- AND 0.2-μm GATE MODFET'S WITH PSEUDOMORPHIC $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ QUANTUM WELLS CALCULATED BY USING (1)

$f_{T,\text{int}}$ / x/L_g	300 K 0.8 μm	40 K 0.8 μm	300 K 0.2 μm	40 K 0.2 μm
0.53	39.5	75.7	176.2	396.1
0.60	44.4	87.7	189.2	426.1
0.70	52.7	102.4	223.9	474.4

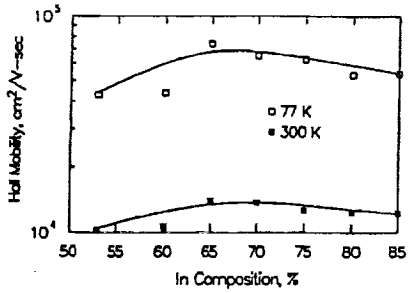

Fig. 6. Hall mobility versus In composition in pseudomorphic $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ ($0.53 \leq x \leq 0.85$) channel MODFET structures.

TABLE III
MEASURED MICROWAVE ROOM-TEMPERATURE CHARACTERISTICS OF 0.8- AND 0.2-μm GATE MODFET'S WITH PSEUDOMORPHIC $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ QUANTUM WELLS

L_g (μm)/x		0.53	0.60	0.65	0.70	0.75	0.80	0.85
0.8	f_T (GHz)	22-35	29-40	40-45	35-50	30-40	40-45	30-35
0.8	f_{max} (GHz)	40-55	40-60	45-55	60-70	40-50	40-55	45-50
0.2	f_T (GHz)	80-115	100-155		121-180			

purity scattering, piezoelectric scattering, and alloy scattering become the dominant scattering mechanisms. With decreasing gate length from 0.8 to 0.2 μm, velocity overshoot of the electrons increases the average velocity in the channel which leads to higher values of cutoff frequency. When combining the improvements seen with two or more of the variables (In composition, temperature, and gate length) interesting trends can be seen. The improvement seen with decreasing temperature is smaller as the In composition is increased in the channel. Also, the improvement seen with decreasing temperature is smaller with decreasing gate length. It should be noted that the data obtained from the analysis represent the theoretical uppermost limit in cutoff frequency obtainable for these devices. Due to nonideal device characteristics, such as interface roughness and interface traps in the layers, it is expected that any experimental data would show lower values for cutoff frequency compared to the theoretical ones, as will be evident in Section VI.

III. Molecular Beam Epitaxial Growth and Transport Properties

The next step was to attempt to verify experimentally some of the results and their trends derived from the theoretical analysis. Schematic of the typical MODFET structure grown by MBE is shown in Fig. 1. Hall measurements were first made on van der Pauw samples to determine the transport properties. The Hall samples were recessed so that the InGaAs cap layers were removed to reduce parallel conduction. The sheet electron density in all the samples varied in the range of $2.0\text{–}3.2 \times 10^{12}$ cm^{-2}. In Fig. 6, we show a plot of the 300 and 77 K mobilities versus In content in the channel. It may be noted that as excess In is added, initially the mobility increases as expected. However, upon further increase of In, the mobility starts to saturate and even decrease. We have recently analyzed this transport behavior in detail and have found that the turnaround in mobility occurs at large misfits ($>1.5\%$) due to the onset of a three-dimensional island growth mode [10]. In other words, the minimum free energy for a strained system for misfits $>1.5\%$ favors a three-dimensional surface. It is interesting and important to note that the dc and microwave characteristics of the MODFET's made with channels of increasing In content also exhibit the same behavior. In other words, the performance peaks at about $x = 0.70$ beyond which there is an observed degradation. The measured microwave characteristics of 0.8- and 0.2-μm gate pseudomorphic MODFET's at room temperature are listed in Table III.

IV. Device Fabrication

The heterostructures, shown in Fig. 1, were used to fabricate both 0.8- and 0.2-μm gate-length pseudomorphic $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ ($x = 0.53$, 0.60, and 0.70) MODFET's. Standard lithography was used to fabricate the devices. The source-to-drain separation for the 0.8- and 0.2-μm gate length devices were 3.5 and 2.0 μm, respectively. For the 0.8-μm gate devices, optical lithography was used while for the 0.2-μm gate devices, electron-beam lithography using a P(MMA-MAA)/PMMA bilayer resist system was used. With the bilayer resist, T-shaped gates consisting of Ti/Pt/Au were realized and the gate length was measured using Scanning Electron Microscopy (SEM) to be 0.15–0.2 μm. The gate widths on the devices ranged between 50 and 150 μm.

V. DC Characteristics

The 0.8-μm gate device showed a peak transconductance of 510 mS/mm at 300 K with a channel current of

200 mA/mm while the 0.2-μm gate device showed a peak transconductance of 705 mS/mm with a channel current of 300 mA/mm. Both devices were biased at a drain voltage of 1.5 V. The devices also showed low gate leakage (110 μA at $V_g = -0.5$ V for a 0.2 $\times$ 45 μm^2 device) and good pinchoff characteristics although in the submicrometer devices, output conductance increased dramatically. This increase in the output conductance may be attributed to an increase in leakage in the buffer layer, an increase in the background impurities (we observed a significant increase in the background impurities in our system when the wafers used for 0.2-μm gate devices were grown), and short-channel effects. 77 K dc measurements on the 0.8-μm gate device showed an increase in peak transconductance to 680 mS/mm, a decrease in output conductance from 40 to 20 mS/mm, and a decrease in gate leakage from 9 to less than 1.0 μA measured at a drain bias of 1.5 V and a gate bias of 0 V.

VI. Microwave Characteristics at Room and Cryogenic Temperatures

Room-temperature microwave characteristics were measured for both 0.8- and 0.2-μm gate devices and for each In channel composition. The scattering parameters were measured using an HP8510 automatic network analyzer and a CASCADE wafer probe station from 0.5 to 26.5 GHz at various gate and drain bias voltages. Table III shows some of the results of the pseudomorphic $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ MODFET's ($0.53 \leq x \leq 0.85$) that have been fabricated in our laboratory. Estimation of the maximum available gain cutoff frequency f_{max} for the submicrometer devices were not made because the stability factor k was smaller than 1.0 over the entire measured frequency range. The current-gain cutoff frequency f_T was extrapolated from the measured current gain (H_{21}) versus frequency dependence with a -6-dB/octave slope. The best result achieved was an extrapolated f_T value of 180 GHz for an $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ MODFET with a gate dimension of 0.15 $\times$ 150 μm^2 with a maximum stable gain (MSG) of 17.5 dB at 26.5 GHz.

For cryogenic microwave characterization, the devices were diced, mounted, and bonded to coplanar chip carriers. The devices were measured in a coplanar waveguide test fixture (DESIGN TECHNIQUES). A spring loading capability was added to the test fixture to ensure repeatable contacts between the device carrier and the coaxial connectors especially during cooling. The cryogenic system included a helium closed-cycle refrigerator, a temperature controller, a silicon diode thermometer, and the test fixture attached to the refrigerator cold finger in a vaccum environment. The cryogenic system is capable of achieving and stabilizing temperature down to 40 K. The microwave measurements were again done using an HP8510 automatic network analyzer. Prior to cooling the device, the measurement setup was calibrated at room temperature using a set of open, short, and through standards. Then, a short-circuit standard was

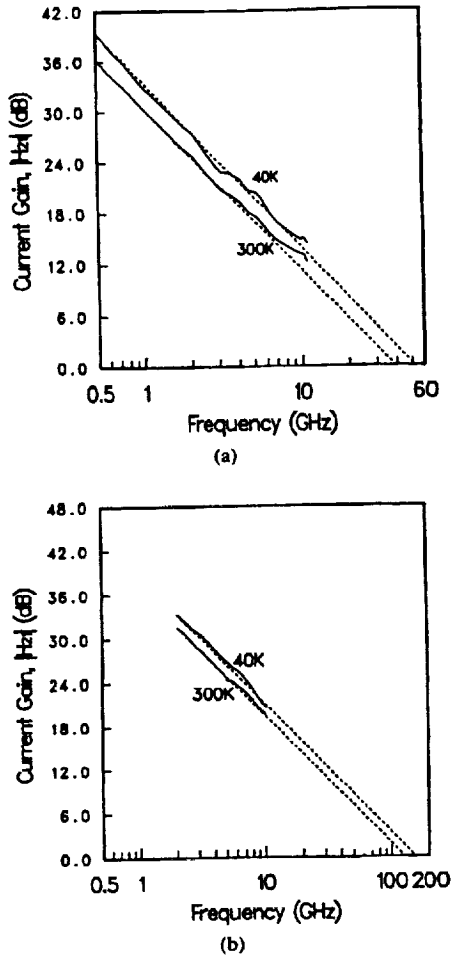

Fig. 7. Current gain H_{21} versus frequency for a pseudomorphic $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ channel MODFET at 40 and 300 K for (a) a 0.8-μm gate-length device and (b) a 0.2-μm gate-length device.

cooled to the desired temperatures to account for any shifts in the reference plane caused by the contraction of the cables, connectors, and the coplanar lines due to the lowering of temperature. This calibration method was found to be valid up to a frequency of 10–11 GHz. The problems at higher frequencies seem to be due to the fact that accounting for shifts in the reference plane is not sufficient to correct for the differences between room temperature and cryogenic temperatures. For example, the return loss for a through line measured at cryogenic temperatures after using the calibration routine becomes significantly degraded at higher frequencies.

The microwave characteristics of each device were measured at 300, 200, 120, 77, and 40 K from 0.5 to 11.0 GHz. The devices were measured over a range of V_{ds} from 1.2 to 1.8 V and at various values of V_{gs} near the peak g_m point. For both the 0.8- and the 0.2-μm gate devices, there was an observed increase in the measured magnitude of S_{21} of up to 3 dB and commensurate increase in the current gain H_{21} with decreasing temperature (shown in Fig. 7(a), (b) for the 0.8- and 0.2-μm gate devices with an $In_{0.70}Ga_{0.30}As$ channel) with decreasing temperature. The

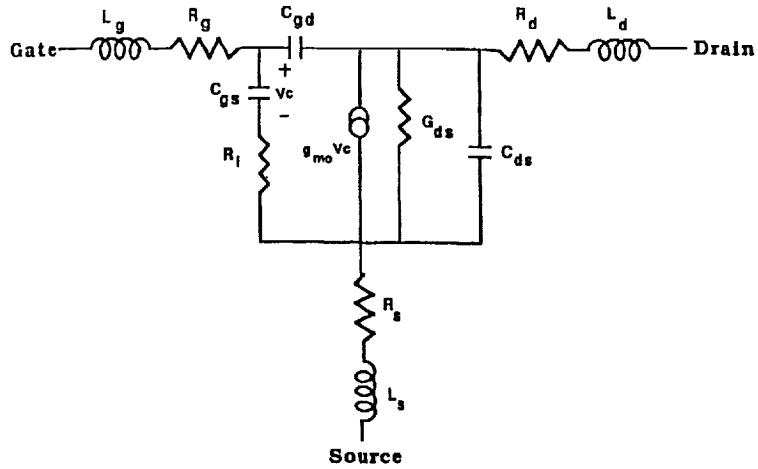

Fig. 8. Standard equivalent circuit model for a MODFET.

TABLE IV
EXTRAPOLATED VALUES FOR CUTOFF FREQUENCY f_T (GHz) FROM CRYOGENIC MICROWAVE CHARACTERISTICS OF 0.2- AND 0.8-μm GATE MODFET'S WITH PSEUDOMORPHIC $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ QUANTUM WELLS (V_d = 1.5 V)

f_T / x/L_g	300 K 0.8 μm	40 K 0.8 μm	300 K 0.2 μm	40 K 0.2 μm
0.53	22	29	92	105
0.60	29	38	105	130
0.70	38	51	121	145

data are summarized in Table IV, which gives the characteristics of specific devices measured at 300 and 40 K. The improvement in cutoff frequency with lowering of temperature from 300 to 40 K was generally found to be between 15 and 30% for all the devices.

TABLE V
EQUIVALENT CIRCUIT PARAMETERS OF 0.8-μm (V_d = 1.5 V, V_g = 0.0 V) AND 0.2-μm (V_d = 1.4 V, V_g = 0.15 V) GATE-LENGTH MODFET'S WITH PSEUDOMORPHIC $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ QUANTUM WELLS

	0.8 μm 300 K	0.8 μm 40 K	0.2 μm 300 K	0.2 μm 40 K
L_g (nH)	0.63	0.64	0.28	0.30
L_s (nH)	0.05	0.05	0.07	0.07
L_d (nH)	0.51	0.53	0.07	0.10
R_g (Ω)	5.61	4.27	8.14	7.78
R_s (Ω)	3.79	3.46	3.33	2.50
R_d (Ω)	3.78	3.37	3.64	3.08
R_i (Ω)	12.16	9.08	9.30	8.30
C_{gs} (pF)	0.265	0.286	0.15	0.17
C_{gd} (pF)	0.012	0.010	0.020	0.019
C_{ds} (pF)	0.052	0.054	0.060	0.065
τ_c (ps)	5.95	5.81	1.5	1.5
g_{mo} (mS)	75.0	97.9	133	184
G_{ds} (mS)	4.08	3.65	18.8	19.0

VII. Device Analysis and Discussion

The measured microwave data were modeled to a standard equivalent circuit model for a MODFET (Fig. 8). The fitting of the microwave data had a maximum error of 5–10% over the frequency range of 0.5 to 11.0 GHz primarily due to noise in the measured data. Table V shows the equivalent circuit parameters that were extracted for the pseudomorphic $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ MODFETs at 40 and 300 K. The parasitic gate-to-source capacitance C_{gs} is decreased as the gate length decreased from 0.8 to 0.2 μm, which will lead to an increase in cutoff frequency and hence the maximum oscillation frequency. The intrinsic f_T values showed approximately the same improvement in performance with lowering of temperature as the extrinsic f_T. The improvement in microwave performance for both the 0.8- and 0.2-μm gate-length devices is approximately 15–30% when the temperature is lowered from 300 to 40 K and the relative improvement is found to be approximately the same as In composition in the channel is increased. The experimental results indicate a smaller improvement of cutoff frequency as In composition is increased and temperature is decreased than the values predicted in the analysis. More experiments need to be done to further investigate this point. However, the improvement with decreasing temperature was found to be slightly higher in the 0.8-μm device (25–30%) compared to the 0.2-μm (15–20%) device. This is consistent with the trend predicted by the analysis. Also, the values for cutoff frequency measured experimentally are significantly less than those predicted in the analysis section. Part of the reason may be due to the fact that effective gate length of a MODFET is larger than the metallurgical gate length [11]. The extra effective gate length can add up to an increase of 0.08 μm to the gate length of the device and can explain part of the difference between the calculated and measured data. Note that the transconductance delay time τ_c, which is obtained from a fit of the measured microwave data with the equivalent circuit, is different from τ in (1).

The extracted output conductance G_{ds} decreases with lowering of temperature, as shown in Fig. 9 for a 0.8-μm gate device with an $In_xGa_{1-x}As$ channel (x = 0.53, 0.60, and 0.70), and this trend is the same as that for the dc

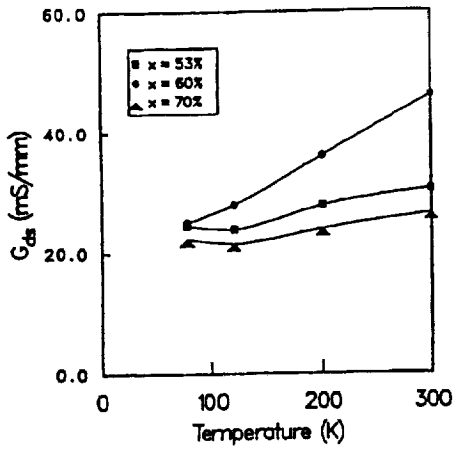

Fig. 9. Output conductance G_{ds} versus temperature for pseudomorphic $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ (x = 0.53, 0.60, and 0.70) channel MODFET's with V_{ds} = 1.5 V and V_{gs} biased for peak gain.

measured output conductance. The main reason for this is the improved confinement of the carriers in the 2DEG channel at lower temperatures. A slight increase in the extracted gate to source capacitance C_{gs} was also observed (10%). This has been previously observed and modeled in GaAs/AlGaAs MODFET's [12]. It should be noted that the trends in G_{ds} and C_{gs} with temperature were observed for both the 0.2- and 0.8-μm gate-length devices.

Another observation that was made during these measurements was the absence of significant effects due to deep-level traps such as the collapse of I–V characteristics which have been seen in AlGaAs/GaAs MODFET structures at low temperatures [13]. It should be noted that since the chamber was completely enclosed, the measurements were carried out in the dark. A small threshold shift of up to +0.21 V was observed in the dc characteristics for both the 0.2- and 0.8-μm gate-length devices. This value is smaller compared to the threshold shifts observed in AlGaAs/GaAs MODFET devices which typically range from +0.2 to +0.4 V [13]. The threshold shift in AlGaAs/GaAs MODFET's were mainly due to DX centers in the AlGaAs layers. Meanwhile, the threshold voltage shift in InAlAs/InGaAs MODFET's were due to interface traps in the InAlAs/InGaAs interface.

VIII. Conclusion

In conclusion, we have investigated the performance characteristics of InP-based pseudomorphic MODFET's with varying the In composition ($0.53 \leq x \leq 0.70$) which changes the strain in the channel. The temperature is varied in the range of 40–300 K and the devices have gate lengths L_g of 0.8 and 0.2 μm. The analytical analysis predicts an increase in the intrinsic cutoff frequency with increasing In composition and decreasing temperature and gate length. Also, the analysis predicts that the increase in cutoff frequency with decreasing temperature is less significant with increasing In composition and decreasing gate length. Preliminary experimental results show that as In composition increase from 0.53 to 0.70, f_T increase by 30–40%, and as the temperature decrease from 300 to 40 K, f_T improves by 15–30%, both for 0.8- to 0.2-μm devices. These are among the first reported microwave measured data of pseudomorphic $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ MODFET's at cryogenic temperatures.

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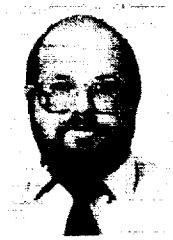

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PERFORMANCE OF A WIDEBAND GaAs LOW-NOISE AMPLIFIER AT CRYOGENIC TEMPERATURES

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KEY TERMS

GaAs low-noise amplifier, cryogenic temperatures, microwave measurements

ABSTRACT

The gain, noise figure, and 1-dB compression point of a commercially available GaAs amplifier were measured at cryogenic temperatures. The gain and noise figure characteristics were improved by decreasing temperature, while the 1-dB compression point remained unchanged. Repeated temperature cycling had no adverse effect on amplifier performance. © *1992 John Wiley & Sons, Inc.*

I. INTRODUCTION

It is well known that semiconductor devices and circuits exhibit lower noise figures and higher gains at cryogenic temperatures [1–3]. The lower noise figure is due to reduced lattice vibrations in the device and the fact that external, additive noise varies directly with the absolute temperature. Gallium arsenide (GaAs) devices have better low-temperature characteristics than silicon devices, since they do not suffer from carrier freeze out when the doping is insufficient to form impurity bands. As a result, GaAs conductivity remains high even at very low temperatures, where Si conductivity is decreasing. The higher conductivity of GaAs makes it the key semiconductor in microwave devices and circuits. GaAs and heterostructure FETs have been extensively investigated at cryogenic temperatures [1–3]; however, GaAs monolithic microwave integrated circuits (MMIC) only recently have been evaluated. It was found that cryogenic operation would result in an increase in gain and a reduction in noise figure of MMICs, as is observed for discrete GaAs FET amplifiers [4, 5].

While important parameters for determining the cryogenic gain of an FET circuit, such as the transconductance at cryogenic temperatures, can sometimes be inferred from room-temperature data, this is not uniformly true. The same holds for cryogenic temperature values of minimum noise temperature. The spread in values is smaller for FETs from the same lot than for FETs from different lots. This means that before any amplifier design with stringent specifications can be carried out, extensive testing of the devices to be used will have to be performed. For devices such as distributed amplifiers, an additional problem is one of maintaining the integrity of bonds, traces, and/or solder joints. This is especially true if the device is repeatedly cycled over temperature.

II. EXPERIMENTAL DESIGN

For our experiment we used an AVANTEK low-noise amplifier (LNA), the PGM 11421. The amplifier is specified with a frequency response from 4 to 11 GHz, a minimum gain of 8.0 dB, a typical noise figure of 2.5 dB, and a minimum power output for 1-dB gain compression of +5 dBm. The dc bias for the package was 8 V at 60 mA (max.) The amplifier was mounted in a brass test fixture between 50-Ω input/output microstrip lines which were fabricated on a 10-mil Duroid (ϵ_r = 2.3) substrate, designed to be 1-λ_g long at 8 GHz. This length as chosen so as to minimize the interaction between the launcher pins and the amplifier. The coax to microstrip connection was accomplished by using SMA female flange connectors. A small amount of silver paint was used to improve the contact between the center conductor of the launcher and the microstrip line, and 0.010-in. diameter gold bond wire was used to connect the microstrip line to the amplifier package.

To measure the performance of amplifiers at low temperatures, a cryogenic system was used. It consists of a test chamber which can be evacuated by a vacuum pump, a cold finger on which the sample is mounted, an electrical feedline which supplies dc bias to the amplifier, and two electrical temperature sensors. With no thermal load, the cold finger is capable of achieving a temperature of 10 K. The sensors were connected to a temperature controller which could maintain a desired temperature by controlling a heater element wrapped around the cold finger via a feedback system. Two semirigid copper coaxial cables which extend beyond the cryocooler are used as input and output lines for the RF signals. Each semirigid cable is 12 in. long to minimize the thermal load on the circuit in the cryostat as well as the thermal gradient between the inside and outside environments. A piece of indium foil was put between the cold finger and the test fixture to help increase the thermal conductivity.

One of the temperature sensors was mounted on the cold finger; the other one was alternately mounted on the top surface of the test fixture, or on the side of the fixture as close as possible to the amplifier. There is a temperature difference between the two locations of the sensor on the test fixture of nearly 4 K. This temperature difference would vary with different types of amplifiers that had different dc bias levels. This is due to the fact that the amplifier is dissipating heat into the test fixture. While the sensor near the amplifier may indicate a temperature of 77 K, clearly the amplifier package is at a higher internal temperature. This is not considered a problem since the purpose of the experiment is to see whether or not commercially packaged devices could function in the cryogenic environment which is required to exploit the advantages of high-temperature superconducting passive (HTS) devices that must operate at cryogenic temperatures. Whatever advantages may be obtained by cooling the package amplifier to its actual internal temperature is an added bonus to the primary advantage of using these packaged devices in the same cryogenic environment along with HTS passive devices.

The *S* parameters were measured on a HP 8510B automatic network analyzer. A full two-port calibration was performed at the ends of the semirigid coax inside the cryostat so as to establish the reference planes at the terminals of the amplifier test fixture. The calibration performed at 300 K was used to make the measurements at 77 K, since no practical method exists at the present to perform this calibration at 77 K inside the cryostat. A two-port calibration was chosen over a TRL calibration since the amplifier test fixture was one piece, so that separate TRL fixtures would be required to perform the calibration. Using separate test fixtures would introduce errors due to physical differences in the test fixtures used to perform the TRL. As is the case for two port calibration, no

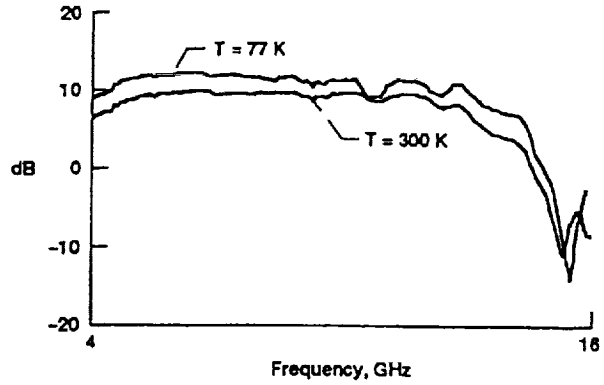

Figure 1 Gain of the LNA at T = 300 K and T = 77 K

technique exists at present to perform a TRL calibration at low temperature that does not involve repeated temperature cycling. Since the purpose of this experiment was to determine whether or not commerical amplifier packages can operate reliably at cryogenic temperatures, it was determined that a two-port calibration would suffice for this experiment. Future work will focus on optimum measurements and characterization of these devices, at which time a text fixture suitable for accurate TRL calibration will be used.

III. RESULTS

Figure 1 displays the measured S_{21} values for the PGM 11421 GaAs FET amplifier at room temperature and 77 K. The useful frequency range of this amplifier is specified as 4–11 GHz. These figures show that the gain increased about 2 dB with decreasing temperature from 300 to 77 K. As expected, the bandwidth increased at low temperature since the transconductance increases and output capacitance decreases with decreasing temperature, and these parameters determine the high-frequency cutoff for an FET [7].

Noise-figure measurements were made on a HP 8970A noise figure meter. Figure 2 shows the values for the noise figure at 300 and at 77 K. These results show that the noise figure was about 2.5 dB at room temperature, and dropped to about 1 dB at 77 K.

To obtain accurate noise figure measurements, the LNA was replaced by a 50-Ω thru line supplied by Avantek, and the insertion loss for the test fixture, along with the two semirigid cables of the cryostat were measured on the ANA at 300 and at 77 K. This loss was measured to be nearly 2 dB at 300 K, and 1 dB at 77 K, over the frequency range of 4.0–11.0 GHz. One half of this loss, representing the loss of the test setup up to the input to the LNA, was subtracted away

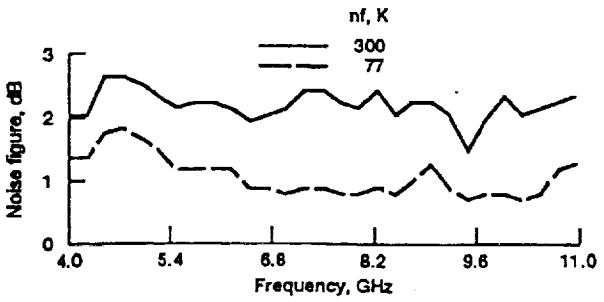

Figure 2 Noise figure of the LNA at T = 300 and 77 K

TABLE 1 Measured Input 1-dB Gain Compression Points at Selected Frequencies for the PGM 11421 Low-Noise Amplifier at 300 and at 70 K. These Values have an Accuracy of ±0.5 dB.

	P_{in-1} (dBm)	
Frequency (GHz)	300 K	70 K
4.0	3.0	2.5
4.5	3.0	2.5
5.0	4.0	3.5
5.5	4.0	4.0
6.0	3.5	3.5
6.5	4.0	3.5
7.0	3.5	3.5
7.5	4.5	4.5
8.0	4.5	5.0
8.5	4.5	4.0
9.0	5.0	4.5
9.5	5.0	4.5
10.0	5.5	5.0
10.5	6.0	6.0
11.0	6.5	6.0

from the noise figure values obtained for the LNA. The other half of this insertion loss acts as a second stage contribution to the measured noise figure, and this was entered into the 8970A as a correction factor to the calibration that was performed. The effects of the bond wires are included in this measurement. The total insertion loss of the test fixture alone can be used to determine the actual gain of the LNA as well.

Table 1 shows the result obtained for the input 1-dB compression point at 300 and at 77 K. As may be seen from this table, the change in compression point with temperature is negligible. In order to perform this measurement, the loss in the cables used was measured in the HP 8510B at 300 and at 77 K. This information was used to accurately determine the input 1-dB compression point (P_{in-1}) for the amplifier.

To obtain these measurements, the LNA was cycled down to 77 K five times. It was used in other experiments as well, and has been cycled down to 35 K 30 times to date, and there has been no loss of performance noticed so far. The only low-temperature failures noticed in this experiment involved broken bond wires between the amplifier and the input/output microstrip lines. For reliable performance, it was found that the amplifier bonding pads should be located at the same height as the microstrip lines, and that there should be some slack introduced into the bond wire to allow for vibration from the compressor pump in the cold head assembly and thermal contraction in the Duroid substrate. The Duroid substrate had to be firmly bonded to the test fixture near the amplifier to ensure against warping in the substrate as the fixture is cycled over temperature.

IV. CONCLUSION

This article has presented gain and noise figure performance of the commercial packaged GaAs amplifier at different temperatures. As expected, a lower noise figure and a higher gain were induced by decreasing the temperature. No significant change in the input 1-dB compression point was observed.

The results obtained in this experiment would indicate that commercially packaged devices can be used at cryogenic temperatures. This would be a significant help in developing cryogenic microwave sytems where packaged devices can be used in conjunction with high-temperature superconducting (HTS)

passive components [8], all at the same temperature. While this experiment does not establish the long-term reliability of commercial MMIC packages that are repeatedly cycled over temperature, it shows that there is potential for reliable operation in circumstances where the MMIC package is cooled only once, and kept at cryogenic temperatures for an extended length of time.

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FULL WAVE CHARACTERIZATION OF MICROSTRIP OPEN END DISCONTINUITIES PATTERNED ON ANISOTROPIC SUBSTRATES USING POTENTIAL THEORY

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Abstract

A technique for the full wave characterization of microstrip open end discontinuities fabricated on uniaxial anisotropic substrates using potential theory is presented. The substrate to be analyzed is enclosed in a cut-off waveguide, with the anisotropic axis aligned perpendicular to the air-dielectric interface. A full description of the sources on the microstrip line is included with edge conditions built in. Extention to other discontinuities is discussed.

Introduction

While there is extensive data available on the microwave characterization of a variety of microstrip discontinuities using both quasi-static [1-3] and full wave techniques [4-6], the characterization has been restricted to isotropic substrates. To date, there is no published data regarding microstrip discontinuities patterned on anisotropic substrates. Some very useful microwave substrates however, like sapphire, are anisotropic and so any discontinuity structures fabricated on them can not be properly characterized by the techniques that have been developed for isotropic dielectric substrates.

A technique for the full wave characterization of microstrip open ends fabricated on lossless uniaxial anisotropic substrates has been developed and is presented here. It is based on a dynamic source reversal technique that uses potential theory [7], which is a generalization of the charge resversal technique introduced several years ago [1]. The discontinuity is enclosed in a waveguide of infinite extent whose dimensions are such that the guide is cut-off for the propagating frequency on the microstrip. All sources on the microstrip are represented, and the technique does not require a model for the source exitation.

Dynamic Source Reversal Technique

The anisotropic axis of the substrate is aligned perpendicular to the air-dielectric interface as shown in Fig. 1. The anisotropic dielectric may be represented as a tensor quantity given by

$$\kappa(y) = \kappa(y)\mathbf{I} + [\kappa_y(y) - \kappa(y)]\mathbf{a}_y\mathbf{a}_y \tag{1}$$

where I is the unit dyad and $\kappa(y) = \kappa_y(y) = 1$ for $y > h$. The microstrip line is assumed to be infinitely thin and located at a height $y = h^+$. In terms of the sources on the microstrip line, the scalar and vector potentials, Φ and A respectively, for the dielectric loaded waveguide may be determined from

$$(\nabla^2 + \kappa k_0^2)A_x = -\mu_0 J_x \tag{2}$$

$$(\nabla^2 + \kappa k_0^2)A_z = -\mu_0 J_z \tag{3}$$

$$(\nabla^2 + \kappa_y k_0^2)A_y = j\omega\mu_0\epsilon_0(\kappa - 1)\Phi(h)\delta(y - h) + j\omega\mu_0\epsilon_0(\kappa_y - \kappa)\partial\Phi/\partial y \tag{4}$$

$$[\kappa(\partial^2/\partial x^2 + \partial^2/\partial z^2) + \partial(\kappa(y)\partial/\partial y)/\partial y + \kappa^2(y)k_0^2]\Phi = -\rho/\epsilon_0 + j\omega(\kappa_y - 1)A_y(h)\delta(y - h) - j\omega(\kappa_y - \kappa)\partial A_y/\partial y \tag{5}$$

The potentials appearing in Eqs. (2) to (5) are obtained from the appropriate Green's functions and the corresponding sources using

$$A_{x,z}(x,h,z) = \mu_0 \int_{x'} \int_{z'} G_{x,z}(x,h,z;x',h,z')J_{x,z}(x',h,z')dx'dz' \tag{6}$$

*National Research Council—NASA Research Associate at Lewis Research Center.

$$\epsilon_0\Phi(x,h,z) = \int_{x'}\int_{z'} G_\Phi(x,h,z;x',h,z')\rho(x',h,z')dx'dz' \quad (7)$$

From these potentials the electric field components are found using

$$E_x = -j\omega A_x - \partial\Phi/\partial x$$

$$E_y = -j\omega A_y - \partial\Phi/\partial y$$

$$E_z = -j\omega A_z - \partial\Phi/\partial z \quad (8)$$

where it is required that for this particular geometry E_x and E_z vanish on the microstrip. The fields thus obtained are expressed in terms of LSE and LSM modes of the dielectric loaded waveguide. The anisotropic effect appears only in the LSM mode terms, which are present in A_y and Φ. The LSE modes are unchanged from those obtained for the isotropic case.

A complete set of dominant mode sources on the microstrip are represented; the longitudinal and transverse currents, as well as the charge on the microstrip line, with appropriate edge conditions built in. For a wide range of practical open end discontinuities, a valid approximation is that $J_x = 0$, so therefore $A_x = 0$. As a result, only the boundary condition $E_z = 0$ is required for this problem.

A line terminated at $z = 0$, thus forming an open end, would create reflected dominant mode sources on the line, along with perturbed sources localized near the discontinuity. The total source distribution on an open end may be written as

$$J_z(x',h,z') = J_{0\,z}(x')(e^{-j\beta_z z'} - Re^{+j\beta_z z'}) + J_{1\,z}(x',z') \quad (9)$$

$$\rho(x',h,z') = \rho_0(x')(e^{-j\beta z'} + Re^{+j\beta z'}) + \rho_1(x',z') \quad (10)$$

for $z' \leq 0$, where $J_{0\,z}$, ρ_0 and β are the yet to be determined amplitudes and propagation constant, respectively of the dominant microstrip mode, R is an unknown reflection coefficient, and $J_{1\,z}$ and ρ_1 represent the perturbed source amplitudes near the open end. Weighted Chebychev polynomials are used to represent the sources in x for both dominant and perturbed sources, while triangle and pulse functions are used to represent the perturbed sources in z.

Equations (9) and (10) may be written as

$$J_z(x',h,z') = [j(1+R)J_{0\,z}(x')(B_{in}\cos(\beta z') - \sin(\beta z')) + jJ_{1\,z}(x',z')] \cdot [1 - U(z')] \quad (11)$$

$$\rho(x',h,z') = [(1+R)\rho_0(x')(B_{in}\sin(\beta z') + \cos(\beta z')) + \rho_1(x',z')] \cdot [1 - U(z')] \quad (12)$$

where $U(z')$ is the Heavyside unit step function which is 0 for $z' < 0$ or 1 for $z' > 0$, and $jB_{in} = (1-R)/(1+R)$ is the normalized input susceptance for the open end. In Eqs. (11) and (12) the dominant mode sources are assumed to exist for $-\infty \leq z' \leq \infty$. Then dominant mode sources for $z' > 0$ are subtracted away to create the terms that multiply the $(1 + R)$ coefficient in (11) and (12). Since the amplitudes of $J_{1\,z}$ and ρ_1 are arbitrary at this point, they may be defined so as to include the $(1 + R)$ term. Now the $(1 + R)$ term is common to all of the source terms, so it may be normalized to 1.0. Using Eqs. (11) and (12) in Eqs. (6) and (7) and substituting into Eq. (8) gives the electric field in terms of the sources on the open end microstrip line. When the requirement that $E_z = 0$ on the microstrip is enforced, the terms corresponding to the dominant mode on the infinite line already satisfy the boundary condition on the strip, so they drop out. The sources existing for $z' > 0$ may be considered "source reversed" terms which produce an impressed field in the reigon $z \leq 0$ but localized near the discontinuity. The factor $(1 + R)$ can be included into the arbitrary amplitude of the dominant mode sources. Thus, apart from the unknown parameter B_{in}, the dominant mode sources in $z' > 0$ produce a known forcing function in the strip for $z' < 0$. The electric field produced by the perturbed sources $J_{1\,z}$ and ρ_1, must cancel the tangential component of the applied field for $z \leq 0$. A modified perturbation technique [8] is used to determine the unknown dominant mode amplitudes and propagation constant for an infinite line. The method of moments is then used to reduce the resulting integral equation to a matrix equation which can be solved for the unknown input admittance B_{in}, as well as for $J_{1\,z}$ and ρ_1. Only one matrix inversion is required to find B_{in}.

Results

The pulse width, Δ, of the expansion functions was chosen to be 0.32 mm at f = 2.0 GHz (or $\Delta \simeq 0.0053\lambda_g$ for sapphire). This pulse width guaranteed a converged value for B_{in} [7] for all of the examples presented. To verify the accuracy of the theory as well as the resulting program, the program was checked for the isotropic case, and was able to duplicate data obtained in [1] and [7].

Table I shows the results obtained using this technique for several different anisotropic substrates as a function of microstrip line width. The open circuit capacitance, C_{oc} is found using $C_{oc} = B_{in}/\omega Z_0$, where the characteristic impedance Z_0 is obtained from a computer program developed on the basis of the theory presented in [8] for the characterization of infinite microstrip lines with sidewalls, but no top cover. To justify using values of Z_0 thus obtained, calculations performed for a microstrip line with an air dielectric showed less than 2% difference in Z_0 values obtained with and without a top cover. Table II shows the variation of C_{oc} as a function of line width for sapphire, and compares the results obtained for a substrate with an isotropic dielectric constant of 9.4, as well as for an isotropic dielectric constant of 11.6. Table III shows the effects of fixed waveguide dimensions on B_{in} and C_{oc} as a function of frequency of the propagating microstrip mode. For low frequencies, B_{in} varies linearly with frequency, starting to deviate as the frequency increases, this effect becomes more pronounced until the cut off frequency of the E_{11} waveguide mode is reached. This effect may be overcome by either frequency scaling the input parameters or by adjusting the waveguide dimensions accordingly.

The BASIC computer program developed to implement this technique can be executed on a personal computer with as little as 640K of RAM. Other discontinuity structures can be characterized in a similar manner. The technique is computationally efficient, there is no need to model the source excitation, and the admittance can be solved for directly in the case of a one port network. All integrals involving the expansion and testing functions are performed analytically so no numerical integrations are necessary, and the dominant portions of slowly converging series can be extracted and summed into closed form.

This technique can be extended to rapidly and accurately characterize a number of other commonly used discontinuity structures, especially "coaxial" two port structures such as asymmetrical gaps and steps in width. To characterize a two port structure in terms of an equivalent "Tee" or "Pi" network, the Tangent Plane method [9] can be used to extract parameter values.

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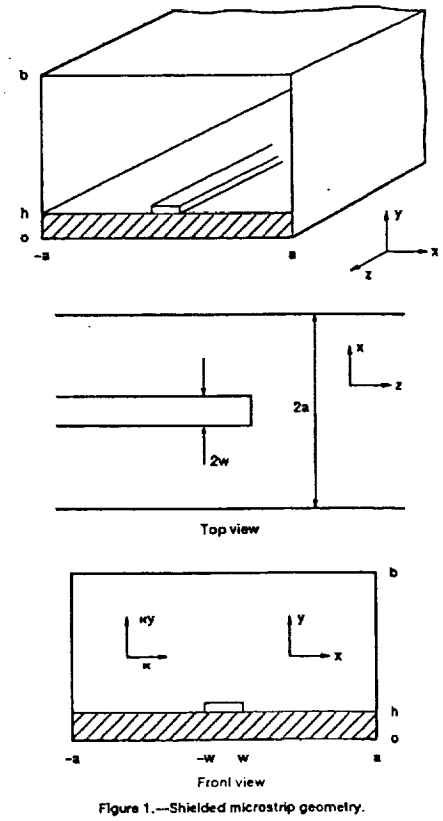

Figure 1.—Shielded microstrip geometry.

TABLE I.—OPEN CIRCUIT CAPACITANCE, C_{oc}, FOR SEVERAL ANISOTROPIC DIELECTRIC MATERIALS. FREQUENCY = 2.0 GHz, h = 1.0 mm, b = 11 mm, 2a = 20 mm FOR W/h < 4.0 ELSE 2a = 10(W/h). Z_0 VALUES OBTAINED FROM REF. 8. UNITS ARE pF/METER FOR C_{oc}.

		W/h					
		0.25	0.5	1.0	2.0	4.0	6.0
PTFE/Woven glass	κ_e	1.914	1.941	1.981	2.042	2.129	2.182
$\kappa = 2.84$	Z_0	150.5	119.9	90.02	62.46	39.82	29.50
$\kappa_y = 2.45$	C_{oc}/W	29.85	23.71	19.90	17.66	16.29	15.60
Boron nitride	κ_e	2.676	2.699	2.738	2.808	2.922	2.999
$\kappa = 5.12$	Z_0	127.4	101.7	76.68	53.38	34.09	25.25
$\kappa_y = 3.4$	C_{oc}/W	43.04	33.95	28.27	24.84	22.72	21.66
Sapphire	κ_e	6.724	7.012	7.647	8.145	9.007	9.514
$\kappa = 9.4$	Z_0	80.90	63.65	46.94	31.82	19.80	14.52
$\kappa_y = 11.6$	C_{oc}/W	80.36	65.56	56.38	50.95	47.43	45.35
Epsilam 10	κ_e	6.885	7.047	7.306	7.721	8.308	8.679
$\kappa = 13$	Z_0	79.90	63.44	47.39	32.61	20.55	15.14
$\kappa_y = 10.3$	C_{oc}/W	95.28	76.26	64.44	57.35	52.93	50.49

TABLE II.—VARIATION OF C_{oc} AS A FUNCTION OF LINE WIDTH FOR SAPPHIRE, $k = 9.4$, $k_y = 11.6$ COMPARED TO THAT OF AN ISOTROPIC DIELECTRIC. FREQUENCY = 2.0 GHz, h = 1.0 mm, b = 11 mm, 2a = 20 mm FOR W/h < 4.0, ELSE 2a = 10(W/h). UNITS ARE pF/METER FOR C_{oc}.

		W/h					
		0.25	0.5	1.0	2.0	4.0	6.0
Sapphire $\kappa = 9.4$ $\kappa_y = 11.6$	C_{oc}/W	80.36	65.56	56.38	50.95	47.43	45.35
$\kappa = 9.4$ $\kappa_y = 9.4$	C_{oc}/W	75.56	61.06	52.10	46.80	43.42	41.52
$\kappa = 11.6$ $\kappa_y = 11.6$	C_{oc}/W	90.18	73.27	62.58	56.21	52.13	49.77

TABLE III.—VARIATION OF THE NORMALIZED INPUT SUSCEPTANCE, B_{in}, AND OPEN CIRCUIT CAPACITANCE, C_{oc}, WITH FREQUENCY. WAVEGUIDE DIMENSIONS ARE 2a = 20 mm, b = 11 mm AND h = 1 mm.

Frequency, GHz	B_{in}	C_{oc}(pF/m)
0.5	0.008388	56.26
1.0	.016776	56.26
2.0	.033256	56.38
4.0	.068373	56.85
6.0	.167738	90.81