Space Qualified High Speed Reed Solomon Encoder[1]

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Abstract - **This paper reports a Class S CCSDS recommendation Reed Solomon encoder circuit baselined for several NASA programs. The chip is fabricated using United Technologies Microelectronics Center's UTE-R radiation-hardened gate array family, contains 64,000 p-n transistor pairs, and operates at a sustained output data rate of 200 MBits/s. The chip features a pin selectable message interleave depth of from 1 to 8 and supports output block lengths of 33 to 255 bytes. The UTE-R process is reported to produce parts that are radiation hardened to 1^6 Rads (Si) total dose and 1.0^{-10} errors/bit-day.**

1 General Description

This paper reports a JAN Level S radiation hardened gate-array implementation of a Reed Solomon (RS) encoder meeting the Consultative Committee for Space Data Systems (CCSDS) recommendations for code length and error detecting and correcting capability[1]. The gate-array meets the functional specification as the full custom CMOS VLSI encoder described by Whitaker and Liu[4]. A RS code is a powerful, relatively low overhead, cyclic symbol error correcting code which is particularly useful in correcting data suffering burst errors. In a spacecraft telemetry encoding system, a RS code may be used by itself or it may be concatenated with additional encoding for improved performance. While RS is used for burst error correction, CCSDS recommends convolutional encoding for correction of disbursed errors that result from Gaussian type noise. The RS code not only protects against burst errors resulting from the communications channel but also those resulting from the Viterbi decoding, used for decoding the CCSDS Convolutional code, where the decoded bit errors tend to clump together when its decoding capability is exceeded. The CCSDS recommendation calls for a (255,223) RS code where a data block contains 255 symbols, consisting of 223

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information symbols and $255 - 223 = 32$ RS check symbols. Since two check symbols are required for each error to be corrected, 32 RS symbols can correct 16 symbols errors. Such a code may be referred to as a RS16 code. Each symbol of this code has a length of eight bits, or one byte. Due to the flexible nature of the algorithms being implemented, the circuit will support the encoding of shortened, as well as full length RS codes. Specifically, the codes which are supported are of the form: $(255 - i, 223 - i)$, where i can be any integer from 0 to 222.

The code is defined over the finite field $GF(2^8)$. The field defining primitive polynomial is $p(x) = x^8 + x^7 + x^2 + x^1 + x^0$ and the generator polynomial is given by:

$$G(x) = \prod_{i=112}^{143} (x - \beta^i)$$

where $\beta = \alpha^{11}$. The encoder represents data in the Dual Basis defined by the following transforms:

$$[z_0, z_1, \ldots, z_7] = [u_7, u_6, \ldots, u_0] \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$[u_7, u_6, \ldots, u_0] = [z_0, z_1, \ldots, z_7] \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 \end{bmatrix}$$

where $[z_0, z_1, \ldots, z_7]$ is the symbol represented by the dual basis and $[u_7, u_6, \ldots, u_0]$ is the symbol represented by the normal basis.

2 Features

A block diagram of the chip is shown in Figure 1. Before circuit operation can begin, the encoder must be reset and the chosen interleave depth, I, must be set by bringing the interleave depth control pins, S_0, S_1 and S_2 to the appropriate state. The encoder can be programmed to interleave the data at depths of one, two, ... or eight. Interleaving of two or more encoded messages allows higher burst error correction capabilities.

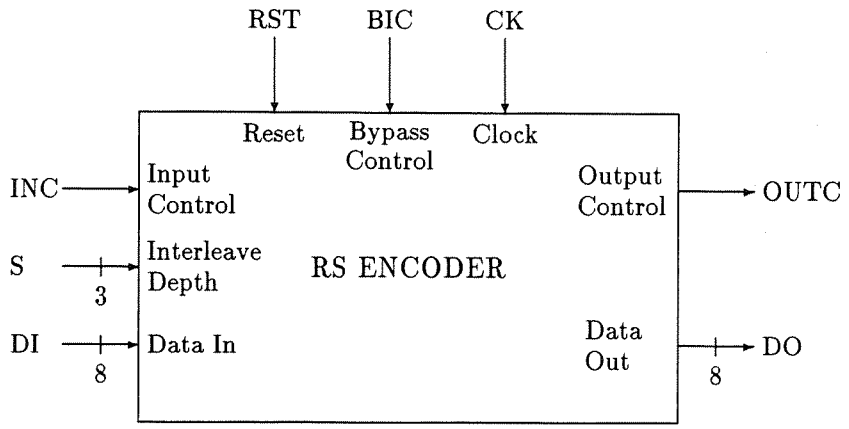

Figure 1: Block Diagram for the RS Encoder.

2.1 Encoder Operation

The encoder has eight data input ports, DI0-7, and eight data output ports, DO0-7. The information symbols are input at a constant rate in a byte serial fashion and the RS16 code is output byte serial after a fixed latency of one clock cycle. The input control (INC) pin must be brought high coincident with the first information symbol of the message to be encoded and remain high while all message symbols are clocked into the encoder. The INC pin is then brought low to signal the encoder that the last information symbol has been input. For a RS code encoding k information symbols, the first k codeword symbols are exactly the input symbols. While data is being clock into the encoder it is also passed directly to the output, with the fixed one clock cycle latency. The output control (OUTC) signal is brought high by the encoder to signal that the input data being encoded is being passed directly to the output. The OUTC output returns low after the last information symbol has been passed to the output. Beginning the next clock cycle after the last information symbol has been output, the 32 RS check symbols are concatenated to the output. The data and control signal timing is shown in Figure 2. The output data rate for the chip is 200 Mbits/sec when clocked at the maximum clock rate of 25 MHz.

2.2 Bypass Operation

A bypass mode included in the chip allows data flow through the encoder without being encoded. This is accomplished by bringing the bypass input control (BIC) pin high coincidentally with the first byte of data to be passed unprocessed by the chip. After the fixed one clock cycle latency, the data entering on the input appears on the output and continues to be passed through the chip as long as the BIC remains high. The INC pin should be held low during bypass operation to disable the generation of check check symbols within the encoder and keep the storage registers cleared.

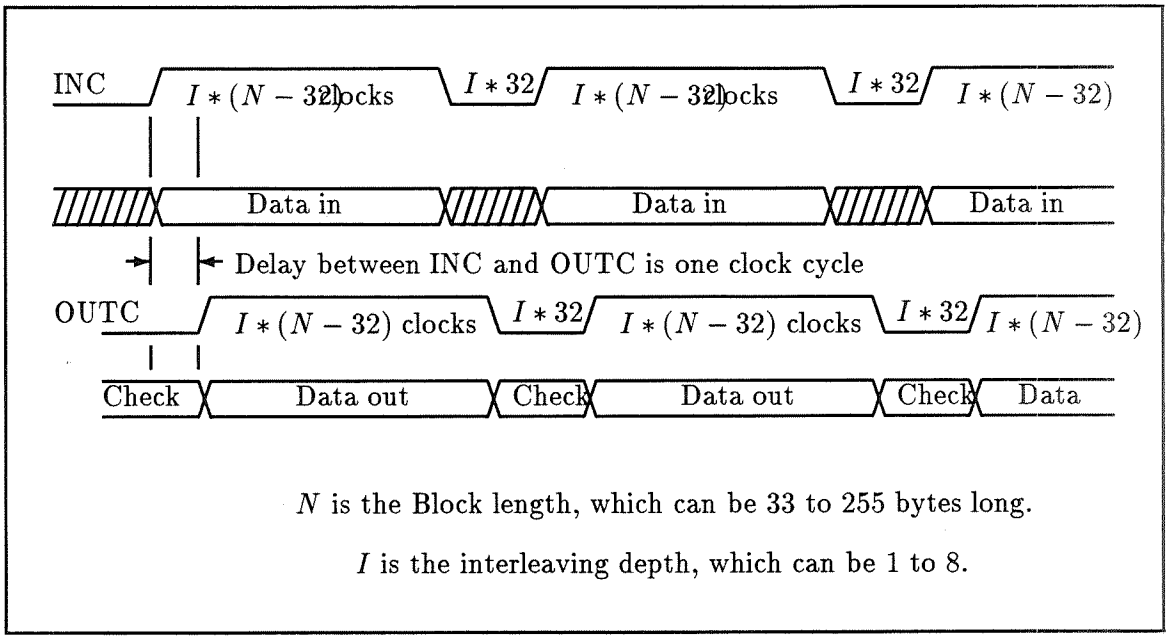

Figure 2: Input/Output Timing Diagram.

3 Chip Applications

Several NASA programs have baselined the use of this chip. They include the X-Ray Timing Explorer (XTE) and Tropical Rainfall Measuring Mission (TRMM). By encoding the telemetry data from these missions with the RS chip, a highly reliable data link will be established.

In addition to the RS coding, Convolutional encoding is performed after RS encoding to provide a higher coding gain than RS encoding alone. Figure 3 shows the theoretical performance of using various coding schemes[1].

The vertical axis shows the probability that there will be an uncorrectable bit error while the horizontal axis shows the information bit energy to noise ratio for a given communications link. For a desired probability of 10^{-5}, an information bit energy to noise ratio of 9.5 db is needed without any encoding and 2.3 db for a concatenated code (using both the RS and Convolutional codes). Therefore, using the concatenated code will give the desired bit error rate in the presence of considerable more noise than without encoding.

The selectable interleaving (I in Figure 2) provides mission flexibility to choose the interleaving while taking into account the tradeoffs for different interleave factors. No interleaving results in small data blocks while higher interleaving results in large data blocks. Large blocks are desirable because they provide better burst error correction. However, if a data dropout occurs, data will be lost on a block basis. Using large blocks will result in more data loss, while small blocks, because of their modularity, will result in less data lost. An interleave depth of 5 has been selected as a compromise for the XTE and TRMM programs.

The flexibility to vary the data block length (N in Figure 2) is important. Although

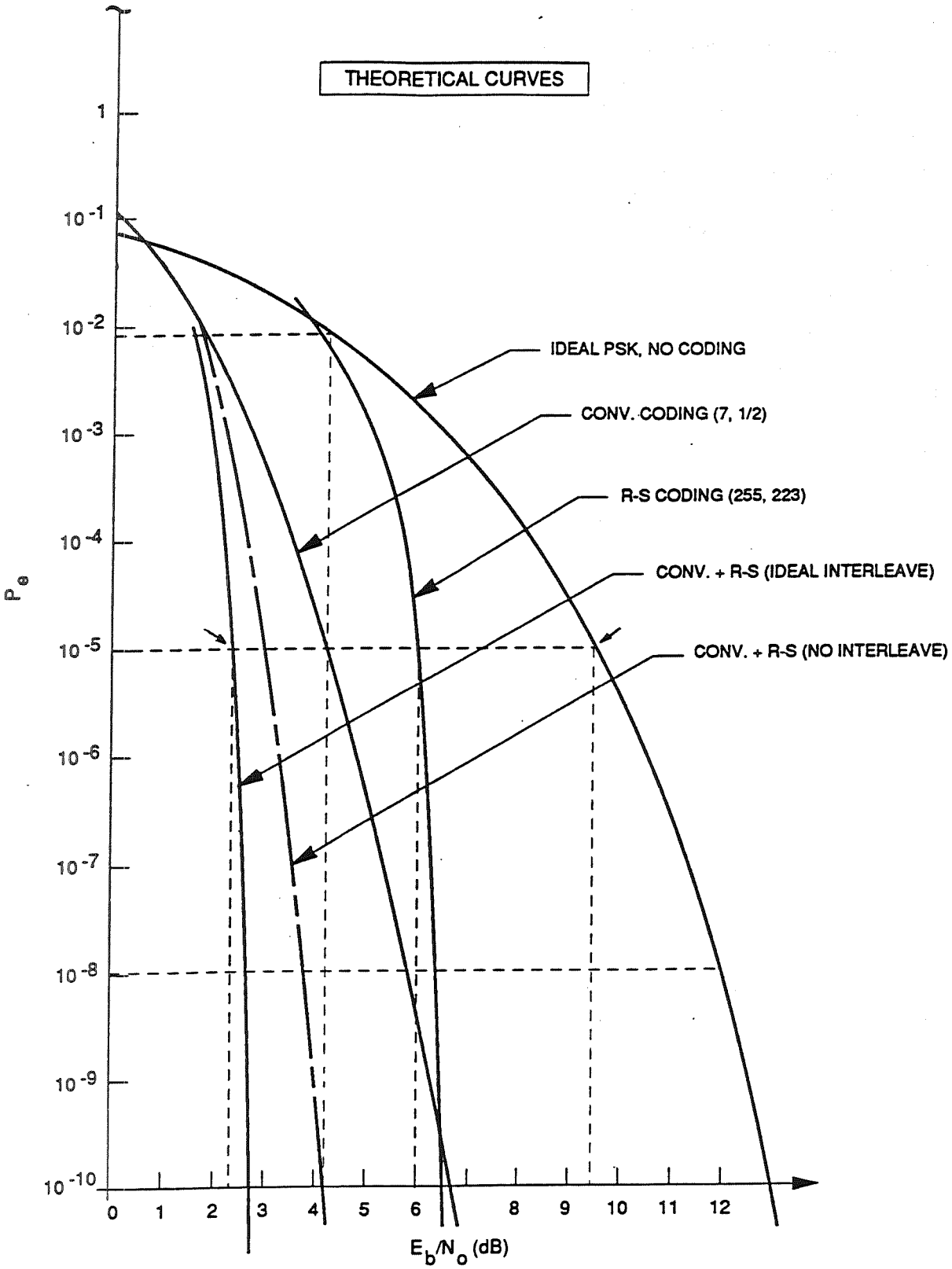

Figure 3: Relative Performance of Concatenated Coding with RS Outer Code (RS Ideal Interleaving and No-Interleaving Comparison)

the highest data throughput is achieved when the maximum size data block is used, a full data block may be impractical. The full code block is 255 bytes per interleave factor. When processed by a 32 bit (4 byte) word computer, the block will not fall on word boundaries. The XTE and TRMM programs will use the largest possible block that will fit on word boundaries. The resulting code is then a (252,220) code. For every 252 bytes, 220 are data and 32 are check symbols. Without the flexibility of the chosen RS algorithm to obtain the (252,220) code, zero fill would have to be used. In other words, the chip would have to receive 3 leading bytes of zeros to make 223 bytes of data instead of 220. At the output of the encoder the zeros should then be taken out so bandwidth is not wasted. Clearly, allowing for variable block sizes makes interfacing to the chip a lot cleaner for shortened code blocks.

CCSDS recommends that a 32 bit telemetry frame synchronization marker precede each data block. CCSDS also recommends that this marker not be included in the RS symbol calculations. The bypass mode allows the 32 bits to flow through the chip and not be included in the RS data block. This is also a cleaner approach than trying to insert the frame marker at the output of the RS chip.

Finally, the chip is available in a 84 pin QFP package which allows surface mounting of the device. This is the package used for XTE and TRMM.

4 The Implementation

4.1 Space Enhancement Features

The encoder has been fabricated using the United Technologies Microelectronics Center (UTMC) UTE-R Radiation-Hardened double metal gate-array process. The UTE-R process features submicron effective channel lengths (0.9μ leff, 1.2μ drawn) in a twin-tub, P-well epitaxail bulk CMOS technology employing special low-temperature processing techniques that enhance the total dose radiation hardness of the field and gate oxides[3]. The process is reported to be capable of producing parts tolerant of total dose radiation levels up to 1 Mrad (Si). UTMC gate-array products are listed on QPL-38510 and their double metal gate array process has been qualified for JAN Class S production.

In addition, the chip is designed to provide protection against Single Event Upsets (SEU) in two ways. First, the process and gate array cells are reported to be hardened against errors to less than $1.0X10^{-10}$ errors/bit-day. Second, the control structure and data path are configured to completely reset after each message insuring that an SEU of the data registers will effect at most one encoded message.

4.2 The Design

The encoder contains 32 multipliers and 33 adders which operate in parallel so that the mathematics required for check symbol generation can be performed at the data input clock rate. The encoder also contains 2048 bit registers (8 bits x 8 level interleave x 32 generated symbols). The input data, DI0-7, is framed by the INC input signal. As the data is input into the chip, it is presented to the check symbol generator and also passed directly to the

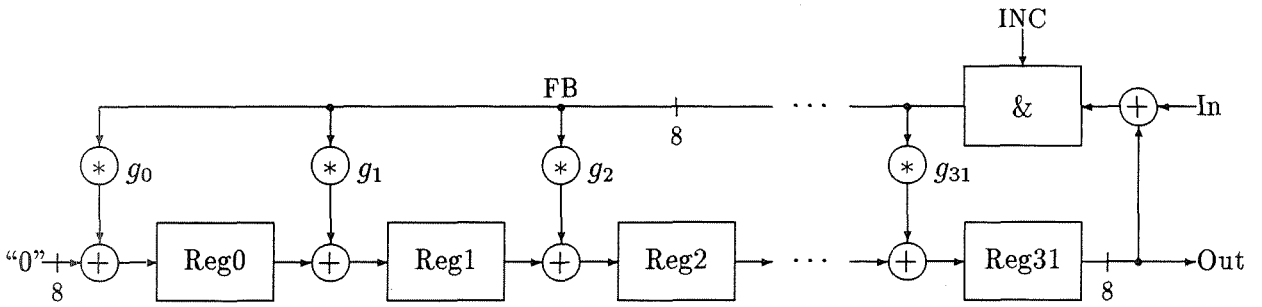

Figure 4: Check Symbol Generator Block Diagram.

output port DO0-7. At the end of the input data block, INC transitions low and the output of the check symbol generator passes out DO0-7. With INC low, 0's are input to the check symbol generator clearing out the registers. By the time that all of the check symbols have been clocked out of the encoder, all of the registers will be completely reset for the coding of the next block. Figure 4 shows a block diagram of the logic for the check symbol generator.

Each register is a 1 to 8 byte shift register, depending on the interleave depth set up during initialization. The 32 constant multiplier cells each multiply the 8-bit feedback value, FB, by a programmed constant, g_n. Each of these constant multipliers consists of an 8X8 XOR/ZERO cell array. A ZERO cell is simply defined as the absence of a XOR. The value of the constant, g_n, determines which array elements are XOR and which elements pass data unchanged (ZERO cell). The XOR/ZERO constant multipier array also performs the addition operation of the value from the previous register. An example of one of the 32 constant multiplier/addition cells is shown in Figure 5.

4.3 Design Evaluation Summary

The design was completed using Mentor Graphics IDEA version 7.1 and UTMC Mentor workstation toolkits. Test vector set fault grading was conducted using the Mentor QuickFault© tool. A total of 10100 nets were traversed during simulation with 98.58% toggled to both one and zero. All 143 untoggled nets are associated with unused JTAG circuitry included in the UTMC I/O pads. The projected fault detection is 99%.

The prototype parts where delivered on September 3, 1992. Heavy ion testing was conducted at Brookhaven National Laboratory's Single Event Upset Test Facility jointly by MRC and Goddard Space Flight Center personnel on December 3, 1992. The SEU Linear Energy Transfer threshold (LET_{th}) was found to be approximately 38 with the 10% threshold ($LET_{0.1}$) approximately 58. The test report concludes that the RS parts have Single Event Latchup (SEL) and SEU thresholds high enough to provide nearly zero probability for SEUs or SEL during extended mission lifetimes[2].

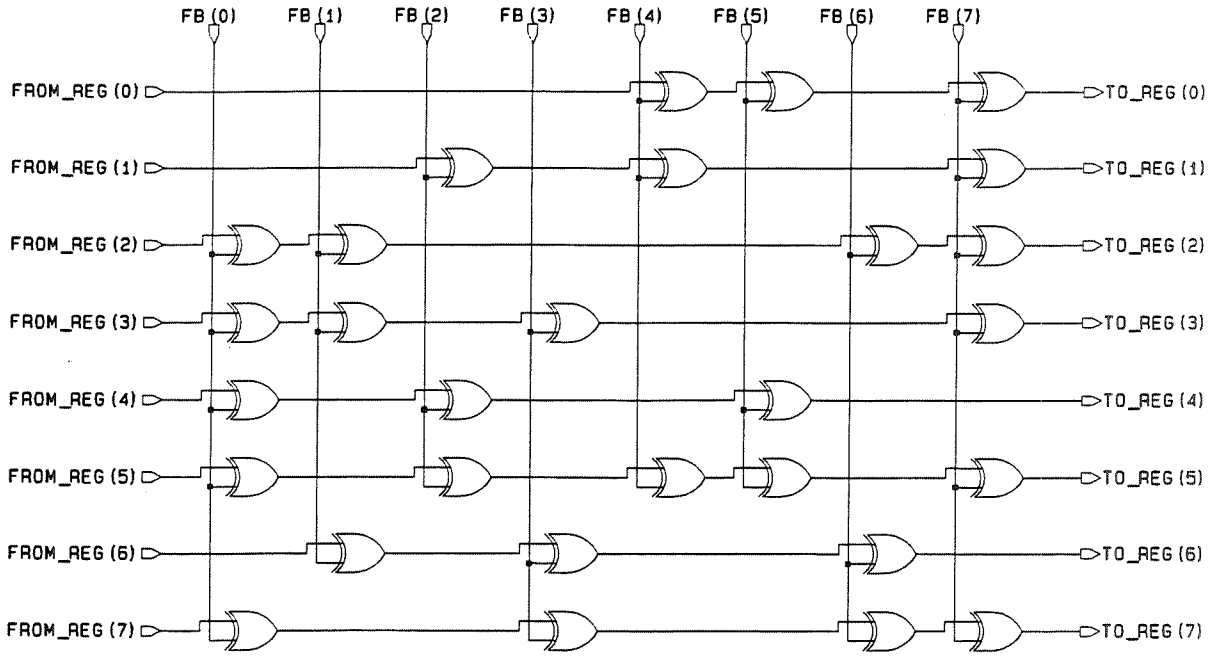

Figure 5: Constant Multiplier/Addition Cell.

5 Summary

A Reed-Solomon error correcting code encoder that meets the CCSDS recommendation for telemetry channel coding has been designed for the Goddard Space Flight Center. The chip was designed using the UTMC 1.2μ radiation-hardened gate-array technology and operates up to a 200Mbit/sec output data rate. The UTE-R process has been approved for the production of MIL-STD-883 Level S and JAN MIL-M-38510 Class S parts. Level B parts are also available, at reduced cost. In addition to meeting the CCSDS coding recommendation, the encoder includes shortened code and bypass mode operations that act to facilite clean interfacing of the chip to other system components. The chip has been baselined into flight hardware for the TRMM and XTE missions. The RS encoder chip is available from ICs as p/n RH-RS16-SE, (505) 277-9700.

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6 Key to Acronyms Used

CCSDS Consultative Committee For Space Data Systems.

CMOS Complementary Metal Oxide Silicon.

JAN Joint Army Navy.

JTAG Joint Test Action Group – IEEE 1149.1 Standard for boundry scan.

LET Linear Energy Transfer (MeV·cm^2/mg).

MRC Microelectronics Research Center

QFP Quad Flat Pack(age).

RS Reed-Solomon.

SEL Single Event Latchup.

SEU Single Event Upset.

TRMM Tropical Rainfall Measuring Mission.

UTE-R UTMC's 1.2-micron gate array technology.

UTMC United Technologies Microelectronics Center.

VLSI Very Large Scale Integration.

XTE X-Ray Timing Explorer.

References

[1] Consultative Committee for Space Data Systems. "Advanced Orbiting Systems, Networks and Data Links" (CCSDS 700.0-G-3), November 1992.

[2] K. A. LaBel *et.al.* "Heavy Ion Results for Electronic Devices". In Workshop Record of 1993 IEEE Radiation Effects Data Workshop.

[3] United Technologies Microelectronics Center. Radiation-hardened CMOS. Technical Description, April 1990.

[4] S. Whitaker and K. Liu. "A High Speed CCSDS Encoder for Space Applications". In *2nd NASA Symposium on VLSI Design*, pages 1.3.1–1.3.9, Moscow, Idaho, Novemeber 1990. NASA Space Engineering Research Center, University of Idaho.