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QPPM Receiver for Free-Space Laser Communications

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Abstract

A prototype receiver developed at NASA Lewis Research center for direct detection and demodulation of quaternary pulse position modulated (QPPM) optical carriers is described. The receiver enables dual-channel communications at 325-Megabits per second (Mbps) per channel. The optical components of the prototype receiver are briefly described. The electronic components, comprising the analog signal conditioning, slot clock recovery, matched filter and maximum likelihood data recovery circuits are described in more detail. A novel digital symbol clock recovery technique is presented as an alternative to conventional analog methods. Simulated link degradations including noise and pointing-error induced amplitude variations are applied. The bit-error-rate performance of the electronic portion of the prototype receiver under varying optical signal-to-noise power ratios is found to be within 1.5-dB of theory. Implementation of the receiver as a hybrid of analog and digital application specific integrated circuits is planned.

Introduction

Beginning in the early 1980's, NASA's Lewis Research Center (Lewis) has conducted a space communications technology development program for commercial applications of higher radio frequency (rf) bands such as Ka (20- to 30-GHz). Over the past three years, Lewis has also developed the electronics for high data rate applications of free-space communications using optical carriers. Laser communications offers the potential of significantly higher destination power flux density than rf communications in point-to-point free-space applications due to more precisely focused beams. If the system cost is competitive with rf solutions, direct detection of pulse modulated laser light may be used to link future constellations of tens or hundreds of commercial satellites in low Earth orbits. NASA relay satellites in geostationary orbits and deep-space planetary probes may also require the high capacity (over 1-Gbps) links that laser communications afford.

This paper describes the prototype receiver developed at Lewis for detection and demodulation of quaternary pulse position modulated (QPPM) signals. Under the high-speed laser integrated terminal electronics (Hi-LITE) project, Lewis has constructed a dual-channel QPPM transmitter and receiver operating at 325 Megabits per second (Mbps) per channel. Figure 1 shows a photograph of the Hi-LITE racks plus special test equipment.

The initial concept for the project including a description of the communications electronics and computer controlled special test and demonstration equipment was reported in an earlier paper[1]. Since that time, several changes have been made to the functional designs and implementation approaches. This paper reviews the final optical, analog, and digital hardware implementation of the prototype receiver and summarizes its performance. A companion paper[2] reviews the prototype transmitter, and discusses the implementation and testing issues encountered during its development. A future paper will describe the capabilities of the automated special test equipment and present final test results for a wide range of simulated operating conditions.

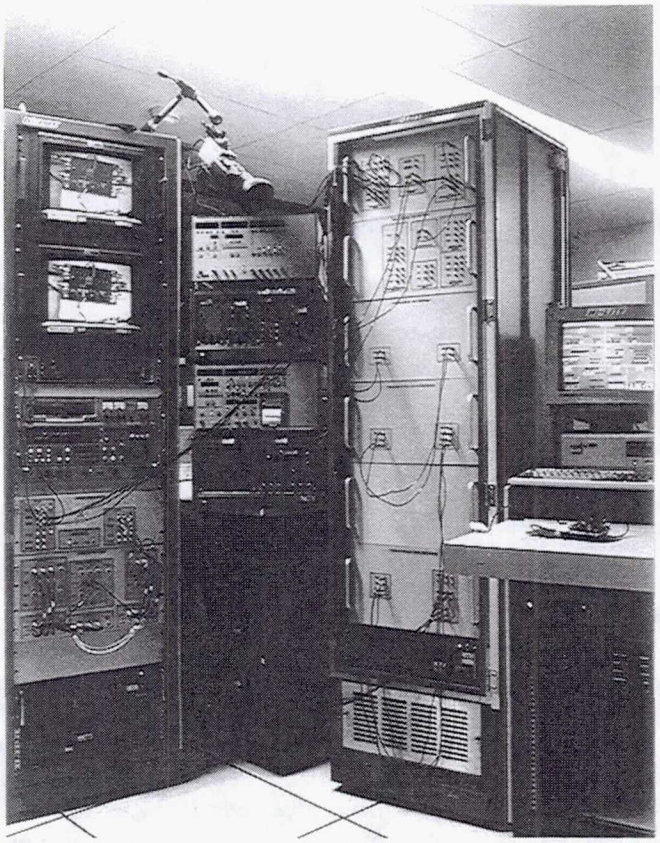

Figure 1.-- Hi-LITE system. (left to right: video rack, special test equipment, electronics, and computer).

In the following sections of this paper, individual subsystems of the prototype receiver are discussed. Figure 2 shows a functional block diagram of the entire receiver. The optical receiver, including the avalanche photodiode (APD) and preamplifier, is presented first. Next, the receiver's front-end analog electronics, including signal conditioning, slot clock recovery, matched filter data recovery, and maximum likelihood detection are discussed. Then, the digital electronics for symbol clock recovery and data decoding and demultiplexing are described. Some test results are presented for the prototype receiver operating under both an rf and optical simulation of actual intersatellite links. The paper concludes with a statement of future plans for the project.

Quaternary Pulse Position Modulation

Recall that QPPM is one of a family of M-ary pulse position modulation formats, where $k=\log_2 M$ bits of information are conveyed in each symbol. In QPPM, $M=4$, and therefore $k=2$ bits per symbol.

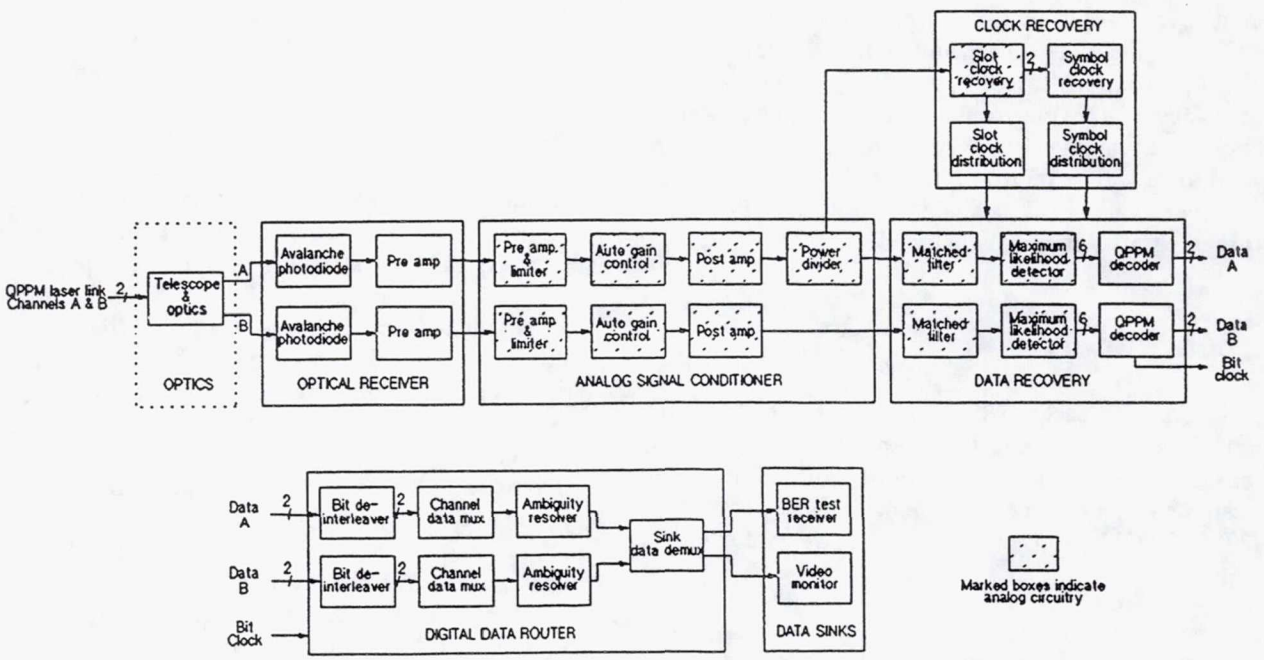

Figure 2.--Block diagram of Hi-LITE dual-channel QPPM receiver.

Figure 3 shows the mapping of each group of two information bits into one of the four possible QPPM symbols used in Hi-LITE.

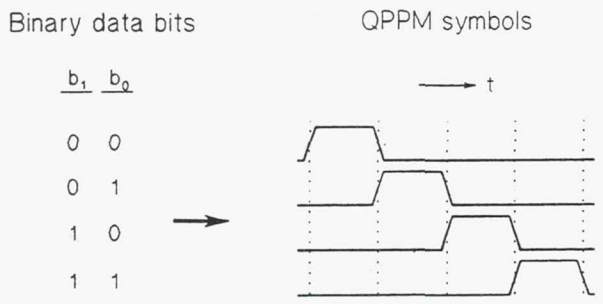

Figure 3.--Encoding binary data into QPPM symbols.

A maximum of 650-Mbps of source data are demultiplexed onto two channels at 325-Mbps each. The timing for binary information bits and QPPM symbols along with their synchronized clocks is shown in figure 4.

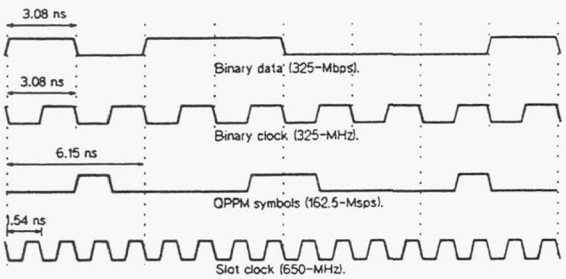

Figure 4.--Timing relationship of binary source data, QPPM, and clocks.

Optical Receiver

In an actual intersatellite link, two 325-Mbps QPPM encoded laser beams (A and B) would impinge on a telescope and then be directed to the optical receiver. In the laboratory configuration at Lewis, the space link, the telescope, and associated optics are replaced by optical special test equipment (STE) whose main component is a variable density optical filter. Only one channel (one laser beam) is simulated with this STE. Figure 5 shows a photograph of the optical STE rack, designed and fabricated by NASA Goddard Space Flight Center. The optics, including the laser, filter, and APD are located in the top portion of the rack. The primary function of the optical receiver is to convert the detected modulated laser beam to an electrical waveform using the APD.

The beams, each in the 810-830 nm wavelength range, are separated by at least 10 nm. The APD is sensitive to a relatively large range of wavelengths, so an interference filter with a passband centered at the laser frequency is inserted to prevent optical channel crosstalk. The filter also blocks laser noise emission and broadband background solar and stellar radiation in an operational system. Following the filter is a focusing lens, used to concentrate the incident laser beam upon a detector area of about 3×10^{-4} cm^2.

The development of high speed, high sensitivity APD's is critical for free-space laser links. For optimum performance, a state-of-the-art hybrid package, combining a high-sensitivity APD and a preamplifier is required. One such package is a 900-MHz, 128 amp/watt optical receiver made by EG&G for NASA Goddard Space Flight Center.

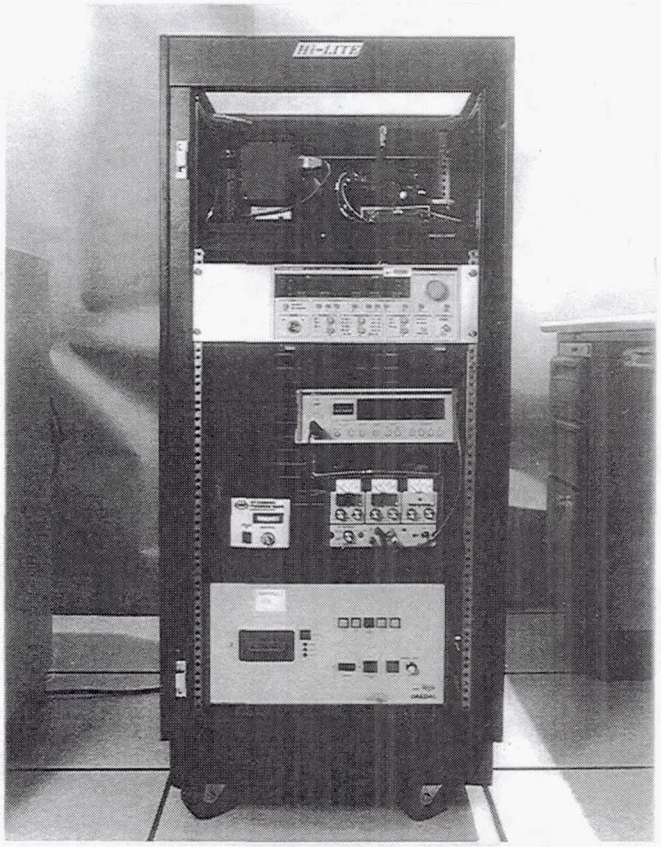

Figure 5.--Optical special test equipment rack.

A Newport model 877 APD having a greater bandwidth (1.7-GHz) but less sensitivity (0.2 amp/watt) than the EG&G unit was available for use in the Hi-LITE project. This APD was coupled to a 2.0-dB noise figure preamplifier to increase the signal amplitude.

Analog Circuits

In a satellite link, the low level signals out of the optical receiver exhibit link degradations including pointing-error induced amplitude variations (with an expected dynamic range of 35-dB at up to 1-KHz), noise, and timing jitter. These signals are not suitable for digital processing at standard logic levels, and must therefore be conditioned by analog circuitry, indicated by the marked boxes in figure 2, and shown in greater detail in figure 6. The analog signal conditioning circuitry compensates for degradations and rapid power fluctuations in the received signal using amplifiers, automatic gain control (AGC), and filters to provide uniform level outputs to be used by the clock and data recovery circuits that follow.

The first element of the analog signal conditioner is a limiting amplifier to protect vulnerable components from damage due to excessive voltage (up to 4-volts). The normal operating input signal range is from 1 to 100-mv. In addition, the limiting amplifier has a low noise figure (2.8-dB), which greatly influences the 4.5-dB noise figure of the entire signal conditioner subsystem. The attenuator ensures that the signal feeding the AGC circuit stays within prescribed limits.

The AGC circuit consists of a variable gain control (VGC) amplifier having a dynamic range of 35-dB and a 3-dB bandwidth from 100-KHz to 2.5-GHz. A low-pass filter attenuating unwanted high frequency noise feeds a power divider. One output of the divider goes to a detector producing a feedback signal to be amplified and filtered by two operational amplifier circuits, resulting in a 0- to -5-volt control input to the VGC amplifier.

The other output of the power divider is routed through two linear amplifiers to compensate for signal splitting losses, then further divided (three ways) to provide signals for slot clock and data recovery and a test output. At this point in the circuit the binary waveform amplitude is fairly constant at a nominal level of 0.5-volts peak-to-peak.

Slot clock recovery is obtained with a Broadcast Communications Products (BCP) model 50-b bit-synchronizer module. It generates a slot clock (650-MHz) and a synchronized digital logic level representation of the QPPM waveform obtained by straightforward threshold comparison. This first-order approximation of the transmitted waveform is used by subsequent circuitry to recover symbol clock timing (discussed in the digital circuits section), but not for final data recovery.

Only one bit synchronizer module (on channel A) is required as long as the timing skew between channels A and B can be maintained within one-half of one slot period (+/-769-ps). The clock is then buffered and distributed to be used by both channels throughout the receiver.

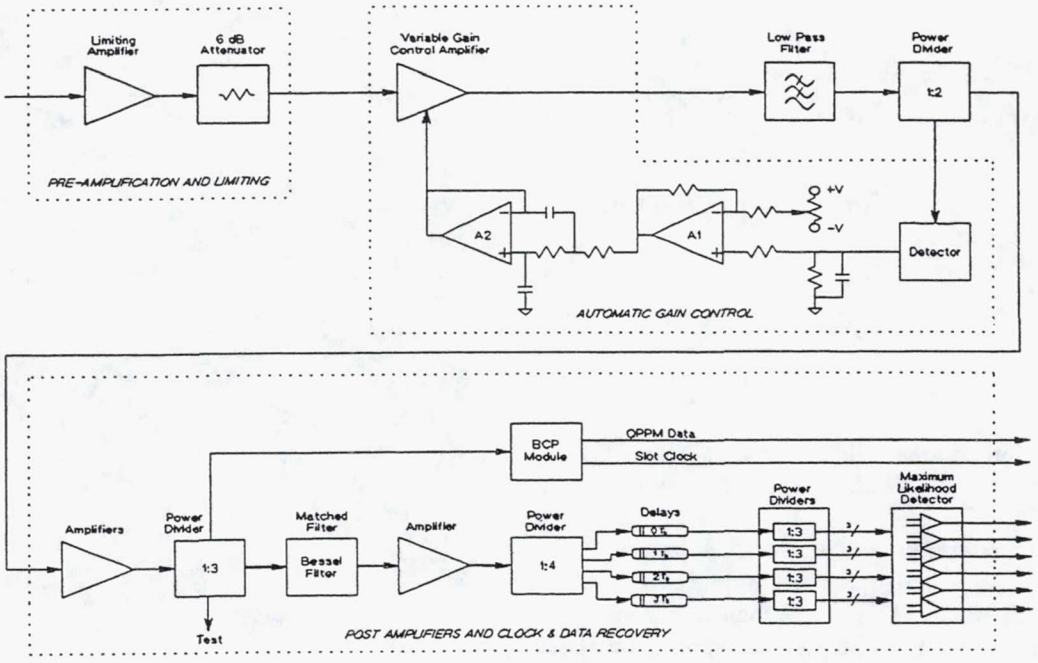

Figure 6.--Analog electronics subsystem.

Alternate methods of data recovery were investigated and implemented to enhance the performance of those reported in an earlier paper[1]. As shown in figure 6, an output of the 3-way power divider is used to feed a matched filter and other components of the data recovery circuit. For the matched filter, three versions of 4-tap delay line integrators and low pass filters were implemented, using analog delay lines, coaxial delay modules, and microstrip circuits. Each was physically large and worked better with ideal rectangular pulses than the more trapezoidal pulses obtained in the actual system. An alternative matched filter consists of a 7th order Bessel low-pass filter that approximates a raised cosine response rather than a triangular output waveform that would be produced by an ideal matched filter with rectangular input pulses. This approximation has been shown by Sun[4] to be a practical alternative to an ideal matched filter when using components with limited electrical bandwidth.

In theory, the ideal matched filter gives optimal BER performance since it gives maximum signal-to-noise ratio (SNR) at its output when the input PPM pulse shape is rectangular. However, the matched filter is not the optimal filter for non-rectangular PPM pulse shapes created by lasers and electronics with less than infinite bandwidth and degraded by non-additive white Gaussian noise (AWGN). The bandwidth of the laser, APD, preamplifier, and all electronics prior to the matched filter must be greater than $2/\tau_s$ (where τ_s is one PPM slot) to obtain an ideal triangular matched filter response. By using a raised cosine filter, the bandwidth requirements of the laser APD preamplifier and electronics can be reduced by nearly half (about $1/\tau_s$) while the BER is still very nearly the same as that using a matched filter. A low-pass Bessel filter of seventh-order, with a 3-dB cutoff frequency of 845-MHz, approximates the desired equalizer output. Figure 7 shows the effect of the analog signal conditioning circuits, including the matched filter, on an input signal of 8-dB E_b/N_o with 12-dB 1000-Hz amplitude variation. The significantly improved signal is suitable for input to the digital receiver circuits. However, the contribution of the matched filter alone was found to be negligible mainly due to bandwidth limitations of upstream components.

A four-way splitter at the matched filter output is used to delay successive outputs by QPPM slot period increments (0, τ_s, $2\tau_s$, and $3\tau_s$). These delay lines are amplitude equalized to compensate for unequal insertion losses. Each delay line output is further split three ways, producing twelve signals. The twelve signals are fed into six comparators to produce six ECL-level output signals for the QPPM decoder circuitry. The six outputs of the maximum likelihood detector represent the six combinations of comparing the energies of the slots two at a time. Each six-way comparison is latched once per slot clock period precisely when the matched filter output is at its maximum. However, only one out of every four sets of comparisons represents a valid 4-slot QPPM symbol. The task of determining the correct phase to establish the proper symbol boundaries is performed by the symbol clock recovery circuit, described in the following section.

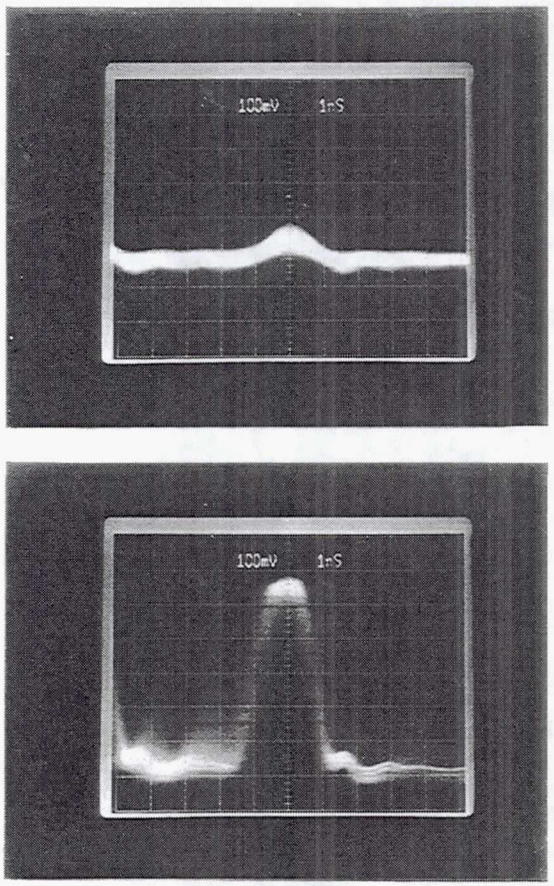

Figure 7.--Analog signal conditioning waveforms: (top) input signal, (bottom) amplified matched filter output.

Digital circuits

The digital circuitry is represented by the non-shaded boxes within the clock recovery, data recovery, and digital data router sections shown in figure 2. The circuits are implemented with the Picologic family of GaAs logic from TriQuint Semiconductor (formerly GigaBit Logic). Figure 8 shows a typical digital prototype board. The leadless IC packages along with surface-mount components are mounted on special four layer prototype boards that accommodate eight Picologic IC's and eight 0.4" wide 24-pin components such as ECL integrated circuits. Picologic is compatible with the 100K ECL family using similar logic levels (-0.7 volt logic high and -1.8 volt logic low). Typical propagation delay times are on the order of 400-ps. On-board signal interconnections between chip sites are made

using semi-rigid micro coaxial cable, and inter-board signals use RG-174/U coaxial cable via SMA connectors. All signals are terminated to -2 volts through 50 ohm surface-mount resistors. Extreme care had to be taken in the design and layout to account for signal propagation times due to delays internal to the IC's and the interconnect cables (50-ps per centimeter). These delays become very significant at 650-MHz, where the clock period is only 1,538 ps. References 1 and 2 describe the hardware implementation in greater detail.

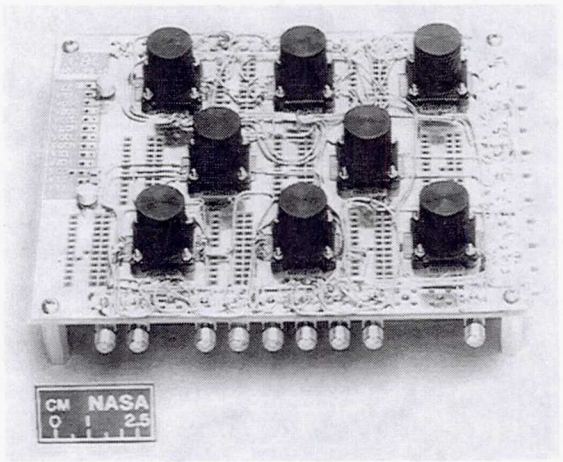

Figure 8.--Typical digital circuit board.

As previously indicated in the analog circuits section, a simple threshold comparitor in the BCP bit synchronizer module provides a first order approximation of the QPPM waveform at ECL logic levels, suitable for the symbol clock recovery circuit. The function of this circuit is to determine where to partition the 1's and 0's of the recovered data stream into groups of valid four-bit QPPM symbols. Specifically, it assigns the correct one of the four possible phases to the 162.5-MHz symbol clock. A "valid/invalid" test is applied using combinational logic to the binary waveform over a sliding window of the last four received time slots. To be valid, a QPPM symbol must contain only a single logic "one" and three logic "zeros". Each time an invalid symbol is detected, one of four counters corresponding to that specific symbol timing is incremented. When any one of the counters reaches a limit (14 is used in the prototype), the other three are surveyed to determine if one and only one of them has detected no invalid QPPM symbols. If so, the symbol clock is set to the phase represented by the counter registering zero. If two or more counters show that no invalid symbols were detected, arbitration is imposed with the following priorities: (1) keep the present phase, (2) shift the phase by $+90^{\circ}$, (3) shift by -90°, and (4) shift by 180°. At this point, the counters are reset and the process begins anew, regardless of whether or not a symbol clock adjustment was made.

The counter limit of 14 is a compromise between hardware constraints and the probability of timing error as predicted by a computer model simulation. The arbitration rationale recognizes that an absence of any slot clock shift is the most probable occurrence, and one clock shift is more probable than two over a given test period. Once symbol clock timing is established, the recovery circuit can be disabled until needed (for example, if major slot clock timing errors are detected). This scheme relies on varying source data that produces a distribution of "ones" and "zeros", resulting in approximately the same probability of occurrence of the four possible QPPM symbols. A cycle slip in the slot clock recovery will cause a shift in the symbol clock, resulting in invalid symbol timing until the symbol clock recovery circuit re-establishes the correct timing.

Once generated, both slot and symbol clocks are buffered and distributed to various components of the receiver electronics. The 162.5-MHz symbol clock is used to latch the six maximum likelihood comparitor outputs for both channels at the proper sampling instant. Each latched set can then be decoded into the two binary data bits represented by the recovered QPPM symbol. These two channels of two-bit binary signals are the outputs of the data recovery portion of the receiver.

The binary data channels enter the digital data router to be de-interleaved if required, combined, and converted to serial data. De-interleaving is necessary if the transmitter[2] is configured to interleave the data. The purpose of interleaving is to infer the bit error rate (BER) of signals on one optical channel that are not pseudo random bit sequence (PRBS) data (such as video) from the BER measured on the channel carrying PRBS data. The assumption is that the interleaved non-PRBS data undergoes the same path degradations and interference as the PRBS data. In this way a quantitative estimation can be made on the non-PRBS transmission and compared to a qualitative evaluation. De-interleaving is accomplished by swapping the low-order bits of the output buses.

The two-bit signals from each channel are next combined into single 325-Mbps data streams in the channel data multiplexers. Since the system uses no frames, unique words, nor headers, there is no direct way to discern one channel from the other if they were once interleaved. However, this two-way ambiguity can be resolved indirectly by monitoring the BER measurement. The channel carrying PRBS data should exhibit a BER several orders of magnitude below 0.5, while the non-PRBS channel's BER will be very close to 0.5. Once channel ambiguity is resolved, the process need not be repeated as long as the data transmission is uninterrupted.

The final process of digital data routing is for the sink data

multiplexer to combine the two binary data channels into a single 650-Mbps data stream or keep the two 325-Mbps data streams separate, depending on the data sinks in the particular experiment. All three outputs (650-Mbps data and two channels of 325-Mbps data) are available on SMA connectors as complimentary pairs. In addition, all are accompanied by an appropriate clock and its compliment.

Figure 9 shows the digital electronics chassis. To minimize board-to-board interconnection cable lengths, some analog circuit boards are included.

Figure 9.--Digital electronics chassis.

Testing and Results

The receiver was tested using the fully integrated Hi-LITE system, including the QPPM transmitter with laser, special test equipment (optical and rf analog), the QPPM receiver with an APD and preamplifier, data sources and sinks, and a control and monitoring computer. Figure 10 shows a block diagram of the system test configuration. Link degradations in the optical path between the QPPM transmitter and receiver were simulated by both analog and optical STE. Preliminary testing and system debugging was performed using the analog STE consisting of an additive white Gaussian noise (AWGN) generator, an rf mixer, filters, and attenuators. Figure 11 shows a photo of the analog STE chassis. Once the electronic components of the system proved to work satisfactorily, testing through the optical STE with a laser and APD commenced.

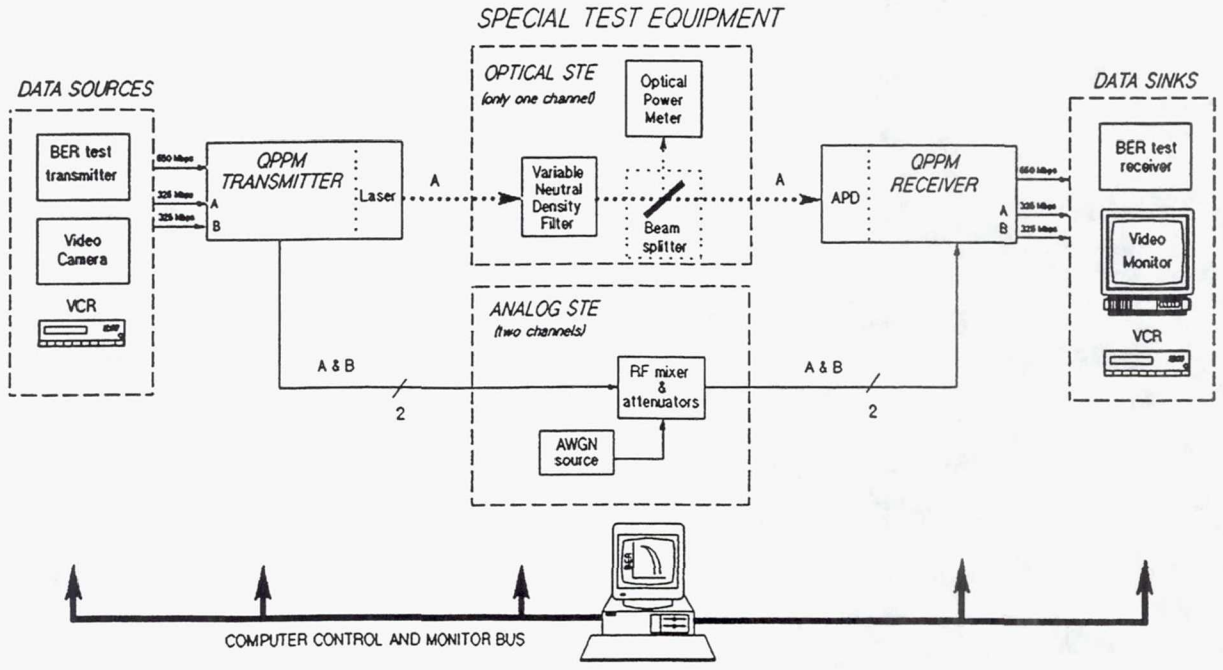

Figure 10.--System test configuration block diagram.

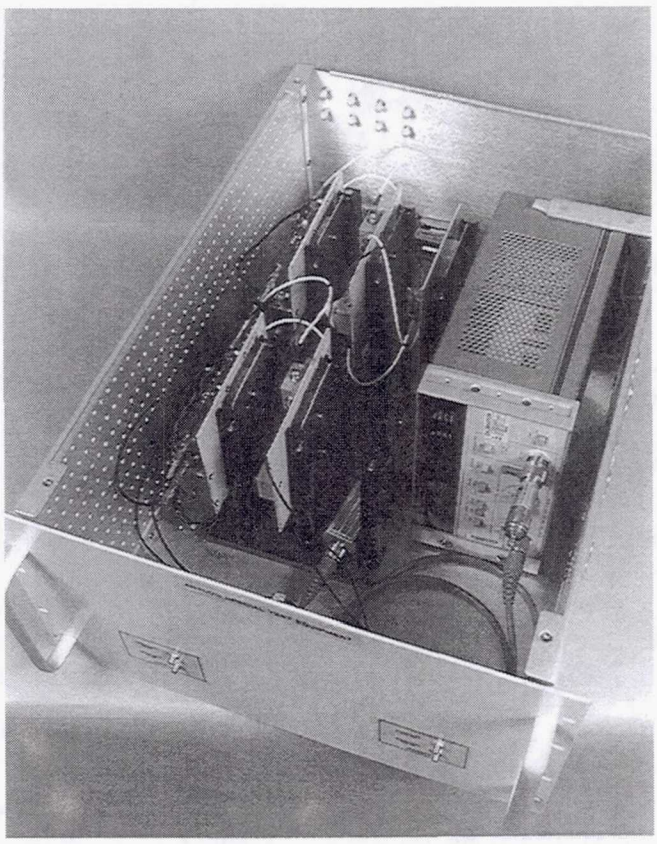

Figure 11.--Analog special test equipment chassis.

The optical STE includes a variable neutral-density optical filter, followed by a beam splitter which feeds both an optical power meter for power measurements, and the APD. Figure 12 shows a photograph of the optical link components, including: laser, variable neutral-density filter, fixed attenuation filters, mirrors, beam splitter, power meter sensor, focusing lens, and the APD.

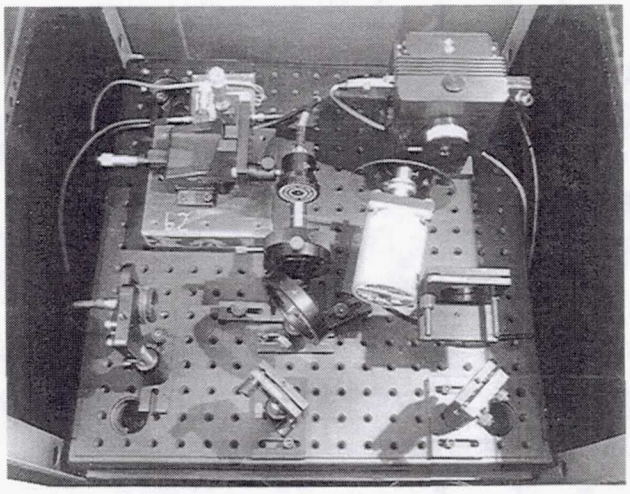

Figure 12.--Optical special test equipment.

A camera and video cassette recorder (VCR) provide live or recorded studio-quality video data at 325-Mbps through a custom digital interface[1] to be displayed by a video monitor or recorded on a VCR. For quantitative performance measurements, a commercial BER test set transmitter and receiver pair provide pseudorandom bit sequences up to 2^{23}-1 bits in length.

A 386SX personal computer is used for automated testing. It interfaces to the system hardware over digital and analog control lines and to the commercial equipment via an IEEE-488 general purpose interface bus. A typical test involves incremental rotation of the neutral density filter using its stepper motor controller to simulate specific signal-to-noise power conditions, taking optical power and BER measurements, and storing the data on disk. The computer has a graphical user interface enabling automated or manual system testing and configuring. Figure 13 shows a typical computer control screen.

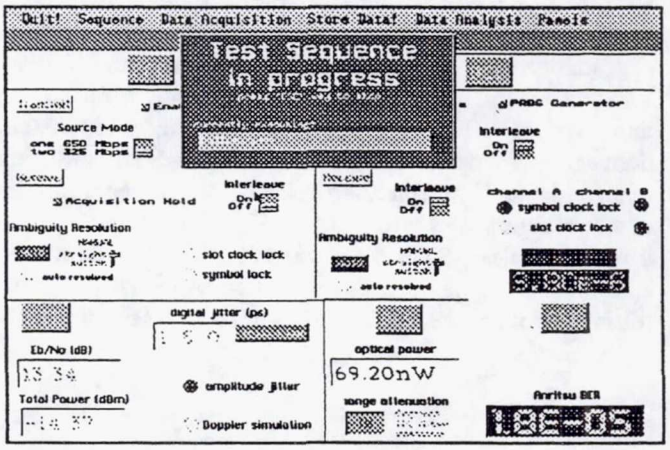

Figure 13.--Computer control and monitor screen.

In the analog STE test configuration, AWGN is controlled by a variable attenuator and imposed on the signal by means of an rf mixer. Test results for the QPPM system using analog link simulation are very close to theoretical predictions. Figure 14 shows plots of the measured BER versus E_b/N_o as compared to the theoretical limit for orthogonal signaling[7]. The receiver performance is less than 1-dB from optimum for high BER and within 2-dB for lower BER. Causes of this slight degradation from optimum include: non-ideal pulse shapes coming from the QPPM transmitter, slot clock recovery jitter, and other circuit implementation losses in the receiver hardware.

Degraded performance due to slot clock recovery jitter can be clearly seen in Figure 14, where the measured BER versus E_b/N_o data is also compared to performance with a hardwired clock directly from the transmitter. The BCP module used for slot clock recovery is a commercial unit designed for fiber optic applications, not intended for use

below about 21-dB E_b/N_o. Not surprisingly, it starts slipping clock cycles at an E_b/N_o of around 12-dB. When a slot clock cycle slip occurs the symbol timing becomes incorrect and remains so until the receiver re-acquires proper timing. The slot clock recovery performance was improved by cascading the BCP module with a clock recovery circuit from Hewlett-Packard (HDMP-2501). Adding some custom signal conditioning circuitry enabled the system to operate down to nearly 8-dB E_b/N_o with much improved performance. A flight system receiver would require a more stable phased locked loop, custom designed to operate at low E_b/N_o levels.

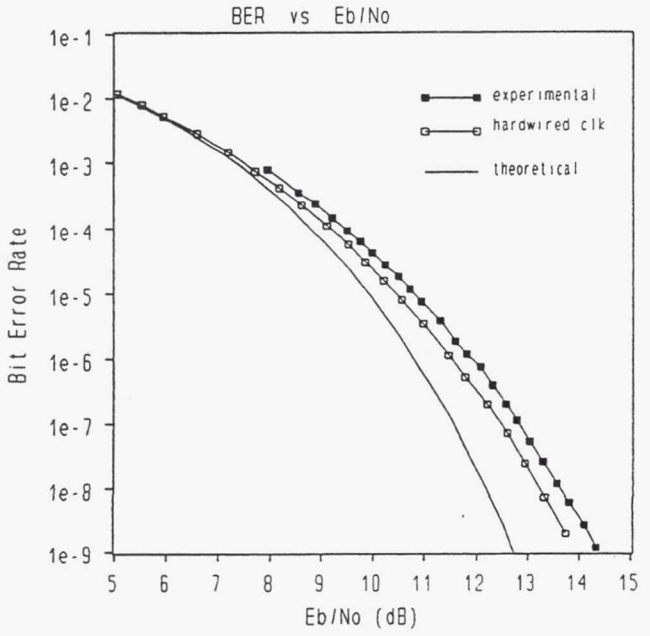

Figure 14.--Analog STE configuration results comparing theory to experimental data with and without hardwired slot clocks.

Test results using the optical STE are shown in Figure 15. A plot of BER versus average received photons per bit is compared to the theoretical optimum for the APD[6]. Optimizing the APD bias set point for the lowest BER fixed the APD gain at 100, though a gain of 200 is theoretically optimal for the APD alone[6]. The theoretical curve does not take into account the implementation loss of the receiver electronics, as shown in figure 14. Experimental data shown are from hardwired clock tests, allowing operation at higher BER without experiencing slot clock cycle slips due to poor clock recovery circuit performance at low photon per bit levels. As discussed previously under analog STE testing, slot clock recovery circuit cycle slips begin at around 500 photons per bit, and performance is degraded from hardwired clock operation by about 40 photons per bit. The photons per bit values were calculated from the received average optical power measurement using the following equation[5]:

$$\frac{photons}{bit} = \frac{\eta P_{ave} T_{sym}}{2hf(1+3/R_e)}$$

where η is 0.77, the quantum efficiency of the APD (dimensionless), P_{ave} is the average optical power in watts, T_{sym} is the symbol period for 162.5-Megasymbols/second, hf is the photon energy at the laser frequency f (h is Plank's constant, 6.626×10^{-34} J-s, f = $c\lambda$, where c = 3×10^8 m/s and λ = 830-nm), and R_e is the laser extinction ratio factor (dimensionless) estimated at 20. The $(1 + 3/R_e)$ term comes from the finite extinction ratio of a QPPM modulated laser. The 3 "off" slots per QPPM symbol actually contribute to some of the measured average power. The factor of 2 in the denominator accounts for one QPPM symbol representing two binary bits.

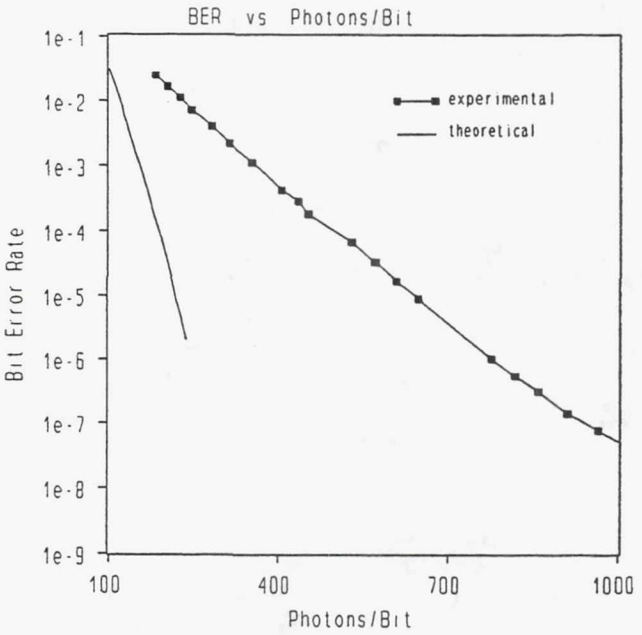

Figure 15.--Optical STE configuration results comparing theory to experimental data.

The high number of photons per bit in figure 15 is due primarily to the relatively low sensitivity of the Newport APD. With the state-of-the-art hybrid APD and preamplifier developed by EG&G, the receiver is expected to operate below 100 photons per bit at 10^{-6} BER[3]. Also, a laser with a bandwidth of only 500-MHz was used instead of the required 650-MHz. This causes additional degradation from the theoretical curve. The lower laser bandwidth increases the pulse rise and fall times, degrading performance through increased intersymbol interference. Finally, implementation loss in the electronics, as measured with the analog STE, also contributes to the deviation from

theory. A plot of the data in decibels relative to one photon (Figure 16) shows the total system implementation loss of about 5-dB: 1.5-dB of it due to the electronics and 3.5-dB from the laser, optics and APD.

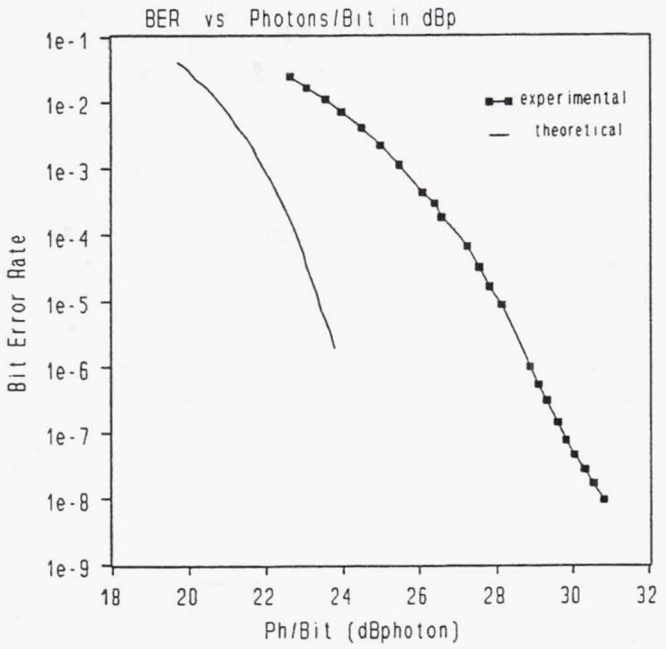

Figure 16.--Optical STE configuration results comparing theory to experimental data on a dB scale relative to one photon.

Plans and Conclusions

A single digital application specific integrated circuit (ASIC) has been designed by Lewis to replace all of the digital boards included in both the prototype receiver and transmitter. It has not yet been fabricated. A hybrid version of the analog electronics could be developed to compliment the digital ASIC in size. The resulting demonstration model would be representative of the form, fit, and functionality required for commercial and NASA mission applications.

Potential enhancements to the prototype system include a wider bandwidth laser, a more sensitive APD, a wider bandwidth low-noise amplifer, and an improved slot clock recovery scheme. The prototype optical communications receiver will be used at Lewis to compare rf and optical intersatellite link performance in greater detail. The effect of platform jitter, pointing errors, and Doppler frequency shifting will be assessed using some additional STE described in an earlier paper[1]. The prototype QPPM receiver developed under the Hi-LITE project has demonstrated the viability of multichannel direct detection laser communications at 325-Mbps per channel.

References

1. Budinger, J.M., et.al., "Quaternary Pulse Position Modulation Electronics for Free-Space Laser Communications," NASA Technical Memorandum 104502, AIAA-91-3471, AIAA/NASA/OAI Conference on Advanced SEI Technologies, Cleveland, Ohio, Sept 4-6, 1991.

2. Soni, N.J., and Lizanich, P.J., "Integration and Test of QPPM Transmitter for Free-space Laser Communications," 15th AIAA International Communications Satellite Systems Conference, San Diego, CA, February 28 - March 3, 1994.

3. NASA Space Communications Symposium, pp. 5A-6, hosted by NASA Lewis Research Center, Space Electronics Division, Cleveland, Ohio, Oct. 20-21, 1992.

4. Davidson, F.M., and Sun, X., "Direct Detection Optical Communication Receiver Performance With PPM Signaling and Raised Cosine Filtering," July 9, 1990.

5. Sun, X., Davidson, F., and Field, C., "50-Mbps Free Space Direct Detection Laser Diode Optical Communications System With Q=4 PPM Signaling," SPIE Vol. 1218 Free-Space Laser Communications Technologies II, 1990.

6. Davidson, F., Sun, X., "Reduced Electronic Bandwidth Receivers for Direct Detection 4-ary PPM Optical Communications Intersatellite Links," NASA Grant NAG5-1510, 1993.

7. Sklar, B., "Digital Communications," p. 177, Prentice Hall, 1988.

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13. ABSTRACT ***(Maximum 200 words)***

A prototype receiver developed at NASA Lewis Research center for direct detection and demodulation of quaternary pulse position modulated (QPPM) optical carriers is described. The receiver enables dual-channel communications at 325-Megabits per second (Mbps) per channel. The optical components of the prototype receiver are briefly described. The electronic components, comprising the analog signal conditioning, slot clock recovery, matched filter and maximum likelihood data recovery circuits are described in more detail. A novel digital symbol clock recovery technique is presented as an alternative to conventional analog methods. Simulated link degradations including noise and pointing-error induced amplitude variations are applied. The bit-error-rate performance of the electronic portion of the prototype receiver under varying optical signal-to-noise power ratios is found to be within 1.5-dB of theory. Implementation of the receiver as a hybrid of analog and digital application specific integrated circuits is planned.

14. SUBJECT TERMS
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