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SPACE STATION FREEDOM (SSF) DATA MANAGEMENT SYSTEM (DMS) PERFORMANCE MODEL DATA BASE

November 1993

John R. Stovall

Prepared by:

Lockheed Engineering & Sciences Company
Houston, Texas

Job Order 60-911
Contract NAS 9-17900

for

FLIGHT DATA SYSTEMS DIVISION
JOHNSON SPACE CENTER

LESC-30966

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DOCUMENT CHANGE RECORD

The following table summarizes the change activity associated with this document.

ISSUE AND DATE	PAGE NO.	CHANGE SUMMARY	SECTION

PAGE ii INTENTIONALLY BLANK

CONTENTS

Section		Page

APPENDICES **Page**

TABLES

Table **Page**

FIGURES

ACRONYMS

0-FT	0-Fault tolerant
1-FT	1-Fault tolerant
2-FT	2-Fault tolerant
ACD	Architecture Control Document
ACRV	Assured Crew Rescue Vehicle
ACS	Assembly Contingency Sub-System
ACSS	Atmospheric Control & Supply Subsystem
ADCS	Attitude Determination Control System
AL/EVAS	Airlock Extra Vehicle Activity System
ANSI	American National Standards Institute
API	Applications Programing Interface
APM	Attached Payload Module
APP	Application
APPL	Application
ARC	Ames Research Center
ARS	Air Revitalization System
ASRM	Advanced Solid Rocket Motor
AUX	Auxiliary
BC	Bus Controller
BCU	Bus Control Unit
BDT	Binary Data Transfer
BIA	Bus Interface Adaptor
BIT	Built-In-Test
BITE	Built-In Test Equipment
BIU	Bus Interface Unit
BSP	Baseband Signal Processor
C&T	Communications and Tracking
C&T-ACS	Communication and Tracking - Assembly Contingency Subsystem
C&T-IAV	Communications and Tracking - Internal Audio and Video
C&T-SGS	Communications and Tracking - Space to Ground Subsystem
C&T-UHF	Communications and Tracking - Ultra High Frequency
C&W	Caution and Warning
CDR	Critical Design Review
CEI	Contract End Item

CETA	Crew and Equipment Translation Assembly
CHeCS	Crew Health Care System
CM	Configuration Management
CMG	Control Moment Gyro
CNTL	Control
CPU	Central Processing Unit
CSA	Canadian Space Agency
CSCI	Computer Software Configuration Items
CSDL	Charles Stark Draper Laboratory (MIT)
CW	Command Word
DMA	Direct Memory Access
DMS	Data Management System
DRAM	Dynamic Random Access Memory
DSAR	Data Storage and Retrieval
DW	Data Word
EATCS	External Active Thermal Control System
ECLSS	Environmental Control and Life Support System
EDAC	Error Detection and Correction
EDP	Embedded Data Processor
EEPROM	Electronically Erasable Programmable Read Only Memory
ELM	Equipment Logistics Module
EMU	External Maneuvering Unit
EPROM	Erasable Programmable Read Only Memory
EPS	Electrical Power System
ES	Equipment Section
ESA	European Space Agency
ETCS	External Thermal Control System
FDDI	Fiber Distributed Data Interface
FDIR	Fault Detection, Isolation and Recovery
FDS	Fire Detection & Suppression
FDSD	Flight Data Systems Division
FEL	First Element Launch
FEU	Functional Equivalent Unit
FLOPS	Floating Point Operations per second
FRR	Flight Readiness Review

G&N	Guidance and Navigation
GCA	Gas Conditioning Assembly
GN&C	Guidance, Navigation and Control
GNCPM	GN&C Propulsion Manager
GW	Gateway
HAB	Habitation
HRFM	High Rate Frame Multiplexer
HRM	High Rate Multiplexer
HRS	Heat Rejection Subsystem
IL	Inner Loop
I/O	Input/Output
IMG	Inter-Message Gap
INFO	Information
INSTR	Instruction
INT	Integrated
IOCC	Input/Output Card Controller
IODB	Input Output Data Base
IPL	Initial Program Load
iPSB	Intel Multibus II Parallel System Bus
IRGW	Intermediate Rate Gateway
ISA	Instruction Set Architecture, Inertial Sensor Assembly
IISA	Instruction Set Architecture
ISE	Integrated Station Executive/Software
ISO	International Standards Organization
ITCS	Internal Thermal Control System
ITS	Integrated Truss Segment
ITVE	Integrated Test and Verification Environment
JEM	Japanese Experiment Module
JSC	Johnson Space Center
Kbps	Kilo bits per second
Kbytes	Kilo-bytes
KIPS	Kilo Instructions per second
LB	Local Bus
LESC	Lockheed Engineering & Sciences Company
LLC	Logical Link Control
LNS	Lab Nitrogen System

MAC	Media Access Control
MAN SYS	Manual Systems
MB	Mission Build
MBCU	Main Bus Controller Unit
MBII	Multibus II
Mbps	Megabits per second
MBS	Mobile Base System
MDM	Multiplexer-DeMultiplexer
MDSSC	McDonnell Douglas Space Systems Company
MEM	Memory
MGMT	Management
MIPS	Millions of Instructions per second
MMD	Mobile Service Center Maintenance Depot
MODB	Master Object Data Base
MPAC	Multipurpose Application Console
MPC	Message Passing Coprocessor
MRS	Mobile Remote Servicer
MS	Manipulator Subsystem
ms	milliseconds
MSD	Mass Storage Device
msec	Millsecond (one thousandth of a second)
MSS	Mission Support System, Mobile Servicing System
MSU	Mass Storage Unit
MT	Mobile Transporter
MTC	Man Tended Configuration
MWS	Mixed Waste Gas Subsystem
NASA	National Aeronautics and Space Administration
NIA	Network Interface Adapter
NIU	Network Interface Unit
NOS	Network Operating System
OBCO	Onboard Check Out (Instrumentation)
OH	Overhead
OL	Outer Loop
OPS	Operations Planning System
ORU	Orbital Replaceable Unit
OS	Operating System

OSI	Open System Interconnect
OTDB	Outboard
P/L	Payload
PDR	Preliminary Design Review
PLM	Payload Logistics Module
PMA	Pressurized Mating Adaptor
PMC	Permanent Manned Configuration
PPM	Primary Propulsion Module
PROM	Programmable Read-Only Memory
PROP	Propulsion
PS	Payload Support
PTCS	Passive Thermal Control System
PTS	Precision Time System
PVCU	Photo Voltaic Converter Unit
RAD	Radiator
RAM	Random Access Memory
RC	Ring Concentrator
RJ	Rotary Joint
RJS	Rotary Joint System
RODB	Remote Object Data Base
RT	Remote Terminal
RTE	Run Time Environment
S&M	Structures and Mechanical
SARJ	Solar Array Rotary Joint
SCSI	Small Computer Systems Interface
SDP	Standard Data Processor
SEPS	Secondary Electrical Power System
SGS	Space-to-Ground Subsystem
SLOC	Source Line of Code, Standard Line of Code
SLOCS	Standard Lines of Code per second
SM	Systems Manager, Systems Management
SPDM	Special Purpose Dexterous Manipulator
SRAM	Static RAM
SSF	Space Station Freedom
SSMDM	Space Station Multiplexer-Demultiplexer
SSRMS	Space Station Remote Manipulator System

ST	Star Tracker
STRUCT	Structures
STSV	Standard Services
SW	Status Word
SYS	System
TCP/IP	Transmission Control Protocol/Internet Protocol
TCS	Telemetry Control System, Thermal Conditioning System
TDB	Time Distribution Bus
TDRSS	Tracking & Data Relay Satellite System
TGS	Time Generation System
TGU	Time Generation Unit
TM	Telemetry
TRRJ	Thermal Radiator Rotary Joint
TS	Telerobotic Servicer
UIL	User Interface Language (DMS Software)
USE	User Support Environment (DMS Equipment)
USL	United States Laboratory
VS	Video System
WP	Work Package
WRM	Water Recovery & Management Subsystem
XCVR	Transceiver
XPDR	Transponder
ZOE	Zone of Exclusion

1. INTRODUCTION

1.1 PURPOSE AND SCOPE

The purpose of this document was originally to be a working document summarizing Space Station Freedom (SSF) Data Management System (DMS) hardware and software design, configuration, performance and estimated loading data from a myriad of source documents such that the parameters provided could be used to build a dynamic performance model of the DMS. The document is published at this time as a close-out of the DMS performance modeling effort resulting from the Clinton Administration mandated Space Station Redesign. The DMS as documented in this report is no longer a part of the redesigned Space Station. The performance modeling effort was a joint undertaking between the National Aeronautics and Space Administration (NASA) Johnson Space Center (JSC) Flight Data Systems Division (FDSD) and the NASA Ames Research Center (ARC) Spacecraft Data Systems Research Branch.

The scope of this document is limited to the DMS core network through the Man Tended Configuration (MTC) as it existed prior to the 1993 Clinton Administration mandated Space Station Redesign. Data is provided for the Standard Data Processors (SDPs), Multiplexer/ Demultiplexers (MDMs) and Mass Storage Units (MSUs). Planned future releases would have added the additional hardware and software descriptions needed to describe the complete DMS. Performance and loading data through the Permanent Manned Configuration (PMC) was to have been included as it became available. No future releases of this document are presently planned pending completion of the present Space Station Redesign activities and task reassessment.

1.2 ORGANIZATION OF DOCUMENT

Section 2.1 defines the DMS System configurations by Mission Build (MB). Presented are the hardware/Orbital Replaceable Units (ORU) complement, definition of the ORUs connected to the DMS Optical Networks and a description of the hardware/software implementations of the Engineering Design Councils new Avionics Architecture to become two fault tolerant (2-FT). The local bus rechannelization is also described to the extent presently known. Section 2.2 presents the ORUs specified performance and actual measured performance where available. Section 2.3 presents the DMS software specified performance and estimated/measured performance data. Section 3 presents the allocations of the DMS Resources to satisfy application requirements and loading on each SDP and MDM. Section 4 is the Glossary. Appendix A contains SDP and MDM Performance Measurements/ Projections and Constants that are mostly taken from the "DMS Resource Model" (Reference 4) with additional data from other sources referenced to the source. Appendix B contains relevant notes and assigns numbers to the 28 Space Station Freedom documents that were referenced in the preparation of this document and are referred to in this document by the reference document number.. A Reference Library containing all of the referenced documents is available from John R. Stovall of the Lockheed Engineering & Sciences Company (LESC) at 713-333-7406.

1.3 <u>REFERENCE DOCUMENTS</u>

Comments on some of the Reference Documents are contained in Appendix B. Reference documents commented on in Appendix B are numbered by Reference Document Number and are also referred to by that number in the text. A listing of all reference documents is provided below.

1.3.1 NASA

a. SP-M-001, "Contract End Item Specification for Data Management System, Vol. 1: Data Management system Requirements", Rev. E, (NASA Approval Pending), Feb. 14, 1992. Reference Document #1.

b. CCBD JJ020746R1, "Avionics Architecture", Sept. 26, 1992. Reference Document #2 Rev. 1.

c. No Number, "Recommended Avionics Architecture", Architecture Group/SDT Engineering Design Council Support Group, July 29, 1992. Reference Document #2.

d. Number TBD, "Integrated Avionics Software Description", November 6, 1992. Reference Document #3 Rev. 2.

e. SSP 30255 Change Request Number BB003488A, "Baseline SSP 30255 Volume 2 Part 1, Introduction and Integrated Configuration", March 10, 1993.

f. No Number, " DMS Review Reston", January 21, 1992. Reference Document #5.

g. SSP 30261 Section 3 Revision D, "Data Management System Architecture Control Document Section 3: Data Management System" with Revisions D1 and D2, September, 1991.

h. JSC 36024, "Integrated Operations Scenarios MB-1 through MB-7, and UF-1", Feb. 1992.

1.3.2 CONTRACTOR

a. Number TBD, "DMS Resource Model Rev. G.1", MDSSC, October 8, 1992. Reference Document #4.

b. Number TBD, "SDP & MDM Resource Modeling Status", IBM, November 10, 1992. Reference Document #4A.

c. Number TBD, " DMS Resource Model Macro & Constant Definitions", IBM, September 21, 1992. Reference Document #4B.

d. Number TBD, "DMS Resource Model Constants", IBM, October 7, 1992. Reference Document 4C.

e. MSS 4-335-069-002, "Avionics Architecture Performance Assessment Report, Appendix B, Model Description", SSEIC, February 28, 1991. Reference Document #6.

f. No Number, Contract NAS 9-18200, "Data Management System (DMS) Technical Interchange Meeting Work Package No. 2 (WP-2)", MDSSC, July 8, 1992. Reference Document #7.

g. MDC 92H0252 Rev. A, SSFP, DR SY-03, Contract NAS 9-18200. "Software Release Contents Document", MDSSC, Dec. 10, 1992 Reference Document #8A replaces: No Number, "DMS Release Contents Version T1 Restructure Detailed Version Preliminary", IBM, June 30, 1992. Reference Document #8.

h. No Number, "Local Bus I/O Chaining An Introduction and Overview", Draper Labs, August 25, 1992. Reference Document #9.

i. No Number, "Performance Requirements and Load Point of the EDP/NIA", IBM, August 11, 1992. Reference Document #10.

j. No Number, "End to End Latency", IBM, November 6, 1991. Reference Document #11.

k. SSFP DR SY-40.1I, Contract No. 87916006, MDC H4542, "User's Guide (Software) for DMS Release 2", MDSSC, September 30, 1992. Reference Document #12.

l. SSFP DR SY-01.3I, Contract No. 87916006, 90IBMX0032R1, " Systems Engineering and Integration Trade Studies DMS Performance Analysis Summary White Paper", IBM, December 30, 1990. Reference Document #13.

m. SSFP DR SY-01-1.3I, Contract No. 87916006, 91IBMX0017R1, "System Engineering and Integration Trade Studies DMS Local Bus Performance Analysis White Paper", IBM, October 16, 1992. Reference Document #14.

n. No Number, "Best Estimate of Summary SLOCS Including Threats", IBM, June 24, 1992. Reference Document #15.

o. SSFP DR SY-06.2I, Contract No. 87916006, 153A101-PTIC, "Critical Item Development Specification for Mass Storage Unit", IBM, Oct. 9, 1992.

p. SSFP DR SY-06.2I, Contract No. 87916006, 152A401-PT1D, "Critical Item Development Specification for the Standard Data Processor", IBM, Oct. 9, 1992.

q. SSFP DR SY-06.2I, Contract No. 87916006, 152A403-PT1D, "Critical Item Development Specification for the Embedded Data Processor", IBM, Oct. 9, 1992.

r. SSFP DR SY-06.2I, Contract No. 87916006, 152A404-PT1D, "Critical Item Development Specification for the Network Interface Adapter", IBM, Oct. 9, 1992.

s. SSFP DR SY-06.23I, DID DI-E-3132, Contract No. ?, X8262556, Space Station Multiplexer/Demultiplexer (SSMDM) Functional Equivalent Unit (FEU) Critical Item Product Specification, Honeywell, Oct., 92.

t. No Number, Contract NAS 9-18200, "Data Management System (DMS) Software Detailed Design Review No. 3.2 (WP-2)", MDSSC, December 14, 1992. Reference Document #16.

u. LESC-29688-B, "Space Station Freedom Program Acronym List", Lockheed Engineering and Sciences Company, Nov. 2, 1992. Reference Document #17.

v. SSFP DR SY-01.3I, Contract No. 87916006, 91 IBMX0025, "Systems Engineering and Integration Trade Studies BIU Performance Measurement White Paper", IBM, August 5, 1991. Reference Document #18.

w. SSFP DR SY-28.1I, Contract No. 87916006, 150A243-02, " Software Detailed Design Document for the Standard Services (STSV), IBM, Nov. 16, 1992. Reference Document #19.

x. SSFP DR SY-55.1, Contract No. 87916006, 150A202-03, "Software Interface Control Document (Data Management System Release 2) Annex 1 - Onboard Application Programming Interface Definition (APID), IBM, September 1992. Reference Document #20.

y. SSFP DR SY-34.1, Contract No. 87916006, 150A241C Revision C, "Software Requirements Specification (DMS Standard Services)", IBM, August 1992. Reference Document #21.

z. SSFP DR SY-34.1, Contract No. 87916006, 150A141-02, "Software Requirements Specification (Data Management System - Release 2, Operating System/Ada Run Time Environment Annes II - Ada Run Time Environment Interface Definition", IBM, September 1992. Reference Document #22.

aa. SSFP DR SY-28.1) Contract No. 87916006, 150A143-01, "Software Detailed Design Document (Data Management System Operating System/Ada Run Time Environment for Release 2)", IBM, September, 1992. Reference Document #23.

ab. L. Shaw and J. B. Goodenough, "Real-Time Scheduling Theory and Ada", Computer Magazine, April 1990, pp53-62. Reference Document #24.

ac. R. Brown, The Charles Stark Draper Laboratory, Inc., "Priority Inversions in R1 STSV Design", October 1, 1990. Reference Document #25.

ad. No Number, "Viewfoils for DMS Software Detailed Design Review", IBM, December 14, 1992. Reference Document # 26.

ae. No Number, "Resource Model Documentation", IBM, March 1, 1993. Reference Document #27.

af. No Number, "Avionics System Management Document Volume 1", MDSSC, May 1993, Reference Document #28.

2. SYSTEM CONFIGURATION

Building of the SSF is a very complex undertaking. The SSF was planned to be assembled in 17 steps or Mission Builds (MBs) from First Element Launch (FEL) through PMC as is shown in Table 2.1-1, Assembly Sequence Launch Manifest from Reference #3 Rev. 2 and NASA Reference Document f.

2.1 CONFIGURATION

System configurations are shown in Figure 2.1-1 and Figure 2.1-2 for Stage 4 configuration(MB-4) and MTC respectively from Reference #3 Rev. 2. Figures 2.1-3 and 2.1-4 are the system configuration for PMC as discussed in paragraph 2.0.4. Table 2.1-2 lists the DMS components by name, description and MB sequence. Table 2.1-2 does not include interfaces to European Space Agency (ESA) and Japanese Experiment Module (JEM) networks. A complete list of the SSFP equipment can be found in Reference #3 Rev. 2. This build up sequence was verified against Reference Document f(CR# BB003488A).

2.1.1 CONFIGURATION FOR MB-2 (FEL) THROUGH MB-4

The configuration to be supported at MB-4 by the external SDPs and MSUs is shown in Figure 2.1-1. No DMS equipment is active with MB-1. On MB-2, the DMS becomes active in the equipment mounted on the truss and remains active during buildup through MB-4. The external SDPs and MSUs are unused after phase-over to the internal SDPs on MB-5. The DMS is single fault tolerant during this period.

SDP A and SDP B are both 9 bus SDPs (SDP-B3). Reference 2 Rev. 2 directs implementation of this configuration and provides detailed configuration information. All software runs in SDP A with SDP B the backup.

2.1.2 CONFIGURATION FOR MB-5

The first internal DMS SDPs and MSUs (in Node 2) and MPACs (in Node 2 and the Cupola) arrive on MB-5. Processing is moved into the two internal SDPs and MSUs from the 2 external SDPs and MSUs that were used for MB-2 through MB-4. This configuration is shown in Figure 2.1-2 "MTC Processing Architecture" less SDPs 3 and 4, the Lab Multi-purpose Application Console (MPAC), and MSU 2 all of which arrive at MB-6.

The DMS Architecture to achieve the required SSF fault tolerance is discussed in section 2.1.5. Fault tolerance at MB-5 is unique in the build-up sequence. The software in the internal SDPs is designed around the PMC fault tolerance levels, a 2 fault tolerant (2-FT) set and a 1 fault tolerant (1-FT) to achieve software compatibility from MTC forward. This hardware and software implementation design is shown in Figure 2.1-5, "Recommended SDP Software Functional Allocation" and discussed in section 2.1-5. The 2-FT software normally executes in one SDP and the 1-FT software in the other SDP. However, the first fault in the 2-FT SDP causes the only remaining SDP to begin execution of the 2-FT software and stop executing the 1-FT software, with the effect that for MB-5 the 1-FT software is actually zero-fault tolerant. The Zone of Exclusion (ZOE) MSU also serves as the back-up core MSU at MB-5. The Canadian Space Agency SDP (SDP-11) becomes available at MB-5 for operating the Space Station Remote Manipulator System (SSRMS) at a zero fault tolerance level, with the backup-drive software in the core SDPs.

The SDP to Local Bus Architecture is shown in Figure 2.1-6, "Recommended DMS SDP to Local Bus Architecture." SDP-1 and SDP-2 are both 18 bus SDPs (SDP-B6). Reference 2 Rev. 2 directs implementation of this configuration providing detailed configuration information, a detailed explanation of the reason for the new architecture and how this architecture should function.

2.1.3 CONFIGURATION FOR MB-6

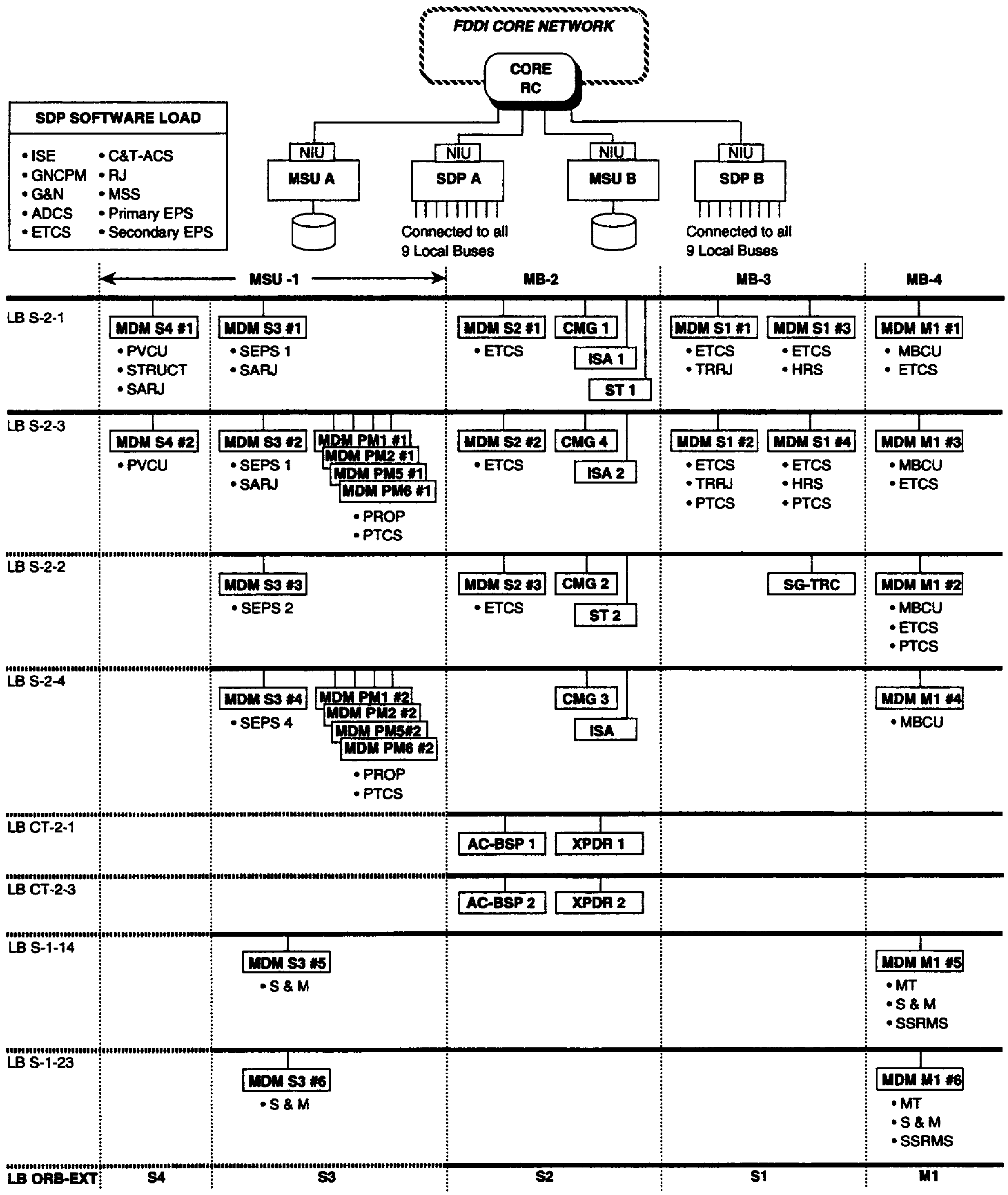
The core SDPs and MSUs become 2-FT starting at MB-6 (MTC) with the arrival of the US. Lab module containing SDP-3, SDP-4, an MPAC-F and MSU-2. Figure 2.1-2, "MTC Processing Architecture" shows this configuration. The arrival of another core MSU allows the ZOE MSU to be used just for ZOE recording and playback starting at MTC. SDP-11 remains at the zero fault tolerance level with the backup drive software in the core SDPs.

2.1.4 CONFIGURATION FOR MB-7 THROUGH MB-17 (PMC)

This configuration is shown for reference only in Figures 2.1-3 and 2.1-4. Additional DMS equipment arrives during the build-up to PMC at MB-17. The Canadian Space Agency (CSA) SDP-11 becomes single fault tolerant with the arrival of Node 1 at MB-11, which also includes the final MPAC. Additional information for PMC will be included as it becomes available.

Table 2.1-1. Assembly Sequence Launch Manifest

Milestone	Flight	Sub-elements
FEL	MB-1	ITS-S4, ITS-S3, STBD INBD SOLAR ARRAYS, MOBILE TRANSPORTER, UNPRESSURIZED BERTHING -MECHANISM
	MB-2	ITS-S2,2 PROPULSION MODULES (A&B)
	MB-3	ITS-SI, STBD CNTL RAD PANELS & BOOM, TDRSS ANTENNA, SSRMS
	MB-4	ITS-M1, CETA DEVICES (A&B),.MT BATTERIES, GAS CONDITIONING ASSEMBLIES (A&B)
	MB-5	NODE 2 CORE, NODE RACKS, PRESSURIZED BERTHING MECHANISM-A, CUPOLA WITH WORKSTATION
MTC	MB-6	U.S. LAB MODULE CORE, USL SYSTEM RACKS, USL PAYLOAD RACKS (7 MINIMUM), MBS (ASRM REQUIRED)
	MB-7	AIRLOCK, SPACE SHUTTLE EMUs, PRESSURIZED BERTHING MECHANISM-B, SPDM, MMD
	MB-8	ITS-PI, PORT CNTL RAD PANELS & BOOM
	MB-9	ITS-P2, 2 PROPULSION MODULES (C&D)
	MB-10	TS-P3, ITS-P4, PORT INBD SOLAR ARRAYS
	MB-11	NODE 1 CORE, NODE RACKS, ITS-S5
	MB-12	JEM MODULE CORE, JEM SYSTEM RACKS, JEM PAYLOAD RACKS (9 MINIMUM) (ASRM REQUIRED)
	MB-13	COLUMBUS MODULE FUNCTIONALLY OUTFITTED, NASA-PROVIDED EQUIPMENT, APM STOWAGE, APM PAYLOAD RACKS (9 MINIMUM) (ASRM REQUIRED)
	MB-14	ITS-S6, STBD OTBD SOLAR ARRAYS
	MB-15	JEM EXPOSED FACILITY, JEM ELM PS CORE, JEM ELM ES, JEM RACKS, JEM PS RACKS (ASRM REQUIRED)
	MB-16	HAB MODULE CORE, HAB RACKS, USL RACKS (ASRM REQUIRED)
PMC	MB-17	ACRV

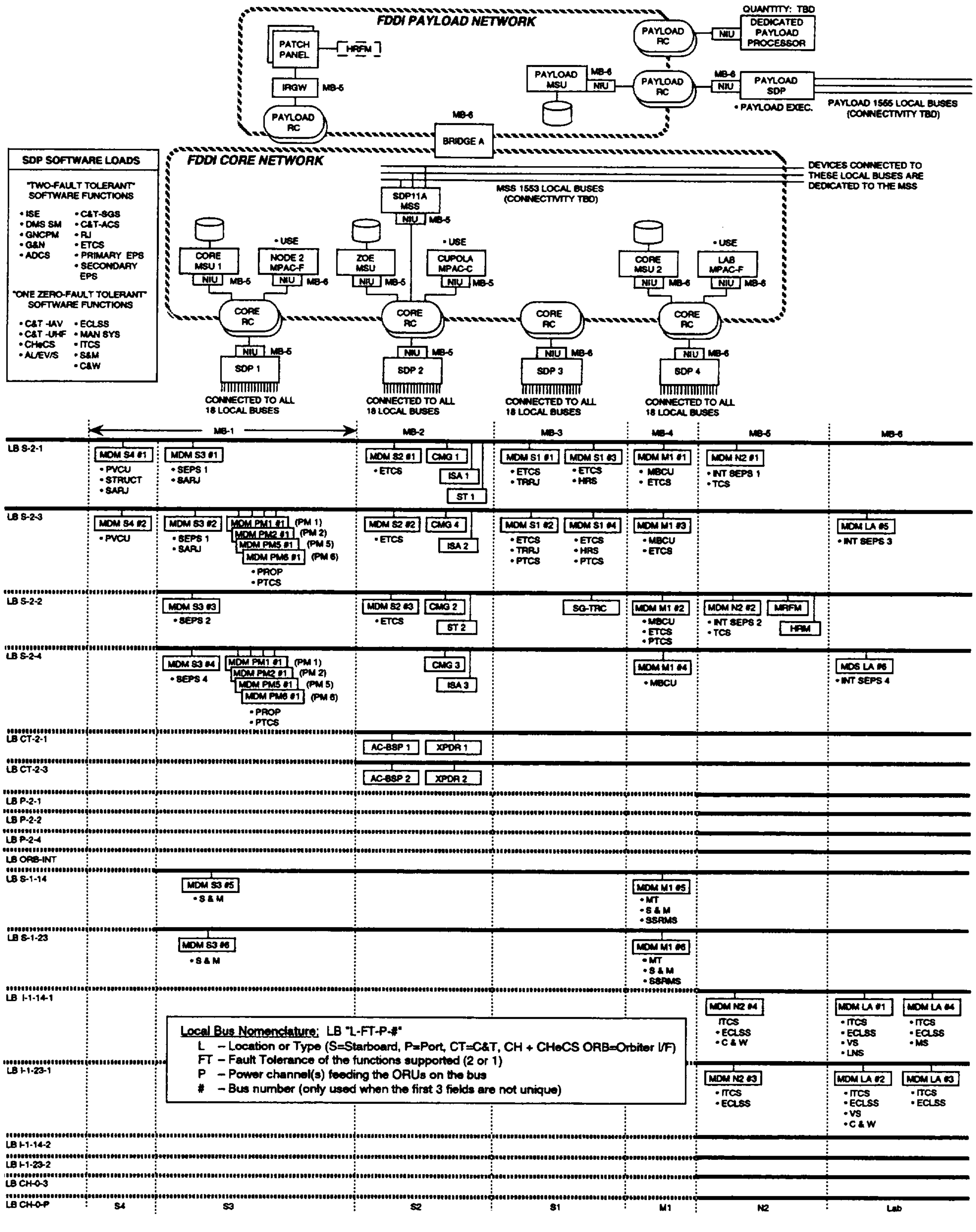


Local Bus Nomenclature: LB "L-FT-P-#"

L – Location or Type (S=Starboard, P=Port, CT=C&T, ORB=Orber I/F)
FT – Fault Tolerance of the functions supported (2 or 1)
P – Power channel(s) feeding the ORUs on the bus
\# – Bus number (only used when the first 3 fields are not unique)

Sources:
• Technical Description Document, 9/24/92
• Device Connectivity Data Base, 9/18/92

Figure 2.1-1. Processing Architecture MB-4 Configuration



Sources: Technical Description Document (9/24/92) and Device Connectivity Data Base, 9/18/92

Figure 2.1-2. MTC Processing Architecture

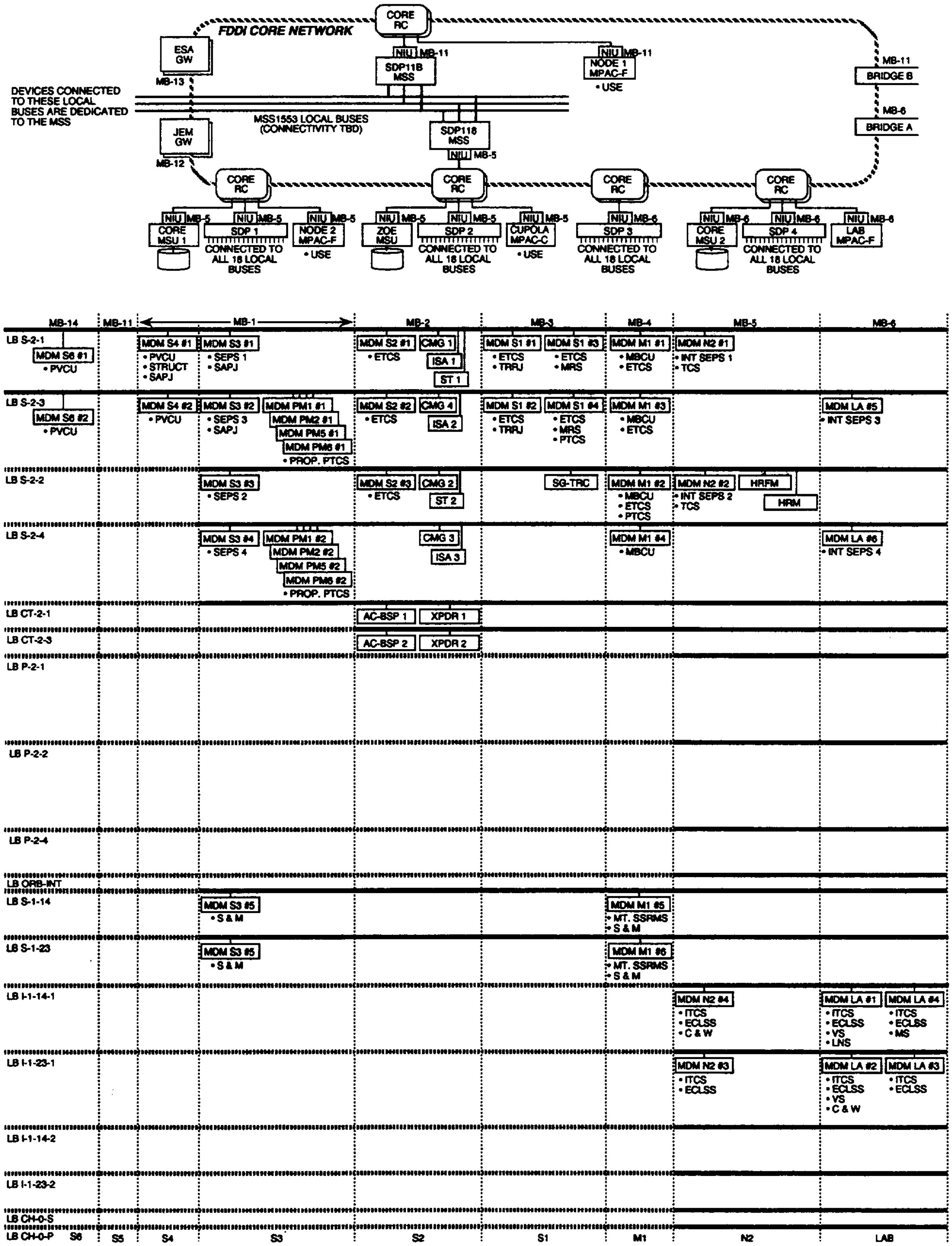
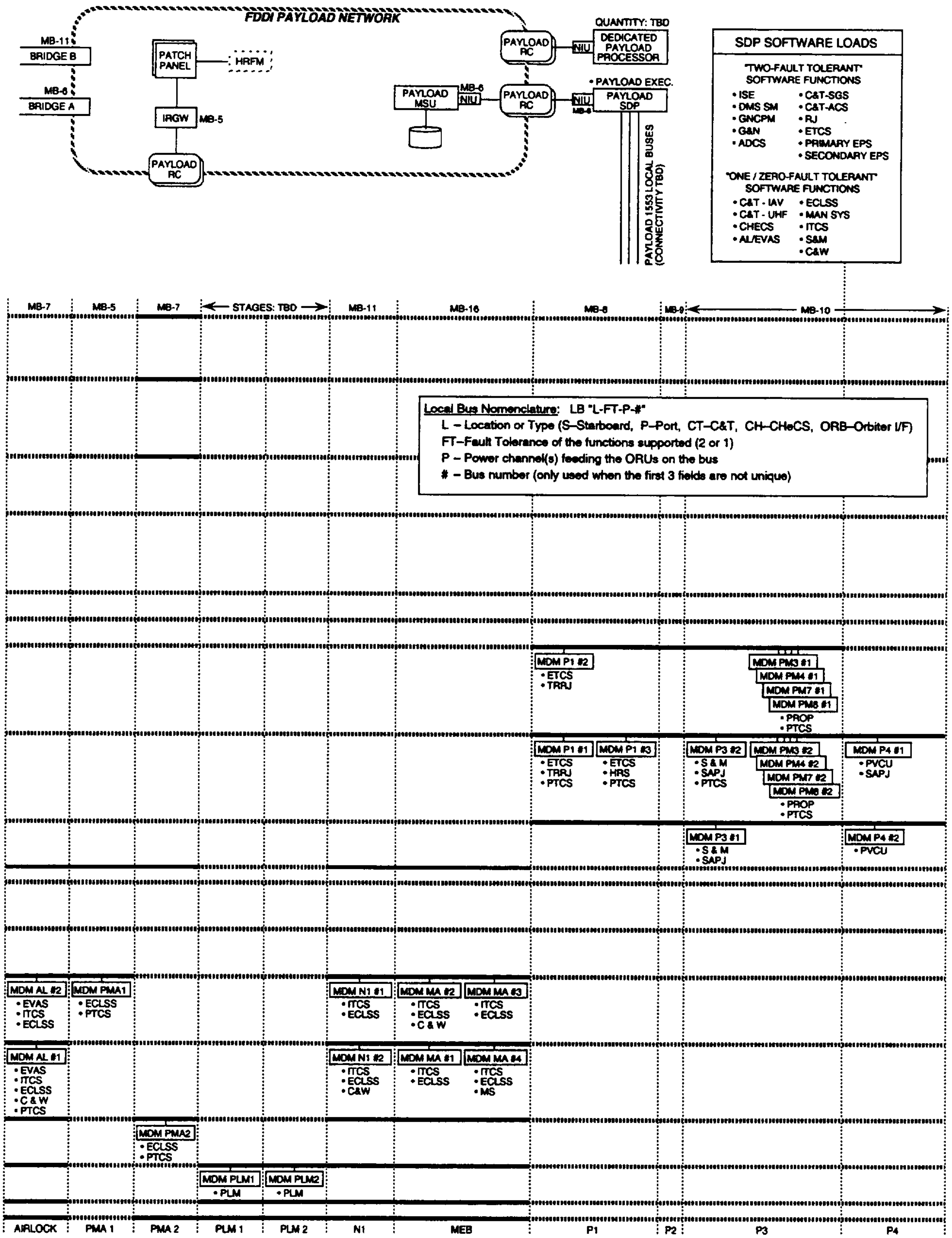


Figure 2.1-3. PMC Processing Architecture (Page 1 of 2)



SOURCE: TECHNICAL DESCRIPTION DOCUMENT (9/24/92) AND DEVICE CONNECTIVITY DATA BASE (9/18/92).

Figure 2.1-4. PMC Processing Architecture (Page 2 of 2)

Table 2.1-2. DMS Components Mission Build Sequence

ORU Name	Description	WP	SEG ELE	MB	QTY
MB-2 SDPs A & B	SDP-B3/See Table 2.1-4 for Applications	2	S2	2	2
MTC SDP 1&2	SDP-B6/See Tables 2.1-5 and 2.1-6 for Applications	2	N2	5	2
MTC SDP 3&4	SDP-B6/See Tables 2.1-5 and 2.1-6 for Applications	2	Lab A	6	2
SDP 7	SDP-B1/See Table 2.1-5 for Applications	1	Lab A	6	1
SDP 11A	SDP-B1/See Tables 2.1-5 and 2.1-6 for Applications	2	N2	5	1
SDP 11B	SDP-B1/See Tables 2.1-5 and 2.1-6 for Applications	2	N1	11	1
MSU 1	MSU/See Table 2.1-5 for Applications	2	N2	5	1
MSU 2	MSU/See Table 2.1-5 for Applications	2	Lab	6	1
MB-2 MSU A&B	MSU/See Table 2.1-4 for Applications	2	S2	2	2
MB-2 TGU A&B	TGU/DMS	2	S2	2	2
TGU A	TGU/DMS	2	N2	5	1
TGU B	TGU/DMS	2	N1	11	1
MPAC-F	MPAC-F/See Table 2.1-5 for Applications	2	N2	5	1
MPAC-C	MPAC-C/See Table 2.1-5 for Applications	2	CUP	5	1
MPAC-F	MPAC-F/See Table 2.1-5 for Applications	2	Lab A	6	1
MPAC-F	MPAC-F/See Table 2.1-5 for Applications	2	N1	11	1
Bridge A	Bridge	2	N2	5	1
Bridge B	Bridge	2	N1	11	1
RC	Ring Concentrator	2	-	-	16
IRGW A&B	Intermediate Rate Gateway	2	N2	5	2

2.1.5 RECOMMENDED SDP TO LOCAL BUS ARCHITECTURE

This architecture is described in detail in Reference Document #2 Rev. 1.

2.1.5.1 SDP Architecture for Increased Failure Tolerance

The recommended SDP will service eighteen local busses. It is a modification to the baseline accomplished by adding three additional Bus Interface Units (BIUs) to a standard SDP. This SDP is designated SDP B-6. Additional detail on the SDP B-6 is provided in paragraph 2.2.1.1. The change was made in order to provide sufficient local bus capacity to correct a number of deficiencies in the previous architecture. Vital SSF system functions were reassigned in this new architecture to different fault containment domains thus providing separate redundant strings in order to prevent any individual failure from causing the loss of multiple redundant strings of system function. To support these containment domains, the Recommended Avionics Architecture Channelization and Functional Repartioning redefines the DMS MIL-STD-1553 user bus architecture's and reallocates system function/ORUs to these devices. Separate DMS control paths are defined for 2-FT functions and 1-FT functions, with 0-FT functions assigned according to design constraints defined in Reference Document #2. Figure 2.1-6 illustrates the assignment of the eighteen local bus busses to accommodate the rechannelization. There are seven 2-FT busses, two S-Band local busses(also 2-FT), one Orbiter local bus(0-FT), six 1-FT local busses and two CHeCS(0-FT) local busses.

In order to support the defined containment domains, the software operational concepts were also modified as follows and as illustrated in Figure 2.1-5.

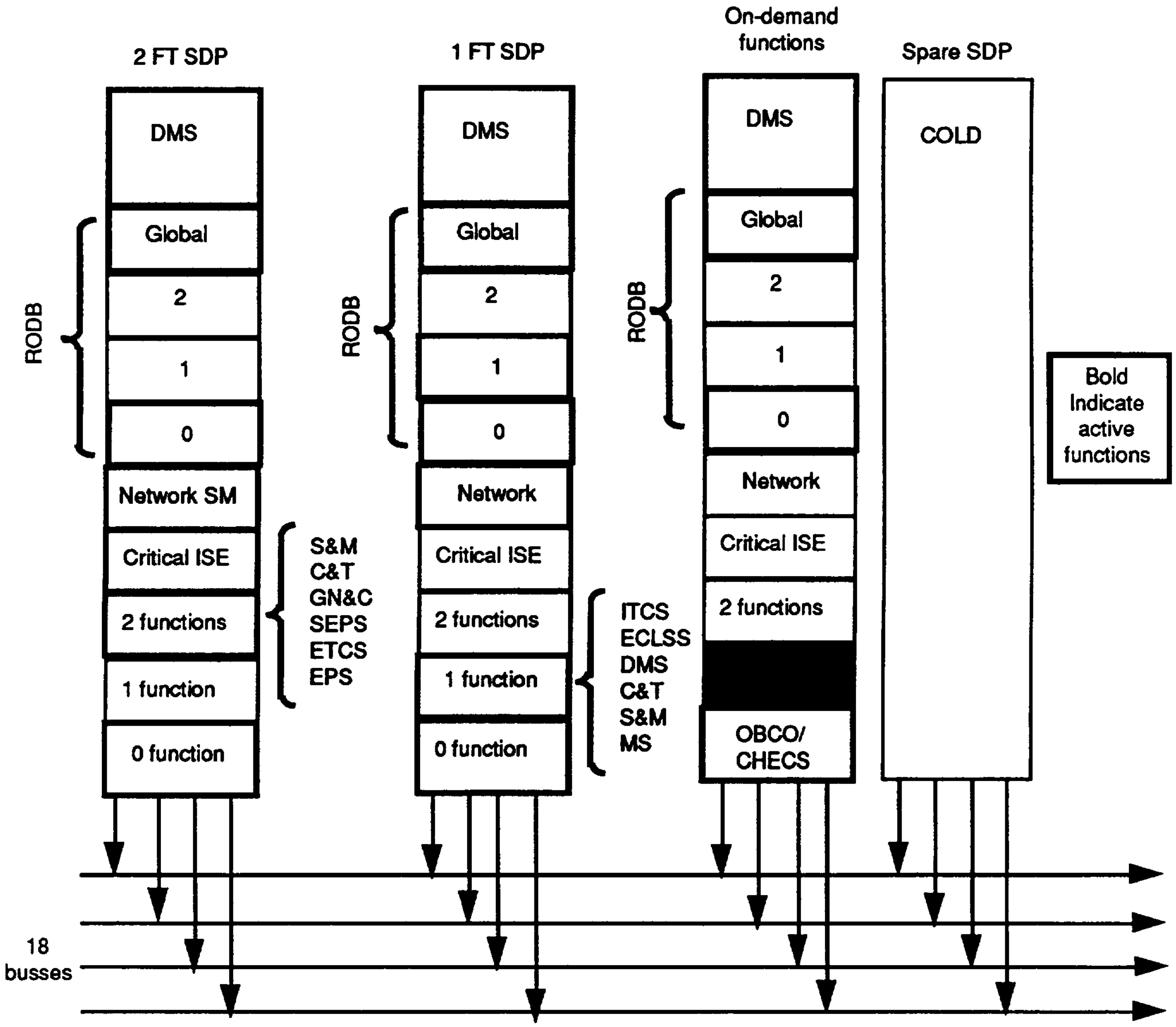
a. All software performing 2-FT functions will be resident and active in one of the four recommended SDP's.

b. All software performing 1-FT functions will be resident and active in one of the three remaining SDP's.

c. Software performing 0-FT functions will be resident and active in the SDP controlling the local busses which provide connectivity to the 0-FT on demand functions.

d. Upon detection of a 2-FT SDP failure during normal operations, the 1-FT SDP will assume immediate responsibility of the 2-FT functions and a cold/spare SDP will be powered up to resume the 1-FT functions. The architecture for this switch over is described in Reference Document #28, the Avionics System Management Design Document. The 2-FT SDP writes critical data at the required intervals into the backup 1-FT SDP to enable rapid switch over to be accomplished.

e. Either 2-FT or 1-FT functions will be active within a single SDP at a given time not both, however, both software partitions will be loaded into all powered SDPs at Initial Program Load (IPL) time. All SDP's will contain the same software load.



NOTE: Software load is identical in all SDPs shown
1 FF capabilities are inactive in 2 FT
likewise for 2 FT capabilities in 1 FT

2-FT SDP is nominally SDP-1
1-FT SDP is nominally SDP-2
0-FT SDP is nominally SDP-3
SPARE SDP is nominally SDP-4

Figure 2.1-5. Recommended SDP Software Functional Allocation

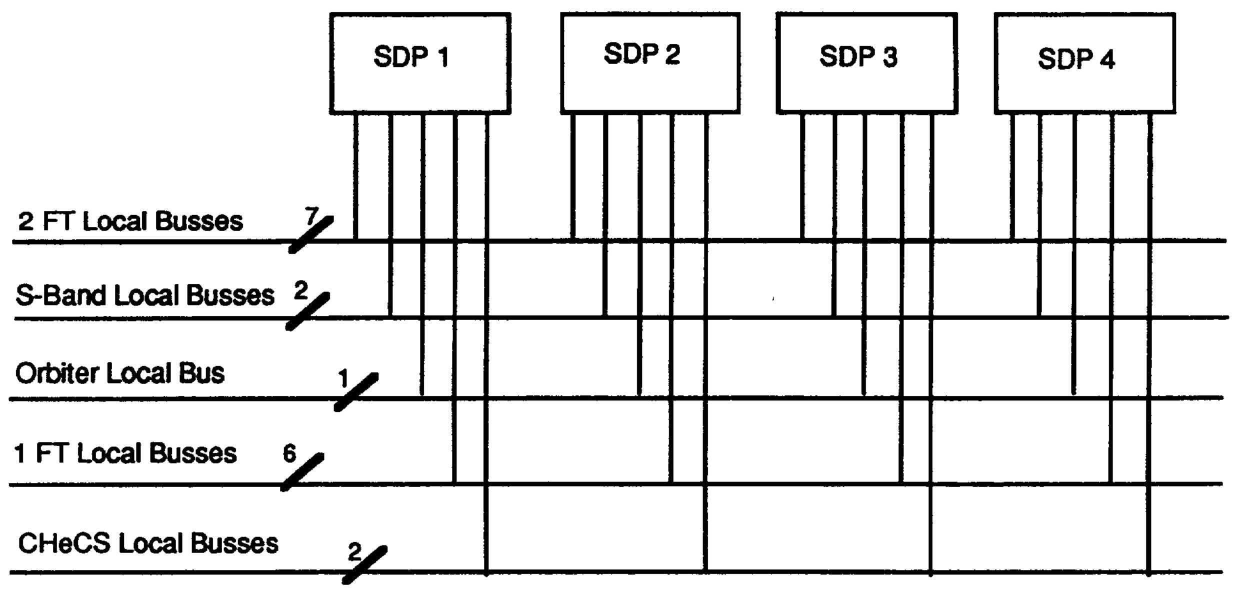


Figure 2.1-6. Recommended DMS SDP to Local Bus Architecture

2.1.6 DMS SOFTWARE ARCHITECTURE AND PARTITIONING

DMS software is divided into ten packages called Computer Software Configuration Items (CSCIs). Section 2.3.1 gives a concise functional description of each CSCI. In order to understand the DMS hardware architecture and how the DMS software is implemented in this architecture, it is necessary to have an understanding of the three software architecture domains. They are illustrated and defined in Figure 2.1-7 and consist of the Information Management Domain, Communications Domain and the Process Control Domain. All software in the Communications Domain and the Information Management Domain is contained within the DMS. The software in the Process Control Domain is composed of multiple work packages' designs and codes. Since the SSF is built in increments called MB's, the need for software varies based on each MB and depends on the configuration of the SSF at that specific MB. Tables 2.1-3 through 2.1-6 describe the DMS CSCI and Application Software partitioning by MB, fault containment domain and by DMS ORU. An X in the table indicates that this software is loaded and active in that particular hardware device. Table 2.1-3 for the Communications Domain applies to all MBs. Table 2.1-4 for both the Process Control and Information Management Domains applies to MB 2-4. Tables 2.1-5 for the Information Management Domain and 2.1-6 for the Process Control Domain apply to MB-5 and subs. Note that Table 2.1-6 does not assign any functions to the 0 Fault tolerant (0-FT) SDP. CHeCS, a 0-FT function is shown to be active in the 1-FT SDP. Table 2.1-7 is the DMS Release Contents Summary. The dates shown in Table 2.1-7 are only approximate as they were continually changing. A complete set of the DMS Release Contents can be found in Reference #8. Table 2.1-8 is a functional partitioning of the MDM software by application. In addition to the application software shown, each MDM also contains a complete set of MDM Run Time Environment (RTE) and MDM Services Software. Figure 2.1-7 and Tables 2.1-3 through 2.1-8 are from Reference 3 Rev. 2.

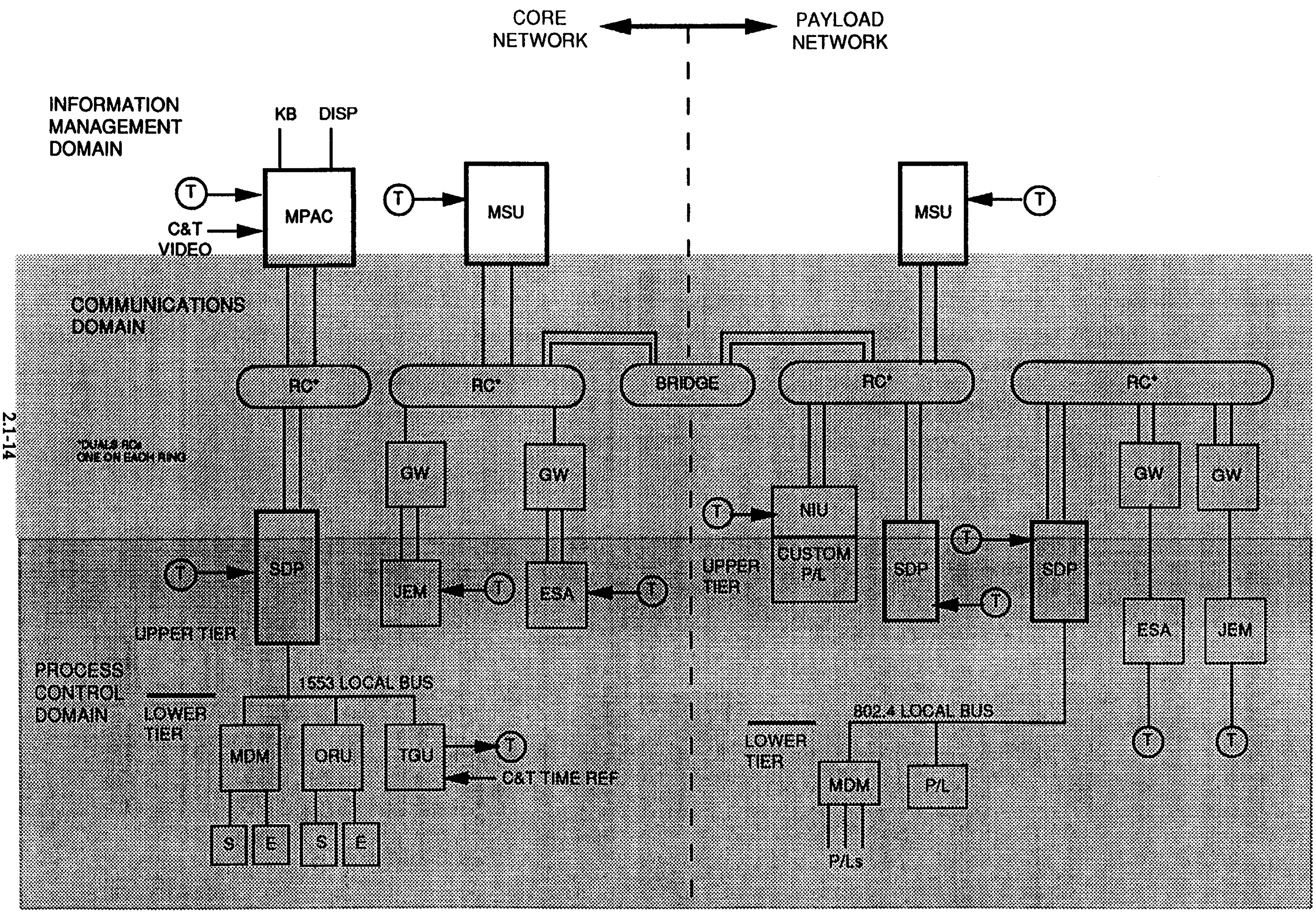


Figure 2.1-7. DMS Architecture Domains

Table 2.1-3. Software Partitioning Communication Domain-All MBs

DMS CSCIs	LOADED IN				
	ALL SDPs IN NOS EDP	BRIDGE IN NOS EDP	GW IN NOS EDP	ALL MPACs IN NOS EDP	ALL MSUs IN NOS EDP
OS/ADA RTE	X	X	X	X	X
NOS	X	X	X	X	X
SM NODE MGMT	X	X	X	X	X

Assumptions:

1. Systems Management (SM) is monitoring processor page for faults.
2. After MB-4, at least one MSU is powered up at all times to load or change the contents of DMS ORUs.
3. For MB-2 through MB-4, all MSUs and SDPs are powered as long as they function without error.

Table 2.1-4. Software Partitioning - Process Control and Info Management MB 2-4

DMS CSCIs	LOADED AND ACTIVE IN			
	SDP A&B		MSU A&B	
	NOS EDP	APP EDP	NOS EDP	APP EDP
OS/Ada RTE	X	X	X	X
NOS	X		X	
DSAR				X
DSAR CLIENT		X		
ZOE RECORDING				X
STSV		X		X
SM NODE		X		X
SM NETWORK				X
APPLICATIONS SOFTWARE	NOS EDP	APP EDP	NOS EDP	APP EDP
GCA		X		
CRITICAL ISE				X
UIL EXEC				X
PROP		X		
GN&C		X		
C&T ACS		X		
ETCS		X		
S&M		X		
CHeCS (RAD ONLY)		X		
PRIMARY EPS		X		
SECONDARY EPS		X		

Table 2.1-5. Software Partitioning - Information Management MB-5 and Subs

DMS CSCIs	LOADED AND ACTIVE IN					
	ALL MPACs	SDPs 1-4	SDP 11 (A&B)	SDP 7	CORE MSUs	PAYLOAD MSU
	APP EDP	APP EDP	APP EDP	APP EDP	APP EDP	APP EDP
OS/Ada RTE	X	X	X	X	X	X
DSAR SERVER					X	X
DSAR CLIENT	X	X	X	X		
ZOE RECORDING					X	
STSV	X	X	X	X	X	X
SM NODE	X	X	X	X	X	X
SM NETWORK		X				X
SYS LOADER					X	X
USE	X					
APPLICATIONS	APP EDP	APP EDP	APP EDP	APP EDP	APP EDP	APP EDP
CRITICAL ISE		X				
NON-CRITICAL ISE					X	
UIL EXECUTOR			X		X	X
PAYLOAD EXECUTIVE				X		

Assumptions:

1. At least one MSU is powered up at all times to load or modify the contents of DMS ORUs.

Table 2.1-6. Software Partitioning - Process Control MB-5 and Subs

MB-5 AND SUBS	2 FT SDP	1 FT SDP	SDP 11A
DMS			
OS/Ada RTE	A	A	A
DSAR CLIENT	A	A	A
STSV	A	A	A
SYS MGMT NODE	A	A	A
SYS MGMT NETWORK	A	A(backup)	
APPLICATIONS			
TWO FAULT TOLERANT			
CRITICAL ISE	A	R	
PROP	A	R	
GN&C	A	R	
EATCS	A	R	
C&T-ACS	A	R	
C&T-SGS	A	R	
ROTARY JOINTS	A	R	
S&M	A	R	
EPS			
Primary	A	R	
Secondary	A	R	
ONE FAULT TOLERANT			
ITCS	R	A	
IAS	R	A	
IVS	R	A	
BM	R	A	
HISS	R	A	
VS	R	A	
MAINTENANCE W/S	R	A	
ECLSS	R	A	
CHECS	R	A	
AL/EVAS	R	A	
GCA	R	A	
MTE	R	A	
MSS BACKUP DRIVE	R	R	
MSS			A

Assumptions:

1. A capital A in the column denotes the function is resident and active in the respective fault tolerance SDP.
2. A capital R in the column denotes the function is resident but not active in the respective fault tolerance SDP.
3. At lease one MSU is powered up at all times to load or change the contents of DMS ORUs.

Table 2.1-7. DMS Release Contents Summary

Release	CI Date	Contents Summary
R1	4/30/92	Supports OS, initial STSV local bus support, internal RODB read/write, file I/O to local MSD, IPL, and initial display prototyping
R2	6/22/92	Supports local bus serial devices, action read/write, initial MODB object definition/table generation
R3	12/21/92	Supports 6/9 bus SDP, complete local bus processing, initial USE flight execution environment, MODB upgrades for CM, table generation and object definition
R4	9/6/93	Supports remote data access/commanding, telemetry, monitor data/command applications via displays, file uplink, MSU, network IPL and status monitoring, TGU, ITVE table building
OI-1	4/11/94	Certified R1-R4 capabilities to support MB-2
R5	3/28/94	Supports alarm and message management, network management, table generation for IODB and C-MDM
OI-2	10/31/94	Certified R1-R5 capabilities to support MB-5
R6 OI-3	1/31/95	Supports commanding in blind, direct API for telemetry, UIL, TGU arbitration, delta table build
R7	11/27/96	Supports ZOE, USE crew aids (editors, E-mail, etc.) X-Virtual Terminal

Table 2.1-8. MDM Software Partitioning by Application

MDM NAME	FLT	SYSTEMS
S3 #1	MB01	SEPS,SARJ
S3 #2	MB01	SEPS,SARJ
S3 #3	MB01	SEPS
S3 #4	MB01	SEPS
S3 #5	MB01	STRUCT,MECH
S3 #6	MB01	STRUCT,MECH
S4 #1	MB01	EPS PVCU,STRUCT,SARJ
S4 #2	MB01	EPS PVCU
PM1 #1	MB02	PROP,PTCS
PM1 #2	MB02	PROP,PTCS
PM2 #1	MB02	PROP,PTCS
PM2 #2	MB02	PROP,PTCS
S2 #1	MB02	EATCS
S2 #2	MB02	EATCS
S2 #3	MB02	EATCS,PCTS
S1 #1	MB03	TRRJ,EATCS
S1 #2	MB03	TRRJ,EATCS,PTCS
S1 #3	MB03	EATCS HRS
S1 #4	MB03	EATCS HRS,EATCS,PTCS
M1 #1	MB04	EPS MBCU,EATCS
M1 #2	MB04	EPS MBCU,EATCS,PTCS
M1 #3	MB04	EPS MBCU,EATCS
M1 #4	MB04	EPS MBCU
M1 #5	MB04	MT,STRUCT,MECH
M1 #6	MB04	MT,STRUCT,MECH
N2 #1	MB05	SEPS,EATCS
N2 #2	MB05	SEPS,EATCS
N2 #3	MB05	ITCS,ECLSS
N2 #4	MB05	DMS C&W,ITCS,ECLSS
PMA1 #1	MB05	DMS C&W,ITCS ECLSS
LA #5	MB06	SEPS
LA #6	MB06	SEPS
LA #1	MB06	LNS,ITCS,ECLSS,VS
LA #2	MB06	ITCS,ECLSS,MS
LA #3	MB06	DMS C&W,ECLSS,VS
LA #4	MB06	ITCS,ECLSS
LA #5	MB06	SEPS
LA #6	MB06	SEPS

2.2 DMS HARDWARE DESIGN/PERFORMANCE

This section addresses the DMS SDP, MSU and MDM ORUs.

2.2.1 GENERAL SDP, EDP, NIU AND BIU CARD CAPACITIES

This paragraph provides specified and measured performance data for the SDP to include the hardware modules that make up an SDP. Allocations of the SDP processing resources are provided in Reference 3 Revision 2 Section 4.2, p 4-1 and Section 3.1 this document.

2.2.1.1 SDP

The SDP is the primary computational device for Space Station. The SDP consists of an Embedded Data Processor (EDP) with the option for an additional EDP, is connected to the DMS optical network via a Network Interface Unit (NIU) and to from three to eighteen local busses(1553B) via a BIU. The following data was extracted from the Contract End Item (CEI) Specification for the Standard Data Processor, Document Number 152A401-PTID dated Oct. 9, 1992.

a. Figure 2.2-1 (figure 1 from 152A401-PT1D) is the functional block diagram for the SDP-B1, B2 and B3. The SDP-B6 (EDC-001 Configuration) as shown in Figure 2.2-2 would have three more BIUs for a total of 6.

b. Local Bus and Optical Network addresses are hardwired into each rack location and input to the SDP by an external connector. See 3.1.2.1.5 of 152A401-PT1D.

c. SDP has capacity for installation of 16 Mbyte Aux memory card(152A401-PT1D paragraph. 3.2.1.2.1).

d. SDP has capacity for installation of an additional EDP-16.

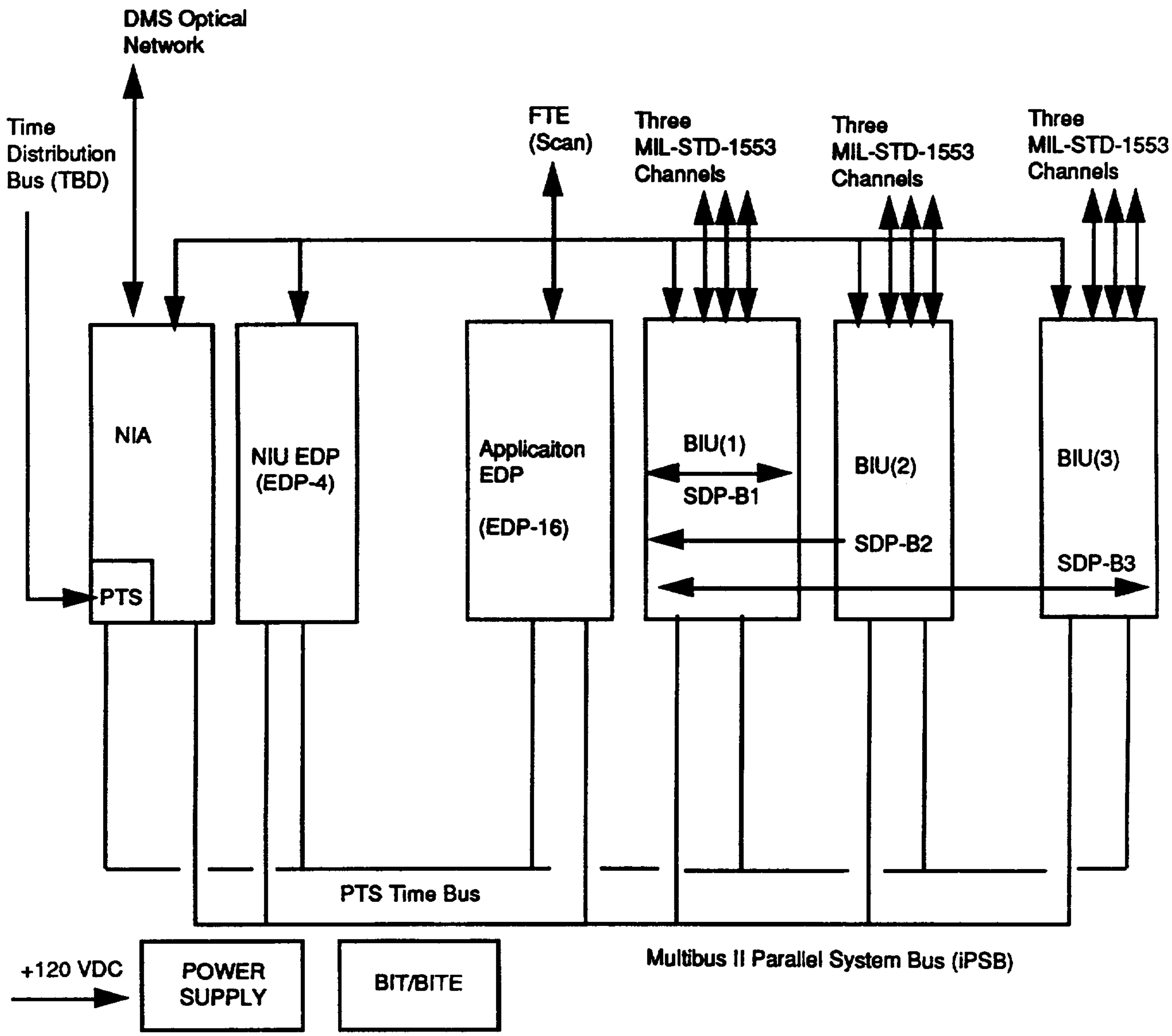


Figure 2.2-1. SDP Block Diagram

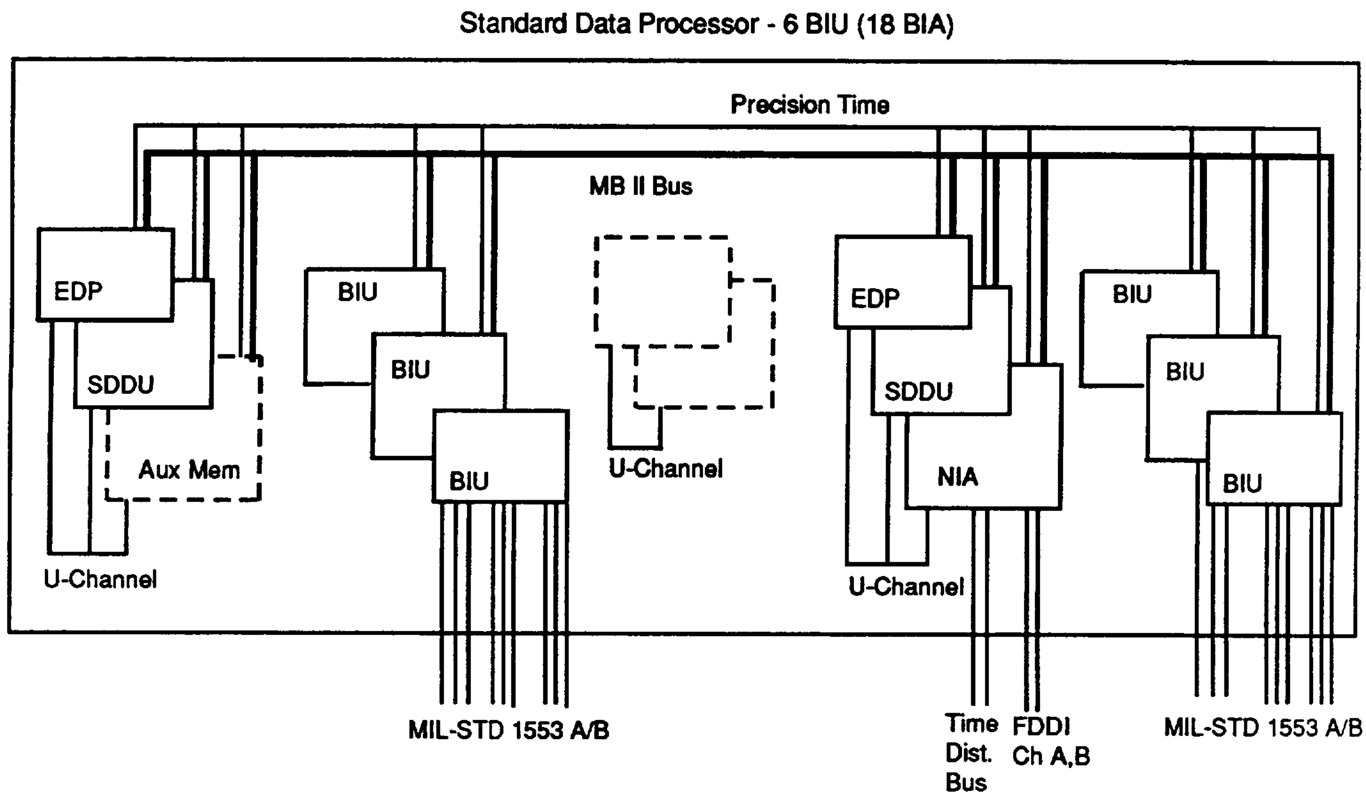


Figure 2.2-2. Eighteen Bus SDP-B6

2.2.1.2 APPLICATION Processor

The Application Processor is an EDP and is a single page, general purpose processor with a standard Instruction Set Architecture (ISA) using an Intel 80386 microprocessor or a functional equivalent. It is connected to a Intel Multibus II Parallel System Bus (iPSB) and the 32 bit (Level C) IBM Micro Channel.

2.2.1.2.1 Hardware Specifications

The following data was extracted from the CEI Specification for the Embedded Data Processor, Document 152A403-PTID Draft dated 10/9/1992 and other documents as referenced.

a. Figure 2.2-3 (figure 1 from 152A403-PT1D) is the functional block diagram for the EDP-16, the application EDP. The application EDP provides 16 Mbytes of Dynamic Random Access Memory (DRAM) user memory.

b. Figure 2.2-4 (figure 2 from 152A403-PT1D) is the functional block diagram for the EDP-4, the NIU EDP. The NIU EDP provides 4 Mbytes of DRAM user memory.

c. EDP-16 and EDP-4 provide support for an optional 16 Mbytes of additional Random Access Memory (RAM).

d. EDP-16 fixed point instruction execution rate = 3.9 Millions of Instructions per second (MIPs) for the weighted instruction mix in Intel document 230985. The Reference #1 requirement is presently 4 MIPs; however, it is being changed to 3.9 MIPs..

e. EDP-4 fixed point instruction execution rate = 3.4 MIPs for the weighted instruction mix in Appendix A of SSFP DR SY-06.2I, Contract No. 87916006 IBM152A403, 10/9/92, the EDP specification.

f. DMA logic shall support 16 and 18 bit data transfers at a rate of 4 Mbytes per sec.

g. The main processor shall be equivalent to an Intel 80386 microprocessor with a 80387 numeric coprocessor.

h. Memory cycle times vary from a minimum of 100 nanoseconds to 350 nanoseconds. They are given in paragraph 3.2.1.7.3 of the EDP specification. It is not anticipated that the model will require this low level of detail, but it is available if needed.

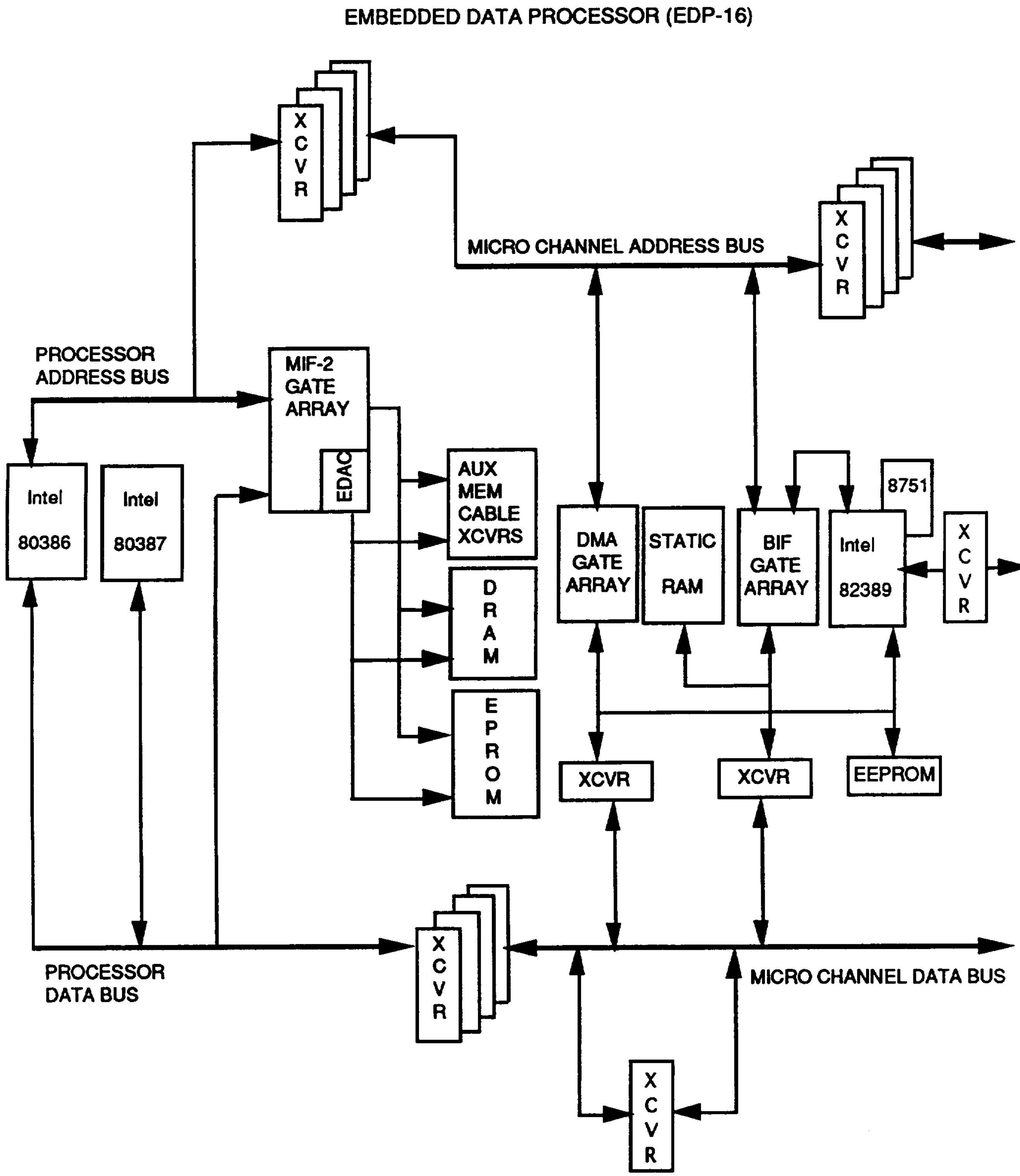


Figure 2.2-3. EDP-16 Block Diagram

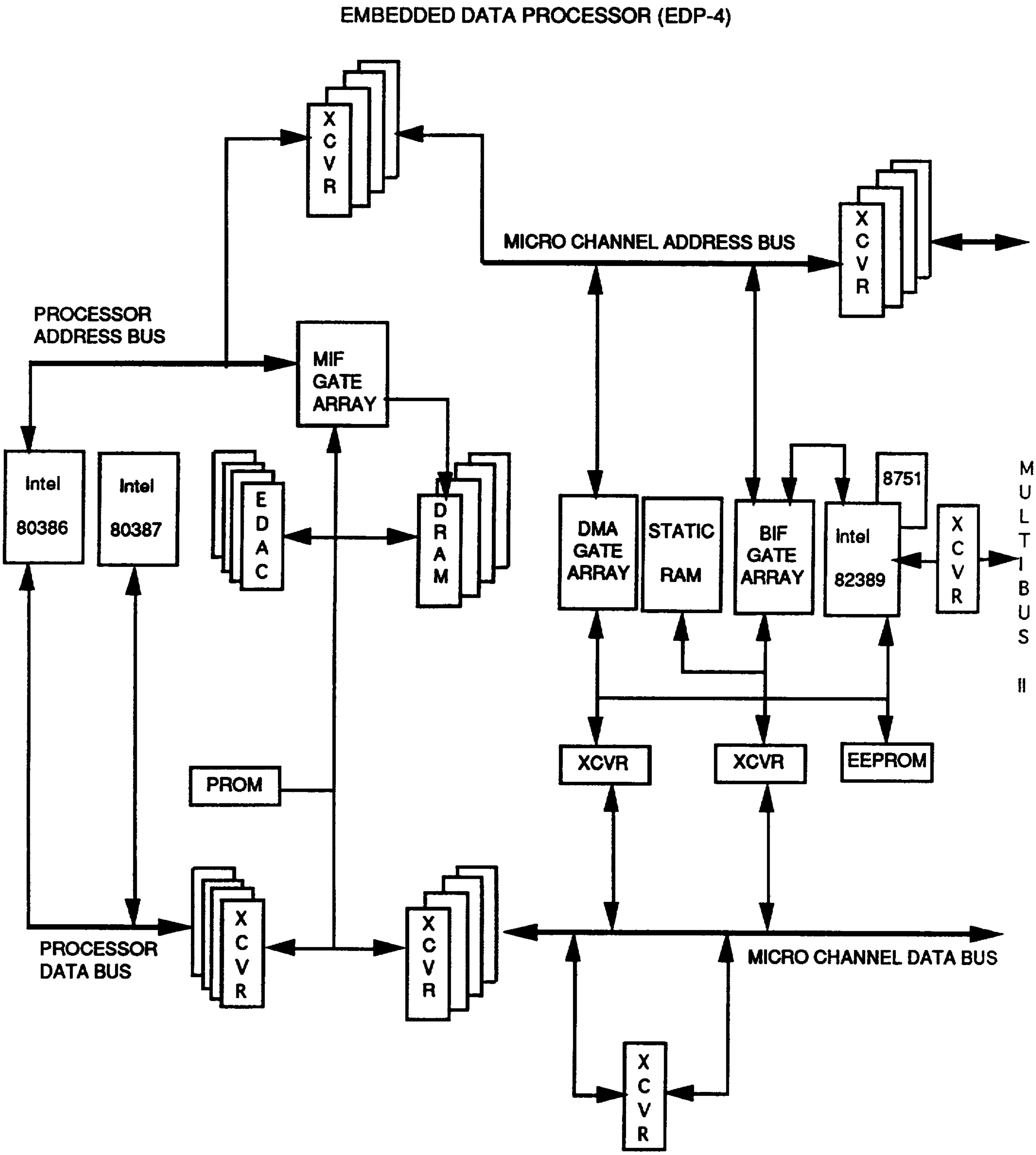


Figure 2.2-4 EDP-4 Block Diagram

2.2.1.2.2 Performance Parameters

a. See Section 2.3.4 and 3.2 this document.

b. See Appendix A "SDP Performance Measurements/Projections and Constants" this document. Note that the majority of this appendix is available in electronic form in the SDP constants file of Ref. #4. Data from other sources in Appendix A is marked by an *. In addition, the data in Appendix A has been modified to account for the increase in the EDP processing speed from 3.1 to 3.9 MIPs as explained in the appendix.

2.2.1.3 Network Interface Unit (NIU)

The NIU provides the host ORU with functional and physical interfaces to the Time Generation System (TGS) and to the DMS optical network. It consists of an EDP-4 and an Network Interface Adapter (NIA). The EDP-4 is addressed in 2.2.1.2

2.2.1.3.1 NIA Hardware Specification

The following data was extracted from the Critical Item Development Specification for the Network Interface Adapter Document 152A404-PT1D dated October 9, 1992.

a. Figure 2.2-5 (Figure 1 from 152A404-PT1D) is a functional interface diagram for the NIA.

b. The International Standards Organization (ISO) 8802-2 information field packet size packet size is variable up to 4475 bytes.

c. The NIA shall execute a minimum of 500 Logical Link Control (LLC) type 1 frames per sec. (data frames up to 4096 bytes) throughput at the MBII Interface when the NIA is not executing downloaded software.

d. The NIA performs functions associated with OSI Reference Model Layers 1 and 2.

   (1) Physical Layer (OSI Layer 1) conforms to ISO 9314-1 and ISO 9314-3 Standards.

   (2) Data Link Layer (OSI Layer 2) is composed of two sublayers. Lower sub layer is media access control (MAC) and is implemented per ISO 9314-2 and upper sub layer is LLC and is implemented per ISO 8802-2. LLC sub layer supports LLC Type 1 connectionless service.

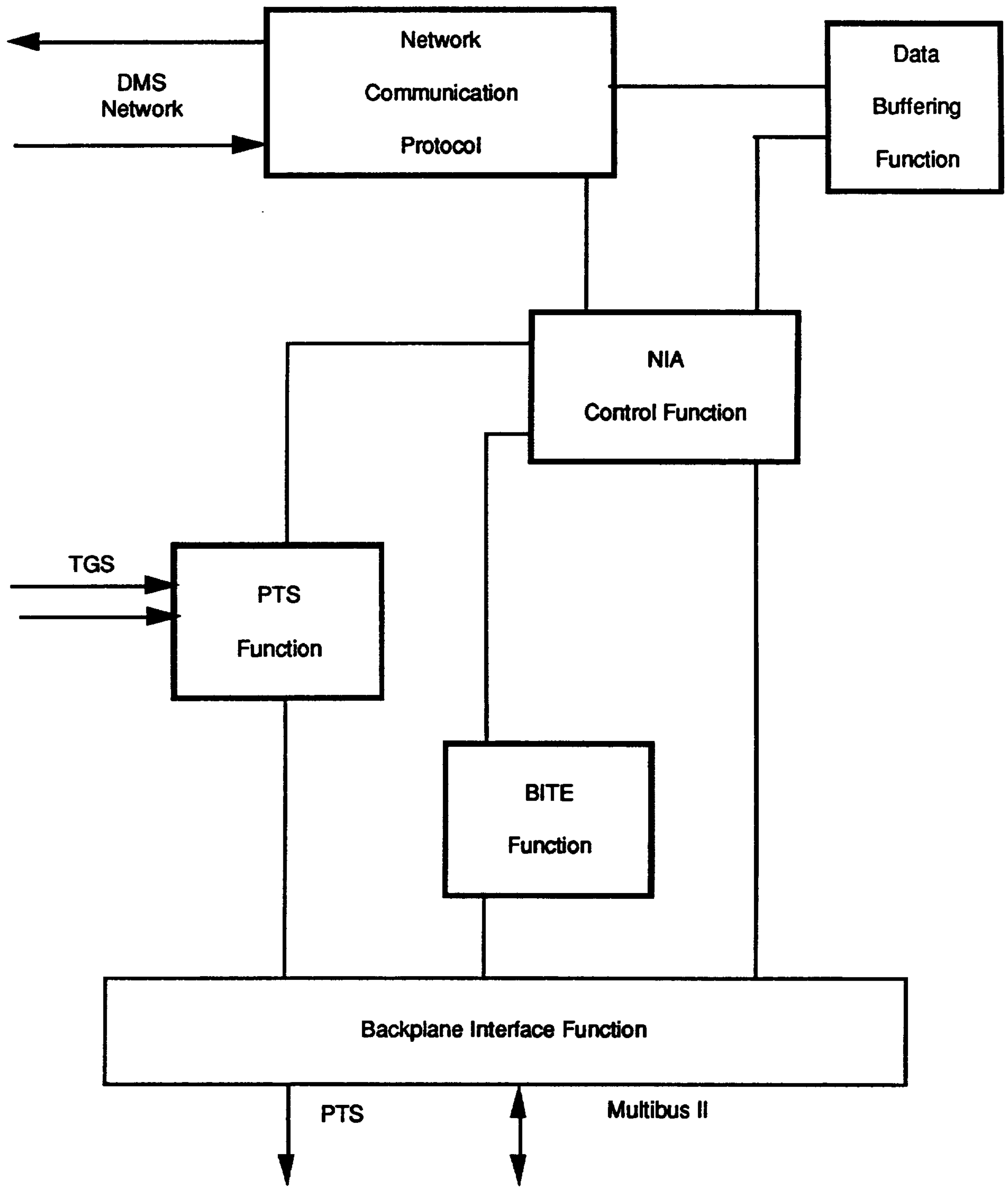


Figure 2.2-5. NIA Functional Block Diagram

e. Supports Station Management per American National Standards Institute (ANSI) X3T9.5/84-89. The NIA shall support a single MAC - Dual Attachment station.

f. General Computer Architecture

(1) Equivalent to Intel 80386 DX processor.

(2) 1 Mbyte of Static RAM (SRAM) expandable to 4 Mbytes.

(3) 512 Kbytes of Programmable Read Only Memory (PROM)

(4) Can download software from optical network at up to 25 frames/second (up to 4 Kbytes /frame) to its SRAM or via the MBII to another agent. The NIA shall accept download software from the MBII at the same rate.

2.2.1.3.2 Core Network Performance Requirements

The data in this section is extracted from Reference 10 and the DMS CEI Specification (Reference 1)

a. NODE

(1) Performance Requirement: > or = to 10 Mbits/sec (Mbps) throughput

(2) Load

- 4096 Bytes/message
- 90% direct Access
- 10% ISO
- < = 80% Utilization of any element.
- Poisson Arrivals

b. NODE

(1) Performance Requirements:> or = to 5 Mbps

(2) Load

- 4096 Bytes per message
- 100% Full ISO/OSI
- < or = to 80% utilization of any element
- Poisson arrivals

c. NETWORK

(1) Performance Requirement Latency

- Emergency Messages: 20 milliseconds (msec) avg., 25 msec 95% of time.
- Expedited Messages: 20 msec avg., 25 msec 95% of time.
- Normal Messages: 50 msec avg., 80 msec 95% of time.
- Background Messages: 80 msec avg., 100 msec 95% of time.

(2) Load

- < = 1 Mbps ISO at each node.
- < = 1 Mbps total emergency on the net.
- < = 1 Mbps total expedited on the net.
- < = 80% utilization of any element
- Poisson arrivals

2.2.1.3.3 Estimated NIU Performance

Note that the NIU and FDDI Network Performance is not included in Appendix A, nor in the "DMS Resource Model". The data presently available is presented in this paragraph.

a. NOS EDP processing delay (As of 10/15/92 no actual measurements have been made).

(1) 10 msec estimate, reference 6, paragraph. 3.1.4, p 11

(2) 7 msec estimate, reference 11, p 4. This is also the best estimate from IBM as of 10/15/92.

(3) Note that Network Operating System (NOS) EDP processing delay is only applicable to full ISO messages. Full ISO messages are now defined as layers 3 & 4. Direct Access messages are passed directly to the NIA.

b. NIA service time = 1.0 msec estimate , reference 11, p2. NIA performs layers 1 & 2.

c. Application EDP service time = .5 msec estimate, reference 11, p2

d. Data Transfer time NOS EDP to NIA and Application EDP to NOS EDP for ISO messages and from the Application EDP to the NIA for Direct Access messages is = to MBII. Overhead (OH) in reference 4 = 990 microsec.

e. Application EDP usage by Operating System (OS)/Ada Run Time Environment (RTE) for each message sent or received by the FDDI network projected to be 400 microsec. in reference 12, paragraph 3.1.4, p 38.

f. Application EDP usage by interface routine called by application initiating transfer is projected to be 200 microsec, in reference 12, paragraph 3.1.4, p 38.

g. FDDI digital data transfer rate = 100 Mbps instantaneous, in reference 6, paragraph 3.1.5, p11.

h. Hand off delay in passing token between NIUs = 50 microseconds, in reference 6, paragraph 3.1.5, p11.

i. Max. time a station can hold a token = .333 msec., in reference 6, paragraph 3.2.1, p 15.

2.2.1.4 Bus Interface Unit (BIU)

Serial local bus functions are performed by the BIU which contains three Bus Interface Adapters (BIA) and one Bus Control Unit (BCU). Each BIU provides interfaces for three dual - redundant MIL-STD-1553 channels.

2.2.1.4.1 Hardware Specification

The following data is extracted from the CEI Specification for the Standard Data Processor 152A401-PT1D paragraph. 3.2.1.5 dated October 9, 1992.

a. See Figure 2.2-6 (Figure 2 from 152A401-PT1D) for functional block diagram.

b. Each of the three BIA channels in a BIU can operate in Remote Terminal (RT) or Bus Controller (BC) mode independently of the other two channels.

c. Each BIA supports a burst data rate of up to .7 Mbps. Valid for a message chain where each message contains up to 32 data words. For MDMs 4 words are required for control leaving up to 28 words for data. See Figure 2.2-7 (Figure 1 from Reference #14).

d. Each BIU supports three BIAs operating at up to .7 Mbps data rate each.

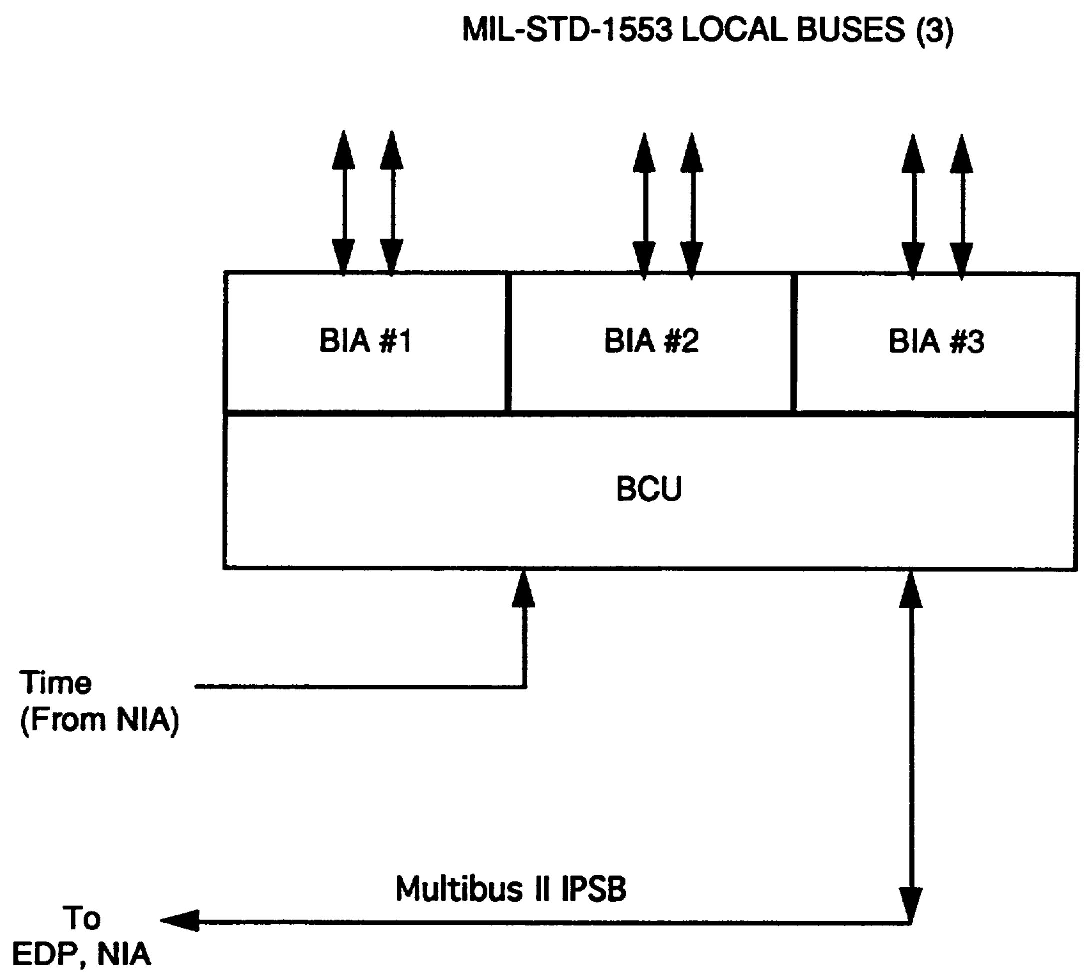
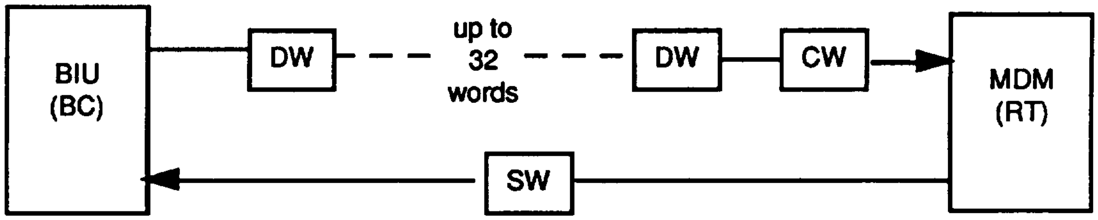
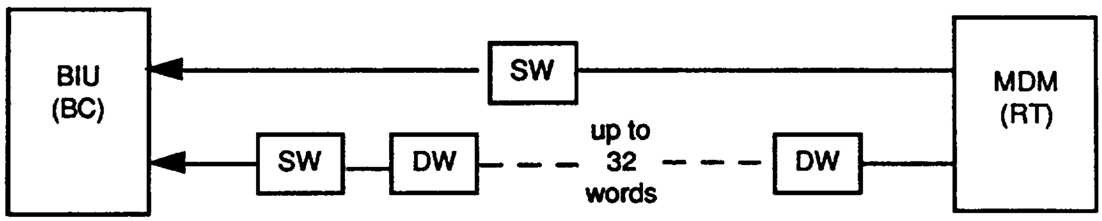


Figure 2.2-6. BIU Block Diagram

Local Bus (1553) Protocol Diagrams and Definitions



Effector Command Protocol

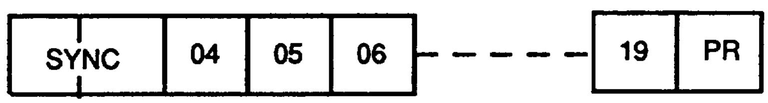


Sensor Read Protocol

Command Word (CW) contains 20 bits
Status Word (SW) contains 20 bits
Data Word (DW) contains 20 bits, but just 16 bits of data
4 DWs required for header words and information,
so Max. of 28 DWs of data per message.

Sensor/Effector Overhead = 1 CW, 1 SW and 4 Dw. i.e. 6 words, or 120 bits.

DW: 20 bits, but only 16 of data

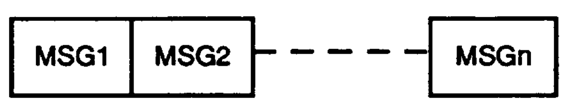


Analog Objects use 12 bits, however assume 1 analog per word
Discrete Objects use 1 to 8 bits, so from 16 to 2 discretes per word

(1553B)
Message,
up to 32 words

A word contains 2 bytes of data
A message comprises up to 32 words, or 64 bytes.

A chain/scan: a group of messages



if, maximum SDP buffer size = 4K bytes and each message is accompanied by 1 status word
then, max. # of messages per chain = 4K / (64+2) = 62 messages
then, max. # of sensors/effectors per scan = 62 * 28 = 1736

34 words at 20 µs + SW response time of 12 µs + Inter-message Gap (IMG) of 4 µs
equals 696 µs, or 1437 messages/sec or 45,977 words/sec or 91,954 bytes/sec.
Since only 28 of 32 words are data, this becomes 40,230 data words/sec or 80,459 bytes/sec.

Effector commands originate in Application, split at BIU into separate chains for each bus.
Sensor read chains originate in MDMs, collected at BIU into combined scan for MB II transfer.

Figure 2.2-7. Local Bus Messages

2.2.1.4.2 Performance

a. BIU/BIA Function - Note that reference 7 is a good explanation of how the BIU/BIA functions with release 3.2.

b. Table 2.2-1 from Reference 7, page B.1-17 provides the latest local bus scan read performance estimates at Release 3.2.

c. Figure 2.2-8 from Reference 7, page C.2-1 illustrates the BIU Services Domain. The BIU consists of a 80c186 processor, 3 MIL-STD-1553B BIAs, three (3) 64 Kbyte local bus memory segments, a 64 Kbyte global data memory segment, and 128 Kbytes of program memory. MPC in the figure is the Message Passing Coprocessor.

d. Table 2.2-2 provides Effector Command Latencies that are not provided in the DMS Resource Model. These latencies have been included in Appendix A.

2.2.2 MULTIPLEXER-DEMULTIPLEXER (MDM)

2.2.2.1 Hardware Specification

The MDM FEU Critical Item Product Specification X8262556, Rev.-, Honeywell SSO 61962 was reviewed. The document stated that performance data would be included in the next revision. Functional performance requirements for the FEU are the same as for the flight unit.

a. Hardware Configuration

   (1) RAM = 2 Mbytes, Reference 3 Rev. 2, page 3-77, Reference 1, page 3-259.

   (2) Electronically Erasable Programmable Read Only Memory (EEPROM) = 1 Mbyte, Reference 1, page 3-259.

b. Local Bus Configuration - Figures 2.1-1, 2.1-2, 2.1-3 and 2.1-4 identify the SDP local busses to which each MDM is assigned.

c. Main processor uses 386 SX instruction set, Reference 1, page 3-259.

d. Each MDM is attached to one 1553B Local Bus.

Table 2.2-1. Scan Read Performance Estimates at R3.2

Multiplier	Item	Required	Estimated(R3.2)
Per-Scan	Cyclic Asynchronous	100 us	700 us
	Cyclic Synchronous		1700 us
	On-Demand		3200 us
Per-Message	Timestamp Pre-processing	n/a	50 us
	Timestamp Write		4 us
	Timestamp Read		6 us
	Data Quality Pre-processing		20 us
Per-Analog	Raw Pre-processing	50 us	0 us
	Raw Write		8 us
	Raw Read		N/A
	Data Quality Pre-processing		N/A
	Data Quality Write		3 us
	Data Quality Read		N/A
	Timestamp Write		N/A
	Timestamp Read		N/A
	Data Conversion (1st Order Polynomial)		25 us
	Converted Write		4 us
	Converted Read		6 us
	Limit Check		0 us
	Total		46 us
Per Discrete		30 us	30 us

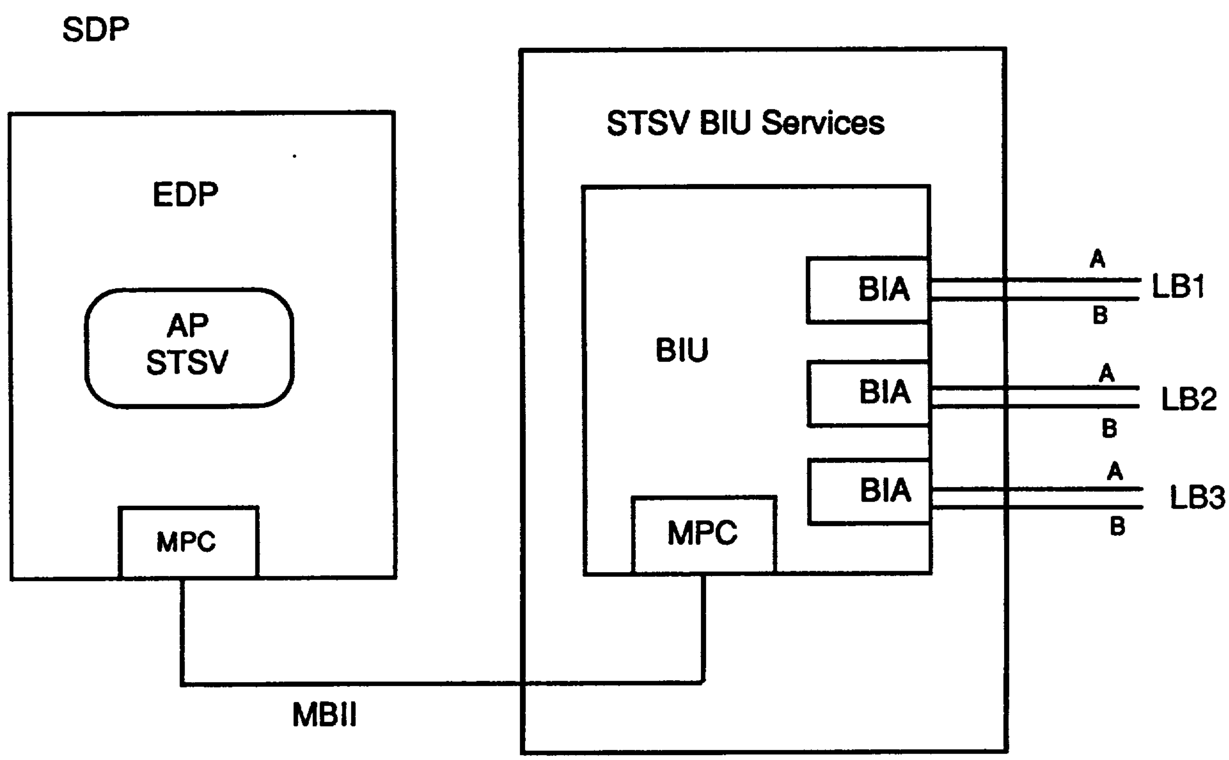


Figure 2.2-8. BIU Services Domain

Table 2.2-2. Effector Command Latencies µsec

Additional Dependency	12/90 Model	LBus Model	Resource Model
MDM overhead, one time only	150	`150	n/a
MDM cost per word, up to 1400 µs maximum	50	50	n/a
1553B response time and IMG per message	16	16	n/a
1553B overhead per command message	120	120	n/a
1553B cost per word	20	20	n/a
BIU processing latency	800	1870	n/a
portion of MBII driver not latency in-line	250	250	n/a
DMA across MBII, per 28-word message	10	20	n/a

2.2.2.2 Performance Parameters

a. Major/Minor Cycles

   (1) Specified Major Cycle = 1 sec., Reference 1, p 3-261.

   (2) Specified Minor cycle = 12.5 ms, Reference 3 Rev. 1, p 3-48, Reference 1, p 3-262.

   (3) Time synchronization = + or - 100 microsec.

b. Specified CPU speed = 1.6 Mips, Reference 1, page 3-259.

c. Table 2.2-3 from Reference 14 page 8 provides Sensor Read Latencies in microsec. that are not provided in the DMS Resource Model. These latencies have been included in Appendix A.

d. 1553B travel time from SDP to MDM = 4 ms. Reference 14, page 3

e. MDM response time is the time between receipt of on-demand sensor read request and when data is ready to be transmitted back to the SDP over the Local Bus = 17 msec average and 29 msec maximum, Reference 14, page 3. Specified times in Reference 1, p 3-357 = no greater than 22 msec on average and 37 msec 95% of the time.

f. With standard I/O cards an MDM is specified to perform 6000 I/O operations (one I/O operation to a single sensor effector) per second with a maximum sampling rate of 80 samples per second, Reference 1, page 3-263. Note that on p 3-351 in addition to 6000 I/O operations per second it is specified that the number of message per second shall be 215.

g. Maximum latency from time operation is requested at the Input/Output Card Controller (IOCC) interface until operation is completed is specified to be no greater than 150 microsec plus 50 microsec for each item in the scan list, Reference 1, page 3-263.

h. MDM processing for immediate (on-demand) lists takes up to 29 msec to execute. Reference #14.

Table 2.2-3. Sensor Read Latencies μsec

Additional Dependency	12/90 Model	LBus Model	Resource Model
MDM overhead, one time only	150	`150	n/a
MDM cost per word, up to 1400 μs maximum	50	50	n/a
Sync delay for 1553B transfer	100	100	n/a
1553B response time and IMG per message	16	16	n/a
1553B overhead per command message	120	120	n/a
1553B cost per word	20	20	n/a
BIU processing latency	800	535	n/a
DMA across MBII, per 28-word message	10	20	n/a

2.2.3 MASS STORAGE UNIT (MSU)

The MSU is the primary bulk data storage device for the DMS. It consists of an EDP-16, a Mass Storage Device (MSD) with a minimum of 320 Mbytes of nonvolatile memory, a connection to the DMS optical network via an NIU and a connection to the TGS.

2.2.3.1 Hardware Specification

The following data was extracted from the CEI Specification for the Mass Storage Unit, Document 153A101-PTIC Draft dated 10/9/1992 and other documents as referenced.

a. Figure 2.2-9 (figure 1 from 153A101-PT1C) is the functional block diagram for the MSU.

b. The EDP-16 Central Processor Unit (CPU) is discussed in paragraph 2.2.1.2.

c. The NIU is discussed in paragraph 2.2.1.3.

d. Average access time shall be less than 12.5 ms not including applicable latency periods.

e. Minimum burst data transfer rate with media shall be 2 Mbytes per second.

f. The MSU shall provide a formatted storage capacity of at least 320 Mbytes.

2.2.3.2 Performance

Note that MSU performance data is not included in Appendix A.

a. Actual Disk Storage Capacity = 400 Mbytes, Reference 3 Rev. 2, p 4-3.

b. Average seek and latency time for a read or write assumed to be 20.5 msec which corresponds to 50 disk accesses per second. Reference 6 page 10.

c. SCSI interface throughput = 10 Mbps. Reference 6 page 10.

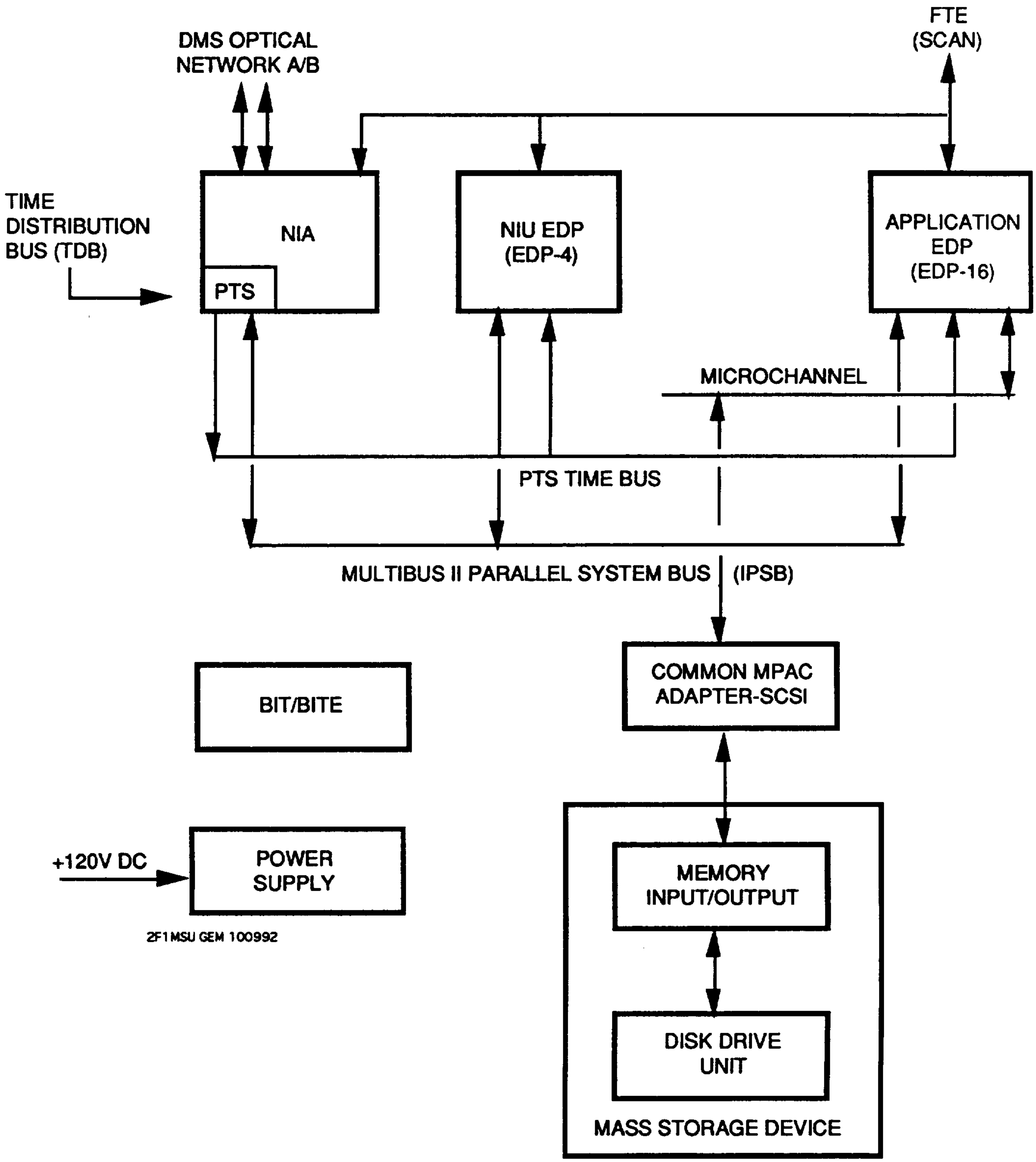


Figure 2.2-9. MSU Block Diagram

2.3 DMS SYSTEM/SOFTWARE DESIGN AND PERFORMANCE

2.3.1 SOFTWARE CSCI DESCRIPTIONS

The DMS software is divided into ten CSCIs. The nine CSCIs dealing with flight software are briefly described in the following paragraphs. The Master Object Data Base (MODB) CSCI is not described as it is a ground repository of information and not relevant to the flight system performance model. The software is being developed by several different organizations as referenced in the following paragraphs. Each of the CSCIs is specified by a Type B specification and the detailed design of each CSCI described in a Type C detailed design document. In addition, Reference # 3 Revision 2, the "Integrated Avionics Software Description Document" is recommended as the best general source of information available on the complete DMS software architecture. Reference #12, "User's Guide (Software) for DMS Release 2 is the best general source of information on DMS software use. The following descriptions are extracted from Reference #3 Rev. 2.

2.3.1.1 Operating System/Ada Run Time Environment (OS/Ada RTE) (IBM)

The OS/Ada RTE resides in the SDP, MPAC, MSU, Bridge and Gateways and provides the layer of DMS software that isolates other services as well as applications software from the underlying data processing hardware. The OS/Ada RTE provides management, allocation, and deallocation of CPU, memory, clock, and Input/Output (I/O) device data processing resources for Ada software, including DMS utilities and applications. The OS/Ada RTE also provides transparent interfaces for application-to-application communications and file access via the Network operating System (NOS).

2.3.1.2 Network Operating System (NOS) (IBM)

The NOS provides data transmission and communications resources and services to automated on-board systems. The NOS manages delivery services for on-board applications. The NOS performs formatting, encoding and sequencing as necessary to the delivery of data packets to network nodes.

2.3.1.3 Data Storage and Retrieval (DSAR) (IBM)

The NIU provides the host ORU with functional and physical interfaces to the TGS and to the DMS optical network. It consists of an EDP-4 and an NIA. The EDP-4 is addressed in 2.1.1.2

2.3.1.4 Standard Services (STSV) (IBM)

STSV provides a common messaging service between applications programs independent of the processor location of the program. STSV handles all local bus I/O and I/O management and provides services needed by two or more applications such as telemetry formatting, Caution and Warning (C&W) messaging, limit sensing and measurement biasing and calibration

2.3.1.5 System Management (SM) (IBM)

SM provides for the startup and shutdown of nodes on the DMS optical network. SM monitors and reports DMS errors, faults, overloads and anomalies found in the onboard hardware and distributed system configuration. SM facilitates or initiates corrective action to insure the availability and integrity of the DMS. SM manages planned changes to the DMS configuration such as initialization of devices/process/network. It also manages unplanned changes such as those necessitated by hardware or software failure.

2.3.1.6 User Support Environment (USE) (IBM)

USE provides the crew interface required for the runtime control of all MPAC displays. The USE provides the runtime services for a direct manipulation graphics interface and an English like User Interface Language (UIL). The USE supports autonomous hardware and software process control systems with crew monitoring and manual intervention capabilities for trouble shooting and override of automated control functions.

2.3.1.7 MDM RTE (Honeywell)

The MDM RTE resides in the MDM and provides the layer of DMS software that isolates other services as well as application software from the underlying processing hardware. The MDM RTE provides management, allocation, and deallocation of CPU, memory, clock, and I/O device data processing resources for Ada software.

2.3.1.8 MDM Services (Honeywell)

The MDM services provide support functions on behalf of applications programs. The MDM services is responsible for communication on the local and user bus, provides I/O services to/from sensors and effectors and a common interface for applications code which is a subset of the SDP applications program interface device.

2.3.1.9 User Interface Language (UIL) Executor (Charles Stark Draper Laboratory)

The UIL Executor (Time liner) is a language interpreter used to automate crew or ground initiated procedures. The UIL Executor will execute a priori defined and compiled procedures referenced by a unique name. UIL is planned for MB-2, but is not expected to be used for basic vehicle operations.

2.3.2 DMS RELEASE CONTENTS

Reference 8, the. "**DMS Release Contents Version T1 Restructure Detailed Version Preliminary dated June 30, 1992**" document describes in detail the contents of the DMS releases and the capabilities that exist at each stage in the build process. A top level summary was shown in Table 2.1-7.

2.3.3 DMS CSCI SLOC COUNT ESTIMATES

Reference 15, the DMS "**BEST ESTIMATE OF SUMMARY SLOCS INCLUDING THREATS**" is a detailed listing of the best estimate of DMS sizing as of 6/92. This is the latest estimate available. It is presented by language type, CSCI and Release version. The software estimates are given in cumulative form by how many additional SLOCs are added for each release. It is reproduced here as Table 2.3-1. R1 through R4 supports MB-2 and R1 through R5 is for MB-5 support.

2.3.4 PERFORMANCE

Included in this section are system performance requirements and parameters both specified and measured.

2.3.4.1 Performance Model Parameters

Table 2.3-2 defines the hardware parameters that are recommended for input to the model in order to define each hardware unit. This table may require modification to satisfy specific system configurations.

Table 2.3-1. Best Estimate of DMS Summary SLOCS Including Threats

LANG	CSCI	R1	R2	R3.1	R3.2	R4	R5	R6	R7	TOTAL
Ada	OS	0.4	0.0	0.0	1.0	0.5	0.5	0.0	0.0	2.4
	STSV	13.7	3.5	5.0	9.5	18.4	5.5	0.5	0.5	56.6
	USE	0.0	0.0	0.0	5.4	1.0	3.7	0.0	0.0	10.1
	NOS	0.0	0.0	0.0	8.0	0.0	0.0	0.0	0.0	8.0
	SM	0.3	1.6	0.0	0.2	15.4	4.7	8.0	0.3	30.4
	DSAR	3.7	5.8	0.5	0.0	8.2	1.6	0.0	5.0	24.8
	MODB	0.0	15.0	47.8	26.4	41.9	30.0	13.0	0.5	174.5
Ada TOTAL		18.1	25.8	53.3	50.5	85.3	46.0	21.4	6.3	306.8
C	OS	5.7	2.3	0.0	2.0	2.0	0.6	2.0	(0.1)	14.5
	STSV	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	USE	7.4	12.2	5.4	6.1	7.7	39.3	6.1	31.0	115.2
	NOS	0.0	36.0	0.0	8.9	0.0	0.6	2.1	0.0	47.6
	SM	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	DSAR	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	MODB	0.0	0.0	32.5	2.5	7.5	20.5	3.6	0.0	66.6
C TOTAL		13.1	50.5	37.9	19.5	17.2	61.0	13.8	30.9	243.9
ASM	OS	4.5	0.7	2.6	3.5	0.9	0.0	0.0	0.0	12.1
	STSV	0.0	0.2	0.2	0.1	0.1	0.0	0.0	0.0	0.6
	USE	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	NOS	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	SM	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	DSAR	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	MODB	0.0	0.0	1.0	0.0	0.0	0.0	0.0	0.0	1.0
ASM TOTAL		4.5	0.9	3.8	3.6	1.0	0.0	0.0	0.0	13.7
COTS	OS	61.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	61.0
	STSV	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	USE	268.0	14.3	3.1	0.0	0.0	0.0	0.0	1.6	287.1
	NOS	0.0	55.6	0.0	23.8	0.0	0.0	0.0	0.0	79.4
	SM	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	DSAR	0.0	0.0	0.0	0.0	0.0	19.4	0.0	0.0	19.4
	MODB	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
COTS TOTAL		329.0	69.9	3.1	23.8	0.0	19.4	0.0	1.6	446.8
OTHER	OS	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	STSV	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	USE	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	NOS	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	SM	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	DSAR	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	MODB	0.0	0.0	2.0	0.0	0.0	0.0	0.0	0.0	2.0
OTHER TOTAL		0.0	0.0	2.0	0.0	0.0	0.0	0.0	0.0	2.0
TOTAL CUSTOM		35.7	77.3	97.0	73.6	103.5	107.0	35.2	37.2	566.4
TOTAL COTS		329.0	69.9	3.1	23.8	0.0	19.4	0.0	1.6	446.8
DMS TOTAL		364.7	147.2	100.1	97.4	103.5	126.4	35.2	38.8	1013.2

LEGEND:

- (thin box) R4 Functions reviewed at DDR3.2 and DDR4. Some development may occur in R3.2 timeframe
- (thin oval) NOS Engineering Release - not delivered to field until R4
- (thick oval) NOS R4 Development - Not delivered until R4
- (thick box) USE functions developed for R5, may not be delivered until MB5

Table 2.3-2. Hardware Modeling Parameters

	CPU	Local Bus	Global Bus	MSU	MDM	Dedicated I/O
CPU Speed with Baseline Instr. Mix	X			X	X	
RAM Size	X				X	
Backplane Bus Latency	X					
Interrupt Latency (Priority/Normal)	X					
DMA Latency	X	X	X		X	X
Mass Storage Size				X		
Mass Storage Read Latency				X		
Mass Storage Write Latency				X		
Define Data Busses and Dedicated I/O Channels by Type (Discrete, Analog, Digital)		X	X		X	X
Bus/Channel Media Latency		X	X		X	X
Message length		X	X			
Number of Connections		X	X			
Response Time of RTs/Hosts		X	X			
Protocol (Message) Overhead(ISO/OSI, TCP/IP, 1553, etc.)		X	X			
Bus/Channel Hardware Physical Interface Latency		X	X		X	X
Bus/Channel Throughput Rates		X	X		X	X
Bus/Channel Interface Unit Processing Latency		X	X		X	X
CPU Service Time Latency	X	X	X		X	X
Data Word Overhead		X	X			
Buffer Capacity		X	X			
Maximum Token Hold/Hand Off Delays			X			
Scan Rate(I/O Operations per sec)/Sampling Rate					X	X
On-Demand Scan Processing Latency					X	X

Table 2.3-3 defines the performance parameters that should be input to the model to define the system loading and performance requirements. This table addresses the expected performance of the system to be evaluated/modeled, the sizing and performance parameters of the software required to perform the required task scenarios for the system to be modeled and the expected data system loading for the system to be modeled. Software sizing and performance and hardware loading requirements for the Space Station DMS are expected to be extracted from the "DMS Resource Model" as discussed in Section 3.2. Custom software tasking models for specific Space Station DMS tasks to be modeled may be built as required by using the Appendix A "SDP Performance Measurements/Projections and Constants.". The model input parameters for other systems will most likely be different from the Space Station and will require definition prior to input to the model.

Table 2.3-4 defines the recommended model outputs in order to evaluate system performance regardless of the particular system being evaluated.

2.3.4.2 System Performance Requirements

Tables 2.3-5(A), (B), and (C) from reference 1 page 3-210 allocates performance requirements from the system level to DMS software CSCIs and also has a column for H/W CIs that is mostly TBD.

2.3.4.3 DMS Estimated/Measured Performance

DMS software performance data has been gathered from a multitude of sources and is summarized in Appendix A. The majority of the data in Appendix A was extracted from Reference 4, the "DMS Resource Model." The data in Reference 4 consists of mostly measured data with some estimates. The data source is referenced along with each constant. The data in reference 4 was measured on a 3.1 MIP EDP. The data in Appendix A was modified to more closely approximate the new 3.9 MIP EDP by the ratio multiplier of 3.9/3.1 to give a new estimated latency.

Measurements are yet to be made on the 3.9 MIP EDP. Data that was not included in Reference 4, but was from another source is identified by an * and the source identified. Source documents on how to use the data in Appendix A to calculate system performance are Reference Documents 4B,7, 9 and 13 as defined in Appendix B.

Table 2.3-3. DMS Performance Model Input Parameters

	CPU	Local Bus	Global Bus	MSU	MDM	Dedicated I/O
Task Software Size(SLOCS/FLOPS)	X			X	X	
Task Software Execution Rate	X			X	X	
Task Software Complexity	X			X	X	
Number and Identity of Concurrent Tasks	X				X	
Service Software Processing Overhead	X			X	X	
Processing/Response Latency by Task (Tailored to Application Program Requirements See Appendix A)	X			X	X	
Task I/O Rates by Channel/Bus(Sample Data, TM Data, Journaling Data to Data Base, Task to Task Communications)	X	X	X	X	X	X
Protocol Type(1553, ISO/OSI, etc.)	X	X	X	X	X	X
Bus Throughput Rate Requirements by Service Class and Message Priority	X	X	X	X		
Mass Memory File Accesses Size/Rates	X		X	X		
Task Program Mass Memory Storage Requirements	X			X		
Measurements In by Sample Rate, Type(analog/digital/discrete) and Size	X				X	X
Special Measurement Processing Requirements (Engineering Unit Conversion, etc.)	X				X	X
Commands Out by Rate and Type	X				X	
Context/Task Switch Latency	X					
Exception Handling Latency	X	X	X	X	X	

Table 2.3-4. DMS Performance Model Outputs

- CPU Utilization in KIPs by Task
- CPU Total Utilization in KIPs by Task
- RAM Utilization Requirements by Task in Kbytes
- RAM Total Utilization Requirements in Kbytes
- CPU Task Response Latency
- Bus Loading by Task by Bus(Global and/or Local)
- Total Bus Loading by Bus(Global and/or Local)
- Scan Latency by Special Processing Requirement Type (Engineering Unit Conversion, etc.)
- Scan Latency Digital Data
- Scan Latency Discrete Data
- Global Bus Bi-directional Throughput
- Local Bus Bi-directional Throughput
- Message Arrival Time Latency
- Mass Storage Utilization by Task
- Mass Storage Total Utilization
- File Retrieval Latency (Local)
- File Retrieval Latency (Remote)
- Dedicated I/O Channel Loading

Table 2.3-5(A). DMS System Performance Allocation Matrix

DMS Function	CEI Paragraph	Requirement Description	System Performance Value	3.7.2.1 OS/Ada RTE	3.7.2.2 NOS	3.7.2.3 USE	3.7.2.4 Std Svcs	3.7.2.5 DSAR	3.7.2.6 SM	3.7.2.8 HCAS	3.7.2.9 MODBM	3.7.2.10 MDM Svcs	3.7.2.11 MDM Ada RTE	3.7.1.X HWCI
User Information	3.2.1.1.1.q	DMS time contributing to end-to-end response time for any system or element to accept and execute authorized ground-originated override or inhibit commands of any automated function, exclusive of ground to space communication delays..	<0.5 seconds	<TBD seconds	<TBD seconds	(N/A)	<TBD seconds	(N/A)	(N/A)	(N/A)	(N/A)	<TBD seconds	<TBD seconds	(N/A)
Global Communi-cation	3.2.1.1.1.1.1.d	Emergency (priority 1) message transfer latency between onboard DMS application program interface (with no greater than 1 Mbps of emergency traffic).	Avg <20 ms 95% <25 ms	Avg <4 ms 95% <5 seconds	Avg <16 ms 95% <20 seconds	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)
Global Communi-cation	3.2.1.1.1.1.1.d	Expedited (priority 2) message transfer latency between onboard DMS application program interfaces (with no greater than 1 Mbps of exxpedited traffic).	Avg <20 ms 95% <25 ms	Avg <4 ms 95% <5 seconds	Avg <16 ms 95% <20 seconds	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)
Global Communi-cation	3.2.1.1.1.1.1.d	Normal (priority 3) message transfer latency between onboard DMS application program interfaces.	Avg <50ms 95% <80 ms	Avg <4 ms 95% <6 seconds	Avg <46 ms 95% <74 seconds	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)
Global Communi-cation	3.2.1.1.1.1.1.d	Background (priority 4) message transfer latency between onboard DMS application program interfaces.	Avg <80 ms 95% <150 ms	Avg <4 ms 95% <7 seconds	Avg <76 ms 95% <143 seconds	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)
Global Communi-cation	3.2.1.1.1.1.1.j	Response for delivery of emergency or expecited messages from DMS network function until receiving process notification.	Avg ≤5 msec 95% ≤10 msec	TBD	TBD	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)
Processing Environ-ment	3.2.1.1.1.2.j	Time to suspend a task due to an external event.	≤1 ms	<1 ms	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	≤1 ms	(N/A)
Input/ Output Manage-ment	3.2.1.1.1.2.3.1.f	Delay time from when an application process requests data from a multiplexer/demulti-plexer to when the data is returned to the application process for predefined synchronous I/O.	Avg ≤10 ms 95% ≤20 ms	AVG ≤1 ms 95% ≤20 ms	(N/A)	(N/A)	Avg ≤9 ms 95% ≤18 ms	(N/A)	(N/A)	(N/A)	(N/A)	Avg ≤1 ms 95% ≤1 ms	(N/A)	TBD

Table 2.3-5(B). DMS System Performance Allocation Matrix

DMS Function	CEI Paragraph	Requirement Description	System Performance Value	3.7.2.1 OS/Ada RTE	3.7.2.2 NOS	3.7.2.3 USE	3.7.2.4 Std Svcs	3.7.2.5 DSAR	3.7.2.6 SM	3.7.2.8 HCAS	3.7.2.9 MODBM	3.7.2.10 MDM Svcs	3.7.2.11 MDM Ada RTE	3.7.1.X HWCI
Input/ Output Management	3.2.1.1.1.2.3.1.g	Delay time from when an applicaiton process requests data from a multiplexer/demultiplexer to when the data is returned to the application process for a single aperiodic request.	Avg ≤50 ms 95% ≤85ms	Avg ≤1 ms 95% ≤2 ms	(N/A)	(N/A)	AVG <22 ms 95% <37 ms	(N/A)	(N/A)	(N/A)	(N/A)	Avg ≤22 ms 95% ≤37 ms	(N/A)	TBD
Human/ Computer Interface	3.2.1.1.1.4.h	Response time to pass authorized crew-entered command inputs to the appropriate system/element.	≤0.5 second	≤.02 seconds	≤.42 seconds	≤12.5 ms	≤12.5 ms	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	TBD
Human/ Computer Interface	3.2.1.1.1.4.j	Time between initiation of a display screen request and a response to the operator that his request is being processed.	≤2.50 ms avg ≤500 ms 95%	Avg ≤1 ms 95% ≤1 ms	(N/A)	Avg ≤2.50 ms 95% ≤500 ms	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	TBD
Input Device Functions	3.2.1.1.1.4.3.c.3	Latency between hand controller command initiation to availability at the local bus interface.	≤25 msec	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	≤12.5 msec	(N/A)	(N/A)	(N/A)	(N/A)
Mass Storage Data Management	3.2.1.1.1.5.4.3.h	Data retrieval of up to 2048 bytes from an open file on mass storage.	Avg ≤200 ms 95% 300 ms	Avg ≤50 ms 95% ≤75 ms	Avg <145 ms 95% <217 ms	(N/A)	(N/A)	Avg <5 ms 95% <7.5 ms	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	TBD
Mass Storage Data Management	3.2.1.1.1.5.4.3.l	Data write of up to 2048 bytes into a file on mass storage.	Avg ≤200 ms 95% 300 ms	Avg ≤50 ms 9% <75 ms	Avg ≤145 ms 95% ≤217 ms	(N/A)	(N/A)	Avg ≤5 ms 95% ≤7.5 ms	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	TBD
Initialization/Shutdown	3.2.1.1.2.1.f	DMS initialization time from a cold start to a condition permitting control and monitoring of systems and elements.	15 minutes	TBD	TBD	TBD	TBD	TBD	TBD	TBD	(N/A)	<60 seconds	TBD	TBD
Fault Detection, Isolation and Recovery	3.2.1.1.2.6.c	System safing response, following loss of essential communicaiton for greater than 5 seconds.	≤5 seconds	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	(N/A
Fault Detection, Isolation and Recovery	3.2.1.1.2.6.d	Availability of system status and configuration changes for crew viewing, downlink to ground, and ISE.	≤1 second	≤TBD seconds	≤TBD seconds	(N/A)	≤TBD seconds	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)
Fault Detection, Isolation and Recovery	3.2.1.1.2.6.g	Response time to accept and execute crew override or inhibit commands of automated funcitons.	≤1 second	(N/A)	TBD	TBD	TBD	(N/A)	TBD	(N/A)	(N/A)	TBD	(N/A)	(N/A)

Table 2.3-5(C). DMS System Performance Allocation Matrix

DMS Function	CEI Paragraph	Requirement Description	System Performance Value	3.7.2.1 OS/Ada RTE	3.7.2.2 NOS	3.7.2.3 USE	3.7.2.4 Std Svcs	3.7.2.5 DSAR	3.7.2.6 SM	3.7.2.8 HCAS	3.7.2.9 MODBM	3.7.2.10 MDM Svcs	3.7.2.11 MDM Ada RTE	3.7.1.X HWCI
Fault Detection, Isolation and Recovery	3.2.1.1.2.6.h	Response time to accept and execute ground-originated override or inhibit commands of automated functions.	≤1 second	(N/A)	TBD	TBD	TBD	(N/A)	TBD	(N/A)	(N/A)	TBD	(N/A)	(N/A)
Redun-dancy Manage-ment	3.2.1.1.2.6.1.g.2	Error recovery using the cold backup technique from the detection and isolation of the error until the backup ORU begins executing the interrupted function.	≤60 second	TBD	TBD	TBD	TBD	TBD	TBD	(N/A)	(N/A)	TBD	TBD	TBD
Redun-dancy Manage-ment	3.2.1.1.2.6.1.g.4	Error recovery using the warm backup technique from the detection and isolation of the error until the backup ORU begins executing the interrupted function.	≤5 seconds	TBD	TBD	TBD	TBD	TBD	TBD	(N/A)	(N/A)	TBD	TBD	TBD
Caution and Warning	3.2.1.1.2.6.3.b	Warning alarm annunciation latency after occurrence of the warning conditon.	≤0.5 second	≤440 ms	≤33 ms	≤23 ms	≤4 ms	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	TBD
Caution and Warning	3.2.1.1.2.6.3.c	Caution alarm annu ciation latency after detection of the caution condition.	≤0.5 second	≤440 ms	≤33 ms	≤23 ms	≤4 ms	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	TBD
Caution and Warning	3.2.1.1.2.6.3.d	Emergency alarm annunciation latency after detection of the emergency condition.	≤0.5 second	≤440 ms	≤23 ms	≤4 ms	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	(N/A)	3.7.1.26 EMADS: TBD

3. PROCESSING ALLOCATIONS AND LOADING

Section 3.1 provides the ground rules for allocation of the DMS resources to itself and to applications including processor utilization limitation limits from Preliminary Design Review (PDR) through Flight Readiness Review (FRR), discusses common allocations of hardware unit capacities to satisfy DMS and user requirements, allocation of the DMS resources by type and by mission build stage to all applications and the allocation of SDP Resources to specific WP-2 Applications.

Section 3.2 1 provides summaries extracted from Reference #4A Rev. 2 of the best estimates presently available of the DMS loading from MB-2 to MTC at a application(task) level. Section 3.2.2 provides the SDP load calculations for Work Package (WP)-1, WP-4 and CSA in depth. The load calculations for the WP-2 applications, Guidance, Navigation and Control (GN&C), External Active Thermal Control System (EATCS), and Communications and Tracking (C&T), in Section 3.2.2.1 are presented at a detailed level by function with the Secondary Electrical Power System (SEPS) and Rotary Joint System (RJS) being very approximate. Similarly, detailed load calculations for WP-1 are presented in Section 3.2.2.2, CSA in Section 3.2.2.3 and WP-4 in Section 3.2.2.4. Note that for all of these load calculations, CPU loading is based on measurement of the operations as defined in Appendix A using a 3.1 MIP SDP. The present EDP is a 3.9 MIP CPU, but measurements have not yet been made on a 3.9 MIP EDP CPU. To approximately compensate for this speed change in calculation of CPU loading until new measurements are made, the processing times for the number of instructions required for an operation was decreased by the ratio of 3.1/3.9 in Reference 4A Rev. 2 "DMS Resource Model" calculations. DMS self usage calculations are presented at the summary level in Tables 3.2-1, 3.2-2 and 3.2-3. No detailed DMS calculations are presented in 3.2.2 as any DMS usage service requirements dependent on system loading are allocated to the specific application using the service. Section 3.3 provides MDM allocation and loading estimates.

3.1 RESOURCE ALLOCATION

3.1.1 ALLOCATION GROUND RULES (from Reference Document #3 Rev. 2)

Processing resources are allocated to provide resources for all identified applications. In addition, these allocations are limited to less than processor capacity to provide for the growth in resource usage requirements that normally occurs during the development phase of a program. The resource margin (the difference between the projected usage and the allocation) is used to identify potential resource over commitments. The DMS is allocated 15% of the memory and 5% of the CPU utilizable capacity in the application EDPs.

Table 3.1-1 lists the worst case instantaneous utilization limits as defined in Reference #1 and Reference 3 Rev. 2.

The allocations apply to usage by DMS as well as the system application software developed by the work packages and the CSA. Resources required by the DMS for its own purpose (e.g. status messages, heartbeats, basic RODB Tables and ISO Associations) are bookkept against the DMS. The allocations to the application software include any resources (such as local bus I/O interrupts, RODB accesses and OS configuration data, etc.) provided by DMS on behalf of the application software.

Table 3.1-1. Processor Utilization Limits by Development Milestone

RESOURCE	PDR	CDR	FRR (PMC)
Processor-Based Memory	50%	65%	85%
CPU Capacity	50%	50%	65%
Mass Storage	50%	65%	85%
Local Bus Throughput	50%	65%	85%

3.1.2 COMMON ALLOCATIONS

Section 4.2 of Reference 3 Rev. 2 defines the common resource allocations and processing capacities for the various categories of DMS provided processors. For convenience, these allocations are shown below in Table 3.1-2. This table defines the total processor capacity, the allocable capacity corresponding to the present PDR time frame, the allocation to DMS and the user allocable resource capacity. Since no model presently exists for estimating application software usage of MPACs, NIUs, BIUs, Bridges and Gateways, the total allocable capacities are allocated to the DMS. Specific processor allocations to DMS, work packages and the CSA are provided in paragraph 3.1.3 and 3.1.4.

Table 3.1-2. Common Allocations

	CPU CAPACITY (measured in KIPS)				RAM CAPACITY (measure in KBytes)			
	Total Capacity	Allocable Capacity	DMS Allo-cation	User Allocable	Total Capacity	Allocable Capacity	DMS Alloca-tion	User Allocable
Appl EDP	3,900	1,950	195	1,755	16,084	8,042	2,458	5,584
NIU (NOS EDP)	3,100	1,550	1,550	-	4,096	2,048	2,048	-
BIU	1,000	500	500	-	256	128	128	-
MDM	1,600	800	480	320	2,048	1,024	350	674
Bridge	3,100	1,550	1,550	-	4,096	2,048	2,048	-
Gateway	3,100	1,550	1,550	-	4,096	2,048	2,048	-

In the case of the MDMs, there are two types of processor based memory, EEPROM and RAM. MDM RAM allocation was defined in Table 3.1-2 above. MDM EEPROM is limited to a 75% utilization of a 1024 Kbyte capacity. Specific allocations are shown in Table 3.1-3.

Table 3.1-3: Common MDM EEPROM Allocations (measured in Kbytes)

	Available Capacity	Allocable Capacity	DMS Allocation	User Allocable
MDM	1,024	768	350	418

Table 3.1-4 defines the mass storage allocations for the core systems MSUs. On stages 2-4 the DMS and applications software loads only require 150 Mbytes out of the 400 Mbyte capacity. The remaining 250 Mbytes of storage capacity are allocable for ZOE recording. As defined in the DMS Architecture Control Document (ACD), the mass storage allocation to DMS is fixed at 50 Mbytes from MB-2 onward for the core systems MSUs.

Table 3.1-4. **Common Mass Storage Capacity** (measured in Mbytes)

Stages	Total Capacity	Allocation for Operations	Available Capacity	Allocable Capacity	DMS Allocation	User Allocable
2 thru 4	400	250	150	75	50	25
MTC	400	TBD	TBD	TBD	50	TBD
PMC	400	TBD	TBD	TBD	50	TBD

3.1.3 INDIVIDUAL ALLOCATIONS (from Reference Document #3 Rev. 2)

Table 3.1-5 lists the CPU allocations for the MB-2 SDP, the 2-FT SDP, the 1-FT SDP, the Payload SDP, the MSS SDP and all of the MSUs to the WP's, CSA, Charles Stark Draper Laboratory (CSDL), Operations Planning System (OPS) and DMS. In Table 3.1-6, the RAM allocations are defined for the same set of processors. The allocations of MB-2 SDP and MB-2 MSU capacities only apply to MB-2 through MB-4 as these resources are not presently planned for use after MB-4. A complete rational for all of the allocations in these tables can be found in paragraph 4.3 of Reference 3 Rev. 2.

CPU capacities available for allocation at PDR time are provided in Table 3.1-2.

The RAM allocations in Table 3.1-6 to DMS for the 2-FT SDP and the 1-FT SDP include the "fixed" allocations of 2,458 Kbytes plus 350 Kbytes for the Network SM portion of the DMS System Manager. The RAM allocations on the 2-FT SDP and the 1-FT SDP are the same because software functions for all core systems are loaded and remain memory resident when any of the SDPs (1-4) is powered on.

It should also be noted that the allocations of RAM capacity do not account for the Integrated Station Executive (ISE) as the ISE requirements are TBD. When ISE is resolved, the allocations will be modified to include ISE.

The CPU allocations in Table 3.1-5 to DMS for the 2-FT SDP include the fixed allocation of 195 KIPS plus the additional CPU capacity required to perform the Network SM function.

For the Mission Support System (MSS) SDP, Draper Labs is allowed 300 Kbytes for Timeliner and the remaining allocable RAM capacity is available to CSA for their software and Timeliner procedures. In terms of the allocable CPU capacity, DMS receives the fixed allocation of 195 KIPS and the remaining capacity is allocated to CSA for the MSS applications processing load and the execution of any Timeliner procedures.

3.1.4 ALLOCATION OF SDP RESOURCES TO WP-2

(from Reference Document #4A Rev. 2)

Table 3.1-7 is the recommended allocation of CPU resources to the various WP-2 applications. This allocation is somewhat arbitrary and not presently binding.

Table 3.1-5. CPU Allocations (measured in KIPS)

Processor	WP-1	WP-2	WP-4	CSA	CSDL	OPS	DMS	Total Allocable
MB-2 SDP	105	1,355	295	—	—	—	195	1,950
MB-2 MSU	—	—	—	—	—	TBD	TBD	1,950
2FT SDP	—	1,376	310	—	—	—	264	1,950
1FT SDP	1,678	77	—	TBD	—	—	195	1,950
MSU 1 (Stage 5)	—	TBD	—	—	—	TBD	TBD	1,950
MSU 2 (Stage 5)	—	—	—	—	—	TBD	TBD	1,950
MSUs 1 & 2 (MTC onward)	—	TBD	—	—	—	TBD	TBD	1,950
Payload SDP7	1,755	—	—	—	—	—	195	1,950
Payload MSU	TBD	—	—	—	—	—	TBD	1,950
ZOE MSU	—	—	—	—	—	—	1,950	1,950
MSS SDP11	—	—	—	1,755	—	—	195	1,950

Table 3.1-6. RAM Allocations (measured in Kbytes)

Processor	WP-1	WP-2	WP-4	CSA	CSDL	OPS	DMS	Total Allocable
MB-2 SDP	2,264	2,188	654	128	—	—	2,808	8,042
MB-2 MSU	—	—	—	—	300	TBD	TBD	8,042
2FT SDP	2,264	2,188	654	128	—	—	2,808	8,042
1FT SDP	2,264	2,188	654	128	—	—	2,808	8,042
MSUs 1 & 2	—	TBD	—	—	300	TBD	TBD	8,042
Payload SDP	5,584	—	—	—	—	—	2,458	8,042
Payload MSU	—	—	—	—	300	TBD	TBD	8,042
ZOE MSU	—	—	—	—	—	—	8,042	8,042
MSS SDP	—	—	—	5,248	300	—	2,458	8,042

Table 3.1-7. WP-2 Resource Allocations, KIPS

SDP	MB-2	2-FT at MB-5	1 FT at MB-5
GN&C	803	840	
C&T	75	75	25
EATCS	80	80	
RJS	150	150	
SEPS	137	137	
CHeCS	25	25	25
MTE	25	25	
ISE	25	25	25
UIL	25	25	

3.2 SDP LOADING

The "SDP & MDM Resource Model" has been used to estimate the current resource loading for the SDPs through MB-5(MTC). The loading is summarized in this section with the detailed summary estimates by application presented in Section 3.2.2

3.2.1 SDP RESOURCE MODEL LOADING SUMMARY BY APPLICATION
(from Reference Document #4A Rev. 2)

Tabulated in this section are the current estimated loading requirements for the SDPs. Input data to the resource model is based on surveys of DMS users. Section 5.0 of Reference Document #4A Rev. 2 contains printouts of the detailed survey input data. This data is being constantly refined. Surveys for SEPS and RJS are incomplete resulting in the data included being very approximate.

a. Table 3.2-1 shows the summary estimated resource requirements for MB 2-4. The CPU usage is 2157 KIPS, 55% of capacity and 111% of allocation.

b. Table 3.2-2 shows the summary estimated resource requirements for MB-5 (MTC) for the 2-FT SDP. The CPU usage is 3194 KIPS, 82% of capacity and 164% of allocation.

c. Table 3.2-3 shows the summary estimated resource requirements for MB-5 (MTC) for the 1-FT SDP. The CPU usage is 1246 KIPS, 32% of capacity and 58% of allocation.

Table 3.2-1. MB 2-4 Resources

Item	CPU, KIPS	Memory, KB	TM Kbps	Notes
DMS	195	2400	.5	from R2 data
ISE	0	300	0	see 3.2.2.1.6
GN & C	1021	669	58.9	see 3.2.2.1.2
C&T ACS	22	152	2.2	see 3.2.2.1.3
RJS	300	150	TBD	see 3.2.2.1.5
SEPS	200	170	16.0	see 3.2.2.1.7
CHeCS	20	100	2	see 3.2.2.1.8
UIL	0	600	0	see 3.2.2.1.9
WP-1	105	100	9.0	see 3.2.2.2; GCA on MB-4
WP-4	294	378	20.0	see 3.2.2.4
CSA	(363)	128	6.0	see 3.2.2.3; MSS c/o on MB-3
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WP-2 Total	1563	2141	79	132% of CPU Allocation
Net Totals	2157	5019	109	111% of CPU Allocation

Table 3.2-2. MB-5 2-FT SDP Resource Loading Requirements

Item	CPU, KIPS	Memory, KB	TM Kbps	Notes
DMS	195	2400	.5	from R2 data
Net SM	117	350	.5	estimated
ISE	0	TBD	0	Design TBD
GN & C	1596	772	58.9	see 3.2.2.1.2
C&T ACS/SGS	80	170	4.4	see 3.2.2.1.3
EATCS	396	170	4.4	see 3.2.2.1.4: MB-8
RJS	300	150	TBD	see 3.2.2.1.5
SEPS	200	200	16.0	see 3.2.2.1.7
CHeCS		100		see 3.2.2.1.8
UIL		600		see 3.2.2.1.9
WP-1		2156		see 3.2.2.2
WP-4	310	530	21.0	see 3.2.2.4
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WP-2 Total	2572	2162	84	186% of CPU Allocation
Net Totals	3194	7598	106	164% of CPU Allocation

Table 3.2-3. MB-5 1-FT SDP Resource Loading Requirements

Item	CPU, KIPS	Memory, KB	TM Kbps	Notes
DMS	195	2400	.5	
Net SM		350		
ISE	0	TBD	0	
GN & C		1100		
C&T Video	25	150	2.0	see 3.2.2.1.3
EATCS		170		
RJS		150		
SEPS		200		
CHeCS	50	100	6.0	
UIL	0	600		
WP-1	105	100	9.0	
WP-1	871	2056	48.8	see 3.2.2.2; MB-6
WP-4		530		
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WP-1 Total	976	2156	58	58% of CPU Allocation
Net Totals	1246	7598	66	64% of CPU Allocation

3.2.2 SDP RESOURCE MODEL LOADING SUMMARY FOR EACH APPLICATION
(from Reference Document #4A Rev. 2)

Included in this section are the detailed MB-2 through MB-5 SDP loading summaries for WP-2, WP-1, CSA and WP-4 application software.

3.2.2.1 WP-2 Model Results

A detailed resource requirements/loading summary is provided in the following paragraphs for each WP-2 application as of 11/10/92.

3.2.2.1.1 DMS and Net SM Model Results

DMS self usage calculations are presented at the summary level in Section 3.2.1 with no detail calculations presented in this section.

3.2.2.1.2 GN&C Model Results

GN&C resources were calculated for a MB-5 re-boost scenario, comprised of 3 Inertial Sensor Assemblies (ISAs), 2 Star Trackers (STs), 4 Primary Propulsion Modules (PPMs), and 4 Control Moment Gyros (CMGs). The results of these calculations are shown in Table 3.2-5. CPU was calculated at 1596 KIPS of which FLOPS consumed 298 KIPS. FLOPS processing for GN&C was estimated by the MDSSC MOODS model. A breakdown of GN&C SLOCs by sub-task and processing required for FLOPS expressed in KIPS is contained in Table 3.2-4.

The model data for the preceding scenario was then modified to the MB-2 configuration consisting of 2 ISAs, 1 ST, 2 PPMs and 0 CMGs. The results of these calculations are shown in Table 3.2-6. CPU was calculated to be 1021 KIPS. This is only an approximation as FLOPS were not adjusted to account for the reduced hardware set supported and the differences between OI1 and OI2 software releases were not considered.

Table 3.2-4. GN&C FLOPS/SLOCs KIPS Estimates

System	KSLOCS	FLOPS(KIPS)
Exec.	3	none
Att. Det.	78	187
Att. Cntl.	41	17
P&S	16	66
Guidance	15	13
Nav.	13	15
GN&C PPC	8	0

Table 3.2-5. MB-5 GN&C DMS Resource Requirements(REVG_MB5.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System:	GN&C
Company:	IBM
POINT OF CONTACT:	KEITH CULLEY/8720
DMS Point of Contact:	
Assembly Sequence:	
Mode:	

Summary Information
Totals

RAM (KB)	771.59
Non-FLOPS Proc. (KIPS)	1297.98
FLOPS Proc. (KIPS)	298.00
Total Proc. (KIPS)	1595.98
Mass Storage (KB)	519.69
Bus Throughput (Kbps)	51.28
NIU Throughput (Kbps)	104.00
Unique SLOCs	17323

Statistics

NIU Throughput (Msgs/Sec)	0.01
Bus Throughput (Msgs/Sec)	0.12
Bus Throughput (Meas/Sec)	5.50
Worst Case Task Rate (Hz)	5.00
Average Task Rate (Hz)	0.62

Sensor Summary		451.52
Discretes	2584	
Analogs	672	
16-bit fixed	152	
32-bit fixed	18	
32-bit floats	0	
64-bit fixed	0	
poly eucs	788	
piece eucs	0	

Effector Summary		243.15
Discretes	75	
Analogs	0	
16-bit fixed	54	
32-bit fixed	9	
32-bit floats	0	
64-bit fixed	0	
ploy eucs	63	
piece eucs	0	

Telemetry Summary	35.89
Journalling Summary	18.27
Attribute I/O Summary	274.49

EDP RAM (KBytes)

Ada Executable	519.69
Heap Size	0.00
Stack Size	1.95
EDP Local Dir	0.00
EDP Op. Attr.	0.00
EDP Component	0.00
Action I/O Queue	0.00
Journalling Table	0.12
TOL Table	3.92
Handle Size	67.71
Scan Table	171.30
Control Table	6.90

Non-FLOPS Proc. (KIPS)

Ada Non-FLOPS	175.76
Task Overhead	7.74
Inner Loop Byte	87.07
Inner Loop Bit	0.00
Outer Loop	72.23
NIU/MBII	78.26
Other STSV	25.42
Remote Rd/Wr	65.68
Cond.Conv.	0.00
Action Write	0.00
Action Read	0.00
Response Read	0.00
Response Write	0.00
BIU/MBII	91.15
Journalling	0.00
Scan Meas.	160.05
Scan Message	22.82
Scan	41.16
Polynomial EUC	226.50
Piecewise Linear	0.00
Event	0.00
Data Derivation	0.00
Control Meas.	20.76
Control Message	7.12
Control	215.26

FLOPS Proc. (KIPS)

Unary FLOPS	0.00
Complex FLOPS	0.00

Mass Memory (KB)

Ada	519.69
Local Directory	0.00
Op. Attr. Table	0.00
Component Table	0.00
Files	0.00

NIU Throughput (Kbps)

Attribute Journalling	18.95
Attribute Telemetry	58.88
Attribute I/O	26.17
Action I/O	0.00

NIU Throughput (Msgs/Sec)

Attribute Journalling	0.00
Attribute Telemetry	0.00
Attribute I/O	0.01
Action I/O	0.00

Bus Throughput (Kbps)

Action I/O	0.00
Scan Lists	43.96
Control Lists	7.32

Bus Throughput (Msgs/Sec)

Action I/O	0.00
Scan Lists	0.09
Control Lists	0.03

Bus Throughput (Meas/Sec)

Scan Lists	5.27
Control Lists	0.23

Table 3.2-6. MB-2 GN&C DMS Resource Requirements(REVG_MB2.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System:	GN&C
Company:	IBM
POINT OF CONTACT:	KEITH CULLEY/8720
DMS Point of Contact:	
Assembly Sequence:	
Mode: 2 ISA, 1 ST, 2 PPM, 0 CMG	

Summary Information Totals

RAM (KB)	668.84
Non-FLOPS Proc. (KIPS)	723.49
FLOPS Proc. (KIPS)	298.00
Total Proc. (KIPS)	1021.49
Mass Storage (KB)	519.69
Bus Throughput (Kbps)	21.23
NIU Throughput (Kbps)	104.00
Unique SLOCs	17323

Statistics

NIU Throughput (Msgs/Sec)	0.01
Bus Throughput (Msgs/Sec)	0.04
Bus Throughput (Meas/Sec)	2.36
Worst Case Task Rate (Hz)	5.00
Average Task Rate (Hz)	0.62

Sensor Summary 184.04

Discretes	1149
Analogs	224
16-bit fixed	71
32-bit fixed	12
32-bit floats	0
64-bit fixed	0
poly eucs	280
piece eucs	0

Effector Summary 17.31

Discretes	24
Analogs	0
16-bit fixed	23
32-bit fixed	6
32-bit floats	0
64-bit fixed	0
ploy eucs	29
piece eucs	0

Telemetry Summary	35.89
Journalling Summary	18.27
Attribute I/O Summary	274.49

EDP RAM (KBytes)

Ada Executable	519.69
Heap Size	0.00
Stack Size	1.95
EDP Local Dir	0.00
EDP Op. Attr.	0.00
EDP Component	0.00
Action I/O Queue	0.00
Journalling Table	0.12
TOL Table	3.92
Handle Size	67.71
Scan Table	72.80
Control Table	2.65

Non-FLOPS Proc. (KIPS)

Ada Non-FLOPS	156.89
Task Overhead	7.74
Inner Loop Byte	87.07
Inner Loop Bit	0.00
Outer Loop	72.23
NIU/MBII	78.26
Other STSV	25.42
Remote Rd/Wr	65.68
Cond.Conv.	0.00
Action Write	0.00
Action Read	0.00
Response Read	0.00
Response Write	0.00
BIU/MBII	28.85
Journalling	0.00
Scan Meas.	65.32
Scan Message	9.18
Scan	42.16
Polynomial EUC	67.38
Piecewise Linear	0.00
Event	0.00
Data Derivation	0.00
Control Meas.	2.33
Control Message	1.09
Control	13.89

FLOPS Proc. (KIPS)

Unary FLOPS	0.00
Complex FLOPS	0.00

Mass Memory (KB)

Ada	519.69
Local Directory	0.00
Op. Attr. Table	0.00
Component Table	0.00
Files	0.00
	0.00

NIU Throughput (Kbps)

Attribute Journalling	18.95
Attribute Telemetry	58.88
Attribute I/O	26.17
Action I/O	0.00

NIU Throughput (Msgs/Sec)

Attribute Journalling	0.00
Attribute Telemetry	0.00
Attribute I/O	0.01
Action I/O	0.00

Bus Throughput (Kbps)

Action I/O	0.00
Scan Lists	18.76
Control Lists	2.47

Bus Throughput (Msgs/Sec)

Action I/O	0.00
Scan Lists	0.04
Control Lists	0.00

Bus Throughput (Meas/Sec)

Scan Lists	2.34
Control Lists	0.03

3.2.2.1.3 WP-2 C&T Model Results

The C&T resources for MB-2 is comprised of only the Assembly-Contingency-Sub-System (ACS) for S-band. No audio is active so the full ACS bandwidth is available for data. ACS CPU processing is estimated to be 22 KIPS. Table 3.2-7 is a summary of the estimated SDP loading from C&T ACS for MB-2.

At MB-5, ACS is joined by the Space-to Ground Subsystem (SGS) for KU-band in the 2-FT SDP. SGS CPU processing is estimated to be 58 KIPS The total KIPS for MB-5 is equal to the sum of ACS(Table 3.2-7) and SGS (Table 3.2-8) for a total of 80 KIPS.

For the 1-FT SDP the total C&T processing load is estimated to be 25 KIPS. The scenario consists of 4 video cameras.

Table 3.2-7. C&T, 2-FT-ACS Resource Requirements(REVG_CT2.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System:	C&T, 2FT - ACS
Company:	GE
POINT OF CONTACT:	
DMS Point of Contact:	
Assembly Sequence:	
Mode:	

Summary Information Totals

RAM (KB)	151.58
Non-FLOPS Proc. (KIPS)	21.90
FLOPS Proc. (KIPS)	0.00
Total Proc. (KIPS)	21.90
Mass Storage (KB)	155.90
Bus Throughput (Kbps)	1.82
NIU Throughput (Kbps)	2.25
Unique SLOCs	4806

Statistics

NIU Throughput (Msgs/Sec)	0.00
Bus Throughput (Msgs/Sec)	0.01
Bus Throughput (Meas/Sec)	0.07
Worst Case Task Rate (Hz)	1.00
Average Task Rate (Hz)	0.10

Sensor Summary	7.87
Discretes	6
Analogs	0
16-bit fixed	63
32-bit fixed	0
32-bit floats	0
64-bit fixed	0
ploy eucs	0
piece eucs	0

Effector Summary	2.10
Discretes	0
Analogs	0
16-bit fixed	4
32-bit fixed	0
32-bit floats	0
64-bit fixed	0
poly eucs	4
piece eucs	0

Telemetry Summary	0.40
Journalling Summary	0.00
Attribute I/O Summary	5.69

EDP RAM (KBytes)

Ada Executable	144.18
Heap Size	0.00
Stack Size	3.54
EDP Local Dir	0.00
EDP Op. Attr.	0.00
EDP Component	0.00
Action I/O Queue	0.00
Journalling Table	0.01
TOL Table	0.15
Handle Size	0.05
Scan Table	3.45
Control Table	0.20

Non-FLOPS Proc. (KIPS)

Ada Non-FLOPS	3.70
Task Overhead	0.93
Inner Loop Byte	0.48
Inner Loop Bit	0.00
Outer Loop	5.61
NIU/MBII	0.00
Other STSV	0.00
Remote Rd/Wr	0.00
Cond.Conv.	0.00
Action Write	0.00
Action Read	0.00
Response Read	0.00
Response Write	0.00
BIU/MBII	1.23
Journalling	0.00
Scan Meas.	4.72
Scan Message	2.03
Scan	1.05
Polynomial EUC	0.06
Piecewise Linear	0.00
Event	0.00
Data Derivation	0.00
Control Meas.	0.06
Control Message	0.05
Control	1.98

FLOPS Proc. (KIPS)

Unary FLOPS	0.00
Complex FLOPS	0.00

Mass Memory (KB)

Ada	144.18
Local Directory	0.00
Op. Attr. Table	0.00
Component Table	0.00
Files	11.72

NIU Throughput (Kbps)

Attribute Journalling	0.00
Attribute Telemetry	2.25
Attribute I/O	0.00
Action I/O	0.00

NIU Throughput (Msgs/Sec)

Attribute Journalling	0.00
Attribute Telemetry	0.00
Attribute I/O	0.00
Action I/O	0.00

Bus Throughput (Kbps)

Action I/O	0.00
Scan Lists	1.79
Control Lists	0.03

Bus Throughput (Msgs/Sec)

Action I/O	0.00
Scan Lists	0.01
Control Lists	0.00

Bus Throughput (Meas/Sec)

Scan Lists	0.07
Control Lists	0.00

Table 3.2-8. C&T, 2-FT-SGS Resource Requirements(REVG_CT1.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System:	C&T, 2FT - SGS
Company:	GE
POINT OF CONTACT:	
DMS Point of Contact:	
Assembly Sequence:	
Mode:	

Summary Information
Totals

RAM (KB)	19.15
Non-FLOPS Proc. (KIPS)	58.41
FLOPS Proc. (KIPS)	0.00
Total Proc. (KIPS)	58.41
Mass Storage (KB)	13.86
Bus Throughput (Kbps)	2.70
NIU Throughput (Kbps)	2.18
Unique SLOCs	462

Statistics

NIU Throughput (Msgs/Sec)	0.00
Bus Throughput (Msgs/Sec)	0.01
Bus Throughput (Meas/Sec)	0.10
Worst Case Task Rate (Hz)	1.00
Average Task Rate (Hz)	1.00

Sensor Summary		19.94
Discretes	18	
Analogs	0	
16-bit fixed	72	
32-bit fixed	0	
32-bit floats	0	
64-bit fixed	0	
poly eucs	0	
piece eucs	0	

Effector Summary		10.48
Discretes	0	
Analogs	0	
16-bit fixed	4	
32-bit fixed	0	
32-bit floats	0	
64-bit fixed	0	
ploy eucs	4	
piece eucs	0	

Telemetry Summary	0.43
Journalling Summary	0.00
Attribute I/O Summary	13.72

EDP RAM (KBytes)

Ada Executable	13.86
Heap Size	0.00
Stack Size	0.30
EDP Local Dir	0.00
EDP Op. Attr.	0.00
EDP Component	0.00
Action I/O Queue	0.00
Journalling Table	0.00
TOL Table	0.11
Handle Size	0.17
Scan Table	4.50
Control Table	0.20

Non-FLOPS Proc. (KIPS)

Ada Non-FLOPS	3.70
Task Overhead	0.93
Inner Loop Byte	0.63
Inner Loop Bit	0.00
Outer Loop	13.52
NIU/MBII	0.00
Other STSV	0.00
Remote Rd/Wr	0.00
Cond.Conv.	0.00
Action Write	0.00
Action Read	0.00
Response Read	0.00
Response Write	0.00
BIU/MBII	9.21
Journalling	0.00
Scan Meas.	6.11
Scan Message	2.98
Scan	10.54
Polynomial EUC	0.31
Piecewise Linear	0.00
Event	0.00
Data Derivation	0.00
Control Meas.	0.31
Control Message	0.25
Control	9.92

FLOPS Proc. (KIPS)

Unary FLOPS	0.00
Complex FLOPS	0.00

Mass Memory (KB)

Ada	13.86
Local Directory	0.00
Op. Attr. Table	0.00
Component Table	0.00
Files	0.00

NIU Throughput (Kbps)

Attribute Journalling	0.00
Attribute Telemetry	2.18
Attribute I/O	0.00
Action I/O	0.00

NIU Throughput (Msgs/Sec)

Attribute Journalling	0.00
Attribute Telemetry	0.00
Attribute I/O	0.00
Action I/O	0.00

Bus Throughput (Kbps)

Action I/O	0.00
Scan Lists	2.56
Control Lists	0.14

Bus Throughput (Msgs/Sec)

Action I/O	0.00
Scan Lists	0.01
Control Lists	0.00

Bus Throughput (Meas/Sec)

Scan Lists	0.09
Control Lists	0.00

3.2.2.1.4 EATCS Model Results

No CPU Resources are required for Thermal Conditioning System (TCS) prior to MB-5.

The calculations shown in Table 3.2-9 are for MB-8. At MB-8, 3 TCS loops become available. The scenario used for the calculations has 2 Low Temp Loops active and the Medium Temp Loop in start-up. The CPU processing requirements calculated are 396 KIPS, of which 200 KIPS are estimated for the Radiator pointing calculations.

3.2.2.1.5 RJS - TBD

No detailed estimates are available. Estimated resource requirements in Section 3.2.1 should be used until detailed estimates become available.

3.2.2.1.6 ISE

No cyclic transfers required. Code size of about 10,000 SLOCS. At 30 Bytes per SLOC, 300 Mbytes of memory are required. CPU processing requirements are TBD.

3.2.2.1.7 SEPS

No detailed estimates are available. Estimated resource requirements in Section 3.2.1 should be used until detailed estimates become available.

3.2.2.1.8 Crew Health Care System (CHeCS) Data

Resource requirements are summarized in Section 3..2.1. Binary Data Transfer (BDT) is used to send data from the CHeCS ORU to the SDP for transfer on to the MSU.

For MB-2 a block of 4 Kbytes will be sent every 30 seconds. MB-2 CPU processing is estimated to be 20 KIPS.

For MB-5, 2 blocks of 4 Kbytes will be sent every 30 seconds plus about 100 Bits/second for Fault Detection, Isolation and Recovery (FDIR).

Software size of 100 Kbytes is estimated to be sufficient.

Telemetry consists of 2 Kbps at MB-2 increasing to 6 Kbps at MB-5.

Table 3.2-9: EATCS Resource Model Requirements(MB-8)(REVG_TCS.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System:	EATCS
Company:	
POINT OF CONTACT:	
DMS Point of Contact:	
Assembly Sequence:	
Mode:	

Summary Information Totals

RAM (KB)	170.56
Non-FLOPS Proc. (KIPS)	169.96
FLOPS Proc. (KIPS)	26.32
Total Proc. (KIPS)	396.28
Mass Storage (KB)	147.78
Bus Throughput (Kbps)	5.88
NIU Throughput (Kbps)	6.37
Unique SLOCs	4926

Statistics

NIU Throughput (Msgs/Sec)	0.00
Bus Throughput (Msgs/Sec)	0.01
Bus Throughput (Meas/Sec)	0.42
Worst Case Task Rate (Hz)	1.00
Average Task Rate (Hz)	0.00

Sensor Summary 77.67

Discretes	216
Analogs	204
16-bit fixed	0
32-bit fixed	0
32-bit floats	0
64-bit fixed	0
poly eucs	204
piece eucs	0

Effector Summary 0.00

Discretes	0
Analogs	0
16-bit fixed	0
32-bit fixed	0
32-bit floats	0
64-bit fixed	0
ploy eucs	0
piece eucs	0

Telemetry Summary	18.90
Journalling Summary	11.04
Attribute I/O Summary	43.18

EDP RAM (KBytes)

Ada Executable	147.78
Heap Size	0.00
Stack Size	0.24
EDP Local Dir	0.00
EDP Op. Attr.	0.00
EDP Component	0.00
Action I/O Queue	0.00
Journalling Table	0.02
TOL Table	1.19
Handle Size	0.33
Scan Table	21.00
Control Table	0.00

Non-FLOPS Proc. (KIPS)

Ada Non-FLOPS	12.11
Task Overhead	0.93
Inner Loop Byte	3.65
Inner Loop Bit	9.89
Outer Loop	16.49
NIU/MBII	18.41
Other STSV	12.40
Remote Rd/Wr	12.28
Cond.Conv.	0.00
Action Write	0.00
Action Read	0.00
Response Read	0.00
Response Write	0.00
BIU/MBII	6.14
Journalling	0.00
Scan Meas.	17.36
Scan Message	2.23
Scan	10.54
Polynomial EUC	47.53
Piecewise Linear	0.00
Event	0.00
Data Derivation	0.00
Control Meas.	0.00
Control Message	0.00
Control	0.00

FLOPS Proc. (KIPS)

Unary FLOPS	5.40
Complex FLOPS	4.50

Mass Memory (KB)

Ada	147.78
Local Directory	0.00
Op. Attr. Table	0.00
Component Table	0.00
Files	0.00

NIU Throughput (Kbps)

Attribute Journalling	0.44
Attribute Telemetry	4.35
Attribute I/O	1.58
Action I/O	0.00

NIU Throughput (Msgs/Sec)

Attribute Journalling	0.00
Attribute Telemetry	0.00
Attribute I/O	0.00
Action I/O	0.00

Bus Throughput (Kbps)

Action I/O	0.00
Scan Lists	5.88
Control Lists	0.00

Bus Throughput (Msgs/Sec)

Action I/O	0.00
Scan Lists	0.01
Control Lists	0.00

Bus Throughput (Meas/Sec)

Scan Lists	0.42
Control Lists	0.00

3.2.2.1.9 UIL Data

The UIL/Timeliner estimate assumes that the calling system is charged for the processing used, so the UIL KIPS will be zero.

3.2.2.2 WP-1 Model Results

The MB-4 CPU processing required is estimated to be 105 KIPS.

Following lab installation, the WP-1 sub-systems modeled are Air Revitalization System(ARS), Atmospheric Control & Supply Subsystem(ACSS), Electrical Power System (EPS), Fire Detection & Suppression System(FDS), Internal Thermal Control System (ITCS), Mixed Waste Gas Subsystem(MWS), SM and Water Recovery & Management Subsystem (WRM). Table 3.2-10 contains a summary of the calculation for WP-1. The MB-6 usage determined for these system is 871 KIPS.

3.2.2.3 CSA Model Results

The MB-3 CSA usage determined for the MSS checkout is 363 KIPS for non-cyclic checkout.

As shown in Table 3.2-11 the MB-6 CSA usage determined is 2480 KIPS. This software runs on SDP-11 to be installed with MB-5.

3.2.2.4 WP-4 Model Results

3.2.2.4.1 MB-2 Worst Case

The overall WP-4 CPU processing requirements for a worst case scenario that includes diagnostic processing is shown in Table 3.2-12 and is calculated to be 294 KIPS.

3.2.2.4.2 MTC Normal Operations

The nominal WP-4 CPU processing requirements at MB-5 is calculated to be 310 KIPS as shown in Table 3.2-13.

Table 3.2-10. WP-1 Resource Requirements(REVG_WP1.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System:	WP1
Company:	Boeing
POINT OF CONTACT:	
DMS Point of Contact:	
Assembly Sequence:	
Mode:	

Summary Information
Totals

RAM (KB)	2056.05
Non-FLOPS Proc. (KIPS)	839.09
FLOPS Proc. (KIPS)	31.43
Total Proc. (KIPS)	870.52
Mass Storage (KB)	801.44
Bus Throughput (Kbps)	61.23
NIU Throughput (Kbps)	57.13
Unique SLOCs	18393

Statistics

NIU Throughput (Msgs/Sec)	0.01
Bus Throughput (Msgs/Sec)	174.00
Bus Throughput (Meas/Sec)	2122
Worst Case Task Rate (Hz)	2.07
Average Task Rate (Hz)	0.63

Sensor Summary 488.37

Discretes	1306
Analogs	481
16-bit fixed	2030
32-bit fixed	100
32-bit floats	0
64-bit fixed	0
poly eucs	203
piece eucs	177

Effector Summary 4.59

Discretes	503
Analogs	73
16-bit fixed	462
32-bit fixed	1
32-bit floats	0
64-bit fixed	0
ploy eucs	49
piece eucs	0

Telemetry Summary	178.57
Journalling Summary	3.05
Attribute I/O Summary	50.36

EDP RAM (KBytes)

Ada Executable	863.94
Heap Size	0.00
Stack Size	18.36
EDP Local Dir	160.02
EDP Op. Attr.	384.62
EDP Component	243.63
Action I/O Queue	3.06
Journalling Table	9.42
TOL Table	20.13
Handle Size	6.97
Scan Table	278.95
Control Table	66.95

Non-FLOPS Proc. (KIPS)

Ada Non-FLOPS	24.50
Task Overhead	4.54
Inner Loop Byte	66.08
Inner Loop Bit	0.02
Outer Loop	53.53
NIU/MBII	37.20
Other STSV	75.16
Remote Rd/Wr	0.00
Cond.Conv.	0.00
Action Write	50.74
Action Read	10.60
Response Read	0.00
Response Write	0.00
BIU/MBII	15.21
Journalling	8.54
Scan Meas.	265.95
Scan Message	36.93
Scan	8.55
Polynomial EUC	31.14
Piecewise Linear	145.27
Event	0.54
Data Derivation	0.00
Control Meas.	1.81
Control Message	0.43
Control	2.36

FLOPS Proc. (KIPS)

Unary FLOPS	24.50
Complex FLOPS	6.92

Mass Memory (KB)

Ada	18.36
Local Directory	160.02
Op. Attr. Table	384.62
Component Table	238.44
Files	0.00

NIU Throughput (Kbps)

Attribute Journalling	4.08
Attribute Telemetry	48.81
Attribute I/O	0.00
Action I/O	4.24

NIU Throughput (Msgs/Sec)

Attribute Journalling	0.00
Attribute Telemetry	0.01
Attribute I/O	0.00
Action I/O	0.00

Bus Throughput (Kbps)

Action I/O	4.86
Scan Lists	56.01
Control Lists	0.36

Bus Throughput (Msgs/Sec)

Action I/O	14.00
Scan Lists	158.00
Control Lists	2.00

Bus Throughput (Meas/Sec)

Scan Lists	2107
Control Lists	15

Table 3.2-11. Mobile Servicing System Resource Requirements(SDPG1.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System: Mobile Servicing System
Company: SPAR Aerospace Ltd.
POINT OF CONTACT: Ed Brewer, N. Tripathy (SPAR), Don Peterson (C)
DMS Point of Contact:
Assembly Sequence:
Mode:

Summary Information Totals

RAM (KB)	1211.06
Non-FLOPS Proc. (KIPS)	2480.82
FLOPS Proc. (KIPS)	0.02
Total Proc. (KIPS)	2480.84
Mass Storage (KB)	5739.39
Bus Throughput (Kbps)	170.32
NIU Throughput (Kbps)	62.95
Unique SLOCs	32515

Statistics

NIU Throughput (Msgs/Sec)	0.05
Bus Throughput (Msgs/Sec)	0.38
Bus Throughput (Meas/Sec)	7.96
Worst Case Task Rate (Hz)	20.00
Average Task Rate (Hz)	8.67

Sensor Summary		892.05
Discretes	850	
Analogs	0	
16-bit fixed	1481	
32-bit fixed	116	
32-bit floats	0	
64-bit fixed	0	
poly eucs	0	
piece eucs	0	

Effector Summary		221.42
Discretes	18	
Analogs	0	
16-bit fixed	36	
32-bit fixed	0	
32-bit floats	0	
64-bit fixed	0	
poly eucs	0	
piece eucs	0	

Telemetry Summary	587.98
Journalling Summary	0.00
Attribute I/O Summary	544.30

EDP RAM (KBytes)

Ada Executable	975.45
Heap Size	0.00
Stack Size	2.21
EDP Local Dir	70.87
EDP Op. Attr.	3.84
EDP Component	19.64
Action I/O Queue	3.93
Journalling Table	0.01
TOL Table	5.39
Handle Size	4.67
Scan Table	122.35
Control Table	2.70

Non-FLOPS Proc. (KIPS)

Ada Non-FLOPS	3.18
Task Overhead	48.36
Inner Loop Byte	167.52
Inner Loop Bit	384.38
Outer Loop	130.60
NIU/MBII	150.99
Other STSV	292.64
Remote Rd/Wr	6.14
Cond.Conv.	0.00
Action Write	0.00
Action Read	14.68
Response Read	0.00
Response Write	0.00
BIU/MBII	159.59
Journalling	9.27
Scan Meas.	640.14
Scan Message	88.54
Scan	163.37
Polynomial EUC	0.00
Piecewise Linear	0.00
Event	0.00
Data Derivation	0.00
Control Meas.	18.06
Control Message	4.96
Control	198.40

FLOPS Proc. (KIPS)

Unary FLOPS	0.02
Complex FLOPS	0.00

Mass Memory (KB)

Ada	975.45
Local Directory	70.87
Op. Attr. Table	3.84
Component Table	112.13
Files	4577.10

NIU Throughput (Kbps)

Attribute Journalling	0.00
Attribute Telemetry	57.46
Attribute I/O	5.05
Action I/O	0.44

NIU Throughput (Msgs/Sec)

Attribute Journalling	0.00
Attribute Telemetry	0.05
Attribute I/O	0.00
Action I/O	0.00

Bus Throughput (Kbps)

Action I/O	0.00
Scan Lists	165.52
Control Lists	4.80

Bus Throughput (Msgs/Sec)

Action I/O	0.00
Scan Lists	0.36
Control Lists	0.02

Bus Throughput (Meas/Sec)

Scan Lists	7.74
Control Lists	0.22

Table 3.2-12. WP-4 Electrical Power System MB-2 Worst Case Processing Load (WP4MB2.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System: Electric Power System
Company: Rocketdyne Date: 10/21/92
POINT OF CONTACT: Zarik Boghossian, Tin Nguyen
DMS Point of Contact: WP-04
Assembly Sequence: MB-02
Mode: SAFE
Comment: Worst Case; Including Diagnostic Telemetry
Date: 11/3/92

Summary Information Totals	
RAM (KB)	377.63
Non-FLOPS Proc. (KIPS)	208.39
FLOPS Proc. (KIPS)	85.63
Total Proc. (KIPS)	294.02
Mass Storage (KB)	255.66
Bus Throughput (Kbps)	31.19
NIU Throughput (Kbps)	21.16
Unique SLOCs	8400

Statistics

NIU Throughput (Msgs/Sec)	0.00
Bus Throughput (Msgs/Sec)	49.20
Bus Throughput (Meas/Sec)	1133
Worst Case Task Rate (Hz)	1.00
Average Task Rate (Hz)	0.24

Sensor Summary	93.89
Discretes	0
Analogs	993
16-bit fixed	34
32-bit fixed	105
32-bit floats	0
64-bit fixed	0
poly eucs	0
piece eucs	0

Effector Summary	10.26
Discretes	0
Analogs	0
16-bit fixed	0
32-bit fixed	1
32-bit floats	0
64-bit fixed	0
poly eucs	0
piece eucs	0

Telemetry Summary	63.09
Journalling Summary	0.00
Attribute I/O Summary	10.41

EDP RAM (KBytes)	
Ada Executable	252.00
Heap Size	0.00
Stack Size	16.60
EDP Local Dir	3.66
EDP Op. Attr.	0.00
EDP Component	32.77
Action I/O Queue	6.92
Journalling Table	0.01
TOL Table	8.50
Handle Size	0.53
Scan Table	56.60
Control Table	0.05

Non-FLOPS Proc. (KIPS)	
Ada Non-FLOPS	14.20
Task Overhead	1.12
Inner Loop Byte	26.36
Inner Loop Bit	8.78
Outer Loop	10.55
NIU/MBII	9.21
Other STSV	18.60
Remote Rd/Wr	0.00
Cond.Conv.	0.00
Action Write	7.44
Action Read	0.00
Response Read	0.00
Response Write	0.00
BIU/MBII	6.14
Journalling	1.85
Scan Meas.	76.96
Scan Message	11.66
Scan	5.27
Polynomial EUC	0.00
Piecewise Linear	0.00
Event	0.00
Data Derivation	0.00
Control Meas.	0.09
Control Message	0.25
Control	9.92

FLOPS Proc. (KIPS)	
Unary FLOPS	85.63
Complex FLOPS	0.00

Mass Memory (KB)	
Ada	252.00
Local Directory	3.66
Op. Attr. Table	0.00
Component Table	0.00
Files	0.00

NIU Throughput (Kbps)	
Attribute Journalling	0.00
Attribute Telemetry	20.46
Attribute I/O	0.00
Action I/O	0.70

NIU Throughput (Msgs/Sec)	
Attribute Journalling	0.00
Attribute Telemetry	0.00
Attribute I/O	0.00
Action I/O	0.00

Bus Throughput (Kbps)	
Action I/O	0.43
Scan Lists	30.32
Control Lists	0.44

Bus Throughput (Msgs/Sec)	
Action I/O	1.20
Scan Lists	47.00
Control Lists	1.00

Bus Throughput (Meas/Sec)	
Scan Lists	1132
Control Lists	1

Table 3.2-13. WP-4 Electrical Power System MB-5(MTC) Nominal Processing Load (WP4MTCN.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System: Electric Power System
Company: Rocketdyne Date: 10/20/92
POINT OF CONTACT: Zarik Boghossian, Tin Nguyen
DMS Point of Contact: WP-04
Assembly Sequence: MTC
Mode: Safe
Comment: Normal Case; No Diagnostic Telemetry
Date: 11/3/92

Summary Information Totals

RAM (KB)	530.13
Non-FLOPS Proc. (KIPS)	224.54
FLOPS Proc. (KIPS)	85.63
Total Proc. (KIPS)	310.17
Mass Storage (KB)	278.78
Bus Throughput (Kbps)	33.27
NIU Throughput (Kbps)	21.66
Unique SLOCs	8400

Statistics

NIU Throughput (Msgs/Sec)	0.00
Bus Throughput (Msgs/Sec)	58.20
Bus Throughput (Meas/Sec)	1356
Worst Case Task Rate (Hz)	1.00
Average Task Rate (Hz)	0.24

Sensor Summary	96.70
Discretes	352
Analogs	815
16-bit fixed	0
32-bit fixed	216
32-bit floats	0
64-bit fixed	0
poly eucs	0
piece eucs	0

Effector Summary	10.94
Discretes	0
Analogs	0
16-bit fixed	0
32-bit fixed	3
32-bit floats	0
64-bit fixed	0
poly eucs	0
piece eucs	0

Telemetry Summary	63.02
Journalling Summary	0.00
Attribute I/O Summary	23.13

EDP RAM (KBytes)

Ada Executable	252.00
Heap Size	0.00
Stack Size	16.60
EDP Local Dir	26.78
EDP Op. Attr.	0.00
EDP Component	136.90
Action I/O Queue	20.30
Journalling Table	0.01
TOL Table	8.22
Handle Size	1.52
Scan Table	67.65
Control Table	0.15

Non-FLOPS Proc. (KIPS)

Ada Non-FLOPS	14.20
Task Overhead	1.12
Inner Loop Byte	33.97
Inner Loop Bit	10.53
Outer Loop	13.85
NIU/MBII	9.21
Other STSV	18.60
Remote Rd/Wr	0.00
Cond.Conv.	0.00
Action Write	7.44
Action Read	0.00
Response Read	0.00
Response Write	0.00
BIU/MBII	6.14
Journalling	1.85
Scan Meas.	78.04
Scan Message	13.39
Scan	5.27
Polynomial EUC	0.00
Piecewise Linear	0.00
Event	0.00
Data Derivation	0.00
Control Meas.	0.28
Control Message	0.74
Control	9.92

FLOPS Proc. (KIPS)

Unary FLOPS	85.63
Complex FLOPS	0.00

Mass Memory (KB)

Ada	252.00
Local Directory	26.78
Op. Attr. Table	0.00
Component Table	0.00
Files	0.00

NIU Throughput (Kbps)

Attribute Journalling	0.00
Attribute Telemetry	20.46
Attribute I/O	0.00
Action I/O	0.70

NIU Throughput (Msgs/Sec)

Attribute Journalling	0.00
Attribute Telemetry	0.00
Attribute I/O	0.00
Action I/O	0.00

Bus Throughput (Kbps)

Action I/O	
Scan Lists	0.43
Control Lists	31.52

Bus Throughput (Msgs/Sec)

Action I/O	1.20
Scan Lists	54.00
Control Lists	3.0

Bus Throughput (Meas/Sec)

Scan Lists	1353
Control Lists	3.0

3.2.2.4.3 MTC Worst Case

The worst case WP-4 CPU processing requirements at MB-5 including diagnostics is calculated to be 361 KIPS as shown in Table 3.2-14.

Table 3.2-14. Electrical Power System MB-5 Worst Case Processing Load (WP4MTCW.XLS)

DMS Resource Requirement Model - Rev. G.1
11/10/92

System: Electric Power System
Company: Rocketdyne Date: 10/20/92
POINT OF CONTACT: Zarik Boghossian, Tin Nguyen
DMS Point of Contact: WP-04
Assembly Sequence: MTC
Mode: Safe
Comment: WorstCase; Including Diagnostic Telemetry
Date: 11/3/92

Summary Information Totals

RAM (KB)	544.36
Non-FLOPS Proc. (KIPS)	275.41
FLOPS Proc. (KIPS)	85.63
Total Proc. (KIPS)	361.04
Mass Storage (KB)	278.78
Bus Throughput (Kbps)	44.15
NIU Throughput (Kbps)	29.85
Unique SLOCs	8400

Statistics

NIU Throughput (Msgs/Sec)	0.00
Bus Throughput (Msgs/Sec)	69.20
Bus Throughput (Meas/Sec)	1537
Worst Case Task Rate (Hz)	1.00
Average Task Rate (Hz)	0.24

Sensor Summary	127.11
Discretes	0
Analogs	1079
16-bit fixed	34
32-bit fixed	199
32-bit floats	0
64-bit fixed	0
poly eucs	0
piece eucs	0

Effector Summary	10.94
Discretes	0
Analogs	0
16-bit fixed	0
32-bit fixed	3
32-bit floats	0
64-bit fixed	0
poly eucs	0
piece eucs	0

Telemetry Summary	83.48
Journalling Summary	0.00
Attribute I/O Summary	23.13

EDP RAM (KBytes)

Ada Executable	252.00
Heap Size	0.00
Stack Size	16.60
EDP Local Dir	26.78
EDP Op. Attr.	0.00
EDP Component	136.90
Action I/O Queue	20.30
Journalling Table	0.01
TOL Table	13.40
Handle Size	1.52
Scan Table	76.70
Control Table	0.15

Non-FLOPS Proc. (KIPS)

Ada Non-FLOPS	14.20
Task Overhead	1.12
Inner Loop Byte	44.16
Inner Loop Bit	20.79
Outer Loop	13.85
NIU/MBII	9.21
Other STSV	18.60
Remote Rd/Wr	0.00
Cond.Conv.	0.00
Action Write	7.44
Action Read	0.00
Response Read	0.00
Response Write	0.00
BIU/MBII	6.14
Journalling	1.85
Scan Meas.	105.72
Scan Message	16.12
Scan	5.27
Polynomial EUC	0.00
Piecewise Linear	0.00
Event	0.00
Data Derivation	0.00
Control Meas.	0.28
Control Message	0.74
Control	9.92

FLOPS Proc. (KIPS)

Unary FLOPS	85.63
Complex FLOPS	0.00

Mass Memory (KB)

Ada	252.00
Local Directory	26.78
Op. Attr. Table	0.00
Component Table	0.00
Files	0.00

NIU Throughput (Kbps)

Attribute Journalling	0.00
Attribute Telemetry	29.14
Attribute I/O	0.00
Action I/O	0.70

NIU Throughput (Msgs/Sec)

Attribute Journalling	0.00
Attribute Telemetry	0.00
Attribute I/O	0.00
Action I/O	0.00

Bus Throughput (Kbps)

Action I/O	0.43
Scan Lists	42.40
Control Lists	1.32

Bus Throughput (Msgs/Sec)

Action I/O	1.20
Scan Lists	65.00
Control Lists	3.00

Bus Throughput (Meas/Sec)

Scan Lists	1534
Control Lists	3

3.3 <u>MDM INDIVIDUAL ALLOCATIONS AND LOADING ESTIMATES</u>

In the event that detailed modeling of MDMs is required, the following data is presented. Sufficient loading data input to the SDPs from the MDMs located on the local busses is presented in section 3.2 to allow SDP loading analysis. Evaluation of known MDM loading by use of the Reference 4 DMS Resource Model has determined that there is only one case where the allocated capacity at PDR is exceeded and that is the MDM LA #4 (formerly MDM 6-4) where CPU usage is estimated to be 55% of capacity (see Table 3.3-1).

3.3.1 ALLOCATIONS AND SUMMARY LOADING

Tables 3.3-1, 3.3-2 and 3.3-3 extracted from Reference 3 Rev. 2A define the allocations of CPU, RAM and EEPROM capacities respectively. The CPU and RAM allocations are made at the 50% level, while the EEPROM is allocated at 75% of the total capacity. For all three resource types a fixed allocation to DMS to account for Ada RTE and MDM Services is made for each MDM.

Within the tables, MDMs with identical software loads (including IODB objects) are grouped together. MDMs with allocations to more than one work package are considered to be shared MDMs. If a WP has instrumentation associated with an MDM, but no software, it is assumed that the CPU capacity required for I/O of that instrumentation is included within the fixed DMS allocation of 480 KIPs. Both the "old" and "new" (after implementation of Reference 2 Rev. 1) architecture's are provided to facilitate the transition to the revised nomenclature defined in Reference 2 Rev. 1. There are TBDs in some of the tables with regard to MDMs shared by WP-1 and WP-2 as WP-1 still is to provide usage estimated for any MDMs that arrive after MTC.

Table 3.3-1. MDM CPU Allocations vs. Usage Estimates

MDMs	WP-1 Alloc.	WP-1 Usage	WP-2 Alloc.	WP-2 Usage	WP-4 Alloc.	WP-4 Usage	CSA Alloc.	CSA Usage	DMS	Total Usage	% Usage
UBA MDMs #1 and #2	--	--	320	21	--	--	--	--	480	501	31
PM1,2,5,6 #1 and #2	--	--	320	187	--	--	--	--	480	667	42
PMA1 #1	TBD	TBD	TBD	14	--	--	--	--	480	494	31
N2 #3	320	177	--	--	--	--	--	--	480	657	41
N2 #1 and N2 #2	--	--	320	6	--	--	--	--	480	486	30
S3 #3 and S3 #4	--	--	--	--	320	TBD	--	--	480	480	30
S1 #1 and S1 #2	--	--	320	26	--	--	--	--	480	506	32
S3 #5 and S3 #6	--	--	320	52	--	--	--	--	480	532	33
S2 #2 and S2 #3	--	--	320	6	--	--	--	--	480	486	30
S3 #1 and S3 #2	--	--	320	20	--	--	--	--	480	500	31
S2 #1	--	--	320	6	--	--	--	--	480	486	30
S1 #3	--	--	320	32	--	--	--	--	480	512	32
S1 #4	--	--	320	38	--	--	--	--	480	518	32
M1 #5 and M1 #6	--	--	320	77	--	--	TBD	TBD	480	557	35
LA #5 and LA #6	--	--	320	TBD	--	--	--	--	480	480	30
S4 #1	--	--	32	20	288	177	--	--	480	677	42
S4 #2	--	--	--	--	320	177	--	--	480	657	41
M1 #1 thru M1 #3	--	--	41	6	279	41	--	--	480	527	33
M1 #4	--	--	--	--	320	41	--	--	480	521	33
N2 #4	320	208	--	--	--	--	--	--	480	688	43
LA #1	320	122	--	--	--	--	--	--	480	602	38
LA #2	320	209	--	--	--	--	--	--	480	689	43
LA #3	320	207	--	--	--	--	--	--	480	687	43
LA #4	320	399	--	--	--	--	--	--	480	879	55

Table 3.3-2. MDM RAM Allocations vs. Usage Estimates

MDMs	WP-1		WP-2		WP-4		CSA		DMS	Total Usage	% Usage
	Alloc.	Usage	Alloc.	Usage	Alloc.	Usage	Alloc.	Usage			
UBA MDMs #1 and #2	--	--	674	39	--	--	--	--	350	389	19
PM1,2,5,6 #1 and #2	--	--	674	87	--	--	--	--	350	437	21
PMA1 #1	TBD	TBD	TBD	28	--	--	--	--	350	378	18
N2 #3	674	242	--	--	--	--	--	--	350	592	29
N2 #1 and N2 #2	--	--	674	22	--	--	--	--	350	372	18
S3 #3 and S3 #4	--	--	--	--	674	TBD	--	--	350	350	17
S1 #1 and S1 #2	--	--	674	43	--	--	--	--	350	393	19
S3 #5 and S3 #6	--	--	674	103	--	--	--	--	350	453	22
S2 #2 and S2 #3	--	--	674	22	--	--	--	--	350	372	18
S3 #1 and S3 #2	--	--	674	21	--	--	--	--	350	371	18
S2 #1	--	--	674	22	--	--	--	--	350	372	18
S1 #3	--	--	674	33	--	--	--	--	350	383	19
S1 #4	--	--	674	55	--	--	--	--	350	405	20
M1 #5 and M1 #6	--	--	674	277	--	--	TBD	TBD	350	627	31
LA #5 and LA #6	--	--	674	TBD	--	--	--	--	350	350	17
S4 #1	--	--	91	51	583	327	--	--	350	728	36
S4 #2	--	--	--	--	674	327	--	--	350	677	33
M1 #1 thru M1 #3	--	--	60	22	614	245	--	--	350	617	30
M1 #4	--	--	--	--	674	245	--	--	350	595	29
N2 #4	674	250	--	--	--	--	--	--	350	600	29
LA #1	674	231	--	--	--	--	--	--	350	581	28
LA #2	674	241	--	--	--	--	--	--	350	591	29
LA #3	674	253	--	--	--	--	--	--	350	603	29
LA #4	674	302	--	--	--	--	--	--	350	652	32

Table 3.3-3. MDM EEPROM Allocations vs. Usage Estimates

MDMs	WP-1 Alloc.	WP-1 Usage	WP-2 Alloc.	WP-2 Usage	WP-4 Alloc.	WP-4 Usage	CSA Alloc.	CSA Usage	DMS	Total Usage	% Usage
UBA MDMs #1 and #2	--	--	418	39	--	--	--	--	350	389	38
PM1,2,5,6 #1 and #2	--	--	418	87	--	--	--	--	350	437	43
PMA1 #1	TBD	TBD	TBD	28	--	--	--	--	350	378	37
N2 #3	418	242	--	--	--	--	--	--	350	592	58
N2 #1 and N2 #2	--	--	418	22	--	--	--	--	350	372	36
S3 #3 and S3 #4	--	--	--	--	418	TBD	--	--	350	350	34
S1 #1 and S1 #2	--	--	418	43	--	--	--	--	350	393	38
S3 #5 and S3 #6	--	--	418	103	--	--	--	--	350	453	44
S2 #2 and S2 #3	--	--	418	22	--	--	--	--	350	372	36
S3 #1 and S3 #2	--	--	418	21	--	--	--	--	350	371	36
S2 #1	--	--	418	22	--	--	--	--	350	372	36
S1 #3	--	--	418	33	--	--	--	--	350	383	37
S1 #4	--	--	418	55	--	--	--	--	350	405	40
M1 #5 and M1 #6	--	--	418	277	--	--	TBD	TBD	350	627	61
LA #5 and LA #6	--	--	418	TBD	--	--	--	--	350	350	34
S4 #1	--	--	56	51	362	327	--	--	350	728	71
S4 #2	--	--	--	--	418	327	--	--	350	677	66
M1 #1 thru M1 #3	--	--	37	22	381	245	--	--	350	617	60
M1 #4	--	--	--	--	418	245	--	--	350	595	58
N2 #4	418	250	--	--	--	--	--	--	350	600	59
LA #1	418	231	--	--	--	--	--	--	350	581	57
LA #2	418	241	--	--	--	--	--	--	350	591	58
LA #3	418	253	--	--	--	--	--	--	350	603	59
LA #4	418	302	--	--	--	--	--	--	350	652	64

3.3.2 MDM Processor Utilization Estimates

Tables 3.3-4(A) through 3.3-4(G) provide utilization estimates by MDM. The tables provide for all known MDMs through PMC. The MDMs that are present at each stage of the mission build can be selected from the overall set of MDMs provided. The utilization of an MDM is not expected to change once installed. Shown are the software tasks by MDM, the function performed by each task and the memory, processor, mass storage and local bus utilization by task.

Table 3.3.-4(A). MDM Processor Utilization Estimates

11/9/92

WORK PACKAGE	SYSTEM/ELEMENTS	FUNCTION	MEMORY (KB)	PROCESSOR (KIPS)	MASS STORAGE (KB)	LOCAL BUS UTILIZATION (KBPS)
	MDM AL #1	TOTAL	356	482	0	1
2	MDM SERVICES	MDM SERVICES +Ada RTE+UAS Services	350	480	0	0
2	EVAS	Extra Vehicular Activity System	4	1	0	1
2	DMS C&W	Caution and Warning	0	1	0	0
1	ITCS, ECLSS	Internal Thermal Control + Environmental Control				
2	PTCS	Passive Internal Control System	2	0	0	0
	MDM AL #2	TOTAL	354	481	0	1
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
2	EVAS	Extra Vehicular Activity System	4	1	0	1
1	ECLSS	Enviornmental Control & Life Support System				
	MDM HA #1	TOTAL	350	480	0	0
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
1	ITC, ECLSS	Internal Thermal Control_Environmental Control				
	MDM HA #2	TOTAL	350	481	0	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
1	ITCS, ECLSS	Internal Thermal Control + Environmental Control				
2	DMS C&W	Caution and Warning	0	1	0	0
	MDM HA #3	TOTAL	350	480	0	0
2	MDM SERVICES	MDM SERVICES+AdaRTE +UAS Services	350	480	0	0
1	ITCS, ECLSS	Internal Thermal Control+Environmental Control				
	MDM HA #4	TOTAL	350	480	0	0
2	MDM SERVICES	MDM SERVICES_Ada +UAS Services	350	480	0	0
1	ITCS, ECLSS, MS	Internal Thermal Control+Environmental+Manned				
	MDM LA #1	TOTAL	581	602	48	10
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
1	ITCS, LNS, ECLSS, VS	Internal Thermal Control System	231	122	48	10
	MDM LA #2	TOTAL	591	689	63	15
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
1	ITCS, ECLSS, MS	Internal Thermal Control+Environmental+Manned	241	209	63	15
	MDM LA #3	TOTAL	603	687	76	6
2	MDM SERVICES	MDM SERVICES+Ada+UAS Services	350	480	0	0
2	DMS C&W	Caution and Warning	253	207	76	6
1	ITCS, ECLSS, VS	Internal Thermal Control+Environmental Control				
	MDM LA #4	TOTAL	652	879	120	13
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
1	ITCS, IAV, ECLSS	Internal Thermal Control+Environmental Control	302	399	120	13
	MDM LA #5	TOTAL	350	480	0	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
4	SEPS	Secondary Electrical Power System				

Table 3.3.-4(B). MDM Processor Utilization Estimates

11/9/92

WORK PACKAGE	SYSTEM/ELEMENTS	FUNCTION	MEMORY (KB)	PROCESSOR (KIPS)	MASS STORAGE (KB)	LOCAL BUS UTILIZATION (KBPS)
	MDM LA #6	TOTAL	350	480	0	0
2	MDM SERVICES	MDM SERVICES +Ada RTE+UAS Services	350	480	0	0
4	SEPS	Secondary Electrical Power				
	MDM M1 #1	TOTAL	617	527	112	8
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
4	EPS MBCU	Primary Power Control	245	41	98	8
2	EATCS	ETCSLTL-ACP	22	6	14	0
	MDM M1 #2	TOTAL	619	527	112	8
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
4	EPS MBCU	Primary Power Control	245	41	98	8
2	EATCS	ETCS MTL CP	22	6	14	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM M1 #3	TOTAL	617	527	112	8
2	MDM SERVICES	MDM SERVICES+AdaRTE +UAS Services	350	480	0	0
4	EPS MBCU	Primary Power Control	245	41	98	8
2	EATCS	ETCS LII-BCP	22	6	14	0
	MDM M1 #4	TOTAL	595	521	98	8
2	MDM SERVICES	MDM SERVICES +Ada +UAS Services	350	480	0	0
4	EPS MBCU	Primary Power Control	245	41	98	8
	MDM M1 #5	TOTAL	657	824	187	49
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	MT	Mobile Transporter	174	25	97	8
2	STRUCT	Structural Analysis	30	267	13	39
2	MECH	Mechanical Systems	103	52	77	2
	MDM M1 #6	TOTAL	657	824	187	49
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	MT	Mobile Transporter	174	25	97	8
2	STRUCT	Structural Analysis	30	267	13	39
2	MECH	Mechanical Systems	103	52	77	2
	MDM N1 #1	TOTAL	350	480	0	0
2	MDM SERVICES	MDM SERVICES+Ada+UAS Services	350	480	0	0
1	ECLSS	Environmental Control & Life Support System				
	MDM N1 #2	TOTAL	350	481	0	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	DMS C&W	Caution and Warning	0	1	0	0
1	ITCS, ECLSS	Internal Thermal Control + Environmental Control				
	MDM N2 #1	TOTAL	372	486	14	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
4	SEPS	Secondary Electrical Power System				
2	EATCS	ETCS LTL-AHX, ETCSLTL BHX	22	6	14	0

Table 3.3.-4(C). MDM Processor Utilization Estimates

11/9/92

WORK PACKAGE	SYSTEM/ELEMENTS	FUNCTION	MEMORY (KB)	PROCESSOR (KIPS)	MASS STORAGE (KB)	LOCAL BUS UTILIZATION (KBPS)
	MDM N2 #2	TOTAL	372	486	14	0
2	MDM SERVICES	MDM SERVICES +Ada RTE+UAS Services	350	480	0	0
4	SEPS	Secondary Electrical Power System				
2	EATCS	ETCS MIL HX	22	6	14	0
	MDM N2 #3	TOTAL	592	657	63	8
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
1	ITCS, ECLSS	Internal Thermal Control + Environmental Control	242	177	63	8
	MDM N2 #4	TOTAL	549	656	34	1
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
2	DMS C&W	Caution and Warning	0	1	0	0
1	ITC, ECLSS	Internal Thermal Control +Environmental Control	199	175	34	1
	MDM P1 #1	TOTAL	395	506	27	2
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	TRRJ	Thermal Rotary Joint Control	21	20	13	2
2	EATCS	ETCS MTL PMA,ETCS NH3 Tank,ETCS MIL CP	22	6	14	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM P1 #2	TOTAL	393	506	27	2
2	MDM SERVICES	MDM SERVICES+AdaRTE +UAS Services	350	480	0	0
2	TRRJ	Thermal Rotary Joint Control	21	20	13	2
2	EATCS	ETCS ETL-ACP	22	6	14	0
	MDM P1 #3	TOTAL	407	518	36	3
2	MDM SERVICES	MDM SERVICES +Ada +UAS Services	350	480	0	0
2	EATCS	ETCS MTL	22	6	14	0
2	EATCS HRS	ETCS Heat Rejection System	33	32	22	3
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM P3 #1	TOTAL	504	819	103	43
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	SARJ	Solar Alpha Joint Rotary Joint Control	21	20	13	2
2	STRUCT	Structural Analysis	30	267	13	39
2	MECH	Mechanical Systems	103	52	77	2
	MDM P3 #2	TOTAL	506	819	103	43
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	SARJ	Solar Alpha Joint Rotary Joint Control	21	20	13	2
2	STRUCT	Structural Analysis	30	267	13	39
2	MECH	Mechanical Systems	103	52	77	2
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM P4 #1	TOTAL	698	677	166	34
2	MDM SERVICES	MDM SERVICES+Ada+UAS Services	350	480	0	0
4	EPS PVCU	Primary Power Control, PV, THERMAL	327	177	153	32
2	SARJ	Solar Alpha Joint Rotary Joint Control	21	20	13	2

Table 3.3.-4(D). MDM Processor Utilization Estimates

11/9/92

WORK PACKAGE	SYSTEM/ELEMENTS	FUNCTION	MEMORY (KB)	PROCESSOR (KIPS)	MASS STORAGE (KB)	LOCAL BUS UTILIZATION (KBPS)
	MDM P4 #2	TOTAL	677	657	153	32
2	MDM SERVICES	MDM SERVICES +Ada RTE+UAS Services	350	480	0	0
4	EPS PVCU	Primary Power Control, PV, Thermal	327	177	153	32
	MDM PLM1#1	TOTAL	350	480	0	0
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
1	PLM					
	MDM PLM2 #1	TOTAL	350	480	0	0
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
1	PLM					
	MDM PM1 #1	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM1 #2	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE +UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM2 #1	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES +Ada +UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM2 #2	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM3 #1	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM3 #2	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+Ada+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM4 #1	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0

Table 3.3.-4(E). MDM Processor Utilization Estimates

11/9/92

WORK PACKAGE	SYSTEM/ELEMENTS	FUNCTION	MEMORY (KB)	PROCESSOR (KIPS)	MASS STORAGE (KB)	LOCAL BUS UTILIZATION (KBPS)
	MDM PM4 #2	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM5 #1	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control Syystem	2	0	0	0
	MDM PM5 #2	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM6 #1	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM6 #2	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE +UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM7 #1	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES +Ada +UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM7 #2	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM PM8 #1	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control	2	0	0	0
	MDM PM8 #2	TOTAL	439	667	80	0
2	MDM SERVICES	MDM SERVICES+Ada+UAS Services	350	480	0	0
2	PROP	Propulsion	87	187	80	0
2	PTCS	Passive Thermal Control System	2	0	0	0

Table 3.3.-4(F). MDM Processor Utilization Estimates

11/9/92

WORK PACKAGE	SYSTEM/ELEMENTS	FUNCTION	MEMORY (KB)	PROCESSOR (KIPS)	MASS STORAGE (KB)	LOCAL BUS UTILIZATION (KBPS)
	MDM PMA1 #1	**TOTAL**	**380**	**494**	**19**	**0**
2	MDM SERVICES	MDM SERVICES +Ada RTE+UAS Services	350	480	0	0
2	PTCS	Passive Thermal Control System	2	0	0	0
2	PMA	Pressurized Mating Adapter	28	14	19	0
1	ECLSS					
	MDM PMA2 #1	**TOTAL**	**380**	**494**	**19**	**0**
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
2	PTCS	Passive Thermal Control System	2	0	0	0
2	PMA	Pressurized Mating Adapter	28	14	19	0
1	ECLSS					
	MDM S1 #1	**TOTAL**	**393**	**506**	**27**	**2**
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
2	TRRJ	Thermal Rotary Joint Control	21	20	13	2
2	EATCS	ETCS ETL-PMA LTL-BNH3 Tank	22	6	14	0
	MDM S1 #2	**TOTAL**	**395**	**506**	**27**	**2**
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	TRRJ	Thermal Rotary Joint Control	21	20	13	2
2	EATCS	ETCS ETL-BPMA LTL-BNH3 Tank	22	6	14	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM S1 #3	**TOTAL**	**383**	**512**	**22**	**3**
2	MDM SERVICES	MDM SERVICES+AdaRTE +UAS Services	350	480	0	0
2	EATCS HRS	ETCS Heat Rejection System	33	32	22	3
	MDM S1 #4	**TOTAL**	**407**	**518**	**36**	**3**
2	MDM SERVICES	MDM SERVICES +Ada +UAS Services	350	480	0	0
2	EATCS HRS	ETCS Heat Rejection System	33	32	22	3
2	EATCS	ETCS ETL-B	22	6	14	0
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM S2 #1	**TOTAL**	**372**	**486**	**14**	**0**
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	EATCS	ETCS LTL-A	22	6	14	0
	MDM S2 #2	**TOTAL**	**372**	**486**	**14**	**0**
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
2	EATCS	ETCS ETL-B	22	6	14	0
	MDM S2 #3	**TOTAL**	**374**	**486**	**14**	**0**
2	MDM SERVICES	MDM SERVICES+Ada+UAS Services	350	480	0	0
2	EATCS	ETCS MIL	22	6	14	0
2	PTCS	Passive Thermal Control System	2	0	0	0

Table 3.3.-4(G). MDM Processor Utilization Estimates

11/9/92

WORK PACKAGE	SYSTEM/ELEMENTS	FUNCTION	MEMORY (KB)	PROCESSOR (KIPS)	MASS STORAGE (KB)	LOCAL BUS UTILIZATION (KBPS)
	MDM S3 #1	**TOTAL**	**371**	**500**	**13**	**2**
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
4	SEPS	Secondary Electrical Power System				
2	SARJ	Solar Alpha Joint Rotary Joint Control	21	20	13	2
	MDM S3 #2	**TOTAL**	**371**	**500**	**13**	**2**
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
4	SEPS	Secondary Electrical Power System				
2	SARJ	Solar Slpha Joint Rotary Joint Control	21	20	13	2
	MDM S3 #3	**TOTAL**	**352**	**480**	**0**	**0**
2	MDM SERVICES	MDM SERVICES+Ada RTE+UAS Services	350	480	0	0
4	SEPS	Secondary Electrical Power System				
2	PTCS	Passive Thermal Control System	2	0	0	0
	MDM S3 #4	**TOTAL**	**350**	**480**	**0**	**0**
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
4	SEPS	Secondary Electrical Power System				
	MDM S3 #5	**TOTAL**	**483**	**799**	**90**	**41**
2	MDM SERVICES	MDM SERVICES+AdaRTE +UAS Services	350	480	0	0
2	STRUCT	Structural Analysis	30	267	13	39
2	MECH	Mechanical Systems	103	52	77	2
	MDM S3 #6	**TOTAL**	**483**	**799**	**90**	**41**
2	MDM SERVICES	MDM SERVICES +Ada +UAS Services	350	480	0	0
2	STRUCT	Structural Analysis	30	267	13	39
2	MECH	Mechanical Systems	103	52	77	2
	MDM S4 #1	**TOTAL**	**728**	**944**	**179**	**73**
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
4	EPS PVCU	Primary Power Control, PV, Thermal	327	177	153	32
2	STRUCT	Structural Analysis	30	267	13	39
2	SARJ	Solar Alpha Joint Rotary Joint Control	21	20	13	2
	MDM S4 #2	**TOTAL**	**677**	**657**	**153**	**32**
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
4	EPS PVCU	Primary Power Control, PV, Thermal	327	177	153	32
	MDM S6 #1	**TOTAL**	**677**	**657**	**153**	**32**
2	MDM SERVICES	MDM SERVICES+Ada+UAS Services	350	480	0	0
4	EPS PVCU	Primary Power Control, PV, Thermal	327	177	153	32
	MDM S6 #2	**TOTAL**	**677**	**657**	**153**	**32**
2	MDM SERVICES	MDM SERVICES+AdaRTE+UAS Services	350	480	0	0
4	EPS PVCU	Primary Power Control, PV, Thermal	327	177	153	32

4. GLOSSARY

11/9/92

Action I/O may be a command from Tier 1 or a message generated by the SDP due to a limit being exceeded in an application. May also be from BIU limit checking or a value generated in application processing.

Ada.XLS is the execution rate for the application software.

Ada SLOC Rolled The number of source lines of code before any loops are implemented(used to calculate memory and mass storage requirements.

Ada SLOC Unrolled The actual number of Ada SLOC executed per cycle including the number of times through any loops(used to calculate processing requirements).

Ancillary Frequency is the rate at which data is sent to other users. This is applicable if a set of user applications require this data.

Attribute Journaling is writing to the journal in the MSU.

Attribute telemetry is the telemetry data going to C&T

Attribute I/O is the traffic due to an SDP reading and writing to a remote RODB.

Bus -A 1553 redundant pair of cables controlled by a BIA.

Chain - A set of messages for one or more busses that are executed contiguously, with multiple busses active simultaneously.

Channel - A particular cable (A or B) that is either primary or backup for a given bus.

Complex FLOP - A calculation consisting of a series of floating point operations.

Control - A chain of messages that write data to Effectors/IODB/ORUs.

Control Lists - Outgoing commands issued from an SDP. Control lists define commands to Effectors (may or may not be a MDM) from the SDP over the local bus.

Cyclic - A scan chain that is repeated with a given period and phase.

Derived Data is defined as data that is generated by a function and is placed in the RODB for access by the crew, ground or other applications. The RODB data associated with the Sensors and Effectors or Commands and Responses is not considered to be Derived Data.

Data Size is the sizes in bytes of the data item to be read or written to a RODB.

EATCS is the external active thermal conditioning system.

Event is a message saying that a limit was exceeded.

Function Cycle Rate is the rate at which the read/write is executed.

FLOPS is the number of SLOCS performing floating point operations.

Heap is a segment of memory allocated to an application program.

History Data is not used for reconfiguration.

History Entries is the number of history entries that are stored on the MSD.

History Frequency is the rate the data is to be stored on the MSD.

Journaled Data is data needed for reconfiguration in the event of a restart.

Journaled Entries is the number for Journal entries that are stored on the MSD.

Journaling Frequency is the rate the data is journaled, or stored, on the MSD.

Mass storage shown in the resource model summary is the amount of memory required in the MSU to support this application.

Message - A single 1553 command and its associated data (0-32 words)

Mode(1553) - A collection of scans and controls for use by a system.

Non-RODB Data is the data that is needed for RAM, Tables, etc. that is not included in the RODB.

On-Demand - An unscheduled scan or control chain that is executed on a priority bus reservation basis.

Redundant Software is sued to reference multiple copies executing simultaneously. (used to determine mass store requirements.

Rolled SLOCs is the actual SLOC count that must be stored in memory.

Scan - A chain of messages that read data from sensors/IODB/ORUs.

Scan lists define the inputs to the SDP over the local bus from MDMs or other ORUs.

System(1553) - A logical entity, not tied directly to an Ada program.

Telemetry Frequency is the rate the data are to be sent to the ground.

Unary Flop - A simplex (single) floating point operation.

Unrolled SLOCs are lines that actually execute including do loops, what ifs, etc..

APPENDIX A
SDP AND MDM PERFORMANCE MEASUREMENTS/PROJECTIONS AND CONSTANTS

APPENDIX A
SDP AND MDM PERFORMANCE MEASUREMENTS/PROJECTIONS AND CONSTANTS

NOTES :

(1) Value traceability is the same as the "SDP RESOURCE MODEL CONSTANTS" (Ref. Document #4) with exceptions noted.

(2) EDP processing speed increased from 3.1 MIPs to 3.9 MIPs based on latest EDP specification 152A403-PT1D. Processing time numbers decreased by ratio of 3.1/3.9 from values in "SDP RESOURCE MODEL CONSTANTS" (Ref. Document #4) and from other sources that referenced a 3.1 MIP EDP. Note that for the "DMS Resource Model" calculations, the adjustment to 3.9 MIPs was accomplished by decreasing the time required to perform the calculated number of instructions by the ratio of 3.1/3.9.

(3) NIU EDP processing speed increased from 3.1 MIPs to 3.4 MIPs based on latest EDP specification 152A403-PT1D. Processing time numbers decreased by ratio of 3.1/3.4 from values in "SDP RESOURCE MODEL CONSTANTS" (Ref. Document #4) .

(4) * = additional data not in Ref. Document #4 is identified by source.

(5) "**Systems Engineering and Integration Trade Studies DMS Performance Analysis Summary White Paper**" Document No. 901IBMX0032R1. This is a 12/20/90 document so it does not include the present Space Station Network Architecture nor are the performance figures up to date. It is the latest document published by IBM that attempts to address performance of all facets of the DMS as is such is useful as a reference document on performance analysis techniques and concepts for evaluation of DMS performance.

(6) Other parameters are taken from Reference document #14, the DMS Local Bus Performance White Paper". #14 gives information on how the performance parameters are used to calculate local bus performance.

(7) Reference #7, the "DMS TIM WP #2 dated 7/8/92" has additional measurements on BIU (local bus) performance 7. This TIM discussed the design of the STSV software for the DMS local busses and the latest local bus overview and performance data. This document along with #14 contains the local bus performance data that should be used in the model.

(8) Reference #9, "**Local Bus I/O Chaining**" : This presentation by Dr. Robert Brown of Draper Labs presents in a short concise manner data from Ref. Document # 7. Refer to slide #11 for an example of how to calculate scan response time. Added to the per scan times on slide 11 is an additional 200 microsec by Keith Culley for a missing task switch. All times shown on slide 11 are EDP Standard Services (STSV) Processing times only. They do not include BIU or MB II times.

A. Per Analog and Per Discrete times are self explanatory and are EDP processing times. Discrete processing time is presently estimated at 30 microsec.

B. Note that an MDM can only accommodate 28 sixteen bit words per message.

C. A scan list is a chain of messages and can accommodate up to 4 Kbytes of data. This is called a buffer of data at times in the documentation.

(9) Reference *14, "**DMS Local Bus Performance White Paper**" - This paper is the latest IBM analysis of the DMS 1553 bus performance. It uses the same measured and estimated performance parameters as Reference #4, the DMS Resource Model. The paper is very difficult to follow as little explanation is given as to the manner in which numbers are summarized in the example figures.

Act.Size - With regard to action I/O, this is the size of the actions. (Bytes) = 24.

Ada.Task.Switch - Task switch overhead: Processing time = 159 microsec. (Instr) = 620.

AIO.Queue.R.Proc - Instruction per Action I/O Queue Read: Processing time = 1590 microsec. (Instr). = 6200

AIO.Queue.W.Proc - Instruction per Action I/O Queue Write: Processing time = 1590 microsec. (Instr). = 6200

AIO.A.Request.Proc - Instructions required to interpret the action request.: Processing time = 795 microsec.(Instr). = 3100

AIO.R.Request.Proc - Instruction required to interpret the response request: Processing time = 1590 microsec. (Instr) = 6200

Anal.Scan.Proc - The instructions required to process an analog measurement: Processing time = 17 microsec. (Instr) = 65. Value traceable to ref. 7. Note that this is processing of a basic analog measurement without data conversion. Data conversion is Poly.Proc.1. Total process time for this process from Ref. #7 = 8 microsec (Raw Write) + 3 microsec (Data Qual Write) + 4 microsec. (converted write) + 6 microsec (converted read) = 21 microsec.. 17 microsec = (21) (3.1/3.9).

Anal.Control.Proc - Instructions required for an analog control list measurement: Processing time = 40 microsec. (Instr). = 78. (Total per analog from Reference #16).

Appl.STSV.Proc - The amount of processing required to pass the read/write data to/from the MBII interface: This is the MB II driver latency. Processing time = 787 microsec. (Instr). = 3069. In Ref. #14, Table 4, p9 199 microsec is defined as that portion of the MB II driver that is not in-line latency for BIU transfers, i.e. it occurs in parallel with BIU processing; however, it does not occur in parallel with EDP processing.

Bits.Per.Word - The number of bits including overhead per word. (Bits) = 20.

Bytes.Per. SLOC - Bytes per Ada SLOC = 30.

Complex.Instr - The complex IPS per FLOPS (Instructions/Floating Point SLOC) = 128.

Com.Word - With regard to the 1553 Local Bus, the size of the command word sent to the RT (Bits) = 20.

Cond.Conv.Element - The amount of processing required for each element in the read/write handle: Processing time = 20 microsec. (Instr) = 78.

Cond.Conv.OH - The amount of processing required to set up the conditional conversion: Processing time = 1987 microsec. (Instr) = 7750.

Control.Mess.Proc - Instructions required to process each of the 1553 messages: Processing time = 64 microsec. (Instr) = 233. Total time from Ref. #7 and Ref. #16 = 50 microsec (time stamp processing) + 4 microsec (time stamp write) + 6 microsec (time stamp read) + 20 microsec (data qual pre-proc) = 80 microsec.. 64 microsec = (80)(3.1/3.9).

Control.Proc - Instructions required process each of the control lists: Processing time = 2384 microsec. (Instr) = 9300.

Control.Size - The size of a table needed to support a Control List. (Bytes) = 50.

Deriv.Proc - Instructions required for each data derivation: Processing time = 795 microsec. (Instr) = 3100.

Dis.Control.Proc - Instructions required for a discrete measurement.: Processing time = 24 microsec. (Instr) = 93

Dis.Scan.Proc - The instructions required to process a discrete control list measurement: Processing time = 4.9 microsec. (Instr) = 19.

EDP.Event.Op.Attr - The size of the event optional attributes stored in the EDP for each instance (bytes) = 6.

EDP.Event.Size - The size of the event object class stored in the EDP for each instance (bytes) = 62.

* Effector Command - BIU processing = 1870 microsec. From Reference 14, "DMS Local Bus Performance White Paper".

* Effector Command DMA across MB-II - per 28-word message = 20 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Effector Command - 1553B cost per word - 20 microsec. From Reference 14, "DMS Local Bus Performance White Paper".

* Effector Command - MDM cost per word = 50 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Effector Command - MDM overhead - one time only for each message = 150 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Effector Command 1553B Overhead - per command message = 120 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Effector Command portion of MBII driver not latency in-line = 250 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Effector Command 1553B Response Time and IMG - per message = 16 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

Event.Proc - Instructions required for each Event: Processing time = 1590 microsec. (Instr) = 6200

FDDI.Pack.OH - Overhead per FDDI packet. (Bytes) = 22

FDDI.Bit.Byte - FDDI Bits per Byte (Bits/Byte) = 8

File.OH - the amount of overhead space required on the MSD to store the data for each file (Bytes) = 200.

Fix.16.Control.Proc - Instructions required for a 16 Bit Fixed Point measurement: Processing time = 40 microsec. (Instr) = 155

Fix.32.Control.Proc - Instructions required for a 32 Bit Fixed Point measurement: Processing time = 44 microsec. (Instr) = 171

Fix.16.Scan.Proc - The instructions required to process a 16 Bit Fixed Point Measurement: Processing time = 20 microsec. (Instr) = 78. Value traceable to discussion with Keith Culley on 10/8/92.

Fix.32.Scan.Proc - The instructions required to process a 32 Bit Fixed Point Measurement: Processing time = 24 microsec. (Instr) = 93. Value traceable to discussion with Keith Culley on 10/8/92.

Float.32.Control.Proc - The instructions required to process a 32 Bit Floating Point Measurement: Processing time = 24 microsec. (Instr) = 93.

Float.64.Control.Proc - The instructions required to process a 64 Bit Floating Point Measurement: Processing time = 28 microsec. (Instr) = 109.

Float.32.Scan.Proc - The instructions required to process a 32 Bit Floating Point Measurement: Processing time = 24 microsec. (Instr) = 93.

Float.64.Scan.Proc - The instructions required to process a 64 Bit Floating Point Measurement: Processing time = 28 microsec. (Instr) = 109.

Heap.Stack.Size - The threshold that determines whether the allocated RAM will be in the Heap or the Stack = 0.

IL.Read.Attr.Div - The amount of inner loop (IL) processing required for the integer per four bytes per read attribute: Processing time = .8 microsec. (Instr) = 3

IL.Read.Attr.First - The amount of processing required for the first four bytes per attribute read: Processing time = 3.9 microsec. (Instr) = 15.

IL.Read.Attr.Mod - The amount of processing required for the module four per read attribute: Processing time = .5 microsec. (Instr) = 2.

IL.Read.Bit.OH - The amount of processing required per Read for the first eight bits: Processing time = 6.7 microsec. (Instr) = 26

IL.Read.Bit. - The amount of processing required for each bit module eight: Processing time = 1.8 microsec. (Instr) = 7.

IL.Write Attr.Div - The amount of IL processing required for the integer per four bytes per write attribute: Processing time = .7 microsec. (Instr) = 3

IL.Write.Attr.First - The amount of IL processing required per attribute write for the first four bytes per write attribute: Processing time = 3.9 microsec. (Instr) = 15

IL.Write.Attr.Mod - The amount of processing required for the module four per write attribute: Processing time = .5 microsec. (Instr) = 2.

IL.Write.Bit. - The amount of processing required for each bit module eight: Processing time = 2.1 microsec. (Instr) = 8

IL.Write.Bit.OH - The amount of processing required per Write for the first eight bits: Processing time = 6.9 microsec. (Instr) = 27

Instruction.SLOC(Ada) - The number of Instructions per Source Line of Code = 10.

Journal.Inst.Size - The amount of memory each instance in the journalling table requires. (Bytes) = 6.

Loc.Dir.Size.EDP - The size of the local directory on the EDP required for each instance of an object class (Bytes) = 62.

Loc.Dir.Size.MSD - The size of the local directory on the MSD required for each instance of an object class (Bytes) = 62.

MBII.OH - The amount of processing required to pass a 4 Kbyte buffer of data across the MBII interface at a 1Hz rate: Processing time = 787 microsec. (Instr) = 3069

MDM.Word.OH - The number of bits of MDM word overhead per 1553 message. (Bits) = 80 microsec.

MSD.Event.Op.Attr - The size of the event optional attributes stored in the MSD (bytes) for each instance = 6.

MSD.Event.Size - The size of the event object class stored in the MSD (bytes) for each instance = 62.

Network.OH.Item - The number of bytes of overhead per FDDI Object (Bytes) = 9

Num.Copies- The number of copies of Ada software required on the MSU = 1.

Number.Switches - The number of task switches required. (Number of Task Switches/Task) = 15.

OL.Read.Attr - The amount of processing required for an outer loop (OL) RODB read: Processing time = 423 microsec. (Instr) = 1649.

OL.Write.Attr - The amount of processing required for an outer loop (OL) RODB write: Processing time = 423 microsec. (Instr) = 1649

On.Demand.Write - Instructions to issue an Action I/O Write: Processing time = 1590 microsec. (Instr) = 6200

Op.Attr.Size.EDP - The size of the optional attribute table on the EDP required for each instance of an optional attribute (Bytes) = 6.

Op.Attr.Size.MSD - The size of the optional attribute table on the MSD required for each instance of an optional attribute (Bytes) = 6.

ORU.Word.OH -The amount of DMS overhead per 1553 message for an ORU. (Bits) = 20

Other.JT.Proc -Other STSV processing associated with journaling or telemetry excluding attribute read processing and MBII processing: Processing time = 1590 microsec. (Instr) = 6200

PL.Proc - Processing required for each endpoint of Piece wise Linear Engineering Unit Conversion(EUC): Processing time = 16 microsec. (Instr) = 62.

Poly.Proc.1 = Processing required for a first order of polynomial engineering unit conversion(EUC): Processing time = 20 microsec. (Instr) = 78

Poly.Proc.2 = Processing required for a second order of polynomial engineering unit conversion(EUC): Processing time = 40 microsec. (Instr) = 155

Poly.Proc.3 = Processing required for a third order of polynomial engineering unit conversion(EUC): Processing time = 60 microsec. (Instr) = 233

Scan.Mess.Proc - Processing required to process each of the 1553 messages: Processing time = 64 microsec. (Instr) = 248. Value traceable to ref. 7.

* Scan.Proc.CA - Processing required to process each cyclic asynchronous scan: Processing time = 700 microsec x 3.1/3.9 = 556 microsec. (Instr) = 2170. Value traceable to ref. 7, "DMS TIM WP #2 dated 7/8/92" with 200 microsec added for a task switch that was missing per K. Culley on 10/14/92. This data item is not in reference #4.

Scan.Proc.CS - Processing required to process each cyclic synchronous scan. This is the Scan.Proc shown in the constant table.: Processing time = 1700 microsec. x 3.1/3.9 = 1351 microsec. (Instr) = 5270. Value traceable to ref. 7 with 200 microsec added for a missing task switch. This data item is in reference #4 as Scan.Proc.

* Scan.Proc.OD - Processing required to process each on-demand scan: Processing time = 3200 microsec x 3.1/3.9 = 2544 microsec. (Instr) = 9920. Value traceable to ref. 7, "DMS TIM WP #2 dated 7/8/92" with 200 microsec task switch time added. This data item is not in reference #4.

Scan.Size - The size of all the tables needed to support the Scan lists. (Bytes) = 50.

* Sensor Read - BIU processing = 535 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Sensor Read cost per word - up to 1400 microsec. max. per 28 word message = 50 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Sensor Read DMA across MB-II - per 28-word message = 20 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Sensor Read - 1553B cost per word - 20 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Sensor Read MDM overhead - one time only per message = 150 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Sensor Read Synch Delay for 1553b transfer = 100 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Sensor Read 1553B Overhead - per response message = 120 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

* Sensor Read 1553B Response Time and IMG - per message = 16 microsec. from Reference 14, "DMS Local Bus Performance White Paper".

Stat.Word - With regard to the 1553 local bus, the size of the status word from the RT. (Bits) = 20.

Telem.Inst.Size - The amount of memory each instance in the telemetry table requires. (Bytes) = 6.

Tel.Pack.OH - Overhead per FDDI Telemetry Packet. (Bytes) = 28.

Unary.Instr - The unary IPS per FLOPS (Instructions/Floating Point SLOC) = 27

APPENDIX B
REFERENCE DOCUMENT NOTES

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REFERENCE DOCUMENT NOTES

(1) **Contract End Item Specification for DMS,** Vol. 1: DMS Requirements, 212001A(DR SY-06.1), Specification SP-M-001 Rev. E. This document describes the present requirements for the DMS.

(2) The **"Avionics Architecture Document - CCBD JJ020746R1"** which is Revision 1 of Reference Document #2 contains the directed September 1992 DMS redesign from the Engineering Design Council. The DMS Resource Model (Reference Document #4) has been updated by IBM and MDSSC to match the redesign architecture. Also provided was reference document #2A "Recommended Avionics Architecture" (no number), the presentation in July 1992 by Rubenstein that presented the results of the follow-up study to reference document #5 and is the source for the directed avionics architecture. The directed architecture does not implement all of the recommendations in the Rubenstein presentation.

(3) **"Integrated Avionics Software Description - No Number"**. Reference Document #3 Rev. 2 dated 11/6/92 is a description of the DMS software and contains the data on DMS hardware performance and processing allocations. The performance and processing allocations in the latest versions of this document and Ref. #4 are the ones that were used in the performance model. Ref. #3 Rev. 2A is a copy of the PSAR presentation for review of this document. The document reflects implementation of the Ref. #2 design. Note that two more revisions of this document were released following the information contained in Revision #2. Revision #3 was released in May 1993 and reviewed for updates that would significantly impact the model. None were found. Revision #4 was released in September 1993 following completion of the modeling effort and was not reviewed for impact since the DMS is being redesigned.

(4) **"DMS Resource Model -No Number":** System loading was based on the latest version of reference document #4 ("DMS Resource Model") available. The latest version is Rev. G.1-1 as of June 1993 and this will be the last version as the DMS Resource Modeling task has been terminated as a result of the redesign activities. Reference document #4 is an electronic copy of the complete Resource Model on Macintosh floppies using the Excel tool. This latest version of this electronic document was distributed to the NASA Ames Research Center in order that the most up to date data could be used in the performance model. With regard to this data:

A. Ref. Document 4A Rev. 2, "SDP & MDM Resource Modeling Status Report" was the last published version of this report. The report contains detailed loading data for the WP-2 GN&C, C&T, EATCS , WP-1, WP-4 and CSA resources with regard to the DMS SDPs. Preliminary estimates for WP-2 SEPS and RJS are also included. The document also contains allocation of SDP resources and analysis results. The data being used in the model is based on the worst case "Reboost" scenario.

B. IBM provided a preliminary hard copy of the macro and constants definitions contained in reference document #4.. This document is labeled 4B. The handwritten notes are a test case and should be ignored. This document also contains descriptions of the arguments and constants used in the macros that complements reference document #4.

C. Each of the summary sheets in Reference Document #4A Rev. 2 is a rollup of all the data in the detail sheets that follow the summary sheets for each of the systems.

D. Attribute Journaling, Attribute Telemetry and Attribute I/O are unique to the Global Bus.

E. Scan lists and control lists are unique to the local bus.

F. The mass storage shown in the summary is the amount of memory required in the MSU to support the application

G. Reference document #4C is a printout of the constants for the resource model. It has corrections to the data in the floppies handwritten in as of 10/7/92. The number of instructions to be performed in doing an operation is based on a measure of the time it takes to perform that operation and not a count of the actual number of instructions performed. In other words, it is equivalent instructions. For example, look at Ada.Task.Switch = 620 instructions. As shown in the printout, the task was measured to take 200 microsec on a 3.1 MIP EDP. Since the latest application EDP is a 3.9 MIP machine measurements will have to be made again and the resource model updated. In the meantime, an approximation of task time is : (200 microsec)(3.1 MIPs/3.9 MIPs) = 159 microseconds. This is equivalent to 620 instructions on a 3.9 MIP machine.

H. Reference Document #27 ("Resource Model Documentation") is a summary and update to the data contained in preliminary documents #4B and #4C.

I. The "DMS Resource Model" does not contain FDDI performance. data.

(5) **"DMS Review January 21, 1992 - No Number"**, the Rubenstein Report. A copy was distributed. I do not recommend using the performance data included in this report. It is obsolete. The resource data in reference document #4 and the hardware performance data in reference document #3 should be used. In addition, many of the recommendations made may or may not be implemented. The software allocations in the Rubenstein Report will all be changed by the reference document #3 which contains the present recommended design. Recognize that reference document #3 is an unapproved document.

(6) "**Avionics Architecture Performance Assessment Report - MSS 4-335-069-002**" : A level 2 report received from Terry Grant.

(7) **"DMS TIM WP #2 dated 7/8/92 - No Number"**: This TIM discussed the design of the STSV software for the DMS local busses and the latest local bus overview and performance data.

(8) **"Software Release Contents Document - MDC 92H0252 Revision A"** is the release version of and replaces **"DMS Release Contents Version T1 Restructure Detailed Version Preliminary dated June 30, 1992"** - This document describes in detail the contents of the DMS releases and the capabilities that exist at each stage in the process.

(9) **"Local Bus I/O Chaining - No Number"** : This presentation by Dr. Robert Brown of Draper Labs presents in a short concise manner data from Ref. Document # 7. Refer to slide #11 for an example of how to calculate scan response time. Added to the per scan times on slide 11 is an additional 200 microsec by Keith Culley for a missing task switch. All times shown on slide 11 are EDP Standard Services (STSV) processing times only, they do not include BIU or MB II times. The following comments are made relative to this document:

A. Per Analog and Per Discrete times are self explanatory and are EDP processing times. Discrete processing time is presently estimated at 30 microsec.

B. Note that an MDM can only accommodate 28 sixteen bit words per message.

C. A scan list is a chain of messages and can accommodate up to 4 Kbytes of data. This is called a buffer of data at times in the documentation.

D. The following is an example of a STSV processing time calculation:

Assume a scan list consisting of two cyclic async messages, with the first message consisting of 28 analog words requiring data conversion and the second message consisting of 28 words of 16 discretes each. The total processing time is then: (700 microsec per scan) + (2 messages x 80 microseconds per message) + (28 analogs x 46 microsec per analog) + (28 words x 16 discretes per word x 30 microseconds per discrete) = 15.588 millisec.

E. Note that the times given are for a 3.1 MIP EDP. For a 3.9 MIP EDP and no change in BIU/BIA processing rates, the EDP processing time would be an estimated 3.1/3.9 = .79. Therefore, total processing time would be (700 x .79) + (2 x 80) + (28 x 46 x .79) + (28 x 16 x 30 x .79) = 12.349 millisec.

F. A note of interest is that a written in comment says that the killer is MDM response time of approximately 25 millisec.

(10) "**Performance Requirements and Load Point of the EDP/NIA - No Number**" - This paper discusses the performance requirements of the onboard, end-to-end communications across the FDDI network, and the load point at which these requirements must be met. A range of possibilities is presented since detailed measurements of the NOS EDP and NIA is not yet available. As of 10/14/92 measurements had still not been made according to N.N. Heise.

(11) "**End-to-End Latency - No Number**" - This paper discusses the end-to-end performance of the ISO commands across the FDDI network, the no-load latency requirements of the EDP, and the necessity for command priorities.

(12) "**User's Guide (Software) Volume 1 Flight Software for DMS Release 2 - Document No. 150A128-01**": The purpose of this document is to serve as a reference guide for users of the DMS. The document contains background information for application software builders about the DMS software services and user scenarios for use of these services. In its final form it will contain the specific steps to be followed and information needed for users to create applications.

(13) "**Systems Engineering and Integration Trade Studies DMS Performance Analysis Summary White Paper - 901IBMX0032R1**": This is a 12/20/90 document so it does not include the present Space Station Network Architecture nor are the performance figures up to date. It is the latest document published by IBM that attempts to address performance of all facets of the DMS and as such is useful as a reference document on performance analysis techniques and concepts for evaluation of DMS performance..

(14) "**DMS Local Bus Performance White Paper - 911IBMX0017R1**" - This paper is the latest IBM analysis of the DMS 1553 bus performance. It uses the same measured and estimated performance parameters as Reference #4, the DMS Resource Model. The paper is very difficult to follow as little explanation is given as to the manner in which numbers are summarized in the example figures.

(15) DMS "**BEST ESTIMATE OF SUMMARY SLOCS INCLUDING THREATS - No Number**" is a detailed listing of the best estimate of DMS sizing as of 6/92. This is the latest estimate available. It is presented by language type, CSCI and Release version. The software estimates are given in cumulative form by how many additional SLOCs are added for each release.

(16) "**Data Management System (DMS) Software Detailed Design Review No. 3.2 (WP-2) - No Number**" is a detailed description of the DMS Software contained in Release 3.2. It is a good reference document to describe and illustrate how the DMS software is designed to function. It is a two volume set. The CSCIs addressed are OS/Ada RTE, NOS(design only, release in 4.0), and STSV. The latest performance estimates on the Local Bus are provided. These estimates were incorporated into Appendix A.

(17) "**Space Station Freedom Program Acronym List - LESC-296888-B**" is an internal Lockheed document defining all known (as of Nov. 2, 1992) SSF acronyms.

(18) "**BIU Performance Measurement White Paper - 91IBMX0025**" documents how the BIU latency measurements used in Reference #14 were made.

(19) - (23). are self explanatory by their titles and are reference documents W through aa in Section 1.3.2.

(24) "**Real-Time Scheduling Theory and Ada - No number**" is a paper that discusses rate monotonic scheduling theory and its implications for Ada. Rate monotonic scheduling was implemented in the DMS.

(25) **"Priority Inversions in R1 STSV Design - No Number"** is a paper that discusses priority inversion issues with the implementation of rate monotonic scheduling in the DMS STSV R1 design and recommends solutions to the problems. The DMS design was revised to incorporate these solutions.

(26) is self explanatory by its title and is reference document ad in Section 1.3.2.

(27) **"Resource Model Documentation - No Number"** is a description of the "DMS Resource Model" theory, inputs and outputs, constants and equations for DMS SDPs and MDMs.

(28) **"Avionics System Management Design Document Volume 1 - No Number"** contains the results of an integration activity performed on the SSF Avionics Architecture. The document states that the architecture was analyzed for viability and operability of the integrated design in terms of its role in supporting the SSF mission. Areas addressed included Command and Control; Fault Detection, Isolation and Recovery; Onboard Data Management; and Onboard Checkout. The document presents operational concept for managing the integrated Avionics System and defines associated design requirements. Several recommendations for improvement are also made.