INTEGRATION AND TEST OF HIGH-SPEED TRANSMITTER ELECTRONICS FOR FREE-SPACE LASER COMMUNICATIONS

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Abstract

The NASA Lewis Research Center in Cleveland, Ohio, has developed the electronics for a free-space, direct-detection laser communications system demonstration. Under the High-Speed Laser Integrated Terminal Electronics (Hi-LITE) Project, NASA Lewis has built a prototype full-duplex, dual-channel electronics transmitter and receiver operating at 325 megabits per second (Mbps) per channel and using quaternary pulse-position modulation (QPPM). This paper describes the integration and testing of the transmitter portion for future application in free-space, direct-detection laser communications. A companion paper[1] reviews the receiver portion of the prototype electronics. Minor modifications to the transmitter were made since the initial report on the entire system,[2] and this paper addresses them. The digital electronics are implemented in gallium arsenide integrated circuits mounted on prototype boards. The fabrication and implementation issues related to these high-speed devices are discussed. The transmitter's test results are documented, and its functionality is verified by exercising all modes of operation. Various testing issues pertaining to high-speed circuits are addressed. A description of the transmitter electronics packaging concludes the paper.

I. Introduction

The High-Speed Laser Integrated Terminal Electronics (Hi-LITE) Project at the NASA Lewis Research Center in Cleveland, Ohio, has undertaken the development of the communications electronics portion of a free-space, direct-detection laser communications system. The transmitter outputs two channels of quaternary pulse-position-modulated (QPPM) data at 325 megabits per second (Mbps) per channel, requiring QPPM symbol slot periods of 1.54 nanoseconds (nsec).

The package described in this paper is a prototype, to be followed by a demonstration model. The prototype communications electronics (PCE) has been constructed at NASA Lewis from discrete high-speed integrated circuits and analog components with SMA connectors on 20 individual circuit boards housed in three chassis. The PCE transmitter chassis contains five boards. The demonstration communications electronics (DCE), currently under development, will collapse the 10 boards of digital electronics into a single application-specific integrated circuit (ASIC).

The PCE transmitter has been fully integrated and tested. The functionality of the transmitter is briefly summarized here, and its recent modifications are described in detail. The uniqueness of the board fabrication process, issues related to integration of various boards, testing and debugging concepts, packaging, and thermal stability concerns for high-speed circuits are described for the transmitter electronics in the sections that follow.

Section II briefly outlines the operation of the PCE transmitter, noting modifications since the previous report.[2] Transmitter board fabrication and simulation issues are discussed in Section III. Section IV includes testing and debugging concepts of the PCE transmitter and documents appropriate results. Packaging and thermal stability practices for high-speed circuits are given in Section V. Finally, the Appendix presents computer-aided design (CAD) schematics and interface control documents and includes a glossary.

II. PCE Transmitter Operation

Source Data Multiplexer/Channel Data Demultiplexer

Figure 1 shows the functional elements of the Hi-LITE PCE transmitter, each of which is under computer control. The data sources feed the digital data router, where they are processed for output to the optical transmitter, whose output is the QPPM dual-channel laser link. In an operational intersatellite link the transmitted beams pass through optics and a telescope. For laboratory testing of the transmitter the optical transmitter outputs are connected to a bit-error-rate (BER) test set receiver through the PCE receiver electronics.[1] The source data multiplexing allows the option of selecting dual 325-Mbps sources

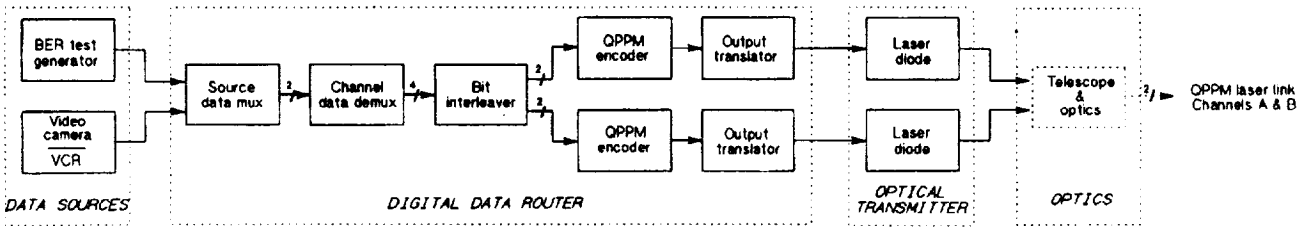

Figure 1.—Block diagram of Hi-LITE dual-channel QPPM transmitter.

or single 650-Mbps source and their accompanying clocks. The source data multiplexer accepts pseudorandom bit sequences (PRBS) and digitized nonreturn-to-zero (NRZ) video data as its primary inputs and provides two serial 325-Mbps signals to the demultiplexer. The demultiplexer converts these signals into two 2-bit parallel signals per channel, for a total of four 162.5-Mbps binary data streams. The parallel signals are used to construct QPPM symbols for their respective channels.

Bit Interleaver/QPPM Encoders

The bit interleaver provides the options to route the four 162.5-Mbps binary data streams directly to the QPPM encoders or to interleave them bit by bit. The purpose of interleaving is to be able to infer the BER performance of the optical channel that carries the video data from that of the channel that carries the PRBS data. The PRBS data format lends itself to BER measurement (unlike the video data format), and the assumption is that the interleaved video data undergo the same path degradations and interference. Each QPPM symbol encoder accepts the two 162.5-Mbps parallel data streams per channel and converts them into a 325-Mbps QPPM encoded data stream. The QPPM encoders finally pass two 325-Mbps QPPM encoded data streams to the output translator, a feature added to the PCE transmitter since the last report.[2]

QPPM Output Translator

The purpose of the output translator is to create dc-coupled and ac-coupled outputs, through different terminations, for each 325-Mbps data stream. These outputs are used to drive other electronics within the Hi-LITE system. Data streams from both encoders are used to modulate the two lasers. A computer-controlled signal disables either channel by transmitting zeros in each of the four slots so that the laser power is conserved. This helps distinguish whether the channel is turned off intentionally or not.

A clock generation and distribution board, located in the same chassis, provides precisely aligned clock signals at the bit clock rate or submultiples to ensure synchronous operation.

III. Simulation and Fabrication

A Dazix digital CAD system (version 6.3) was used to design and simulate the electronics circuitry. Once the logic design of a high-speed circuit is finalized, simulation and board layout becomes an iterative process. First, a logic simulation is performed to verify circuit functionality. During simulation of these 650-Mbps (1.54-nsec period) signals, a delay of 50 picoseconds per centimeter (psec/cm) for the microcoaxial interconnections must be considered.

Commercial four-layer prototype boards were used for fabrication, providing the option of mounting up to eight GaAs chips per board, each in any of four orientations to optimize interconnection routing. The iterative process of layout, simu-

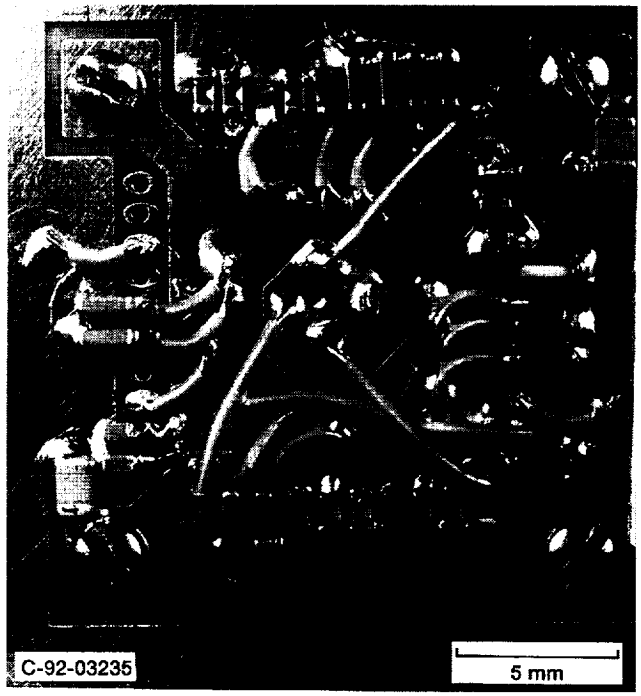

Figure 2.—Typical bottom of a GaAs chip site depicting surface-mount capacitors, resistors, and dc wiring.

lation, and testing is repeated until the designer is satisfied that the hardware will be viable.

The resulting layout is transferred to a specific fabrication document (see Appendix) to aid in assembly. The fabrication of these prototype transmitter boards requires special attention to signal terminations and decoupling power planes. A microscope workstation is used because dimensions as small as several thousandths of an inch are common in surface-mount resistors, capacitors, and dc wiring (Fig. 2). A base socket with gold foils that makes contact with the integrated-circuit (IC) footprints on the board is installed at each chip site. The GaAs IC with a predefined orientation is inserted into the base socket and secured with a heat sink. SMA connectors for interboard and chassis front panel signal routing and a power connector are mounted on each board.

IV. Integration and Testing

The transmitter was integrated and tested in three phases. During Phase I the source data multiplexer alone was tested, and the results were documented. In Phase II the channel data demultiplexer and the bit interleaver were added and tested for validity. Last, in Phase III, QPPM encoders and QPPM output translators were integrated, and their performance was verified.

Phase I

Commercial equipment consisting of a BER test data generator and a video camera or a video cassette recorder (VCR) was used as dual 325-Mbps sources, and a test data source from in-house-built special test equipment was used as a single 650-Mbps source. All data sources and their accompanying clocks were fed into the source data multiplexer. The operation of the source data multiplexer was verified by simply changing the mode select line while observing the signals on a sampling oscilloscope. Figures 3 and 4 show representative signals expected for dual 325-Mbps sources and a single 650-Mbps source, respectively, where T_b and T_s are bit and slot time durations, respectively. For the dual 325-Mbps source mode, Channel A (carrying the 325-Mbps PRBS) and Channel B (carrying the 325-Mbps real-time video data) were passed

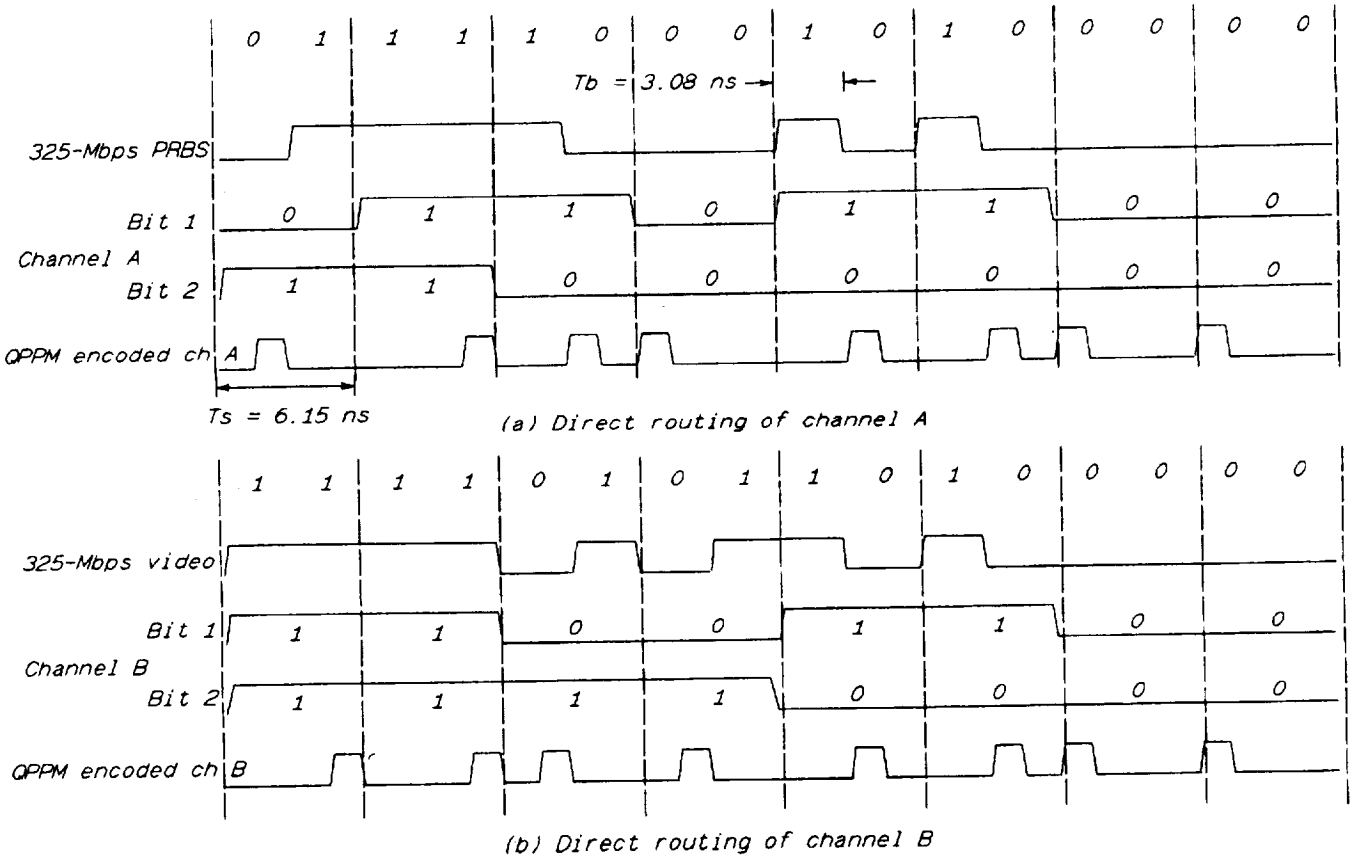

Figure 3.—Timing diagram for dual 325-Mbps sources with direct routing option.

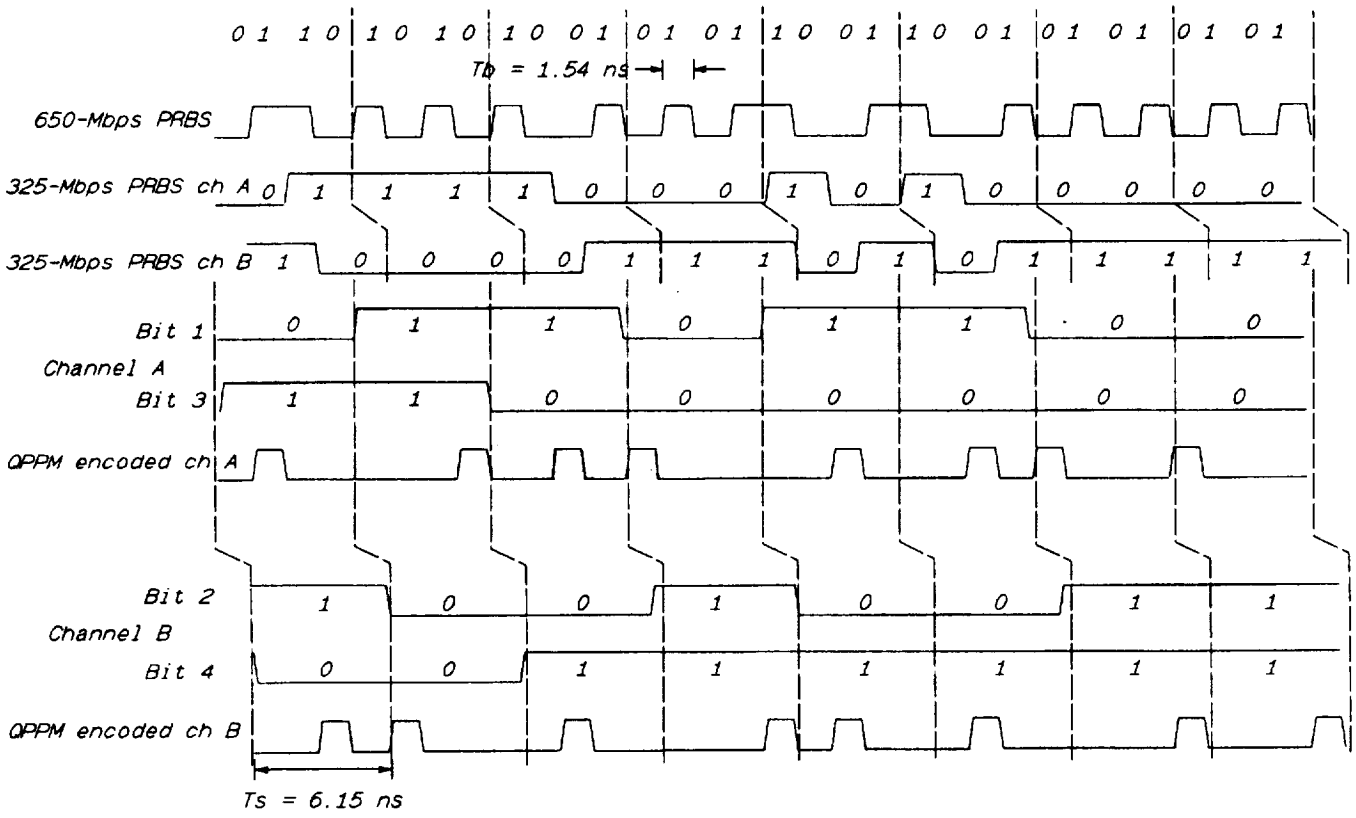

Figure 4.—Timing diagram for single 650-Mbps source mode.

directly through the source data multiplexer to the channel data demultiplexer. There, alternate bits of each channel were split, forming four channels at 162.5 Mbps each. In the single 650-Mbps source mode alternate bits of the PRBS were first split into two 325-Mbps channels prior to passing to the channel data demultiplexer as before. As with any high-speed electronics system minor length adjustments for the microcoaxial interconnects were necessary to optimize timing. Moreover, in order to observe GaAs level signals on the oscilloscope, a signal termination of 50 Ω to ground was required. In order to achieve this, a signal termination board was built and included in the transmit chassis.

Phase II

In Phase II the four 162.5-Mbps signals from the channel data demultiplexer (using both modes described in Phase I) were fed to the bit interleaver and tested under two additional modes, straight or interleaved, using different PRBS patterns. Direct routing is depicted in Fig. 3, which shows each 162.5-Mbps 2-bit pair passing directly to the QPPM encoders. Figure 5 shows the interleaving option. The bit-by-bit interleaving of both channels was accomplished by exchanging the least significant bits only (i.e., bit 2 of Channel A was exchanged with bit 2 of Channel B). The final two 2-bit pairs were passed to the QPPM encoders for QPPM symbol creation. Test points built into the design enabled observation of critical signals.

Phase III

Phase III added the QPPM symbol encoders and QPPM translators. Initially, 16-bit and 32-bit binary data patterns were input to the transmitter for a quick check of the QPPM symbols on the sampling scope. Encoding of information bits into QPPM symbols is described in a previous paper[2] and is summarized in Fig. 6. QPPM encoded signals are shown for all transmitter operating modes in Figs. 3 to 5. More robust testing was then performed using PRBS patterns as long as 2^{23}-1, along with the video data. On a commercial BER test set receiver the bit-error rate observed was zero.

Testing Issues

Special attention to details and a well-thought-out test plan were required for testing the high-speed circuits. The GaAs IC's used were electrostatic-sensitive devices; therefore ground-

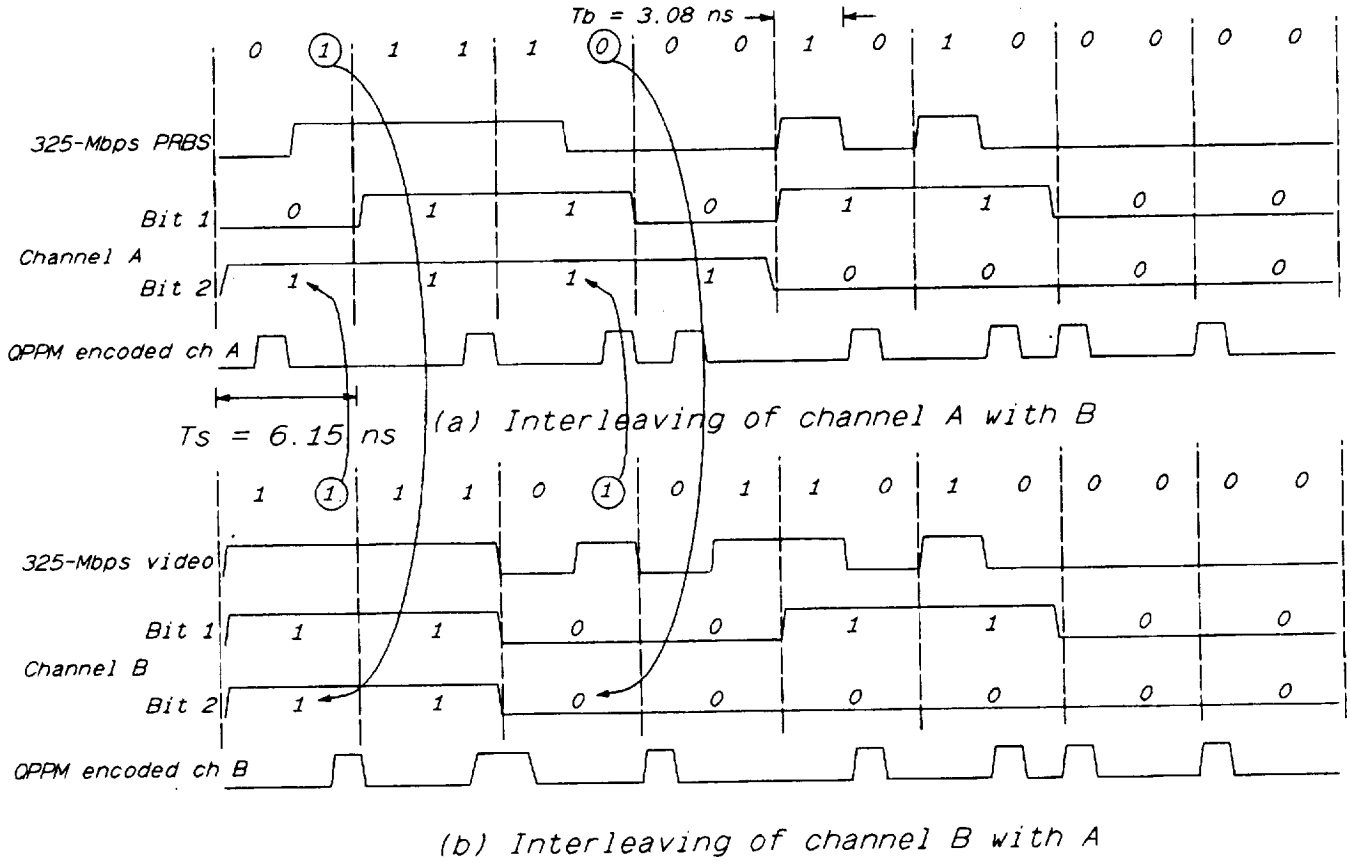

Figure 5.—Timing diagram for dual 325-Mbps sources with interleaving option.

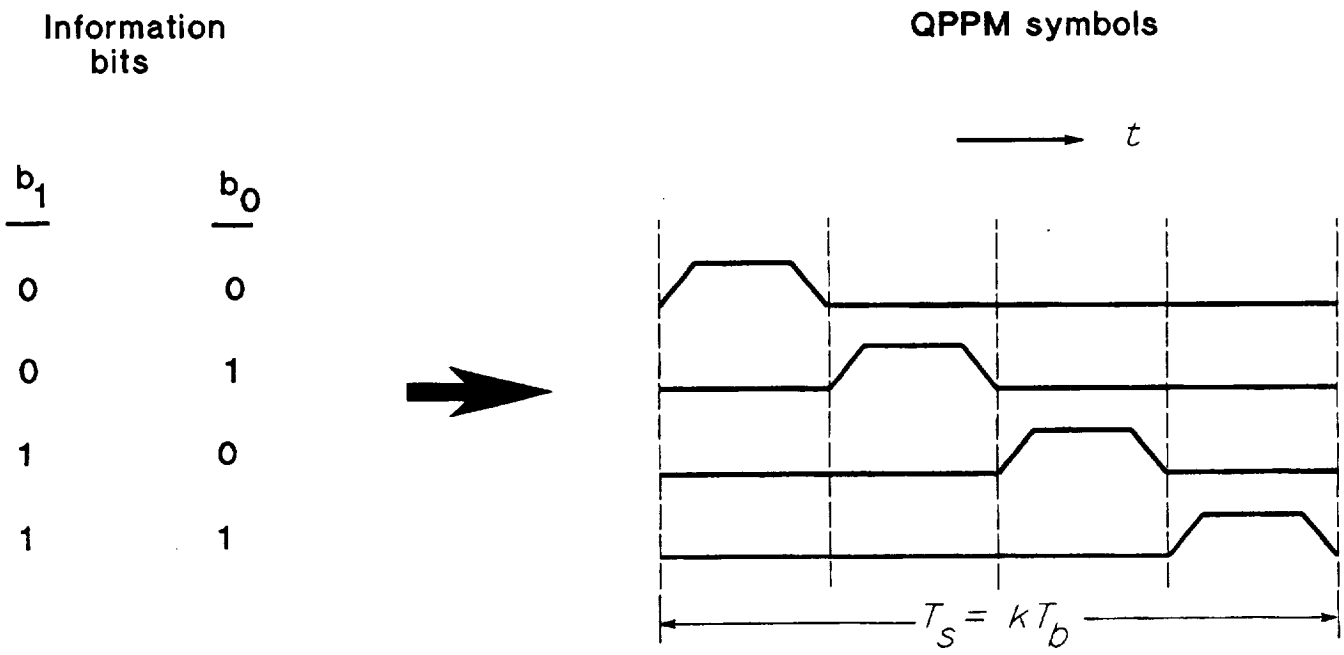

Figure 6.—Encoding of information bits into QPPM symbols.

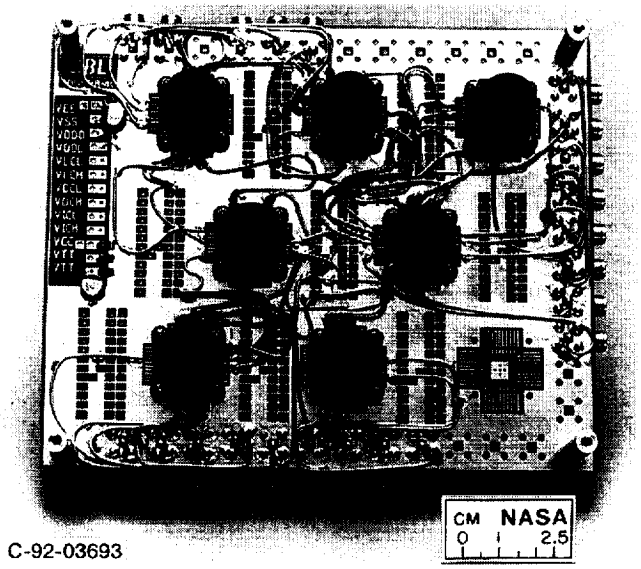

Figure 7.—Top view of a typical prototype board.

ing straps for the operator and properly grounded electrostatic-insensitive surfaces are recommended. Because GaAs IC's are also very sensitive to certain power levels and the order in which they are applied, it is advisable to check them before powering up a board. In order to observe high-speed signals, a Tektronix P6156 probe (3.5-GHz bandwidth) was used, although not without some difficulty because of the high density of components and cables and the very small dimensions. A much better method for observing signals is to predetermine test points and bring them out in the design.

V. Packaging and Front Panel Layout

For ease of debugging the prototype electronics of the Hi-LITE project, the boards are all mounted on slides, allowing probe access. The prototype boards, as shown in Fig. 7, are 4 in. wide and 5 in. high. One edge has a power connector, and the other three have SMA connectors for input/output and test signals. Because the cooling fans are installed on the back panel, the circuit boards are oriented perpendicular to it for free airflow. The front panel is depicted in Fig. 8, and the chassis layout is shown in Fig. 9. Inputs to the source data multiplexer are on the left side of the panel. A reference signal (VBB_{ref} = -1.2 V) is supplied in case the data source is single ended rather than differential. In the middle of the panel the QPPM outputs for both channels are available in either ac-coupled or dc-coupled format. On the right is the input/output for the clock generation and distribution board. Differential clock signals such as 650 and 325 MHz are provided for the transmitter and other Hi-LITE electronics.

The transmitter has been tested and integrated in the Hi-LITE system. A future paper will describe the capabilities of the automated test equipment and present system test results for a wide range of operating parameters.

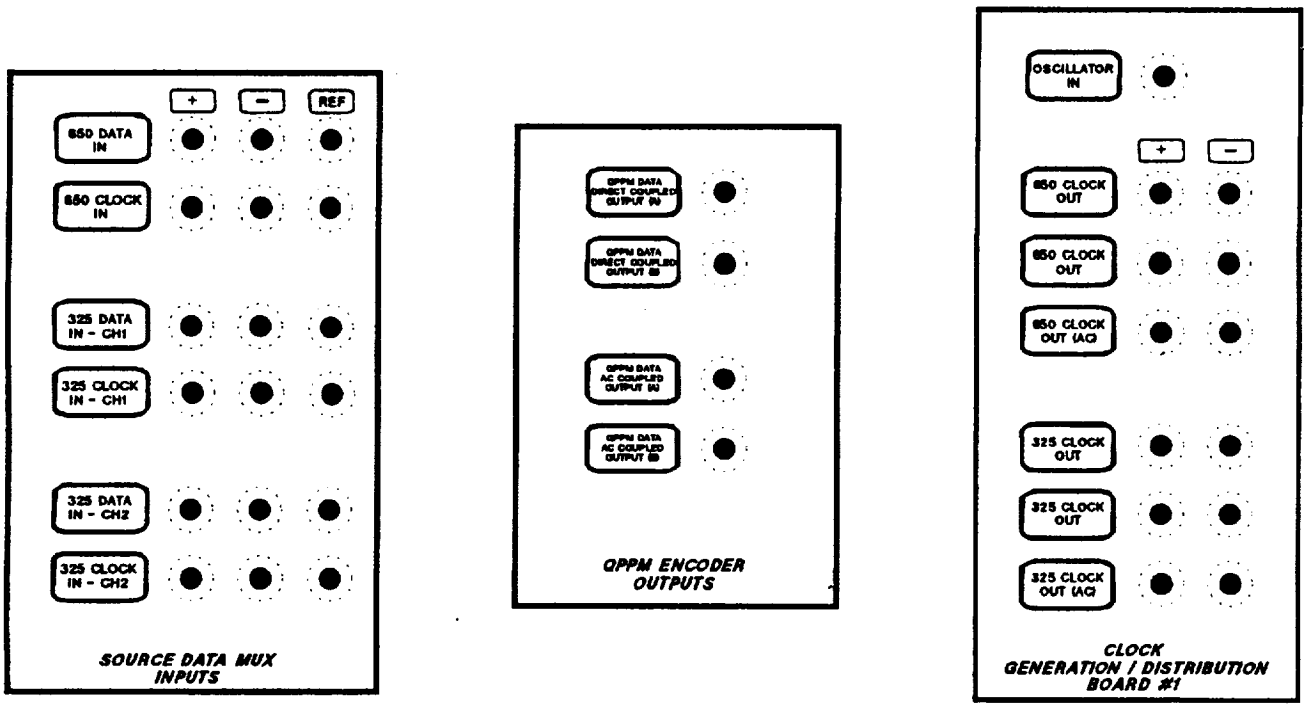

Figure 8.—PCE transmitter chassis front panel layout.

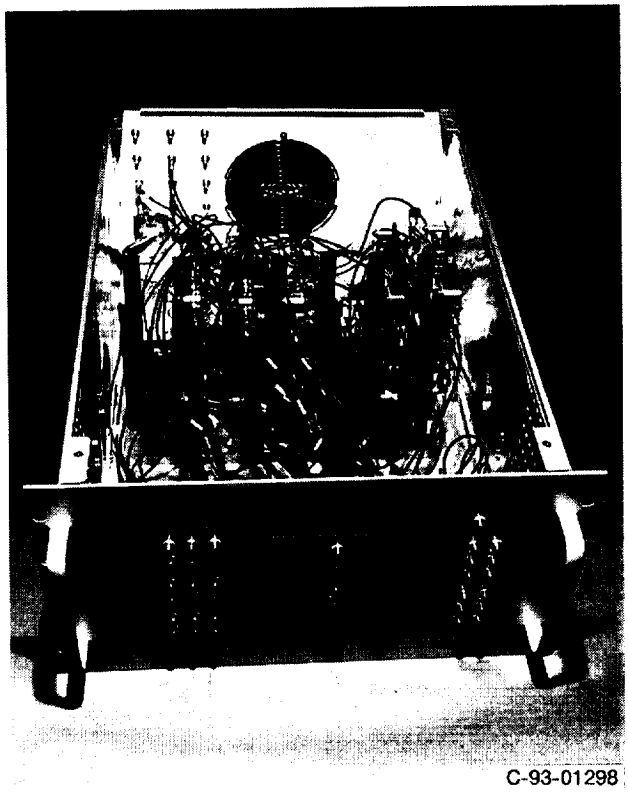

Figure 9.—PCE transmitter chassis assembly layout.

VI. Appendix—Glossary, CAD Schematics, and Interface Control Documents

Glossary

ASIC	application-specific integrated circuit
BER	bit error rate
DCE	demonstration communications electronics
CAD	computer-aided design
PCE	prototype communications electronics
GaAs	gallium arsenide
Hi-LITE	High-Speed Laser Integrated Terminal Electronics
IC	integrated circuit
Mbps	megabits per second
NRZ	nonreturn to zero
PRB	pseudorandom bit sequence
QPPM	quaternary pulse-position modulation
STE	special test equipment
SMA	subminiature amphenol
VCR	video cassette recorder

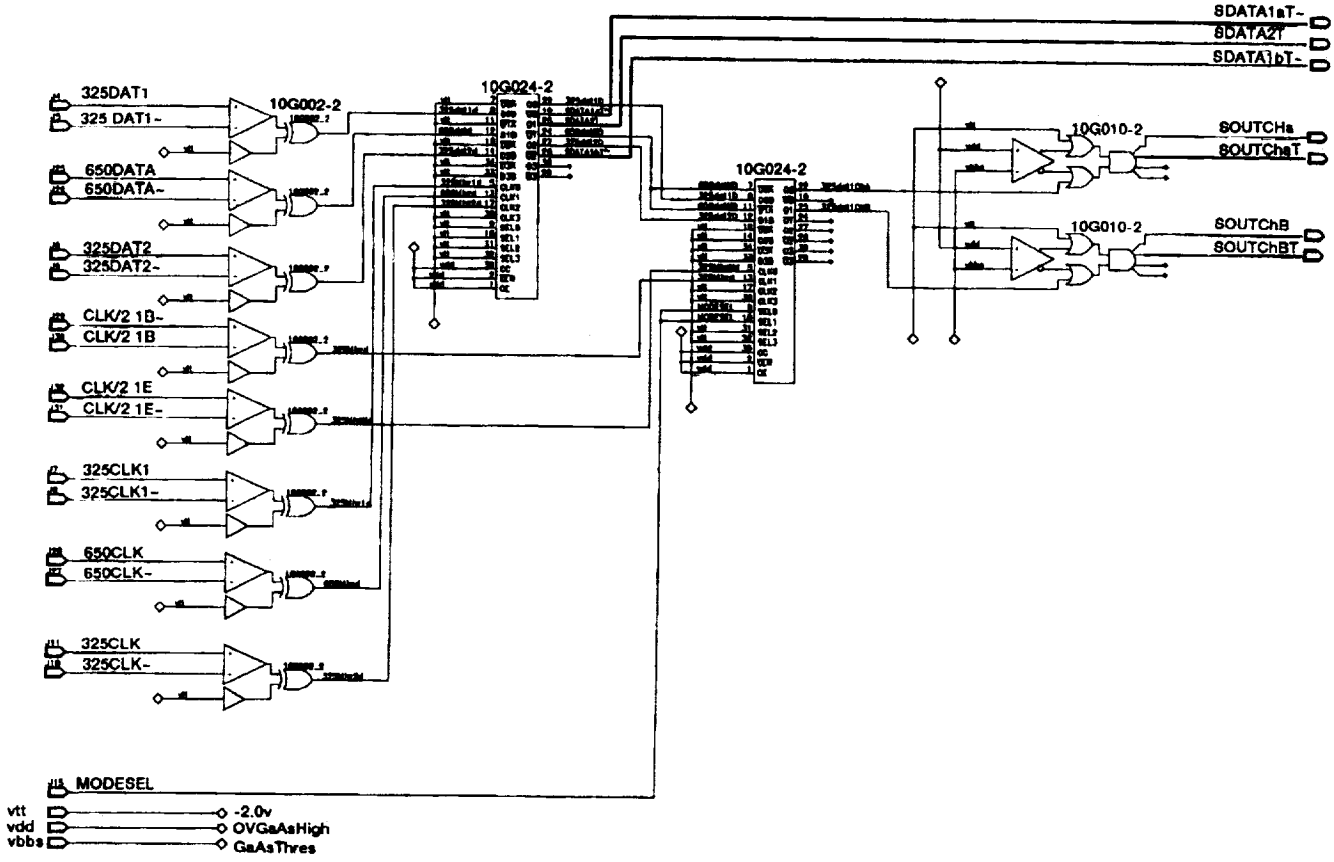

Figure A-1.— CAD schematic for source data multiplexer of PCE transmitter.

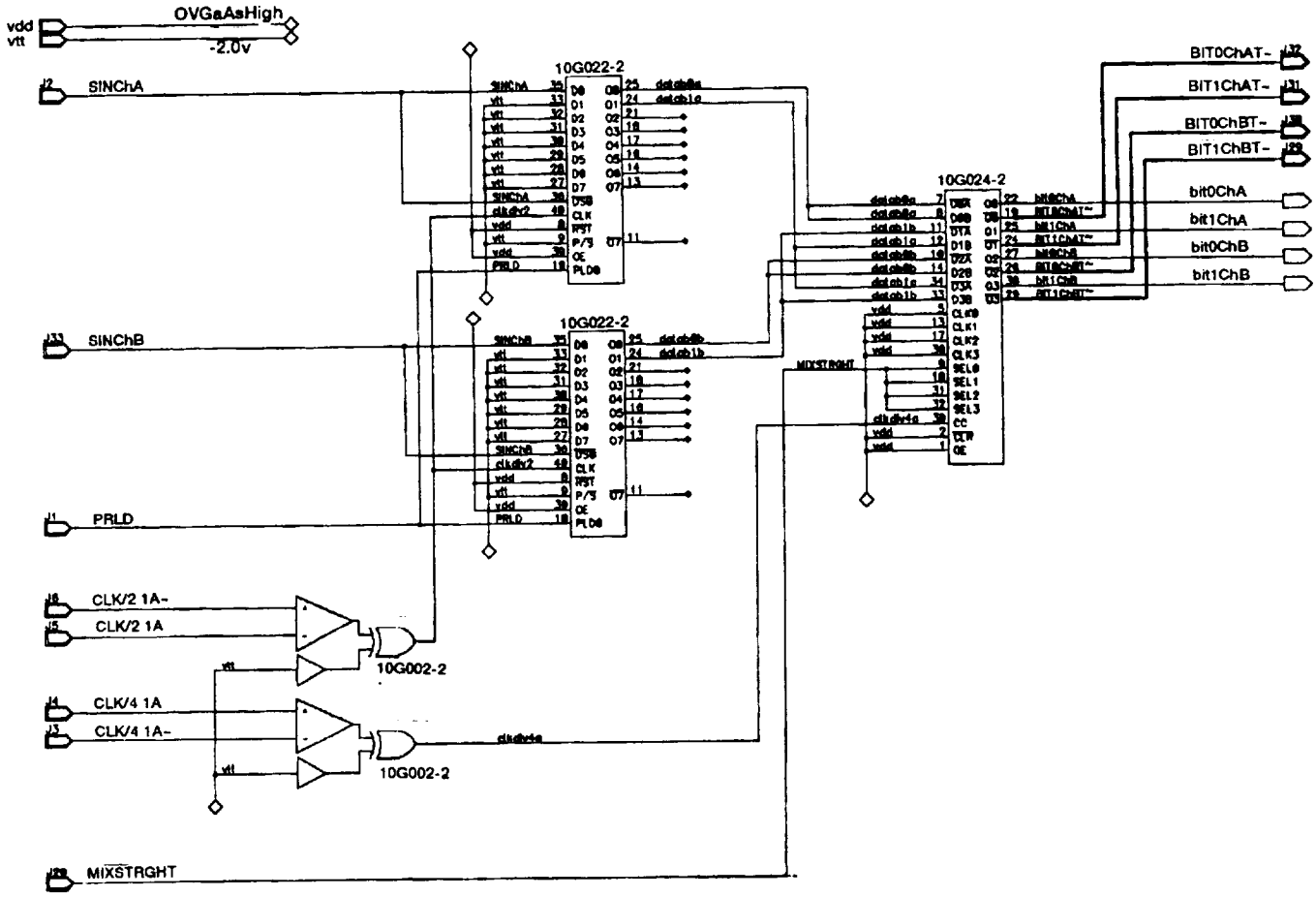

Figure A-2.—CAD schematic for channel data demultiplexer of PCE transmitter.

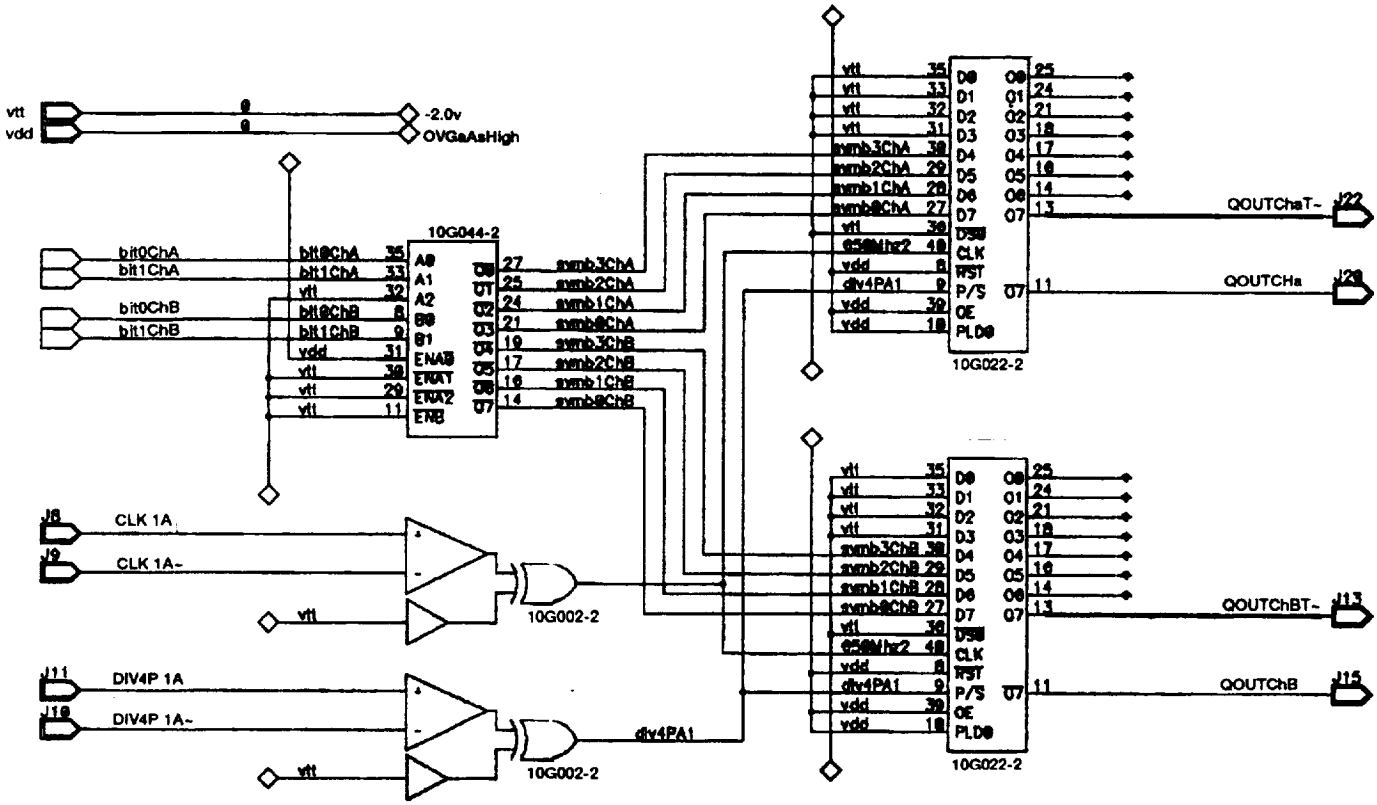

Figure A-3.—CAD schematic for QPPM symbol encoder of PCE transmitter.

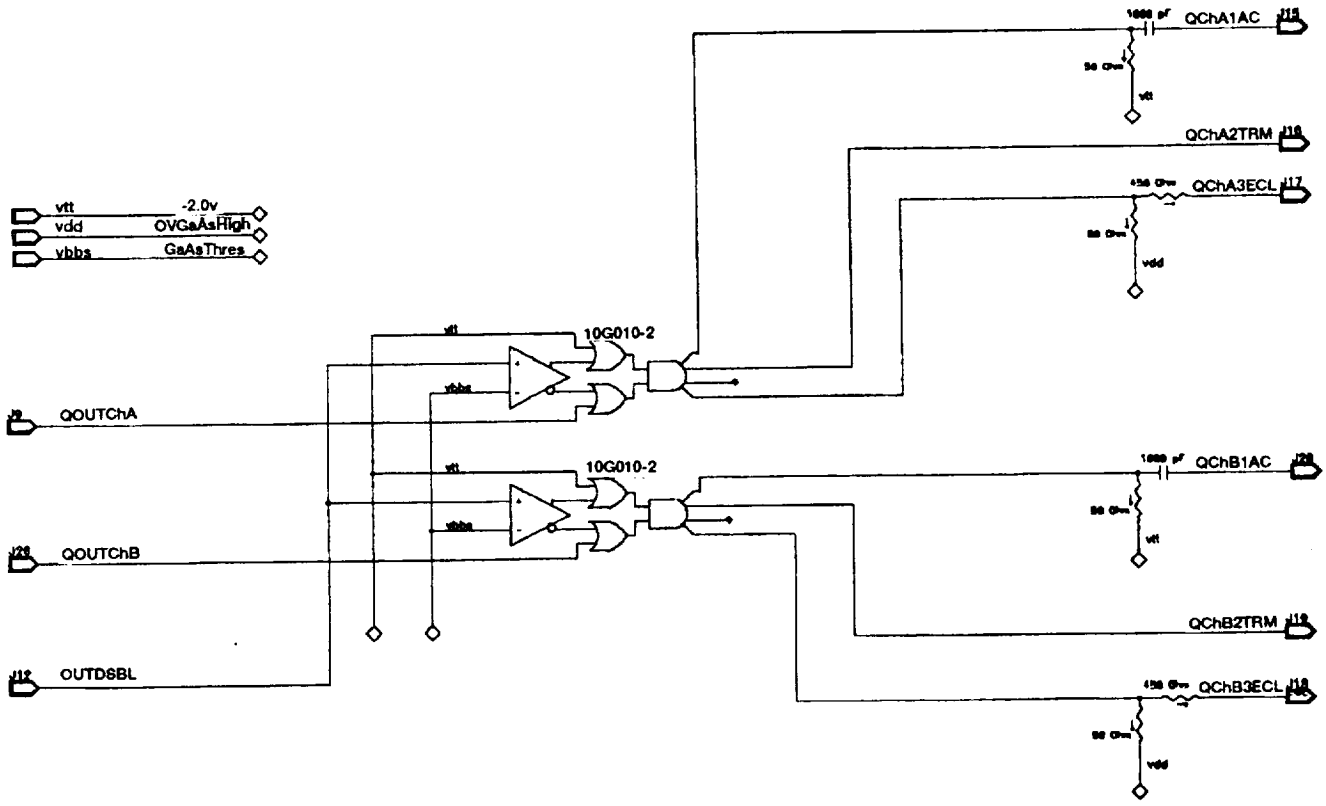

Figure A-4.—CAD schematic for QPPM output translator of PCE transmitter.

Signal Descriptions

Signal Name	Connector	Signal Type	Source	Destination	Description
325DAT1 & 325DAT1~	SMA4 & SMA5	PicoLogic or ECL	BERT or QPPM Test Data Source (TDS)		Source#1:325Mhz Data and Data~ from BERT or STE
325DAT2 & 325DAT2~	SMA8 & SMA9	PicoLogic or ECL	Video or QPPM Test Data Source		Source#2:325Mhz Data and Data~ from VIDEO or STE
650DATA & 650DATA~	SMA25 & SMA26	PicoLogic or ECL	BERT or QPPM Test Data Source		Source#3:650Mhz Data and Data~ from BERT or STE
325CLK1 & 325CLK1~	SMA7 & SMA6	PicoLogic	BERT or TDS		325Mhz Clock to drive data Source#1.
325CLK2 & 325CLK2~	SMA11 & SMA10	PicoLogic	Video or TDS		325Mhz Clock to drive data Source#2.
650CLK & 650CLK~	SMA28 & SMA27	PicoLogic	BERT or TDS		650Mhz Clock to drive data Source#3.
325CLKA & 325CLKA~	SMA31 & SMA32	PicoLogic	CLK GEN/DIST; Clk/2 & Clk/2~		325Mhz Clock to drive Channel A Latch at the Output.
325CLKB & 325CLKB~	SMA29 & SMA30	PicoLogic	CLK GEN/DIST; Clk/2 & Clk/2~		325Mhz Clock to drive Channel B Latch at the Output.
MODESEL	SMA15	TTL	EGSC		Select Line to select either two 325Mhz Sources OR one 650Mhz Source.

Figure A-5.—Typical interface and control document page for PCE transmitter.

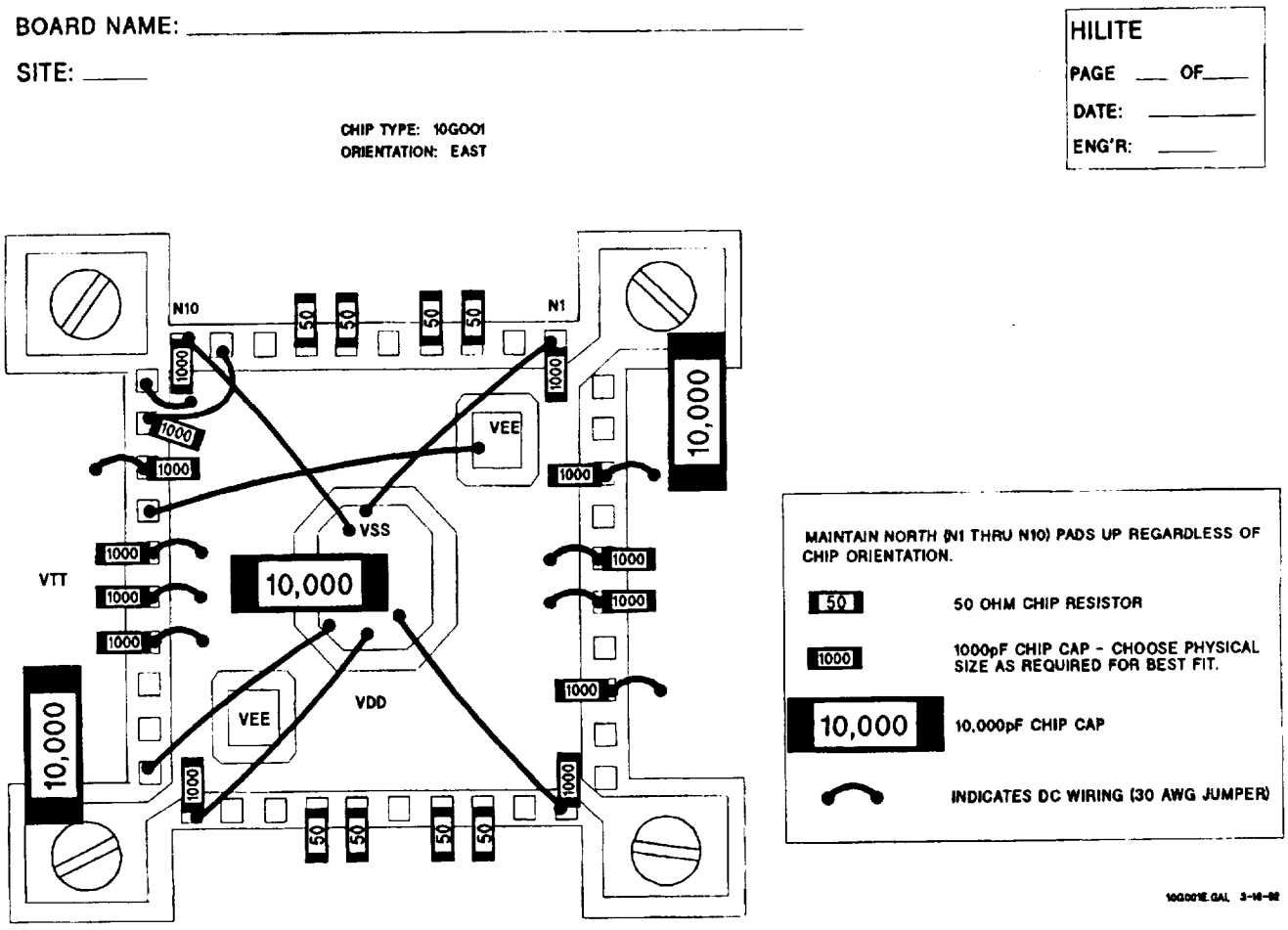

Figure A-6.—Typical fabrication document for GaAs IC's bottom side.

VII. Acknowledgments

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VIII. References

1.Budinger, J.M., et al., "QPPM Receiver For Free-Space Laser Communications," AIAA 15th International Communications Satellite Systems Conference, San Diego, CA, Feb. 28–Mar. 3, 1994.

2.Budinger, J.M., et al., "Quaternary Pulse Position Modulation Electronics for Free-Space Laser Communications," AIAA/NASA/OAI Conference on Advanced SEI Technologies, Cleveland, OH, Sept. 4–6, 1991.

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