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This worst case analysis verifies that the TRMMESA electronic design is capable of maintaining performance requirements when subjected to worst case circuit conditions. The TRMMESA design is a proven heritage design and capable of withstanding the most worst case and adverse of circuit conditions. Changes made to the baseline DMSP design are relatively minor and do not adversely effect the worst case analysis of the TRMMESA electrical design.

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TRMMESA WORST CASE ANALYSIS

Purpose:

This worst case analysis verifies that the TRMMESA electronic design is capable of maintaining performance requirements when subjected to worst case circuit conditions.

Method:

Each electrical part in the design was derated to account for the effects due to initial tolerance, temperature, age, and radiation. The net degradation was determined by RSSing the contributions attributed to each degradation term.

The effects of initial tolerance and temperature were determined by consulting component data book specifications. The temperature range assumed for the analysis was -15C to 65C, with exception to the A2 power supply board which is required to start at the low temperature extreme of -25C. The qual temperature range for the TRMMESA design is -15C to 50C; thus the analysis allows for a 15C component temperature rise above the qual ambient.(The qual temperature range might possibly be changed to -15C to 35C. One of the major reasons for this possible spec. change is to allow the ORS loop to maintain the loss to space at a fixed level. The loop is subject to run out of available heater power at the higher temperature extremes.)

The degradation attributed to age was determined by referencing the guidelines used on the DMSP and TIROS programs, which are similar to the TRMMESA requirements. The DMSP and TIROS guidelines are in most cases based on MIL-STD-1547 derating criteria. (As a side note, most of the electrical parts for the TRMMESA design are being transferred from DMSP stock.)

Finally, radiation degradation was determined by once again referencing the guidelines used for the DMSP program. In those few cases for which the DMSP guidelines contained no information on the part in question, radiation degradation was determined by referencing other sources available at Barnes.

The electrical parts in the design are exposed to a maximum radiation level of 1.84KRAD, determined by referencing document CDRL #10B which just considers the radiation shielding provided by the 20mil. aluminum end cover of the unit. As discussed by document CDRL #10B, in actuality, the radiation exposure levels are closer to about .1KRAD.

The design is required to meet a ten times safety margin, which means that the worst case radiation level to be considered is 18.4KRAD. The DMSP radiation derating information for electrical components is all at a minimum level of 50KRAD. Thus, the radiation degradation assumed for the worst case analysis is very conservative and the total RSS effects due to all of the degradation terms is also in general very conservative since often the radiation term is the most significant contributor.

Appendix A. of this document contains the DMSP guidelines referenced for age and radiation derating as well as the elecrical schematics and a system timing diagram of the similar DMSP design.

Summary:

A1 Board:

The +/- 10V regulators located on the A1 board can tolerate worst case circuit conditions and maintain required performance.

The dc offsets at each output stage on the A1 board is at an acceptable limit.

A2 Board:

The A2 power supply is guarenteed to maintain oscillation after start-up.

The start-up of the power supply board is dependent on the gain of the start transistor being sufficient. No radiation degradation information has been found for the start transistor yet. So, until radiation information for the 2N4405 is available, the analysis can not be completed. No problems are anticipated since the circuit has a great deal of safety margin, but information on the 2N4405 is required to complete the power supply analysis.

The primary current drive capability of the power supply is sufficient to support the primary current loading.

The power supply over current limit trip point is appropriately set at 200mA nominal.

The secondary voltage outputs headroom, gain, and tolerance is sufficient to maintain good regulation and drive the required loads.

The worst case in-rush current meets TRMM specifications.

A3 Board:

Locations Q10 and Q12 on the A3 board should be selected for a low initial gate to source threshold voltage in order to ensure that the FET's will operate properly at these two locations.

With exception to the above requirement, the A3 board demod logic, integrator logic, and comparator logic can tolerate worst case circuit conditions and maintain required performance.

The total A3 board A/D conversion error is 36 counts worst case, which is an acceptable worst case delta

A4 Board:

Locations Q1, Q2, and Q11 on the A4 board should be selected for a low initial gate to source threshold voltage to ensure proper operation.

With exception to the above requirements, the ORS servo loop logic and the reference voltage logic is capable of operating over worst case circuit conditions.

The A4 board telemetry meets TRMM specifications.

The ORS servo loop dc offsets are acceptable.

The drive to the ORS heater is sufficient.

The reference run-out voltage circuitry offset and tolerance is acceptable.

A14 Board:

The analysis of the 17V regulator requires radiation degradation information on the 2N5662 transistor in order to verify that the gain is sufficient to drive the primary load. No problems are anticipated, but the analysis requires additional information in order to complete the A14 board calculations.

The A14 board telemetry meets TRMM specifications.

A5 Board:

The line sync and data clock receiver circuitry can tolerate worst case conditions and has sufficient ac and dc hysteresis to ensure proper operation. Further, the circuitry meets the TRMM specifications with regard to redundancy and input logic level requirements.

The data and data ready outputs meet TRMM specifications.

The series/shunt and demod logic has been properly modified to accommodate simultaneous dual channel operation.

The maximum time required to achieve sync. with the space craft line sync is 45 seconds.

In order to complete the A5 board analysis, radiation degradation for the oscillator must be entered into the calculations. No problems are anticipated since once again the design ~~can~~ has a large safety margin.

A5, A6, and A7 Logic:

The logic and timing for the A5,A6 and A7 boards has not been analyzed in detail. The type of logic used in the design is CMOS CD4000 type. The clock rates of the system are relatively slow, rendering effects such as propagation delay and rise/fall times negligible.

General:

In general the TRMMESA design is a proven heritage design and capable of withstanding the most worst case and adverse of circuit conditions. Changes made to the baseline DMSP design are relatively minor and do not adversely effect the worst case analysis of the TRMMESA electrical design.

A1 BOARD PREAMP

TOPICS TO BE CONSIDERED

1. +/- 10V REGULATOR REQUIREMENTS
2. DC OFFSETS OF FIRST AND SECOND STAGE
3. COMPOSITE FREQUENCY RESPONSE OF THE PREAMP

1. +/- 10V REGULATORS

gain requirements:

The available base drive for both the +10V regulator and the -10V regulator is given by:

$$I_b = I_{p(1N5297)} - I_{z(1N4625)}$$

where

$$I_{p(1N5297)} = \text{spec} - [\text{tol}^2 + \text{temp}^2 + \text{age}^2 + \text{rad}^2]^{1/2}$$

the initial tolerance, temperature, age, and radiation degradations for the 1N5297 are given by:

tol = 10% from the data sheet spec. = .1mA
temp = (-.6%/C)(40C)(1mA) = .24mA where the temp coeff. is the data sheet spec.
age = 10% = .1mA
rad = .05mA from the GE DMSP raiation guidelines at 500KRAD

So,

$$I_{p(1N5297)} = 1\text{mA} - [.1\text{mA}^2 + .24\text{mA}^2 + .1\text{mA}^2 + .05\text{mA}^2]^{1/2} = .7\text{mA}$$

The required 1N4625 zener current is .25mA max., since the part is specified at a zener current of .25mA and guarenteeed to break down. In reality, the 1N4000 series zeners will break down at 10uA typical. But we will assume that a worst case current of .25mA is required.

Thus ,

$$I_b = .7\text{mA} - .25\text{mA} = .45\text{mA}$$

The available gains for q51 and q52 are given by:

$h_{FE(q51)} = [(1/h_{FE(pre\text{-}rad)} + (d(1/h_{FE(post\text{-}rad)})]^{-1}$

where

h_{FE}(pre-rad) = spec.(temp factor)(age factor)

The spec. min. for the dc current gain of the 2N2222A transistor at a curent level of 5mA is 50 minimum.(the loading is +/-5mA w/c)

Over a temperature range of 25C to -55C, the dc gain changes by about 50% by referencing a graph in the data book for the 2N2222A transistor. So, over a qual temperature range of -15C to 50C, the temp factor is approximately given by:

temp factor(2N2222A) = 1 - [(25C + 15C)/(25C + 50C)](50%) = .75

The age derating is conservatively estimated to be 15%.

Thus, the pre-rad dc min. gain is (50)(.75)(.85) = 32

The radiation term is determined by referencing the GE supplied radiation degradation data used for the DMSP design. So, at a current level of 5mA, $d(1/h_{FE(post\text{-}rad)}) = .02$ for a 2N2222A transistor at 100KRADS exposure.

Finally, the computed worst case gain is $h_{FE(q51)} = [(1/32) + .02]^{-1} = 20$

By similar fashion, the gain of q52 is given by:

$h_{FE(q52)} = [(1/100(.70)(.85) + (.03)]^{-1} = 21$

So, the available current drive for the 10V and -10V regulators is given by:

$I_{10V} = h_{FE(q51)} I_b = 20(.45mA) = 9mA$

$I_{-10V} = h_{FE(q52)} I_b = 21(.45mA) = 9.5mA$

The max load on the regulators is 5mA; so the gain and base drive are sufficient to drive the load.

<u>headroom:</u>

It should be verified that both of the regulators have sufficient voltage headroom in order to maintain the gain of the transistors.

The headroom for the 10V regulator is given by:

$V_{hr(q51)} = V_{13V} - 2V_{z(1N4625)} + V_{be(q51)}$

A reasonable rss calculation for the $2V_{z(1N4625)}$ term is given by:

$2Vz(1N4625) = 2(typ.) + [2(tol^2 + temp^2 + age^2 + rad^2)]^{1/2}$

where

initial tolerance = 5%(5.1V) = .26V
temp = [.03%/C](40C)(5.1V) = .06V
age = (2%)(5.1V) = .1V
rad = .05V (DMSP GE rad derating at 500KRAD)

$2V_{z(1N4625)} = 2(5.1V) + [2(.26V)^2 + 2(.06V)^2 + 2(.1V)^2 + 2(.05V)^2]^{1/2} = 10.6V$

The 13V minimum level is $V_{13V} = 12.1V$

The base to emitter drop of q51 is $V_{be(q51)} = .6V$ min.

So the 10V headroom is $V_{hr(q51)} = 12.1V - 10.6V + .6V = 2.1V$, which is adequate. The data book for this part has some performance graphs which show how the dc gain of the part degrades with applied collector to emitter voltage. The graphs indicate that the gain only degrades about 10% between a collector to emitter voltage of 10V and 1V.

By similarity, the -10V regulator has 2.1V of headroom, which is also adequate.

<u>tolerance:</u>

$dV_{10V} = d[2V_{z(1N4625)}] - dV_{be(q51)}$

$dV_{be(q51)} = (tol^2 + temp^2 + age^2 + rad^2)^{1/2}$

$dV_{be(q51)} = [(.2V)^2 + (.1V)^2 + (.1V)^2 + (.1V)^2]^{1/2} = .3V$

Also, referencing the above calculations, $d(2V_{z(1N4625)}) = .4V$

So the 10V tolerance is 9.5V +/-.7V

2. DC OFFSET OF THE FIRST AND SECOND STAGES

It must be verified that the dc offset at each amplifier output is not excessive or capable of bringing either of the amplifiers into saturation.

The offset at the outpput of the first stage is given by:

$$V_{os(u1)} = [I_{g(os)q1}(R1 + R2) + V_{gs(os)q1}][1 + (R_7/R_8)]$$

where

$$I_{g(os)q1} = \text{spec} + [\text{temp}^2 + \text{age}^2 + \text{rad}^2]$$

In the data sheet, the gate offset operating current is not specified. However, the gate operating current is specified and equal to 15pA max at 25C. Assuming the gate operating current doubles for every 10C, at 65C the gate current is $2^4(15pA) = 240pA$. Now, we can conservatively estimate that the gate offset operating current is 25% of the gate operating currrent or 60pA at 65C and 3.75pA at 25C. Thus, the temperature factor is 60pA - 3.75pA = 56.25pA.

The age derating is 10%(spec at 25C) = .10(3.75pA) = .4pA

The rad derating is 3.3pA which was derived by consulting some of the Barnes in house data.

Thus $I_{g(os)q1} = 3.75pA + [(56.25pA^2 + .4pA^2 + 3.3pA^2]^{1/2} = 60pA$

The gate to source offset voltage of u1 is given by:

$$V_{gs(os)u1} = \text{spec} + [\text{temp}^2 + \text{age}^2 + \text{rad}^2]^{1/2}$$

where

spec. = 5mV max at 25C

temp = (10uV/C)(40C) = .4mV

age = .10(5mV) = .5mV

rad = 7mV by referencing some Barnes in house data(no GE DMSP guidelines available)

Thus the gate to source offset voltage is 12mV

Finally, the dc offset at the output of u1 is given by:

$V_{os(u1)} = 104[53M(60pA) + 12mV] = 1.6V$

Since the max signal voltage at the output of u1 is 50mV and the supplies are +/-8.8V minimum, 1.6V is an acceptable amount of offset. Also, note that the first stage is ac coupled to the second stage.

The offset of the second stage is given by:

$V_{os(u3)} = 100[V_{os(u3)} + 1.1M(I_{b(u3)})]$

where

$V_{os(u1)} = .5mV + [.2mV^2 + 1.5mV^2 + .1mV^2]^{1/2} = 2mV$

(The age derating of 1.5mV and the radiation derating of .1mV were derived by consulting some Barnes in house data since the DMSP program had no information regarding this part.)

Also,

$I_{b(u1)} = 130pA + [250pA^2 + 60pA^2 + 910pA^2]^{1/2} = 1.1nA$

So, $V_{os(u3)} = 100[2mV + 1.1M(1.1nA)] = 320mV$

An offset of 320mV is acceptable considering the fact that the max earth signal at the output of the second stage is 5V and the power supplies are +/-12V minimum. Also, as will be discussed later on the A3 board, the demod will eliminate the digitization error associated with preamp offset.

3. COMPOSITE FREQUENCY RESPONSE

Extensive noise analysis regarding the preamp is discussed in document CDRL #22B. The intent of this section is to present the frequency response of the preamp for informatinal purposes only. Figure 1. on the following page illustrates the nominal preamp frequency response.

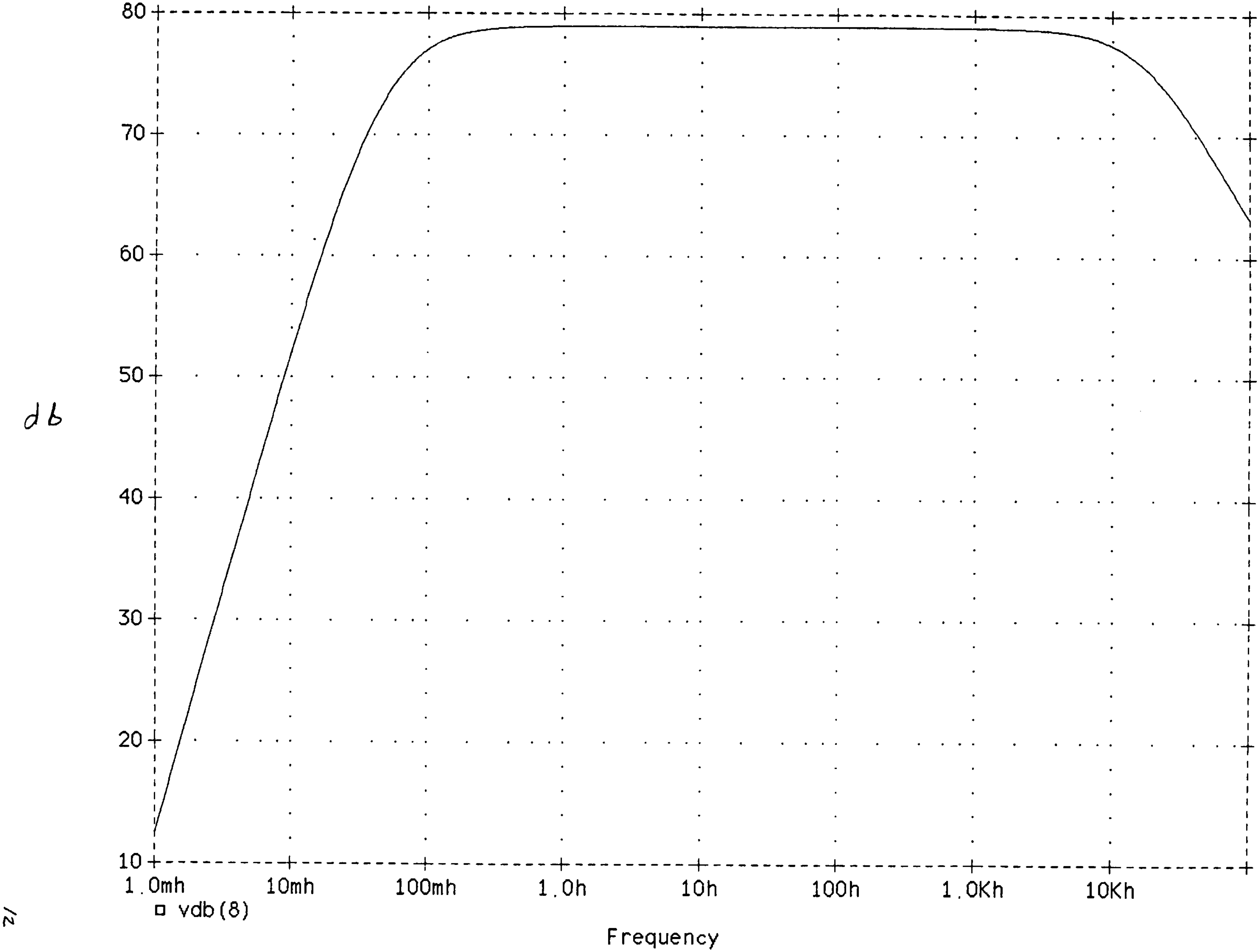
The rather high bandwidth of the preamp is to insure that the commutation spikes associated with the sampling of the detectors, decays at a reasonably fast rate. The preamp output is digitized at the A3 board, which operates as a dual slope A/D. The commutation spikes on the preamp signal occur during the hold times of the integrator on the A3 board. Thus,. by keeping the time of the spikes to a minimum, the A/D is able to reject the spikes by always being in the hold mode until after the spike has decayed to zero.

* p/a freq response

Date/Time run: 11/01/93 18:48:29

FIGURE 1

Temperature: 27.0



12

A2 POWER SUPPLY

TOPICS TO BE CONSIDERED

1. OSCILLATOR START UP
2. PRIMARY CURRENT DRIVE CAPABILITY
3. OVER CURRENT PROTECTION
4. SECONDARY VOLTAGE OUTPUTS(TOLERANCE,HEADROOM,GAIN)
5. INPUT FILTER IN RUSH CURRENT
6. INPUT CURRENT RIPPLE

1. OSCILLATOR START UP

Note that the power supply is configured as a Royer oscillator,thus once start up is accomplished, the power supply will sustain oscillation at approximately 4khz. Start up is accomplished by turning on either of the two switching transistors(Q2 or Q3).

Thus,just before start up:

$$V_{C(Q1)} = V_{FCR4} + R_4(V_{B(Q2)}/R_3) + V_{BQ2}$$

$$V_{BQ2} = V_{BEQ2} + (dV_{BEQ2}{}^2(TEMP) + dV_{BEQ2}{}^2(AGE) + dV_{BEQ2}{}^2(RAD))^{1/2}$$

$$V_{BQ2} = 1.1V + ((.1V)^2 + (.11V)^2 + (.14V)^2)^{1/2} = 1.3V$$

$$V_{FCR4} = .8V + ((.1V)^2 + (.08V)^2 + (.1V)^2)^{1/2} = .96V$$

$$\mathbf{V_{CQ1} = .96V + 2.49K(1.023)(1.3V/.249K(.985)) + 1.3V = 15.8V}$$

Thus, to accomplish start up, a maximum of 15.8V is required at the collector of Q1.

The voltage at the emitter of Q1 is the 17V regulator output voltage. The tolerance on the 17V output is given by:

$$dV_{17V} = 68k(dI_{B(LM108)}) + 8.5(dV_{OS(LM108)}) + .3(dV_{Z(1N4573)})$$

$dI_B = ((TEMP)^2 + (AGE)^2 + (RAD)^2)^{1/2}$

$dI_B = ((1nA)^2 + (.2nA)^2 + (15nA)^2)^{1/2} = 15nA$

$dV_{OS} = ((.25mV)^2 + (.05mV)^2 + (1.6mV)^2)^{1/2} = 1.63mV$

$dV_Z = ((64uV)^2 + (.64V)^2 + (.05V)^2)^{1/2} = .64V$

$\mathbf{dV_{17V} = 1mV + 14mV + .2V = .2V}$

Thus the 17V output is 16.8V min. Therefore, just before start up, the voltage across Q1 is 1V and the current is $I_{R3} + I_{R8}$. The required gain of Q1 is given by:

$h_{FEQ1} = ((I_{R3} + I_{R8})/I_{BQ1}) + 1$

$I_{BQ1} = (V_{17V} - V_{BEQ1} - V_{ZCR3})/R_2$

$V_{ZCR3} = 10V + ((.5V\ tol.)^2 + (.08V)^2 + (.2V)^2 + (.1V)^2)^{1/2}$

$V_{ZCR3} = 10.6V$

$I_{BQ1} = (16.8V - .8V - 10.6V)/(1.023)(12.4K) = .43mA$

$\mathbf{h_{FEQ1}(req'd) = (2(1.3V)/(.985)(.249K))/.43mA) + 1 = 26}$

at 1V,11mA.

Next, we must verify that the gain of Q1 is sufficient:

$h_{FE}(available) = (1/h_{FE}(pre\text{-}rad) + d(1/h_{FE}(post\text{-}rad)))^{-1}$

$h_{FE}(pre\text{-}rad) = (spec\ limit)(temp\ factor)(age\ factor)$

$h_{FE}(pre\text{-}rad) = 100(.7)(.85) = 60$

Therefore, we require

$\mathbf{d(1/hFE(post\text{-}rad)) = (1/26) - (1/60) = .023}$

I have not been able to find radiation information on the 2N4405, so this requirement must be revisited at a later date.

<u>After start up is accomlished, it must be verified that the start transistor(Q1) is shut off.</u>

Q1 is shut off after self sustained oscillation is achieved. Capacitor C1 charges up and shuts Q1 off by feeding a voltage to the cathode of CR6.

Thus,

$$V_{KCR6} = V_{17V} + (V_{17V} - V_{CE(SAT)Q2} - V_{R6} - VF_{CR6})$$

V_{17V} = 16.8V by an earlier result

$$V_{CE(SAT)Q2} = .2V + ((.1V)^2 + (.03V)^2 + (.03V)^2)^{1/2} = .3V$$

V_{FCR6} = .96V by an earlier result

$$V_{R6} = 110mA(4.99OHM)(1.015) = .56V$$

$$V_{KCR6} = 16.8V + (16.8V - .3V - .56V - .96V) = 31.8V$$

So, assuming Q1 and CR1 are off

$$V_{BQ1} = V_{ZCR3} + R_2((V_{KCR6} - V_{ZCR2} - V_{ZCR3})/(R_1 + R_2))$$

$$V_{ZCR3} = (spec.) + (tol^2 + temp^2 + age^2 + rad^2)^{1/2}$$

$$V_{ZCR3} = 10.0V - ((.5V)^2 + (.1V)^2 + (.2V)^2 +(.02V)^2)^{1/2}$$

$$V_{ZCR3} = 9.4V$$

$$V_{ZCR2} = 13V + ((.65V)^2 + (.1V)^2 + (.26V)^2 + (.02V)^2)^{1/2}$$

$$V_{ZCR2} = 13.7V$$

$$R2/(R1 +R2) = .985(12.4K)/(1.65k(1.015) + .985(12.4K)) = .88$$

$$V_{BQ1} = 8.9V(1 - .88) + (31.8V - 13.7V)(.88) = 17.0V$$

V_{EBQ1} = 16.8V - 17.0V = -.2V Thus Q1 is turned off after start up.

2. **PRIMARY CURRENT DRIVE CAPABILITY**

$I_{BQ2} = (V_{2-1} - V_{BEQ2} - V_{R6})/R_3$

$V_{2-1} = (19T/90T)(16.8V - .56V - .4V) = 3.34V$

$V_{BEQ2} = 1.1V + ((.1V)^2 + (.05V)^2 + (.14V)^2)^{1/2} = 1.28V$

$V_{R6} = 4.99(1.015)(110mA) = .56V$

$I_{BQ2} = (3.34V - 1.28V - .56V)/.249k(1.015) = 5.9mA$

$I_{CQ2} = (h_{FEQ2} + 1)I_{BQ2}$ or $h_{FEQ2}(req'd) = (I_{CQ2}/I_{BQ2}) - 1$

$h_{FEQ2}(pre\text{-}rad) = 90(.7)(.85) = 54$

$d(1/h_{FEQ2}(post\text{-}rad)) = .008$

$h_{FEQ2}(derated) = ((1/54) + .008))-1 = 38$

$h_{FEQ2}(req'd) = (110mA/5.9mA) - 1 = 18$

Thus, under worst case primary current loading, the required gain of Q2 and Q3 is 18 and the available worst case gain is 38. Therefore, the base drive to both of the primary switching transistors is adequate.

3. **OVERLOAD PROTECTION**

The 17V regulator located on the A14 board is designed to fold back at an oveload current determined by A14-R8,R9,V_{BEQ4}

Assuming the primary current evenly splits between R8 and R9, the over current limit is set by the equation below:

$I_{pri}(OL) = 2V_{BEQ4}(cut\text{-}in)/R8$

V_{BEQ4}(cut-in) = .7V w/c, .5V typ.

R8 = 4.99 OHM typ., .985(4.99 OHM) w/c

Thus the nominal overload current trip point is set at 200mA and the w/c limit is 285mA.

Since the primary swithing transistors are rated for 1A and the primary transformer windings are 32awg rated at approximately 140mA (assuming 500 cir mils per amp), the current limit trip point is appropriately set with the assumption that the two primary windings of the transformer conduct in alternate half cycles.

4. **SECONDARY OUTPUT VOLTAGES**

Tolerance:

+13V: $V_{13V} = V_{ZCR12} - V_{BEQ5} - V_{R12}$

$dV_{ZCR12} = -(tol^2 + temp^2 + age^2 + rad^2)^{1/2}$

$dV_{ZCR12} = -((.7V)^2 + (.1V)^2 + (.3V)^2 + (.02V)^2))^{1/2}$

dV_{ZCR12} = +/- .8V

dV_{BEQ5} = .2V

dV_{R12} = .1V

V_{13V} = 14V - .7V - .1V = 13.2V typ.

V_{13V} = (14.0V - .8V) - (.7V + .2V) - (.1V+.1V) = 12.1V min

V_{13V} = 14.8V - .5V - 0V = 14.3V max.

+12V: $V_{12V} = (70T/90T)V_{pri} - V_{FCR26} - I_{HTR}R_{19}$

V_{pri} = 16.8V - .3V -.56V = 16V min

V_{FCR6} = .96V max

I_{HTR} = 10V/300OHM = 33mA max

$R_{19} = 10(1.015) = 10.2$ OHM max.

$V_{12V} = 11.2V$ min.

<u>-16V:</u> $V_{-16V} = -((94T/90T)V_{pri} - VF_{CR14})$

$V_{pri} = 16.5V \; +.3V, -.5V$

$V_{FCR14} = 1V$ max

$V_{-16V} = -16.5V$ typ., $-15.7V$ min, $-17.0V$ max.

<u>+5V:</u> $V_{5V} = V_{ref02}$

$dV_{ref02} = (15mV^2 + 8mV^2 + 10mV^2 + 10mV^2)^{1/2} = +/- 22mV$

Summary:

$\mathbf{V_{13V} = 13.2V +/- 1.1V}$

$\mathbf{V_{-13V} = -13.2V +/- 1.1V}$

$\mathbf{V_{12V} = 11.2V}$ **min**

$\mathbf{V_{-16V} = -16.5V -.5V, +.8V}$

$\mathbf{V_{5V} = 5V +/- 22mV}$

<u>Headroom</u>:

<u>+13V</u>: $V_{ECQ4} = (94T/90T)V_{pri} - V_{FCR16} - V_{R9+R10} - V_{+13V}$

$\mathbf{V_{ECQ4} = (94T/90T)16V - 1V - .3V - 14.3V = 1.1V}$

<u>+5V</u>: $\mathbf{V_H = V_{12V} - V_{5V} = 11.2V - 5.02V = 6.2V}$

<u>-13V</u>: **By similiarity, the -13V headroom is 1.1V**

The 5V headroom is more than sufficient for good regulaton. The +/- 13V headroom is also adequate since the +/- 13 V

regulators are configured as a darlington pair requiring only 1 volt of headroom to maintain good regulation.

+/- 13V Regulator gain requirements:

For this analysis:

$I_{p1N5290} = .47mA - (.047mA^2 + .094mA^2 + .047mA^2 + .023mA^2)^{1/2}$

$I_{p1N5290} = .35mA$

$I_B = .35mA - .25mA = .10mA$

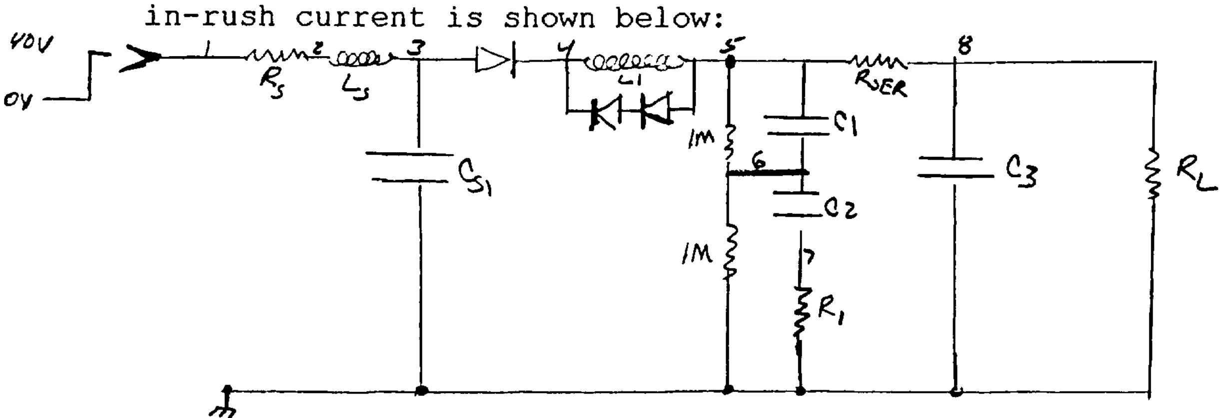
$h_{FE2N4236} = ((1/60(.75)(.85)) + .01))^{-1} = 29$

$h_{FE2N4239} = ((1/30(.70)(.85)) + .005))^{-1} = 17$

$h_{FE2N4236}(h_{FE2N4239})I_B = 29(17)(.10mA) = 49mA$ which is adequate since the loading is 35mA max. Thus the base drive to the +/- 13V regulators is adequate.

5. IN RUSH CURRENT

PSPICE was used to simulate the expected worst case in-rush current. It is assumed that primary return is tied to chassis at the spacecraft. The circuit used to simulate the in-rush current is shown below:



Worst case component values are:

CS1 = 700pF

L1 = 178uH

C1 = C2 = 1.34uF

R1 = 4.93 OHM

C3 = 25uF

RL = 214 OHM

RS = .06 OHM

RSER = 125 ohm

LS = 2uH

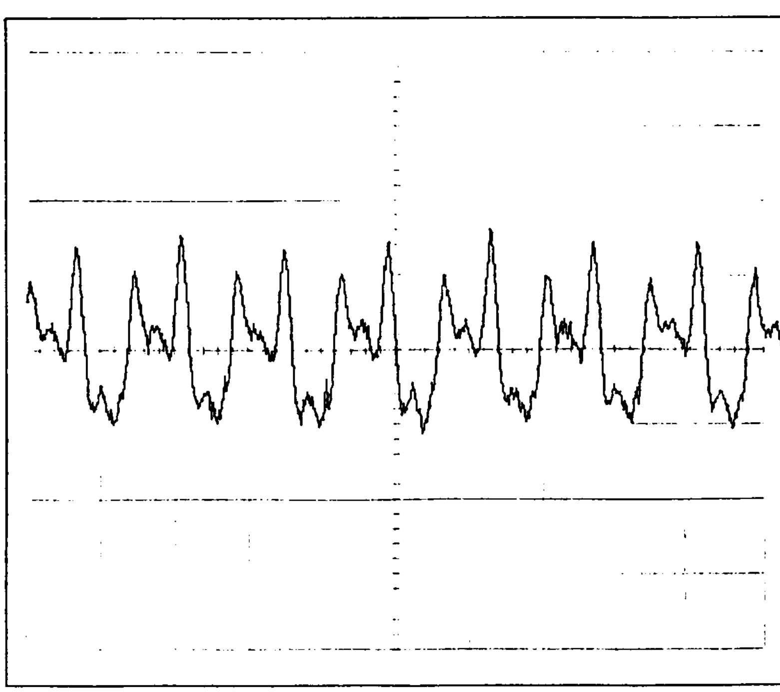
Figure 1. illustrates the predicted worst case in-rush current, note that the current is within TRMM 733-043 specifications.

Figure 2 illustrates the bread board measued in rush current.

6. INPUT CURRENT RIPPLE

The input current ripple was measured from the breadboard, rather than calculated. Reference the scope picture below:

MELCO/TRMM



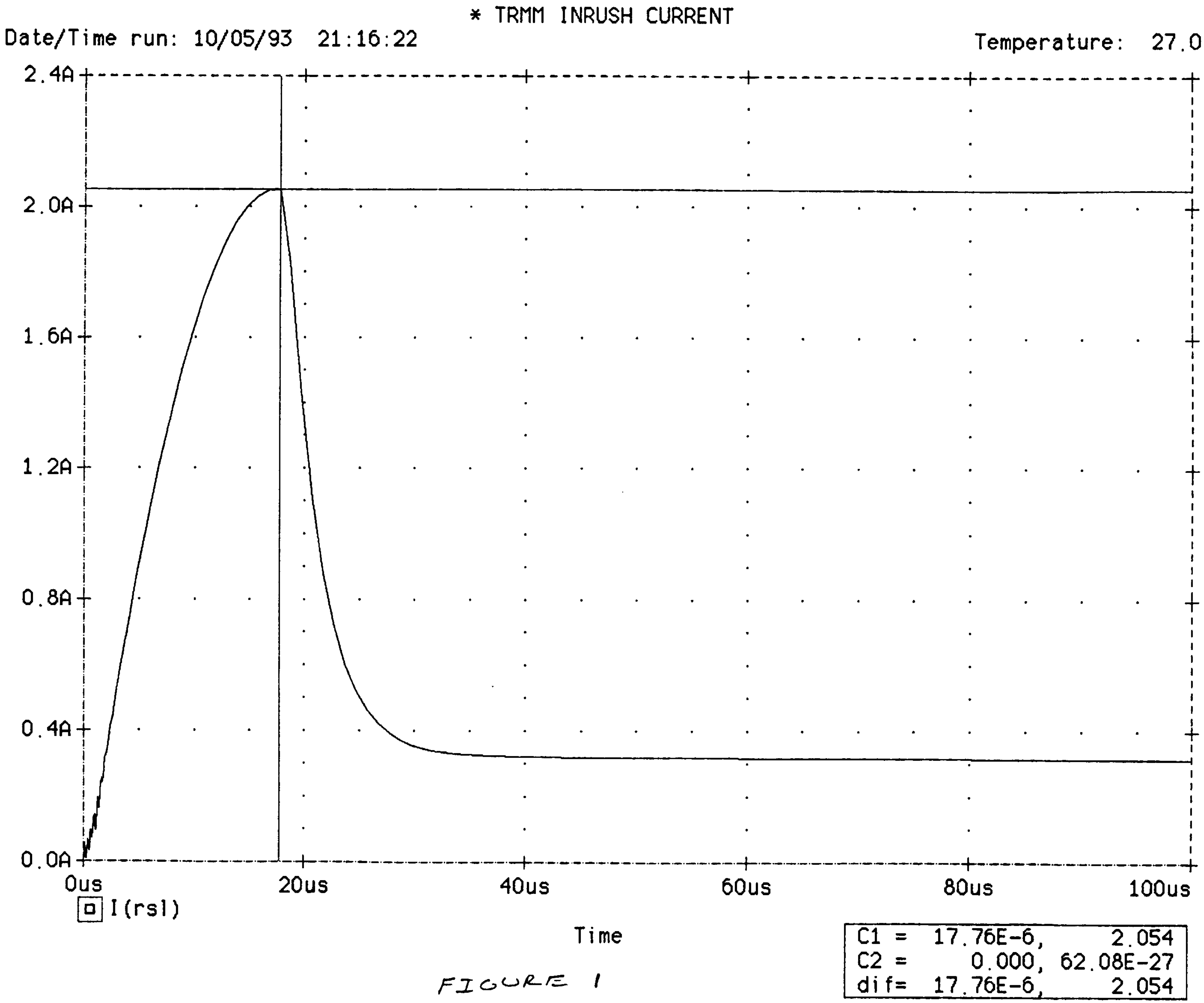
DATE:Nov 01/93

TIME:17:40:33

CH1: ~~10.0mV~~ :200us

2MA

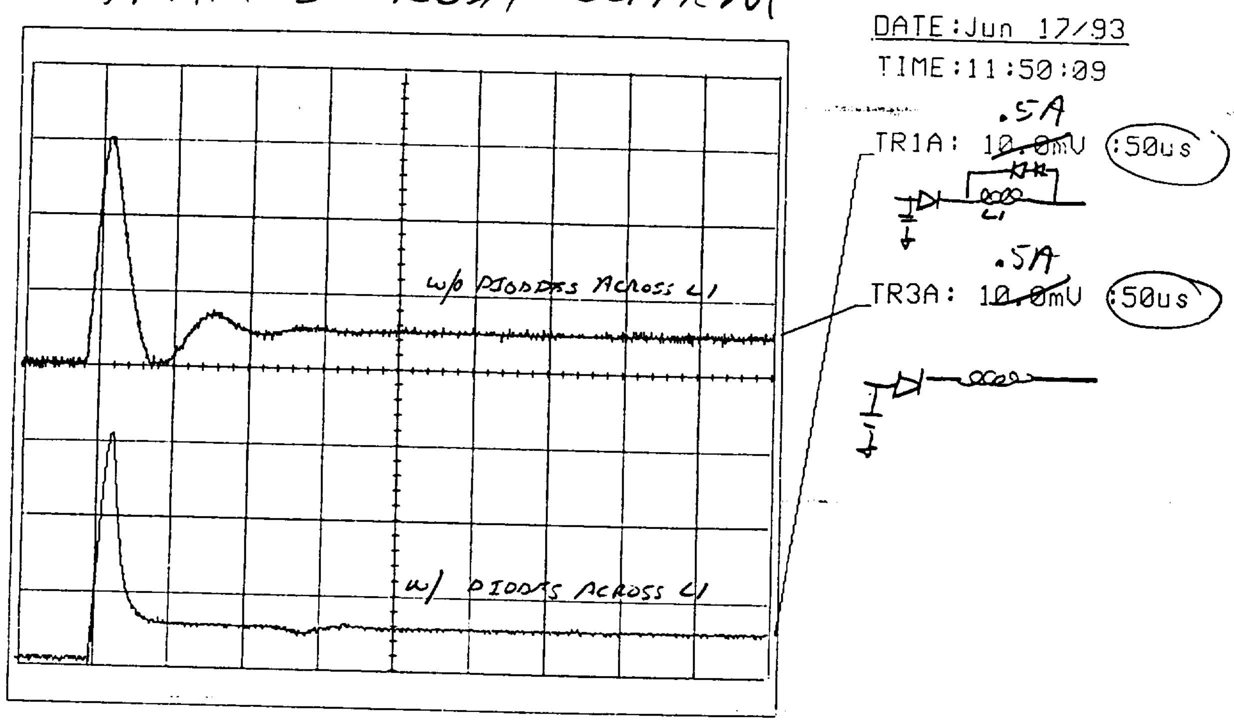
	ACROSS
+13v/619Ω	C4A
-13v/487Ω	C8A
+12v/374Ω (CRS HTR)	C10A



* TRMM INRUSH CURRENT
Date/Time run: 10/05/93 21:16:22
Temperature: 27.0
2.4A
2.0A
1.6A
1.2A
0.8A
0.4A
0.0A
0us
20us
40us
60us
80us
100us
I(rsl)
Time
C1 = 17.76E-6, 2.054
C2 = 0.000, 62.08E-27
dif= 17.76E-6, 2.054

FIGURE 1

TRMM-INRUSH CURRENT



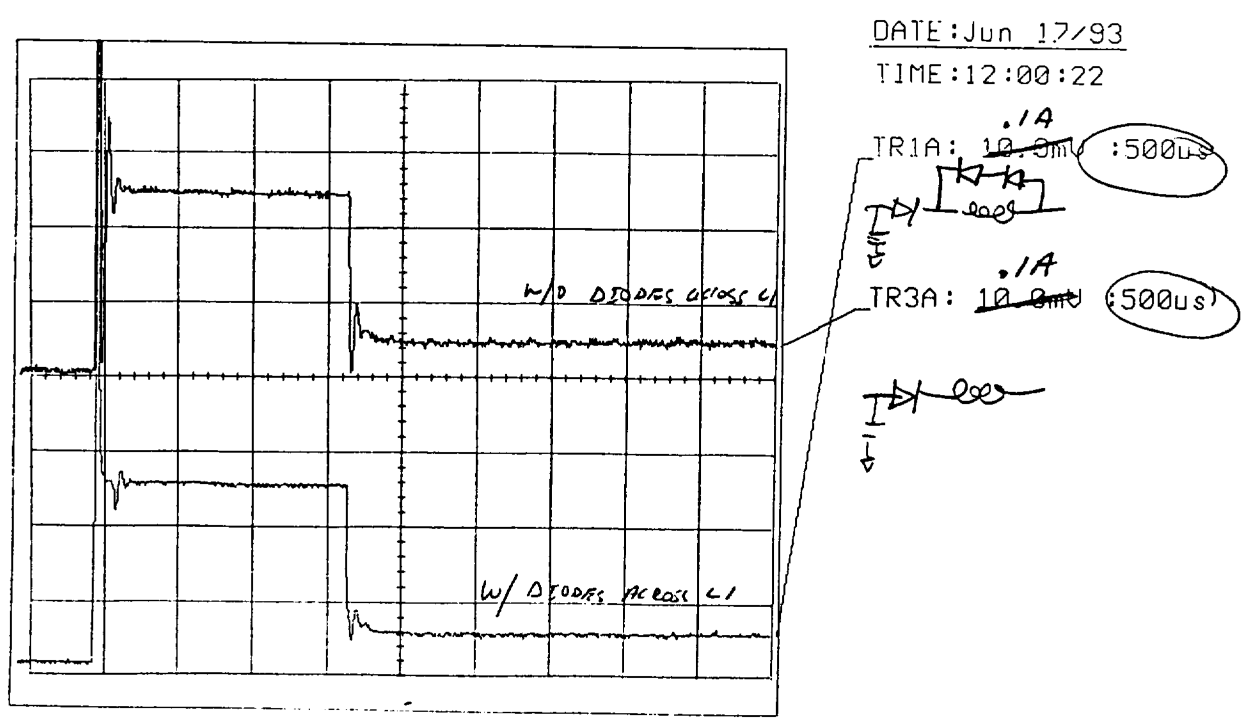


FIGURE 2

A3 A/D CONVERSION BOARD

TOPICS TO BE CONSIDERED

1. DEMOD STAGE

   A. DEMOD REJECTION CAPABILITIES AND CHARACTERISTICS

   B. A/D CONVERSION ERROR RELATED TO DEMOD OFFSETS

   C. DEMOD LOGIC REQUIREMENTS

2. INTEGRATOR STAGE

   A. INTEGRATOR LOGIC REQUIREMENTS

   B. A/D CONVERSION ERROR RELATED TO INTEGRATOR OFFSETS

   C. A/D CONVERSION ERROR RELATED TO FINITE OPEN LOOP GAIN AND BANDWIDTH

3. COMPARATOR STAGE

   A. COMPARATOR LOGIC REQUIREMENTS

   B. A/D CONVERSION ERROR RELATED TO COMPARATOR OFFSETS

4. SYSTEM CONSIDERATIONS

   A. PITCH/ROLL ERROR ASSOCIATED WITH A/D CONVERSION ERROR

1. DEMOD STAGE

A. DEMOD REJECTION CAPABILITIES AND CHARACTERISTICS

The A/D convertor is seperated into three major blocks. The first block is the demod stage which is followed by an integrator stage and a comparator stage, The integrator and comparator are configured as a standard dual slope A/D convertor.

The demod's purpose is to eliminate pre-amp dc offset, reject noise outside of the pass band of the system, and reject any signal which varies in a linear fashion with respect to time. The demod is able to accomplish its rejection characteristics by swithing between a gain of 1 and -1/2. The pre-amp signal, which precedes the demod, is a series of twelve detector signals interlaced with a ground sample between each detector sample at an ac chop rate of 25hz. The demod's gain is 1 during the detector signal sample and -1/2 during the ground sample.

DC REJECTION

To illustrate how the demod rejects pre-amp dc offset in the A/D conversion scheme, consider the following analysis:

The pre-amp input to the demod is given by the equations below:

$V_{pre} = V_{pre(os)}$ for $0 < t < T$ (during the ground look, only pre-amp dc offset is present)

$V_{pre} = V_{pre(os)} + V_{det}$ for $T < t < 2T$ (during the detector look, there is signal + offset)

$V_{pre} = V_{pre(os)}$ for $2T < t < 3T$ (only dc offset is present at the second ground sample)

The above equations represent the A/D conversion sequence of a single detector field. T is the sampling time constant equall to 15m-sec.

The demod output, neglecting for now the fixed electronic offset, is given by:

$V_{dem} = -.5*V_{pre(os)}$ $0 < t < T$

$V_{dem} = V_{pre(os)} + V_{det}$ $T < t < 2T$

$V_{dem} = -.5*V_{pre(os)}$ $2T < t < 3T$

The above equations represent the input to the integrator, at the end of the third integration cycle the output of the integrator is given by:

$$V_{INT} = (-1/T)\left[-\frac{1}{2}\int_0^T V_{pre(os)}\,dt + \int_T^{2T} (V_{pre(os)} + V_{det})\,dt - \frac{1}{2}\int_{2T}^{3T} V_{pre(os)}\,dt \right]$$

$$V_{INT} = (-1/T)\left[-\frac{T}{2} V_{pre(os)} + T(V_{pre(os)} + V_{det}) - \frac{T}{2} V_{pre(os)} \right] = -V_{det}$$

Note that the preamp offset term present on both the ground sample and the detector sample is rejected since the output of the integrator at $t = 3T$ is simply $-V_{det}$.

What makes the dc rejection imperfect is the fact that the demod gains are not precisely -.5 and 1. Initial tolerances in the demod gains can be accounted for and calibrated out of the system, but changes in the demod gains due to other effects will result in A/D conversion error. The delta dc A/D conversion error associated with preamp offset and demod gain drift is given by:

$$dV_{dem(os)} = (1-(2R_{7A}/R_{7B}))dV_{pre(os)}$$

$$R_{7A} = 15K(1 - (3PPM/C)(40C) - .001)$$

$$R_{7B} = 30K(1 + (3PPM/C)(40C) + .001)$$

$$V_{dem(os)} = .002(dV_{pre(os)})$$

$dV_{pre(os)}$ = 256mV by an earlier calculation on the A1 board.

$dV_{dem(os)}$ = .002(256mV) = .5mV.

.5mV(1count/.31mV) = 1.6 counts.

So the worst case A/D conversion error attributed to preamp offset is 1.6 counts.

<u>FREQUENCY REJECTION CAPABILITIES OF THE DEMOD</u>

In addition to the demod's ability to reject dc, the demod is also able to reject many other frequencies which are common to the ground reference and detector sample.

As a point of interest, the relative rejection of the demod can be plotted as a function of frequency.

For this analysis, we will assume that the input to the demod is a 1 volt amplitude cosine function given by Vpre = cos(2(pi)ft).

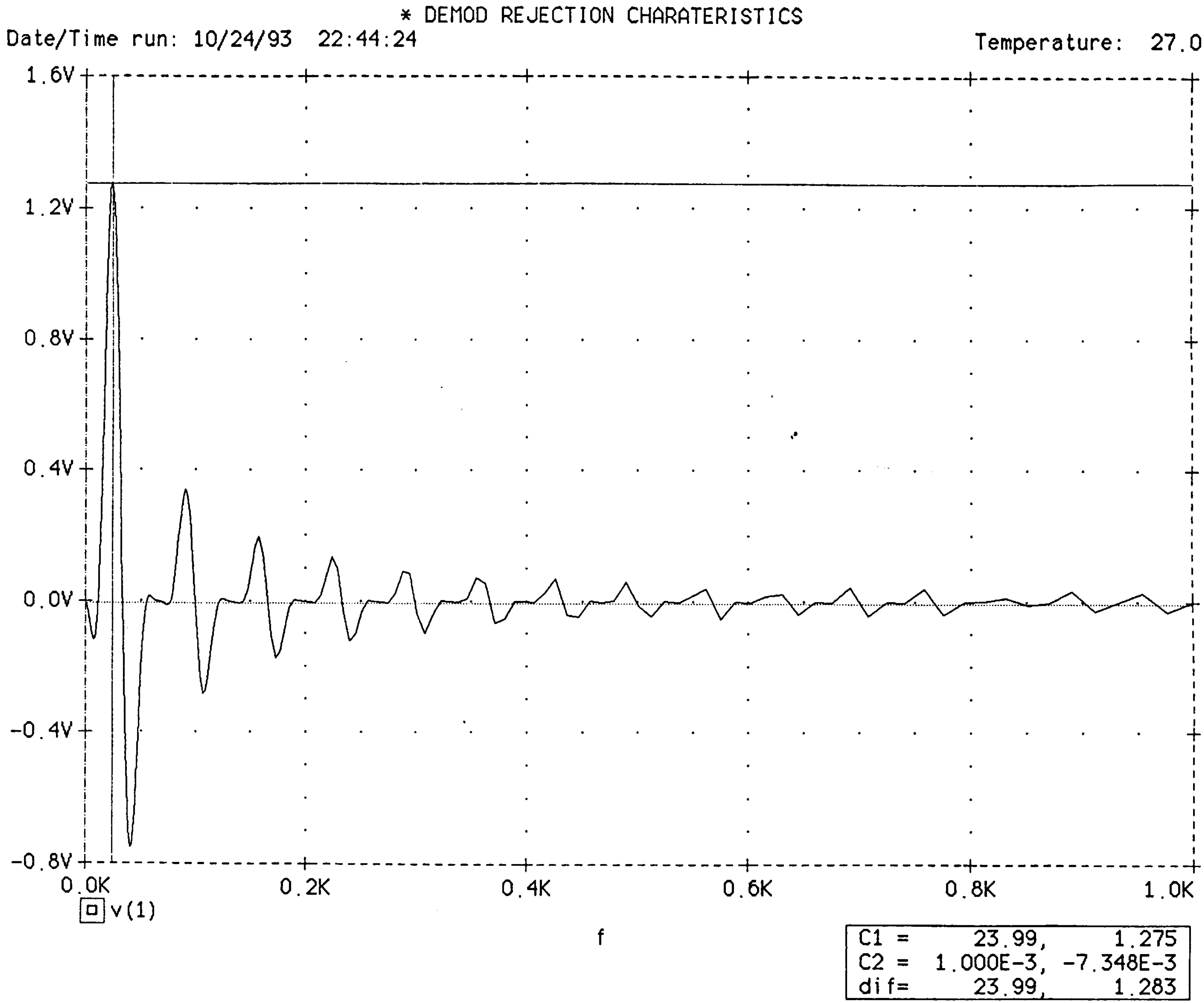
At the end of the third integration cycle of the integrator, the output of the integrator is given by:

$$V_{INT} = (-1/T)[\ -\tfrac{1}{2}\int_0^T \cos 2\pi f t\, dt + \int_T^{2T} \cos 2\pi f t\, dt - \tfrac{1}{2}\int_{2T}^{3T} \cos 2\pi f t\, dt\,]$$

$$V_{INT} = \frac{-1}{2\pi f T}\left[\ \frac{3}{2}(\sin 4\pi T f - \sin 2\pi T f) - \frac{1}{2}\sin 6\pi T f\ \right]$$

where T = 15m-sec

The above equation can be plotted as a funtion of frequency, to gauge the relative rejection of the demod as a funtion of frequency.(Reference figure 1).


* DEMOD REJECTION CHARATERISTICS
Date/Time run: 10/24/93 22:44:24
Temperature: 27.0
1.6V
1.2V
0.8V
0.4V
0.0V
-0.4V
-0.8V
0.0K
0.2K
0.4K
0.6K
0.8K
1.0K
v(1)
f
C1 = 23.99, 1.275
C2 = 1.000E-3, -7.348E-3
dif= 23.99, 1.283

Note that the frequencies in the neighborhood of the 25hz detector sampling ac chop frequency will introduce the greatest A/D conversion error.

Also, another interesting rejection characteristic of the demod is the demod's ability to reject any signal which varies linearly with time. Thus, the demod does a fairly good job of rejecting a slow eponential decay in so far as a slow exponential approximates a linear decay.

B. A/D CONVERSION ERROR RELATED TO DEMOD OFFSETS

Offset votages and currents, as well as bias and leakage currents associated with the circuitry surrounding the demod will contribute to A/D converion error. During the sampling of the detector, the dc offset at the output of the demod is given by:

$$V_{dem(d)} = (1 + (R_{7A}/R_{7B}))V_{os(u1)} + R_{7A}(I_{os(u1)} - I_{d(off)q3})$$

During each of the two ground samples, the offset at the output of the demod is given by:

$$V_{dem(g)} = [1 + (R_{7A}/R_{7B})][R_{47}/(R_{47} + R_{48})]V_{Zcr15} + R_{7A}[I_{os(u1)} + I_{d(off)q1}]$$
$$+ [1+ (R_{7A}/R_{7B})V_{os(u1)}]$$

The total offset at the output of the integrator at the end of the third integration cycle is given by:

$$V_{TOT} = V_{dem(d)} + 2V_{dem(g)}$$

This follows because during the A/D conversion sequence of a single field, the detector is integrated once for T = 15m-sec, and the ground reference is integrated in two seperate 15m-sec integration periods. Also, note that the integrator time constant is 15m-sec.

Thus, the total A/D dc offset at the output of the integrator just before runout, attributed to the demod's offset is given by:

$$V_{TOT} = 2[1+ (R_{7A}/R_{7B})][R_{47}/(R_{47} + R_{48})]V_{Zcr15}$$
$$+ 3[1 + (R_{7A}/R_{7B})][V_{os(u1)}] + 3\, R_{7A}(I_{os(u1)})$$
$$- 2R_{7A}I_{d(off)q1} - R_{7A}I_{d(off)q3}$$

The first term in the above expression represents the intentional fixed electronic offset of the electronics. The nominal value of the fixed electronic offset is given by:

$V_{ETO} = 2(3/2)(1/101)(8.4V)(1count/.31mV) = 805$ counts.

The remaining terms in the total integrator offset contribute to A/D conversion error, by introducing additional counts to every detector field digital output. However, only changes in the A/D conversion error should be considered since initial tolerances can be calibrated out of the system.

Therefore, the delta total offset at the output of the integrator is given by:

$$dV_{TOT} = .03dV_{Zcr15} + 4.5dV_{os(u1)} + 45K(dI_{os(u1)}) - 30K(dI_{d(off)q1}) - 15K(dI_{d(off)q3})$$

$$dV_{Zcr15} = (temp^2 + age^2 + rad^2)^{1/2}$$

$$dV_{Zcr15} = [40C(.0001)(8.4V)^2 + (.005(8.4V))^2 + (.18V)^2]^{1/2} = .2V$$

$$dV_{os(u1)} = [(40C(5uV/C))^2 + (.05mV)^2 + (1.6mV)^2]^{1/2} = 1.6mV$$

$$dI_{os(u1)} = [(40C(2.5pA/C)^2 + (20pA)^2 + (1.9nA)^2]^{1/2} = 1.9nA$$

$$dI_{d(off)q1} = dI_{d(off)q3} = [(3750pA)^2 + (25pA)^2 + (2152pA)^2]^{1/2} = 4.3nA$$

$$dV_{TOT}(RSS) = [(6mV)^2 + (7.2mV)^2 + (.09mV)^2 + (.14mV)^2 + (.07mV)^2]^{1/2} = 9.4mV$$

Thus, the total A/D conversion error attributed to demod offsets is 9.4mV(1count/.31mV) = 30 counts.

C. DEMOD SWITCHING REQUIREMENTS

The gain of the demod is selected by two mutually exclusive swithes(q1 and q3). The switches are controlled by the DEMOD DET command, which switches between a high logic level of 0V and a low logic level of -13V. It must be verified that under worst case conditions, q1 and q3 can be turned on or off.

Thus, if q3 is off:

$$V_{g(q3)} = V_{IL} + 264K(I_{gss(q3)})$$

$V_{IL} = V_{-13V(min)} + 50mV = -12.1 + .05 = -12.05mV$

$I_{gss(q3)} = 2^{(40C/10C)}(.25nA) + .025nA + .32nA = 4.3nA$

$V_{g(q3)} = -12.05V + 264K(4.3nA) = -12.05V$

$V_{s(q3)} = (1K/101K)(8.4V) = 80mV$

$V_{gs(q3)} = V_{g(q3)} - V_{s(q3)} = -12.05V + .08V = -11.97V$

The gate to scource threshold voltage is given by:

$V_{gs(th)q3} = \text{spec} - (\text{temp}^2 + \text{age}^2 + \text{rad}^2)^{1/2}$

$V_{gs(th)q3} = -3V - ((.2V)^2 + (.3V)^2 + (.3V)^2)^{1/2} = -3.5V$

Therefore, the gate to scouce voltage is sufficient to turn q3 off.

Q3 is turned on when the gate to scource voltage is between 0V and -500mV. To conservatively insure that q3 can be turned on, the gate to source voltage should not exceed -200mV in the negative direction. Since the logic which drives q3 is CMOS, the high level voltage will be within 50mV of the 0V input rail. So, the gate to source voltage across q3 in the on state is -50mV - 80mV = -130mV. Thus, q3 can be turned on under worst case conditions.

Q1 is turneed on or off by the state of q2. If q2 is on(i.e. q1 is off) the available base drive to q2 is given by:

$I_{b(q2)} = [(V_{in} - V_{be(q2)} - V_{-13V})/R_1] - (V_{be(q2)}/R_2)$

$V_{in} = -50mV$

$V_{be(q2)} = .8V + ((.07V)^2 + (.08V)^2 + (.01V)^2)^{1/2} = .9V$

$V_{-13V} = -12.1V$

$I_{b(q2)} = [(-.05V - .9V + 12.1V)/69.6K] - (.9V/9.77K) = 68uA$

$h_{FE(q2)} = [(1/35(.75)(.85) + .063)]^{-1} = 9.3$

$I_{C(q2)} = 9.3(68uA) = .63mA$, but $I_{C(q2)}$ max is 25V/120K = .21mA. So, q2 is in saturation.

$V_{ce(sat)q2} = .3V + ((.02V)^2 + (.04V)^2 + (.01V)^2)^{1/2} = .34V$

$V_{g(q1)} = V_{c(q2)} = V_{-13V} + V_{ce(sat)q2} = -12.1V + .34V = -11.8V$

Vs(q1) = -5V worst case, for a maximum preamp signal output.

$V_{gs(q1)} = -11.8V + 5V = -6.8V$, **which is more than adequate since q1's threshold voltage is -3.5V.**

Q1 is turned on when q2 is off. For this case, collector to emitter cut-off current(I_{cex}) will flow through R3. The spec limit for Icex is approximately 3.8uA at 60V, 65C. At 25V, the cut-off current will be approximately (25V/60V)3.8uA = 1.6uA. Thus, the voltage drop across R3 is V_{R3} = 120K(1.6uA) = 192mV = $V_{gs(q1)}$, which above the threshold of -500mV. Therefore, q1 will not be unintentionally biased on when q2 is off.

2. INTEGRATOR STAGE

A. INTEGRATOR LOGIC REQUIREMENTS

The input to the integrator is controled by three switches which control the integration time, run out time, and overange function. The circuitry for the three switches is identical, so only the switch composed of q8 and q9 will be analyzed.

Q8 is shut off by turning q9 on; the available base drive to q9 is 68uA worst case. Also, the gain of q9 at a collector current of 1mA is given by:

$h_{FE(q9)} = [1/h_{FE}(\text{pre-rad}) + d(1/h_{FE}(\text{post rad})]^{-1}$

$h_{FE(q9)} = [1/50(.8)(.85) + .02]^{-1} = 20$

$I_{C(q9)max} = 1mA + [(.1mA)^2 + (0mA)^2 + (.1mA)^2 + (.05mA)^2]^{1/2} = 1.15mA$

$h_{FE(q9)}\, I_{b(q9)} = 20(68uA) = 1.4mA > 1.15mA$, so q9 is in saturation.

Thus, $V_{c(q9)} = -12.1V + .34V = -11.8V = V_{g(q8)}$

Also, $V_{gs(th)q8} = -3V - [(.1V)^2 + (.3V)^2 + (.3V)^2]^{1/2} = -3.4V$

The worst case input to the source of any of the three switches preceding the integrator is V_s = -7.5V . Thus V_{gs} = -11.8V + 7.5V = -4.3 which is adequate to turn off q8. Thus, by similiarity. all three of the switches preceeding the integrator can function under worst case conditions.

B. A/D CONVERSION ERROR RELATED TO INTEGRATOR OFFSETS

Offset voltages, and leakage currents during the integrate and hold times of the integrator will contribute to A/D conversion error. Initial tolerances can be accounted for and calibrated out of the system, but changes in offsets and leakage currents will contribute to A/D conversion error. The delta A/D conversion error (in counts) due to these effects is given by:

$$dN = (3T/V_{run})f_{a/d}[(R_{15} - R_{16})dI_{b(u2)} + dV_{os(u2)} + R_{15}(dI_{d(off)q4}]$$

$$+ (3R_{15}t_h f_{a/d}/V_{run})[dI_{b(u2)} + dI_{d(off)q4} + dI_{d(off)q6} + dI_{d(off)q8}]$$

Where

$f_{a/d}$ = the A/D conversion frequency = 1.59Mhz
T = the period of one of the three integrate times = 15msec
t_h = the period of one of the three hold times following each integration period = 5msec
V_{run} = the reference run-out voltage = 7.42V
dI_b = the LM108A delta bias current = 15nA (reference the A2 board calculations)
dV_{os} = the LM108A delta offset voltage = 1.6mV (reference the A2 board calculatins)
$dI_{d(off)}$ = the 2N4393 switch leakage current

$dI_{d(off)2N4393} = (temp^2 + age^2 + rad^2)^{1/2} = (1.6nA^2 + .02nA^2 + 1.2nA^2)^{1/2} = 2nA$

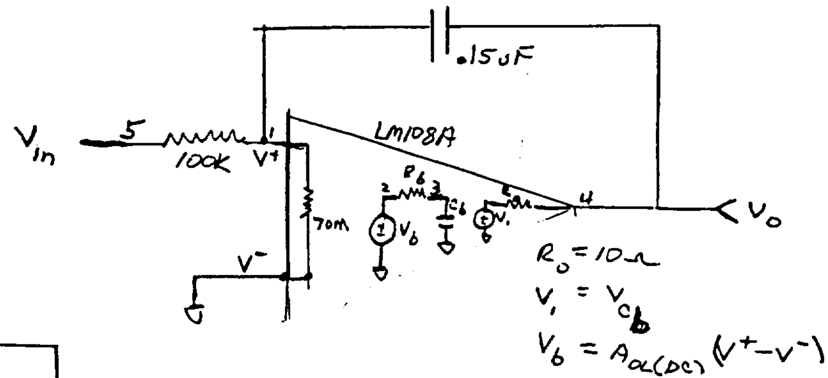
R15 = 1.023(100k) = 102K, R16 = 1.023(178K) = 182K

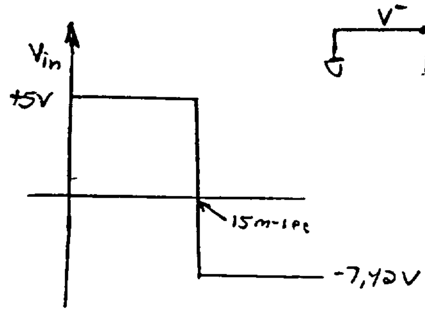
$dN(rss) = [11.6^2 + 15.4^2 + 1.9^2 + 5^2 + .7^2 + .7^2 + .7^2]^{1/2}$ = 20counts

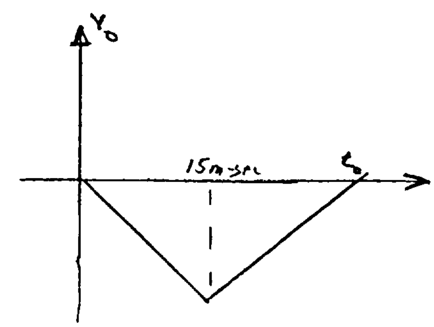
B. A/D CONVERSION ERROR RELATED TO FINITE GAIN AND BW

Since the integrator is not ideal, changes in open loop gain and bandwidth will contribute to delta A/D conversion error.

PSPICE was used to analyze the effects of finite gain and bandwidth. The circuit model used to evaluate this problem is shown below:







Note that the LM108A open loop frequency response was approximated by a single break. To evaluate the digitization error of the integrator, a maximum signal input of 5V was applied at node five for a 15msec integration period after which, the run-out voltage was applied until the resultant integrator output ran out to 0V. The open loop gain and unity gain bandwidth product of the integrator were varied to evaluate the change in A/D counts. The results of the simulation are tabulated below:

V_{in}	A_{OL}	$f_{0\text{-db}}$	$R_b C_b$	t_o	$N = (t_o - 15\text{msec})/.63\text{usec/count}$
-5V F.S.	infinity	infinity	0sec	25.1129msec	16,052.2counts
-5V F.S.	110db	650Khz	.078sec	25.113105msec	16,052.5counts
-5V F.S.	95db	520Khz	.017sec	25.11302msec	16,052.4counts

The first line in the above table represents the case for an ideal opamp. The second line represents the case for a typical LM108A opamp. Finally, the third line represents the case for a degraded LM108A opamp due to the effects of temperature, age, and radiation. The degraded parameter calculations are given below:

$dA_{OL} = (10db^2 + 11db^2 + 4db^2)^{1/2} = 15db$ So, $A_{OL} = 110db - 15db = 95db$.

$df_{0\text{-}db}$ = estimate 20% worst case

Note that the full scale output counts do not vary significantley from each of the three cases run. Thus, the effects of finite gain and bandwidth are neglible.

3 . COMPARATOR STAGE

A. COMPARATOR LOGIC REQUIREMENTS

Switches q10 and q12 alternate which of two integrator outputs is selected to go to the comparator, The switches are identical, so only one needs to be analyzed. Q10 is driven by the state of q11. So, the available base drive to q11 is given by:

$$I_{b(q11)} = [(V_{IH} - V_{z(cr6)} - V_{be(q11)} - V_{-16V})/R_{21}] - (V_{be(q11)}/R_{22})$$

$$I_{b(q11)} = [(-.05V - 10.8V - 1V + 15.7V)/36K)] - (1V/24K) = 65uA$$

$$h_{FE(q11)} = [(1/225(.60)(.85) + .002]^{-1} = 93$$

Since q11's max collector current is 300uA, q11 is saturated when the base drive is applied.

Thus , the voltage at the collector of q11 is given by:

$$V_{c(q11)} = V_{g\ (q10)} = V_{-16V} + V_{ce(sat)q11} = -15.7V + .34V = -15.36V$$

The worst case voltage at the source of q10, occurs when the sun interupts the field of view of a detector. For this case, it is conceivable that the voltage at the source of q10 comes close to within 1 volt of the -13V rail, or as high as -14.3V + 1V = -13.3V. Thus the gate to source voltage across q10 would be -15.36V + 13.3V = -2.06V worst case. This is not sufficient to keep the FET off, I suggest selecting the FET's at locations q10 and q12 for a tighter initial tolerance on the gate to source cut-off voltage. The FET's at these two locations on the A3 board, should be selected for a cut-off voltage which falls between -1.5V to -2.0V.

B. A/D CONVERSION ERROR ATTRIBUTED TO COMPARATOR OFFSETS

Shifts in the comparator threshold voltage will introduce A/D conversion error. The error is given by:

$$dN_{comp} = dV_{os(u3)}[1count/.31mV]$$

$dV_{os(u3)} = 12K(dI_{os(lm111)}) + dV_{os(lm111)}$

$dI_{os(lm111)} = [temp^2 + age^2 + rad^2]^{1/2} = [5nA^2 + 1nA^2 + 1.2nA^2]^{1/2} = 15.2nA$

$dV_{os(lm111)} = [temp^2 + age^2 + rad^2]^{1/2} = [1.0mV^2 + .3mV^2 + .5mV^2]^{1/2} = 1.4mV$

$\mathbf{dN_{comp} = [12K(15.2nA) + 1.4mV]\ (1count/.31mV) = 4.5counts}$

4. SYSTEM CONSIDERATIONS

The total A3 board rss A/D conversion error attributed to preamp offset, demod offset, integrator offset, and comparator offset is given by:

$dN_{A3} = [1.6^2 + 30^2 + 20^2 + 4.5^2]^{1/2} = 36counts$

The question now is can 36counts of A/D conversion error be tolerated?
To answer this question, we must take a look at the equations which determine pitch and roll. The equation for 2 field pitch or roll is given by:

$P_{2\text{-field}} = (.707)[X1 - X2]$

where X1 and X2 are the two horizon depression angles given by:

$X1 = 2\{[(A1\text{-}C) - K_{sa1}(S1 - C)]/[(A1 - C) - K_{sa1}(S1\text{-}C) + (B1\text{-}C) - K_{sb1}(S1\text{-}C)]\}$

$X2 = 2\{[(A2\text{-}C) - K_{sa2}(S2 - C)]/[(A2 - C) - K_{sa2}(S2\text{-}C) + (B2\text{-}C) - K_{sb2}(S2\text{-}C)]\}$

The A, B and S terms are the raw outputs from the earh sensor. C is the fixed electronic offset equall to 800counts nominal. The K terms are factors used to calibrate the system.

We shall only consider the pitch error at null attributed to 36counts of digitization error.

For an altitude of 350km nominal and at a pitch of 0degrees, the nominal raw data from the unit assuming a normalized detector height of 1deg. is approximately as follows:

A1 = 2000counts = A2

B1 = 5600counts = B2

S1 = 400counts = S2

Now, the A3 board A/D conversion error will be common to every detector field since every field is digitized at the A3 board. Thus, 36counts digitization error will be added to every field. If the K terms in the depression angle calculation were all equall to their nominal value of 1.0, the depression angle would not change since the 36counts will cancell when factored out of both the numerator and denominator. However, the K terms will in reality vary by approximately +/-10%.

Thus, the worst case condition for the K values are $K_{sb1} = .9$, $K_{sa1} = 1.1$, $K_{sb2} = 1.1$, $K_{sa2} = .9$.

Given these conditions, along with the fact that 36counts A/D conversion error is added to every field, the two field pitch at null is calculated below:

X1 = 2{[(2000 + 36 -800) -1.1(400 + 36 - 800)]/[(1636.4 + 5163.6)]} = .48129deg.

X2 = 2[1596/1596 +5236.4] = .46719deg.

So $P_{2\text{-field}}$ = .707(.48129 - .46719) = .01degrees at null.

Thus the worst case error attributed to adding 36counts to every detector field is approximately .01degrees at null, which is reasonable. Keep in mind that these calculations are very rough and just intended to give a ball park figure of what effects A/D conversion error might have on system performance.

A4 ORS/REF/TLM BOARD

TOPICS TO BE CONSIDERED

1. ORS and Temperature Telemetry

2. Reference Voltage Circuitry
   A. Switching Level Requirements
   B. Reference Voltage Tolerance

3. ORS Servo Loop
   A. Switching Logic Requirements
   B. Loop Offsets/ S field control variability
   C. Peak Detector Errors
   D. Heater Drive Capability

1. ORS and Temperature Telemetry

The telemetry specifications require that all of the spacecraft telemetry is redundant, capable of sustaining shorts to +/-15V or ground without any degradation to the redundant output, and buffered sufficiently to restrict the maximum output voltage to between -1V and 10V.

ORS Telemetry

The ors telemetry provides information on the level of the drive voltage to the heater, which is a funtion of the S field control set point, the heat lost too space,the gain from the heater to the S field detector, the gain from the detector to the preamp output, and most importantley, the flange temperature of the unit at the detector mount.

Output Voltage Range: 0V to 4.7V worst case

Shorts to +/-15V or Ground: Note that the outputs are well buffered and can sustain a short to -15V with a maximum current draw of 2.1mA from the 12V supply.

Redundancy: Note that there are two independent outputs and that the redundant output will not degrade as a result of the primary output being shorted to +/-15V or ground.

Temperature Telemetry

The temperature telemetry provides information on the temperature of the flange at the detector mount.

Output Voltage Range: -.6V to 8.6V worst case

Shorts to +/-15V or Ground: Note that the outputs are well buffered and can sustain a short to -15V with a maximum current draw of 2.9mA from the 13V supply.

Redundancy: Note that there are two independent outputs and that the LM101A is capable of maintaining the redundant output at normal voltage levels in the event that the primary output is shorted to +/-15V or ground.

2. Reference Voltage Circuitry:

The reference voltage circuitry is responsible for generating the reference run-out voltage used in the dual slope A/D. For normal operation, the reference voltage is at a nominal level of -7.42V. However, in the event that the signal from the integrator is positive, a command designated as POL CONT COMM is used to change the polarity of the reference voltage by turning off q11.

A. Switching Logic Requirements:

It must be verified that q11 can be shut off in order to change the polarity of the reference run-out voltage.

The max. gate to source threshold voltage of q11 is -3.5V as derived by an earlier A3 board calculation.

Also,

$$V_{f(cr12)} = .8V + [(.1V)^2 + .08V)^2 + .03V)^2]^{1/2} = .93V$$

$$V_{z(cr10)} = 8.4V + [(.42V)^2 + (.13V)^2 + (.04V)^2 + (.18V)^2]^{1/2} = 8.9V$$

$$V_{pol\ comm} = V_{-13V} + .05V = -12.1V + .05V = -12.05V$$

Thus, $V_{gs(q11)} = V_{pol\ comm} + V_{f(cr12)} + V_{z(cr10)} = -12.05V + .93V + 8.9V = -2.2V$

This voltage is not sufficient to turn off the FET under worst case conditions, I suggest selecting the FET for a lower initial threshold votage in the range of -1.5V to -2.0V to ensure proper operation of this circuit.

Tolerance:

Factors contributing to the reference voltage tolerance are drift in the gain resistors used to set the voltage, drift in the 1N3154 zener voltage, and dc offset associated with the LM101A amplifier. As usual, initial tolerance is no critical. The total delta due to these effects is given by:

$dV_{ref} = 90K(dI_{b(u4)}) + 2V_{os(u4)} + .9(dV_{z(cr10)}) + .0015(V_{z(cr10)})$

$dI_{b(u4)} = [temp^2 + age^2 + rad^2]^{1/2} = [25nA^2 + 8nA^2 + 375nA^2]^{1/2} = 376nA$

$dV_{os(u4)} = [.6mV^2 + .2mV^2 + 8mV^2]^{1/2} = 8mV$

$dV_{z(cr10)} = [.13V^2 + .04V^2 + .18V^2]^{1/2} = .23V$

$V_{z(cr10)} = 8.9V$

So, the delta change in the reference voltage is given by:

$dV_{ref} = 90K(376nA) + 2(8mV) + .9(.23V) + .0015(8.9V) = 270mV$
This change will effect the gain of the A/D by a percentage given by:

$G_{A/D}$(percent) = [(7.42/(7.42 - .27)) -1)](100) = 3.8%

Can a 3.8% system gain change be tolerated?
To answer this question, consider the simplified formula for the attitude depression angle, which is given by:

$X = 2h(A - S)/(A + B - 2S)$

Note that if A,B, and S were all inreased or decreased by 3.8%, the increase could be factored both from the numerator and denominator and cancelled. Thus, the depression angle calculation is very tolerant of a system gain change and a 3.8% gain change is tolerable.

One other thing to consider is that the timing of the system allows for a maximum run-out time of 20m-sec in the A/D conversion scheme before the next field is digitized. The run-out time for an overange condition is given by:

$t_{run} = 16{,}384counts(.63u\text{-}sec/cnt) + [(V_{max} - 5.08V)/2V_{ref}](1.07)R_{int}C_{int}$

The above formula is derived by noting that after the A/D makes it to 16,384counts, the circuitry realizes that if the output of the integrator is not run-out to 0V, the the over-range logic must kick in in which case the remaining voltage at the output of the integrator is run out twice as fast. The V_{max} term is equal to the max. 13V supply minus 1V or 13.3V.
The integrator time constant is 15m-sec nominal and 1.07(15m-sec) = 16.05m-sec max. The reference voltage will initially be trimmed to 7.42V +/- .02V and will drift a maximum of 270mV as derived above.

So, t_{run} = 10.33m-sec + 9.25m-sec = 19.6m-sec < 20m-sec So, the min. reference voltage level of 7.42V - .02V - .27V = 7.13V is acceptable.

3. ORS Servo Loop

A Switching Logic Requirements

The purpose of the ors servo loop is to maintain the detector loss to space at a fixed level by driving a heater at a power dictated by the coldest S-fiel detector sample. Since, all the detectors are exposed to the heater, the servo loop is able to compensate for and establish a fixed amount of heat lost to space for all the A,B, and S fields.

q1 and q2

Switches q1 and q2 are used to send the four S field outputs to the ors servo loop. The loop peak detector determines which of the four S fields is the coldest. The switches must be able to operate over worst case conditions.

The circuitry which controls the state of q1 and q2 is identical to the comparator switching logic already analyzed on the A3 board. The conclusion is the same, to ensure proper operation of q1 and q2, the FET's should be selected for an initial gate to source threshold voltage in the range of -1.5V to -2.0V.

q5 and q8

Q5 is used to reset the peak detector once per frame in order to obtain the new minimum S field on a per frame basis. The worst case available gate to source voltage available to shut off q5 is given by:

$V_{gs(q5)} = V_{-13V} + V_{f(cr3)} - V_{s(q5)}$ = -12.05V + 1V + 5.2V = -5.9V which is more than adequate.

Q8 is used to transfer the appropriate heater voltage to the heater on a once per frame basis. When q8 is off, the maximum voltage at the source of q8 is 11V. Also, the available gate drive to turn off q7 is -15.4V min. So the available gate to source voltage is -4.4V which is more than adequate.

B. Loop Offsets

Change in dc offsets in the servo loop will cause the S field set point to vary.

The delta dc offset of the first stage is given by:

$dV_{off1} = 90K(dI_{b(u1)}) + 2(dV_{os(u1)}) = 90K(15nA) + 2(1.6mV) = 4.6mV$

The dc offset of the second stage is given by:

$dV_{off2} = 102K(dI_{b(u2)}) + 2.6(dV_{os(u2)}) = 102K(15nA) + 2.6(1.6mV) = 5.7mV$

The dc offset of the third stage is given by:

$dV_{off3} = 231K(dI_{b(u3)}) + 16.8(dV_{os(u3)}) = 231K(15nA) + 16.8(1.6mV) = 30.4mV$

The total loop offset at the output of the final stage is given by:

$dV_{off(tot)} = 42dV_{off1} + 16.8dV_{off2} + dV_{off3} = 320mV$

The open loop gain of the servo loop will compensate for this offset, so the error in S field counts attributed to 320mV dc offset at the heater is given by:

dS = (1count/.31mV)(320mV/80) = 13counts, which is reasonable and will cause negligible pitch/roll error at null. The loss to space is just changed slightly, but all of the detectors are still referenced to the all space output and the depression angle calculation will cancel out the 13 count S field set point delta.

C. Peak Detector Errors

Capacitor C6 is responsible for peak detecting the coldest of the four S fields and must not be allowed to drift too much over a maximum hold time determined by the frame rate period or 500m-sec max. The drift in voltage at C6 is given by:

$dV_{c6} = [I_{dg(q6)} + I_{dg(q5)} - I_{r(cr4)}](500m\text{-}sec)/.042u$

$I_{dg(q6)}$ = spec at 65C + age + rad = 250pA(14V/20V)(16) + 562pA + 273pA = 3.6nA

$I_{dg(q5)}$ = 250pA(5V/20V)16 + 188pA + 97pA = 1.3nA

The above calculations assumes that the leakage is linear with applied voltage and doubles for every 10C and that the age derating is 300%.

The reverse leakage current for cr4 at 30V,125C is 300nA max. Assuming the current is linear with applied voltage and doubles for every 10C, the reverse 1N3595 current is given by:

$I_{r(cr4)}$ = (300nA/64)(14V/30V) + 1nA + .4nA = 3.6nA

So dV_{c6} = 15mV due to leakage currents. This delta divided by the gain of the first two stages is 3mV or about 10counts S field delta, which is acceptable.

Also, the time between when the first S field and last S field is entered into the peak detector is 360m-sec in which time the cap will leak 11mV. Referenced to the input to the first stage, the difference in counts between the first S field entered into the loop and the last is (11mV/5)(1cnt/.31mV) = 7counts. In order to prevent the peak detector from possibly always latching on to the last S field entered into the loop,a seven count spread between S fields is required, but this is reasonable delta between S fields.

D. Heater Drive Capability:

The minimium base drive available to the heater drive transistor is given by:

$I_{b(q10)} = I_{dss(q9)} - (1V/8K)$ = 5mA - .13mA = 4.87mA where the spec min for the zero voltage gate drive current for a 2N3972 is 5mA.

The required max. heater current is 11V/300ohm = 37mA

Thus the required dc gain of q10 is 37mA/4.87mA = 8

The available gain is given by:

$h_{FE(q10)} = 17$, which is determined by an earlier A2 board calculation.

Thus, the drive to the heater can support the worst case loading of the heater.

A5 DATA I/O AND LOGIC BOARD

TOPICS TO BE CONSIDERED

1. Data Clock Receiver and Line Sync Receiver
2. Data/Data Ready Circuitry
3. Changes to the Heritage Design to Support Dual Channel Simultaneos Operation

1. Data Clock/ Line Sync Inputs

As required by the specifications, the data clock receiver as well as the line sync. receiver allow for redundant inputs. The receiver design for both fuctions is basically just a LM193 comparator with a threshold voltage set at 2.4V and a dc hysteresis of .7V along with some ac hysteresis. The LM193 comparator has been used on many other programs at Barnes and is rad hard for TRMM's application to well in excess of 18KRAD. The offset and bias currents of the comparator are insignificant, considering that the threshold is appropriately set at 2.4V and the max level of the clock signal to be rejected by the circuitry is 1.0V as determined by the TRMM specifications.

2. Data/Data Ready Outputs

The data and data ready outputs are driven by a CD4041UB line driver, which remains unchanged from the heritage design. The only change is that the CD4041 is now powered by 5V to accomadate a 0 to 5V logic voltage output range. The outputs are buffered by 1K to the driver in order to sustain a short to +5V or ground without degrading the redundant output, as required by the TRMM specifications. The 5V which powers the outputs is derived by a REF02A which is exclusively dedicated to only the data and data ready outputs.

The REF02A can drive 10mA minimum, which is more than adequate. Also, the REF02A can sustain an indefinite short to ground as specified by PMI and the supply current is only 1mA typical, making the REF02A the ideal choice for this application.

Figure one on the following page illustrates the operation of the line sync and data clock receiver circuitry as taken from the bread board.

3. Dual Channel Operation

The TRMM specifications require that the design be capable of dual channel simultaneous operation. This required a few minor design changes from the basic heritage design.

To accomodate this requirement, the synchronazation of both channels to the falling edge of the line sync had to be tightned up.Further the series/shunt and demod logic had to be changed slightly to allow for slip between the two master oscillators in each channel.

The synchronation to the line sync. was tightned by clocking flip-flop U7 at a faster rate of 200Khz as opposed to the former 3.2Khz rate, this enabled the falling edge of the line sync to be clocked into the flip flop at the start of the frame within only a +/-5 u-sec period of the time at which the line sync falls low. The end of the frame relative to the falling edge of the line sync. was also tightned by re-setting counter U12 at the end of the frame in each channel.

After tightening up the start and end of the frame in each channel relative to the space-craft line sync, it was now possible to accomodate dual channel simultaneous operation by delaying the series/shunt logic to the middle of the hold times of the integrator. This change allowed for slip between the two master 1.6Mhz crystal oscillators in each channel. By delaying the series shunt logic, the common set of detectors to each channel could be sampled simultaneosly by each channel and the commutation glitches at the ouput of preamp of each channel due to the channels own series/shunt logic and the slip of the opposite channels series/shunt logic relative to the its own series/shunt logic could be accounted for and eleminated from causing A/D conversion error by always placing the commutation glitches in the middle of the hold times of the integrators used for the A/D.

All of these changes to the basic heritage design were bread-boarded to ensure that the design changes were appropriate.

Figures 2 through 9 on the following pages illustrate the concepts just dicussed.

Figure 2 and 3 shows the jitter at the start and end of frame relative to the line sync for the heritage design. The FRAME START signal rising and falling edges mark the start and end of the frame.

Figures 4 and 5 illustrate how with the modifications for the TRMM design, the jitter at the start and end of the 496m-sec frame period was eleminated.

Figure 6 illustrates the synchronazation of the U12 counter in the TRMM design.

Figure 7 illustrates the TRMM series/shunt logic relative to the integrate and hold times of the A3 board A/D integrator.

Figures 8 and 9 illustrate the end of frame waveforms showing how the two oscillators have slipped relative to each other; the slip of the two oscillators for the breadboard was exagerated by purposely adjusting the output frequencies of the breadboard LC oscillators to be different. The actual design will incorporate a crystal oscillator in each channel. Note that the slip of the timing between each channels series/shunt logic will be greatest at the end of the frame and this slip will induce an extra commutation spike in the preamp signal. But, as long as the commutation spike decays to zero by the end of the integrator hold time, the spike will not cause any digitization error. The total hold time period is 5m-sec and the delay will be set to between 2 to 2.5m-sec, allowing for a period of 3 to 2.5m-sec for the commutation spike to decay to zero.

Figure 10 illustrates the single channel period of the commutation spike at the output of the preamp caused by the series/shunt sampling of the detectors. Note that the spike decays to zero in about 1m-sec.

Analysis

channel slip

The slip between each of the two channels oscillators can not vary too much for reasons discussed above. The slip between each channels logic will be greatest at the end of the frame. The frame period is given by:

$T_{frame} = 128(128)(12)(4)/f_{osc}$

The oscillator specifications are:

init tol = 15ppm

age = 5ppm/yr(20yr) = 100ppm

temp = 50ppm for -20C to 70C operation

rad = ?

The radiation hardness of the oscillator must be verified at a later date. Neglecting the radiation degradatio for now, the difference between the length of the frame for each channel is given by:

dT = 786432{[1/1.585549M(1 - 165ppm)] - [1/1.585549M(1 + 165ppm)]}

dT = 165u-sec, this is an acceptable drift at the end of the frame, since the hold time of the integrators are long enough to accomodate this drift.

maximum time to achieve sync with the space-craft line sync

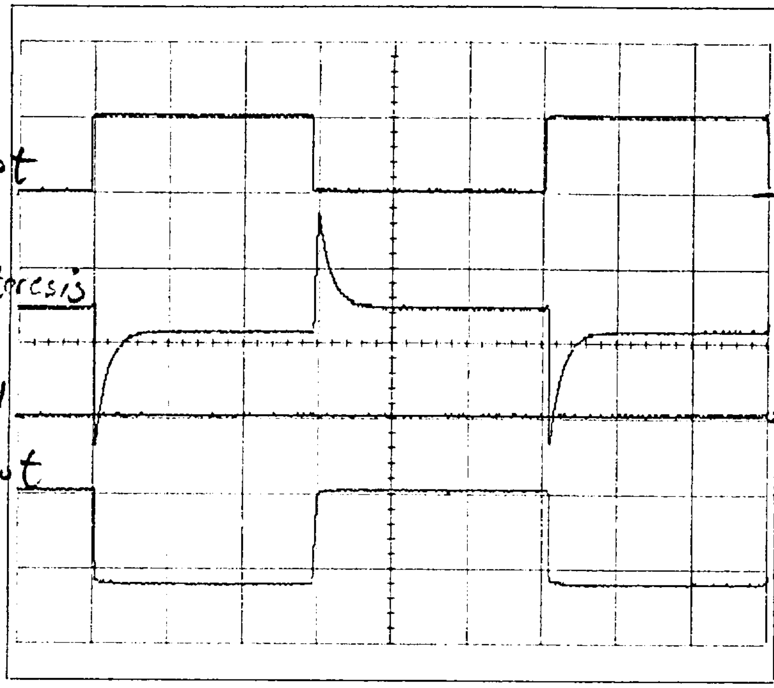
The unit achieves sync with the space-craft by starting the frame at the falling edge of the line sync in each channel. At power on, the detector field commutation logic, which is responsible for sending each sampled detector to the input of the series/shunt switch is in an arbitrary state. The commutation singnal 2S is used to lock the TRMM electronics to the space-craft. The time to lock up is dependent upon the period of the line sync. sent from the space-craft relative to the period of the frame for the TRMMESA electronics.

The worst case time to achieve synchronazation is given by:

$$T_s = [(T_{frame}/2)/(T_{I/s} - T_{frame})](T_{I/s}) = 45\text{seconds}$$

FIGURE 1

AS BD DATA CLK REC.

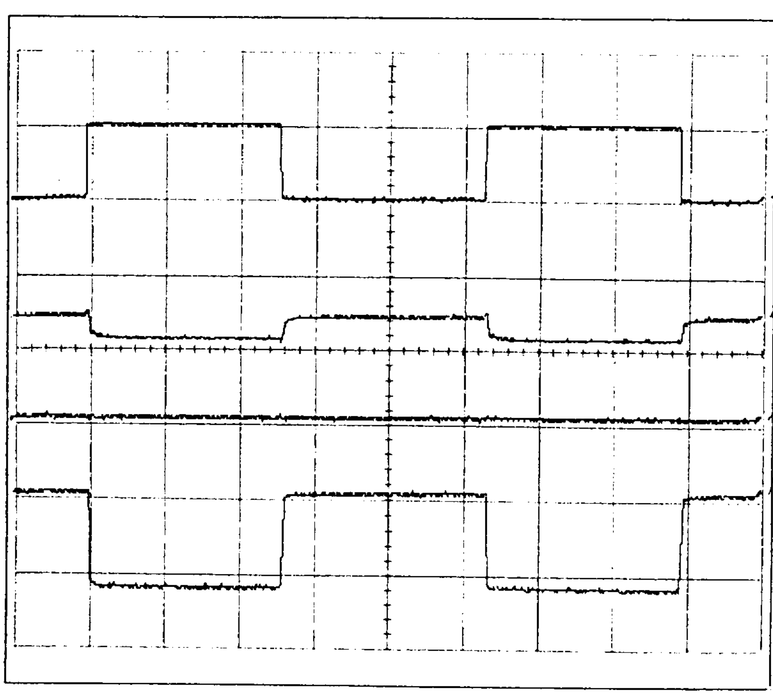


DATE:Jun 24/93
TIME:10:51:34

TR1A: 05.0V :10us
DATA CLK INPUT
TR2A: ~~0.20V~~ :10us, 2V
U15-5
TR3A: ~~1.00V~~ :10us, 10V
U15-7
TR4A: ~~02.0V~~ :10us
CH.2 GND REF

W/C11 IN
(as designed)

AS BD. DATA CLK REC.



DATE:Jun 24/93
TIME:11:30:58

TR1A: 05.0V :10us
DATA CLK INPUT
TR2A: ~~0.20V~~ :10us, 2V
U15-5
TR3A: ~~1.00V~~ :10us, 10V
U15-7
TR4A: ~~0.20V~~ :10us
CH.2 GND REF

W/C11 OUT
(extra information)

~~SAME PLOT~~

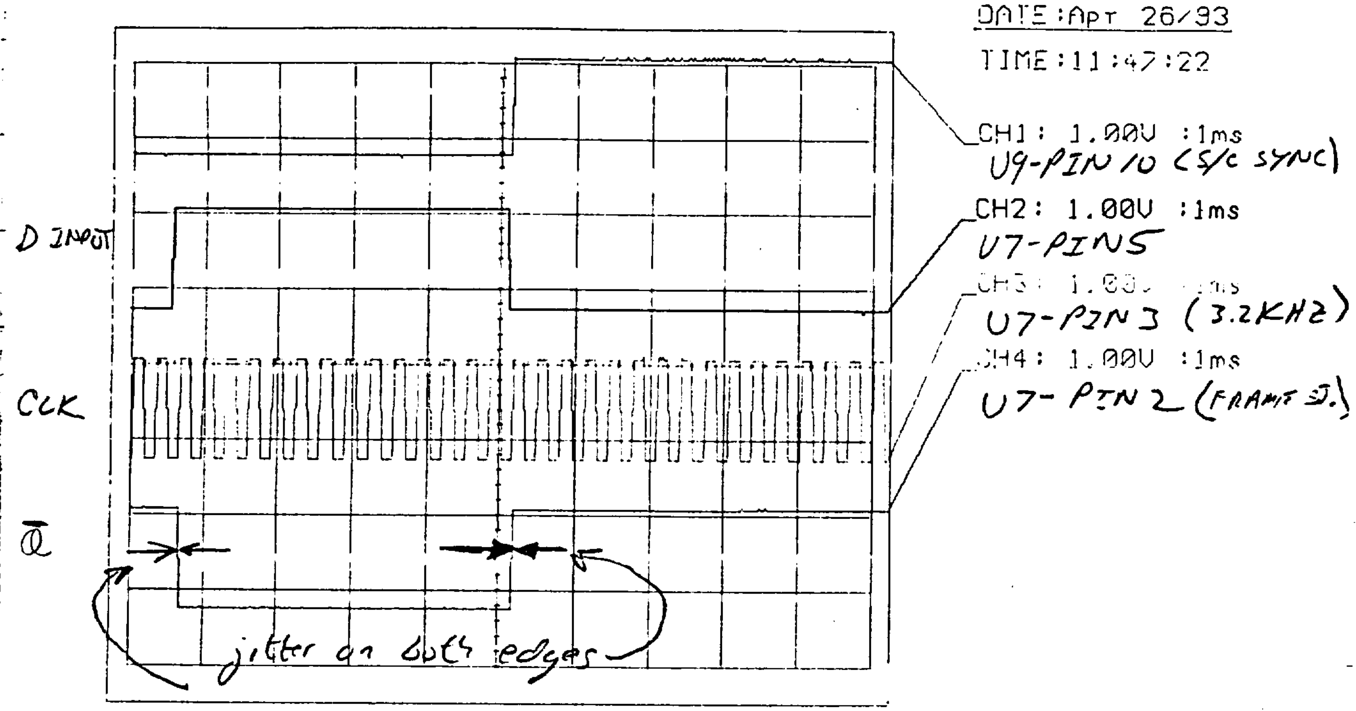


FIGURE 2

HERITAGE DESIGN START/END OF FRAME LOGIC.

JITTER ON START AND END OF FRAME IN HERITAGE DESIGN

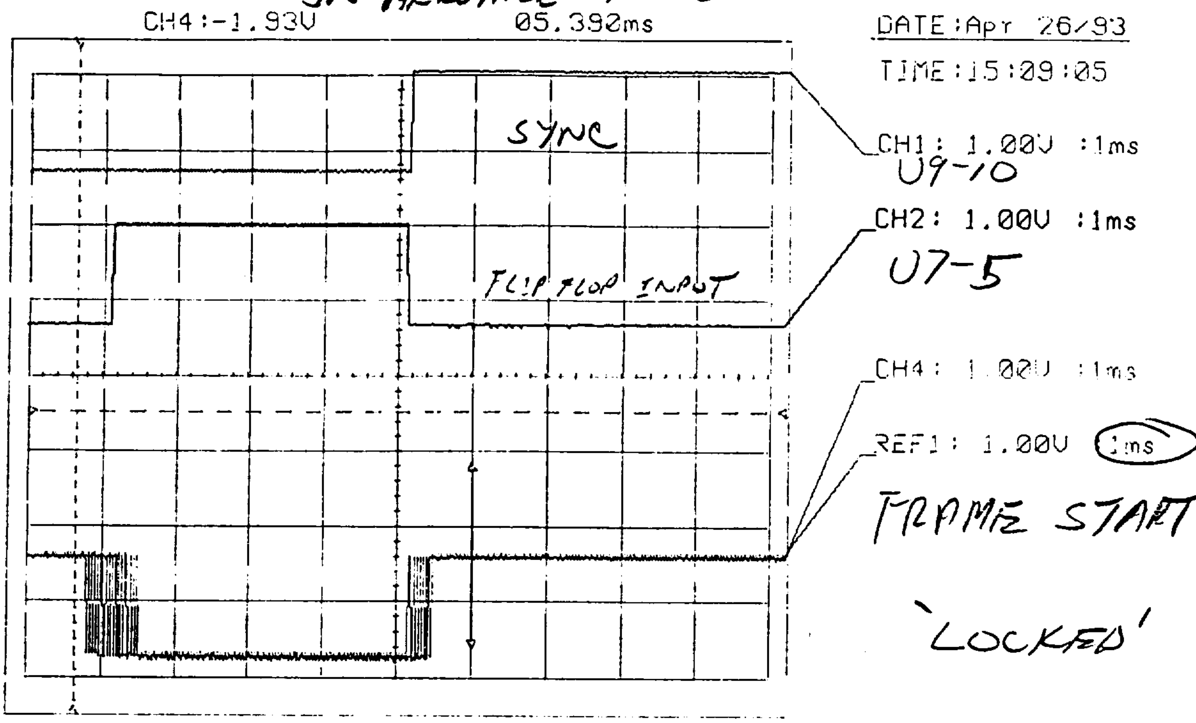


FIGURE 3

- Note jitter on both edges of FRAME START. Also, note the high to low edge has more jitter than the low to high edge.

TRMM DESIGN

CH I + II SYNCRONIZATION
w/ A5 BOARD MODIFICATION

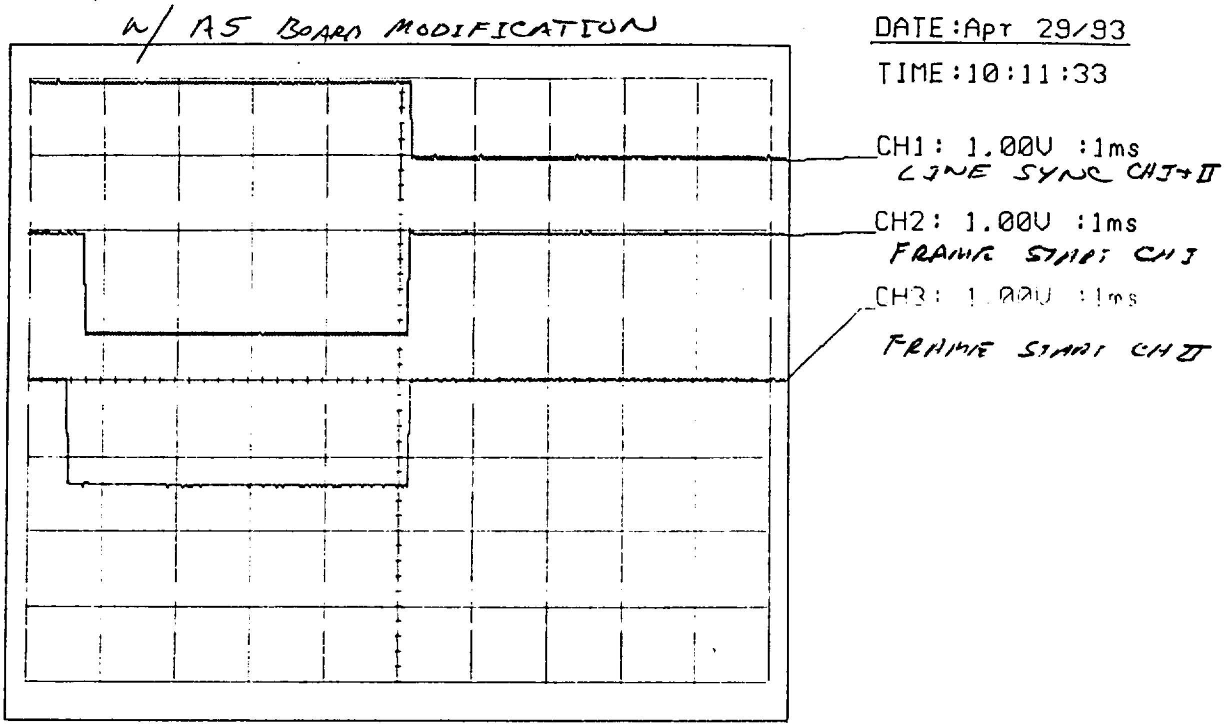


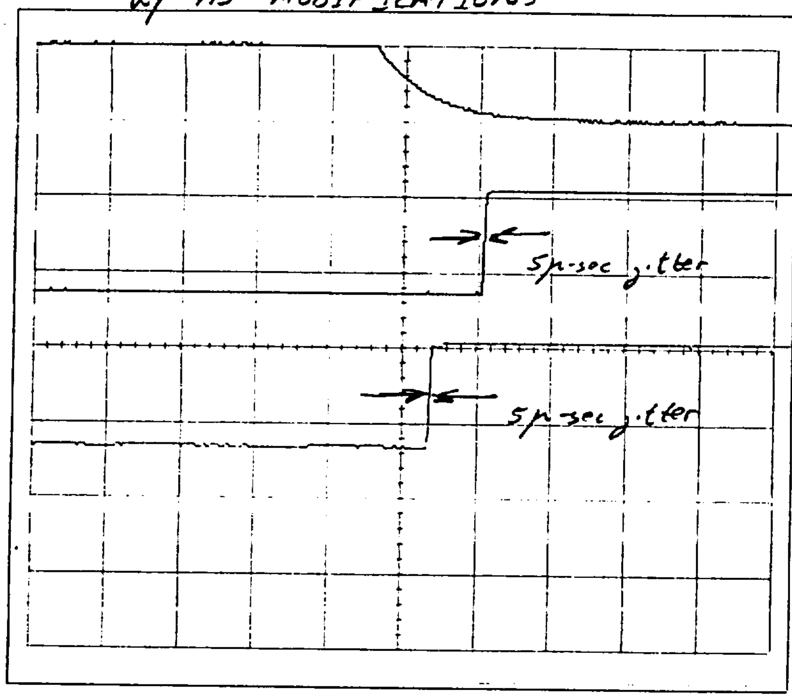
FIGURE 4

- Eliminated the jitter @ start & end of frame by synchronization of the A5 - U12 CNTR w/ the FRAME START signal, which eliminated end of frame jitter. Eliminated start of frame jitter by clocking the frame start flip flop (A5-U7) from 198 KHZ

START & END OF FRAME JITTER

TRMM DESIGN

START OF FRAME CH I + CH II
w/ AS MODIFICATIONS

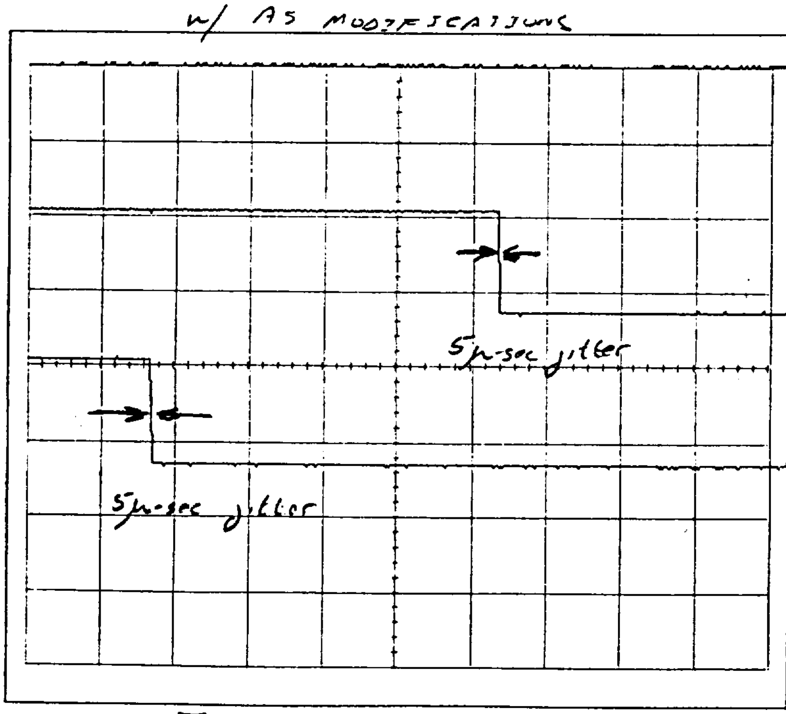


DATE:Apr 29/93
TIME:09:48:54

CH1: 1.00V :5us
LINE SYNC INPUT TO AS
CH2: 1.00V :5us
FRAME START CH I
CH3: 1.00V :5us
FRAME START CH II

FIGURE 5A

END OF FRAME CH I & CH II
w/ AS MODIFICATIONS



DATE:Apr 29/93
TIME:09:52:53

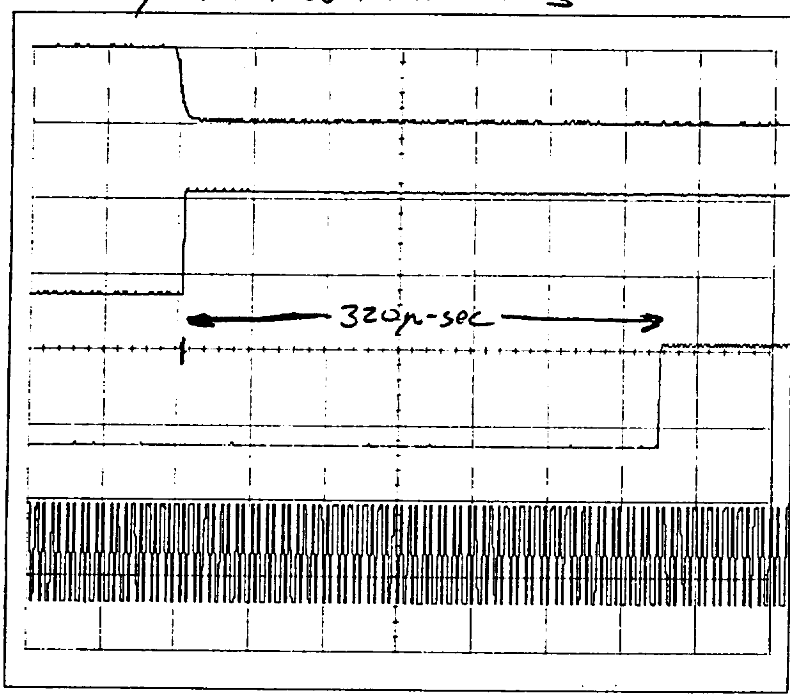
CH1: 1.00V :50us
LINE SYNC INPUT TO AS
CH2: 1.00V :50us
FRAME START CH I
CH3: 1.00V :50us
FRAME START CH II

NOTE: THE TWO L/C OSCILLATORS ARE OFF IN FREQUENCY SO THE END OF FRAME OCCURS AT DIFFERENT PTS. The real design will incorporate a xtal osc.

FIGURE 5B

TRMM DESIGN

SYNCRONAZATION OF AS-U12-CNTR
w/ AS MODIFICATIONS



DATE:Apr 29/93
TIME:10:04:58

CH1: 1.00V :50us
LINE SYNC INPUT TO AS

CH2: 1.00V :50us
FRAME START CH I

CH3: 1.00V :50us
1.55KHZ CH I

CH4: 1.00V :50us
198KHZ CH I

NOTE: $\frac{1}{2}\left(\frac{1}{1.55KHZ}\right) = 320\mu\text{-sec}$

FIGURE 6

TRMM DESIGN

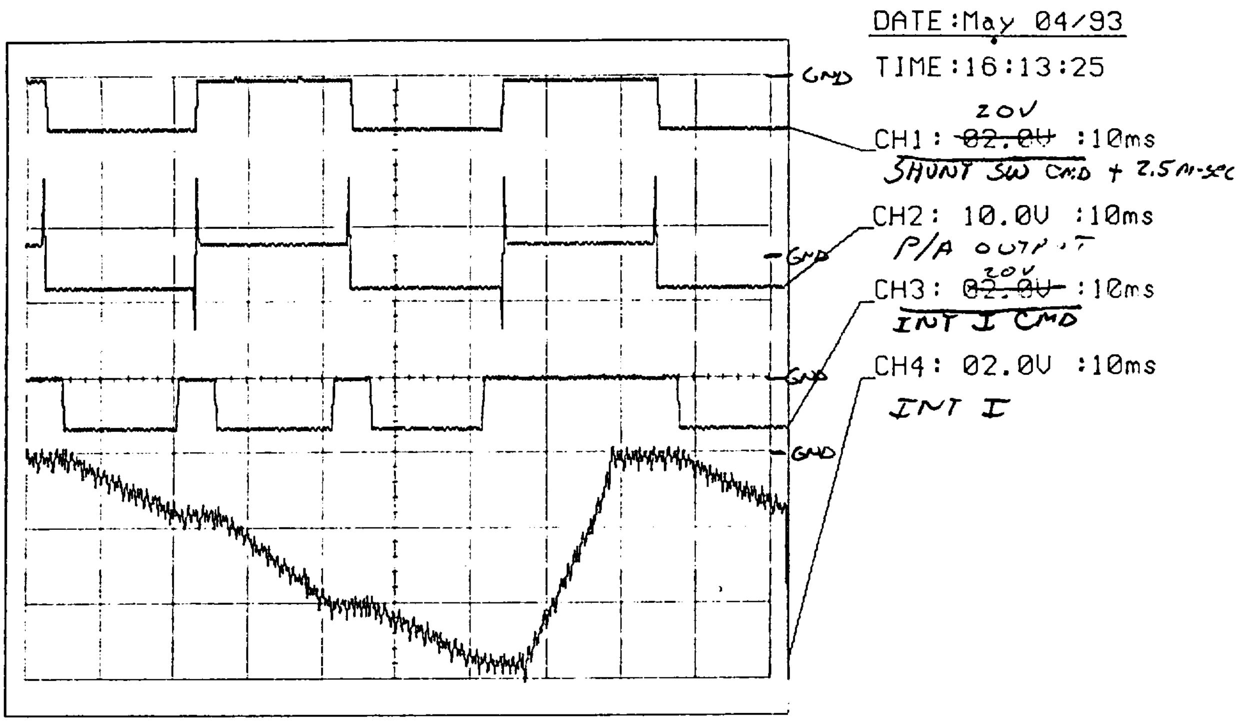


FIGURE 7A

'EXPANDED'

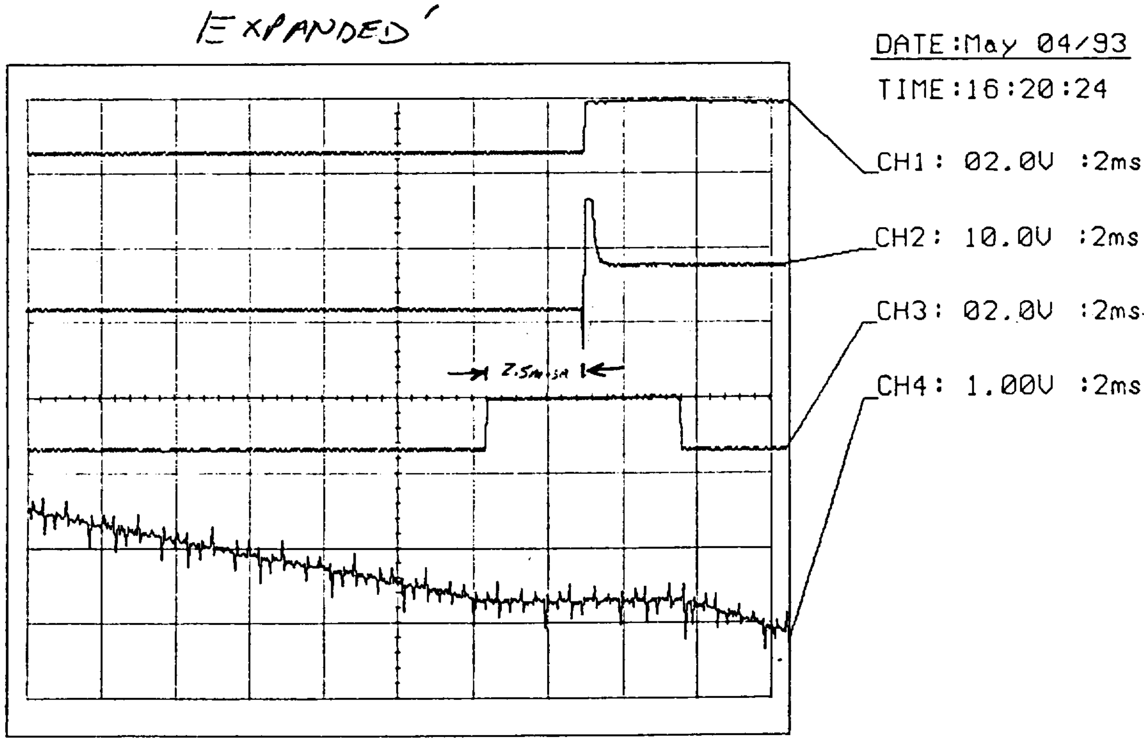


FIGURE 7B

TRMM DESIGN

END OF FRAME CH I + II

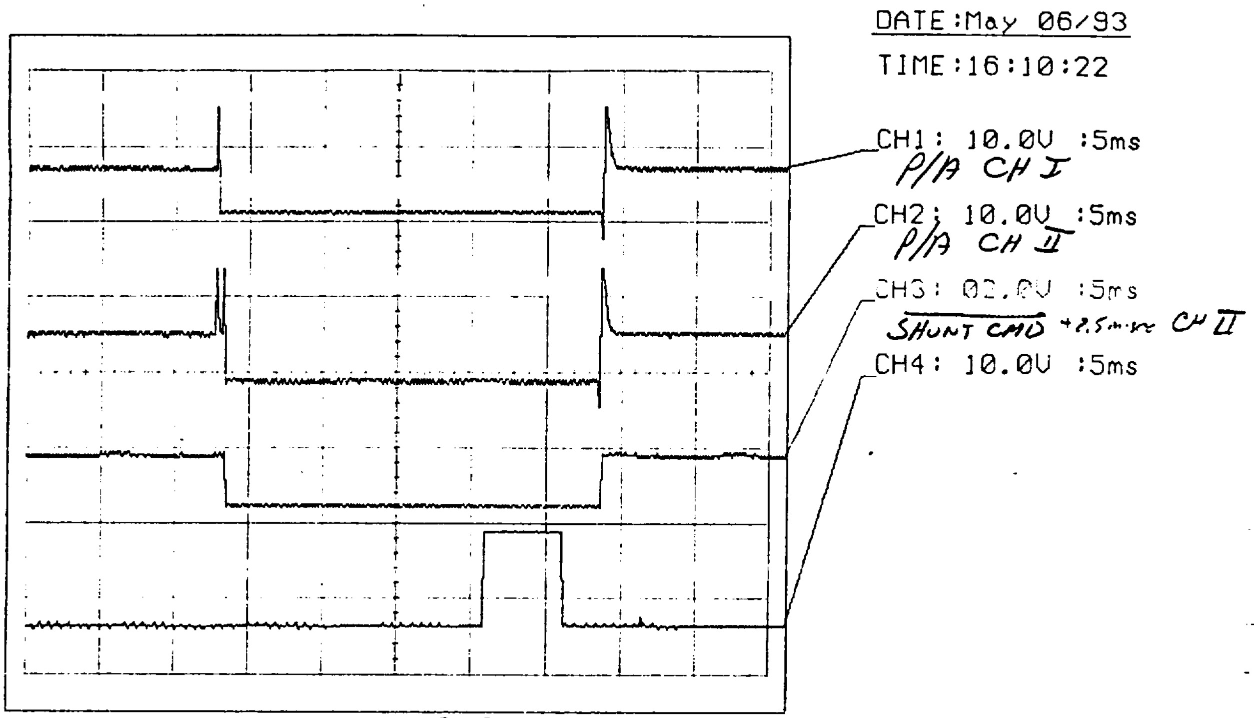


FIGURE 8A

'EXPANDED'

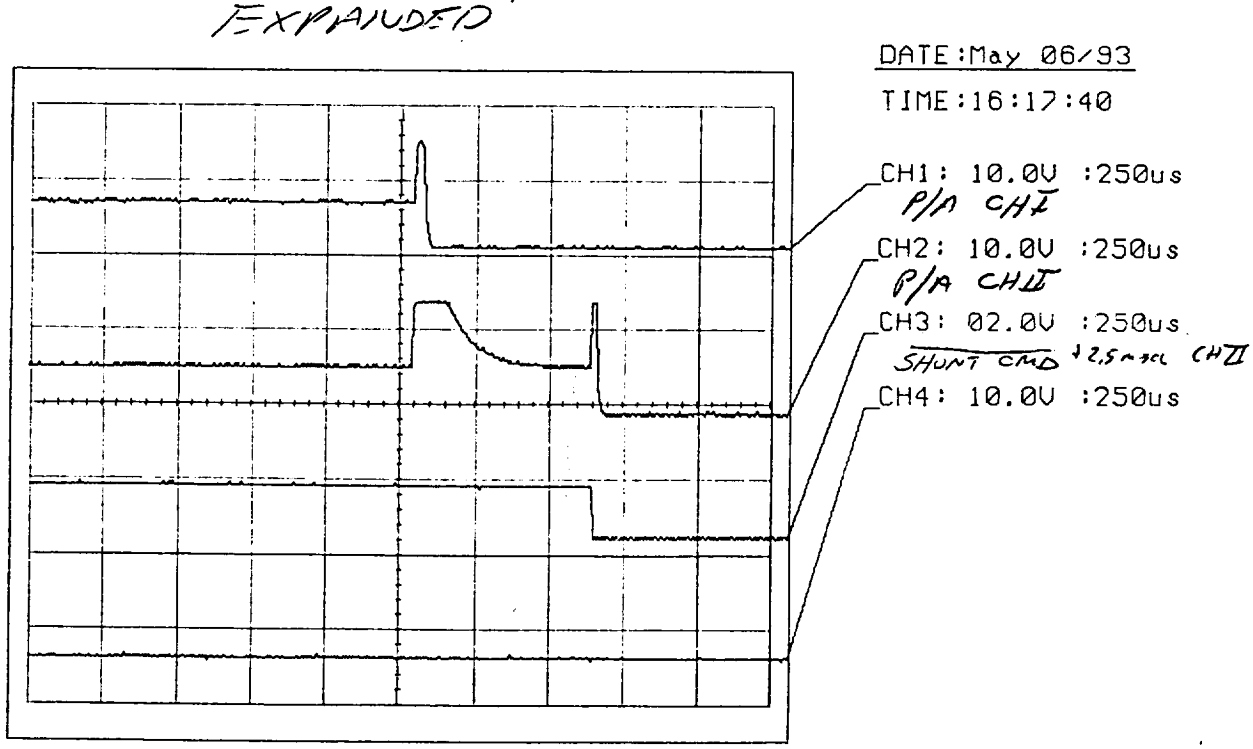


FIGURE 8B

END OF FRAME CH II

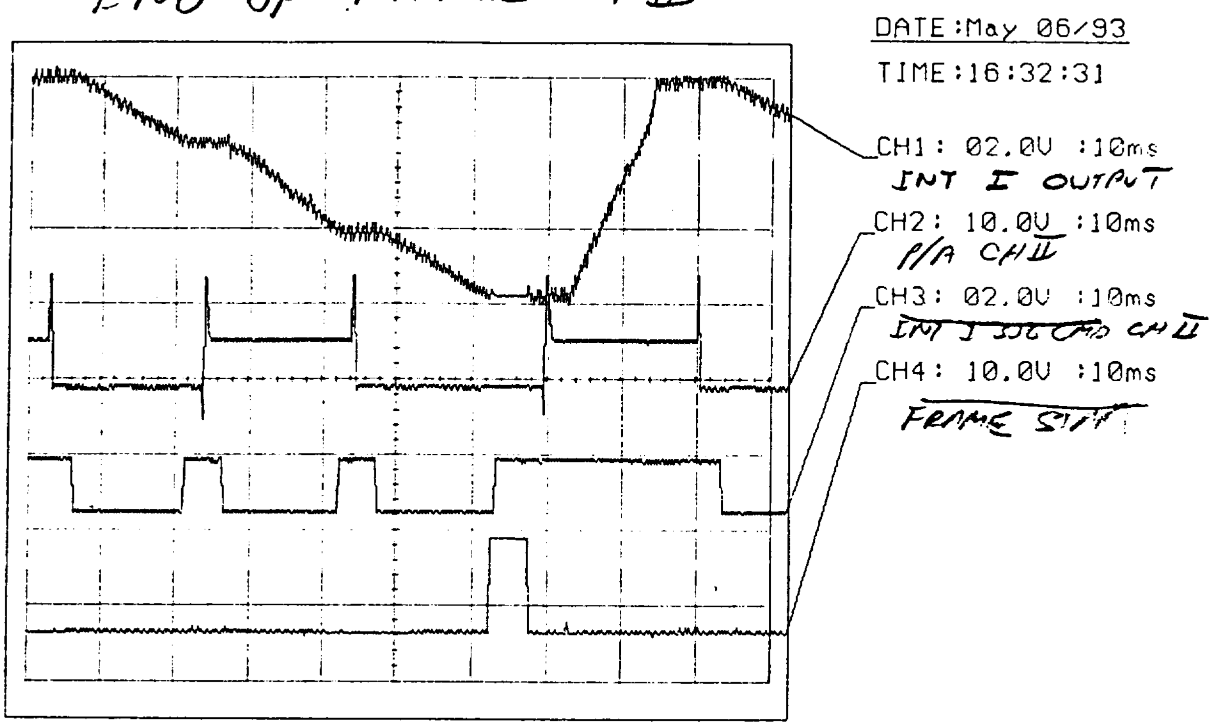


FIGURE 9

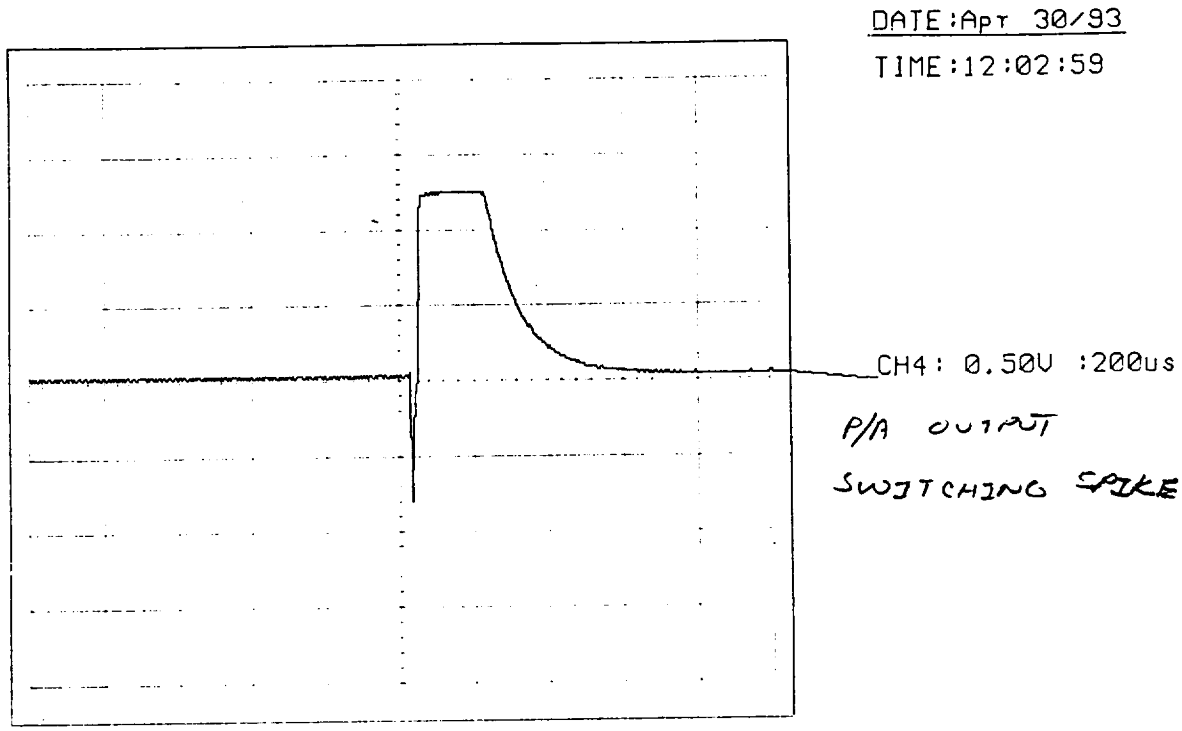
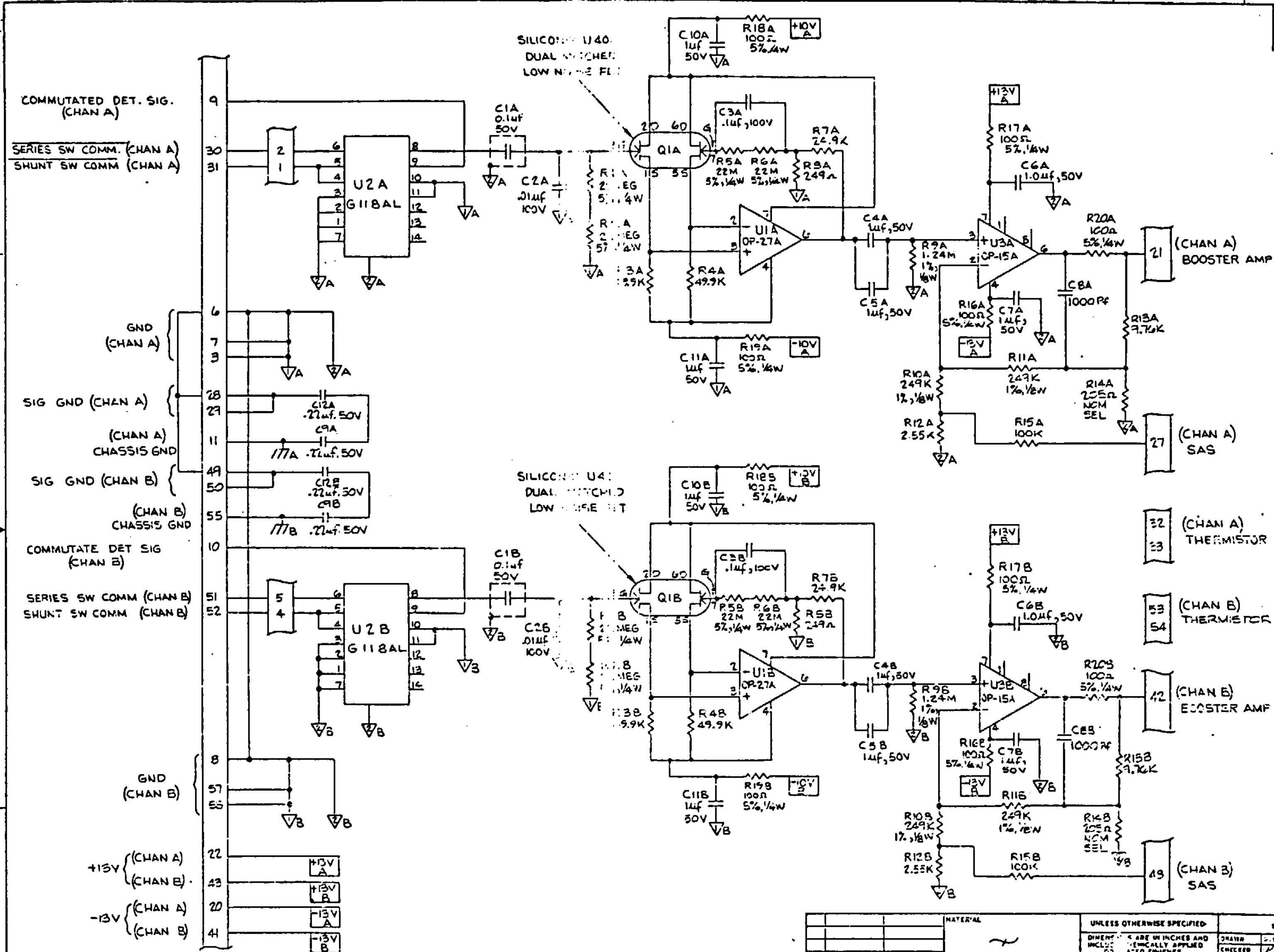


FIGURE 10

SINGLE CHANNEL COMMUTATION SPIKE
AT P/A OUTPUT

$T_{spike} \approx 1m\text{-}sec$

APPENDIX A



ZONE	LTR	DESCRIPTION	DATE	APPROVED
	R1	ENGINEERING RELEASE		

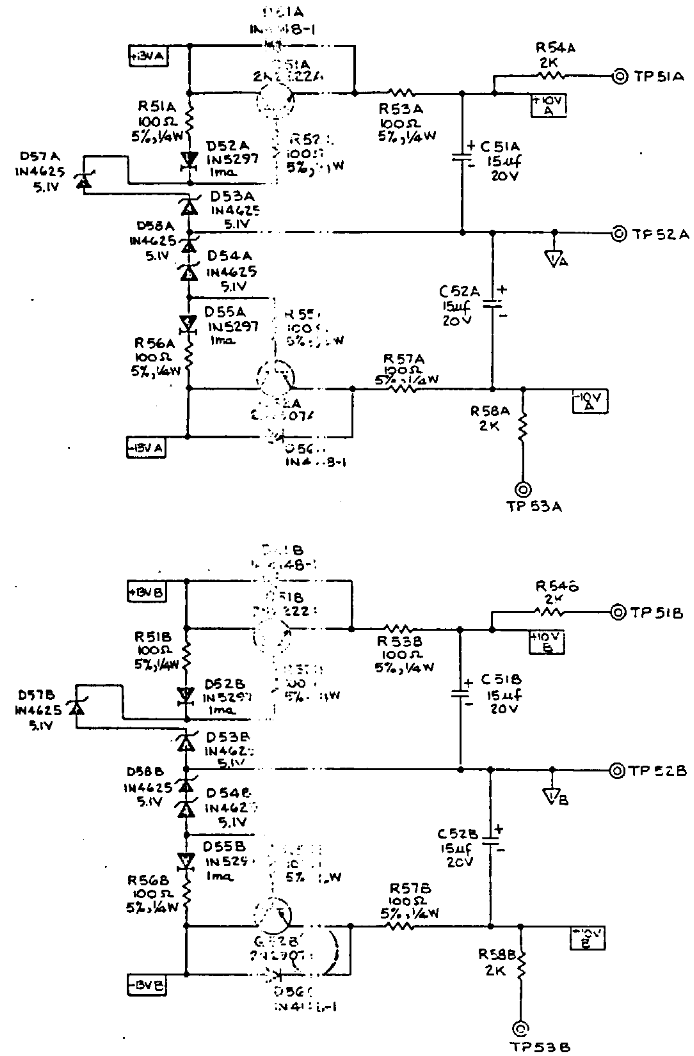
NOTES

1. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-D-1000 LEVEL 3.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTOR ARE 1%, 1/10W
   ALL CAPACITORS ARE ±10%, 200V
4. REF. DESIG. RESERVED FOR THIS SHT. ARE 1-50.

SCHEMATIC, ELECTRICAL
PRE-AMP (A1)

D 00430 257302-3004-7

SHEET 1 OF 2



• REF. DESIG. RESERVED FOR THIS SHT. ARE 51- SUBSEQUENT.

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	R1	SEE SHEET 1		

EDO BARNES ENGINEERING DIVISION

SCHEMATIC, ELECTRICAL
PRE-AMP (A1)

SIZE	CODE IDENT NO.	DWG NO.
D	00430	257302-300

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

MATERIAL ~

FINISH ~

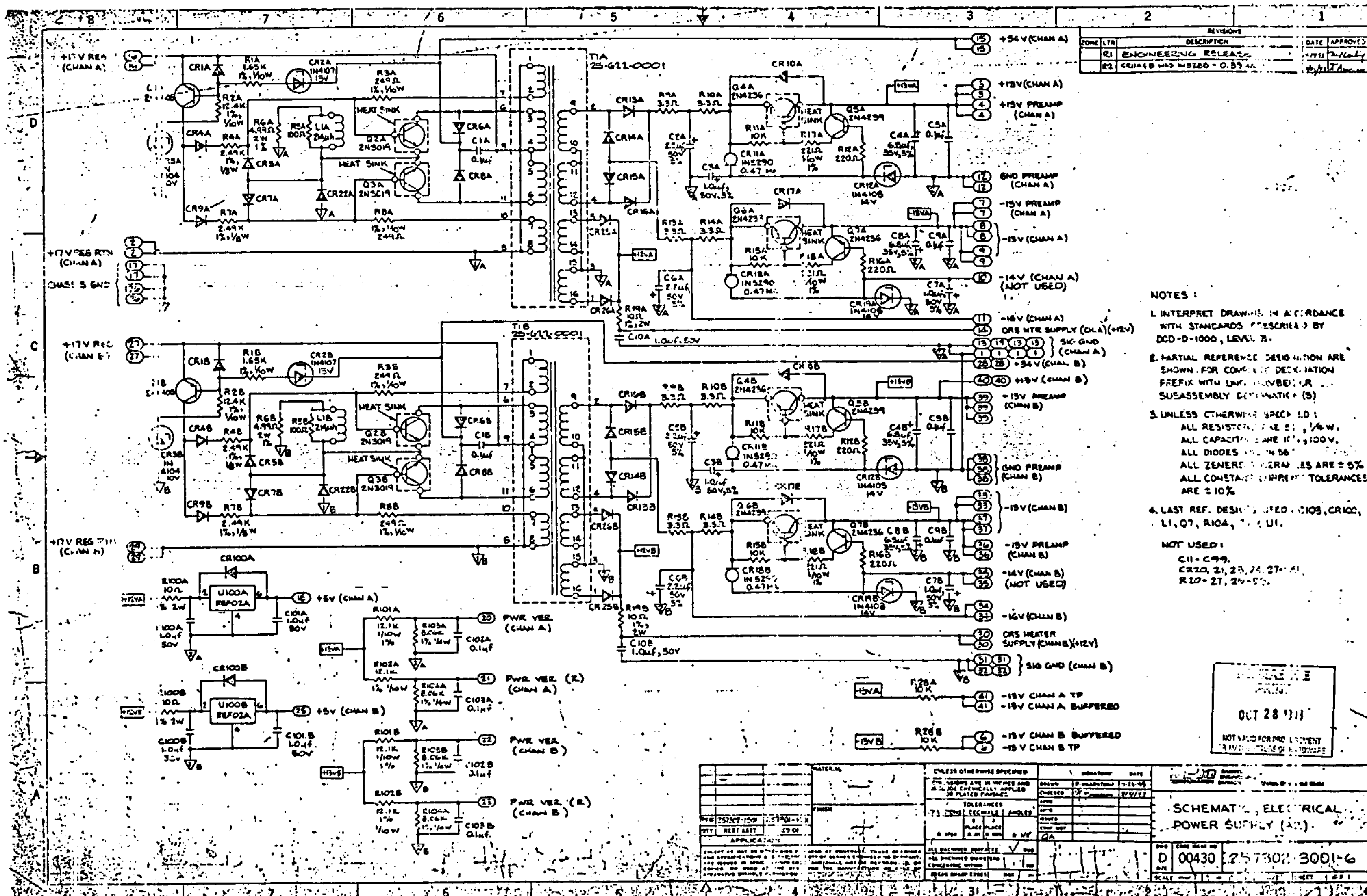
QTY | NEXT ASSY | USED ON

APPLICATION

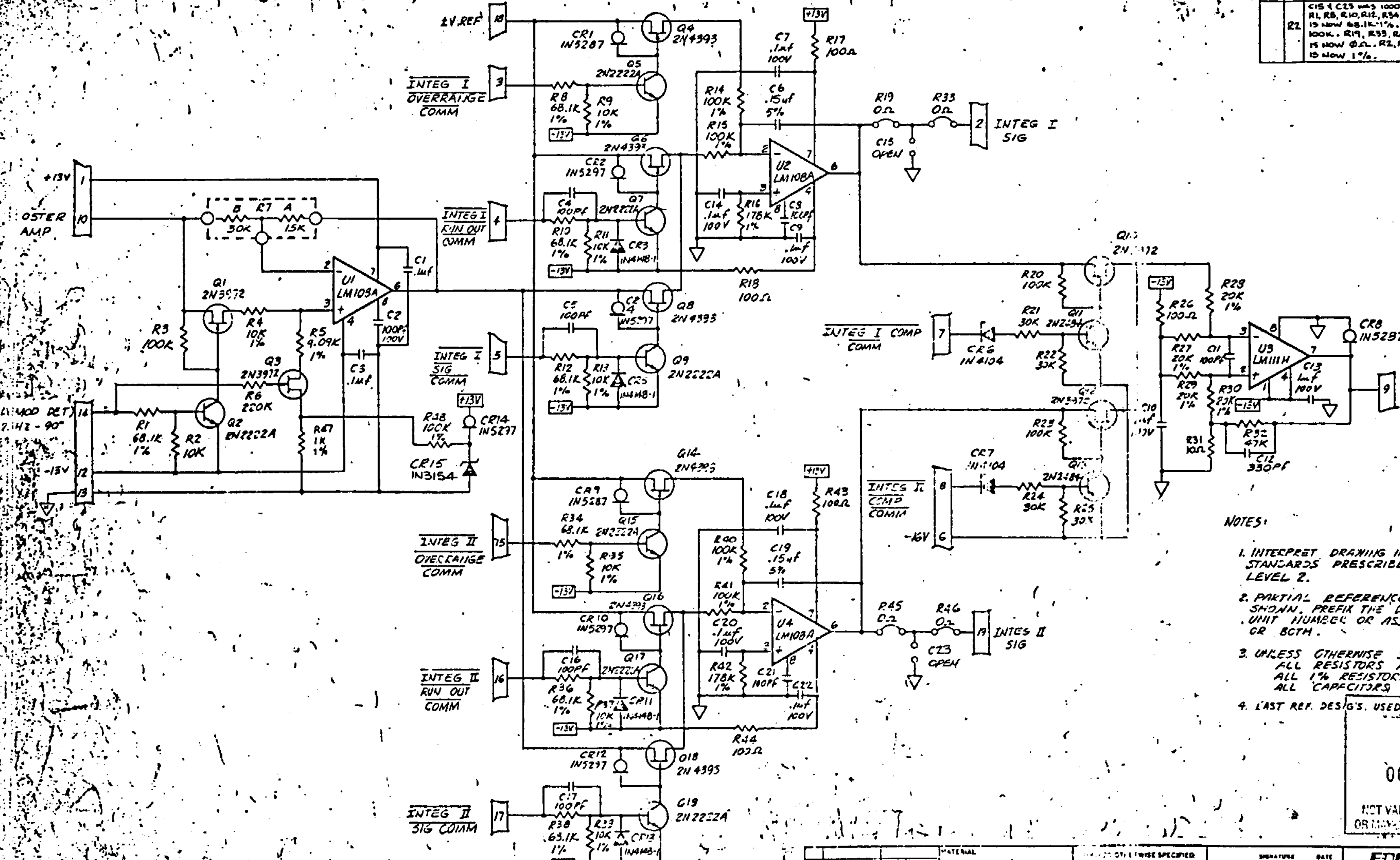
SCALE ~

SHEET

58


NOTES:
1. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-D-1000, LEVEL 3.
2. PARTIAL REFERENCE DESIGNATION ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
3. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 W.
ALL CAPACITORS ARE 100V.
ALL DIODES ARE IN 56
ALL ZENER TOLERANCES ARE ± 5%
ALL CONSTANT CURRENT TOLERANCES ARE ± 10%
4. LAST REF. DESIG. USED: C108, CR100, L1, Q7, R104, U1.
NOT USED:
C11-C99,
CR20, 21, 23, 24, 27-61,
R20-27, 29-
REVISIONS
R1 ENGINEERING RELEASE
R2 CR14A,B WAS IN5285 - 0.33 MA
+17V REG (CHAN A)
+17V REG RTN (CHAN A)
CHASSIS GND
+17V REG (CHAN B)
+17V REG RTN (CHAN B)
T1A 25-622-0001
T1B 25-622-0001
+34V (CHAN A)
+15V (CHAN A)
+15V PREAMP (CHAN A)
GND PREAMP (CHAN A)
-15V PREAMP (CHAN A)
-15V (CHAN A)
-14V (CHAN A) (NOT USED)
-16V (CHAN A)
CRS HTR SUPPLY (CH A) (+12V)
SIG GND (CHAN A)
+34V (CHAN B)
+15V (CHAN B)
-15V PREAMP (CHAN B)
GND PREAMP (CHAN B)
-15V (CHAN B)
-15V PREAMP (CHAN B)
-14V (CHAN B) (NOT USED)
-16V (CHAN B)
CRS HEATER SUPPLY (CHAN B) (+12V)
SIG GND (CHAN B)
-15V CHAN A TP
-15V CHAN A BUFFERED
-15V CHAN B BUFFERED
-15V CHAN B TP
+5V (CHAN A)
+5V (CHAN B)
PWR VER (CHAN A)
PWR VER (R) (CHAN A)
PWR VER (CHAN B)
PWR VER (R) (CHAN B)
OCT 28 1977
SCHEMATIC, ELECTRICAL POWER SUPPLY
D 00430 257302-3001-6

59



REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	R1	ENGINEERING RELEASE	10/14	
	R2	C15 & C23 WAS 1000PF; IS NOW OPEN. R1, R8, R10, R12, R34, R36 & R38 WAS 68K; IS NOW 68.1K-1%. R3 WAS 220K; IS NOW 100K. R19, R33, R45, & R46 WAS 10K; IS NOW 0Ω. R2, R9, R11, R13, R35, R37 & R39 IS NOW 1%.		

NOTES:

1. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-D-1000, LEVEL 2.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.
3. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE ±5%, 1/4W. ALL 1% RESISTORS ARE 1/10W. ALL CAPACITORS ARE ±10%, 200V.
4. LAST REF. DES'G'S. USED: C23, CR15, Q19, R48, U4

OCT 19 1993

NOT VALID FOR PROCUREMENT OR MANUFACTURE OF HARDWARE

EDO BARNES ENGINEERING DIVISION

SCHEMATIC, ELECTRICAL A/D & DEMOD CIRCUITS (ESA A3)

D 00430 257302-3002-4

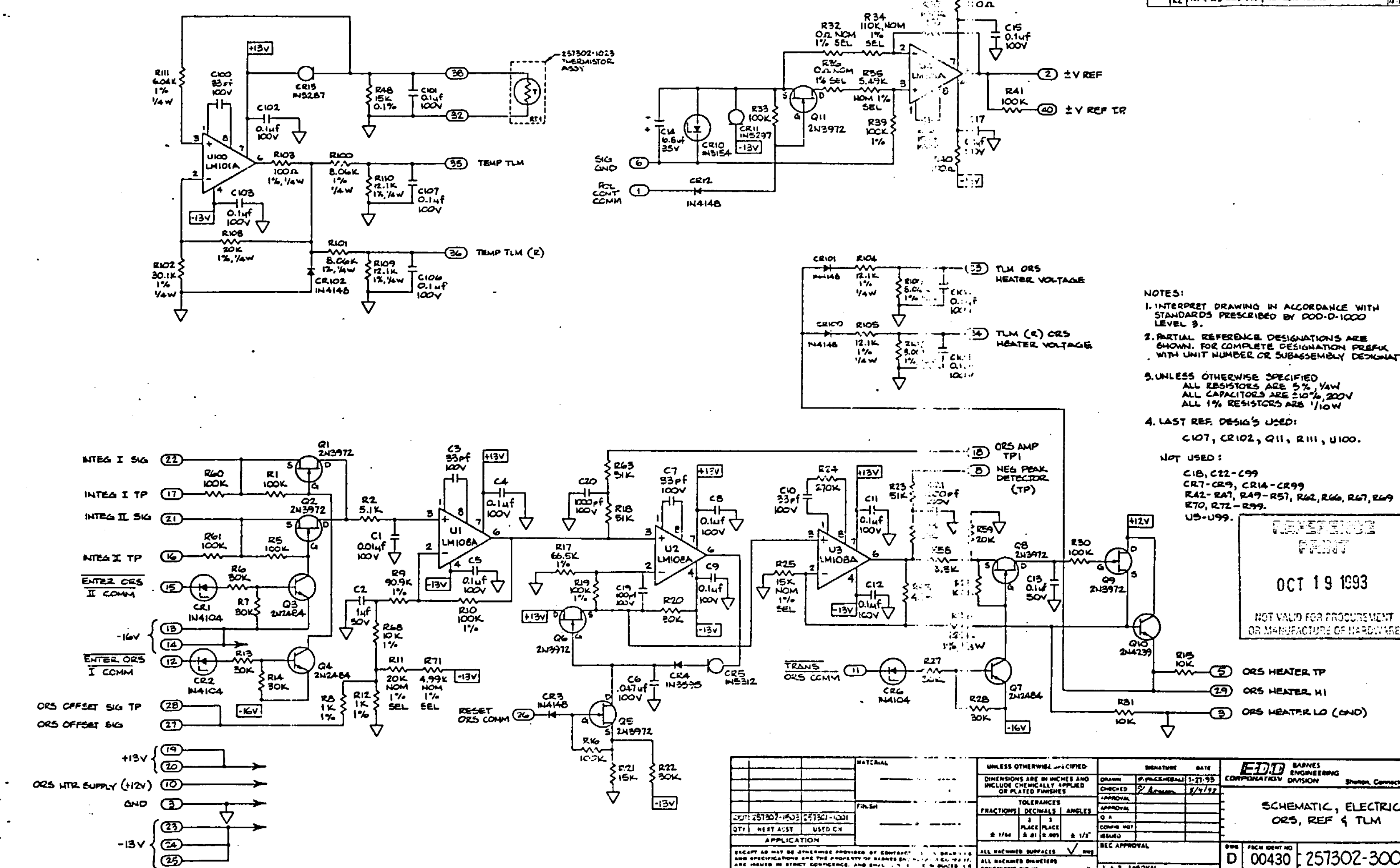
SHEET 1 OF 1

NEXT ASSY	USED ON
257302-1502	257301-1001

APPLICATION

60

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	R1	ENGINEERING RELEASE		
	R2	R1 & R5 WAS 1M, IS NOW 100K		



NOTES:

1. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-D-1000 LEVEL 3.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
3. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS ARE 5%, 1/4W
   ALL CAPACITORS ARE ±10%, 200V
   ALL 1% RESISTORS ARE 1/10W
4. LAST REF. DESIG'S USED:
   C107, CR102, Q11, R111, U100.

NOT USED:
C18, C22-C99
CR7-CR9, CR14-CR99
R42-R47, R49-R57, R62, R66, R67, R69
R70, R72-R99.
U5-U99.

REFERENCE PRINT

OCT 19 1993

NOT VALID FOR PROCUREMENT OR MANUFACTURE OF HARDWARE

257302-1503	257301-1001	
QTY	NEXT ASSY	USED ON
APPLICATION		

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

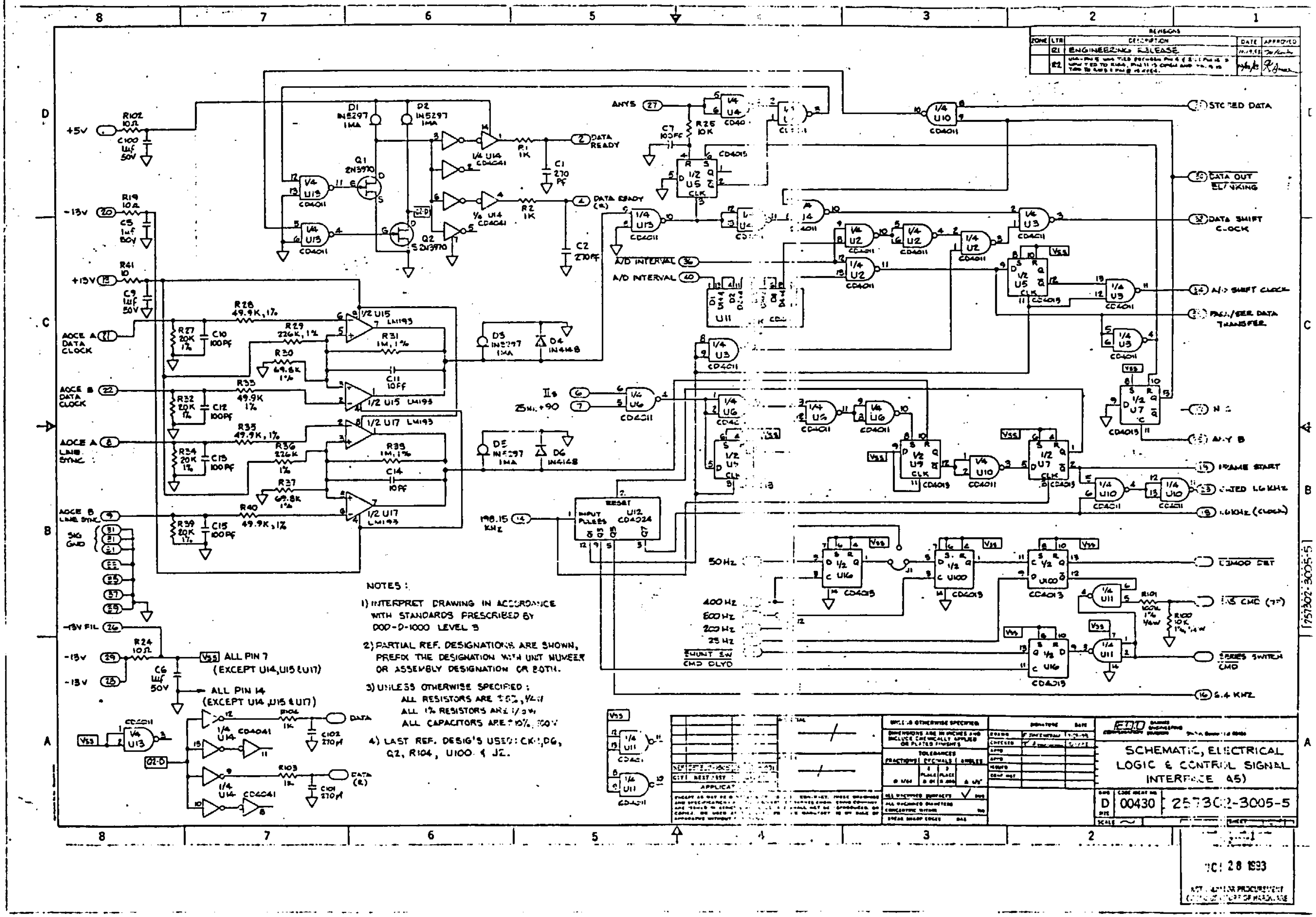
EDO CORPORATION BARNES ENGINEERING DIVISION Shelton, Connecticut

SCHEMATIC, ELECTRICAL ORS, REF & TLM (A4)

SIZE D | FSCM IDENT NO 00430 | 257302-3003-4

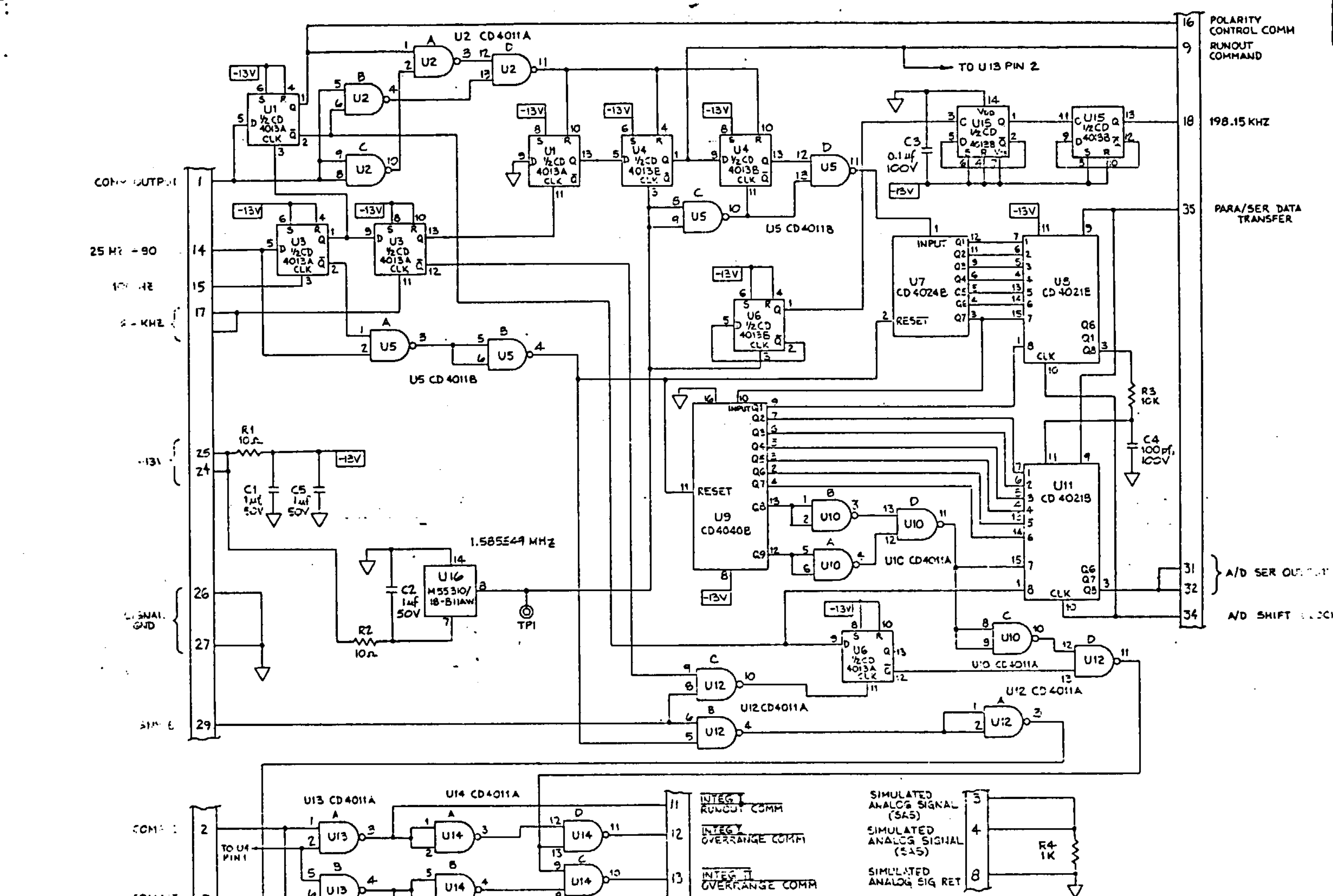
SHEET 1 OF 1

61


NOTES:
1) INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-D-1000 LEVEL 3
2) PARTIAL REF. DESIGNATIONS ARE SHOWN, PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.
3) UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS ARE ±10%, 100V
4) LAST REF. DESIG'S USED: CK, DG, Q2, R104, U100 & J2.
SCHEMATIC, ELECTRICAL LOGIC & CONTROL SIGNAL INTERFACE 45)
D 00430
3005-5
STORED DATA
DATA OUT BLANKING
DATA SHIFT CLOCK
A/D SHIFT CLOCK
FRAME START
50 Hz
400 Hz
800 Hz
200 Hz
25 Hz
SHUNT SW CMD OLYD
SERIES SWITCH CMD
A/D INTERVAL
DATA READY
ADCE A DATA CLOCK
ADCE B DATA CLOCK
ADCE A LINE SYNC
ADCE B LINE SYNC
SIG GND
+5V
-15V
+15V
-15V FIL
ENGINEERING RELEASE

62

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	4	CONTROLLED RELEASE. SEE ECN 2573-E-274		
	3	SEE ECN 2573-E-293		



NOTES:

1. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-D-1000 LEVEL 3.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
3. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS ARE 5%, 1/4W.
   ALL CAPACITORS ARE 10%, 200V.
4. LAST REF. DESIG'S. USED : C4, R4, U16.

REF DES	DEVICE TYPE	-13V	GND
J1, U3, U4, U6, U15	CD4013B	7	14
U2, U5, U10, U12, U13, U14	CD4011B	7	14
U7	CD4024B	7	14
U8, U11	CD4021B	8	16
U9	CD4040B	8	16

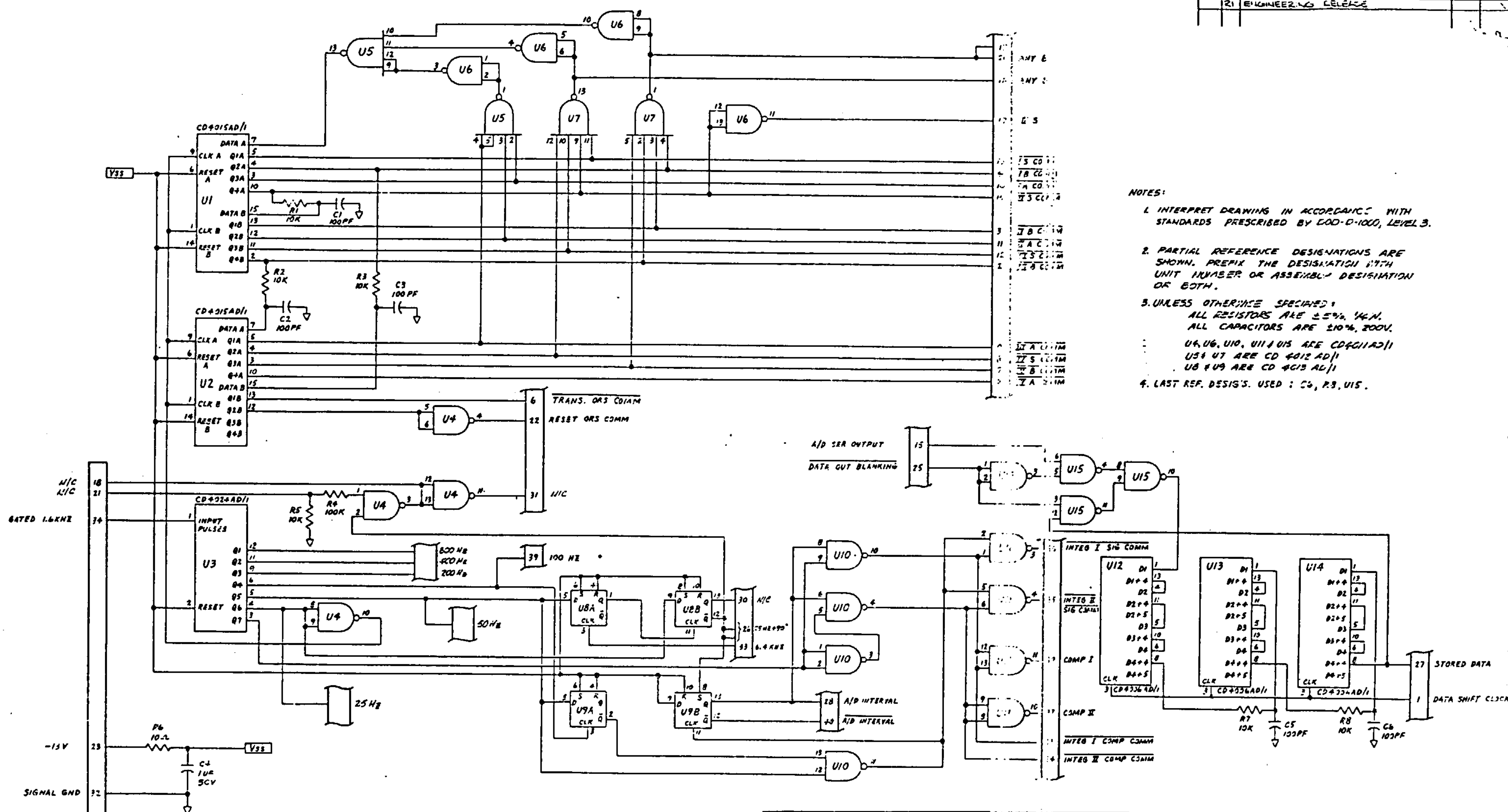
BARNES ENGINEERING COMPANY
STAMFORD, CONNECTICUT

SCHEMATIC, ELECTRICAL LOGIC & SYSTEM CLOCK (A6) (1.535 MHz)

D 00430 257302-3006-4

SHEET 1 OF 1

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	R1	ENGINEERING RELEASE		



NOTES:

1. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-D-1000, LEVEL 3.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE ±5%, 1/4W.
   ALL CAPACITORS ARE ±10%, 200V.
   U4, U6, U10, U11 & U15 ARE CD4011AD/1
   U5 & U7 ARE CD 4012 AD/1
   U8 & U9 ARE CD 4013 AD/1
4. LAST REF. DESIG'S. USED: C6, R8, U15.

257302-1507	257301-1064
NEXT ASSY	USED ON
APPLICATION	

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MATERIAL

FINISH

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND APPLY AFTER CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCES: FRACTIONS | DECIMALS 2 PLACE ±.01, 3 PLACE ±.005 | ANGLES ± 1/2°

DRAWN / CHECKED / APPD / APPD / ISSUED — SIGNATURE — DATE

BEC APPROVAL

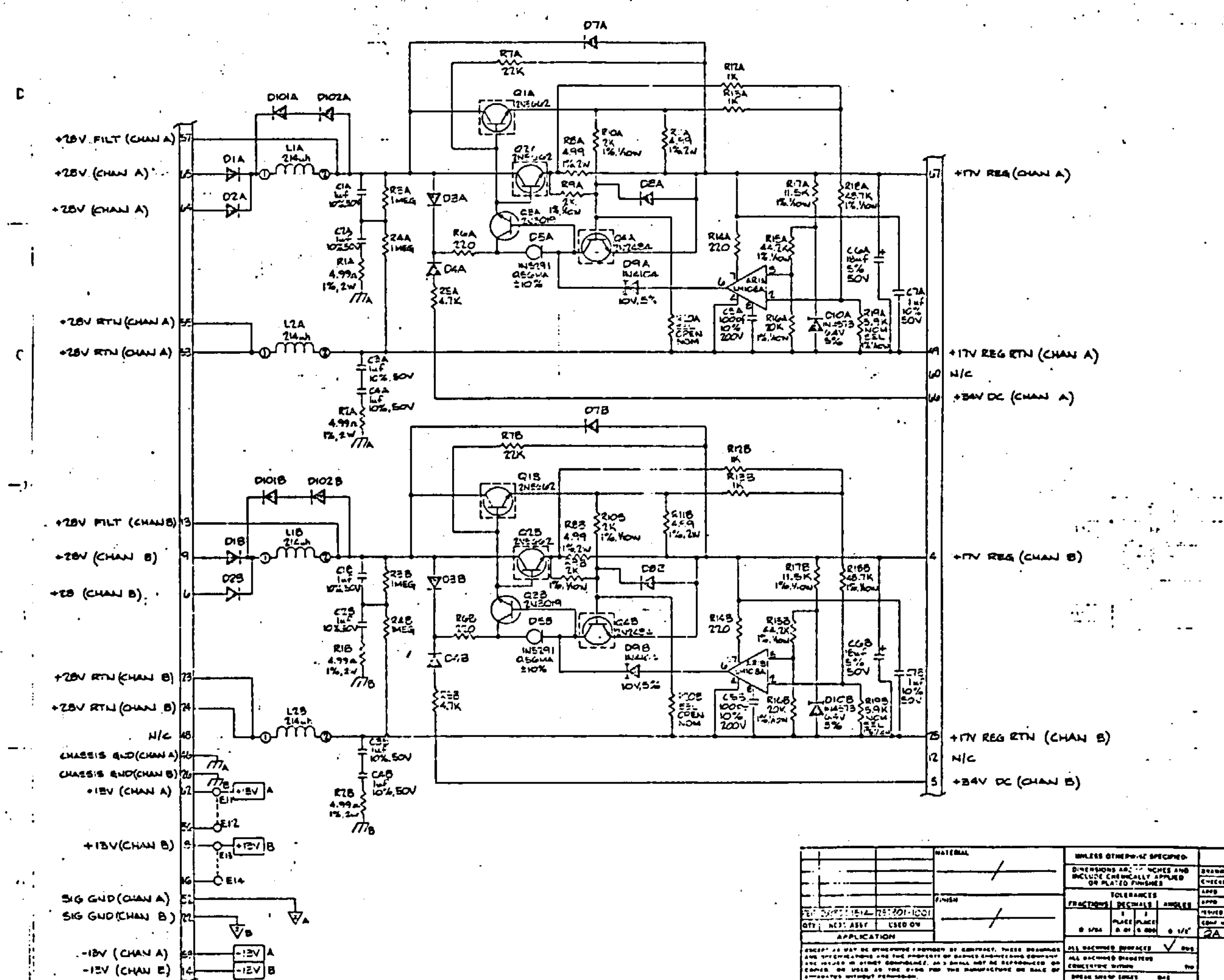
OTHER APPROVAL

BARNES ENGINEERING CORPORATION DIVISION

ELECTRICAL SCHEMATIC
LOGIC
(A7)

SIZE D — CODE IDENT NO. 00430 — DWG 257302-3007-3

SCALE — SHEET 1 OF 1



NOTES:

1) INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-[illegible], LEVEL 3.

2) PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.

3) UNLESS OTHERWISE SPECIFIED:

3.1) ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

3.2) ALL CAPACITOR VALUES ARE IN MICRO[illegible] [illegible], 100V.

3.3) ALL DIODES ARE 1N5617.

4) LAST DESIGNATIONS USED ARE: D102, [illegible], R111 & U100.

NOT USED: C1-C99, D11-D99, R1-R55, R64-R99, U1-U50, U52-U99

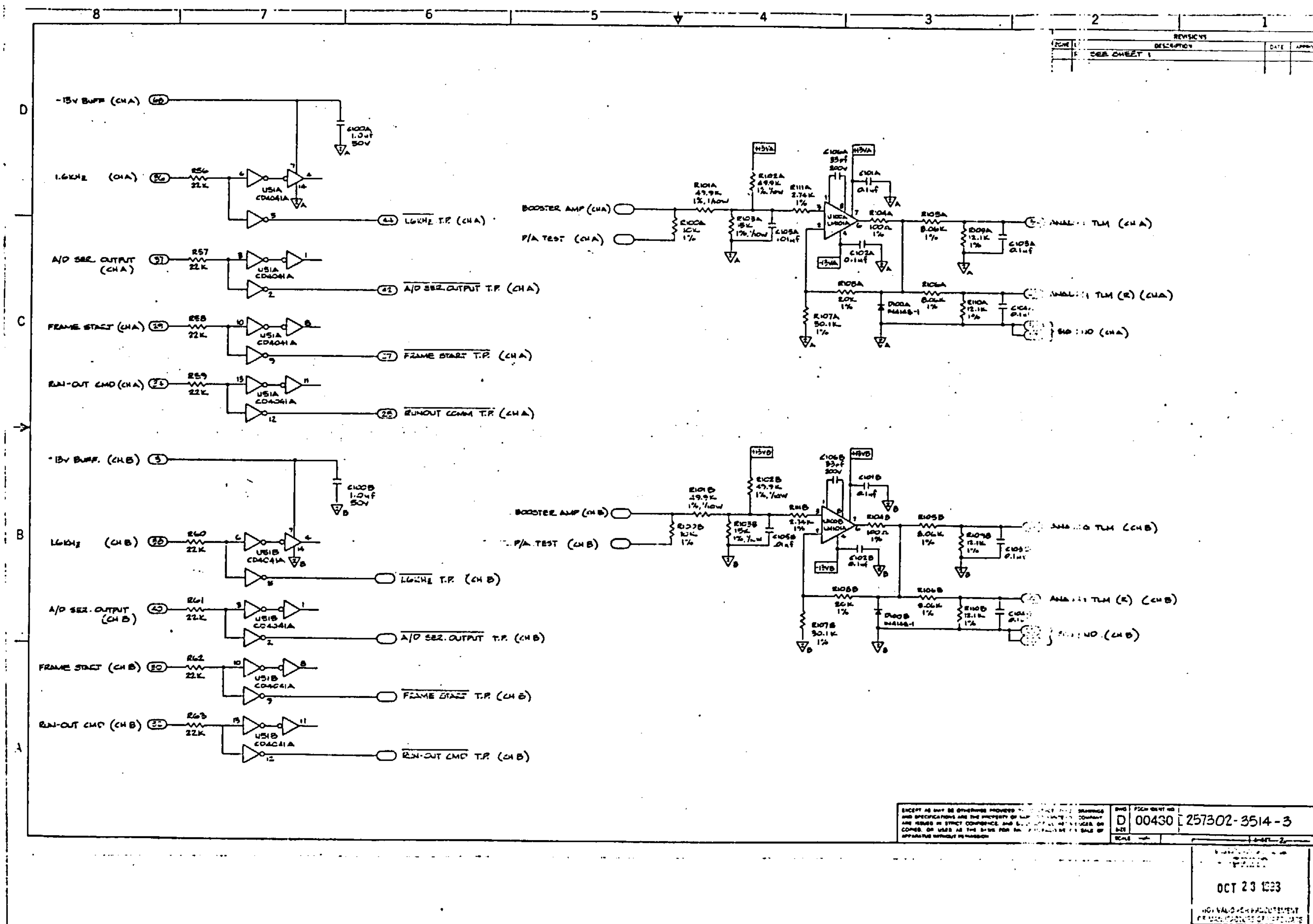
SCHEMATIC, ELECTRICAL, [illegible] REG/F/A TLM/CONSOLE [illegible] (A14)

00430 257302-3514-3

OCT 2[illegible] 1983

ORIGINAL PAGE IS OF POOR QUALITY

65



-15V BUFF (CH A)
1.6KHz (CH A)
A/D SER. OUTPUT (CH A)
FRAME START (CH A)
RUN-OUT CMD (CH A)
-15V BUFF. (CH B)
1.6KHz (CH B)
A/D SER. OUTPUT (CH B)
FRAME START (CH B)
RUN-OUT CMD (CH B)
1.6KHz T.P. (CH A)
A/D SER. OUTPUT T.P. (CH A)
FRAME START T.P. (CH A)
RUNOUT COMM T.P. (CH A)
1.6KHz T.P. (CH B)
A/D SER. OUTPUT T.P. (CH B)
FRAME START T.P. (CH B)
RUN-OUT CMD T.P. (CH B)
BOOSTER AMP (CH A)
P/A TEST (CH A)
BOOSTER AMP (CH B)
P/A TEST (CH B)
ANALOG TLM (CH A)
ANALOG TLM (R) (CH A)
ANALOG TLM (CH B)
ANALOG TLM (R) (CH B)
REVISIONS
SEE SHEET 1
D 00430 257302-3514-3
OCT 23 1983

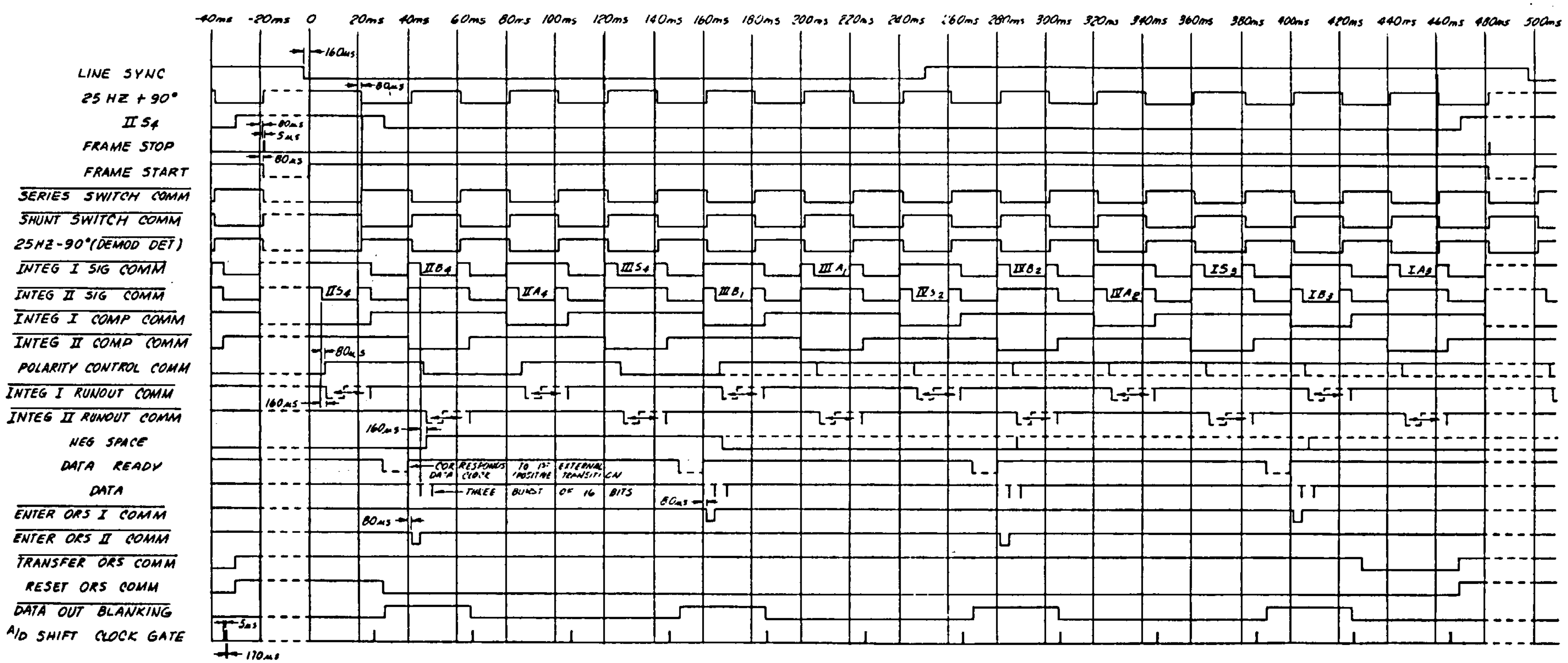


FIGURE 4.6-5 TIMING DIAGRAM

APPENDIX C

COMBINING VARIABLE PARAMETERS

RESISTORS

EOL % Tolerance = $[(\Delta R\ \text{INIT})^2 + (\Delta R\ \text{TEMP})^2 + (\Delta R\ \text{LIFE})^2]^{\frac{1}{2}}$

No measurable radiation effects on resistors

BOL % tolerance = ΔR INIT + ΔR TEMP

Examples:

TYPE	ΔR TOL INITIAL %	ΔR TEMP -34% + 100°C	ΔR LIFE %	ΔR RSS %
Carbon Composition RCR	±5.	±8	±15	±17.7
Film, RLR	±1.0	±0.375	±2	± 2.3
Film, RNC	±1.0	±0.375	±1	±1.5
Film,* RNC90Y (Vishay)	±0.1	±0.04	±0.1	±0.15
Variable, RJR (Non-Wire Wound)*	±5.0	±0.4	±10	±11.2
Variable, RTR (Wire Wound)*	±5.0	±0.4	±10	±11.2
Wire Wound, RBR (Accurate)	±1.0	±0.4	±0.5	±1.2
Wire Wound, RWR (Power)	±1.0	±0.4	±1	±1.5
Wire Wound, RER (Chassis Mount)	±1.0	±0.4	±1	±1.5
Network, RZO	±1.0	±0.4	±1	±1.5
Thermistors, Glass Bead, Neg TC	±5.0	NA	±1.3	±5.2
Bead Encapsulated, Pos TC	±5.0	NA	±1.8	±5.3
Disc, Pos or Neg TC	±5.0	NA	±5	±7.1

Adjustments can be made for different initial tolerances & temps. (50ppm/°C Temp coefficient assumed for most above).

[redacted]

APPENDIX C

COMBINING VARIABLE PARAMETERS

CAPACITORS

EOL % Tolerance = $[(\Delta C_{INIT})^2 + (\Delta C_{TEMP})^2 + (\Delta C_{LIFE})^2]^{1/2}$

No measurable radiation effects on capacitors.

BOL % Tolerance = $\Delta C_{INIT} + \Delta C_{TEMP}$

Examples:

TYPE	ΔC TOL INITIAL %	ΔC TEMP -34% + 100°C	ΔC LIFE %	ΔC RSS %
Ceramic, CKR (General Purpose BX)	±10.0	+12/-7	±30.	+33.8/-32.4
Ceramic, CCR Temperature Compensated BP)	±1.0	+0.025/-0.1777	±0.5(1)	±1.2
Metallized Film, CRH	±1.0	±0.5	±2.0	±2.3
Plastic Film, CQR (Metallized/Non metalized)	±5.0	±0.5(3)	±2.0	±5.4
Glass, CYR	±5.0	±5(3)	±0.5(2)	±7.1
Mica, CMR	±5.0	±5(3)	±0.5	±7.1
Tantalum, Foil CLR	±10	±10(3)	±15.	±20.6
Tantalum, Slug CLR	±10	±20/-25	±10	±24.5/-28.7
Tantalum, Solid, CSR	±10.	±10.	±10	±17.3
Variable Piston, PC	±10	±10(3)	±5	±15.0

Notes (1) OR ±0.75 pf whichever is greater.
(2) OR ±0.5pf " "
(3) Assumed

[redacted]

TABLE 2. EOL DESIGN LIMITS (Continued)

Part Type	Applicable MIL-Spec	Parameter	End-of Life Design Limits
Resistors (Continued)			
Film,* RNC90Y (Vishay)	MIL-R-55182	R	±0.1%
Variable, RJR (Non-Wire Wound)*	MIL-R-39035	R	±10%
Variable, RTR (Wire Wound)*	MIL-R-39015	R	±10%
Wire Wound, RBR (Accurate)	MIL-R-39005	R	±0.5%
Wire Wound, RWR (Power)	MIL-R-39007	R	±1%
Wire Wound, RER (Chassis Mount)	MIL-R-39009	R	±1%
Network, RZO	MIL-R-83401	R	±1%
Thermistors, Glass Bead, Neg TC	MIL-T-23648	R	±1.3%
Bead Encapsulated, Pos TC			±1.8%
Disc, Pos or Neg TC			±5%
EMI Filters	MIL-F-15733 MIL-F-28861	C IR	±20% -30%
Coils, RF Molded*	MIL-C-15305	L Q	±3% ±6%
Transistors	MIL-S-19500	h_{FE}	85%
		I_{CBO}	300%
		I_{CES}	300%
		I_{CEX}	300%
		V_{BE}	±0.01V
		$V_{CE(sat)}$	±15%
		V_t (MOSFETs)*	+0.1V, -0.0V
		t_d, t_f t_r, t_s	120%

*EOL Design Limits were derived from MIL-STD-1547, except those annotated by an asterisk, which were GE derived.

[redacted]

TABLE 2. EOL DESIGN LIMITS (Continued)

Part Type	Applicable MIL-Spec	Parameter	End-of Life Design Limits
Diodes	MIL-S-19500	V_F	±1%
		I_R	+100%
		V_Z	±2%
Reference Diodes	MIL-S-19500	V_Z	±0.5%
Microcircuits*	MIL-M-38510	All	**

*EOL Design Limits were derived from MIL-STD-1547, except those annotated by an asterisk, which were GE derived.

**Use Maximum specification limit for wide temperature range (-55°C to +125°C) for total worst-case tolerance (EOL and temperature).

I.D. 2146G 71

Size	Code Ident No.	
A	49671	PAPL-3267492

2N3501
2N4393
LM111H
2N3965
G118A
2N3972
2N4239
2N4236
2N2432A
LM108A
2N3965
LM108A LINEAR TECH
2N2484
2N3501
2N2484
G118AL
2N3972
LM101A
2N4239
2N4236
2N3811
2N3965
2N2920
2N5042
2N2484
2N4393
2N4236

2N4239
1N645
1N5617
1N3595
2N2907A
2N4236
2N4239
2N4393
2N3972
LM108ARH
1N3595
1N5617
LM101A
2N2432A
1N4111
2N4236
2N4239
2N3965
2N3970

2N4868A
2N2484
2N3972
2N3965
2N2907A
LM101A
2N3970
1N5617
2N3499

2N4236
2N4239
1N5287
1N5617
1N5297
1N3154
1N4148
1N5312
1N5291
1N4148
2N2222A
2N4393
2N3970, 2 2N3[illegible]
77

GE Astro Space

GENERAL ELECTRIC COMPANY ASTRO SPACE DIVISION
VALLEY FORGE SPACE CENTER
SURVIVABILITY ENGINEERING - BLDG. 100, ROOM M5016
KING OF PRUSSIA, PA 19406

FAX NO: (215) 354-3974
DIALCOMM: 8*747-3974
VERIFICATION NO: (215) 354-1581

TO: Fred Zalenski
COMPANY: Barnes
TELEPHONE NO: (203) 926-1777
FAX NO: (203) 926-1030

FROM: James Coleman
DATE: 4/17/91
COMPANY: GE
TELEPHONE NO: (215) 354-4874

NUMBER OF PAGES (INCLUDING LEAD PAGE): 2

MESSAGE: 2N3501 Radiation Hardness Assurance Lot Acceptance Testing Deratings. This is the last part that required testing.

MEMORANDUM

To: Fred Zalenski **Date:** April 17, 1991

From: James Coleman

Subject: 2N3501 Radiation Deratings

Provided in Table I below are the radiation deratings for the 2N3501 transistor. This device is the final device type to be tested by GE as part of the NSUS radiation hardness assurance lot acceptance testing for the ESA. This device is used in the ESA power supply (Board A2). The latest revision for the ESA shielding requirements specifies that shielding is required for the four 2N3501 devices used in the power supply. Based on the deratings from the H.A. testing, this shielding is no longer needed for these devices. The shielding analysis results indicate the dose at Q2A and Q3A is 301 and 314 krads(Si); and the dose at Q2B and Q3B is 184 and 197 krads(Si). The worst case analysis results indicate the required hfe for the 2N3501 circuit application is 17.70. The deratings from the H.A. tests at 500 krads(Si) along with the associated deratings for temperature and aging indicate that end of life gain for the 2N3501 at Ic=43ma is 23.8. This is sufficient for the application. It should be noted that the deratings provided in Table I are based on 99/90 statistics. The k value which is based on the sample size for 5 parts and 99/90 statistics is 4.67. Therefore, since the dose at the device is less than the 500 krads(Si) derating which is based on 99/90 statistics, no additional shielding is required. There is no need to have a radiation design margin of 2X when H. A. testing has been performed on the device and 99/90 statistics indicate the device is acceptable at the 1X or greater test level. Therefore, shielding for these devices is not required.

Table I

2N3501 Radiation Deratings

Device	Parameter	Derating	Rad Test Level
2N3501	Icbo @ Vcb=75V	ΔIcbo=.153μA	200 K
		ΔIcbo=1.284μA	500 K
	Δ1/hfe @ Ic=1mA;Vce=5V	Δ1/hfe=.048	200 K
		Δ1/hfe=.070	500 K
	Δ1/hfe @ Ic=10mA;Vce=1V	Δ1/hfe=.019	200 K
		Δ1/hfe=.029	500 K
	Δ1/hfe @ Ic=43mA;Vce=1V	Δ1/hfe=.019	200 K
		Δ1/hfe=.023	500 K

4/3/91

Table II

Revised Radiation Deratings

2N4393	50 k	200k	400k ~~500k~~	1000k
ΔId(off) @Vds=8V;Vgs=-5V	1171.1 ~~nA~~ pA	5713.9 ~~nA~~ pA	8967pA ~~10,593.9nA~~ pA	14,458.9 ~~nA~~ pA
ΔVgs(off) @Vds=-17V;Id=1μA	-.228V	-.228V	-.090V	-.228V
ΔVgs(off) @Vds=-2.5V;Id=1μA	-.146V	-.146V	-.139V	-.136V
ΔVgs(off) @Vds=8V;Id=1μA	-.155V	-.155V	-.643V	-.563V
ΔVgs(off) @Vds=17V;Id=1μA	-.155V	-.155V	-.183V	-.183V
K=4.67				

LM111H	20k	60k	100k	150k	200k
ΔVos @Vcc=+/-13V;Rs=50Ω	.485 ~~V~~ mV	1.36 ~~V~~ mV	2.12 ~~V~~ mV	2.96 ~~V~~ mV	10.47 ~~V~~ mV
ΔIos @Vcc=+/-13V;Rs=50Ω	1.08nA	38.42nA	281.5nA	396.2nA	1018.9nA
ΔIb+ @Vcc=+/-13V;Rs=50Ω	-116.27nA	-109.41nA	854.08nA	1501.07nA	7403.5nA
ΔIb- @Vcc=+/-13V;Rs=50Ω	-55.93nA	-41.45nA	703.33nA	1189.75nA	6550.9nA
k=4.67					

2N3965	100k	200k	500k
Δ1/hfe @Ic=35μA;Vce=-1V	.004	.005	.011
Δ1/hfe @Ic=35μA;Vce=-4V	.003	.005	.011
Δ1/hfe @Ic=100μA;Vce=-4V	.001	.004	.009
Δ1/hfe @Ic=200μA;Vce=-1V	.001	.003	.005
Δ1/hfe @Ic=2.5mA;Vce=-4V	.001	.001	.003
k=4.67			

G118AL	20k	60k	100k	200k	300k
ΔRds(on) @Vd=-10V;Vdg=-10V	65.8Ω	226.8Ω	489.5Ω	1706.9Ω	2846.1Ω
ΔIs(off) @Vsd=-20V;Vgd=0V	-49.1pA	-89.5pA	-134.5pA	-201.1pA	-279.9pA
ΔId(off) @Vds=-20V;Vgs=0V	-255.8pA	-651.6pA	-1052.9pA	-1668.9pA	-2332.4pA
ΔIgss @Vgd=-20V	-21.4pA	-49pA	-72.6pA	-137.7pA	-205.1pA
ΔVgs(th)#4 @Id=-10μA;Vds=-4V	-1.91V	-4.07V	-5.23V	-7.34V	-8.88V
k=3.44					

2N3972	100k	500k	1000k	2000k
ΔId(off) @Vds=5V;Vgs=-8V	742.4pA	568.7pA	3112.8pA	7450.9pA
ΔId(off) @Vds=10V;Vgs=-13V	2152.2pA	1134.1pA	4185pA	8588.1pA
ΔId(off) @Vds=3V;Vgs=-8V	OK 1143.9pA	1023.9pA	3704.1pA	5070.2pA
ΔIg @Vdg=14V;Vgs=-3V	272.8pA	1733.3pA	5807.7pA	9739.6pA
ΔIgss @Vgs=-20V;Vds=0V	323.7pA	2606.1pA	9699.4pA	16053pA
ΔVgs(off) @Vds=-10V;Id=1μA	-.290V	-.297V	-.290V	-.290V
ΔVgs(off) @Vds=3V;Id=1μA	-.23V	-.23V	-.23V	-.23V
ΔVgs(off) @Vds=10V;Id=1μA	-----------	-.317V	-.290V	-.193V ?
ΔGfs @Ids=.4mA;Vds=13V	.083mMho	.192mMho	.217mMho	.213mMho
k=4.67				

2N4239	50K	100k	300k	500K
Δ1/hfe @Ic=1mA;Vce=2V	.005	.013	.02 @ .9ma (.021)	.039
Δ1/hfe @Ic=20mA;Vce=3.5V	.004	.005	.007	.008
k=4.67	.004	.004		

2N4236	20k	CAL	50k	CAL	100k	CAL	300K	CAL
	.009		.011		.015		.027	
Δ1/hfe @Ic=2mA;Vce=2V	.010	.009	.012	.012	.017	.018	.028	.041
Δ1/hfe @Ic=20mA;Vce=3.5V	.008	.005	.009	.006	.010	.01	.018	.019
k=4.67 18ma Vce=3.5V	~~.006~~ .008		.009		~~.012~~ .011		~~.022~~ .019	
20ma Vce 1V							.018	
18ma Vce 1V							.019	

2N4239
2N 4393
LM 1114
G118AL

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DIALCOMM: 8*747-3974
VERIFICATION NO: (215) 354-1581

****

TO: Fred Zalenski

COMPANY: Barnes Engineering

TELEPHONE NO:

FAX NO: (203) 926-1030

****

FROM: James Coleman

DATE: 4/1/91

COMPANY: GE

TELEPHONE NO: (215) 354-4874

****

NUMBER OF PAGES (INCLUDING LEAD PAGE): 3

MESSAGE: Radiation Deratings for the 2N2432A, LM108AH, and LM108A. Please call if there any questions.

MEMORANDUM

To: Fred Zalenski **Date:** April 1, 1991

From: James Coleman

Subject: Radiation Deratings For 2N2432A and LM108AH and LM108A Devices Used In The ESA Design

Provided in the Table I below are the radiation deratings for the 2N2432A, LM108AH and LM108A devices. The deratings for the 2N2432A devices were calculated after the devices had received 600 krads(Si) total dose and been under high temperature anneal for 24 hours. The reason for subjecting these devices to high temperature anneal was due to a severe problem in collector emitter (Iceo) leakage current at the lower total dose levels. The leakage current had to be annealed out in order to determine what the actual gain degradation was. $\Delta 1/hfe$ and $\Delta Iceo$ are provided the 2N2432A. The transistor application should be revisted to determine if the increase in leakage current can be tolerated.

The deratings for the Linear Technology LM108A at 100 krads that were provided to Barnes on 3/25/91 were reviewed by myself and John Andrews. These deratings seem to be correct and are consistent across the radiation levels tested. I belive the discrepency between this data and previous data provided to Barnes is due to the devices having come from different vendors. I think we should go with the data that we have thus for and shield the devices down to the appropriate levels.

Table I

Device	Parameter	Derating	Test Level
2N2432A	Δ1/hfe@Ic=140μA and Vce=1V	.033	600 krads
	Δ1/hfe@Ic=1.4mA and Vce=1V	.017	600 krads
	Δ1/hfe@Ic=14mA and Vce=1V	.011	600 krads
	ΔIceo@Vce=1V	13uA	600 krads
LM108AH	ΔVos@Vcc=+/-15V and Rs=50Ω	-.1mV	50 krads
	ΔIb+@Vcc=+/-15V	2.8nA	50 krads
	ΔIb-@Vcc=+/-15V	7.2nA	50 krads
	ΔIos@Vcc=+/-15V	-4.7nA	50 krads
LM108A	ΔVos@Vcc=+/-15V and Rs=50Ω	1.6mV	50 krads
	ΔIb+@Vcc=+/-15V	-15nA	50 krads
	ΔIb-@Vcc=+/-15V	-15nA	50 krads
	ΔIos@Vcc=+/-15V	1.9nA	50 krads
	ΔAol@Vcc=+/-15V	4 dB	50 krads

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TO: Fred Zalenski
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FROM: James Coleman
DATE: 3/25/91
COMPANY: GE
TELEPHONE NO: (215) 354-4874

NUMBER OF PAGES (INCLUDING LEAD PAGE): 4
MESSAGE: Radiation Deratings for the 2N2484, 2N3965, LM108A, and 2N3501. Data for the 2N2032A will be provided tomorrow

2N3965 - LM108A - 2N2484 - 2N3501

MEMORANDUM

From: James Coleman

Date: March 25, 1991

To: Fred Zalenski

2N3965 – LM108A – 2N2484 – 2N3501

Subject: ESA Device Radiation Deratings

Provided in Table I below are radiation deratings at various test levels for the 2N3965, 2N2484, LM108A, and the 2N3501. Data for the 2N2432A will be provided tomorrow.

Table I

Device	Parameter	Derating	Test Level(krads(Si))
2N3965	Icbo @Vcb=50V	13 nA	500
	Δ1/hfe @Ic=.035mA;Vce=1V	.012	500
	Δ1/hfe @Ic=.035mA;Vce=4V	.012	500
	Δ1/hfe @Ic=.035mA;Vce=7V	.011	500
	Δ1/hfe @Ic=.2mA;Vce=1V	.007	500
	Δ1/hfe @Ic=.2mA;Vce=4V	.006	500
	Δ1/hfe @Ic=.2mA;Vce=7V	.006	500
	Δ1/hfe @Ic=1.2mA;Vce=1V	.005	500
	Δ1/hfe @Ic=1.2mA;Vce=4V	.004	500
	Δ1/hfe @Ic=1.2mA;Vce=7V	.004	500
	Δ1/hfe @Ic=2.5mA;Vce=1,4,7V	.0035 ~~.035mA~~	500
	Δ1/hfe @Ic=10mA;Vce=4V	.0035 ~~.035mA~~	500
	Δ1/hfe @Ic=.035mA;Vce=1,4,7V	.006	200
	Δ1/hfe @Ic=.2mA;Vce=1,4,7V	.003	200
	Δ1/hfe @Ic=1.2mA;Vce=1,7V	.003	200
	Δ1/hfe @Ic=2.5mA;Vce=1,7V	.0025	200
	Δ1/hfe @Ic=.035mA;Vce=1V	.003	100
	Δ1/hfe @Ic=.2mA;Vce=1V	.002	100

DATA
1/14/91

	Δ1/hfe @Ic=1.2mA;Vce=1V	.002		100
	Δ1/hfe @Ic=2.5mA;Vce=1V	.0015		100
LM108A LINEAR TECH	ΔVos @R=50 Ω, V=+/-15V	3.2mV	-0.3mV	100
	ΔIos	3.7nA	-18na	100
	ΔIb+	30nA	8.9na	100
	ΔIb-	-28nA	15na	100
	ΔAol	-10dB		100
2N2484	Icbo @Vcb=45V	.1nA		50
	Icbo	.2nA		200
	Icbo	.4nA		500
	Δ1/hfe @Ic=.02mA;Vce=1,5V	$\boxed{.002}$		50
	Δ1/hfe @Ic=.2mA;Vce=1,5V	.0015		50
	Δ1/hfe @Ic=1mA;Vce=1,5,10V	.001		50
	Δ1/hfe @Ic=.02mA;Vce=1,5V	$\boxed{.007}$		200
	Δ1/hfe @Ic=.2mA;Vce=1,5V	.003		200
	Δ1/hfe @Ic=1mA;Vce=1,5V	.003		200
	Δ1/hfe @Ic=10mA;Vce=10V	.002		200
	Δ1/hfe @Ic=.02mA;Vce=1,5V	$\boxed{.013}$		500
	Δ1/hfe @Ic=.2mA;Vce=1,5V	.005		500
	Δ1/hfe @Ic=1mA;Vce=1,5V	.005		500
	Δ1/hfe @Ic=.02mA;Vce=1,5V	$\boxed{.017}$		750
	Δ1/hfe @Ic=.2mA;Vce=1,5V	.007		750
	Δ1/hfe @Ic=1mA;Vce=1,5V	.006		750
2N3501	Δ1/hfe @Ic=43mA;Vce=5V	.03		50
	Δ1/hfe @Ic=43mA;Vce=1V	.04		50
	Δ1/hfe @Ic=43mA;Vce=1V	.055		200

4/1/91

LINEAR APPROX BASED ON TELCOM WITH JAME COLEMAN

$$\Delta \frac{1}{h_{FE}} = \frac{\overset{.004}{(.007-.003)}}{\underset{550}{(750-200)}} \times 1800 + .002$$

$$\Delta \frac{1}{h_{FE}} = .016$$

$$\Delta \frac{1}{h_{FE}} = \frac{\overset{.002}{(.007-.005)}}{\underset{250}{(750-500)}} \times 1500 + .005$$

$$\Delta \frac{1}{h_{FE}} = .017$$

$$\Delta \frac{1}{h_{FE}} = \frac{(.017-.007)}{(750-200)} \times 800 + .007$$

$$\Delta \frac{1}{h_{FE}} = .022$$

$$\Delta \frac{1}{h_{FE}} = \frac{(.017-.013)}{(750-500)} \times 500 + .013$$

$$\Delta \frac{1}{h_{FE}} = .021$$

$\Delta 1/h_{fe}$ @Ic=43mA;Vce=5V	.042	200
$\Delta 1/h_{fe}$ @Ic=43mA;Vce=5V	.065	500
$\Delta 1/h_{fe}$ @Ic=43mA;Vce=1V	.084	500

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TO: Fred Zalenski

COMPANY: Barnes

TELEPHONE NO:

FAX NO: (203) 926-1030

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FROM: James Coleman

DATE: 3/22/91

COMPANY: GE

TELEPHONE NO: (215) 354-4874

****

NUMBER OF PAGES (INCLUDING LEAD PAGE): 2

MESSAGE: 2N2484 and G118AL Deratings.

JNN7XV

DMSP 5D3 PARTS LIBRARY INPUT FORM
(Barnes)

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
2N2484	7.5	Δ1/hFE	0.017	0.02mA, 1V		500	EXTRAP M9027	RAY
			0.017	↓ , 5V				
			0.007	0.2mA, 1V				
			0.007	↓ 5V				
			0.006	1mA, 1V				
			0.006	↓ 5V				
G118AL	2.0	ΔVGS(TH)	-8V	VDS=VB(?)=0	Norm. off	200	M9026	SIL
			-5.5V			100K		
		ΔISOFF	-3μA/+3μA	VD=VS=VB=0	#4			
				VGS=-13V				
		ΔID(OFF)	+3μA/-2.5μA	VD=VS=VB=0				
				VGS=-13V				
		ΔIGSS	-170pA	VGB=-20V	#1			
			-136pA		#4			
		RDS(ON)	4.2KOHMS	VDB=-10, VGD=-10	#4			
			-2.7V			60K		

3/22/'91

Analyst JLA

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TO: Fred Zalenski

COMPANY: Barnes

TELEPHONE NO:

FAX NO: (203) 926-1030

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FROM: James Coleman

DATE: 3/22/91

COMPANY: GE

TELEPHONE NO: (215) 354-4874

****

NUMBER OF PAGES (INCLUDING LEAD PAGE): 5

MESSAGE: Radiation Deratings for 2N3972, LM101A, and 2N4239. Will send deratings for G118A and 2N2484 within the next hour. Call if there are any more questions.

2N39' - UM101A - 2N4239

DMSP 5D3 PARTS LIBRARY INPUT FORM

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
2N3972	1	ΔVGS(off)	-0.2V	VDS = -10V, ID = 1μA		100	M9030	SIL
	5		-0.2V			500		
	10		-0.35V			1000		
	20		-0.35V			2000		
	1		-0.2V	VDS = 3V				
	5		-0.2V					
	10		-0.3V					
	20		-0.3V					
	1		-0.2V	VDS = 10V				
	5		-0.2V					
	10		-0.3V					
	20		-0.3V					
	1	ΔID (off)	2.4nA	VDS = 10V, VGS = 13V				
	5		2.4nA					
	10		4.5nA					
	20		9.5nA					
	0.2		0.5nA		INTERP.			
	1	ΔID (off)	0.6nA	VDS = 5V, VDG = 13V				
	5		0.8nA					
	10		3.5nA					
	20		8.5nA					

– more –

3/4/91

Analyst JLA

DMSP 5D3 PARTS LIBRARY INPUT FORM

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
2N3972 (cond.)	1	ΔID(OFF)	1.0 nA	VDS=3V, VGS=-8V				
	5	↓	1.2 nA	↓		$\Delta I_{D(OFF)}$	$(50K) = -\frac{(4200pA-1000pA)}{(1000-100)}(50) + 1000$	
	10	↓	4.2 nA	↓				
	20	↓	5.8 nA	↓		$\Delta I_{D(OFF)}$	$(50K) = -178 + 1000 = 822$ pA	
	1	ΔIG	0.3 nA	VDG=14V, VGS=-3V				
	5	↓	1.9 nA	↓		ΔI_G	$(50K) = -\frac{(1.9n-.3n)}{(500-100)} \times (50) + .3na$	
	10	↓	6.6 nA	↓				
	20	↓	11 nA	↓		ΔI_G	$(50K) = -\frac{(1.6n)}{400}(50) + .3na = .1na$	
	1	ΔIGSS	0.4 nA	VGS=-20V, VDS=0				
	5	↓	3.0 nA	↓				
	10	↓	11 nA	↓				
	20	↓	18 nA	↓				
	1	Δgfs	±0.1 mMho	IDS=0.4mA, VDS=13V				
	5	↓	-0.6	↓				
	10	↓	-0.6	↓				
	20	↓	-0.6	↓				
	1	Δgfs	-0.19 mMho	IDS=2mA, VDS=6V				
	5	↓	-1.2	↓				
	10	↓	-1.6	↓				
	20	↓	-1.6	↓				

3/4/91

Analyst ______

DMSP 5D3 PARTS LIBRARY INPUT FORM

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
LM101A	0.2	ΔVOS	±0.02mV	+/- 15V, 2kΩ	Barnes	20	M9038	LINTECH
		ΔIOS	1.8nA					
		ΔIB	-17nA					
		AOL	1115 V/mV	121 db (120.95)				
	0.6	ΔVOS	±0.026mV					
		ΔIOS	2.7nA			60		
		ΔIB	-70nA					
		AOL	855 V/mV					
	1.0	ΔVOS	-0.2mV					
		ΔIOS	6.1nA			100		
		ΔIB	-130nA					
		AOL	783 V/mV					
	2.0	ΔVOS	-0.6mV					
		ΔIOS	12.5nA			200		
		ΔIB	-270nA					
		AOL	612 V/mV					
	4.0	ΔVOS	-1.2mV					
		ΔIOS	18nA			400		
		ΔIB	-510nA					
		AOL	186 V/mV	105 db (105.39)				

Δ = 16db (15.56db)

3/7/91

Analyst JLA

DMSP 5D3 PARTS LIBRARY INPUT FORM

V1

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
2N4239	7.5	Δ 1/hFE	0.07	$I_C = 1mA, V_{CE} = 2V$	Barnes	750	M9032	PPC
				or 3.5V				
			0.031	5mA				
			0.017	20mA				
			0.015	50mA				
			0.018	$I_C = 15mA, V_{CE} = 6V$				
Δ 1/hFE @ 25mA	→	$\frac{.017-.015}{50-20} =$	$\frac{.002}{30mA}$					
Δ $\frac{1}{hFE}$ @ 25mA	= .015	+ $\frac{.002}{30mA} \times 25mA =$	.015 + .002	= .017				

Data avail for lower rad levels also.

3/5/91

Analyst JLA

CARROLL

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TO: Fred Zalenski

COMPANY: Barnes

TELEPHONE NO:

FAX NO: 203 926 1030

FROM: John Andrews

DATE: 3-18-91

COMPANY: GE

TELEPHONE NO: 215 354 3840

NUMBER OF PAGES (INCLUDING LEAD PAGE): 2

MESSAGE: These 2N4236 deratings supersede memo by J. Coleman dated 2-28-91. We will be out on 3/19 if any problems.

DMSP 5D3 PA...S LIBRARY INPUT FORM

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
2N4236	0.2	Δ 1/hFE	0.006	Ic = 18mA, 1V		20	M9031	SOL.
	↓	↓	0.006	18mA, 3.5V				
			0.007 ✓	2mA, 2V				
	0.5		0.009	18mA, 1V		50	LINEAR	APPROX
	↓		0.009	18mA, 3.5V				
			0.011 ✓	2mA, 2V			$\Delta \frac{1}{hFE}$ (200K)	$= \frac{.023-.012}{300-100} \times 100 + .012$
	1.0		0.012	18mA, 1V		100	$\Delta \frac{1}{hFE}$ (200K)	= .0175
	↓		0.012	18mA, 3.5V				
			0.015 ✓	2mA, 2V				
	3.0		0.023	18mA, 1V		300		
	↓		0.022	18mA, 3.5V				
		↓	0.027 ✓	2mA, 2V	—			

3/18/91

Analyst JLA

DMSP 5D3 PARTS LIBRARY INPUT FORM

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfr.	
2N3811	7.5	Δ^1/h_{FE}	0.14	1μA V_{CE}=1V			JPL EXTRAP.	MOTA	
			0.033	10μA					
			0.013	100μA					
			0.011	500μA					
			0.009	1mA					
			0.007	10mA					
	→ delete prior		Δ^1/h_{FE}	line					
2N3965	5	Δ^1/h_{FE}	0.012	0.1mA, 0.5V	REV.	500	JPL 85-43	MOTA	(3964)
			0.007	1mA, 0.5V					
			0.0045	1mA, 30V					
			0.007	20mA, 30V					
2N2920	7.5		0.07	0.1mA, 10V			JPL EXTRAP.	MOTA	
			0.012	10mA, 10V					
			0.024	1mA, 10V					
			0.007	0.5mA, 10V					
2N5042	7.5	Δ^1/h_{FE}	0.032	50mA, 1V			JPL EXTRAP.	FAS	(2605)
			0.10	6mA, 1V					
		I<80	-32nA	V_{CB}=30V					

$\Delta \frac{1}{h_{FE}}$ @ .25ma → $\frac{.012 - .007}{1 - .1ma} = \frac{.005}{.9ma}$

3/7/91

$\therefore \Delta \frac{1}{h_{FE}}$ @ .25ma = .007 + $\frac{.005}{.9ma}$ × .75ma = .011

Analyst ____________

JNNTXV2N24…

DMSP 5D3 PARTS LIBRARY INPUT FORM

(Barnes)

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl (krads(Si))	Data Source	Tested Mfgr.
2N2484	0.5	ICBO	0.1nA	45V		50	M9027	RAY
	2	↓	0.2nA			200		
	5		0.4nA			500		
	0.5	Δ1/hFE	0.002	0.02mA, 1V				
			0.002	↓ 5V				
			0.0015	0.2mA, 1V				
			0.0015	↓ 5V				
			0.001	1mA, 1V				
			0.001	↓ 5V				
			0.001	10mA 10V				
	2.0		0.007	0.02mA, 1V				
			0.007	↓ 5V				
			0.003	0.2mA 1V				
			0.003	↓ 5V				
			0.003	1mA 1V				
			0.003	↓ 5V				
			0.002	10mA, 10V				
	5.0		0.013	0.02mA, 1V				
			0.013	↓ 5V				
			0.005	0.2mA 1V				
			0.005	↓ 5V				

0.005 1mA 1V
0.005 ↓ 5V

/ 191

Analyst ______

94

To: Fred Zalenski

Date: March 4, 1991

From: James Coleman

Subject: Radiation Deratings For 2N4393 Transistor Used In ESA

Provided in the Table I below are the radiation deratings for the 2N4393 n-channel JFET. The 2N4393 is one of the part types provided by Barnes for radiation hardness assurance testing. If there are any questions regarding the deratings provided, please don't hesitate to call.

Table I

Device	Parameter	Derating	Test Level
2N4393	ΔId(off) @Vds=8V and Vgs=-5V	1.35 nA	50 krads
		6.5 nA	200 krads
		12 nA	500 krads
	ΔVgs(off) @Vds=17V and Id=1μA	-.26 V	500 krads
		-.26 V	2000 krads
	ΔVgs(off) @Vds=-2.5V, 8V,17V and Id=1 μA	-.2 V	2000 krads

MEMORANDUM

To: Fred Zalenski

Date: Feb. 28, 1991

From: James Coleman

Subject: Radiation Deratings For 2N4236 Transistor Used In ESA

Provided in the Table I below are the Δ1/hfe radiation deratings for the 2N4236 transistor. The 2N4236 is one of the part types for which Barnes provided samples for radiation hardness assurance testing. If there are any questions regarding the deratings provided, please don't hesitate to call.

Table I

Device	Parameter	Derating (SEE MEMO DATED 3/18/91)			Test Level
2N4236	Δ1/hfe@Ic=2mA and Vce=2V	~~.008~~ .009			20 krads
		~~.010~~ .011			50 krads
		~~.013~~ .015			100 krads
		~~.023~~ .027			300 krads
	Δ1/hfe@Ic=~~20mA~~ 18ma and Vce=3.5V	.003	.006	1K .006	20 krads
		.004	.009	.009	50 krads
		.005	.012	.012	100 krads
		.009	.022	.023	300 krads

$\Delta \frac{1}{hfe}$ @ 14ma

$$\frac{.023-.009}{20-2} = \frac{.014}{18} = .00078/ma$$

$\therefore \frac{1}{hfe}$ @ 14ma $= .009 + (.00078)(6) = .014$

$\Delta \frac{1}{hfe}$ @ 14ma

$$\frac{.027-.023}{18-2} = \frac{.004}{16} =$$

$\therefore \frac{1}{hfe}$ @ 14ma $= .023 + \frac{.004}{16}(4) = .024$

C-2

MEMORANDUM

To: Fred Zalenski

Date: Feb. 27, 1991

From: James Coleman

Subject: Radiation Deratings For Devices Used In ESA Design

Provided in the Table I below are the Δ1/hfe radiation deratings for the 2N4239 transistor. The 2N4239 is one of the part types for which Barnes provided samples for radiation hardness assurance testing. Additional deratings are also provided per your request for the 1N645, 1N5617, and 1N3595 diodes. Deratings on the diodes were requested during our phone conversation last week. If there are any questions regarding the deratings provided, please don't hesitate to call.

Table I

Device	Parameter	Derating	Test Level
2N4239	Δ1/hfe @Ic=1mA	.014 → .0148 @ .9mm	100 krads
	Δ1/hfe @Ic=5mA	.007	100 krads
	Δ1/hfe @Ic=20mA	.005	100 krads
	Δ1/hfe @Ic=50mA	.004	100 krads
1N645	Ir @Vr=1V	300 nA	500 krads
1N5617	ΔVf @If=10mA	0.4 mV	750 krads
1N3595	Ir @Vr=10V	3 nA	750 krads

GE Astro Space

GENERAL ELECTRIC COMPANY ASTRO SPACE DIVISION
VALLEY FORGE SPACE CENTER
SURVIVABILITY ENGINEERING - BLDG. 100, ROOM M5016
KING OF PRUSSIA, PA 19406

FAX NO: (215) 354-3974
DIALCOMM: 8*747-3974
VERIFICATION NO: (215) 354-1581

****

TO: FRED ZALENSKI

COMPANY: BARNES

TELEPHONE NO: X311

FAX NO: 203 926 0049

****

FROM: JOHN ANDREWS

DATE: 2-14-91

COMPANY: GE

TELEPHONE NO: 215 354 3840

****

NUMBER OF PAGES (INCLUDING LEAD PAGE): 3

MESSAGE: MORE FOR NSUS PER YOUR FAX OF 2/7/91

DMSP 5D3 PARTS LIBRARY INPUT FORM

Barnes pg. 1A

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
2N2907A	0.5	Δ1/β	0.015	IC=1mA VCE=10V		100	F1099A	MOTA
		Δ1/β	0.01	IC=10mA VCE=10V				
2N4236		TEST NEEDED	; NO PRIOR DATA					
2N4239								
2N4393	2	ΔVGS(OFF)	-0.04 V	VDS=15V, ID=1mA		200	H9087	SIL
	1	↓	-0.02 V			100		
	0.5	↓	-0.01 V	↓		50		
	2	ΔID(OFF)	5 nA	VDS=10V, VGS=-5V		200	JPLVI	SIL
	1	↓	3 nA			100	↓	
	0.5	↓	2 nA	↓				
	1	ΔIDGO	4 nA	VDG=13V			EVALJA	
	0.5	↓	2 nA	↓				
2N3972	0.2	ΔID(OFF)	1 mA	VDS = 5V			EVALJA	
	0.2	ΔIDGO	1 mA	VDG=12V				
LM108ARH	5	AOL	110V/mV	VS=±13V	RL=10KΩ REV.	500	K9158	NSC
	1	AOL	70V/mV	↓		100		
	5	ΔVOS	0.5mV	RS=50Ω	REV.			
	1	ΔVOS	0.2 mV					
	5	ΔIOS	4 nA	Rs=50Ω	REV.			
	1	ΔIOS	3 nA					
	5	ΔIB	- 13mA		REV.			
	1	ΔIB	- 4nA					

2/10/91

Analyst J.L. Andrews

DMSP 5D3 PARTS LIBRARY INPUT FORM

Barnes pg 1B

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Total Mfgr.
1N3595	2	ΔIR	0.8nA	VR = 10 V	JANTXV P/N	250	B0181	ISC
	1	ΔIR	0.4nA	VR = 10 V				
	5	ΔIR	2nA					
1N5617	10	VBKDN	380 V	I=50 μA		—	EVALJA	
	5		410 V					
	2		430 V					
LM101A	2.5	ΔIOS	250 nA	Vcc=+/-15V	REV	250	D0029	LINT.
	2.5	ΔAOL	-14 DB					
LM101A		LOT	TEST RE	COMMENDED				
2N2432A	3	Δ1/hFE	0.16	Ic= 3/4 mA	JANS	500	JPL81-66	TI
	2		0.12					
	1		0.07					
1N4111	5	ΔVZ	±0.2V	Iz= 1/4 mA			H5084	
2N4236								
2N4239		derating	by 2/27					
2N3965		derating	by 2/23					
2N3970		derating	by 2/23					

2/14/91

Analyst J. Andrews

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GENERAL ELECTRIC COMPANY ASTRO SPACE DIVISION
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KING OF PRUSSIA, PA 19406

FAX NO: (215) 354-3974
DIALCOMM: 8*747-3974
VERIFICATION NO: (215) 354-1581

****

TO: Carroll Klech

COMPANY: EDO Corp.

TELEPHONE NO: 203-926-1777

FAX NO: 203-926-1030

****

FROM: James Coleman

DATE:

COMPANY:

TELEPHONE NO:

****

NUMBER OF PAGES (INCLUDING LEAD PAGE): 6

MESSAGE: CARROll,

This is most of the data that you requested to complete the Worst Case Analysis. Additional data will be provided to you on Monday.

James Coleman

010-LLR-1

Test Candidates (for Barnes)

1. 2N 3970 100, 300, 700, 1200, 1800 KRads

2N 4236, 2N 4239: 50, 100, 500, 1000, 1500

2N 3965 25, 50, 100

J. Andrews
1-24-94

DMSP 5D3 PARTS LIBRARY INPUT FORM

(BARNES REQUIRED DATA PP1-3)

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
2N4868A	1.00	ΔIGS	0.3 mA	VDG = 5V		100	JPL-VI	SIL
	1	Δgfs	0	ID = .03mA and				
				VDS = 5V				
	6	ΔIGS	35mA					
	6	Δgfs	0					
2N2484	1	Δ1/hFE	0.042	VCE = 3V,		100	JPL-VI	MOTA
				IC = 1mA				
2N3972	3	ΔIDGO	7.5mA	VDG = 10V		300	JPL Vol I	SIL
	7	ΔIDGO	12 mA	VDG = 10V		700		
2N3965		See below			TEST			
2N2907A	0.5	Δ1/hFE	0.005	Ic = 1mA, VCE		250	F0101	MOTA
				= 5V				
LM101A	0.5	ΔAOL	±10dB	V = ±15V, 5mA		50	JPL VII	NSC
LM108ARH	0.5	ΔIB	−2.5mA	VS = ±15V		100	K9158	NSC
		See below	for contin	uation				
2N3970		TEST RE	QUIRED;	WOULD ALSO	GET			
		DATA FOR	2N3972 IN	SAME FAMILY.	SEE			

BELOW FOR DERATINGS BASED ON SIMILAR 2N4391.

1/24/91

Analyst J. Andrews

DMSP 5D3 PARTS LIBRARY INPUT FORM

(BARNES REQUIRED DATA pp 4 - 5)

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
1N5617	18	ΔVBR	-10V	I = 50 μA				
	5	ΔVBR	2V	I = 50 μA			LM-M/S	
							-WGJA	
2N3499	0.5	Δ1/hFE	0.012	IC = 40mA	SIM. TO 2N3501	≥80	JPL-VI	MOTA
	18	Δ1/hFE	0.09	IC = 40mA				
2N4236		TEST RECO	MMENDED	NEED 6 SAM	PLES			
2N4239		TEST RECO	MMENDED	NEED 6 SAM	PLES			
1N5287	7	ΔIP	± 5μA	VS = 15V				
	20	ΔIP	±20 μA	VS = 15V		5	F1185A	MOTA
	7	ΔIP	±10 μA	VS = 25V				
	20	ΔIP	±40 μA	VS = 25V				
1N5617	20	ΔVBR	-12 V	I = 50 μA				
							LM-M/S	
1N5297	20	ΔIP	±12 μA	VS = 5V				
	20	ΔIP	±26 μA	VS = 12V		5	F1185A	MOTA
1N4104	20	ΔVF	500N	IF = 0.2mA				

1/24/91

Analyst J. Andrews

DMSP 5D3 PARTS LIBRARY INPUT FORM
(BARNES REQUIRED DATA PP5-6)

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
1N3154	20	ΔVZ	−1V	IF ≥0.5mA				
			TEST RECOMMENDED				JA-WG	
1N4148	10	ΔVF	0.6mV	IF=0.1mA		500	EVAL JA	
1N5312	10	ΔIP	±13μA	VS=10V		500	F1185A	MOTA
1N5291	7	ΔIP	±3μA	VS=7V		500	F1185A	MOTA
1N4148	10	ΔIR	200nA	VR=10V		500	LM EVAL	UNI
	10	ΔVF	6mV	IF =1.2mA				
	10	ΔVF	0.5mV	IF =0.1mA				
2N2222A	2	Δ1/hFE	0.026	IC=1mA VCE=1V			F1032R	
	10		0.075					
	20		0.104					
2N4393	5	ΔID(OFF)	9nA	VDS=10V, VGS=-5V		500	JPLVI	SIL
	20	ΔID(OFF)	26nA	VDS=10V, VGS=-5V		2000		
	5	ΔVGS	~~0.1V~~	VDS=10V		500		
	20	ΔVGS	0.3V	VDS=10V		2000		

1/24/91 Analyst J. Andrews

DMSP 5D3 PARTS LIBRARY INPUT FORM

BARNES REQUIRED DATA PP 3, 7 (1-2)

Generic Part Number	Rad Lvl	Parameter	Derating	Test Conditions	REMARKS 3	Test Lvl Krads(Si)	Data Source	Tested Mfgr.
2N3970	1	ΔVGS(OFF)	+20mV	VDS=10V		100	JPL Vol I	SIC
	6.5	ΔVGS	+0.12V	VDS=10V		650		
	18	ΔVGS	+0.3V	VDS=10V		1000		
	1	ΔIGSS	2nA	VGS=-12V		100		
	6.5	ΔIGSS	11mA	VGS=-12V		650		
	18	ΔIGSS	25nA	VGS=-12V		1000		
2N3972		ΔVGS	See 2N3970 Deratings					
	5,10	Δgfs	0					
		others	500n					
continuation LM108ARH	0.5	ΔVOS	0.8mV	50 OHM				
	0.5	ΔIOS	-1.4nA					
	0.5	ΔAOL	100 V/mV	RL=10KOHM				
2N3965	.25	Δ1/hFE	.0025	IC=30μA				
	.5	↓	.006	↓	TEST		NSREC-72 CORRAGE/	?
	1.0		.02		RECOMMENDED		WEC CLAIM	
	.25	Δ1/hFE	.0015	IC=0.2mA				
	.5	↓	.0025	↓				
	1		.006					
	.25	Δ1/hFE	.0015	IC=1mA				
	.5	↓	.0025	↓				
	1		.006					

Analyst J. Andrews

GENERAL ELECTRIC
SPACE DIVISION
PHILADELPHIA

PROGRAM INFORMATION REQUEST / RELEASE

PIR NO.	*CLASS. LTR.	OPERATION	PROGRAM	SEQUENCE NO.	REV. LTR.
	U	— 1M93	— DMSP	— 3648	D

*USE "C" FOR CLASSIFIED AND "U" FOR UNCLASSIFIED

FROM	TO
John Andrews	Tom Linnen (10)

DATE SENT	DATE INFO. REQUIRED	PROJECT AND REQ. NO.	REFERENCE DIR. NO.
JAN. 11,1991			

SUBJECT

DMSP 5D3/NSUS RADIATION DERATINGS

INFORMATION REQUESTED/RELEASED

1. SUMMARY

This PIR provides total dose radiation deratings for radiation sensitive parts on the current (Rev. L) DMSP Program Parts List of GE-ASD and its subcontractors. Accompanying text aids its use. A small team of Valley Forge and East Windsor staff has contributed to this activity.

A vertical bar in the left margin of Table 2 indicates a change from the Rev. C issue. These changes affect about 5% of the parts and include additions of alternate parts less sensitive or hardened against dose effects.

Missing deratings for about three part types will be developed in February following development testing.

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107

PAGE NO. ___ OF ___

RETENTION REQUIREMENTS

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☐ 1 MO.	☐ 3 MOS.
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For some parts only one vendor's parts can meet the stated derating; remarks 3 surface this limitation; this is especially true for CMOS technology.

In some instances a vendor makes parts in both soft and hard processes. The hard parts may have a substantial impact on procurement costs whereas soft parts usage may have an impact on shielding costs.

5. METHODOLOGY OF DERATING

The methodology of deratings usually employed here is as follows: An applicable data set is found (vendor, environment, etc.) and then the mean (x) and standard deviation (sigma) are located or determined for each parameter. The derating for each parameter is developed by summing the mean and ±5.54 sigmas and then rounding up to the next round number (i.e. 1.97 is rounded to 2.0) at each test radiation level of interest. Files are maintained in Survivability Engineering to show calculations and/or generate additional deratings as appropriate.

Resultant deratings are related to device radiation capability and are not likely to be exceeded in subsequent hardness assurance testing at the cited radiation level.

TABLE 2

JMSP 5D3/NSUS RADIATION DERATINGS PAGE: 1 DATE:01-14-1991

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
1N645-1	SMALL SIGNAL	JANS1N645-1	5	DELTA IR	10 uA	VR = 28 V	
				DELTA VF	30 mV	IF = 0.1 A	
1N645-1	RECTIFIER	JANS1N645-1					
1N645-1	SMALL SIGNAL	JANS1N645-1					
1N647-1	GENERAL PURPOSE	JANS1N647-1	5	DELTA IR	10 uA	VR = 50 V	
				DELTA VF	30 mV	IF = 0.4 A	
1N746A-1	ZENER 3.3V	2613110-2	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N747A-1	VOLT REGULATOR	34054666-001	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N748A-1	ZENER 3.9V	2613110-3	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N751A-1	ZENER 5.1V	2613110-4	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N751A-1	VOLT REGULATOR	34054667-001					
1N752A-1	VOLT REG	317839-001	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N753A-1	VOLT REGULATOR	34054668-001	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N754A-1	ZENER 6.8V	JANS1N754A-1					
1N754A-1	ZENER 6.8V	5961012352222	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N754A-1	SWITCHING	JANS1N754A-1					
1N756A	VOLT REG	JANS1N756A-1					
1N756A-1	ZENER 8.2V	JANS1N756A-1	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N756A-1	VOLT REG	317839-005					JANTXV
1N757A-1	VOLT REGULATOR	JANS1N757A-1	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N759A-1	ZENER 12V	JANS1N759A-1					
1N759A-1	ZENER 12V	5961012352225	5	DELTA VZ	+/- 2 %	IZ = 20 mA	
1N821-1	VOLTAGE REF	2613110-5	5	DELTA VZ	0.02 V	IZ = 7.5 mA	
1N821-1	ZENER	2613120-2					
1N829-1	VOLT REFERENCE	34054669-001	5	DELTA VZ	0.02 V	IZ = 7.5 mA	
1N935B	VOLTAGE REF	2613110-6	5	DELTA VZ	0.05 V	IZ = 7.5 mA	
1N943B-1	VOLT REFERENCE	34058411-001	5	DELTA VZ	-0.1 V	IZ = 7.5 mA	
1N965B-1	ZENER	49868-9716-S965B	5	DELTA VZ	+0.1 V	IZ = 8.5 mA	
1N967B-1	ZENER 18V	JANS1N967B-1					
1N967B-1	ZENER 18V	5961012359290	5	DELTA VZ	0.2 V	IZ = 7 mA	
1N967B-1	ZENER	49868-9716-S967B					
1N968B-1	ZENER 20V	JANS1N968B-1					
1N968B-1	ZENER 20V	5961012359291	5	DELTA VZ	0.2 V	IZ = 6.2 mA	
1N973B-1	ZENER 33V	JANS1N973B-1	5	DELTA VZ	0.4 V	IZ = 3.8 mA	
1N981B-1	VOLTAGE REGULATOR	JANS1N981B-1	5	DELTA VZ	-5 V	IZ = 1.8 mA	
				DELTA IR	10 nA	VR = 50 V	
1N1202A	RECTIFIER	2613110-7	5	DELTA IR	200 nA	VR = 100 V	
				DELTA VF	0.1 V	IF = 0.1 A	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
1N3023B	ZENER	49868-9716-3023B	5	DELTA VZ	-0.5 V	IZ = 19 mA	
1N3154	VOLTAGE REFERENCE	49868-9716-3154	5	DELTA VZ	-0.18 V	IZ = 10 mA	
1N3337RB	ZENER, HI-SURGE	3261143-1	5	DELTA IR	20 uA	VR = 56 V	
				DELTA VZ	3 %	IZ = 170 mA	
1N3595	SWITCHING	2613110-8	5	DELTA IR	10 nA	VR = 5 V	
1N3595	RECTIFIER	JANTXV1N3595-00W					
1N4103	VOLT REG	317839-002					
1N4103	VOLT REGULATOR	34054711-001	5	DELTA VF	0.03 V	IF = 250 mA	Same family as 1N4104.
1N4104	ZENER	JANTXV1N4104-00W					
1N4104	VOLT REG	317839-003	10	DELTA VF	0.02 V	IF = 1 mA	
			5	DELTA VF	0.03 V	IF = 250 uA	
1N4108	ZENER	JANTXV1N4108-00W	5	DELTA VF	0.03 V	IF = 250 mA	Same family as 1N4104.
1N4111	ZENER	JANTXV1N4111-00W	5	DELTA VF	0.03 V	IF = 250 mA	
1N4148	SWITCHING	JANS1N4148-1	5	DELTA IR	40 nA	VR = 5 V	JANTXV
				DELTA VF	30 mV	IF = 10 mA	
1N4148-1	SWITCHING	5961012352206					
1N4148-1	SWITCHING	JANS1N4148-1					
1N4148-1	SWITCHING	JANS1N4148-1					
1N4150-1	SWITCHING	5961012352207	5	DELTA IR	50 nA	VR = 5 V	
				DELTA VF	0.1 V	IF = 0.2 A	
1N4153-1	SWITCHING	2613110-10	5	DELTA IR	50 nA	VR = 5 V	DIE SIMILAR TO 1N4148
				DELTA VF	0.1 V	IF = 0.2 A	
1N4153-1	SILICON SWITCHING	49868-9716-4153					
1N4245	RECTIFIER	JANTXV1N4245					
1N4245	POWER RECTIFIER	97009-000-453	5	DELTA VF	0.13 V	IF = 3 A	JANTXV
				DELTA VR	5 uA	VR = 100 V	
1N4371A	VOLT REGULATOR	JANTXV1N4371A	5	VF	0.027	IF = 5 mA	
1N4454-1	**WITHDRAWN**	34058412-001					
1N4454-1	**WITHDRAWN**	34064306-001					
1N4565A	VOLT REFERENCE	34054670-001	5	DELTA VZ	-0.07 V	IZ = 0.5 mA	
1N4567A	VOLT REF	JANTXV1N4567A	5	DELTA VZ	-0.07 V	IZ = 0.5 mA	Same family as 1N4565A.
1N4569A	VOLTAGE REF	2613110-11	5	DELTA VZ	-0.07 V	IZ = 0.5 mA	
1N4571A	VOLTAGE REFERENCE	97009-000-454	5	DELTA VZ	-0.05 V	IZ = 1 mA	JANTXV
1N4572A	VOLTAGE REF	2613110-12	5	DELTA VZ	-0.05V	IZ = 1 mA	
1N4572A	VOLT REFERENCE	JANTXV1N4572A	5	DELTA VZ	-0.05 V	IZ = 1 mA	
1N4573A	VOLT REFERENCE	JANTXV1N4573A	5	DELTA VZ	-0.05 V	IZ = 1 mA	
1N4627-1	ZENER	2613110-13	5	DELTA VZ	-0.05 V	IZ = 0.25 mA	NOISE CONCERN
1N4774A	VOLTAGE REF	2613109-1	5	DELTA VZ	45 mV	IZ = 1 mA	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
1N4780A	ZENER	21-806-0036-00W	5	DELTA VZ	50 mV	IZ = 1 mA	RAD HARD DEVICE AVAILABLE
				DELTA IR	1 uA	VR = 6 V	
1N4897A	VOLTAGE REF	2613117-1	5	DELTA VZ	80 mV	IZ = 0.5 mA	
				DELTA IR	5 uA	VR = 9 V	
1N4903A	VOLTAGE REF	2613112-1	5	DELTA VZ	40 mV	IZ = 1.0 mA	
				DELTA IR	5 uA	VR = 9 V	
1N4938	SWITCHING	JANTX1N4938	5	DELTA IR	30 nA	VR = 175 V	MSC OR UNITRODE
				DELTA VF	30 mV	IF = 200 mA	
1N4938-1	SWITCH/RECTIFIER	2613111-1	5	DELTA IR	30 nA	VR = 175 V	MSC OR UNITRODE
				DELTA VF	30 mV	IF = 200 mA	
1N4942	SWITCH/RECTIFIER	2613110-14	5	DELTA VF	0.1 V	IF = 1 A	
1N4960	VOLT REGULATOR	JANTXV1N4960	5	DELTA VZ	+/- 1.2 V	IZ = 100 mA	
				DELTA IR	450 nA	VR = 9.1 V	
1N4961	ZENER 13V	3261429-1	5	DELTA VZ	+/- 1.3 V	IZ = 100 mA	
				DELTA IR	450 nA	VR = 9.9 V	
1N4973	VOLTAGE REGULATOR	97009-000-455	5	DELTA VZ	0.5 V	IZ = 30 mA	JANTXV
				DELTA IR	3 uA	VR = 30 V	
1N4979	ZENER 75 V	2613110-22	5	DELTA VZ	+/- 1 V	IZ = 20 mA	
				DELTA IR	500 nA	VR = 56 V	
1N5148A	VARACTOR	49868-9716-5148A	5	DELTA CT	1 pF	1 MHz	
1N5186	RECTIFIER	317839-004	5	DELTA VF	100 mV	VF = 5 A	
				DELTA IR	10 uA	VR = 60 V	
1N5283	CURRENT REG	2613110-20	5	IP	0.209 mA MIN	V = 25 V	
					0.231 mA MAX		
1N5287	CURRENT REGULATOR	JANTXV1N5287-00W	5	IP	0.314 mA MIN	V = 25 V	
					0.346 mA MAX		
1N5288	CURRENT REGULATOR	JANTXV1N5288-00W	5	IP	0.371 mA MIN	V = 25 V	
					0.409 mA MAX		
1N5290	CURRENT REGULATOR	JANTXV1N5290-00W	5	IP	0.447 mA MIN	V = 25 V	
					0.493 mA MAX		
1N5291	CURRENT REG	2613110-15	5	IP	0.532 mA MIN	V = 25 V	
					0.588 mA MAX		
1N5297	CURRENT REG	2613110-16	5	IP	0.950 mA MIN	V = 25 V	
					1.050 mA MAX		
1N5297	CURRENT REGULATOR	JANTXV1N5297-00W					
1N5310	CURRENT REGULATOR	JANTXV1N5310	5	IP	3.135 mA MIN	V = 25 V	
					3.465 mA MAX		
1N5312	CURRENT REGULATOR	JANTXV1N5312-00W	5	IP	3.805 mA MIN	V = 25 V	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
					4.095 mA MAX		
1N5416	RECTIFIER	JANS1N5416	5	DELTA BV	-40 V	IR = 50 uA	
1N5417	RECTIFIER	JANS1N5417	5	DELTA BV	-40 V	IR = 50 uA	
1N5417	RECTIFIER	5961012352215					
1N5417	RECTIFIER	JANS1N5417					
1N5550	RECTIFIER	2613110-17					
1N5550	RECTIFIER	34062128-002					
1N5550	RECTIFIER	2613120-1	5	DELTA IR	100 nA	VR = 100 V	
				DELTA VF	50 mV	IF = 3 A	
1N5551	RECTIFIER	2613120-1	5	DELTA IR	150 nA	VR = 200 V	
				DELTA VF	50 mV	IF = 3 A	
1N5552	RECTIFIER	2613120-1	5	DELTA IR	170 nA	VR = 300 V	
				DELTA VF	50 mV	IF = 3 A	
1N5615	RECTIFIER	JANS1N5615	5	DELTA IR	20 uA	VR = 28 V	
				DELTA VF	0.12 V	IF = 3A	
1N5615	RECTIFIER	JANS1N5615					
1N5617	RECTIFIER	JANS1N5617	5	DELTA IR	2 uA	VR = 140 V	
				DELTA VF	0.12 V	IF = 3 A	
1N5656A	VOLT SUPPRESSOR	34072821-001	5				PART OUT OF DESIGN.
1N5711	SWITCHING	2613110-25	10	DELTA IR	100 nA	VR = 5 V	
				DELTA VF	30 mV	IF = 500 uA	
1N5711	SWITCHING	JANTXV1N5711					
1N5711	SWITCHING	JANTXV1N5711					
1N5806	FAST RECOVERY	JANS1N5806	5	DELTA IR	10 uA	VR = 28 V	
				DELTA VF	30 mV	IF = 1 A	
1N5809	FAST RECOVERY RECT	JANTXV1N5809	2.5	DELTA IR	170 nA	VR = 50 V	
			5	IR	10 uA	VR = 16 V	
				DELTA VF	50 mV	IF = 10 mA	
				DELTA VF	100 mV	IF = 1 A	
				DELTA VF	50 mV	IF = 10 mA	
				DELTA VF	IF = 1 A		
1N5809	FAST RECOVERY RECT	JANS1N5809					
1N5811	RECTIFIER	JANS1N5811	5	DELTA IR	10 uA	VR = 28 V	
				DELTA VF	30 mV	IF = 1 A	
			10	DELTA VF	50 mV	IF = 1A	
1N5816	RECTIFIER	2613110-24	5	DELTA IR	10 uA	VR = 28 V	
				DELTA VF	30 mV	IF = 1 A	
1N5823	HOT CARRIER RECT	719083-1U	5	DELTA VF	30 mV	IF = 5 A	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
				DELTA IR	20 uA	VR = 10 VDC	
1N5829	HOT CARRIER RECT	719083-2U	5	DELTA VF	30 mV	IF = 25 A	
				DELTA IR	40 uA	VR = 10 VDC	
1N6084B	ZENER	2613113-1	5	DELTA VZ	50 mV	IZ = 250 uA	
				DELTA IR	100 nA	VR = 3 V	
1N6084D	ZENER	2613113-4					
1N6086B	ZENER	34050988-001	5	DELTA VZ	200 mV	IZ = 10 uA	
				DELTA IR	150 nA	VR = 3 V	
1N6088B	ZENER	2613113-2	5	DELTA VZ	200 mV	IZ = 10 uA	
				DELTA IR	150 nA	VR = 4 V	
1N6091B	ZENER	2613113-3	5	DELTA VZ	200 mV	IZ = 10 uA	
				DELTA IR	200 nA	VR = 6 V	
1N6100	DIODE ARRAY	2613110-19	5	DELTA IR	50 nA	VR = 4 V	
HP5082-0020	MICROWAVE	317945	5	ALL	NEGLIGIBLE EFFECT		
HP5082-2411	SCHOTTKY	317949	5	ALL	NEGLIGIBLE EFFECT		
HPA5082-B523	HOT CARRIER	2613122-1	5	ALL	NEGLIGIBLE EFFECT		
HSCH5082-0816	SCHOTTKY BARRIER	49879-9716-1	5	ALL	NEGLIGIBLE EFFECT		
JANTXV1N4148-1	SWITCHING	JANS1N4148-1					
DMF5079A	MIXER, MICROWAVE	317943	5	DELTA VF	20 mV	IF = 1 mA	
SD41	SCHOTTKY	2613114-1	5	DELTA VF	+5, -30 mV	IF = 10 A	
SD51	RECTIFIER	2613119-1	5	DELTA VF	+5, -30 mV	IF = 3 A	
UTX225	RECTIFIER	21-504-0005-10W	10	DELTA VF	30 mV	IF = 0.1 A	
				DELTA VF	30 mV	IF = 0.5 A	
2N918	NPN LOW POWER	JANS2N918	1	DELTA (1/HFE)	.022	VCE =12.5 V,IC =100 uA NOTE 1	
				DELTA (1/HFE)	0.011	VCE =12.5 V,IC =500 uA	
				DELTA (1/HFE)	0.0081	VCE = 12.5 V,IC = 1 mA	
				DELTA (1/HFE)	0.0052	VCE = 12.5 V,IC = 3 mA	
				DELTA (1/HFE)	0.0039	VCE = 12.5 V,IC = 5 mA	
				DELTA (1/HFE)	0.0033	VCE =12.5 V, IC =10 mA	
			5	DELTA (1/HFE)	0.056	VCE =12.5 V,IC =100 uA	
				DELTA (1/HFE)	0.028	VCE =12.5 V,IC =500 uA	
				DELTA (1/HFE)	0.021	VCE = 12.5 V,IC = 1 mA	
				DELTA (1/HFE)	0.015	VCE = 12.5 V,IC = 3 mA	
				DELTA (1/HFE)	0.011	VCE = 12.5 V,IC = 5 mA	
				DELTA (1/HFE)	0.0088	VCE =12.5 V, IC =10 mA	
				DELTA (1/HFE)	0.01	VCE = 5 V, IC = 20 mA	
2N930	NPN LOW POWER	2613184-1					NOT USED IN ORBIT
2N2219A	NPN LOW POWER	5961012353276	1	DELTA (1/HFE)	0.02	IC = 1 mA, VCE = 10 V	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
				DELTA (1/HFE)	0.01	IC = 10 mA, VCE = 10 V	
				DELTA (1/HFE)	0.01	IC = 150 mA,VCE = 10 V	
				DELTA VCE(SAT)	0.05 V	IC = 1 mA, IB = 0.1 mA	
				DELTA VCE(SAT)	0.05 V	IC = 150 mA,IB = 15 mA	
			5	DELTA (1/HFE)	0.04	IC = 1 mA, VCE = 10 V	
				DELTA (1/HFE)	0.02	IC = 10 mA, VCE = 10 V	
				DELTA (1/HFE)	0.015	IC = 150 mA,VCE = 10 V	
				DELTA VCE(SAT)	0.10 V	IC = 1 mA, IB = 0.1 mA	
				DELTA VCE(SAT)	0.15 V	IC = 150 mA,IB = 15 mA	
2N2219A	NPN LOW POWER	JANS2N2219A					
2N2219A	LOW POWER NPN	JANS2N2219A					
2N2222A	LOW POWER NPN	5961012357784	1	DELTA (1/HFE)	0.02	IC = 1 mA, VCE = 10 V	
				DELTA (1/HFE)	0.01	IC = 10 mA, VCE = 10V	
				DELTA (1/HFE)	0.01	IC = 150 mA,VCE = 10 V	
				DELTA VCE(SAT)	0.05 V	IC = 1 mA, IB = 0.1 mA	
				DELTA VCE(SAT)	0.05V	IC = 150 mA,IB = 15 mA	
			5	DELTA (1/HFE)	0.04	IC = 1 mA, VCE = 10 V	
				DELTA (1/HFE)	0.02	IC = 10 mA, VCE = 10 V	
				DELTA (1/HFE)	0.015	IC = 150 mA,VCE = 10 V	
				DELTA VCE(SAT)	0.10 V	IC = 1 mA, IB = 0.1 mA	
				DELTA VCE(SAT)	0.15 V	IC = 150 mA,IB = 15 mA	
2N2222A	NPN LOW POWER	JANS2N2222A					
2N2222A	NPN LOW POWER	JANS2N2222A					
2N2222A	NPN SWITCHING	49870-9716-S2222					
2N2222A	NPN LOW POWER	JANS2N2222A					
2N2222A	LOW POWER NPN	JANS2N2222A					
2N2222A	NPN,SILICON,SWITCH	JANS2N2222A					
2N2369A	NPN LOW POWER	5961012353277	5	DELTA (1/HFE)	0.025	IC = 10 mA, VCE = 10 V	
				DELTA (1/HFE)	0.05	IC = 1 mA, VCE = 2 V	
				DELTA (1/HFE)	0.12	IC = 0.1 mA, VCE = 2 V	
				DELTA (1/HFE)	0.02	IC = 0.1 A, VCE = 2 V	
				DELTA VCE(SAT)	0.15 V	IC = 10 mA, IB = 1 mA	
2N2369A	NPN LOW POWER	49870-9716-S2369					
2N2432A	NPN LOW POWER	5961012352198	5	DELTA (1/HFE)	0.9	IC = 0.1 mA,VCE = 10 V	DATA FOR TI PART
				DELTA (1/HFE)	0.16	IC = 1 mA	
				DELTA (1/HFE)	0.024	IC = 10 mA	
2N2432A	NPN LOW POWER	JANS2N2432A					
2N2432A	NPN LOW POWER	5961012352198					

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
2N2484	NPN LOW POWER	2613180-2	5	DELTA (1/HFE)	0.014	IC = 1 mA, VCE = 10 V	
				DELTA (1/HFE)	0.018	IC = 0.5 mA,VCE = 10 V	
				DELTA (1/HFE)	0.006	IC = 10 mA, VCE = 10 V	
2N2605	PNP LOW POWER	JANS2N2605	2.5	DELTA (1/HFE)	0.015	IC = 1 mA, VCE = 2 V	
2N2658	NPN	2613190-1	5	DELTA (1/HFE)	0.10	IC = 20 mA, VCE = 2 V	
				DELTA (1/HFE)	0.03	IC = 200 mA, VCE = 2 V	
				DELTA (1/HFE)	0.02	IC = 500 mA, VCE = 2 V	
2N2658	NPN POWER	78324-1					
2N2880	NPN POWER	JANTXV2N2880	5	DELTA (1/HFE)	0.045	IC = 1 A, VCE = 5 V	
			1	DELTA (1/HFE)	0.01	IC = 1 A, VCE = 5 V	
			6	DELTA (1/HFE)	0.05	IC = 1 mA, VCE = 4 V	
				DELTA (1/HFE)	0.03	IC = 10 mA, VCE = 4 V	
				DELTA (1/HFE)	0.005	IC = 100 mA, VCE = 4 V	
				ICBO	60 nA	VCE = 10 V	
2N2905A	PNP LOW POWER	5961012352200	1	DELTA (1/HFE)	0.03	IC = 1 mA, VCE = -10 V	
				DELTA (1/HFE)	0.02	IC = 1 mA, VCE = -10 V	
				DELTA (1/HFE)	0.01	IC = 150 mA,VCE =-10V	
				DELTA VCE(SAT)	0.10 V	IC = 150 mA,IB = 15 mA	
			5	DELTA (1/HFE)	0.05	IC = 1 mA, VCE = -10 V	
				DELTA (1/HFE)	0.03	IC = 10 mA, VCE =-10 V	
				DELTA (1/HFE)	0.02	IC = 150 mA, VCE =10 V	
				DELTA (1/HFE)	0.15V	IC = 150 mA,IB = 15 mA	
2N2905A	LOW POWER PNP	JANS2N2905A					
2N2907A	PNP LOW POWER	5961012357785	1	DELTA (1/HFE)	0.03	IC = 1 mA, VCE = -10 V	
				DELTA (1/HFE)	0.02	IC = 10 mA,VCE = -10 V	
				DELTA (1/HFE)	0.01	IC =150 mA,VCE = -10 V	
				DELTA VCE(SAT)	0.10 V	IC = 150 mA,IB = 15 mA	
			5	DELTA (1/HFE)	0.2	IC = 0.01 mA,VCE =10 V	
				DELTA (1/HFE)	0.1	IC = 0.1 mA,VCE =-10 V	
				DELTA (1/HFE)	0.05	IC = 1 mA, VCE = -10 V	
				DELTA (1/HFE)	0.03	IC = 10 mA,VCE = -10 V	
				DELTA (1/HFE)	0.02	IC = 150 mA,VCE =-10 V	
				DELTA VCE(SAT)	0.15 V	IC = 150 mA,IB = 15 mA	
2N2907A	PNP LOW POWER	JANS2N2907A					
2N2907A	PNP LOW POWER	JANS2N2907A					
2N2907A	PNP SWITCHING	JANS2N2907A					
2N2907A	LOW POWER PNP	JANS2N2907A					
2N2920	DUAL NPN	5961012353306	5	DELTA (1/HFE)	0.06	IC = 0.1 mA,VCE = 10 V	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
				DELTA (1/HFE)	0.01	IC = 10 mA, VCE = 10 V	
				DELTA (1/HFE)	0.02	IC = 1 mA, VCE = 10 V	
				DELTA (1/HFE)	0.04	IC = 1 mA, VCE = 1 V	
				DELTA (1/HFE)	0.06	IC = 0.5 mA, VCE = 1 V	
2N2920	NPN DUAL	JANS2N2920					
2N2920	DUAL NPN	JANS2N2920					
2N2946A	PNP CHOPPER	2613180-5	5	DELTA (1/HFE)	0.05	IC = 0.1 mA, VCE = 20V	
				DELTA (1/HFE)	0.03	IC = 1 mA, VCE = 20 V	
				DELTA (1/HFE)	0.02	IC = 10 mA, VCE = 20 V	
2N3251A	PNP SWITCHING	2613180-6	5	DELTA (1/HFE)	0.045	IC = 1 mA, VCE = 10 V	
2N3251A	NPN LOW POWER	49870-9716-3251A					
2N3386	JFET TO-72	2613189-1	5	IGSS	1 uA	VGS = 30 V	
2N3421	NPN POWER	49870-9716-3421	5	DELTA (1/HFE)	0.08	IC = 3 mA, VCE = 2 V	
				DELTA (1/HFE)	0.04	IC = 30 mA, VCE = 2 V	
				DELTA (1/HFE)	0.02	IC = 300 mA, VCE = 2 V	
2N3467	PNP LOW POWER	2613180-7	5	DELTA (1/HFE)	0.03	IC = 0.1 A, VCE = 1 V	
				DELTA (1/HFE)	0.02	IC = 0.35 A, VCE = 1 V	
				DELTA (1/HFE)	0.02	IC = 0.6 A, VCE = 1 V	
				DELTA (1/HFE)	0.15	IC = 0.5 mA, VCE = 1 V	
				DELTA (1/HFE)	0.12	IC = 1 mA, VCE = 1 V	
				DELTA (1/HFE)	0.1	IC = 10 mA, VCE = 1 V	
				DELTA (1/HFE)	0.04	IC = 50 mA, VCE = 1 V	
				DELTA (1/HFE)	0.07	IC = 1 A, VCE = 1 V	
				DELTA VCE(SAT)	0.10 V	IC = 200 mA,IB = 40 mA	
				DELTA VCE(SAT)	0.15 V	IC = 0.1 A, IB = 10 mA	
				DELTA VCE(SAT)	0.15	IC = 0.6 A, IB = 40 mA	
2N3499L	NPN LOW POWER	JANS2N3499L	1	DELTA (1/HFE)	0.013	VCE = 10 V,IC = 150 mA	
				DELTA (1/HFE)	0.098	VCE = 10 V, IC = 1 mA	
			5	DELTA (1/HFE)	0.027	VCE = 10 V,IC = 150 mA	
				DELTA (1/HFE)	0.20	VCE = 10 V, IC = 1 mA	
2N3501	NPN LOW POWER	JANS2N3501L	5	DELTA (1/HFE)	0.05	IC = 10 mA, VCE = 10 V	
				DELTA (1/HFE)	0.02	IC = 0.15 A,VCE = 10 V	
				DELTA VCE(SAT)	0.15 V	IC =0.15 A, IB =0.015A	
2N3501	NPN LOW POWER	JANS2N3501					
2N3501	NPN LOW POWER	JANS2N3501					
2N3501	LOW POWER NPN	JANS2N3501L					
2N3553	RF NPN	2613180-10	5	DELTA (1/HFE)	0.07	IC = 20 mA, VCE = 12 V	
			1	DELTA (1/HFE)	0.03	IC = 20 mA, VCE = 12 V	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
2N3637	LOW POWER PNP	34050986-001	5	DELTA (1/HFE)	0.035	IC = 1 mA, VCE = 10 V	
2N3741	PNP HIGH POWER	2613180-11	6	DELTA (1/HFE)	0.21	IC = 10 mA, VCE = 1 V	Incl. bulk.damage since ft = 4 MHZ.
				DELTA (1/HFE)	0.16	30 mA	
				DELTA (1/HFE)	0.11	100 mA	
				DELTA (1/HFE)	0.075	0.3 A	
				DELTA (1/HFE)	0.11	1 A	
2N3752	NPN POWER	2613185-1	5	DELTA (1/HFE)	0.04	IC = 1 A, VCE = 1 V	
2N3811	DUAL PNP	5961012352227	5	DELTA (1/HFE)	0.11	IC = 1 uA, VCE = 1 V	
				DELTA (1/HFE)	0.025	IC = 10 uA, VCE = 1 V	
				DELTA (1/HFE)	0.01	IC = 0.1 mA, VCE = 1 V	
				DELTA (1/HFE)	0.008	IC = 0.5 mA, VCE = 1 V	
				DELTA (1/HFE)	0.007	IC = 1 mA, VCE = 1 V	
				DELTA (1/HFE)	0.005	IC = 10 mA, VCE = 1 V	
2N3965	PNP LOW POWER	21-134-0008-00W	5	ICBO	30 nA	VCB = 50 V	
				DELTA (1/HFE)	0.05	IC = 1 mA, VCB = 5 V	
2N3965	PNP LOW POWER	21-134-0009-00W					
2N3970	N-CHAN FET	21-313-0001-00W	5	DELTA ID(OFF)	10 nA	VDS = 20 V, VGS = 12 V	
2N3972			5	DELTA ID OFF	10 mA	VDS = 20 V, VGS = 12 V	
2N3997	POWER NPN	34054655-001	1	DELTA (1/HFE)	0.04	IC = 50 mA, VCE = 2 V	
				DELTA (1/HFE)	0.02	IC = 1 A, VCE = 2 V	
				DELTA (1/HFE)	0.02	IC = 5 A, VCE = 5 V	
2N4093	N CHAN JFET	2613180-16	0.5	DELTA ID(OFF)	0.2 nA	VDS = 20 V, VGS = 16 V	
				DELTA IGSS	-0.26 nA	VGS = -20 V	
2N4236	PNP POWER	21-326-0003-00W	5	DELTA (1/HFE)	0.1	IC = 0.25 A, VCE = 1 V	
				DELTA (1/HFE)	0.07	IC = 1 A, VCE = 1 V	
				DELTA VCE(SAT)	0.1 V	IC = 1 A, IB = 0.25 A	
2N4239	NPN POWER	21-327-0004-00W	5	DELTA (1/HFE)	0.03	IC = 2 A, VCE = 5 V	
				DELTA (1/HFE)	0.05	IC = 0.2 A, VCE = 5 V	
2N4393	N-CHAN FET	21-333-0001-	2	DELTA R ON	+ 2 OHMS	VGS = 0, ID = 1 mA	
				DELTA IGSS	-200 nA	VGS = 20 V, VDS = 0 V	
2N4858	N CHAN JFET	2613180-13	0.75	ID(OFF)	0.9 nA	VDS = 9 V, VGS = -9 V	
2N4865	NPN POWER	2613182-1	5	ICBO	0.2 mA	VCB = 10 V	
				IEBO	0.7 mA	VEB = 8 V	
				DELTA (1/HFE)	0.045	IC = 0.5 mA, VCE = 1 V	
				DELTA (1/HFE)	0.014	IC = 7 A	
				DELTA (1/HFE)	0.012	IC = 15 A	
			1	ICBO	30 uA	VCB = 10 V	
				IEBO	80 uA	VEB = 8 V	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
				DELTA (1/HFE)	0.023	IC = 0.5 mA, VCE = 1 V	
				DELTA (1/HFE)	0.007	7 A	
				DELTA (1/HFE)	0.006	15 A	
2N4868A	N-CHAN FET	21-308-0006-00W	5	DELTA IGSS	20 nA	VGS = 30 V	
2N5004	POWER NPN	34069586-001 D	5	DELTA (1/HFE)	0.03	IC = 0.1 A, VCE = 5 V	
				DELTA (1/HFE)	0.02	IC = 1.5 A, VCE = 5 V	
				DELTA VCE(SAT)	150 mV	IC = 1.5 mA,IB =0.15 A	
2N5005	PNP POWER	2613181-2	5	DELTA (1/HFE)	0.04	IC = 0.1 A, VCE = 10 V	
				DELTA (1/HFE)	0.03	IC = 1 A, VCE = 5 V	
				DELTA (1/HFE)	0.13	IC = 1 mA, VCE = 1 V	
				DELTA (1/HFE)	0.05	IC = 30 mA, VCE = 1 V	
				DELTA (1/HFE)	0.04	IC = 2.5 A, VCE = 1 V	
				DELTA VCE(SAT)	0.15 V	IC = 0.1 A,IB = 0.01 A	
				DELTA VCE(SAT)	0.15 V	IC = 1 A, IB = 0.1 A	
2N5005	POWER NPN	34069587-001 E					
2N5042	PNP LOW POWER	2613188-1	5	DELTA (1/HFE)	0.025	IC = 50 mA, VCE = 1 V	
				DELTA (1/HFE)	0.08	IC = 6 mA, VCE = 1 V	
				ICBO	-16 nA	VCB = 30 V	
2N5114	P CHANNEL JFET	2613180-18	5	DELTA VGS(OFF)	2 V	ID = 10 nA	
				DELTA RDS(ON)	30 OHMS	ID = 1 mA	
2N5116	P CHAN JFET	2613180-14	1	VGS(OFF)	3.2 V	ID = 10 nA	BIAS:VDS = -10 V,VGS = 10 V; Derating for Siliconix (Vendor 2).
				RDS(ON)	155 OHMS	ID = -100 uA	
			5	VGS(OFF)	3.3 V	ID = 10 nA	
				RDS(ON)	155 OHMS	ID = -100 uA	
2N5196	DUAL JFET	34054657-002 J	1	ICSS	50 nA	VGS = 30 V, VDS = 0 V	
				DELTA VGSS	-0.2 V, -3.823 V	VDS = 20 V,ID = 200 mA	
				VGS1 - VGS2	10 mV	VDG=20 VDC,ID= 200uADC	
				IDSS	0.56 mA, 7.22 mA	VDS = 20 V, VGS - 0 V	
				IDSS1 / IDSS2	1 + 8 %, - 13 %	VDS = 20 V, VGS = 0 V	
2N5330	NPN HIGH POWER	2613186-1	2.5	DELTA (1/HFE)	0.02	IC = 1 A, VCE = 5 V	
			1	VCE(SAT)	0.8	IC = 15 A	
				DELTA (1/HFE)	0.0028	VCE = 1 V, IC = 7 A	
				DELTA (1/HFE)	0.0071	VCE = 1 V, IC = 15 A	
			5	VCE(SAT)	0.8	IC = 15 A	
				DELTA (1/HFE)	0.0033	VCE = 1 V, IC = 7 A	
				DELTA (1/HFE)	0.008	VCE = 1 V, IC = 15 A	
2N5680	PNP HIGH POWER	2613187-1	5	DELTA (1/HFE)	0.03	IC = 0.05 A, VCE = 2 V	
				DELTA (1/HFE)	0.03	IC = 1 A, VCE = 2 V	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
				DELTA VCE(SAT)	0.1 V	IC = 1 A, IB = 0.2 A	
2N5796	PNP LOW POWER	2613180-15	5	DELTA (1/HFE)	0.08	IC = 0.17 mA,VCE = 1 V	
2N6301	NPN DARLINGTON	49870-9716-6301	5	DELTA (1/HFE)	0.03	IC= 3A,VCE= 3V,F= 1KHZ	
				ICEO	2 mA	VCE = 40 V, IB = 0	
2N6796	POWER	2613180-17	0.25	VGS(TH)	0.79	1.3 V MIN	Degradation critically depends upon application.
				IDSS	-150 nA	VDS = 50 V, VGS = 0 V	
NE21908B	MICROWAVE	PS0261 B	5	DELTA POWER GAIN	0.4 dB	IC = 20 mA	
NE21908B	MICROWAVE	2593363-1					
NE73408B	MICROWAVE	PS0262 B	5	DELTA (1/HFE)	0.01	IB = 0.1 mA, VCE = 4 V	
NE73408B	MICROWAVE	2593361-1					
PVB42004X	MICROWAVE NPN	2624200-1	5	DELTA (1/HFE)	0.01	IC = 10 mA	
QXTR6911	MICROWAVE	317843	5	DELTA 1/HFE	0.03	IC = 10 mA	
SDT-8154	NPN POWER TO-61I	2613193-1	1	DELTA (1/HFE)	0.004	IC= 10 mA, VCE= 14.2 V	
				DELTA VCE(SAT)	10 mV	IC = 10 A, IB = A	
			5	DELTA (1/HFE)	0.008	IC = 50 mA, VCE = 5 V	
				DELTA (1/HFE)	0.005	IC = 1 A	
				DELTA (1/HFE)	0.01	IC = 10 mA	
TRW54101	MOSFET, P-CHANNEL	3261218-1	5	DELTA (1/HFE)	0.03	VCE = 5 V, IC = 100 mA	
098159R0007ABM	IC, OP AMP	071438-000-001					OP-07 DERATINGS
82S191	2KX8 BIPOLAR PROM	2593953-1	5	DELTA VOL	0.1 V	VCC = 4.5 V,IOL = 8 mA	
82S191	2KX8-BIT BPLR PRM	2613174-1001					
82S191	2KX8-BIT BPLR PRM	2613174-1002					
82S191	2KX8-BIT BPLR PRM	2613174-1003					
82S191	2KX8-BT BPLR PROM	JM38510/21002SJA					
94244	2-BIT ADDER,CMOS	2613170-1	1	ALL	NEGLIGIBLE		NOTE 3
98773	MAC GUA, CMOS SOS	2303073-1	0.5	ALL	NEGLIGIBLE		NOTE 3
98774	MEC GUA, CMOS SOS	2593412-1	0.5	ALL	NEGLIGIBLE		NOTE 3
98776	256X16-BT SROM,SOS	2303072-11	1	ALL	NEGLIGIBLE		NOTE 3
98777	256X16-BT SROM,SOS	2303072-12	1	ALL	NEGLIGIBLE		NOTE 3
98778	256X16-BT SROM,SOS	2303072-13	1	ALL	NEGLIGIBLE		NOTE 3
98779	256X16-BT SROM,SOS	2303072-14	1	ALL	NEGLIGIBLE		NOTE 3
98780	256X16-BT SROM,SOS	2303072-15	1	ALL	NEGLIGIBLE		NOTE 3
98781	256X16-BT SROM,SOS	2303072-16	1	ALL	NEGLIGIBLE		NOTE 3
98782	256X16-BT SROM,SOS	2303072-17	1	ALL	NEGLIGIBLE		NOTE 3
98783	256X16-BT SROM,SOS	2303072-18	1	ALL	NEGLIGIBLE		NOTE 3
98784	256X16-BT SROM,SOS	2303072-19	1	ALL	NEGLIGIBLE		NOTE 3
98909	4096X1-BT SRAM,SOS	2303067-2	1	T ACCESS	OVER 10 mS		
				FUNCTIONALITY	NO GO		

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
99588	256X16-BT SROM,SOS	2303072-20	1	ALL	NEGLIGIBLE		NOTE 3
AD571SD	10-BIT A/D CONVTR	2593952-1	3	DELTA VOH	-0.16 V		
				DELTA VOL	0.24 V		
				DELTA IOH	-16 mA		
				DELTA IOL	-16 mA		
				DELTA T CONV	12 uS		
				DELTA IIH	28 uA		
				DELTA IIL	-0.8 uA		
				OFFSET	0.5 V		
				OFF ERROR	50 LSB		
				NON LIN	1.3 LSB		
				DELTA IOZH	12 uA		
				DELTA IOZL	6 mA		
AD581TH/883B	10 VOLT PREC REF	2613167-1	1	DELTA VOUT	+/- 10 mV	VSS = 15 V,	
						RLOAD = 5 K	
				DELTA LINE REG	0.001 V	VSS = 15 V,	
						RLOAD = 5 K	
AM26LS31/BFA	QUAD LINE DRIVER	AM26LS31/BFA	5	DELTA VOH	-0.06 V	VCC = 4.5V, IOH = 20mA	
				DELTA VOL	0.02 V	VCC = 4.5mA,IOH = 20mA	
				DELTA IIH	3 uA	VIN = 2.7 V	
				DELTA IIL	-150 uA	VIN = 0.4 V	
				DELTA TP	NEGLIBILE CHANGE		
AM26LS32	4 DIFF LINE RCV	2624495-1	5	DELTA VOH	5 %	VCC=4.5V, DELTA VIN=1V	
				DELTA VOH	5 %	VENABLE = 0.8 V,	
						IOH = -440 uA	
				DELTA VOL	10 %	VCC=4.5V,DELTA VIN=-1V	
				DELTA VOL	10 %	VENABLE= 0.8V,IOL= 4mA	
				IIH	221 uA MAX	VCC= 5.5 V, VIH= 2.7 V	
				IIL	-372 uA MAX	VCC= 5.5 V, VIL= 0.4 V	
				DELTA TPHL	15 %	CL= 50 pF, RL= 2 KOHMS	
				DELTA TPHL	15 %	VCC = 5 V,	
						VIN - VIH = +/- 2 V	
CA3045/1N	TRANSISTOR ARRAY	2613192-1	5	DELTA (1/HFE)	0.015	IC = 0.1 mA, VCE = 1 V	
				DELTA (1/HFE)	0.01	IC = 0.1 mA, VCE = 1 V	
				DELTA (1/HFE)	0.01	IC = 10 mA, VCE = 1 V	
CA3091D	4 QUAD MULTIPLR	2613194-1					NOT USED ON ORBIT
CD4001B	QUAD NOR GATE	JM38510H05252SCX	1	IDD	2.5 uA	18 V	NOTE 2
CD4001BK/MSR	4 2-IN NOR GATE	2606454-0011					

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
CD4001BK/MSR	4 2-IN NOR GATE	2606454-0012					
CD4001UBDMSR	CMOS LOGIC	34050958-101 J					
CD4001UBK/MSR	4 2-IN NOR GATE	2606454-0018					
CD4002	DUAL NOR GATE	49869-9716-4002	1	IDD	2.5 uA	18 V	
CD4002BK/MSR	2 4-IN NOR GATE	2606454-0021					
CD4002UBK/MSR	2 4-IN NOR GATE	2606454-0028					
CD4006B	COS/MOS REGISTER	21-981-4006-01	1	IDD	25 uA	18 V	
CD4007UBK/MSR	2 COMP PAIR INVR	2606454-0071	1	IDD	2.5 uA	18 V	
CD4008BK/MSR	4-BIT ADDER	2606454-0081	1	IDD	25 uA	18 V	
CD4008BK/MSR	4-BIT ADDER	2606454-0083					
CD4008BK/MSR	4-BIT ADDER	2606454-0088					
CD40103BK/MSR	8 STG PST SYN CNTR	2606454-1031	1	IDD	25 uA	18 V	
CD4011BK/MSR	4 2-IN NAND GATE	2606454-0111	1	IDD	2.5 uA	18 V	
CD4011BK/MSR	4 2-IN NAND GATE	2606454-0112					
CD4011UB	COS/MOS GATES	JM38510R05051SCA					
CD4011UBDMSR	CMOS LOGIC	34050959-102 H					
CD4011UBK/MSR	4 2-IN NAND GATE	2606454-0118					
CD4012B	COS/MOS GATES	JM38510R05052SCA	1	IDD	2.5 uA	18 V	
CD4012BK/MSR	2 4-IN NAND GATE	2606454-0121					
CD4012UBDMSR	CMOS LOGIC	34050960-101 H					
CD4012UBK/MSR	2 4-IN NAND GATE	2606454-0128					
CD4013B	COS/MOS FLIP-FLOP	JM38510R05151SCA	1	IDD	7.5 uA	18 V	
CD4013BK/1S	CMOS B	2606454-0132					
CD4013BK/MSR	2 D FLIP-FLOP	2606454-0131					
CD4013BK/MSR	2 D FLIP-FLOP	2606454-0138					
CD4013BKSR	COS/MOS LOGIC	34050970-101					
CD4013BKSR	CMOS LOGIC	JM38510R05151SCA					
CD4015B	COS/MOS REGISTER	21-981-4015-01	1	IDD	25 uA	18 V	
CD4015BDMSR	CMOS LOGIC	JM38510R05753SEA					
CD4015BK/MSR	2 4-BIT ST.RGSTR	2606454-0151					
CD4016BK/MSR	4 BILATRL SWITCH	2606454-0161	1	IDD	2.5 uA	18 V	
CD4016BKMSR	CMOS LOGIC	34050963-102 H					
CD4017BK/MSR	DECADE CNTR/DIVDR	2606454-0171	1	IDD	25 uA	18 V	
CD4018BK/MSR	PRESET DIV N CNTR	2606454-0181	1	IDD	25 uA	18 V	
CD4018BK/MSR	PRESET DIV N CNTR	2606454-0186					
CD4019BFSR	CMOS LOGIC	JM38510R05352SEA	1	IDD	7.5 uA	18 V	
CD4019BK/MSR	2 AND/OR SLT GATE	2606454-0191					
CD4019BK/MSR	4 AND/OR SLT GAT	2606454-0198					

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
CD4019BK/MSR	4 AND/OR SLT GAT	2606454-0199					
CD4019BKIZ	QUAD AND/OR GATE	49869-9716-4019					
CD4021B	COS/MOS COUNTER	JM38510R05754SEA	1	IDD	25 uA	18 V	
CD4021BFSR	CMOS LOGIC	JM38510R05754SEA					
CD4021BK/MSR	8-STAGE ST REGSTR	2606454-0211					
CD4023BK/MSR	3 3-IN NAND GATE	2606454-0231	1	IDD	2.5 uA	18 V	
CD4023BK/MSR	3 3-IN NAND GATE	2606454-0232					
CD4023UBK/MSR	3 3-IN NAND GATE	2606454-0238					
CD4024B	COS/MOS COUNTER	JM38510R05655SCA	1	IDD	25 uA	18 V	
CD4024BDMSR	CMOS LOGIC	JM38510R05655SCA					
CD4024BK/MSR	7-STGE BIN CNTR	2606454-0241					
CD4024BK/MSR	7-STGE BIN CNTR	2606454-0242					
CD40257BK/MSR	4 2/1 LN DATA SLCT	2606454-2571	1	IDD	7.5 uA	18 V	
CD4025BK/MSR	3 3-IN NOR GATE	2606454-0251	1	IDD	2.5 uA	18 V	
CD4025UBK/MSR	3 3-IN NOR GATE	2606454-0258					
CD4027BDMSR	CMOS LOGIC	JM38510R05152SEA	1	IDD	7.5 uA	18 V	
CD4027BK/MSR	2 JK MS FLIP-FLOP	2606454-0271					
CD4027BK/MSR	2 JK MS FLIP-FLOP	2606454-0272					
CD4028BK/MSR	BCD-DECML DECODER	2606454-0281	1	IDD	25 uA	18 V	
CD4028BK/MSR	BCD-DECML DECODER	2606454-0282					
CD4028BK/MSR	BCD-DECML DECODER	2606454-0288					
CD4029BK/MSR	PRESET UP/DN CTR	2606454-0291	1	IDD	25 uA	18 V	
CD4030BDMSR	CMOS LOGIC	34050969-101 H	1	IDD	7.5 uA	18 V	
CD4030BK/MSR	4 EXCLUS-OR GATE	2606454-0301					
CD4030BK/MSR	4 EXCLUS-OR GATE	2606454-0308					
CD4031BDMSR	CMOS LOGIC	JM38510R05755SEA	1	IDD	25 uA	18 V	
CD4031BK/MSR	64-STG ST REGSTR	2606454-0311					
CD4032BK/MSR	3 SERIAL ADDER	2606454-0321	1	IDD	25 uA	18 V	
CD4035BK/MSR	4-STG PAR I/O REG	2606454-0354	1	IDD	25 uA	18 V	
CD4035BK/MSR	4-STG PAR I/O REG	2606454-0356					
CD4041UB	COS/MOS BUFFER	21-981-4041-01	1	IDD	7.5 uA	18 V	
CD4041UBK/MSR	4 TRU/COMP BUFFER	2606454-0411					
CD4041UBK/MSR	4 TRU/COMP BUFFER	2606454-0412					
CD4041UBK/MSR	4 TRU/COMP BUFFER	2606454-0418					
CD4041UBKMSR	CMOS LOGIC	JM38510R05555SCA					
CD4046BK/MSR	UP PHAS-LOCK LOOP	2606454-0461	1	IDD	25 uA	18 V	
CD4047BK/MSR	MONO/ASTBL MULTVB	2606454-0471	1	IDD	25 uA	18 V	
CD4047BK/MSR	MONO/ASTBL MULTVB	2606454-0472					

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
CD4049UBK/MSR	6 BUF/CONV INVERT	2606454-0491	1	IDD	7.5 uA	18 V	
CD4049UBK/MSR	6 BUF/CONV INVERT	2606454-0492					
CD4050BDMSR	CMOS LOGIC	JM38510R05554SEA	1	IDD	7.5 uA	18 V	
CD4050BK/1S	CMOS B	2606454-0502					
CD4050BK/MSR	6 BUF/COMP NONINV	2606454-0501					
CD4050BK/MSR	6 BUF/COMP NONINV	2606454-0502					
CD4050BK/MSR	6 BUF/COMP NONINV	2606454-0503					
CD4050BK/MSR	6 BUF/COMP NONINV	2606454-0504					
CD4051BK/MSR	8-CHANL MUX/DEMUX	2606454-0511	1	IDD	25 uA	18 V	
CD4066BK/MSR	4 BILATERL SWITCH	2606454-0661	1	IDD	2.5 uA	18 V	
CD4069UBKSR	CMOS LOGIC	JM38510R17401SCA	1	IDD	2.5 uA	18 V	
CD4071BK/MSR	4 2-IN OR GATE	2606454-0711	1	IDD	2.5 uA	18 V	
CD4075BK/MSR	3 3-IN OR GATE	2606454-0751	1	IDD	2.5 uA	18 V	
CD4081BFSR	CMOS LOGIC	JM38510R17001SCA	1	IDD	2.5 uA	18 V	
CD4081BK/MSR	4 2-IN AND GATE	2606454-0811					
CD4502BK/MSR	STRB 6 INV/BUFFER	2606454-5023	1	IDD	7.5 uA	18 V	
CD4508BK/MSR	2 4-BIT LATCH	2606454-5081	1	IDD	25 uA	18 V	
CD4532BK/MSR	8-BIT PROIR ENCDR	2606454-5321	1	IDD	25 uA	18 V	
CD4538BK/MSR	2 PRC MONO MULTVIB	2606454-5381	1	IDD	25 uA	18 V	
CDP1802D	UPRCSR 8-BIT CMOS	2613165-1	1	DELTA TYPICAL PROP. DELAY	100 %	VDD = 5 V	NOTE 4
					30 %	VDD = 10 V	
				DELTA ISS	1 mA	VDD = 10 V	
				DELTA IIH	450 nA	VDD = 12 V, VIN = 12 V	
				DELTA IIL	-450 nA	VIN = 0 V	
				DELTA IZL	-450 nA		
CT840	RELAY DRIVER,HYBRD	2613163-1	5	DELTA IR	9 nA	VIN = -23 VDC	
				DELTA T(OFF)	-1.1 uS	VIN = 0 TO 10 V	50 HZ
G118AL	6 CHAN FET SWITCH	21-926-0001-00W					
GC10881-905	MWV VAR CAPAC	2613123-1	5	ALL	NEGLIGIBLE EFFECT		
GP511AK	8-BIT BIDIR CNVTR	2617281-1	0.5				USE RAD HARD PART BY HARRIS
			1	IDD	5 mA	PER SCD	
				ICC	0.2 mA		
				I(IN) MAX	+/- 60 uA	CMOS TO TTL	
				IOH MIN	-2.5 mR (MAX)	TTL TO CMOS	
				IOL MIN	4.2 mA (MIN)	TTL TO CMOS	
				I(OUT) MAX	-0.5 mA		
				IIL MAX	-0.5 mA		

123

DMSP 5D3/NSUS RADIATION DERATINGS | PAGE: 16 | DATE:01-14-1991

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
				IIH MAX	-0.35 mA		
				DELTA TPHL	40 ns	CMOS TO TTL	
				DELTA TPLH	40 ns	CMOS TO TTL	
HA-2541-8	**WITHDRAWN**	2613161-1					
HI-508A	8-CH MUX	2613162-1		ALL	UNACCEPTABLE		
HS-508ARH	8-CH MUX		1	ID(OFF)	500 nA	VD=10 V; VEN = 0.8 V;	Use HS-500ARH '90 CRT. Rad Hard Process.
HS-508RH						UNUSED INPUTS AT 10 V	
			2	DELTA R ON	40 OHMS	VO = 10 V, IO = 0.1 mA	
				DELTA ID OFF	5 mA	VS = +/-10 V,	
						VD = +/-10 V	
HS-65262RH	16K SRAM, CMOS	2606423-1	2	DELTA IOZ	3 uA	PER SPEC	
				DELTA TAVQV	30 nS	PER SPEC	
				DELTA TSLQV	30 nS	PER SPEC	
				DELTA TAVAX	30 nS	PER SPEC	
JB-830	HALL GENERATOR	2613130-1	5	DELTA VHOC	NO EFFECT		
				DELTA VM	NO EFFECT		
L1A3548	MEU ARA, CMOS LSI	2613183-1					
LF11202D	QUAD JFET SWITCHES	34048608-001	5	DELTA IS (OFF)	10 nA	SW OFF, S=+ 10, D=-10	SHIELD TO RAD LEVEL 0.5
				DELTA ID(OFF)	10 nA	SW OFF, S=+ 10, D=-10	
				DELTA IS(ON) + DELTA ID(ON)	10 nA	SW ON	LEAKAGE
LF11202D	QUAD JFET SWITCHES	34048608-002					
LH0032G	FET OP AMP, HYBRID	2613158-1					
LM101A	OP AMP	M38510/10103SGC					
LM101A	OP AMP	JM38510/10103SGA					
LM101AH	OP AMP	JM38510/10103SGA	1	DELTA VOS	-7.98 mV	VCC=+/-15 V,VIN=+/-1 V	Must be considered highly conservative as most devices improve markedly if allowed to recover under bias.
				DELTA IB+	250 nA		
				DELTA IB-	375 nA		
				DELTA IOS	140 nA		
			1.5	DELTA VOS	-23.5 mV		
				DELTA IB+	450 nA		
				DELTA IB-	630 nA		
				DELTA IOS	250 nA		
LM108A	OP AMP	M38510/10104SGC					
LM108AF	LIN OP AMP	JM38510/10104SHA					
LM108AF	LIN OP AMP	5962012351304					
LM108AF	OP AMP	JM38510/10104SHA					
LM108AH	LIN OP AMP	JM38510/10104SGA	1	DELTA VOS	-0.3 mV		

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
			1.0	DELTA Vos	-0.3 mV		
				DELTA IB+	8.9 nA		
				DELTA IB-	15 nA		
				DELTA IOS	-18 nA		
			1.5	DELTA VOS	-0.85 V mV		
				DELTA IB+	14 nA		
				DELTA IB-	63 nA		
				DELTA IOS	-35 nA		
			2	DELTA VOS	-1.5 V mV		
				DELTA IB+	20 nA		
				DELTA IB-	97 nA		
				DELTA IOS	-57 nA		
LM108AH	LIN OP AMP	5962012351277					
LM108AH	OP AMP	JM38510/10104SGC					
LM108ARH			5	DELTA VOS	0.5 mV	V=+/- 15 V, RS=50 OHMS Rad Hard special part by NSC.	
				DELTA IOS	2 nA	V = +/- 15 V	
				DELTA IB	30 nA	V = +/- 15 V	
				AOL	120 V / mV	V = +/-15 V, RL = 10 K	
LM109	5V REGULATOR	5962012351278	5	VOUT	5 V +/- 5 %	VIN = 10 V, IC = 10 mA LAUNCH USE ONLY	
LM110H	VOLT FOLLOWER	34054650-001	1	DELTA VOS	1.6 mV	VCC = +/-15 V, DELTA VIN = 0 V	
				DELTA I BIAS	-20 nA		
			3	DELTA VOS	2.5 mV		
				DELTA I BIAS	56 nA		
LM110H/883B	VOLT FOLLOWER	34072840-001 A					
LM111H	VOLT COMPARATOR	JM38510/10304SGA	1	DELTA VOS	5 mV	V +/- = 15 V	PRELIM.- MAY NEED TO SWITCH FROM NSC TO PMI
				DELTA IOS	100 nA	V +/- = 15 V	
				DELTA IB	1 uA	V +/- = 15 V	
			5	DELTA VOS	50 mV		PRELIM.- MAY NEED TO SWITCH FROM NSC TO PMI
				DELTA IOS	500 nA		
				DELTA IB	2 uA		
LM111H	VOLT COMPARATOR	5962012351280					
LM111H	VOLT COMPARATOR	JM38510/10304SGA					
LM111H	VOLT COMPARATOR	M38510/10304SGC					
LM111H	OP AMP	49869-9716-S111					
LM111H	VOLT COMPARATOR	JM38510/10304SGA					
LM111H	VOLT COMPARATOR	JM38510/10304SGC					
PM111			1.5	DELTA VOS	0.7 mV		SUBS. FOR LM111 BY NSC
				DELTA IOS	35 nA		

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
				DELTA IB	-60 nA		
				DELTA VOUT LOW	0	IOUT = 50 mA	
				DELTA ICEX	70 uA	VOUT = 50 V	
			6	DELTA VOS	20 mV		
				DELTA IOS	0.7 uA		
				DELTA IB	-0.1 TO +1.0 uA		
				DELTA VOUT LOW	0.08 V	IOUT = 50 mA	
				DELTA ICEX	0.2 mA	VOUT = 50 V	
				DELTA ISINK	-8 mA	VOUT = 0.5 V	
LM117HVH	IC, REG, VOLT	071437-000-001	1	LINE REG.	+/- 30 mV	VIN = 10 -15 V, ILOAD = 100 mA	
				DELTA VOUT	0.21 V	VIN = 10 V, ILOAD = 10 mA	
				DELTA VREF	37.5 mV	VIN = 10 V, ILOAD = 10 mA	
				IADJ	100 uA	VIN = 10 V, ILOAD = 10 mA	
LM118	LIN OP AMP	JM38510/10107SGA	1	DELTA VOS	10 mV	VS = +/- 15 V, RL = 2 KOHMS	
				DELTA IOS	20 nA	VS = +/- 15 V, RL = 2 KOHMS	
				DELTA IB	200 nA	VS = +/- 15 V, RL = 2 KOHMS	
LM118	OP AMP	JM38510/10107SGA					
LM124	QUAD OP AMP	JM38510/11005SCA	2	DELTA IS	4 mA	V = 30 V	
				DELTA VOS	6 mV	V = 30 V	
				DELTA IOS	80 nA	V = 30 V	
				DELTA +/- IB	350 nA	V = 30 V	
				AOL	35 K	V = 30 V	
				CMRR	90 dB	V = 30 V	
			1	DELTA IS	2 mA	V = 30 V	
				DELTA VOS	3 mV	V = 30 V	
				DELTA IOS	40 nA	V = 30 V	
				DELTA +/- IB	200 nA	V = 30 V	
				AOL	50 K	V = 30 V	
				CMRR	100 dB	V = 30 V	
LM124BCC	LIN QUAD OP AMP	5962012351284					
LM139	LIN QUAD COMPTR	5962012351289	1	DELTA VOS	10 mV	VT = 5 V	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
				DELTA IOS	100 nA		
				DELTA IB	400 nA		
			2	SUPPLY CURRENT	2 mA	VT = 5 V, RLOAD = OPEN	
				V OFFSET RS	4.4 mV	VT = 5 V, VO = 1.4 V	
				I(OFFSET)	100 nA	VT = 5 V	
				I(BIAS)	477 nA	VT = 5 V	
				AOL	50 V / mV	VT = 15 V, RLOAD = 15 KOHMS	
				VOUT(LOW)	0.4 V	VT = 5 V,ISINK = 3 mA VIN(DIFF) = -1 VDC	
LM139	QUAD COMP	JM38510/11201SCA					
LM139AF	VOLT AMP	34054653-001					
LM139AJ/883B	VOLT AMP	34072841-001 A					
LM139F	QUAD COMPARATOR	M38510/11201SDA					
LM140LAH-15	IC, REG. VOLT	97020-ESD-103	5	DELTA VOUT	0.1 V	VD = +/-10 V, VIN = 18 - 30 V, IOUT = 0.1 A	
				DELTA IB	-0.6 mA	VD = +/- 10 V, VIN = 18 - 30 V, IOUT = 0.1 A	
				DELTA LINE REG	60 mV	VD = +/- 10 V, VIN = 18 - 30 V, IOUT = 0.1 A	
				DELTA LOAD REG	20 mV	IO = 5 to 100 mA	
				RIP REJ	-12 DB	f = 120 HZ	
LM158AH	DUAL OP AMP	2613157-1	1	DELTA VOS	4.7 mV	VCC = 30 V	
				DELTA IOS	5 nA		
				DELTA IB	30 nA		
LM158AH	DUAL OP AMP	34050978-001					
LM723H	VOLT REGULATOR	5962012351292	5	DELTA VREF	3 %	VIN = 12 V, IC = 1 mA	
				DELTA LINE REG	25 mV	VIN = 12-15V, IL = 1mA	
				DELTA LOAD REG	25 mV	VIN = 12,VIL = 1-50 mA	
LM723H	VOLT REGULATOR	JM38510/10201SIA					
LM741	OP AMP	JM38510/10101SGX	0.75	DELTA VOS	0.4 mV		Input bias strongly affects radiation effects.
				DELTA IB+	14 nA		
				DELTA IB-	25 nA		
				DELTA IOS	10 nA		

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
			1	DELTA AOL	-17 dB	+/-15 V	
				DELTA VOS(abs)	2.4 mV	+/-15 V	
				DELTA IB	200 nA	+/-15 V	
				DELTA IOS(abs)	60 nA	+/-15 V	
			5	DELTA AOL	-40 dB	+/-15 V	OLD DATA,
				DELTA IB	300 nA	+/-15 V	
				DELTA IOS(abs)	150 nA	+/-15 V	
				DELTA VOS(abs)	40 mV	+/-15 V	
LM741	OP AMP	317939					
LM741AH	LIN OP AMP	JM38510/10101SGA					
LM747AH	DUAL OP AMP	JM38510/10102SIA	0.5	DELTA VOS	-10 mV	VCC = +15 V, 0 V; DELTA VIN = 0	Fails between 0.5 and 1.0 rad levels.
				DELTA I(+)BIAS	70 nA		
				DELTA I(-)BIAS	110 nA		
				DELTA I OFFSET	30 nA		
LM747H	DUAL OP AMP	JM38510/10102SIA					
M38510/21002SJA	2KX8-BT BPLR PROM	2613174-1					82S191.
MA42141	MICROWAVE	317844	5	ALL	NEGLIGIBLE EFFECT		
MM54C906	CMOS BUFFER	2613171-1	0.1	ALL	SEE REMARKS3		PARTS BY NSC ARE SOFT. SEE DERATING FOR RAD HARD MICREL PART.
MM54C906	CMOS BUFFER	TBD	5	ALL	10 % CHANGE		MICREL RAD HARD PART
MM70C97	TRI-STATE DRIVER	2613169-1	0.1	ALL	SEE REMARKS3		PARTS BY NSC ARE SOFT. SEE DERATING FOR RAD HARD MICREL PART.
MM70C97	TRI-STATE DRIVER	TBD	5	ALL	10 % CHANGE		MICREL RAD HARD PART
MS556	RF	317944	5	ALL	NEGLIGIBLE EFFECT		
OP-27Z	OP AMP, PREC.	2629568-1	1.5	VOS	72 uV	RS = 50 OHMS	PMI Part
				DELTA IB	1.7 uA		
				IOS	63 nA		
				AOL	1015 V/mV	RL=2 KOHMS, VO=+/-10 V	
			3.0	DELTA IB	3000 nA		
				IOS	150 nA		
				VOS	0.15 mV		
			6	VOS	80 uV	RS = 50 OHMS	
				DELTA IB	3.5 uA		
				IOS	540 nA		
				AOL	500 V/mV	RL=2 KOHMS, VO=+/-10 V	
OP-02AJ	OP AMP		5	DELTA VOS	0.8 mV	50 OHMS	LM741 Substitute
				IB	140 nA		
				DELTA IOS	5 nA		
				AOL	25 V / mV	2 KOHMS, VO = +/- 10 V	

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
			3	DELTA VOS	0.8 mV		
				IB	120 nA		
				DELTA IOS	2 nA		
				AOL	40 V/mV	2 KOHMS, VO = +/- 10 V	
				AOL	200 V/mV	600 OHM, VO = +/- 10 V	
				AOL	100 V/ mV		
OP-14AJ	OP AMP		5	DELTA VOS	2.3 mV	50 OHMS	LM747 Substitute
				IB	80 nA		
				DELTA IOS	6 nA		
				AOL	20 V/mV	2 KOHMS, VO = +/- 10 V	
			3	DELTA VOS	1 mV	50 OHMS	PMI Part
				IB	70 nA		
				DELTA IOS	4.5 nA		
				AOL	25 V/mV		
			1.5	DELTA VOS	0.5 mV	50 OHMS	PMI Part
				IB	50 nA		
				DELTA IOS	2 nA		
				AOL	40 V/mV	2 KOHMS	
OP-07	IC, OP AMP	97020-000-084 B	1.2	DELTA VOS	1 mV	VS = +/- 15 V	
				DELTA IOS	23 nA		
				DELTA IB	80 nA		
				DELTA PSRR	24 uV / V		
				GBWP	-0.2 MHz		
				DELTA SLEWRATE	-0.6 V / uS		
SMP-11AY	AMP, SAMPLE/HOLD	2613200-40					
SMP11AY	S/H AMP	2593954-1	3	DELTA VOS	12 mV		
				DELTA IB	0.25 mA		
				DELTA SLEW	-7 V / uS		
				QTRANS	4.3 NC		
				DELTA IIL	25 uA		
				DELTA IIH	3.3 nA		
				DELTA VDROOP	5.3 V	VIN = +/- 5 V	
				DELTA I DROOP	24 nA	VIN = +/- 5 V	
SN5406J	HEX INVERTER	M38510/00801SCA	5	ALL	NEGLIGIBLE EFFECT		
SN54L00W	QUAD NAND GATE	M38510/02004SDB	5	ALL	NEGLIGIBLE EFFECT		
SN54L00W	QUAD NAND GATE	M38510/02004SDA					
SN54L73W	DUAL FLIP FLOP	M38510/02103BDB	5	ALL	NEGLIGIBLE EFFECT		
SN54L93W	4-BIT COUNTER	M38510/02502SDA	5	ALL	NEGLIGIBLE EFFECT		

GENERIC	DESCRIPTION	PART NUMBER	RAD LEVEL	PARAMETER	DERATING	OPERATING CONDITIONS	REMARKS3
SN54L95W	4-BIT SHIFT REG	M38510/02801SDA	5	ALL	NEGLIGIBLE EFFECT		
SNC5406J	HEX INVERTER	JM38510/00801SCA	5	ALL	NEGLIGIBLE EFFECT		
SNH54LS26W-00	LPSTTL BUFF/DRV OC	M38510/32102SDA	5	ALL	NEGLIGIBLE EFFECT		
TA12702	16K SRAM CMOS/SOS	2613802-1	1	ALL	NOT SPECIFIED		NOT AVAILABLE
TA12702	16K SRAM CMOS/SOS	2613802-2	1	ALL	NOT SPECIFIED		
TA12736	MEU, CMOS SOS LSI	3261412-1		ALL	UNAVAILABLE		NOT AVAILABLE
UA723	VOLTAGE REGULATOR	49869-9716-S723	1	LOAD REG.	0.35 % MAX	VIN = 15 V, ILOAD = 1 mA to 50 mA	
				DELTA VOUT	-0.34 %, +11.1 %	VIN = 15 V, IOUT = 1 mA	
UA741A	OP AMP	49869-9716-S741					
ULS-2804H-883	DARLINGTON ARRAY	2629736-1 C	2	DELTA VCE(SAT)	0.05 V	IC = 35 mA	
				DELTA VCE(SAT)	0.02 V	IC = 212 mA	
				DELTA VCE(SAT)	0.02 V	IC = 359 mA	
				DELTA (1/HFE)	0.005	IC = 30 mA	
				DELTA (1/HFE)	0.003	IC = 200 mA	
TBD	CRYSTAL	3117942	5	DELTA f/f	20 ppm		
TBD	5.12 MHZ CRYSTAL	49835-9716	5	DELTA f	20 HZ		
PUI20	QUARTZ CRYSTAL	PS0258-8, Rev6		DELTA f/f	20 ppm		
PUI20	QUARTZ CRYSTAL	PS0258-9, Rev6					
PUI20	QUARTZ CRYSTAL	PS0258-10, Rev6					
PUI20	QUARTZ CRYSTAL	PS0258-11, Rev6					

NOTE 1

Explanation of DELTA (1/hFE) Calculations

A primary effect of ionizing particulate radiations on bipolar transistors is degradation of forward current gain, hFE. This degradation is dependent upon the initial gain (hFEO), operating point of the transistor and radiation exposure. DELTA (1/hFE) measures the radiation degradation. The hFE of a transistor after exposure to ionizing radiation can be estimated using the following expression:

$$hFE(FINAL) = 1/[1/hFE(Initial) + DELTA\ (1/hFE)]$$

Degraded hFE values should be based on DELTA (1/hFE) values shown for the same collector current value I_C as the application. If no data are available at that I_C, then values for the next lower I_C should be used if I_C is below the preexposure gain peak. If I_C is above the preexposure gain peak, DELTA (1/hFE) values for the next higher I_C should be used. The gain versus I_C relation is generally in vendor catalogs.

NOTE 2

CMOS parts in this CD4000BX/YYR family are sensitive to ionization damage. In addition to the larger quiescent currents (at 18V) shown here, TPLH and TPHL increase as shown below. Also VTN can have a minimum value of 0.3V, VTP can have a maximum value of 2.8V and the delta VT's can be 1.4V maximum. The VT changes may effect non-standard parameters shown in the current Harris Hi-Rel 1990 catalog. When R is replaced by H as the final part number suffix, the part has a nominal Rad level capability of 10 (ten) and the IDD derating is unchanged. IDD values can be assumed as linear with VDD.

	RAD LEVEL			
	1	2.5	5	LOAD
Delta Propagation Delay,	%, compared to typical preradiation value.			
VDD = 5V	20	50	80	<50pF,
VDD = 10V	8	15	25	200Kohm

NOTE 3

Hardness assured by vendor (RCA), per part specification.

NOTE 4

Typical values assumed to be 50% of maximum 25°C value. Tentative and subject to revision.