MODELING OF THE GROUND-TO-SSFMB LINK NETWORKING FEATURES USING SPW

Final Report
NASA/ASEE Summer Faculty Fellowship Program--1993
Johnson Space Center

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Date Submitted:	August 3, 1993
Contract Number:	NGT-44-001-800

ABSTRACT

This report describes the modeling and simulation of the networking features of the Ground-to-Space Station Freedom Manned Base (SSFMB) Link using COMDISCO Signal Processing WorkSystem (SPW). The networking features modeled include the implementation of Consultative Committee for Space Data Systems (CCSDS) protocols in the multiplexing of digitized audio and core data into Virtual Channel Data Units (VCDUs) in the Control Center Complex and the demultiplexing of VCDUs in the onboard Baseband Signal Processor. The emphasis of this work has been placed on techniques for modeling the CCSDS networking features using SPW. The objectives for developing the SPW models are to test the suitability of SPW for modeling networking features and to develop SPW simulation models of the Control Center Complex and Space Station Baseband Signal Processor for use in end-to-end testing of the Ground-to-SSFMB S-band Single Access Forward (SSAF) Link.

INTRODUCTION

The Ground-to-SSFMB Link Networking Features Simulation Model shown in Figure 1 includes the segments of the SSAF link [1] in which networking features of the CCSDS protocol are implemented. Audio data received within the Control Center Complex are formatted into Bitstream Protocol Data Units (BPDUs). Data Management System (DMS) Core Data are received through CCSDS variable-length packets which are multiplexed into a fixed-length Multiplexing Protocol Data Unit (MPDU). In the absence of sufficient core data to complete a MPDU data zone, a fill data CCSDS packet is appended. The Virtual Channel Data Unit (VCDU) Frame Multiplexer receives the BPDUs and MPDUs for insertion into the VCDU data zone which accommodates one BPDU or MPDU. Synchronous audio data receive priority transfer over core data. In the complete SSAF link the VCDUs would be encrypted with the Data Encryption Standard (DES) and Reed-Solomon encoded to form Coded Virtual Channel Data Units (CVCDUs). The CVCDUs would then be scrambled with a pseudorandom noise (PN) sequence to form Channel Access Data Units (CADUs) for transmission to Space Station Freedom. However, since this study primarily concerns the networking features of the SSAF link, the link will be observed immediately after the assembly of VCDUs. At this point, VCDU bit errors are randomly introduced to observe their impact on the proper reconstruction of recovered CCSDS packets and audio data within the Space Station Baseband Signal Processor. The LNA, Transponder, and portions of the Space Station Baseband Signal Processor which perform Frame Sync/Random Sequence Demodulation, Reed-Solomon Decoding, and DES decryption will be bypassed in this analysis which concerns primarily the networking features of the CCSDS protocol as applied to Space Station Freedom.

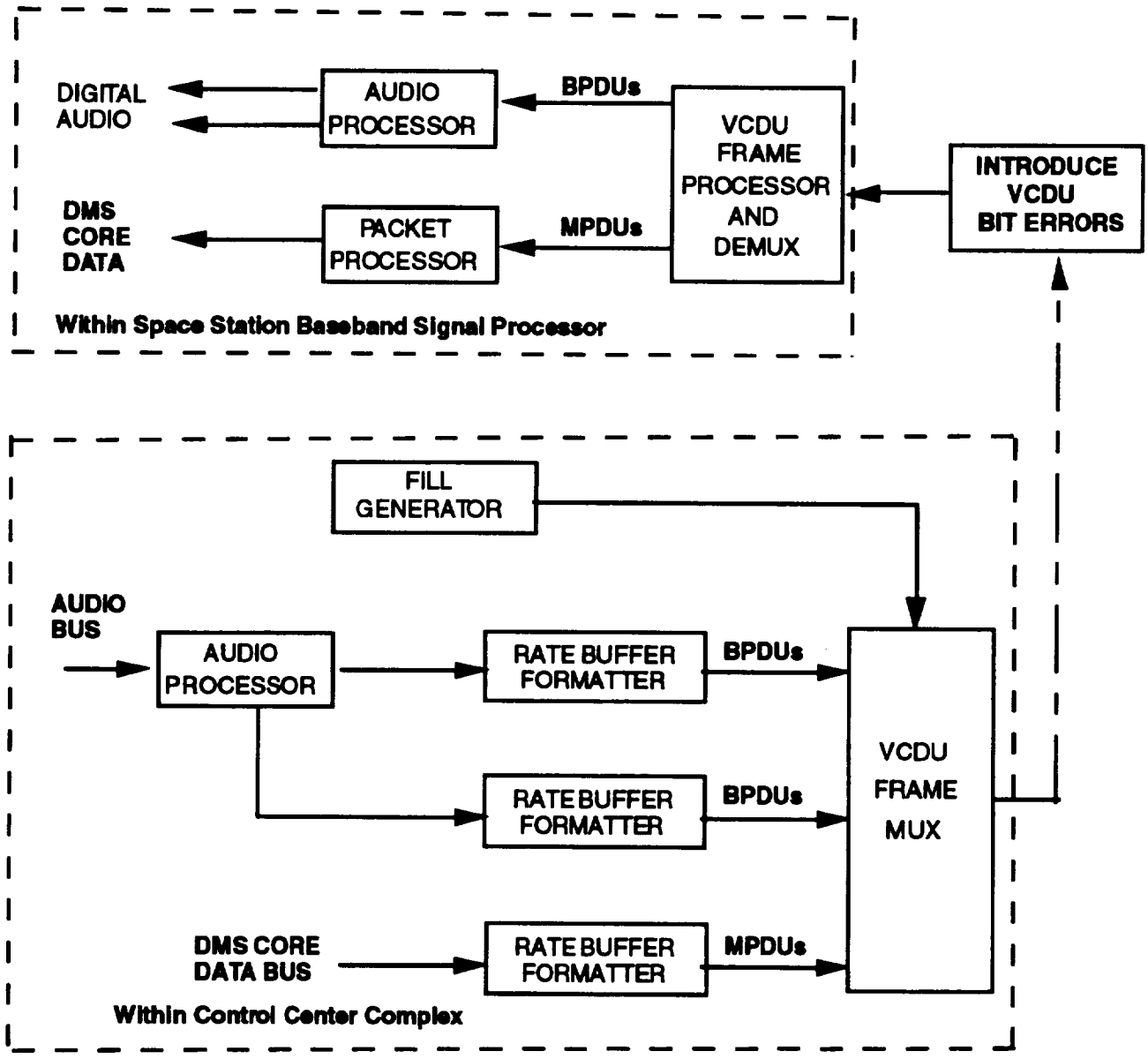

Figure 1. Ground-to-SSFMB Link Networking Features Simulation Model

The VCDUs are received by the VCDU Frame Processor and Demultiplexer where the BPDUs and MPDUs are recovered. The Audio Processor recovers the digital audio data channels from the BPDUs. The Packet Processor recovers the CCSDS packets by reading the CCSDS packet headers to reassemble the variable-length CCSDS packets sent from the Control Center Complex. The Ground-to-SSFMB Link Networking Features Simulation Model shown in Figure 1 was modeled using SPW [2]. SPW is a block-oriented simulator for communication systems. The complete SPW simulation model for the multiplexing and demultiplexing of VCDUs has been described in [3].

SPW Modeling of Networking Features

A primary objective for developing the Ground-to-SSFMB Link Networking Features simulation model was to determine the suitability of COMDISCO Signal Processing WorkSystem (SPW) as a network simulation tool for packet telemetry systems. Major advantages in using SPW are its signal processing capabilities whereby signals can be analyzed and the multi-rate feature which allows processes to operate at different rates during simulation time. For example, the processing rate for a data packet generator can be adjusted so that the packet can be generated within the maximum allowable frame time. When using the multi-rate feature of SPW, care must be taken in generating the required timing signals used to coordinate the various processes used in the simulation model. It can be especially confusing when shifting data between vector and serial forms. SPW appears to have some basic software limitations, however, which must be overcome to develop networking simulation models. Each of these basic limitations will be discussed with suggested techniques for working with the limitation.

SPW Vectors Must Be Fixed-Length

SPW processes data in serial or vector form. SPW vectors used to model transfer frames, protocol data units, and data packets must be fixed-length. The fixed-length vector constraint becomes a problem when attempting to generate the CCSDS variable-length packets which are inserted into the MPDU data zone. For this reason, the CCSDS packet length must be fixed for each CCSDS packet generator modeled in SPW.

Parameters Must Be Deterministic

The parameters used to define SPW block instances cannot be random. For example, in describing a digital data source, the duration of the data transmission cannot be specified as a random variable. This constraint poses a problem in the modeling of random data packet duration and interarrival time. To overcome the deterministic parameter constraint, special modules must be created to provide the necessary statistics for data generation. The Digitized Audio Data Packet Generator is one such module in which a Poisson Impulse Generator, Poisson Random Number Generator, Simple Counter, Comparator, and R-S flip-flop were used to generate digital audio data packets with random data set duration and packet interarrival time.

SPW Library Lacks Basic Functional Modules

Many of the fundamental building blocks for digital systems are omitted in the SPW Library. For example, SPW includes no modules for performing decimal-to-binary conversion and binary-to-decimal conversion. Converters were developed to provide for the generation of CCSDS packet headers and the demultiplexing of CCSDS packet data. SPW does not include shift registers for

sorting through serial data. The Circular Buffer included in the SPW library has a fixed-length vector and does not provide a reset for clearing the buffer. Some of the basic modules for processing vectors were not included in SPW. Modules for performing XOR, AND, OR, and vector switching were exported from COMDISCO to develop the Ground-to-SSFMB link networking SPW simulation model.

Conversion Between SPW Vector and Serial Data Can Be Misleading

Packet telemetry system simulation requires the use of vectors to model transfer frames, protocol data units, and packets. The vectors can be generated by performing a 16-bit scalar to vector conversion using a Scalar Join Vector Block or loading serial data into a Circular Buffer. If a Scalar Join Vector Block is used, the serial-to-vector conversion is accomplished in one simulation iteration. When using a Circular Buffer the length of the Circular Buffer and the data rate of the source loading the buffer must be considered in determining the number of iterations required to convert the serial data to vector data. The timing signal used to drive the Vector Sink Hold pin which allows vector data to be viewed after the completion of the simulation must be synchronized correctly before the vector signal will be displayed. Conversion from serial-to-vector and from vector-to-serial data can introduce phase shifts which make data comparison tricky. For these reasons, the packet telemetry system simulation model uses a vector data representation of the digitized audio and DMS core data. By keeping the Control Center Complex and Baseband Signal Processor digitized audio and core data signals as vector signals, a data comparison can be implemented in the SPW simulation model without compensating for throughput delays.

Ground-to-SSFMB Link Networking Features SPW Model

A SPW simulation model was developed to simulate the networking features of the Ground-to-SSFMB link. The detailed description of the simulation model is described in [3]. The SPW model for simulating the Ground-to-SSFMB Link Networking Features shown in Figure 2 consists of three high-level modules. The SSAF Control Center Complex (ssafccc) module simulates the part of the Control Center Complex which generates VCDUs from digitized audio and DMS core data sources for transmission to Space Station Freedom. The Noise module introduces random bit errors into the VCDU frames. The probability of channel bit error can be adjusted within the Noise module. The SSAF Baseband Signal Processor (ssafbsp) module receives the VCDUs for demultiplexing into audio and DMS core data. The high level modules are linked through the following signals:

vcdu	Virtual Channel Data Unit vector
dms	Data Management System core data vector

audio Digitized audio data vector

ccsdshdr CCSDS header vector

mpduhdr Multiplexing Protocol Data Unit header vector

These vector signals are required to provide an error check of frame, header, and data errors introduced by the Noise source.

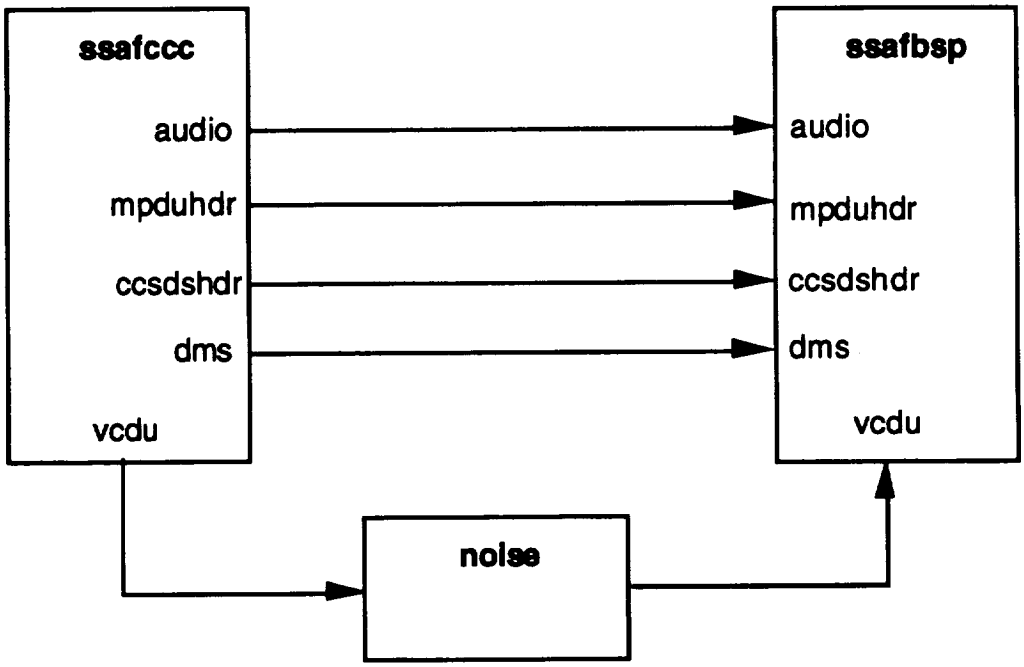

Figure 2. Ground-to-SSFMB Link Networking Features SPW Model

SSAF Control Center Complex SPW Module

The SSAF Control Center Complex SPW module details are shown in Figure 3. Although SPW includes signal generation modules, these modules cannot be set with random variable parameters. The AUDIO module was developed to create a digital data packet generator which has random packet interarrival times and packet length durations. The AUDIO module generates digitized audio data packets which have exponential packet interarrival times and Poisson-distributed packet durations. The BPDUGEN module receives the digitized audio data packets from the AUDIO module and formats them into BPDUs. The DATAFLAG signal in Figure 3 provides a logical true to indicate when audio data are present.

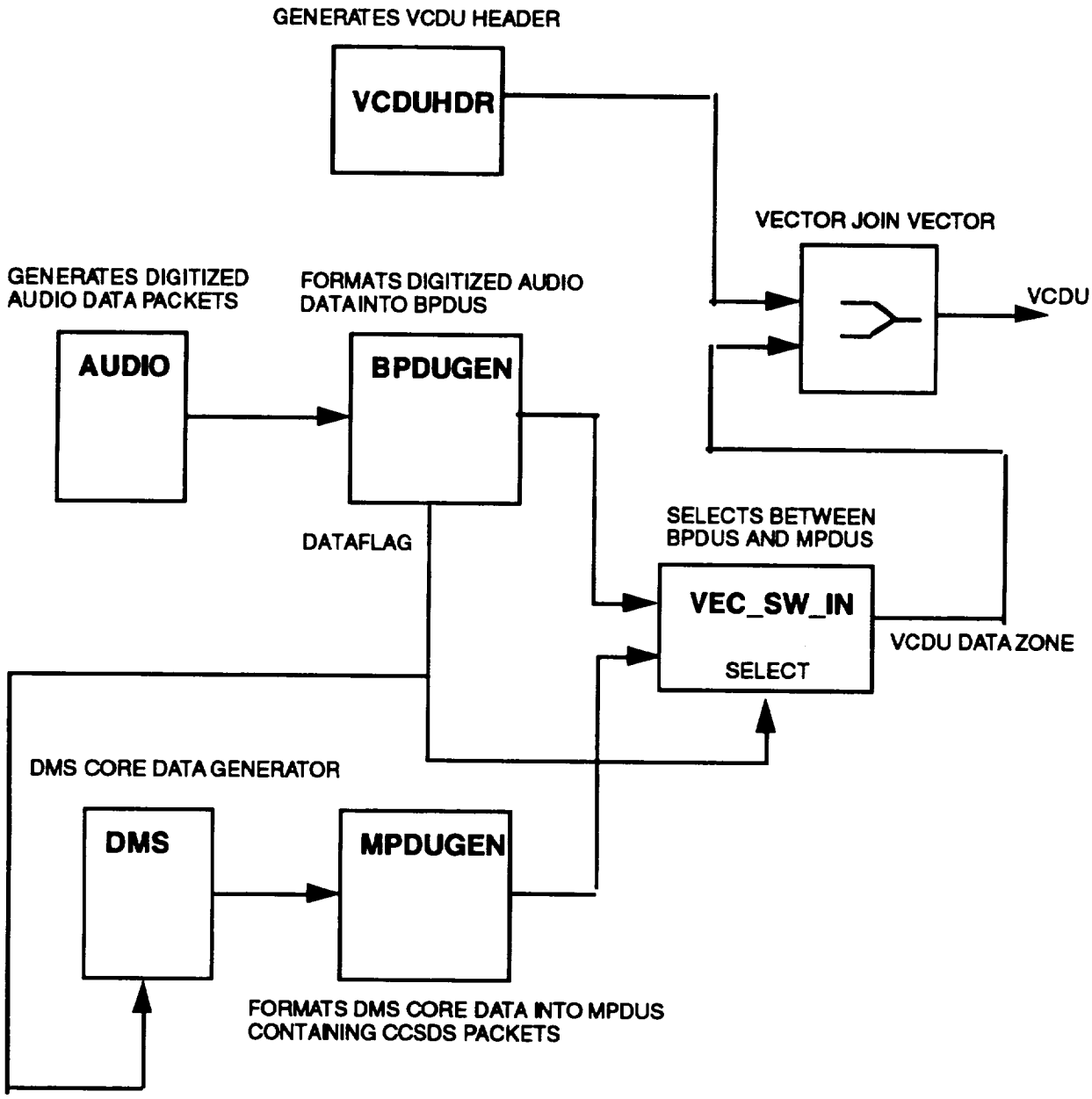

Figure 3. SSAF Control Center Complex Networking Features SPW Module

The DATAFLAG signal drives the BPDU/MPDU Vector Select Switch. BPDUs receive priority transfer over MPDUs since they contain synchronous data. The DMS module generates the Data Management System core data vector to be transferred through the MPDU Generator in the form of CCSDS packets. Conversion of the DMS core data into a vector format provides a data comparison with the recovered DMS core data in the onboard Baseband Signal Processor. The MPDUGEN module inserts the DMS core data into CCSDS

packets. The CCSDS packets are then inserted into the MPDU data zone. Ideally, the MPDUGEN module would generate MPDUs containing variable-length CCSDS packets for transferring the DMS core data. However, the SPW fixed-length vector constraint for SPW block instances complicates the generation of variable-length CCSDS packets. The MPDU Generator module generates MPDUs containing four CCSDS packets. Each CCSDS packet has a 360-bit data field and 48-bit CCSDS packet header for a total CCSDS packet length of 408 bits. Four CCSDS packets complete the 1632-bit MPDU data zone. The MPDUGEN module encodes the Application Process ID, Packet Sequence Number, and Packet Length into CCSDS packet header information. The MPDU and CCSDS headers are provided through output ports to provide header error detection in the onboard Baseband Signal Processor (ssafbsp) module. The Vector Switch-In (VEC_SW_IN) module was exported from COMDISCO to provide vector selection. This module was constructed by COMDISCO and was not part of the SPW library. The Vector Switch-In module selects between a BPDU and MPDU for insertion in the VCDU Data Zone. The VCDUHDR module generates the 48-bit VCDU header and 64-bit VCDU Insert Zone. The VCDU header and Insert Zone were analyzed together in the SPW module since they reside in every SSAF VCDU. This was done to simplify the model although in future models the Crypto Sync code within the VCDU Insert Zone may require analysis separate from the VCDU header. The VCDU header, VCDU Insert Zone, and VCDU Data Zone are combined by the Vector Join Vector block to form the Control Center Complex VCDU.

Noise Module

The Noise Module shown in Figure 4 inserts bit errors into the VCDU Frame by inverting a randomly selected bit. The Random Data Generator in Figure 4 drives the Select signal on the Vector Switch Out block. The Vector Switch Out block either sends the VCDU directly to the Baseband Signal Processor or routes the VCDU through the Extract Component block which removes a randomly selected bit for inversion. The Probability of Zero parameter within the Random Data Generator sets the probability of VCDU frame error. The Noise Generator block in Figure 4 models a Uniform Distribution with limits 0 through 1759 for selecting the index number of the VCDU frame bit to be clobbered. The Insert Component block places the inverted frame bit back into the VCDU.

SSAF Baseband Signal Processor SPW Module

The SSAF Baseband Signal Processor SPW Module shown in Figure 5 models the networking features of the onboard Baseband Signal Processor. The VCDUs from the Control Center Complex are received through the VCDU port of the module. The Vector Split block separates the VCDU Header from the received VCDU. The recovered VCDU Header is compared with a mask of the Control Center Complex VCDU Header. The Vector Compare block, developed by Larry Johnson of Lockheed Engineering and Science Company, provides a logical

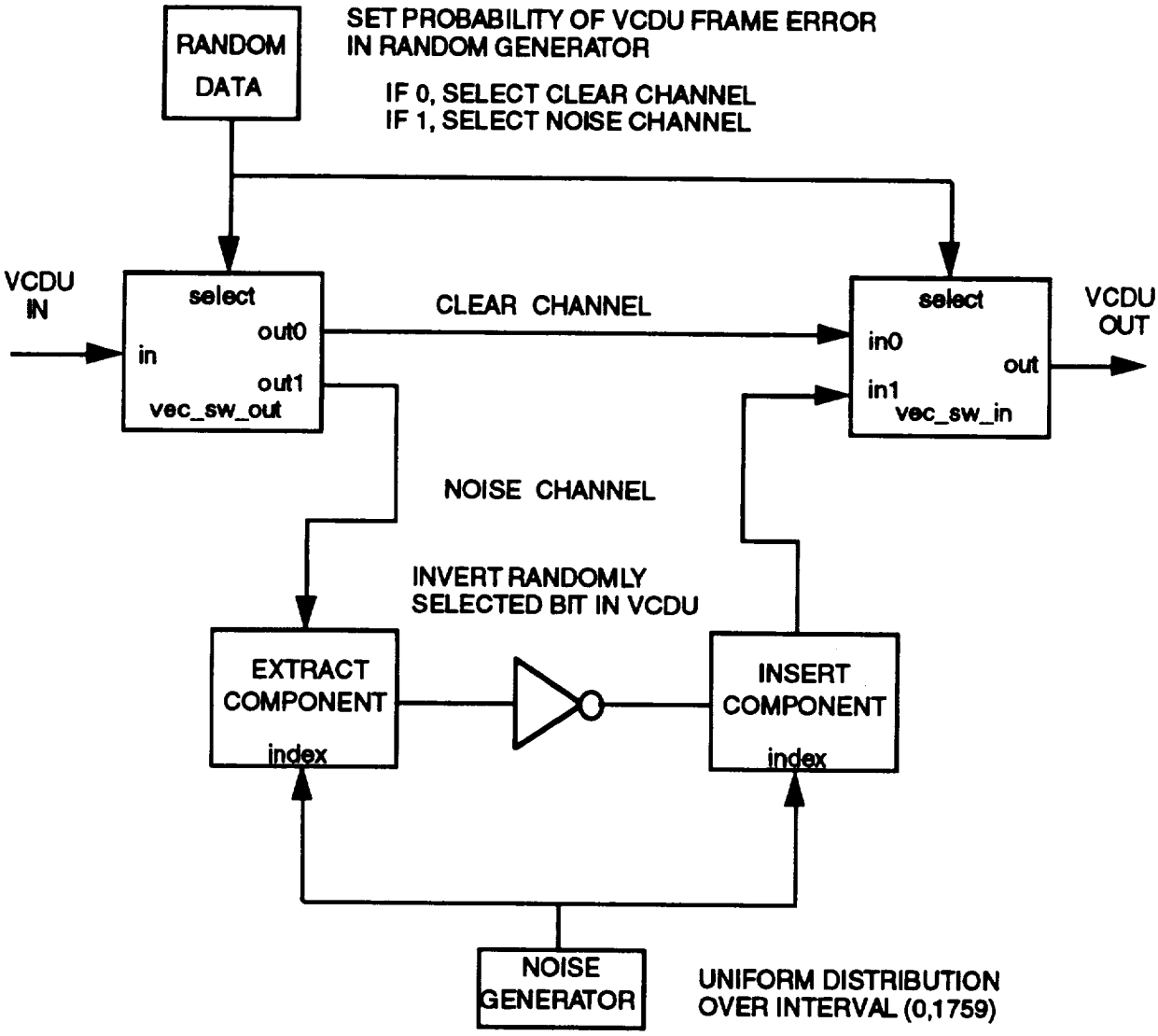

Figure 4. Noise Module

"true" signal output when two input vectors are the same. The signal output of the VCDU Header Vector Compare block (#1) is inverted to provide a VCDU Header error signal. The 1648-bit VCDU Data Zone is removed from the received VCDU at the same time the VCDU Header is removed. The VCDU Data Zone will contain either a BPDU containing digitized audio data or a MPDU containing CCSDS data packets. The VCDU Data Zone is simultaneously tested for a BPDU header and a MPDU header as shown in Figure 5. The BPDU header Vector Compare block (#2) compares the first 16 bits of the VCDU Data Zone with the BPDU Header Mask. The BPDU header has a fixed bit pattern (hexadecimal 3FFF). If the BPDU header Vector Comparator determines that a valid BPDU header is present, then the signal from the Digitized Audio Vector comparator (#3) will be valid. The Digitized Audio Vector comparator tests the

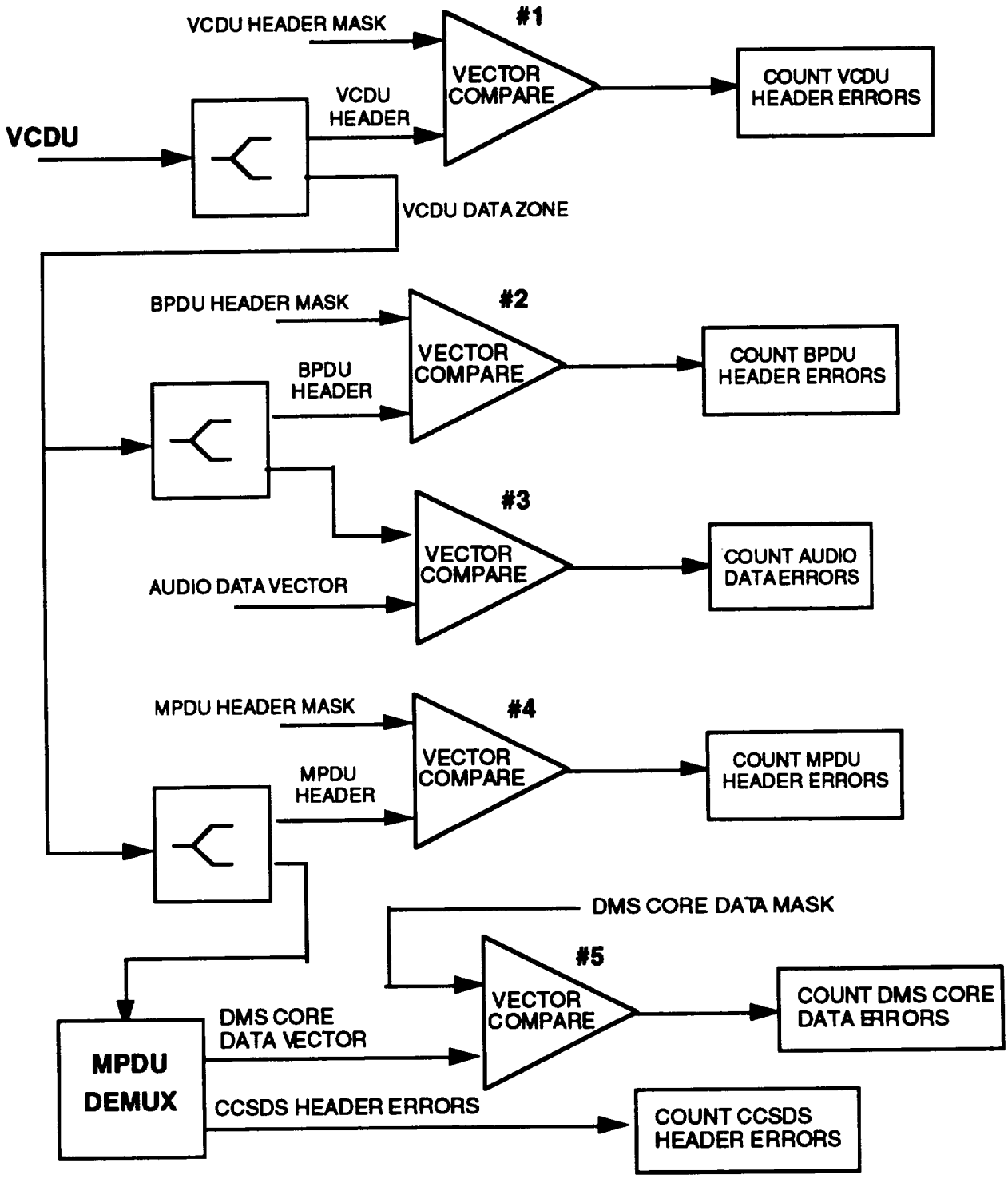

Figure 5. SSAF Baseband Signal Processor SPW Module

BPDU Data Zone with the Control Center Complex digitized audio data vector signal. The BPDU header error signals and Digitized Audio data error signals are recorded using the same procedure used to record VCDU header errors. The MPDU header Vector Compare block (#4) determines whether a valid MPDU header is present in the VCDU Data Zone by comparing the first 16 bits of the VCDU Data Zone with the Control Center Complex MPDU Header vector. If a valid MPDU header is detected, the MPDU Data Zone will be demultiplexed by the MPDU Demultiplexer block. The MPDU Demultiplexer block generates the CCSDS packet header error signal and recovers the DMS core data vector from the MPDU Data Zone. The DMS core data Vector Compare block (#5) compares the recovered DMS core data vector with the Control Center Complex DMS core data vector to determine if bit errors were introduced into the core data. DMS core data errors and CCSDS Header errors are recorded during the simulation. Not shown in Figure 5 are the logical gates required to ensure that a received BPDU will not be recorded as a MPDU header/data error and vice versa.

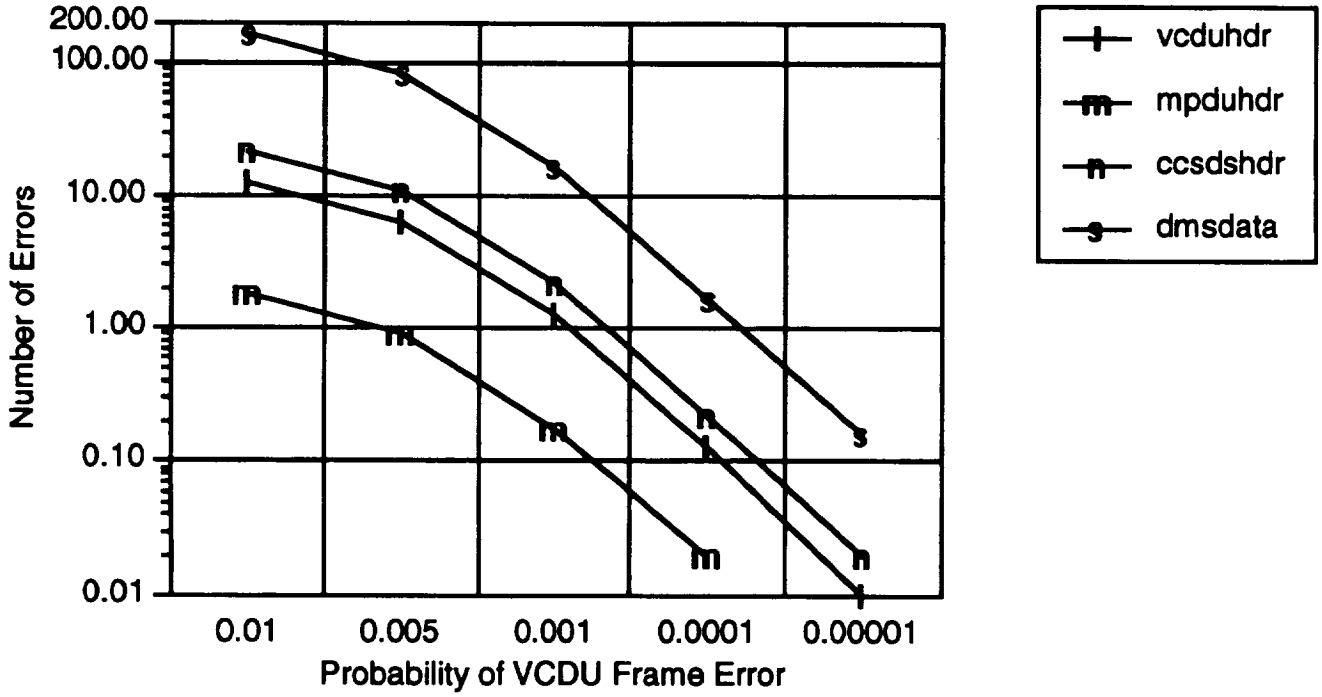

Figure 6. Theoretical Error Performance for MPDU's for 20,000 VCDU Frames

Theoretical Performance

An objective for developing the SPW simulation model for the Ground-to-SSFMB Link was to determine the impact of noise on the recovery of digital audio and core data from the demultiplexed VCDUs in the Baseband Signal Processor. The probability that a header receives a bit error within a VCDU frame increases with

the number of bits in the header. The Theoretical Performance plot shown in Figure 6 displays the expected number of header and data errors over the observation of 20,000 VCDU frames for different VCDU frame error probabilities. The performance plot was developed assuming that one bit error will occur within the 1760-bit VCDU if the VCDU has a frame error. The performance plot in Figure 6 was made for the recovery of MPDU's where each MPDU contains four CCSDS packets transporting DMS core data. A performance plot for BPDU recovery would be similar to Figure 6 except that the number of expected audio data bit errors would differ. The theoretical performance for BPDU and MPDU generation would require defining the percentage of audio data transmission relative to DMS core data transmission.

Simulation Performance

The Ground-to-SSFMB Link SPW Model was simulated for 20,000 VCDU frame generations at different VCDU frame error probabilities to produce the SPW Simulation Performance Plot shown in Figure 7. The Ground-to-SSFMB SPW Simulation Model generates BPDU's whenever audio data packets are received. To observe the generation of MPDU's, the Digitized Audio data generator packet interarrival time within the SPW model was set so that DMS core data transport would dominate to provide a comparison with the Theoretical Performance plot given in Figure 6 for MPDU's. The SPW simulation model records an integer number of errors for the VCDU header, MPDU header, CCSDS packet header,

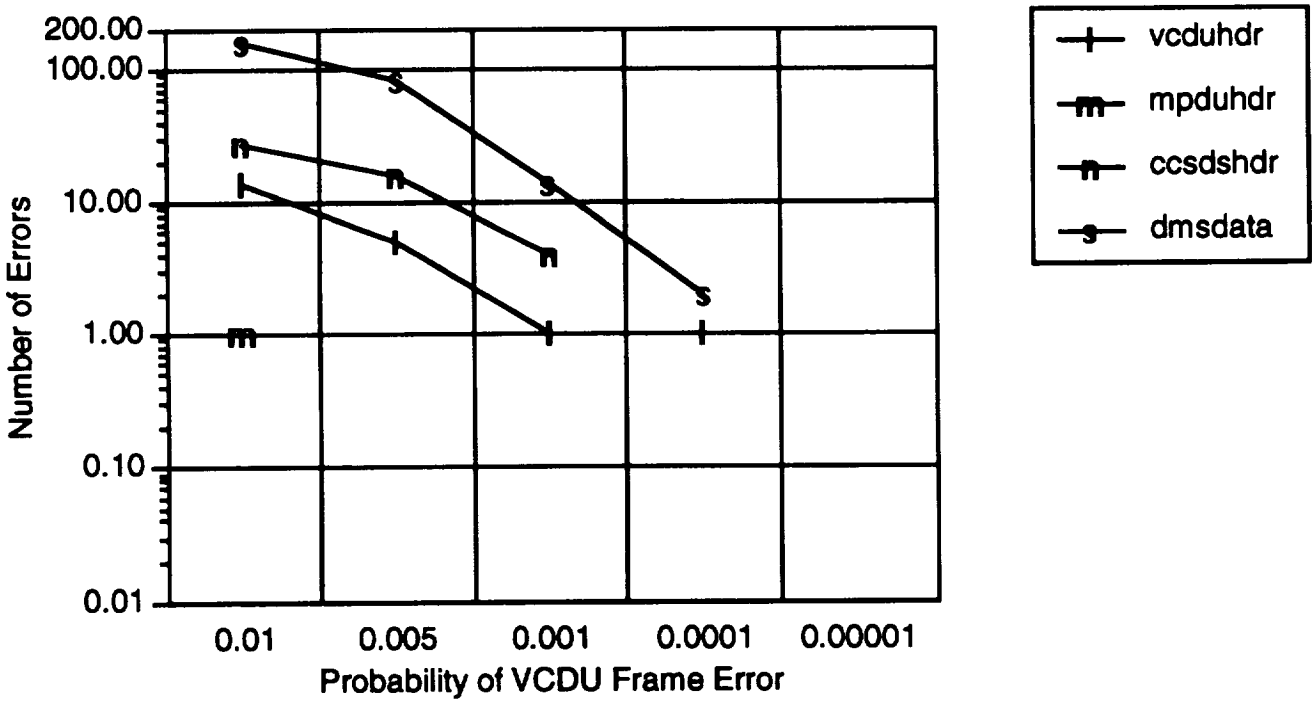

Figure 7. SPW Simulation Error Performance for MPDU's for 20,000 VCDU Frames

and DMS core data error. SPW simulation results agree with the theoretical performance results for an integer number of errors. Longer simulation durations would enable the performance plots to be presented with integer error counts providing a more accurate comparison with the theoretical performance plot for lower VCDU frame error probabilities.

VCDU Frame Simulation Using Delayed Unit Pulse Signals

An alternative method for simulating the networking features of the CCSDS-based packet telemetry system suggested by Karim Alhussiny of Lockheed Engineering and Science Company is to represent packet header and data as unit pulses delayed in time with respect to their appearance in the VCDU. In the delayed unit pulse signal VCDU frame simulation model, each block of header and data information is represented as a unit pulse whose duration is equal in time to the number of bits in the block. For example, in Figure 8, the 48-bit VCDU header has been modeled as a 48-sample unit pulse. The 64-bit VCDU Insert Zone has been modeled as a 64-sample unit pulse delayed 48 samples so that it occurs at the proper time with respect to the VCDU frame. The 16-bit BPDU header has been modeled as a 16-sample unit pulse delayed 112 samples to synchronize the occurence of the BPDU header with the VCDU frame. The unit pulse representation of the VCDU frame blocks models the case in which all bits of each block are set to one. This representation does not reflect variations in VCDU header information, but does provide a method for noise analysis which simulates rapidly. Regardless of how the header bits are initially set, a bit inversion due to noise will have the same impact in terms of performance in the

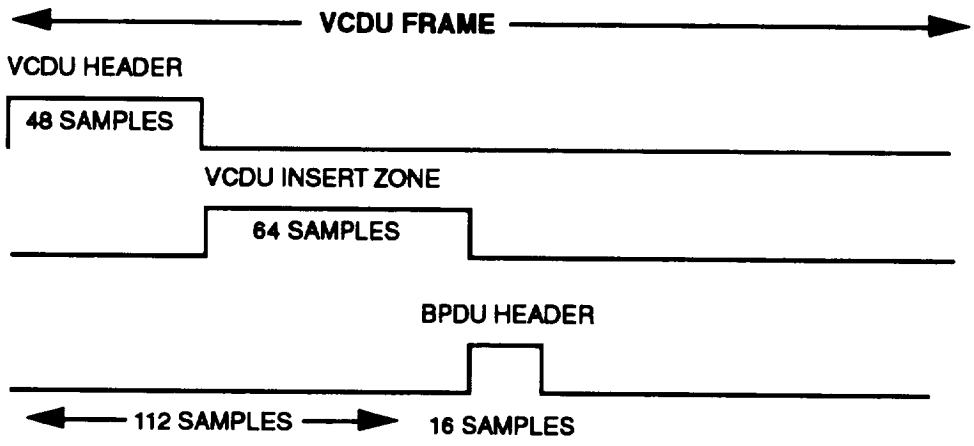

Figure 8. Unit Pulse Representation of VCDU Frame Blocks

presence of noise assuming the header bits do not include a coding scheme. The complete VCDU frame can be modeled as the set of delayed unit pulses ORed together. This generates a unity signal over the 1760 samples contained in the SSAF VCDU. The generated pulses are used to activate HOLD signals on the comparator blocks so that a bit error will not be interpreted over the wrong time

interval for the VCDU block under observation. Ten unit pulse generators are required to generate the VCDU header and Insert Zone (112-bits), MPDU header (16 bits), CCSDS packet headers (48 bits), and CCSDS packet data zones (360 bits). The serial data model was developed to provide a comparison with the vector version of the SPW model for the Ground-to-SSFMB link networking features. The SPW simulation model which decribes the VCDU frame in terms of delayed unit pulses executes very rapidly. The simulation of 20,000 VCDU frames required less than one minute to simulate compared to almost one hour simulation time required for the vector SPW model described earlier in this report. The performance results shown in Figure 9 for the SPW Delayed Unit Pulse Model compare favorably with the theoretical results for VCDU frame errors shown in Figure 6. Although the unit pulse representation of the VCDU frame does not accurately describe header details for signal analysis, it does provide a test for estimating the effect of noise on clobbered VCDU frames without requiring time-intensive simulations. As in the vector SPW model, the Delayed Unit Pulse Simulation model does not represent variable-length CCSDS packets.

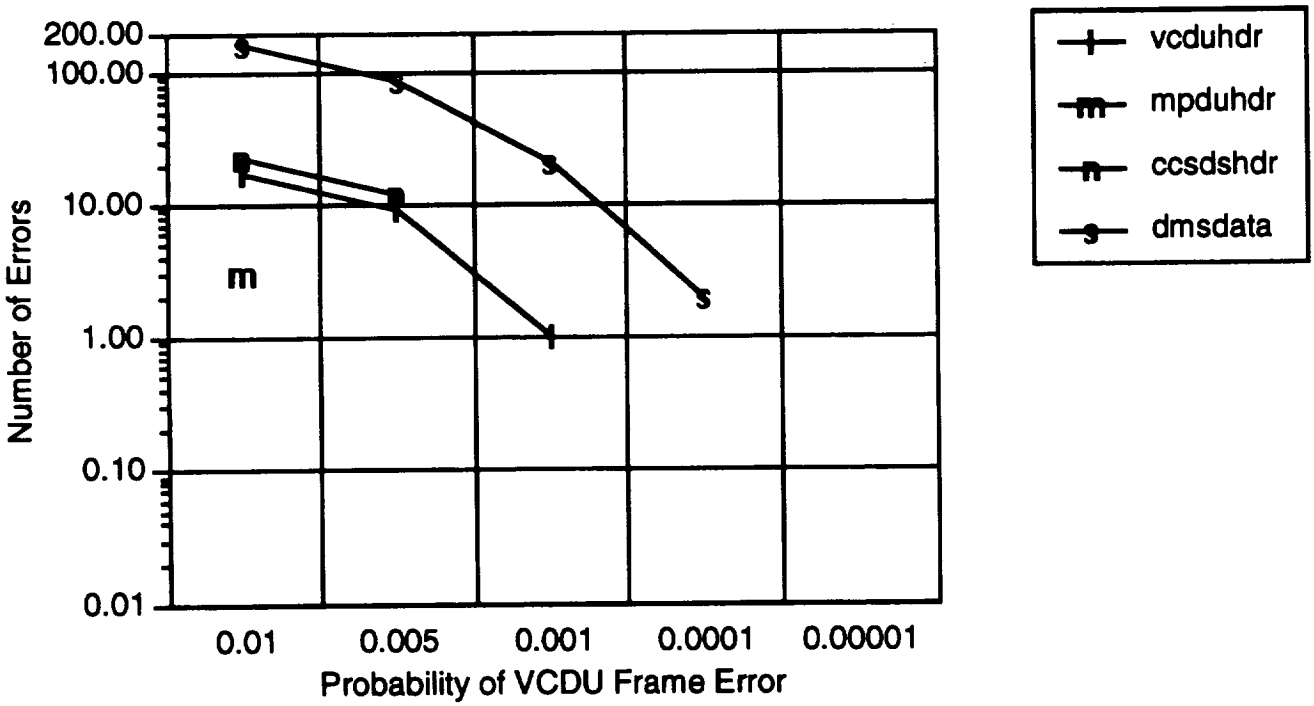

Figure 9. SPW Delayed Unit Pulse Simulation Model Results for 20,000 VCDU Frames

Conclusion

The primary SPW software constraint which must be overcome is the ability to randomly vary the vector lengths so that the generation of variable-length CCSDS data packets can be simulated. The model described in this work assumed the CCSDS data packet generation scenario in which the maximum number of CCSDS packets would be inserted within the MPDU. The effects of channel noise will be paramount whenever the condition of greatest frame overhead occurs, which will be when the CCSDS packets have minimum length. Although the simulation of the SPW model compared well with theoretical performance results, the fixed-length CCSDS packet specification was not the desired design requirement for the SPW model. Ideally, the SPW model would read the CCSDS packet header information within the Baseband Signal Processor to reassemble the segmented data residing in the individual CCSDS packets. Although the SPW model encodes the desired packet header information in binary format, it does not use this information to demultiplex the data once the MPDU has been extracted from the VCDU data zone. The packet header information was not used since the vector length for the data field could not be specified as a variable which could be adjusted by the binary-to-decimal conversion of the packet length field within each CCSDS data packet header. If the SPW fixed-length vector constraint could be circumvented, perhaps through developing specially coded vector block instances, SPW simulation models could be developed which more accurately model the networking features of a CCSDS-based packet telemetry system.

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2. COMDISCO Signal Processing WorkSystem (SPW), Version 3.0, 1992.

3. Ground-to-SSFMB Networking Features SPW Simulation Model, John C. Watson, 1993.