Modeling and Experimental Verification of Single Event Upsets

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OF SINGLE EVENT UPSETS

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Abstract

This paper reviews the research performed and the results obtained at the Laboratory for Radiation Studies, Prairie View A&M University and Texas A&I University, on the problem of Single Events Upsets, the various schemes employed to limit them and the effects they have on the reliability and fault-tolerance at the systems level, such as robotic systems.

Introduction

Random access memory (RAM) based on CMOS technology has gained wide acceptance in space applications [1][2]. It is known that CMOS Static RAMS show an upset sensitivity to single energetic heavy ions including gold, krypton and bromine which is called a single event upset (SEU). Immunity from SEU errors caused by protons or heavy ionizing particles is a requirement for reliable spaceborne integrated circuits. Computer simulation is an important mean to predict, analyze and verify the affects of SEUs on SRAMs. Figure 1a shows the circuit description of a six-transistor SRAM cell which has been used in SEU analyses and computer simulations. When the logic state is set such that node A is biased at Gnd and node B is at V_{dd}, the drain junctions of M1 and M4 are sensitive regions. If an ionizing particle hits the junction of M1, holes will be collected, resulting in a positive voltage spike at node A called the n-hit. Similarly if an ionizing particle hits the junction of M4, electrons will be collected, resulting in a negative voltage spike at node B, called the p-hit. If the voltage spikes are of sufficient amplitude and charge neutrality cannot be established fast enough through the 'ON' transistor, the flip-flop may regenerate and a bit error will occur [2].

Upset rate in CMOS RAMS can be reduced in two ways, either the charge collection capability of the memory can be degraded, or cell design can be altered to require greater critical charge for upset. Diminished coupling between the inverter pair of basic RAM cell decreases the probability of logic upset by slowing the feedback of gate voltage variations. If the gate voltage of the hit inverter remains stable during current impulse, the hit inverter will reestablish its prehit logic state. Maintenance of the hit inverter gate voltage at or near the prehit level is accomplished by maintenance of the voltage at the opposite information node. Thus the upset sensitivity is decreased by increasing the time constant of the feed back paths between the inverters by adding feedback resistors.

Experimental results obtained at the BNL Twin Tandem Van de Graaff Single Event Facility (Figure 1b) are presented for 16K, 64K and 256K Rad Hard Static RAMs(SRAM) [3][4]. Prior total dose radiation (1 MRAD$_{si}$ of 2 MeV protons)

produces imprinting in the Rad Hard SRAM and significantly lowers the SEU LET threshold. In commercial, non-rad hard devices, one would expect a reduction in threshold LET at much lower doses. These results are compared to SPICE models of SRAM with Resistive Feedback to limit Single Event Upsets (SEU). Passive/Active resistance networks, switched capacitor networks for limiting SEU are modeled and compared. The MOS transistor active resistance feedback method of limiting SEU has the advantage that in the absence of Cosmic Ray induced charge, the operation of SRAM is not degraded by high resistance of the active network [6-17].

An extension of this work considers the distribution and dependency of these radiation induced defects to estimate the reliability and fault-tolerance of more complex systems such as A/D converters and CPUs (errors in instruction set and in active logic) [21][22].

BNL Twin Tandem Van de Graaff SEU Test

The beam energy and LET are monitored by four silicon surface-barrier detectors calibrated by an Am-241 alpha source, which makes the energy measurement independent of the information from the accelerator control room. The irradiation chamber contains an adjustable iris aperture and a mobile test board. The effective LET can be varied by rotating the board on the vertical axis to change the particle angle of arrival (Figure 1b). The effective LET is given by:

$$LET_{eff} = \frac{LET}{Cos\theta}$$

where theta is the angle of incidence of ions. A unique feature of the facility is laser optics for accurate device positioning into the beam. A neon laser is placed in the beam line, so that the beam spot can be simulated on the test board by visible light before the experiment. Evacuation and ventilation procedures are fully automated. Device positioning, beam diagnostic, data collection, and data management are computer controlled by user friendly menu driven software. The system specifications are summarized in Table 1.

Table 1. Brookhaven SEU Test Facility
Specifications

Flux	10^1-10^6ions/cm^2/sec
Beam Uniformity	90-98% over 3 in. diameter
Beam Aperture diameter	0.1-1.4 in.
Test board work area	6 by 9 in.
Particle angle of Arrival	0°-73°
Effective LET in Si	1.4-280 MeV cm^2/mg
Cost	$520/h
	$420/h for exempt users

Radiation Hard Technology

The devices were fabricated by AT&T-Bell Laboratories CMOS Twin-Tub IV [4] "1.25um" Rad-Hard technology. As the density of SRAM increases from 16K to 64K and 256K, decrease in lateral dimensions results in lower critical charge due to lower gate and junction capacitances. In order to compensate for this increase in SEU susceptibility, the following process modifications were made;
1) Oxide thickness was reduced and doping density was raised to increase specific capacitances.
2) A twin-Tub process on thin epitaxial substrates reduced the charge collection by cutting off the funnel.
3) Feedback polysilicon resistors were used to reduce the SEU rate by

longer decoupling times for the two inverters.

In addition, radiation hardened gate oxide minimized threshold voltage shifts and transconductance degradation, radiation hardened field oxide eliminated parasitic leakage currents, and modified light doped drain (LDD) N-channel transistors minimized hot carrier effects.

A "2um" design rule 16K, and three "1.25um" design rule (a 64K , a 256K and a 32K x 8) were available for our experiments. The feedback resistor values at room temperature were 82, 109, 151, and 240 Kohms for the "2um" SRAM and 520 ND 670 Kohms for "1.25um" SRAMS. Other important processing and design parameters are given in Table 2.

Table 2. Processing and design parameters

	"2 um"	"1.25 um"
Channel width/length [um]		
NMOS	5.0/2.0	1.50/1.25
PMOS	4.25/2.0	1.75/1.50
Drain area [um^2]		
NMOS	50.3	8.9;7.0
PMOS	25.5	4.3;5.4
Gate oxide thickness [A]	215	240
Epitaxial thickness [um]	1.7	1.7
Surface doping density [#/cm^3]		
N-substrate	4x10^{16}	4x10^{16}
P-well	1.5x10^{17}	1.5x10^{17}

SEU Test Experimental Set-up

Two heavy ion beams were employed in our experiments, ^{81}Br and ^{197}Au. Most of our measurements were performed at elevated temperatures 80-125°C. An individual temperature controller described in [5] was used for each DUT. The chip was plugged into a home-made DIP socket with some extra pins on each side, and thermally coupled with a power resistor from underneath with high-temperature epoxy or heat-sink grease. The temperatures were measured by a precision ACE-48006 thermistor attached with the same compound from the top. The required power was less than 10W for 20 pin SRAM chips, and the nominal power of the heating element was even smaller than that. In the experiment, temperature was controlled within ±1°C.

The experiment was done using a MOSAID Memory Tester with 256K memory depth. Two testing modes are possible with this memory tester, static and dynamic. In static testing a bit map of errors is available but multiple hits are not recorded. In dynamic testing, the memory is checked for SEU during irradiation. If an error is found, the error counter is incremented by one and the error is corrected. Consequently, the error map is no longer available as it was in static testing. 16K, 64K & 256k CMOS SRAMs with feedback resistors performed satisfactorily in our test fixture down to 3.5 V. in both static and dynamic testing. However, preliminary measurements indicated a considerably higher SEU cross section in dynamic testing (Figure 2).

Because of cable capacitance (8 ft of flat cable between the memory tester, vacuum feedthrough, and the DUT), the constant memory reading/loading in dynamic testing resulted in 1 V noise on the power supply line. The lower average power supply voltage decreased the critical charge and increased SEU sensitivity. It is also seen in Fig.2 that dynamic testing performed at 5.0 V

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exhibited the same critical LET as static testing at 4.5 V. By adding a fast
tantalum capacitor 0.47 uF close to the DUT, the noise was reduced to 0.1V and
the SEU cross section decreased. Unfortunately, we did not collect enough
data to determine the critical LET. While dynamic testing is closer to device
field operation, the measured SEU cross section can be substantially varied
depending on the capacitive coupling between power supply and ground. To
avoid this variation, all subsequent measurements were performed in the static
mode. The power supply voltage was 5.0V and 4.5V for 16K and 64K SRAMs,
respectively.

When a single memory cell is upset twice during the static testing, no error
is recorded. If the same memory cell is upset one more time, only one error
is recorded and so on. Clearly, the observed number of SEU is smaller that
the actual number due to the possibility of multiple upsets of the same memory
cell. Depending on the parity, the multiple upsets either escape observation
entirely or are recorded as a single SEU. The following correction was
applied to all experimental data obtained by static testing to account for
multiple upsets:

$$P'_{SEU} = P_{SEU} - P^2_{SEU} + P^3_{SEU} - \ldots = \frac{P_{SEU}}{1 - P_{SEU}}$$

where the probabilities p'_{SEU} and p_{SEU} are given by the observed and corrected
numbers of SEU, respectively, divided by the memory size (16K or 64K). In
order to keep both this correction and statistical uncertainties small, it is
good practice to make the number of SEU approximately 10% of the memory size
by accumulating an appropriate fluence.

SEU Test Results and Discussion

No failures of any of the tested 16K SRAM (TA670) were observed at room
temperature up to the effective LET = 160 MeV cm^2/mg with any value of the
feedback resistors in either static or dynamic testing. The same statement
applies for testing at temperatures up to 50°C.

Data obtained for four 16K SRAMs with variable feedback resistors at 110°C
with Br ions using MOSAID Memory Tester are shown in Figure 3a. Data obtained
for 64K SRAMs at the same temperature and with the same ions using the MOSAID
Memory Tester are displayed in Figure 3b. The critical LET (defined as LET at
which the SEU cross section drops by a factor of 500 compared to its saturated
value, i.e. approximately 10-5 cm^2 for our 16K SRAMs) increased with the
increasing value of the feedback resistance as expected. Since both feedback
resistors values and the power supply voltages were different for 16K and 64K
SRAMs, we find little sense in comparing results for the two design rules.
All feedback resistor values are given at room temperature. They can be
calculated at elevated temperatures using a known temperature coefficient for
polysilicon resistors. The coefficient was measured for a resistor on the
test chip made by the same technology (see Figure 4). The dependence was
found to be exponential, where k is the Boltzman constant and −E = 0.0899(10)
eV the activation energy.

The SEU cross sections of the 16K SRAM with 82 Kohm feedback resistors were
measured at three different temperatures, 90,110,125°C, and with two ion
beams, Br and Au. Results obtained with the HP-8180/82 Data Generator/
Analyzer and with the MOSAID Memory Tester are shown in Figures 5a and 5b,
respectively. A difference was observed in the critical LET for the two ions.
The difference is, at least partially, caused by energy loss in the
passivation layer which has an equivalent thickness of approximately 1 mg/cm^2
of Silicon. The LET vs. energy curves for *Br* and *Au* ions imported from
Ziegler's Tables are plotted in Figure 6. A small energy loss shows 260 MeV
^{81}Br ions gradually approaching a maximum, thus the LET remains relatively
constant. On the other hand, 310 MeV^{197}Au ions have already passed the maximum
and are in the region of steep decay, thus a significant LET reduction is

expected. For example, in our second experiment using the MOSAID Memory Tester, the critical LET measured at 110°C was found to be 63 and 80 MeV cm^2/mg for 260 MeV ^{81}Br and 310 ^{197}Au ions respectively, thus reducing the difference to 10 MeV cm^2/mg. Preliminary measurements showed that LET in Ziegler's Tables is underestimated by 8% for Br and by 4% for Au in the energy regions of interest. Such a correction would reduce the critical LET difference to 8 MeV cm^2/mg. The most probable explanation of the residual difference is based on charge collection effects, where the ion track of Br in the device sensitive region is longer and more diffuse than that for Au, thus there is less recombination and more charge is collected.

Using the error map, the SEU cross sections measured at high angles of particle arrival were corrected for the chip package shadow (up to 40% and 6% at 0-73° for 16K and 64K, respectively) but they still tapered off. The most drastic effect was observed for the 16K SRAM with 240 Kohm feedback resistors tested at 125°C with Au ions (see Figure 7). A sharp maximum occurred around the effective LET = 143 MeV cm^2/mg and the SEU cross section dropped to zero above 180 MeV cm^2/mg. The corresponding angle of incidence were 56° and 63°. After penetrating the passivation layer, the effective LET became 121 and 139 MeV cm^2/mg at these two angles. The calculation proves that the energy loss itself is insufficient for the explanation of the observed data. At high angles of incidence, the collected charge is probably shared by two or more neighboring nodes and becomes insufficient to upset either one.

After initial SEU testing, one of the 64K SRAMs was exposed to 2 MeV protons. A total dose of 1.3 MRad(Si) was accumulated, 0.65 MRad(Si) without operating bias and 0.65 MRad(Si) in the memory state "all 0". After proton irradiation, the SEU test was repeated in both "all 0" and "all 1" memory states. While SEU cross section in the state "all 1" did not differ from its pre-radiation value, the SEU cross section in the state "all 0" showed a slight increase (see Figure 8). The SRAM was found to prefer the state in which it was irradiated. Ionizing radiation induces bias dependent threshold voltage shifts and mobility degradation which cause a CMOS SRAM cell imbalance. Since the most sensitive strike location, for the present technology, is the OFF P-channel drain which is restored through an N-channel transistor, the cell imbalance is defined as the difference between N-channel threshold voltage shifts. As the 64K, 256K and 32K x 8 SRAMs utilize the same "1.25um" process and the same device geometry one would expect similar SEU response. The 64K and 32K x 8 do in fact show similar response (see Figure 9). However, a greater feedback delay time for the same LET threshold is apparent in the 256K. This can only be attributed to circuit pattern effects [4a].

Hardening Approaches for CMOS SRAM

Resistive Hardening

SPICE simulation of SRAM cells with feedback resistors between the inverters [12][13][4a] shows agreement with critical LET threshold considering the decrease in delay as the polysilicon resistor value decreases with temperature increase thus decreasing LET threshold. Cell write delay times are shown in Figures 10 and 11 for the "1.25um" and "2um" processes respectively. The SRAM cells with feedback resistors are shown in Figure 12a. For the "2um" process SRAM disturbed by a 1 mA exponential pulse, the results at room temperature and 87°C are summarized in Table 3.

Table 3. 16K SRAM, 1mA Exponential Pulse

Temp.	Resistance	Max. Wid.to Q_c
27°C	82K	0.8nsec
87°C	46K	0.3nsec

Integrating the current pulse one finds an estimate of the disturbing charge

necessary to reach critical charge and cause an SEU in the SRAM cells at room and elevated temperatures. Clearly less charge is needed to cause an SEU at elevated temperatures.

Capacitive Hardening

In the MOSIS "2um" process the specific resistance of the polysilicon resistors is much lower and simulation of the distributed RC feedback shows that the resistor value may be decreased for equivalent LET threshold. However because of area considerations most commercial vendors will use higher specific resistance and shorter polysilicon resistor length negating the need for this correction [14].

Simulation of the insertion of a capacitance between the drain to gate nodes shows equivalent LET threshold and superior speed when compared with the feedback resistor approach. In this approach the capacitance is not in the write path of the cell. The write time is increased for this approach as the inserted capacitance increases the node capacitance. But this increased time is much smaller than the resistive hardening concept (see Figure 12b)[15].

The critical charge is 4.8 pC for a capacitance of 0.1pF for a rectangular current pulse of 3ns width and 1.6mA amplitude. For a 100 Angstrom oxide thickness the area for this capacitance is nearly equal to the area of an NMOS transistor. Speed performance becomes a problem as larger scales of integration are required. We conclude that the increased area for radiation-hardening can be sacrificed for better speed performance.

Active Hardening

A CMOS Transmission Gate (TG) exhibits a nonlinear current-voltage characteristic when it conducts; hence called nonlinear active resistor. The TG resistance strongly depends on its terminal voltage: increasing rapidly as the terminal voltage increases. This phenomenon can be utilized to increase SEU immunity of a SRAM cell. A SEU hardened CMOS SRAM cell using TGs as feedback resistors is shown in Figure 12c. In this cell, the inverter pair is decoupled by two TGs whose p-channel and n-channel transistors are respectively gated by the ground and power source. These transistors provide the resistance needed for increasing critical charge of the cell and also introduce additional capacitance to the sensitive nodes and feedback paths of the cell, which can effectively increase SEU immunity of the cell [16].

Operation of the cell can be described briefly as following. When the cell operates normally, the resistance of the two TGs is very low since the voltages across the gate terminals are very small. The cell is essentially an unhardened one. When one of the sensitive nodes is hit by an ionizing particle, electrical charges are collected at the hit node, causing a sudden voltage increase or decrease at the hit node while the voltages at other nodes are relatively unaffected. In response to the voltage increase across the terminals of the TG connected to the hit node, the resistance of the TG becomes very high. The high feedback resistance protects the stored cell data from SEU.

Effectiveness of the new SEU-hardening technique was studied numerically. The current induced by a particle hit was simulated by an exponential pulse. The rise and fall time constants of the exponential pulse were set equal to 0.01ns and 0.25ns respectively.

Simulations showed that the new technique improved the SEU immunity of a SRAM cell effectively. With TGs whose channel length was 12um and width was 1.2um, a CMOS SRAM cell did not upset from a current pulse with amplitude of 10mA and width of 1.4ns, as seen in Figure 13a. An estimate for this TG channel resistance is about 100 Kohm. Prevention of upset from the same current pulse required a passive feedback resistor of 205 Kohm. Figure 13b shows the simulation result. We believed that it was the combination of distributed channel resistance and parasitic capacitance, mainly gate capacitance, making

TGs more effective than lumped resistance in increasing critical charge of the cell. This observation agreed with our findings in [14] where distributed RC feedback was shown to be better than lumped RC and pure resistive feedback.

Switched Capacitor SRAM

It can be shown that if clock frequency is high enough, the combination of switches and capacitor can replace a resistor that is dependent only the clock frequency and capacitor [18][19][20].

The switched capacitor network employed in this work is single-phase grounded switched capacitor shown in Figure 14a. It consists of two switches and a capacitor. For SPICE simulations, the equivalent circuit that can be used for the single phase switched capacitor network is shown in Figure 14b.

The switched capacitor network was implemented using MOS technology. The circuit is shown in Figure 15. PSPICE simulations were performed. Samples of the output are shown in Figures 16,17 and 18.
The rise time, fall time, propagation delay, and time shift (T-shift) [i.e. the time required for the output to occur when the input signal is applied]. Table 1 shows the switching times for SRAM with no feedback resistors, switched capacitor SRAM and SRAM with feedback resistors of 40K, 80K, and 150K.

From Table 4, it can be seen that the rise time, fall time, propagation delay and T-shift of the switched SRAM and SRAM without feedback resistance are small compared to those of SRAM with feedback resistors. In addition, switching times of the switched capacitor SRAM are similar to those of SRAM without feedback resistors.

Table 4. Switching Times of SRAMs

Feedback Value	Fall Time * E-9	Rise Time * E-9	Prop. dly * E-9	T-Shift * E-9
SRAM w/out feedback	0.4087	0.380	0.395	0.765
SC SRAM	0.280	1.029	0.654	0.769
40K	1.70	1.581	1.64	2.296
80K	3.15	3.121	3.135	4.019
150K	5.73	5.503	5.616	6.972

Systems Level Analysis

This section addresses the problem of reliability and fault-tolerance from a systems point of view. Due to space considerations we will only provide a broad description of our approach and model. We view the system in a hierarchical fashion, viz., the system is considered as a collection of functional units, each functional unit made up of several functional subunits, and so on to the primitive elements (Figure 19). The black circles in the figure refer to "irreducible modules" -- subsystems that cannot be further subdivided into smaller systems. The white circles refer to "reducible modules."

At any given level of description, the system is seen to have a set of modules of each type. For instance, a private branch exchange system (PBX) consists of several "sequential" and "parallel" subsystems (see Figure 20). Another example is the Intel 80386 microprocessor consists of nine logical units: bus interface unit, prefetch unit, instruction decode unit, execution unit, control unit, data unit, protection test unit, segmentation unit and paging unit. The execution unit is further divided into ALU and the 32-bit register files. Each of these in turn can be broken down into gates and then to

transistors. Two important aspects of our approach are the inclusion of:

1. "correlational dependence'' of failure rates; for instance, the occurrence of one failure may accelerate the occurrence of another; and
2. explicit modeling of failure rates in terms of the geometrical, circuit and material parameters.

Each such unit is then modeled in terms of rate equations that would allow a computation of the MTTF. The reliability at any given level will be calculated by a generalized Markov model. The knowledge of MTTF for each subsystem may then be used in two ways: (i) from the parametric dependence of the MTTF, to choose different material combinations to maximize the MTTF; and (ii) to replicate those subsystems with a lower MTTF, so that the entire system may degrade gracefully. This approach is obviously better than assigning an average MTTF for the whole system.

Formulation

The general approach in terms of a non-Markovian model is given elsewhere [21-23]. In the following we discuss a simplified version, the so-called memory-less or Markovian approximation. In this limit, which is the most common limit used in the literature [24-25]. The corresponding equations are:

$$\frac{dP_i}{dt} = -\alpha_{i,i+1}P_i + \beta_{i+1,i}P_{i+1} + \alpha_{i-1,i}P_{i-1} - \beta_{i,i-1}P_i - \gamma_{i,f}P_i.$$

for i = 1,2,...,N-1, and

$$\frac{dP_0}{dt} = -\alpha_{0,1}P_0 + \beta_{1,0}P_1 - \gamma_{0,f}P_0., \quad \frac{dP_N}{dt} = \alpha_{N-1,N}P_{N-1}, \quad \frac{dP_f}{dt} = \sum_{i=0}^{N-1}\gamma_{i,f}P_i$$

where P_i is the probability that the subsystem is in the state S_i, a_{ij} is the transition (failure) rate from state S_i to state S_j, $b_{j,i}$ is the transition (repair) rate from state S_j to state S_i and $g_{i,f}$ is the transition (failure) rate from state S_i to the fatal state S_f. S_f denotes the "fatal failure state."

Solution

The above equations may be solved iteratively to yield the reliability R(t) and the MTTF:

$$R(t) = \sum_{i=0}^{N-1}P_i(t)$$

$$R(t) = L^{-1}[R(s)] = L^{-1}\left[\sum_{0}^{N-1}P_i(s)\right]$$

$$MTTF = \xrightarrow{\lim t \to 0} \sum P_i(s)$$

(s is the LaPlace Transform variable).

Sample Application

Let us apply this general solution to the case of a system with triple-modular- redundancy (TMR, see Fig. 21). That is, N=3.   In this case, units

A, B and C are identical units, while unit D may be an identical or a different unit. The system will function so long one of the former three units are functioning, but the moment unit D fails, the whole system fails. The failure of D is what is termed fatal or common-cause failure. (An electrical realization of this system is a typical buffer between two large circuits. A, B and C could be simple inverting buffers (INRBs) while D may be a super-inverting buffer (INRBS).] The MTTF for this case is given by,

$$MTTF = \frac{\Delta_1\Delta_2 - \beta_{2,1}\alpha_{1,2} + \alpha_{0,1}\Delta_2 + \alpha_{0,1}\alpha_{1,2}}{\Delta_0\Delta_1\Delta_2 - \Delta_0\alpha_{1,2}\beta_{2,1} - \Delta_2\alpha_{0,1}\beta_{1,0}}$$

Special Cases

Case	MTTF	Comment
$\alpha_{ij} = \alpha, \beta = 0, \gamma = 0$	$3/\alpha$	Three times the survival rate of a single component (or module), as should be expected
$\alpha = \gamma$	$7/8\alpha$	Less than the survival rate of a single component, i.e., inclusion of redundancy does not necessarily augment the reliability of the system in the presence of fatal faults
$\alpha_{0,1} = \alpha, \alpha_{1,2} = k\alpha, \alpha_{2,3} = k^2\alpha$ $\gamma_{i,\phi} = \alpha, \forall i$	$\frac{(k+1)^3 - k^2 - k + 1}{2(k+1)(k^2+1)}\left(\frac{1}{\alpha}\right)$	$k=1$, MTTF$=7/8\alpha$, previous result $k>1$, the MTTF is much smaller. $k=2$, MTTF$=11/15\alpha$

Failure Rate Models

Failure Phenomenon	Failure Rate
Electromigration	$\alpha = AJ^a \exp(-E_a / k_B T)$
Time-Dependent Dielectric Breakdown	$\alpha = AQ_{bd}^{-1} E_c^2 \exp(-B / E_c)$
Thermal Breakdown	$\alpha = \dfrac{P_f}{(\pi K\rho C_p)^{1/2} A_j(T_c - T_0)}$

Similar rates may be constructed for single-event-upsets, stuck-at-faults, etc.

Summary and Conclusions

1. No SEU of AT&T RAD-HARD SRAM was observed at Room Temperature.

2. Critical LET decreased with increasing temperature and/or decreasing value of feedback resistors.

3. Critical LET was different for Bromine and Gold ions because of Zeigler Curve effects and the heavy ion track structure.

4. Imprint of the memory pattern after 1.3 $MRad_{Si}$ TID of protons was consistent with the threshold voltage shift of NMOS transistors. This decrease in critical LET threshold is expected to be significant for non-RAD-Hard devices at much lower prior total dose radiation.

5. SPICE simulation of SRAM cells with feedback resistors between the inverters shows agreement with critical LET threshold considering the decrease in delay as the polysilicon resistor value decreases with temperature increase thus decreasing LET threshold.

6. In the MOSIS "2um" process the specific resistance of the polysilicon resistors is much lower and simulation of the distributed RC feedback shows that the resistor value may be decreased for equivalent LET threshold. However because of area considerations most commercial vendors will use higher specific resistance and shorter polysilicon resistor length negating the need for this correction.

7. Simulation of the insertion of a capacitance between the drain to gate nodes shows equivalent LET threshold and superior speed when compared with the feedback resistor approach. However this approach is not area conservative.

8. The active resistor(TG) SEU-hardening technique for CMOS SRAMs has been identified. This technique is effective in improving SEU immunity and needs no modifications of the fabrication process.The new technique shows low resistance except when necessary to limit cosmic ray induced charge.

9. The switched capacitor SRAM, implemented using MOS technology, has characteristics similar to those of CMOS SRAM without feedback resistors. The switching times of the switched capacitor SRAM are comparable to those of SRAM without feedback resistors. In addition, it was found that the switching times of the switched capacitor SRAM are superior to those of SRAM with feedback resistors. This work shows that switched capacitor SRAM is a viable alternative to SRAM with feedback resistors for SEU immunity.

10. An attempt to formulate a unified framework to compute the reliability of a system in the presence of fatal faults and redundant elements. In particular it is showed that, the inclusion of redundancy does not necessarily enhance the reliability of the system. Though the discussion has been in the framework of electronic systems, our formulation may also be used to describe distributed and parallel processing systems. In such cases, "failure" may be interpreted as "non-availability" of a processor (perhaps owing to its being accessed during its computation cycle) and MTTF might be an estimate of the length of computational time required for a given computation.

References

[1] Kerns, Shafer, Rockett Jr., Pfidmore, Berndt and Van Vonna, Proceedings IEEE, Vol.76, No.11, Nov.1988, pp. 1470-1509.

[2] J.L.Andrews, J.E.Schroeder & B.L. Gingerich, W.A. Kolasinski & R.Koga, S.E. Diehl, "Single Event Error Immune Cmos Ram". IEEE Trans. on Nucl. Sci. Vol. NS-29, No. 6, December 1982.

[3] T.N.Fogarty, C.Herman, K.Diogu, F.Wang, "Simulation of Natural Space Radiation Effects on VLSI Technology", Electrochem.Soc.Ext.Abstracts F87, #624,pp.880-881 (1987).

[4] V. Zajic, K. Kloesel, D. Ngo, P. M. Kibuule, A. Oladipupo, T. N. Fogarty, R. A. Kohler, E. G. Stassinopulos, "Single Event Upset and Total Dose Radiation Effects on Rad-Hard SRAMs","Journal of Electronic Materials, Vol 19, No. 7, 1990.

[4a] Private Communication R.A.Kohler AT&T BL Dec. 26 1986.

[5] W.A.Kolasinski, R.Koga, E.Scnauss, and JDuffey, "The Effect of Elevated Temperatures on Latchup and Bit Errors in CMOS Devices", IEEE Trans.Nucl.Sci.NS-33,pp.1605-1609(1986).

[6] Serafin Castro, "A Study on The Effects Of a Single-Event Upset And Radiation Hardening." M.S Thesis, Texas A&I University, Kingsville, TX, December 1991.

[7] James C. Pickel and James T. Blanford, Jr., " Cosmic-Ray-Induced Errors In MOS Devices," IEEE Transactions on Nuclear Science, Vol. NS-27, No. 2, April 1980.

[8] G. C. Messenger, " Collection of Charge On Junction Nodes From Ion Tracks," IEEE Transactions on Nuclear Science, Vol. NS-29, No. 6, December 1982.

[9] S.E. Diehl, A. Ochoa, Jr. and P.V. Dressendorfer, R. Koga and W.A.Kolasinski " Error Analysis and Prevention of Cosmic Ion-Induced Soft Errors in Static CMOS RAM", " IEEE Transactions on Nuclear Science, Vol. NS-29, No.6, December 1982.

[10] R.C. Jaeger, R. M. Fox and S. E. Dieh, "Analytic Expressions for the CriticalCharge In CMOS Static RAM Cells," IEEE Transactions on Nuclear Science, Vol. NS-30, No. 6, December 1983.

[11] Richard L. Johnson, Jr. and Sherra E. Diehl, " An Improved Single Event Resistive-Hardening Technique for Cmos Static Rams," IEEE Transactions on Nuclear Science, Vol. NS-33, No. 6, December 1986.

[12] Private Communication P.M. Kibole to T.N. Fogarty Hampton University Dec. 1989.

[13] Y.Suneel, S.Castro, T.Tang, J.S.Linder, Texas A&I University & T.N.Fogarty, PV A&M LRS "Simulation Study of Single Event Upset Immune CMOS SRAM". Proceedings PV A&M CEA Symposium, March 15,1993

[14] T.Tang, Y.Suneel, J.S.Linder, Teas A&I University, "Single Event Upset Immune CMOS SRAM With Distributed RC Feedback". Proceedings PV A&M CEA Symposium, March 15,1993

[15] J.S.Linder, S.H.Khan, T.Tang, Texas A&I University, "Capacitive Radiation Hardening Approach for SEUs of SRAM Cell", Proceedings PV A&M CEA Symposium March 15,1993.

[16] T.Tang, I.P.Tadptri, J.S.Linder, Texas A&I University, "An Active Resistive-Hardening Technique for CMOS SRAM". Proceedings PV A&M CEA Symposium, March 15,1993.

[17] F.Eshete, J.O.Attia, Prairie View A&M University, "Radiation Hardening of CMOS SRAM Using Switched Capacitor Networks". Proceedings PV A&M CEA Symposium, March 15,1993.

[18] R.L.Gieger, P.E.Allen, and N.R.Strader "VLSI Design Techniques for Analogue and Digital Circuits" McGraw-Hill, Inc., 1990.

[19] C.F.Kurth and G.S.Moschytz "Nodal Analysis of Switching Capacitor Networks" IEEE Trans. on Circuits and Systems, Vol. CAS-26, No.2, Feb.1979.

[20] B.D.Nelin "Analysis of Switched-Capacitor Networks Using General Purpose Simulation Programs" IEEE Trans. on Circuits and Systems, Vol. CAS-30, No.1, Jan.1983.

[21] A.A.Kumar, "VLSI Space Systems Reliability," Proceedings of the NASA Radiation Conference, Hampton, March 1991.

[22] A. A. Kumar, "Reliability of Large Scale Systems," Proceedings of the E&A'93 Symposium, Prairie View A&M University, Texas, March 15-16, 1993.

[23] A.A. Kumar, Models of Disordered Systems, book under preparation.

[24] W.K. Chung, "A k-Out-Of-N:G Redundant System with Dependent Failure Rates and Common-Cause Failures," Microelectron. Reliab., vol. 28, p. 201, 1988.

[25] W.K. Chung, "Reliabilty Analysis of Repairable and Non-Repairable Systems with Common-Cause Failures," Microelectron. Reliab., vol. 29, p. 545, 1989.
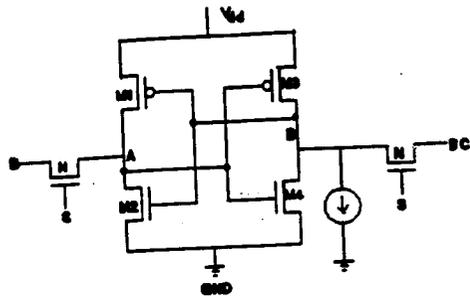
Figure 1a. A SRAM cell
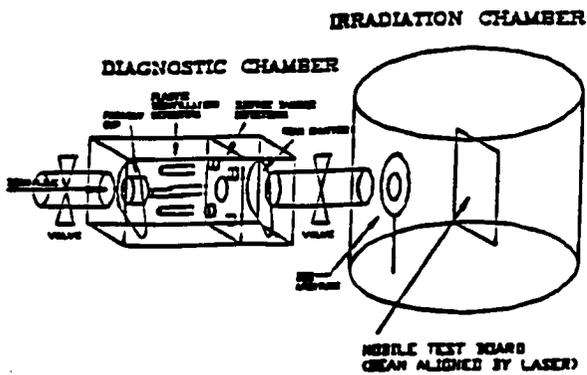
Figure 1b. Brookhaven SEU Test Facility
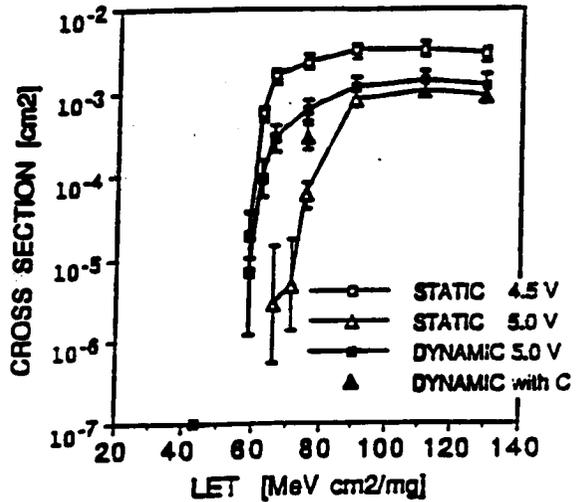
Figure 2. Effect of power supply voltage on SEU of 16K SRAM with 82 Kohm feedback resistor (90°C, Br ions). Zero SEU are displayed on the LET axis.
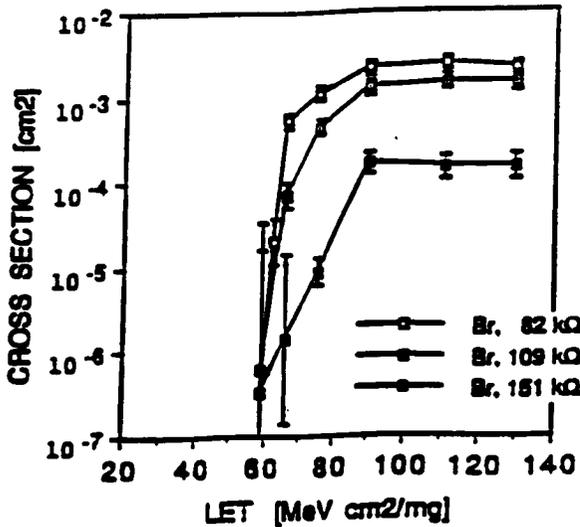
Figure 3a. SEU of 16K SRAMs with variable feedback resistors (110°C, Br ions). Data from MOSAID Memory Tester.
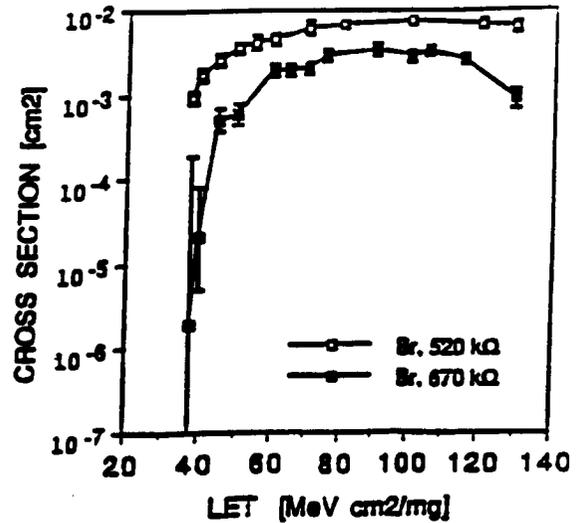
Figure 3b. SEU of 64K SRAMs with variable feedback resistors (110°C, Br ions). Data from MOSAID Memory Tester.
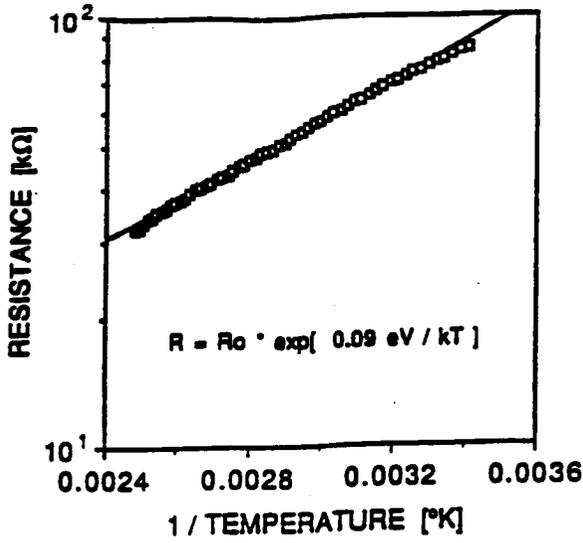
Figure 4. Temperature dependence of a polysilicon resistor.
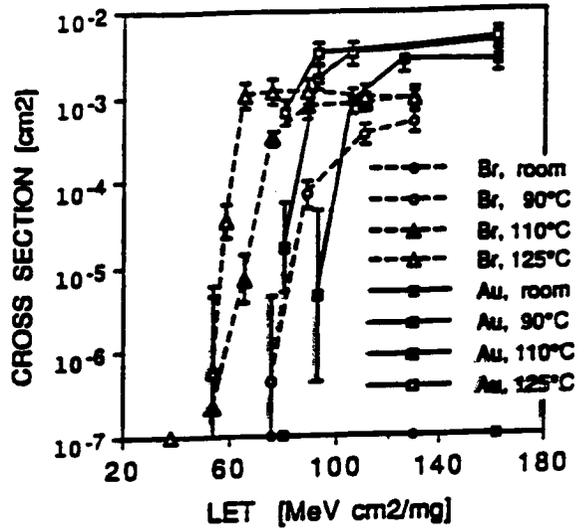
Figure 5a. SEU of 16K SRAM with 82 Kohm feedback resistors at elevated temperatures for Br and Au ions. Data from HP Data/Generator/Analyzer.
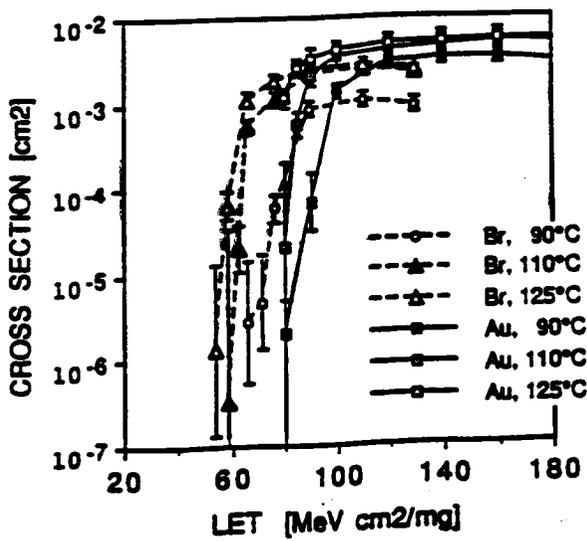
Figure 5b. SEU of 16K SRAM with 82 Kohm feedback resistors at elevated temperatures for Br and Au ions. Data from MOSAID Memory Tester.
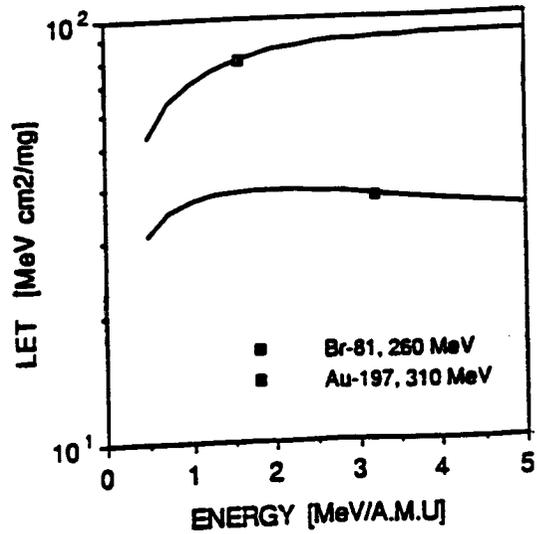
Figure 6. LET vs energy for [81]Br and [197]Au (from Ziegler's Tables).

CROSS SECTION [cm2]

10⁻² → 10^{-2}
10⁻³ → 10^{-3}

10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}

0   100   200   300

LET [MeV cm2/mg]

82 kΩ, 90°C
82 kΩ, 110°C
82 kΩ, 125°C
240 kΩ, 110°C
240 kΩ, 125°C
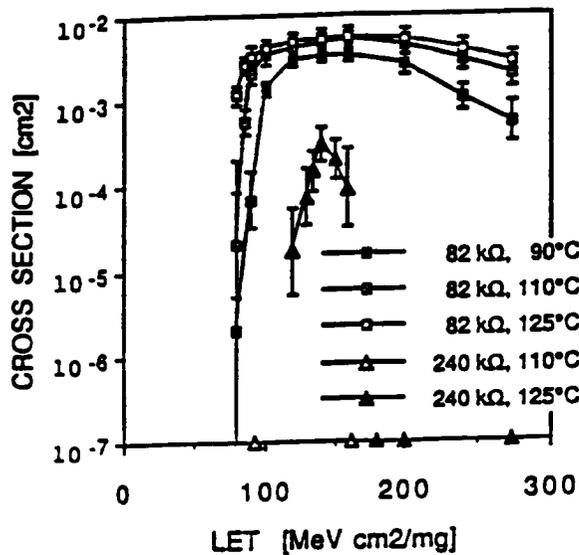
Figure 7. Decrease of SEU of 16K SRAMs at high angles of incidence for Au ions.

CROSS SECTION [cm2]

10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}

20 40 60 80 100 120 14C

LET [MeV cm2/mg]

Br, 80°C
PRE-RAD
POST-RAD 1 -> 0
POST-RAD 0 -> 1
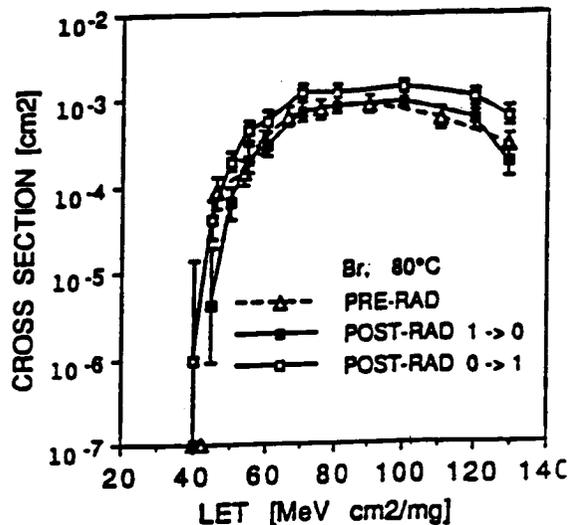
Figure 8. SEU of 64K SRAM with 520 Kohm feedback resistors before and after proton irradiation (80°C, Br ions).

Feedback Delay Time (ns)

8
7
6
5
4
3
2
1
0

20   40   60   80   100   120   140

Threshold LET (MeV/(mg/cm2))
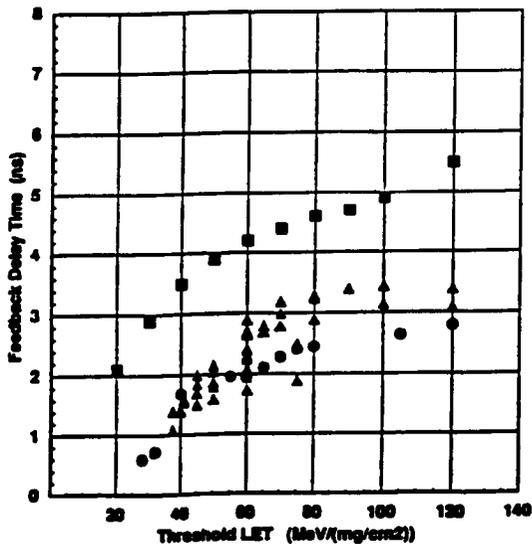
■ 256kx1
● 32kx8
▲ 64k SEC

The plots of the 256kx1 and the 32kx8 feedback delay times use the approximation of 1.5ns/100kΩ and measurement of feedback resistors.

The plot of the 64k SEC comes from direct write time delay measurements at the SEU test site using the baseline delay cell write time method.

The comparison implies that the required feedback delay time is reduced from the 256kx1 by the increased transistor drives in the 32kx8 memory cell.

Figure 9. Comparison of Fundamental SEU Response of 32K x 8 and 256K x 1 SRAMs.

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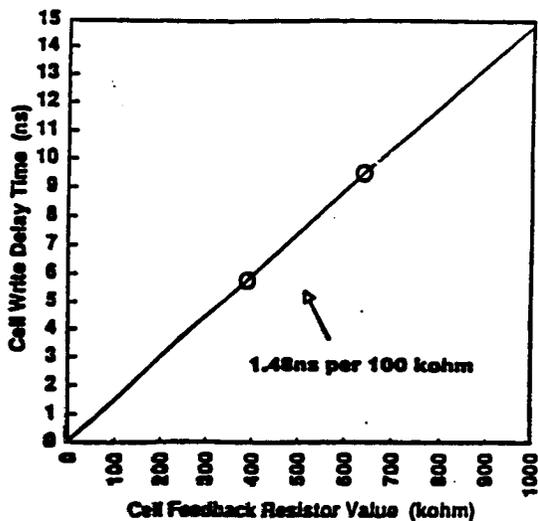
Figure 10. Feedback delay for 32K x 8 ("1.25um" process) cell produced by Cell Feedback Resistance as determined from write time method.
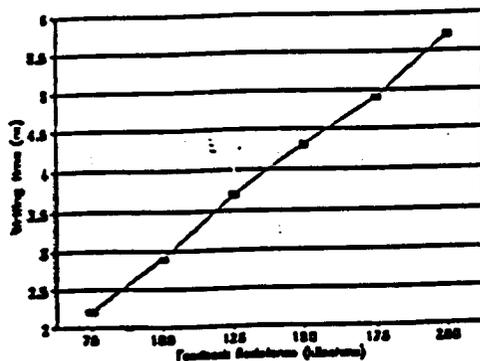
Figure 11. Write time vs. Feedback Resistance for "2um" process.

NODE'1'=Bit line
NODE'2'=Bitline compliment
WL=Word line
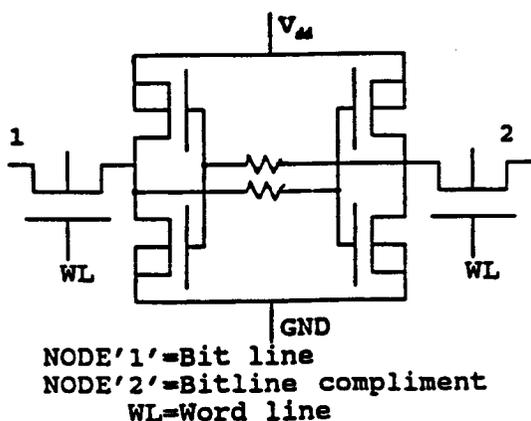
Figure 12a. SRAM Cell with feedback resistors.

NODE'1'=Bit line
NODE'2'=Bitline compliment
WL=Word line
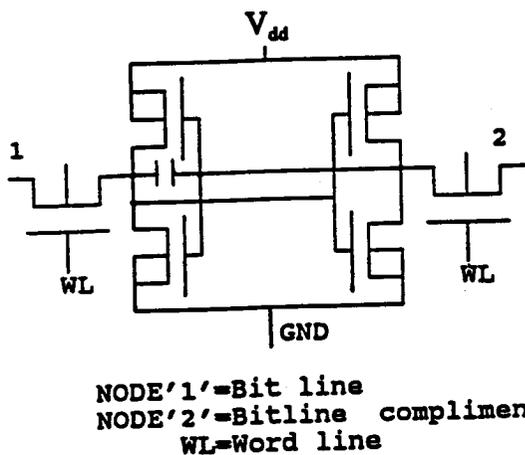
Figure 12b Schematic diagram of a capacitive-hardened SRAM.
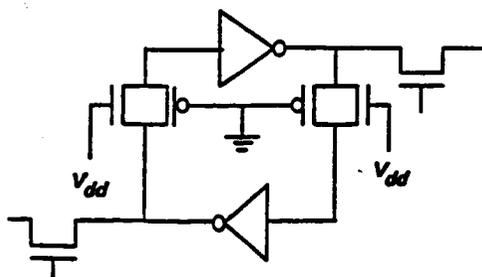
Figure 12c. A CMOS SRAM Cell with TGs as feedback resistors.

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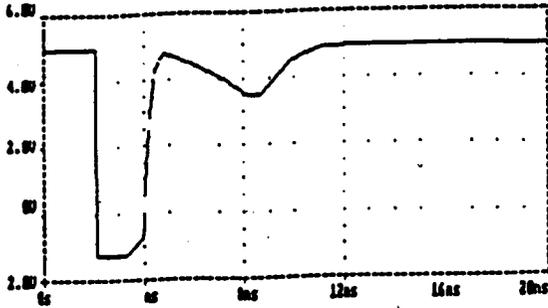
Figure 13a. Simulation Result of SRAM
with TGs as feedback resistors.

Figure 14a. Single phase grounded
switched capacitor.

Figure 13b. Simulation result of SRAM
with passive feedback resistors.
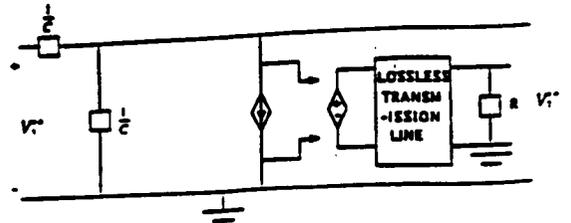
Figure 14b. Continuous-time domain
equivalent circuit with
implementation of lossless
transmission line.
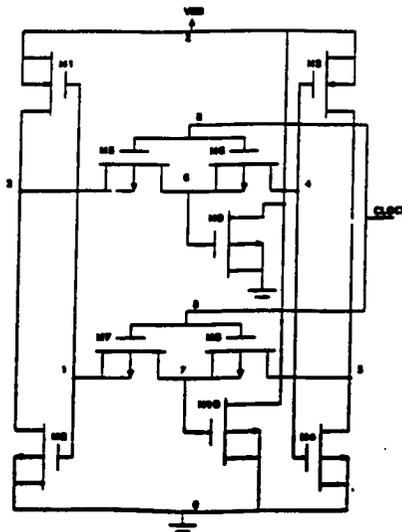
Figure 15. Switched Capacitor SRAM.
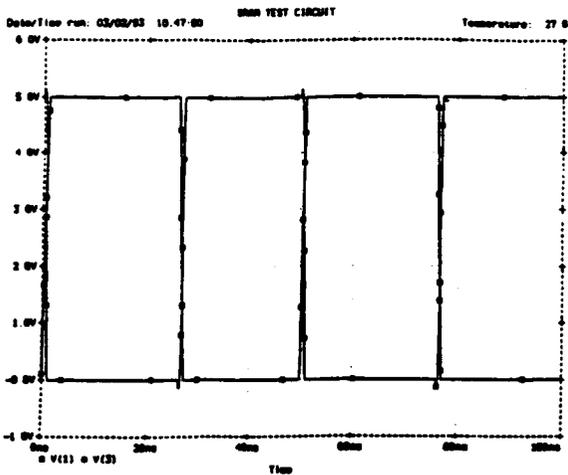
Figure 16. Transient analysis of CMOS SRAM without feedback resistor. V(1) is input and V(3) is output.
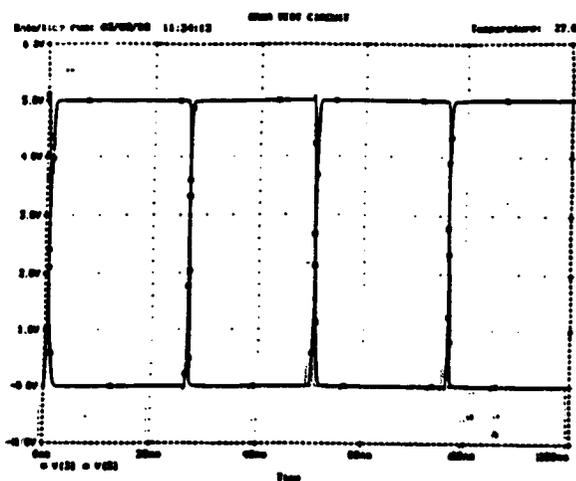
Figure 17. Transient analysis of switched capacitor SRAM. V(3) is input and V(5) is output.
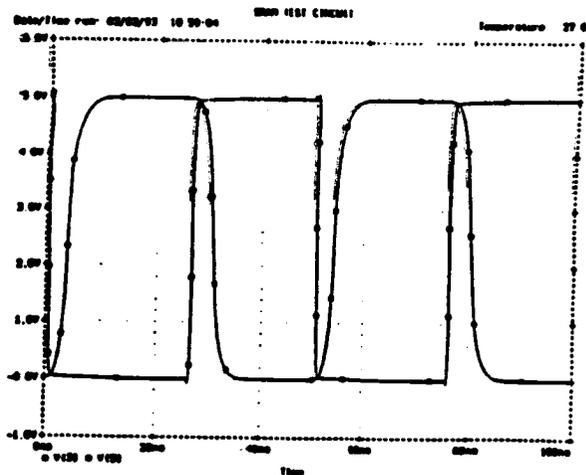
Figure 18. Transient analysis of CMOS SRAM with feedback resistor of 80 Kohms. V(3) is input and V(5) output.
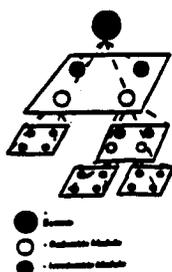
Figure 19. Hierarchical View of a system.
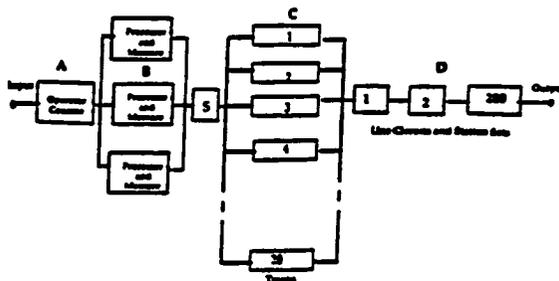
Figure 20. A private branch exchange system (PBX).

Figure 21 TMR System.