SILICON DEVICE PERFORMANCE MEASUREMENTS TO SUPPORT TEMPERATURE RANGE ENHANCEMENT

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Summary

Silicon based power devices can be used at 200°C. The device measurements made during this program show a predictable shift in device parameters with increasing temperature. No catastrophic or abrupt changes occurred in the parameters over the temperature range. As expected, the most dramatic change was the increase in leakage currents with increasing temperature. At 200°C the leakage current was in the milliAmp range but was still several orders of magnitude lower than the on-state current capabilities of the devices under test. This increase must be considered in the design of circuits using power transistors at elevated temperature.

Three circuit topologies have been prototyped using MOSFET's and IGBT's. The circuits were designed using zero current or zero voltage switching techniques to eliminate or minimize hard switching of the power transistors. These circuits have functioned properly over the temperature range. One thousand hour life data have been collected for two power supplies with no failures and no significant change in operating efficiency.

While additional reliability testing should be conducted, the feasibility of designing soft switched circuits for operation at 200°C has been successfully demonstrated.

INTRODUCTION

Semiconductor power devices are typically rated for operation below 150°C. While digital and low power analog devices have been characterized at elevated temperatures [1-4], little data are available for power semiconductors over 150°C [5]. In most cases, the device is derated to zero operating power at 150°C to 175°C. A typical derating curve found in the manufacturer's data book for a power MOSFET is shown in Figure 1 [6].

Typical space-based power sources generate high currents at low voltages. To reduce resistive losses and the weight associated with high current busses, it would be advantageous to locate the power conversion and conditioning electronics as close to the primary source as possible. Location, however, is limited by the local temperature generated by the power source. Electronics capable of operating at higher temperatures could be placed nearer the power source. In addition, conversion and conditioning electronics produce significant heat which must ultimately be removed. High temperature electronics would result in a higher heat rejection temperature for the thermal management system resulting in a reduction in the size of the thermal radiators and decreasing launch weight.

Higher operating temperatures are also beneficial in terrestrial applications. The maximum temperature for automotive underhood electronics is increasing due to changes in styling and airflow patterns for improved fuel efficiency. Recently Texas Instruments discussed an automotive fuel injector power IC for operation to 200°C [7]. In computer and office equipment, higher operating temperatures reduce or eliminate the need for forced air, reducing noise levels.

Temperature variations in the device parameters must be quantified in order to implement extended temperature range operation. The fundemental device physics indicates silicon devices should operate with some variation in device parameters over a temperature range from -125°C to over 300°C. Below -125°C, the impurity (doping) atoms are not 100% ionized and as the temperature decreases further, the ionization percentage decreases. At the high temperature end of the temperature range, the intrinsic carrier concentration increases to equal the doping concentration level and the silicon behaves as an intrinsic semiconductor with no p-n junctions. Figure 2 plots the electron density as a function of inverse temperature for n-type silicon doped at 10^{15} cm^{-3} [8]. The increase in intrinsic carrier concentration, results in a shift of the Fermi level toward mid-bandgap at elevated temperatures. The position of the Fermi level for an intrinsic semiconductor is at mid-bandgap. By increasing the doping concentration, higher operating temperatures can be achieved. The Fermi level as a function of temperature and doping level is plotted in Figure 3 [9]. This technique of increasing doping level has been used to fabricate low power analog and digital devices in silicon with junction operating temperatures in excess of 300°C.

The goal of this program was to characterize four power transistor types: a bipolar junction transistor (BJT), an n-channel metal-oxide-semiconductor field effect transistor (N-MOSFET), an insulated gate bipolar transistor (IGBT), and a MOS-Controlled Thyristor (MCT), and to demonstrate the operation of the some devices in power converter applications.

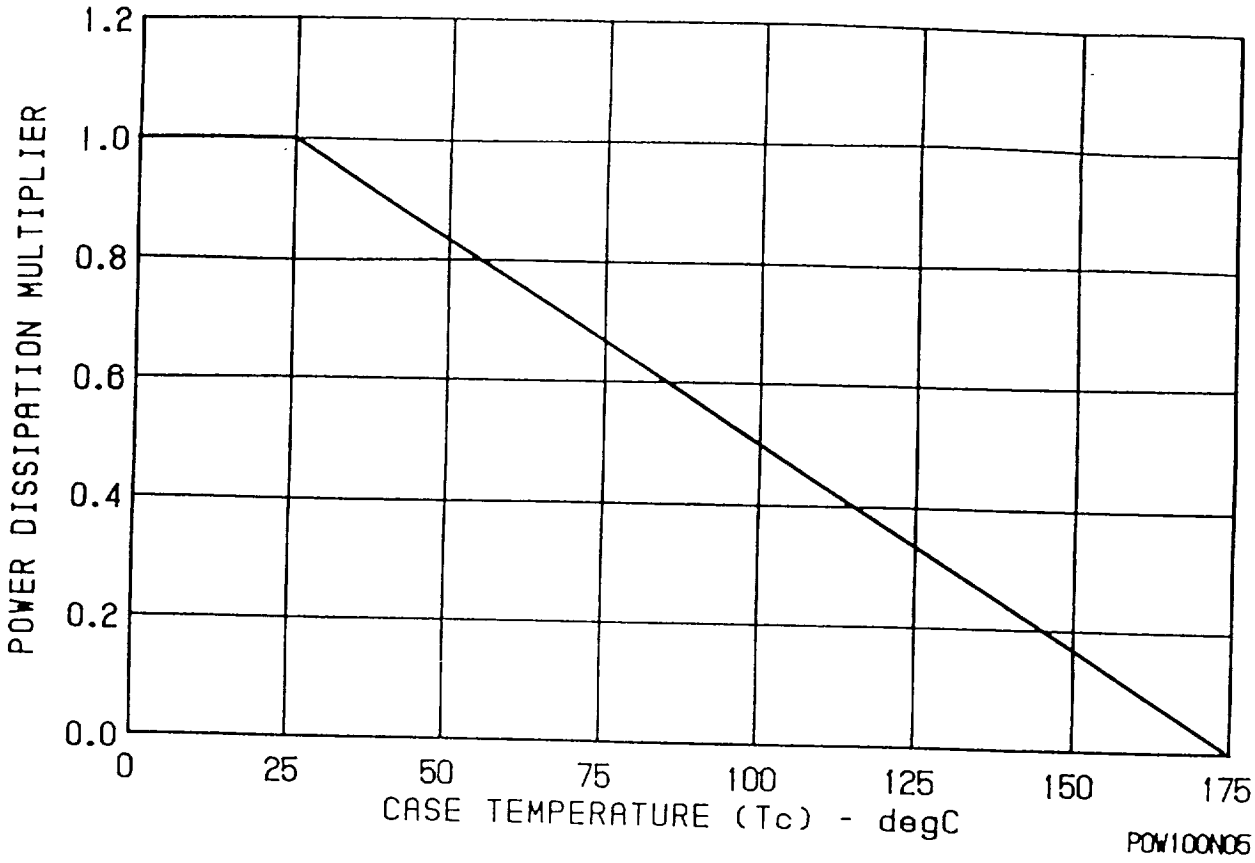

Figure 1. Normalized Power Dissipation VS. Temp. Derating Curve [Ref. 6]

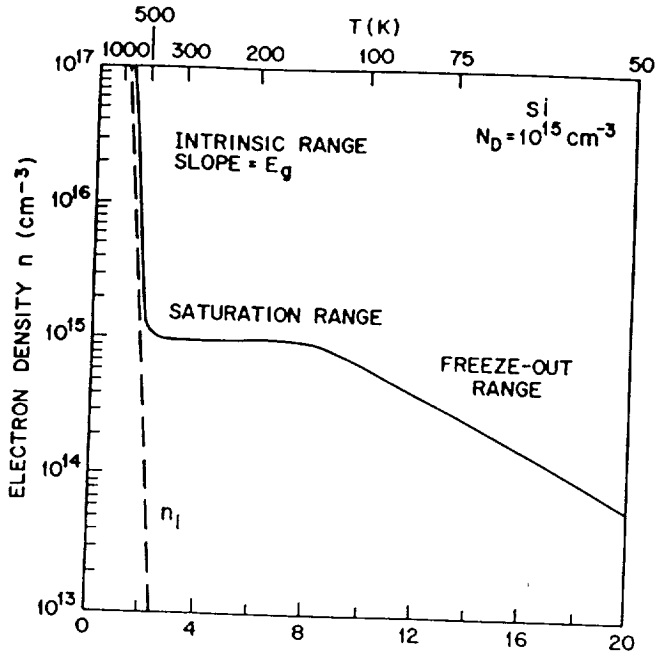

Figure 2. Electron density as a function of temperature for a Si sample with donor impurity concentration of 10^{15} cm^{-3}. [Ref. 8]

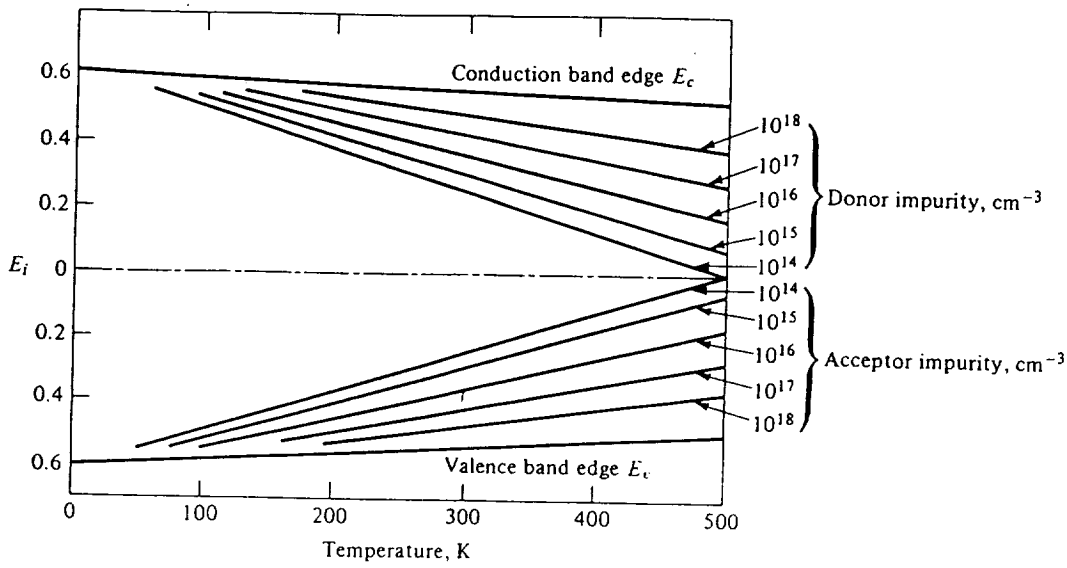

Figure 3. The Fermi level in silicon as a function of temperature for various impurity concentrations. [Ref. 9]

Chapter 1 SEMICONDUCTOR PARAMETERS AS A FUNCTION OF TEMPERATURE

The fundamental properties of the semiconductor device change as a function of temperature. These changes in turn affect the device operating parameters. A number of the basic temperature relationships and their impact on device performance will be reviewed in this section. As discussed above, the intrinsic carrier concentration, n_i, increases with temperature. This relationship is given in equation 1:

$$n_i = \sqrt{N_c N_v}\, e^{-E_g/2kT} \qquad \text{eqn. 1}$$

where N_C = effective density of states in the conduction band
N_V = effective density of states in the valence band
E_g = bandgap energy
k = Boltzmann's constant
T = temperature

The bandgap energy, E_g, is slightly temperature sensitive. For silicon:

$$E_g = 1.21\text{eV} - (2.8\times10^{-4}\text{eV/K})T \qquad \text{eqn. 2}$$

The density of states, N_C and N_V, are also temperature dependent:

$$N_c = 2\left(\frac{2\pi m_e kT}{h^2}\right)^{\frac{3}{2}} \qquad \text{eqn. 3}$$

$$N_v = 2\left(\frac{2\pi m_h kT}{h^2}\right)^{\frac{3}{2}} \qquad \text{eqn. 4}$$

Where: m_e = the effective mass of an electron
m_h = the effective mass of a hole
h = Planck's constant

Substituting equations 3 and 4 in to equation 1 yields:

$$n_i^2 = K_1 T^3 e^{-E_{go}/kT} \qquad \text{eqn. 5}$$

Where K_1 = constant
E_{go} = bandgap at 0°K

As previously noted, the Fermi Level is dependent on temperature and doping level:

$$E_f = E_c - kT\ln\frac{N_c}{N_d} \qquad \text{for n-type} \qquad \text{eqn. 6}$$

$$E_f = E_v + kT\ln\frac{N_v}{N_a} \qquad \text{for p-type} \qquad \text{eqn. 7}$$

Where E_C = conduction band edge energy
N_d = the donor concentration level
E_V = valence band edge energy
N_d = the acceptor concentration level

The conductivity, σ, of the semiconductor is related to the carrier concentration and the mobility of the carrier:

$$\sigma = q\mu_e n + q\mu_p p \qquad \text{eqn. 8}$$

Where q = charge on an electron
μ_e = mobility of an electron
n = electron concentration
μ_p = mobility of a hole
h = hole concentration.

Mobility is a function of temperature and doping concentration as shown in Figure 4 for electrons. The decrease in mobility with increasing temperature is due to increased lattice scattering.

The diffusion constant for electrons and holes is related to temperature and mobility by the following equations:

$$D_n = \mu_e \frac{kT}{q} \qquad \text{eqn. 9}$$

$$D_p = \mu_p \frac{kT}{q} \qquad \text{eqn. 10}$$

At higher doping, mobility is weakly related to temperature and the diffusion constant increases with increasing temperature. At lower doping levels, the mobility decreases exponentially with increasing temperature and the diffusion constant decreases with increasing temperature.

The diffusion length for injected holes and electrons is the mean distance the injected hole or electron travels before recombination takes place and is defined by:

$$L_e = \sqrt{D_e \tau_e} \quad \text{for electrons} \qquad \text{eqn. 11}$$

$$L_p = \sqrt{D_p \tau_p} \quad \text{for holes} \qquad \text{eqn. 12}$$

Where τ_e = electron lifetime before recombination
τ_p = hole lifetime before recombination

Leakage Current

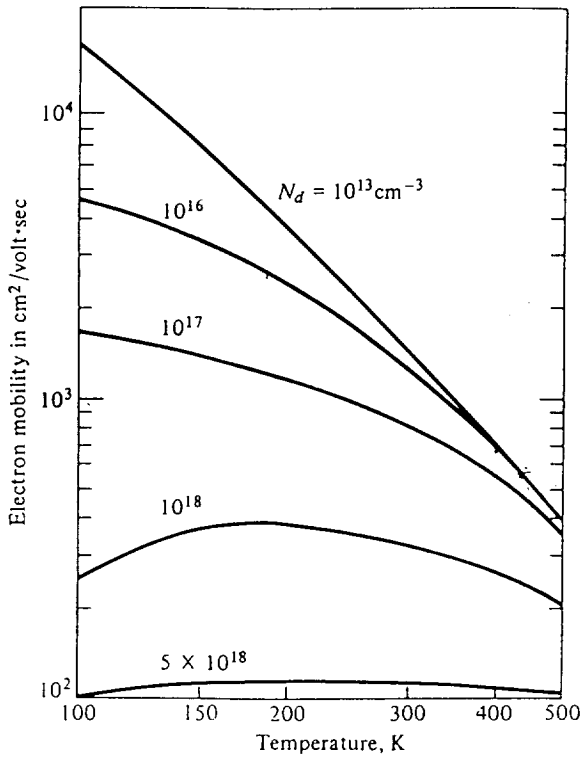

Figure 4. Mobility as a function of temperature in silicon. [Ref. 9]

Device leakage current is often considered the limiting factor in using silicon devices at elevated temperature. In all four transistors, the on-state leakage current is through a reverse biased p-n junction in the transistor structure. The equation for the reverse bias saturation current in a p-n junction is given by:

$$I_o = qA\left[\frac{D_N}{L_N}n_{po} + \frac{D_P}{L_P}p_{no}\right] = qA\left[\frac{D_N n_i^2}{L_N N_A} + \frac{D_P n_i^2}{L_P N_D}\right] \qquad \text{eqn. 13}$$

Where I_o = saturation current
A = area of the junction
n_{po} = equilibrium minority carrier concentration
p_{no} = equilibrium minority carrier concentration
n_i = intrinsic carrier concentration

The intrinsic carrier concentration which increases with increasing temperature has a significant effect on the leakage current. D_N, L_N, n_{po}, D_p, L_p, and p_{no} are also a function of temperature, but their effect is secondary to that of n_i. The approximate fractional change in the leakage current of a reverse biased p-n junction can be estimated. The ideal diode equation is:

$$I = I_o\left(e^{V/V_T} - 1\right) \qquad \text{eqn. 14}$$

Differentiating I with respect to T and neglecting the unity term yields:

$$\left.\frac{dI}{dT}\right|_{V=\text{constant}} = I\left(\frac{1}{I_o}\frac{dI_o}{dT} - \frac{V}{TV_T}\right) \qquad \text{eqn. 15}$$

From equation 1:

$$I_o \alpha\ n_i^2\ \alpha\ T^3 e^{-E_{go}/kT} \qquad \text{eqn. 16}$$

Differentiating with respect to T

$$\frac{1}{I_o}\left(\frac{\partial I_o}{\partial T}\right) = \left(\frac{3}{T} + \frac{E_{go}}{kT^2}\right) \cong \frac{E_{go}}{kT^2} \qquad \text{eqn. 17}$$

Finally substituting into equation 3:

$$\frac{1}{I}\left(\frac{\partial I}{\partial T}\right) = \frac{qV - E_{go}}{kT^2} \qquad \text{eqn. 18}$$

Where: V = the applied voltage
$V_T = kT/q$

The leakage current of a p-n junction increases by approximately +8% per ^{o}C, which corresponds to a doubling for every 10°C - 12°C increase in temperature. Increased leakage results in increased off-state losses in the power switch.

Saturation Voltage And On-Resistance

In current switching applications, the saturation voltage, $V_{ce_{sat}}$, plays a major role in determining the on-state bipolar transistor losses. Under normal switching operation, the saturation voltage drop across the bipolar transistor or insulated gate bipolar transistor occurs in the non-conductivity modulated drift region of the collector. The doping level of this region is typically low. This is necessary in high voltage devices to avoid breakdown. The mobility decrease, as shown in Figure 4, with increasing temperature resulting in an increase in the resistivity of the drift region. At a constant current, the voltage drop across the drift region will increase with increasing temperature.

As reported in refs 10 and 11, the forward voltage drop of the MCT decreases with temperature at high current levels. In the forward conducting state, the transistors in the thyristor structure are in saturation and the excess carrier concentrations in the base regions reach high-level injection. The doping concentrations in these two layers becomes unimportant and the structure behaves like a p-i-n diode with the transistor base layers forming the intrinsic region.

Equation 19 shows that when the p and n regions of the p-i-n diode are in low-level injection, the current density in a p-i-n diode is proportional to the intrinsic carrier concentration.

$$J=\frac{2qL_a n_i}{t_a}\tanh\left(\frac{w_i}{2L_a}\right)\left(e^{(qV_a/2kT - 1)}\right) \qquad \text{eqn. 19}$$

Where L_a = diffusion length
t_a = transit time of carriers
W_i = intrinsic region width
V_a = forward voltage

By substituting in the approximation for n_i shown in Equation 20 into Equation 19, Equation 21 is obtained.

$$n_i = T^{3/2}e^{-E_g/2kT} \qquad \text{eqn. 20.}$$

$$J=\frac{2qL_a T^{3/2}}{t_a}\tanh\left(\frac{w_i}{2L_a}\right)\left(\frac{e^{(qV_a/2kT - 1)}}{e^{(E_g/2kT)}}\right) \qquad \text{eqn.21}$$

This equation shows that for a given forward voltage, the current density through the diode increases with increasing temperature. Conversely, the forward drop decreases with temperature if the forward current in fixed.

The on-state resistance of the MOSFET is determined by the mobility of the carriers. Increasing temperature will result in increased on-state resistance. The extend depends on the doping level.

Breakdown Voltage

The breakdown voltage determines the maximum voltage the device can block. Avalanche multiplication is the most significant mechanism in junction breakdown. It establishes the upper

limit on the reverse bias for most diodes, on the collector voltage of bipolar transistors, and on the drain voltage of MOSFET's. In avalanche multiplication breakdown, under high electric fields impact ionization occurs creating hole-electron pairs. These holes and electrons subsequently have collisions creating additional holes and electrons - a multiplication effect which leads to breakdown of the junction. As the temperature increases the breakdown voltage increases. Carriers traveling through the depletion layer under a high field lose part of their energy to optical phonons after traveling each electron-phonon mean free path λ. The value of λ decreases with increasing temperature:

$$\lambda = \lambda_0 \tanh\left(\frac{E_p}{2kT}\right) \qquad \text{eqn. 22}$$

Where E_p = average energy loss per phonon scattering

Carriers lose more energy to the crystal lattice along a given distance at constant fields with increasing temperature. Therefore, the carries must pass through a greater potential difference (higher voltage) before they can acquire sufficient energy to generate an electron-hole pair. The temperature dependence of breakdown voltage is shown in Figure 5. The increase is also dependent on the doping concentrations.

The MCT requires an applied voltage to hold the device off. When forward biased and held in the off state by a positive gate-to-anode voltage, the collector-base junction of the npn transistor in the thyristor structure is the only reverse biased junction blocking the anode-to-cathode voltage. The transistor action of the npn transistor multiplies the current through this junction. Therefore, it is expected that the forward breakdown voltage of the MCT would decrease as temperature increases. Arther, et. al. have recently reported similar results for P-MCT's showing a decrease in breakdown voltage with increasing temperature[12]. The effect is less evident in N-MCT's, since the transistor action is for a pnp transistor with a lower current gain.

Dc Beta In The BJT

There is a peak in Beta at low current levels in BJT's as the generation and diffusion currents dominate the emitter-base junction. However, Beta "fall-off" occurs at high current levels due to the bandgap narrowing, Auger recombination and the Shockley-Hall-Read process. These effects are shown in Figure 6. In addition, at high current conditions the effective base width increases (Kirk effect) causing a further reduction in Beta.

At low current levels the Beta of the transistor is given by:

$$\frac{1}{\text{Beta}} = \frac{N_a x_B D_p}{N_{dE} x_E D_n} + \frac{x_B^2}{2L_n^2} + \frac{N_a x_B W_E}{2D_n \sqrt{N_c N_v}\,\tau_o} e^{(E_g - V_E)/2kT} \qquad \text{eqn. 23}$$

Where x_B = base width
N_{dE} = donor concentration in the emitter
x_e = emitter width
W_E = emitter depletion layer width
V_E = base-emitter voltage
τ_o = effective minority carrier lifetime in the depletion region

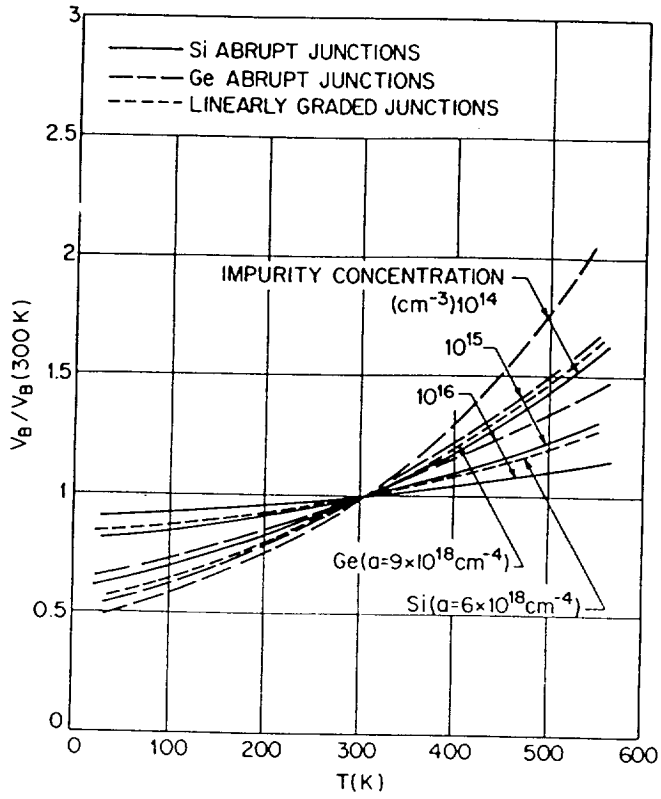

Figure 5. Normalized avalanche breakdown voltage versus lattice temperature. The breakdown voltage increases with temperature. [Ref. 8]

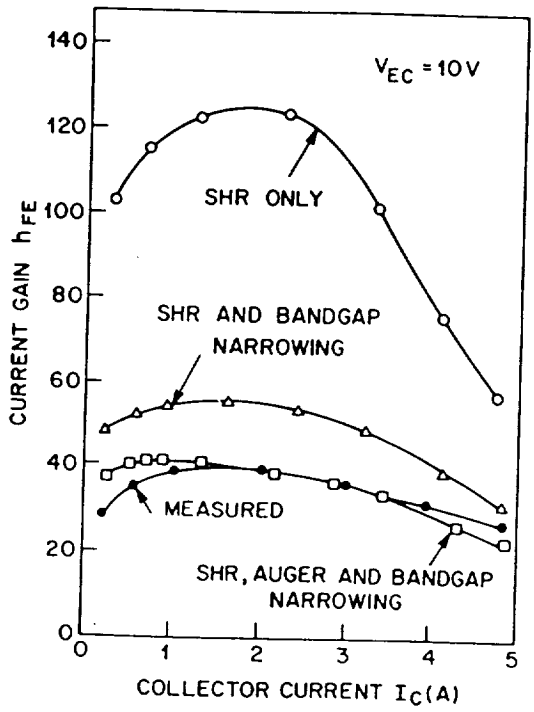

Figure 6. Comparison of calculated current gain with measured current gain versus collector current. [Ref. 8]

Substituting the temperature dependencies into equation 23 yields:

$$\frac{1}{\text{Beta}} = \frac{N_a x_B \mu_p \frac{kT}{q}}{N_{dE} x_E \mu_e \frac{kT}{q}} + \frac{x_B^2}{2\mu_e \frac{kT}{q} \tau_e} + \frac{N_a x_B W_E}{2\mu_e \frac{kT}{q} \sqrt{4\left(\frac{2\pi m_e kT}{h^2}\right)^{\frac{3}{2}} \left(\frac{2\pi m_h kT}{h^2}\right)^{\frac{3}{2}} \tau_o}} e^{(E_g - V_E)/2kT} \qquad \text{eqn. 24}$$

The dependency on temperature largely cancels in the first term. With respect to the second term, its affect is dependent on the doping level of the base. The product of decreasing mobility and increasing T can be assumed to result in only a slight effect on Beta. The third term has a strong temperature dependency. Since the base-emitter voltage, V_E, is less than the bandgap, V_g, for silicon, the value of the exponential term increases with increasing temperature. Also the temperature terms in the denominator will further increase Beta as the temperature increases, which leads to a further increase in Beta at low current levels with increasing temperature.

For high level injection, Beta is given by:

$$\frac{1}{\text{Beta}} = \frac{N_a x_B D_p}{N_{dE} x_E D_n}\left(1 + \frac{I_E x_B}{2qD_n A N_a}\right) + \frac{x_B^2}{4L_n^2} \qquad \text{eqn. 25}$$

In comparison to the equation for low level injection, the temperature dependency is significantly less for high level injection than for low level due to the elimination of the third term. The exact dependency will be determined by the doping level and their impact on mobility and the diffusion constants in equation 22.

Threshold Voltage In The MOSFET

The change in threshold voltage can vary over the range from -2 to -100mV/°C depending on the doping concentration and oxide thickness. The threshold voltage in the linear region is given by:

$$V_T = \phi_{ms} - \frac{Q_f}{C_i} + 2\psi_B + \frac{\sqrt{4\varepsilon_s q N_A \psi_B}}{C_i} \qquad \text{eqn. 26}$$

Differentiating with respect to temperature yields:

$$\frac{dV_T}{dT?} = \frac{d\psi_B}{dT}\left(2 + \frac{1}{C_i}\sqrt{\frac{\varepsilon_s q N_A}{\psi_B}}\right) \qquad \text{eqn. 27}$$

where;

$$\frac{d\psi_B}{dT?} \cong \pm \frac{1}{T}\left(\frac{E_{go}}{2q} - |\psi_B|\right) \qquad \text{eqn. 28}$$

Published experimental results for threshold voltage as a function of temperature, doping level and oxide thickness are presented in Figure 7.

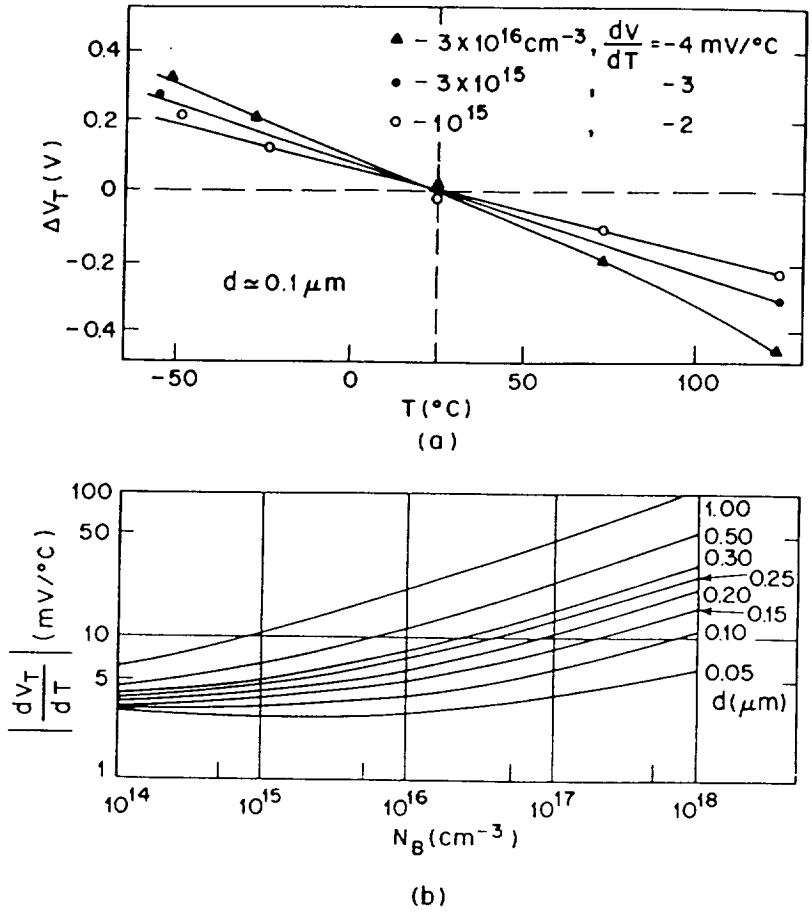

Figure 7. (a) Experimental measurement of threshold voltage versus temperature. (b) dV_T/dT of a Si-SiO_2 system versus substrate doping with oxide thickness as a parameter. [Ref. 8]

Switching Times

The governing equations for the stitching time delays of a bipolar transistor in the common emitter configuration are:

$$\tau_o = \frac{1}{\omega_N(1 - \alpha_N)} \ln\left(\frac{I_{B1}}{I_{B1} - 0.9I_{C1}\left(\frac{1}{\alpha_N} - 1\right)}\right) \qquad \text{eqn. 29}$$

$$\tau_1 = \frac{\omega_N + \omega_I}{\omega_N\omega_I\left(1 - \frac{\alpha_N\alpha_I}{1 - \alpha_N}\right)} \ln\left(\frac{I_{B1} - I_{B2}}{I_{C1}\left(\frac{1 - \alpha_N}{\alpha_N}\right) - I_{B2}}\right) \qquad \text{eqn. 30}$$

$$\tau_2 = \frac{1}{\omega_N(1 - \alpha_N)} \ln\left(\frac{I_{C1} - \left(\frac{\alpha_N}{1 - \alpha_N}\right)I_{B2}}{0.1I_{C1} - \left(\frac{\alpha_N}{1 - \alpha_N}\right)I_{B2}}\right) \qquad \text{eqn. 31}$$

Where
τ_o = turn-on time
$\tau_1 + \tau_2$ = the turn-off time of the transistor
τ_1 = storage time
τ_2 = decay time
ω_N = alpha cutoff frequency
$\omega_N(1 - \alpha_N)$ = beta cutoff frequency
ω_I = inverted alpha cutoff frequency
α_N = normal current gain
α_I = inverse current gain under inverted operating conditions
I_{B1} = base current
I_{C1} = collector current

The delay times are inversely proportional to the cut-off frequency of the transistor. The cutoff frequency, f_T, is given by:

$$f_T = \left\{2\pi\left[\frac{kT(C_E + C_C + C_P)}{qI_C} + \frac{W^2}{\eta D_B} + \frac{x_c - W}{2v_s}\right]\right\}^{-1} \qquad \text{eqn. 32}$$

Where
C_E = emitter capacitance
C_C = collector capacitance
C_E = parasitic capacitance
W = base width
η = 2 for a uniformly doped base layer
v_S = saturation velocity of the collector

From this equation, one finds an inverse relationship between temperature and the cutoff frequency. Therefore, the delay times increase with temperature.

For a MOSFET, the cutoff frequency is given by:

$$f_T = \frac{\mu_n V_D}{2\pi L^2} \qquad \text{eqn. 33}$$

Where V_D = drain voltage
L = channel length

Since mobility generally decreases with increasing temperature (the rate is s function of doping levels), the cutoff frequency decreases with increasing temperature and the delay times should increase.

Chapter 2. DEVICES UNDER TEST

The four devices used for testing were supplied by Harris Semiconductor. The devices were chosen as typical representatives of the four transistor types (See Table 1). The IGBT and the MCT represent higher blocking voltage capability, while the N-MOSFET has the highest current rating. Only the bipolar transistor was available commercially in a hermetic metal package. The other three devices were packaged in plastic packages. The glass transition temperature for semiconductor molding compounds is typically 180°C. Above the glass transition temperature, the thermal coefficient of expansion increases dramatically with a corresponding decrease in the Young's Modulus. Plastic packages are not suitable for 200°C operation due to potential failure modes associated with the packaging material and the internal wire bonds. The N-MOSFET, IGBT and MCT were custom packaged by Harris Semiconductor in hermetic metal packages for testing.

TABLE 1. Devices used in Study

Device Type	Device Number	Current Rating	Voltage Rating
NPN	2N6032	50A	150V
N-MOSFET	RFH75N05E	75A	50V
IGBT	TA9796	34A	1000V
MCT	MCTA60P60	60A	600V

Chapter 3. DEVICE MEASUREMENTS

During the testing, each device was mounted to a heat sink in a Delta Design 9032 test chamber. Teflon insulated, silver plated copper wire was used for electrical connection to the devices under test. Under software control the test chamber was brought to within +/-0.2°C of the desired test temperature and held for 5 minutes. This allowed the heat sink and device to achieve the ambient chamber temperature. The individual test was then performed and the temperature raised. The test temperatures ranged from 20°C to 200°C in 10°C increments.

The test equipment set-up is shown in Figure 8. The test equipment was controlled by a Tektronics PEP 301 80386-16 personal computer through a general purpose interface bus (IEEE 488). The software used to control the temperature tests were Tektronics' GURU II and Microsoft's GWBASIC and Quick Basic. Each piece of test equipment was given a GPIB name and address using the program IBCONF. The software address and programming protocol of each device were confirmed by inputting a single line commands using IBSIC software included in GURU II. When it was established that each component of the test system responded correctly, the tests were repeated using GWBASIC and the driver interface software provided in GURU II. The software codes for each of the semiconductor device parameter measurements were written in Basic.

Tests performed using the TEKTRONIX 371 high power curve tracer utilized pulse current measurements. The pulse (half amplitude pulse width) employed by the curve tracer is 250us +/- 10%, with a rise/fall time of 40μs to 120μs with a repetition rate of 0.25 times the line frequency at power levels of 3kW and 0.5 times the line frequency at power levels of 300W.

Leakage Current

Data for the BJT collector-emitter leakage was measured by applying a collector-emitter voltage of 80V with a HP6030A power supply, shorting the base and emitter leads and reading the collector current with a TEKTRONIX DM5120 programmable digital multimeter. The collector-emitter leakage current, I_{ces}, of the BJT as a function of temperature is plotted in Figure 9. The leakage current increases with increasing temperature after an initial plateau. This plateau is attributed to other parasitic leakage paths in the device which are temperature independent and dominate at the lower temperatures. In the portion of the curve not dominated by the parasitic leakage paths (100°C to 200°C) the leakage current was found to double every 12°C as expected.

Collector-emitter leakage current for the IGBT was performed using the same test circuitry as the BJT with a V_{ce} voltage of 400V. The MOSFET measurements were made with V_{ds} = 50V and the gate connected to the source. The IGBT and MOSFET test results are plotted in Figure 9. An attempt to reduce the MOSFET drain-source leakage current by applying a negative 5V gate-source voltage which reduced the leakage current by a factor of two over the entire temperature range.

Measurements of the off-state leakage current of the MCT versus temperature were made with anode-to cathode voltages of 500V and 300V and a gate to anode voltage of 10V. The 500V measurement lead to breakdown and destruction of the device at temperatures near 200°C. (See Breakdown Voltage section) The MCT leakage data for an anode-to-cathode voltage of 300V is plotted in Figure 9.

The emitter-base leakage current of the BJT was measured by applying emitter-base voltages of 1 to 7V using a PS5010 programmable power supply while measuring the leakage current using a DM5120 programmable digital multimeter. The device again demonstrated a saturation of leakage current in the lower temperature range, Figure 10, with a doubling of leakage current every 10-12°C. Breakdown of the emitter-base junction occurred at V_{eb}=7V near room temperature, but was soon overcome by the increase in the junction breakdown voltage with increasing temperature.

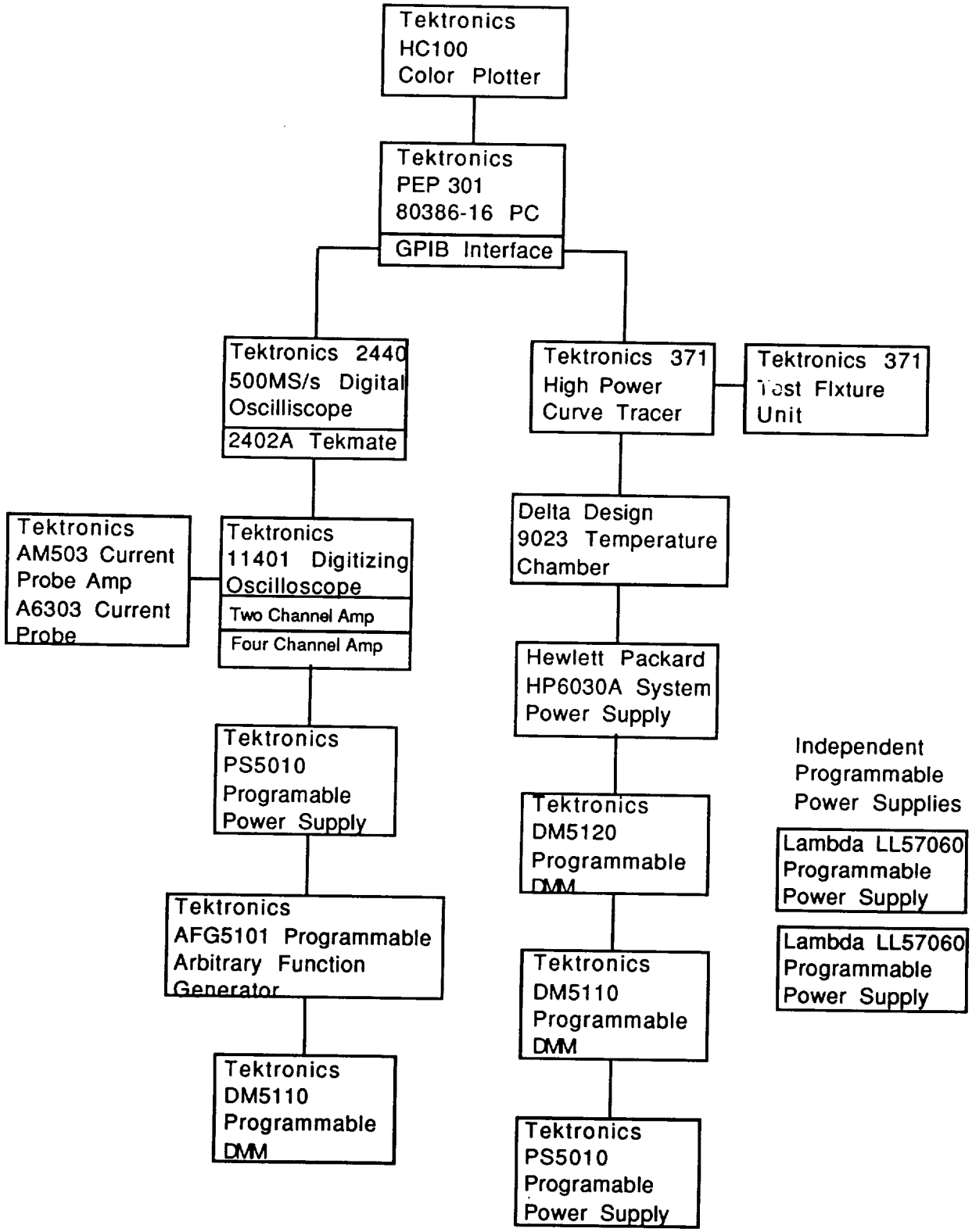

Figure 8. Test Equipment Used in High Temperature Characterization

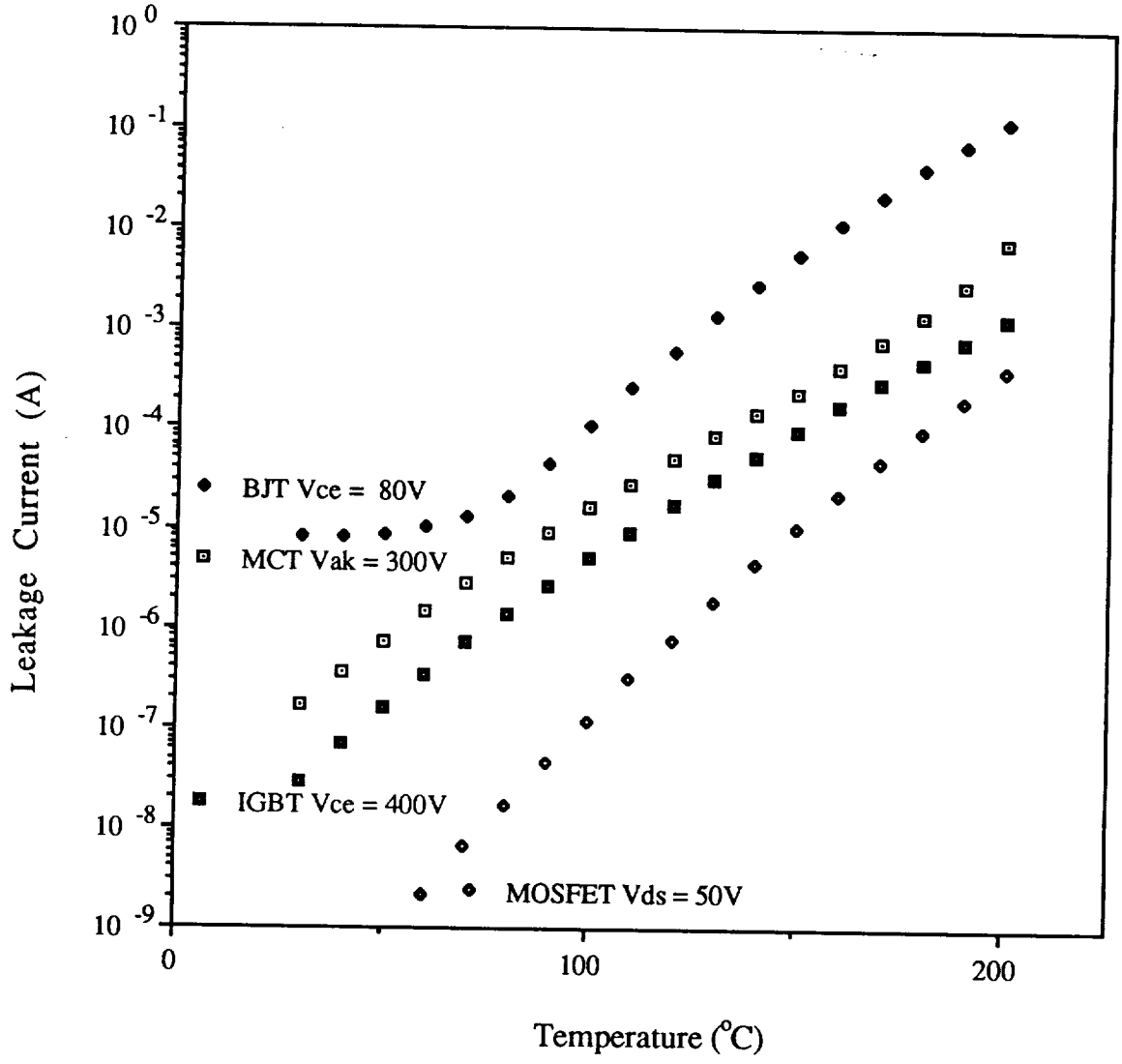

Figure 9. Collector (Drain, Anode) Leakage Current Versus Temperature.

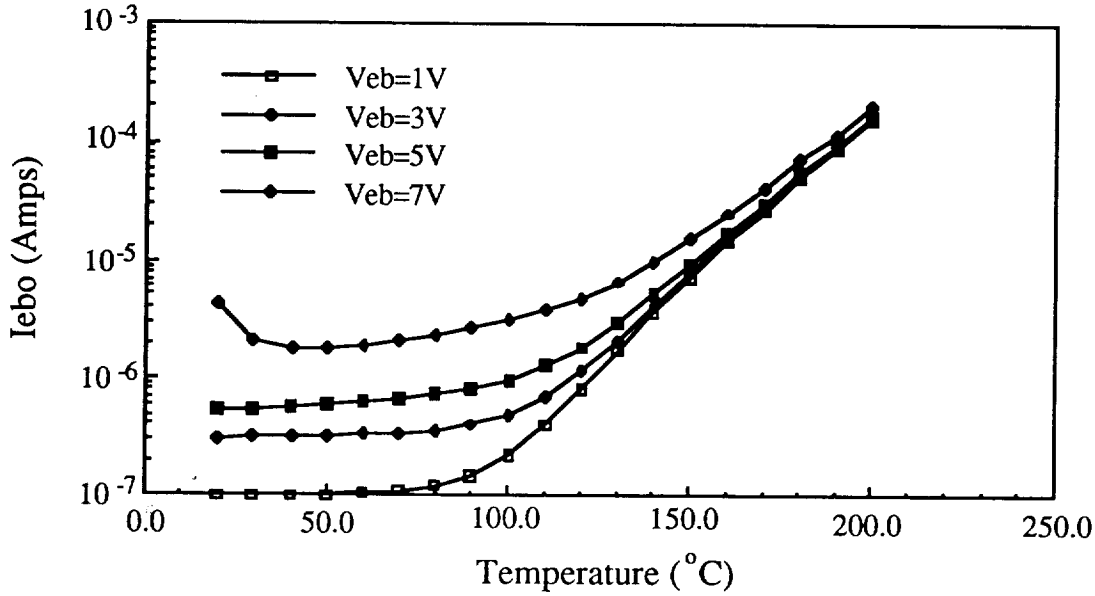

Figure 10. Emitter-Base Leakage Current Versus Temperature.

Analysis of the gate-source and gate-emitter leakage, for the MOSFET and IGBT respectively, indicated currents of less than 10nA (this data was lost in the noise resolution of the measurement equipment) at all temperatures for all gate voltages).

While the leakage currents did increase with increasing temperature, the leakage currents at 200°C were still 3-5 orders of magnitude lower than the typical on-state currents (milliAmps vs 30-75 Amps). No anomalies occurred in the data above 150°C with the leakage currents doubling every 10°C to 12°C. The rate of increase in leakage current was somewhat lower for the IGBT and the MCT.

Saturation Voltage And On-Resistance

The saturation voltage of the bipolar transistor was measured at a forced Beta of 10 (using a base current I_b=5A and limiting the collector current to I_C=50A). Figure 11 shows the measured collector-emitter saturation voltage for the BJT. There is a slight increase in saturation voltage with temperature (1.7mV/°C).

To measure the $V_{ce_{sat}}$ of the IGBT, a gate-to-emitter voltage, V_{ge}, of 10V was applied. The collector-emitter voltage was then acquired at a collector current of I_C=30A, Figure 11. Because of the MOS gate of the IGBT, the base current of the bipolar structure could not be controlled as in the BJT, so unlike the bipolar devices studied, the IGBT shows a negative $V_{ce_{sat}}$ temperature dependence above 80°C.

The MCT's on-state voltage drop was measured with the gate-to-anode voltage (Vga) was set to -10V and the anode-to-cathode current was set to 60A. Figure 11 shows the results of the on-state voltage drop versus increasing temperature as expected.

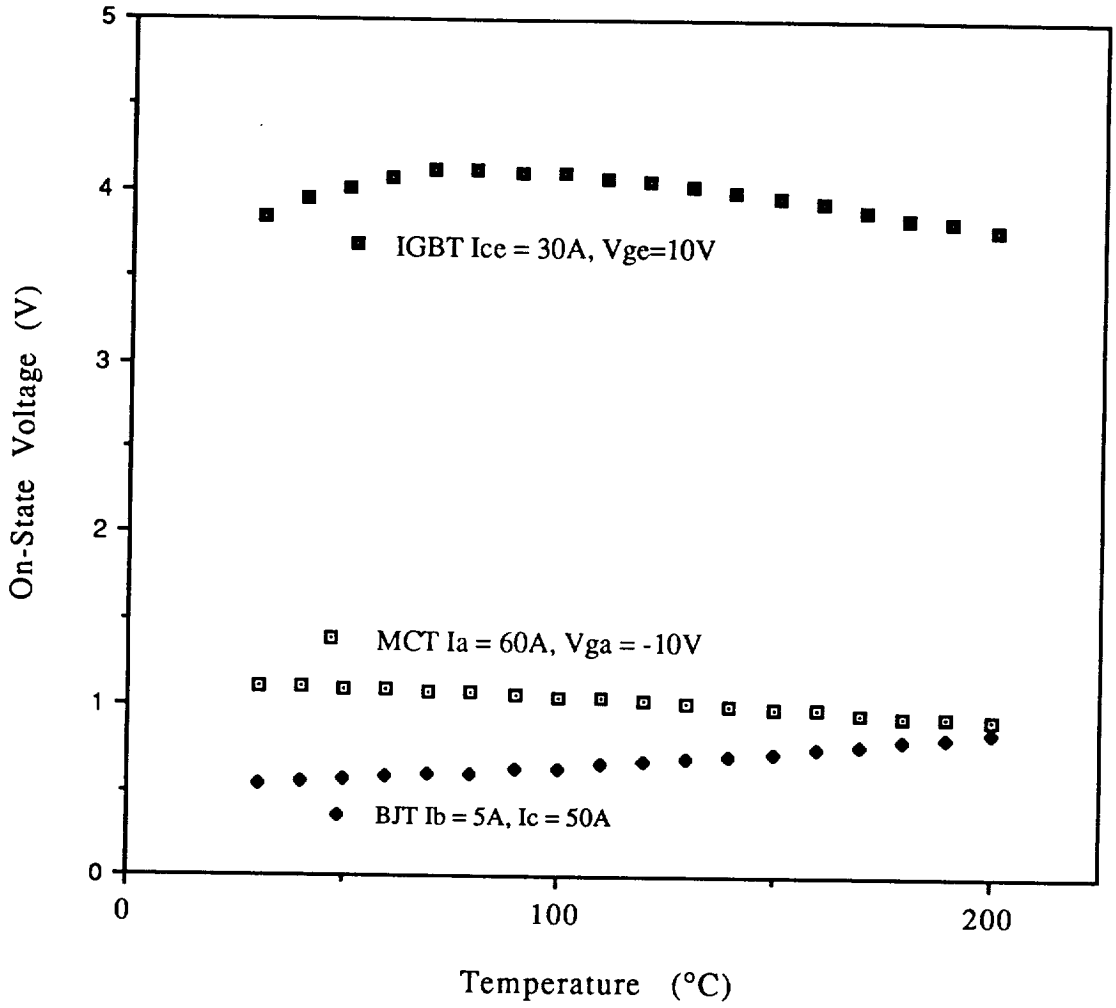

Figure 11. On-State Voltage Of The BJT IGBT And MCT Versus Temperature.

On-resistance ($R_{ds_{on}}$) and RMS drain current determine the power loss in a MOSFET. Using the TEKTRONIX 371 curve tracer with a pulsed drain current, I_d, of 75A and a constant V_{gs}-V_T (using the temperature dependent threshold voltage V_T shown later) of 6.5V, the data in Figure 12 was measured. R_{ds} increases approximately 50μΩ/°C. The increase in R_{ds} was expected due to the decreasing carrier mobility with increasing temperatures as previously discussed.

Breakdown Voltage

The variation in breakdown voltage for the devices were obtained using a TEKTRONIX 371 curve tracer. For the MOSFET, the gate was shorted to the source and the I_{ds} versus V_{ds} transfer characteristic were acquired and used to determine the breakdown voltage plotted in Figure 13. The breakdown voltage increase of about 7.6% per 100°C. The IGBT breakdown voltage data in Figure 14 also shows an increase of about 7.6% per 100°C.

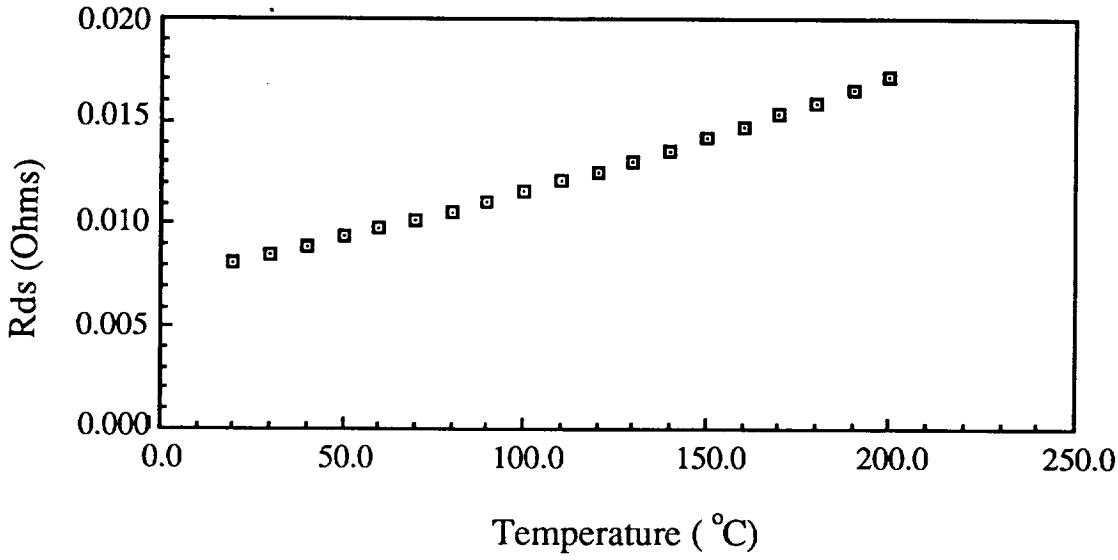

Figure 12. On-Resistance of N-MOSFET Versus Temperature.

Breakdown voltage tests for the bipolar device, Figure 13, display an unexpected drop in V_{ces} breakdown voltage in the temperature region above 140°C. These curves are typical of several devices tested. Because the device base and emitter are shorted externally for this test, it is believed that the increases in the internal base resistance with temperature and the increased leakage with temperature could allow the device to begin to turn-on (internal transistor action) without an applied base current lower the breakdown voltage in the higher temperature range.

The MCT requires an applied voltage to hold the device off. A 10V gate voltage was applied for the breakdown measurements. Figure 13 shows the results of the breakdown versus temperature measurement. When forward biased and held in the off state by a positive gate-to-anode voltage, the collector-base junction of the npn transistor in the thyristor structure is the only reverse biased junction blocking the anode-to-cathode voltage. The transistor action of the npn transistor multiplies the current through this junction. Therefore, it is expected that the forward breakdown voltage of the MCT would decrease as temperature increases. This decrease is evident in the results of the measurement. Arther, et. al. have recently reported similar results for P-MCT's [9].

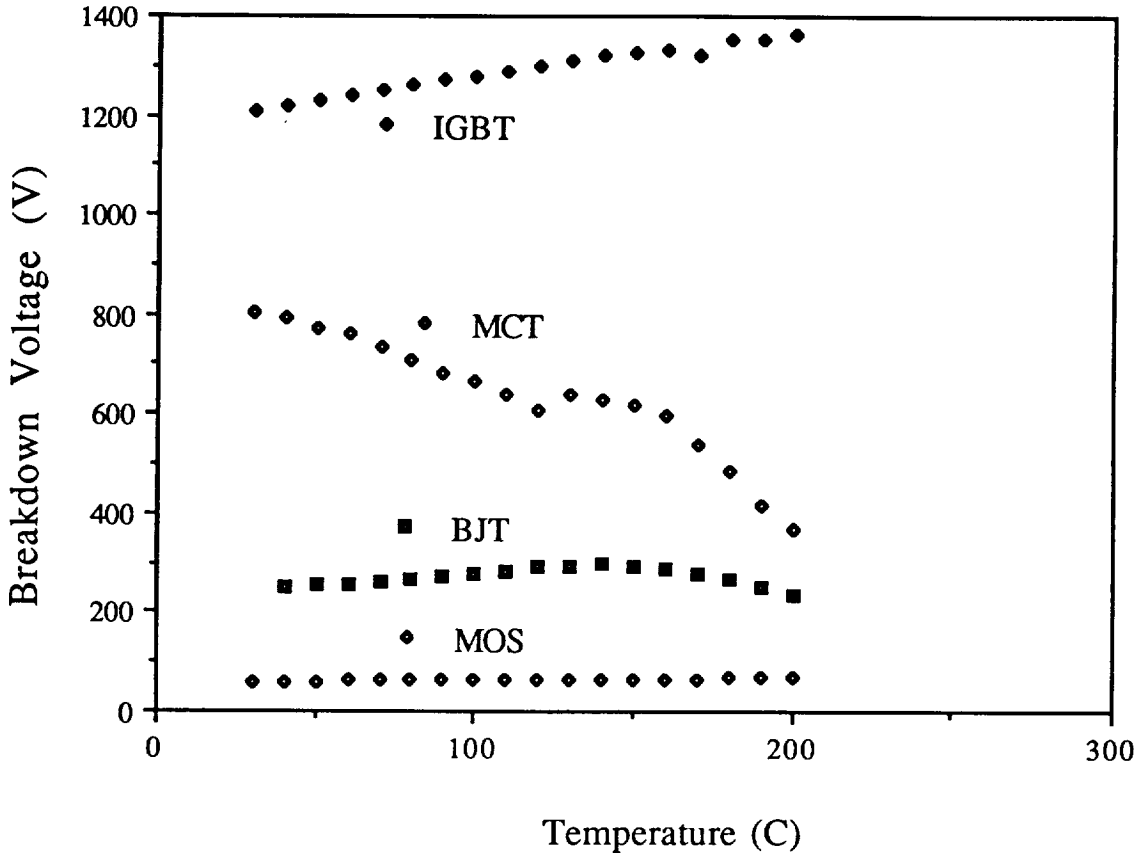

Figure 13. Break-Down Voltage Versus Temperature.

Dc Beta In The BJT

The DC current gain of the bipolar transistor was measured using a TEKTRONIX 371 curve tracer at a constant V_{CE} of 2.6V. Figure 14 shows a typical set of curves for this test. These curves show the peak in Beta at low current levels as the generation and diffusion currents dominate the emitter-base junction, and the Beta "fall-off" at high current levels due to the Webster effect. At high current levels the temperature dependency is less significant as predicted in a previous section.

Threshold Voltage In The MOSFET

Using a TEKTRONIX 371 curve tracer at a V_{ds} of 5V, the transfer characteristics for the MOSFET were obtained. The data was then plotted as $I_d^{1/2}$ versus V_{gs} (Figure 15) and the threshold voltage was determined as the straight line intercept with the I_d=0A (V_{gs}) axis. Figure 16 presents the threshold voltages obtained as a function of temperature. The data has a slope of -4.5mV/°C. At 200°C, the threshold voltage is still sufficiently high for easy control of the transistor.

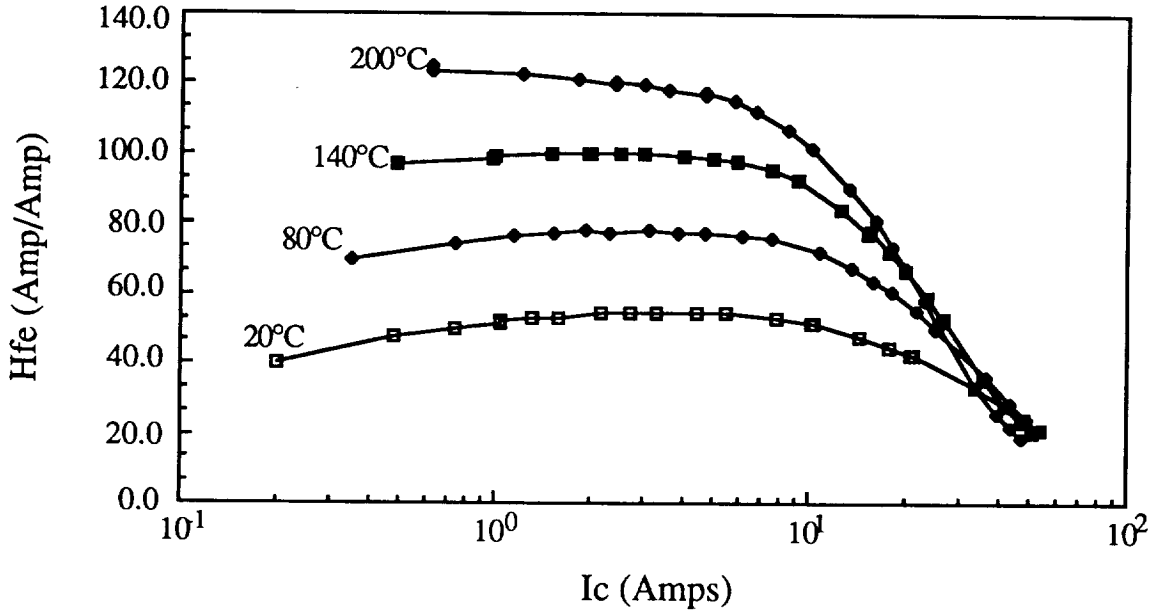

Figure 14. DC Beta Versus Temperature.

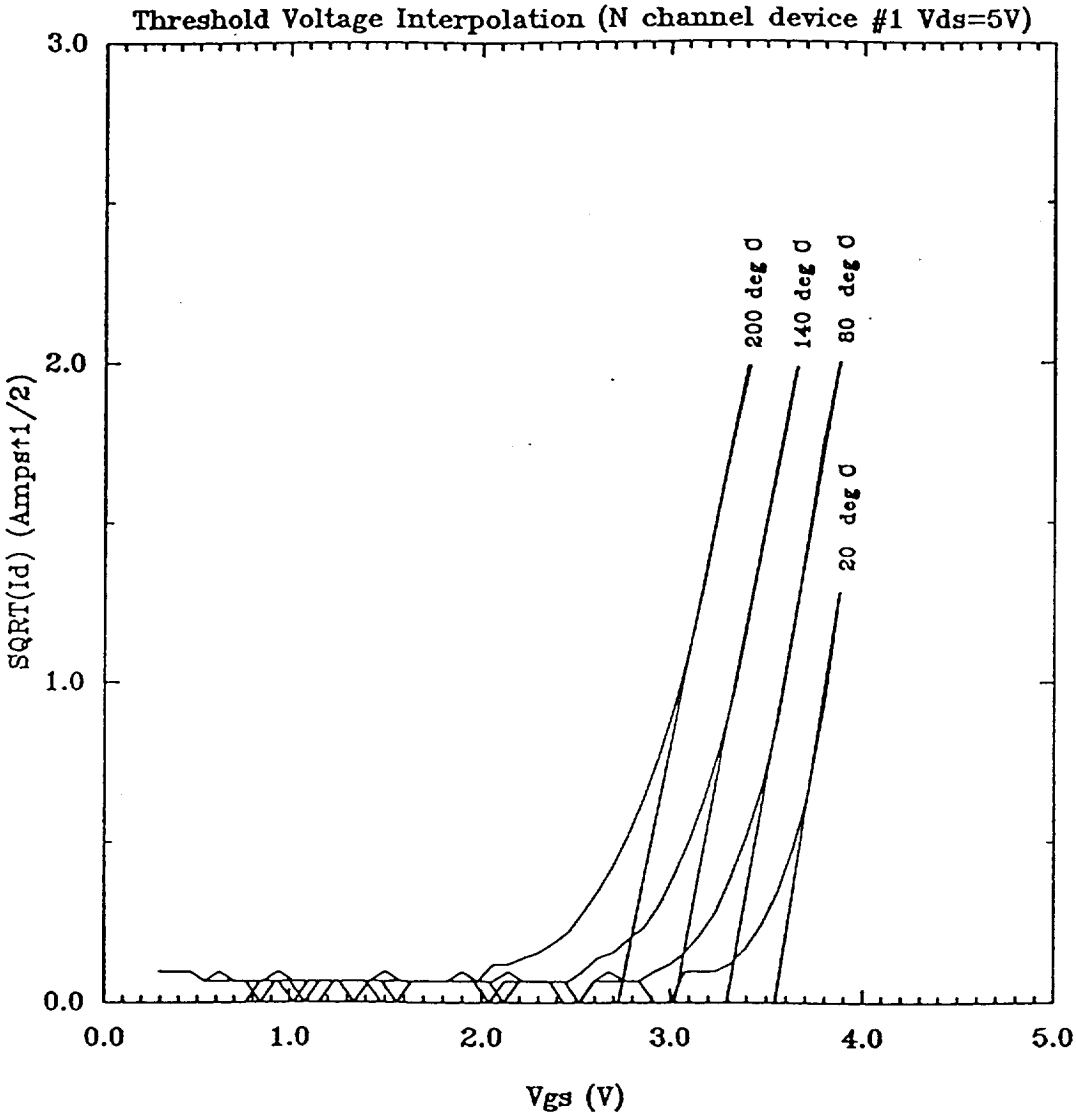

Figure 15. Square Root of Id Versus Vgs

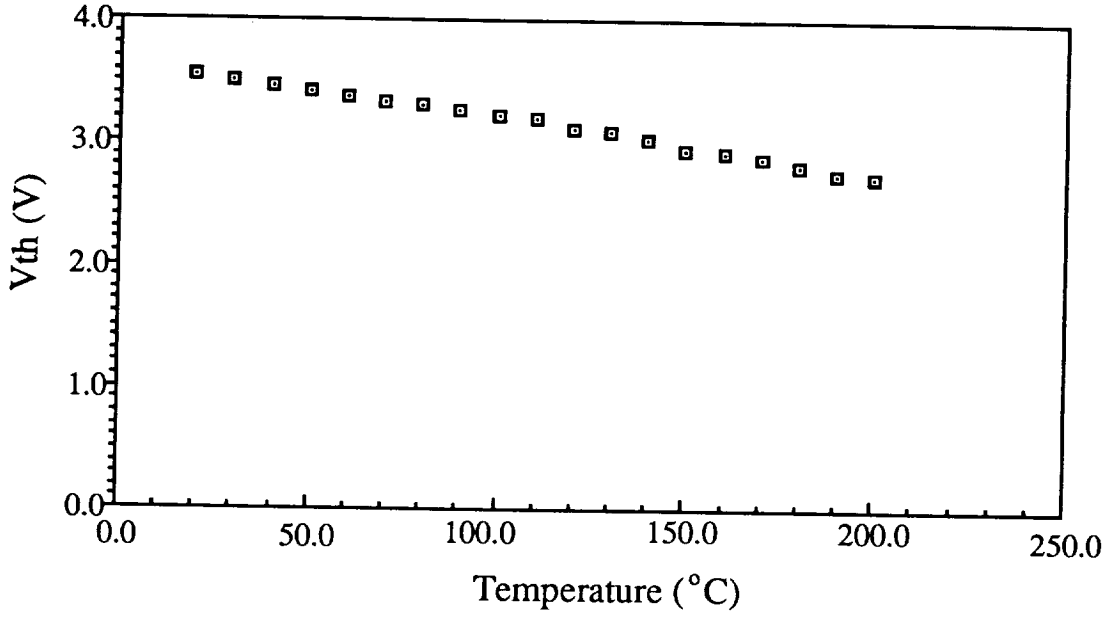

FIGURE 16. MOSFET Threshold Voltage Versus Temperature (V_{ds}=5V).

SWITCHING CHARACTERISTICS

MOSFET

Measurement of switching times proved to be quite challenging due to parasitcs associated with the wiring necessary to connect drive circuitry to the device-under-test in the oven and the difficulty in obtaining a purely resistive load. The gate drive circuit for the N-MOSFET switching tests is shown in Figure 17.

The load was fabricated by a parallel combination of 10Ω, 7W composite power resistors which were placed in the oven with the device-under-test. This produced a load with a low temperature coefficient of resistance, but sizable inductances (R_L = 0.67Ω, 0.21μH as measured with an HP 4275A Multi-frequency LCR meter at 10MHz). Twisted pair leads (<8 inches) connected the device to the gate drive circuitry (driven by the Tektronics AFG5101 Arbitrary Function Generator) and the load to the voltage supply (HP6032). Output waveforms were captured using the Tektronics 2440 oscilloscope, and the AM503 current amp with the A6303 current probe. Tests were performed using 100μsec pulses to avoid junction heating. Figures 18-21 show typical N-MOSFET turn-off and turn-on waveforms at 20°C and 200°C, for V_{DS} = 30V and I_D = 45A (Channel 1 - drain-to-source voltage @ 5V/div, Channel 2 - drain current @ 10A/div). Ringing in the turn-off voltage waveform, Figures 18 and 20, was a result of natural oscillation between the R, L, of the load and the C_{gd} of the N-MOSFET. A 25Ω gate resistor reduced the ringing in the output, but increased the rise and fall times. The graph of switching time

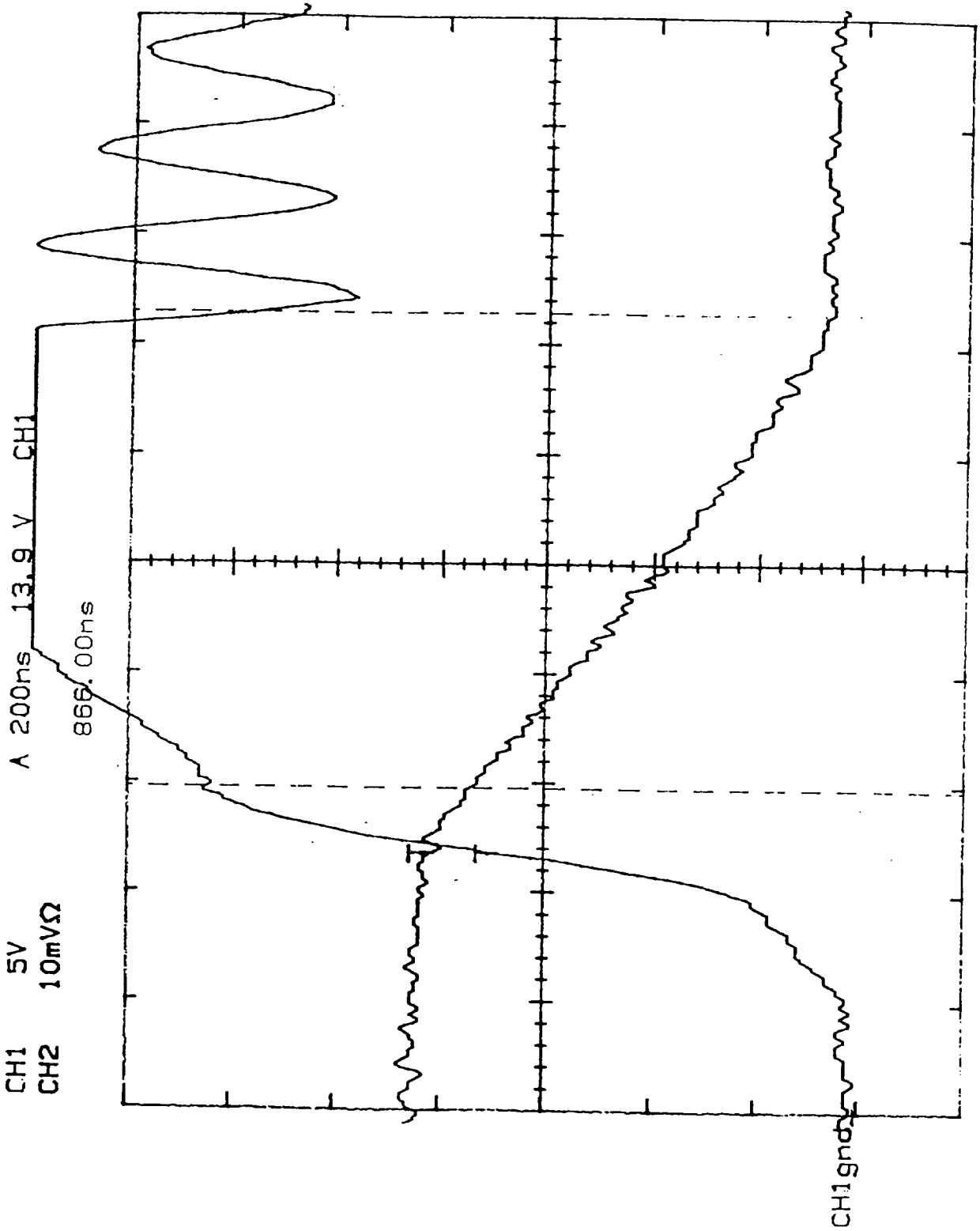

Figure 18. N-MOSFET Turn-off Waveforms at 20°C. Channel 1 is the Drain-to-Source Voltage Displayed at 5V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 200ns per Division.

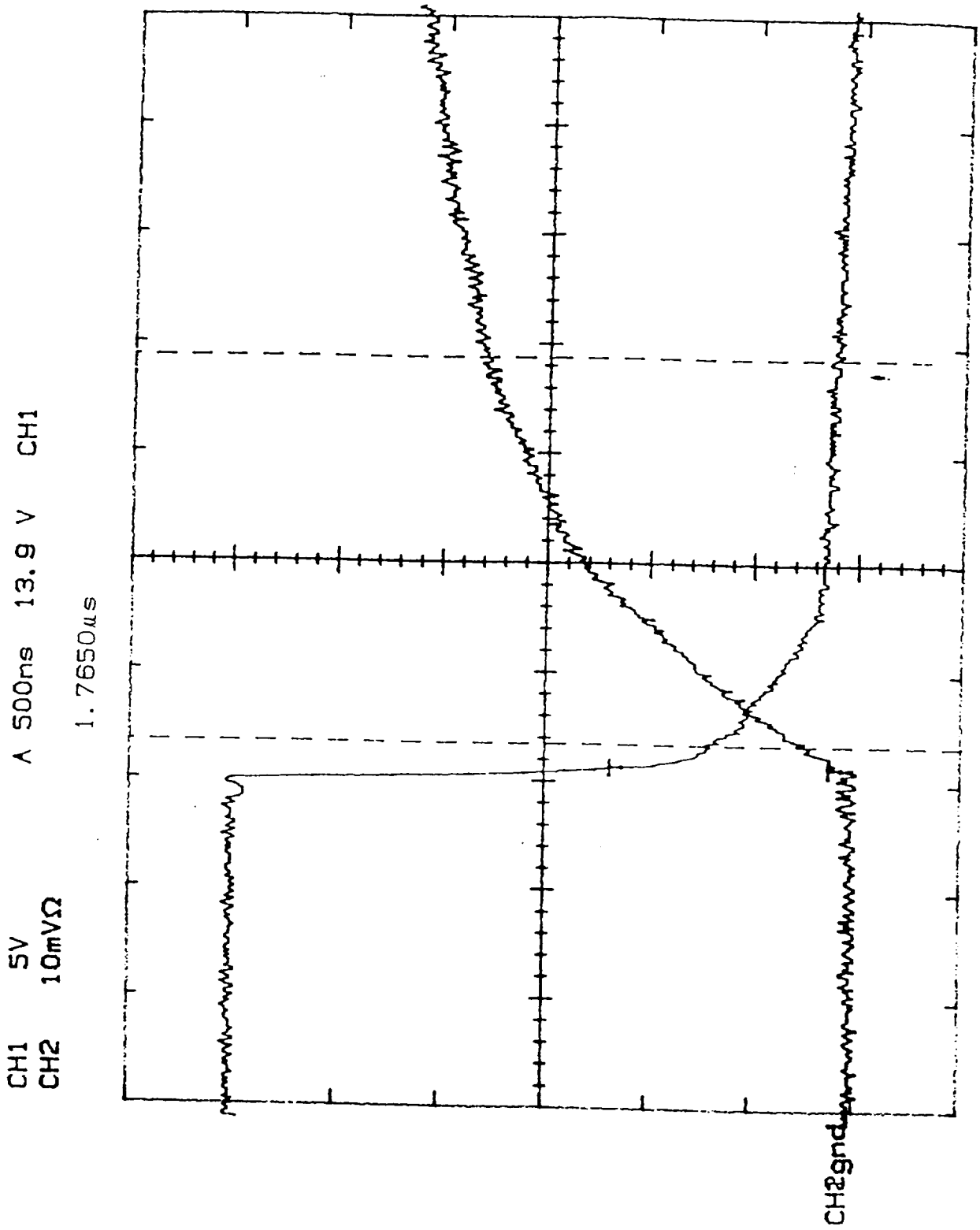

Figure 19. N-MOSFET Turn-on Waveforms at 20°C. Channel 1 is the Drain-to-Source Voltage Displayed at 5V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 500ns per Division.

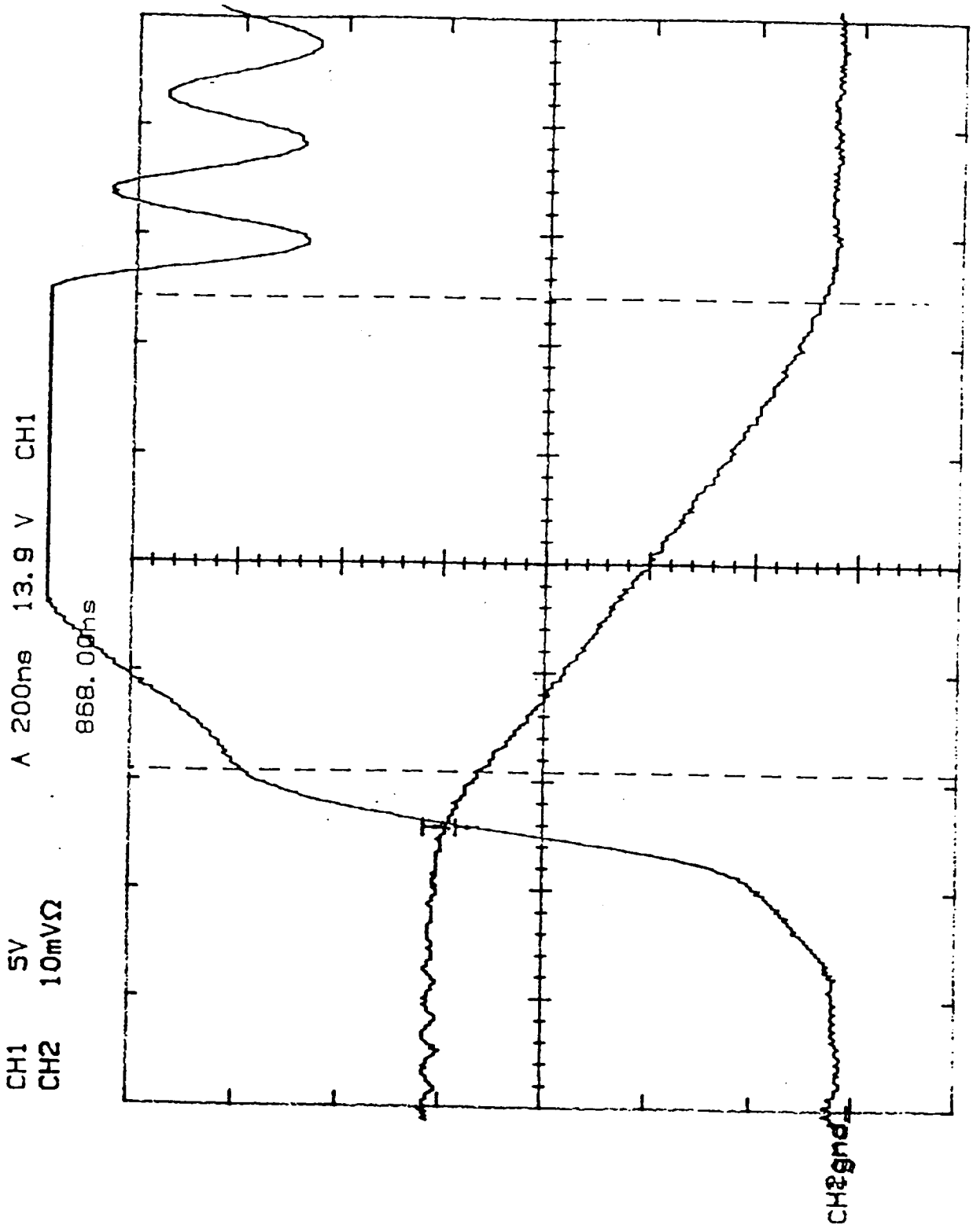

Figure 20. N-MOSFET Turn-off Waveforms at 200°C. Channel 1 is the Drain-to-Source Voltage Displayed at 5V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 200ns per Division.

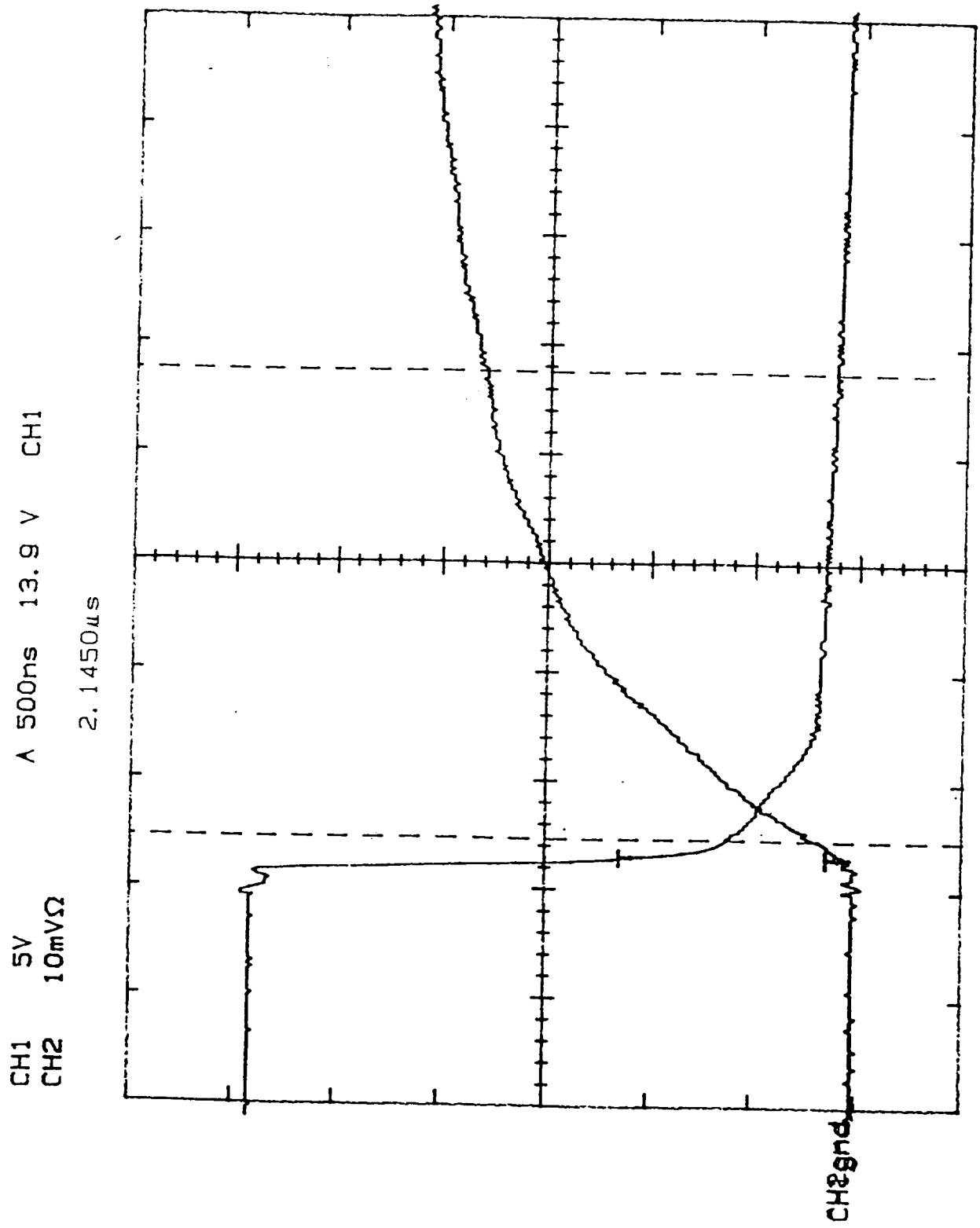

Figure 21. N-MOSFET Turn-on Waveforms at 200°C. Channel 1 is the Drain-to-Source Voltage Displayed at 5V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 500ns per Division.

versus temperature, Figure 22, shows an almost flat response to temperature, but with switching times much higher than specified by the manufacturer. The 0.67Ω load used in the test has a time constant , t_{RL} = 316ns, which results in a 10-90% time of 694ns. This value contributed heavily to the room temperature V_{DS} fall time of 620ns which is more than an order of magnitude longer than the

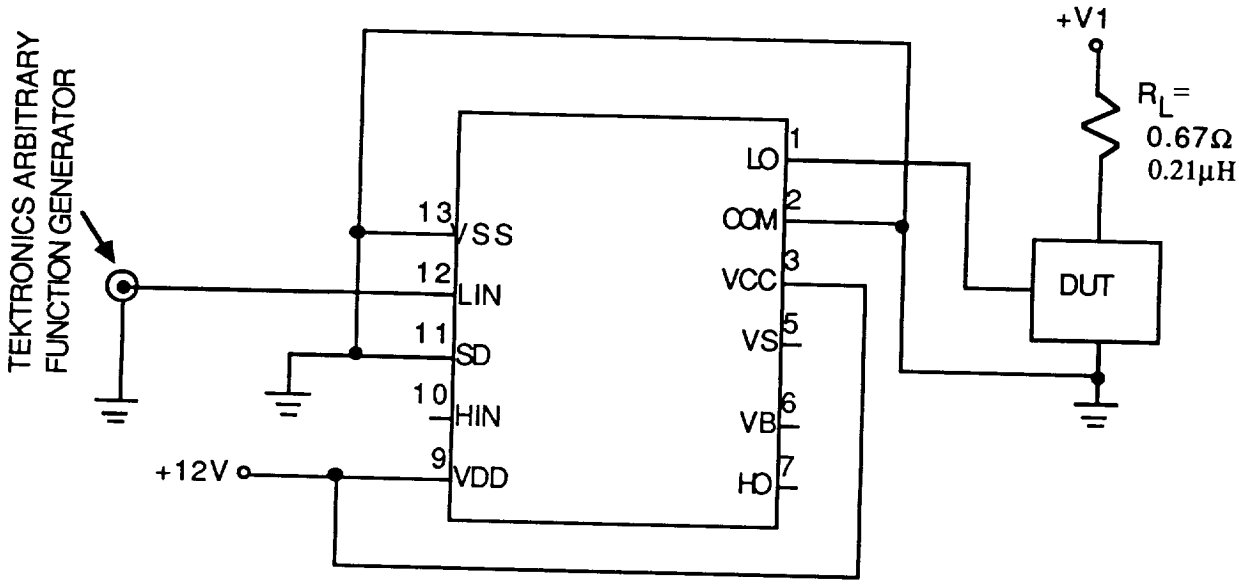

Figure 17. N-MOSFET Switching Test Driver Circuit

manufacturer's specified typical fall time of 17ns. In addition to the RL time constant of the load, drive limitations of the IR2110 and the charge-transfer characteristics of the RFH75N05E also contribute to the slow switching time.

As in most FET's, the input impedance of a power MOSFET consists of a high input resistance in parallel with an equivalent input capacitance. The input capacitance includes the gate-to-source, C_{gs}, and the gate-to-drain, C_{gd}, capacitance. Due to the Miller effect on C_{gd}, the input capacitance of the MOSFET is not well-defined. The effects of the change in the input capacitance can be seen in the normalized charge transfer characteristics of the RFH75N05E MOSFET, Figure 23. Each of the V_{GS} curves can be viewed as having three separate regions of turn-on or turn-off operation. In the first region of turn-on, the V_{GS} curve is linear, the gate voltage has risen to a level where there is drain current conduction. During this period, the gate potential is in the pre-threshold region, and charging the equivalent input capacitance, C_{gd}, thus the slope is relatively constant. The rate of charging in this first region directly affects the turn-on delay. In the second region, turn-on is complete when the drain voltage has switched 90%. There is an abrupt increase in the input capacitance, identified by the flattening of the gate voltage curve. As the MOSFET turns on, the Miller effect becomes dominant. C_{gd} and C_{gs} being depletion dependent are thus voltage dependent and change rapidly in this region. In the third region, since C_{gd} is depletion dependent, its capacitance rises dramatically as the voltage between drain and gate diminishes, and changes polarity when V_{DS} drops below V_{GS}. As C_{gd} rises, the Miller capacitance increases even more rapidly, despite the decrease in voltage gain (dV_{DS}/dV_{GS}). The increasing Miller capacitance

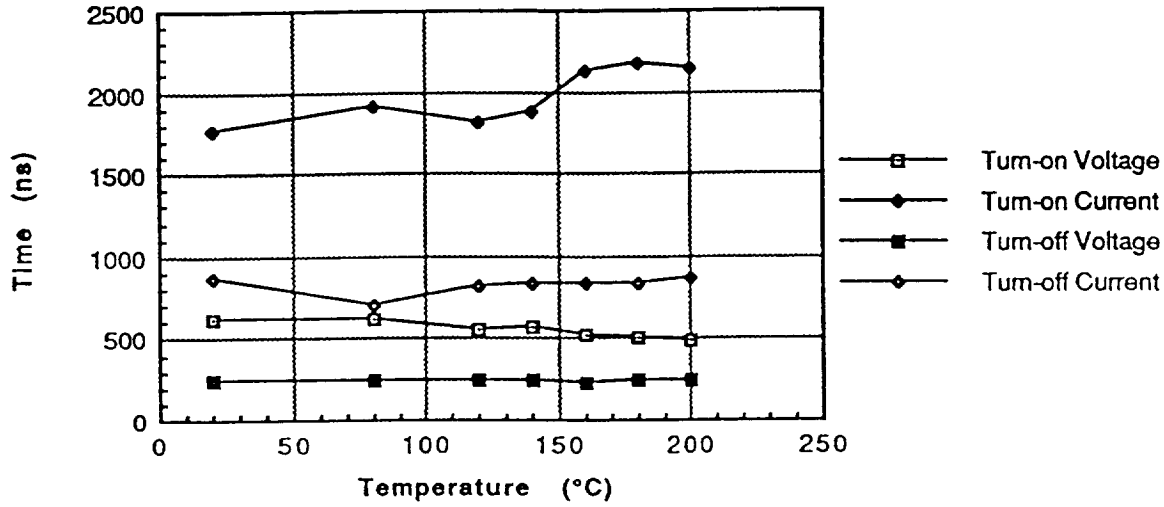

Figure 22. Resistive Switching Times for N-MOSFET as a Function of Temperature (R_L = 0.67Ω, 0.21μH)

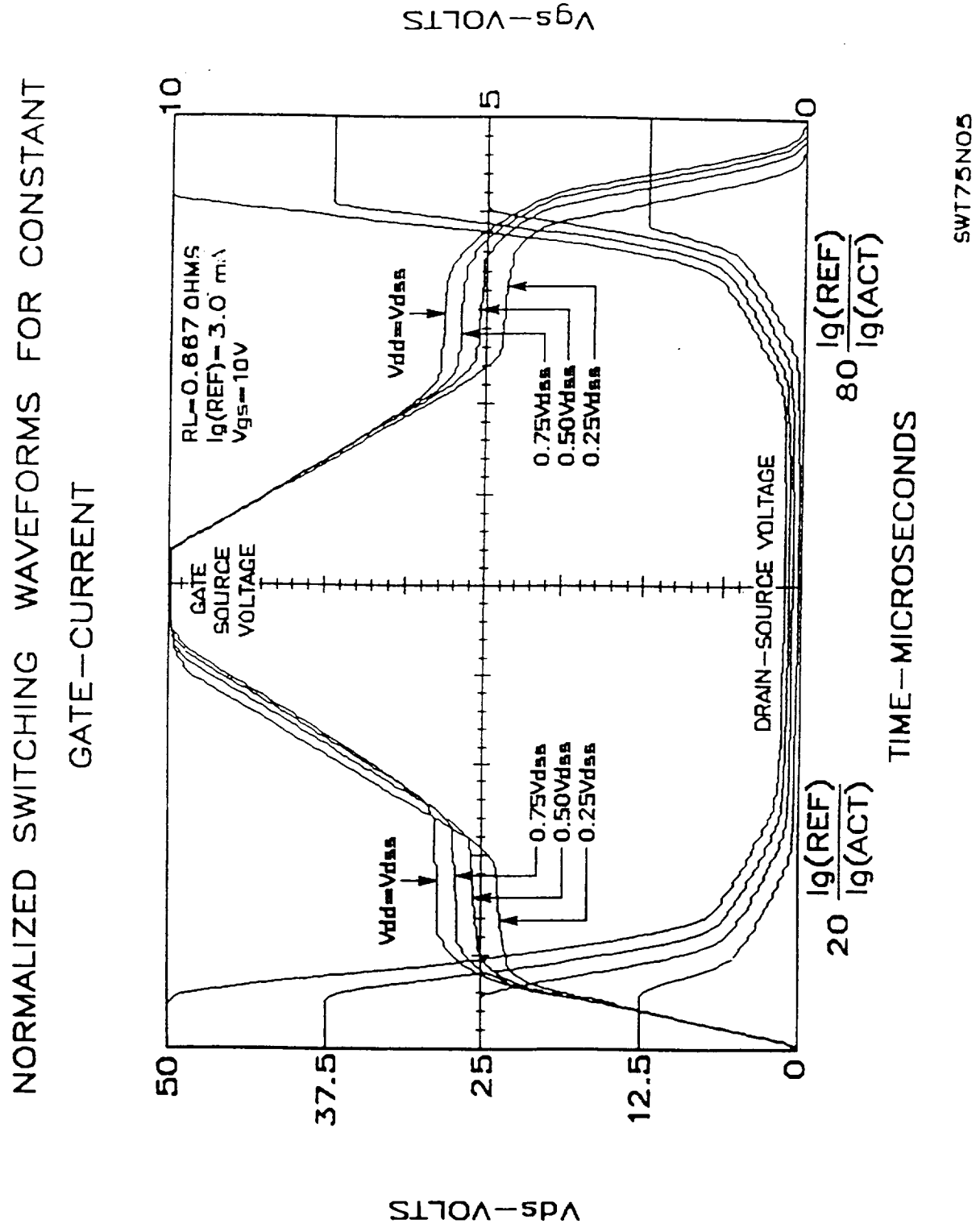

Figure 23. Normalized Switching Waveforms for Constant Gate-Current [ref].

keeps the gate voltage characteristic nearly flat until V_{SAT} is reached. After V_{DS} has decayed to V_{SAT}, the gate then resumes its rise to the imposed gate drive level.

Appropriate gate drive and load resistors could not be designed to adequately test the switching characteristics of the power MOSFET.

Bipolar

The drive circuit for the bipolar switching tests is given in Figure 24. R1 and C1 are selected to produce a 100μs pulse. The IR2110 could not provide the drive current needed by the bipolar transistor.

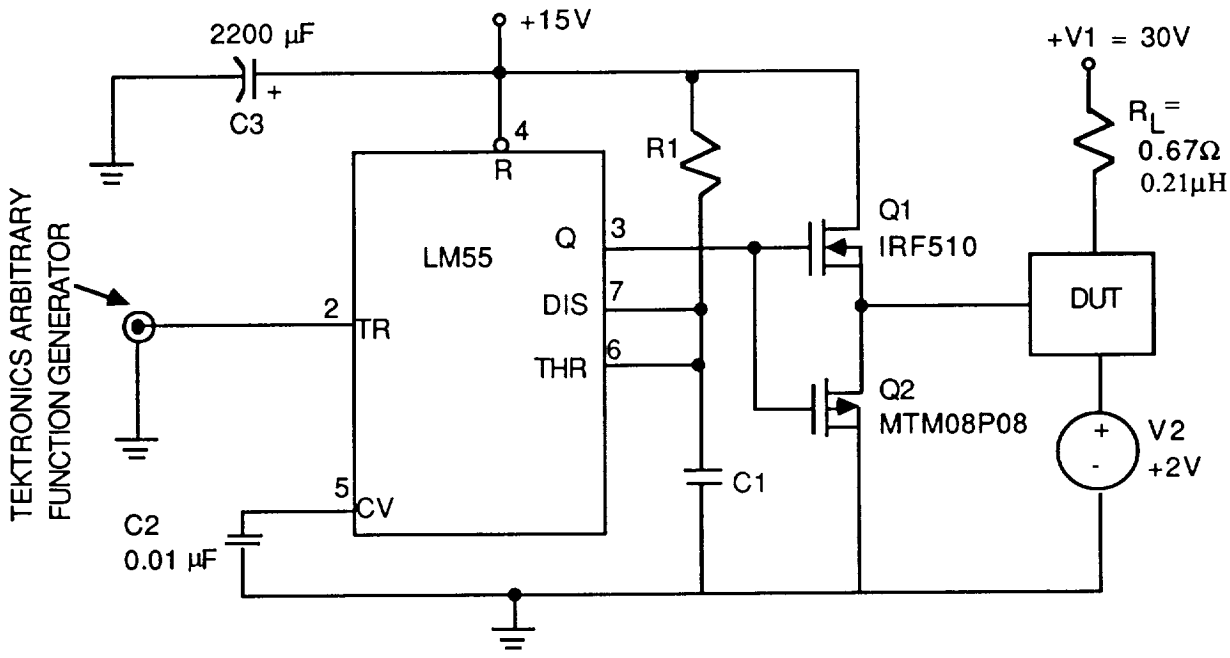

Figure 24. Drive Circuit for the Bipolar Switching Tests

Figures 25-28 show typical BJT turn-on and turn-off waveforms, for V_{CE} = 30V and I_C = 45A. Again ringing in the turn-off voltage, Figure 25 and 27, is due to the inductive component of the load. The maximum specified rise time and fall time for the 2N6032 is 1μs. The values measured at 20°C were a rise time of 180ns and a fall time of 120ns. A graph of the change in switching times for the BJT, Figure 29, indicates a relatively flat response in the turn-off voltage and the turn-on current. Most notable is a 5.6ns/°C increase in the BJT turn-off current and turn-on voltage times.

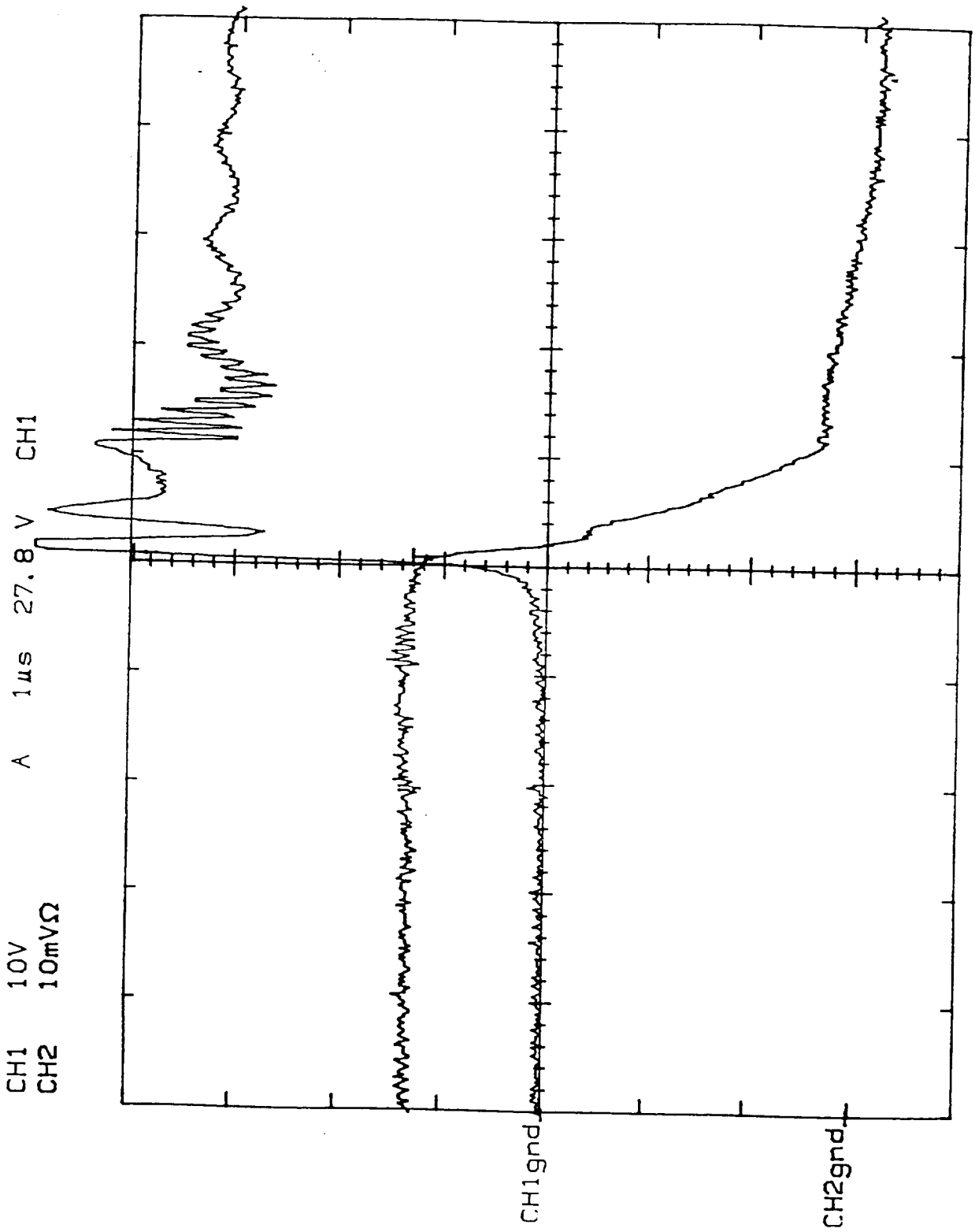

Figure 25. Bipolar Turn-off Waveforms at 20°C. Channel 1 is the Drain-to-Source Voltage Displayed at 10V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 1µs per Division.

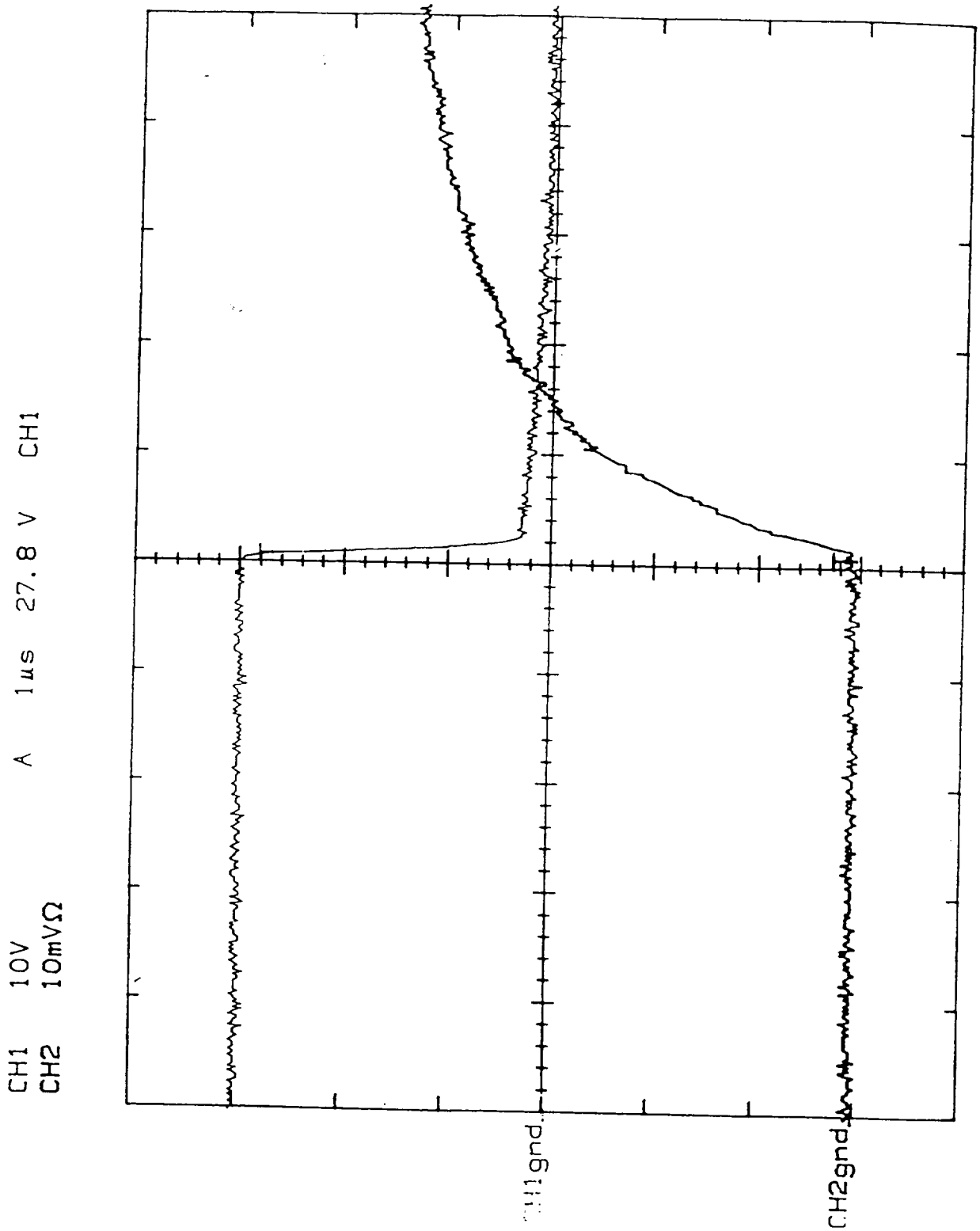

Figure 26. Bipolar Turn-on Waveforms at 20°C. Channel 1 is the Drain-to-Source Voltage Displayed at 10V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 1µs per Division.

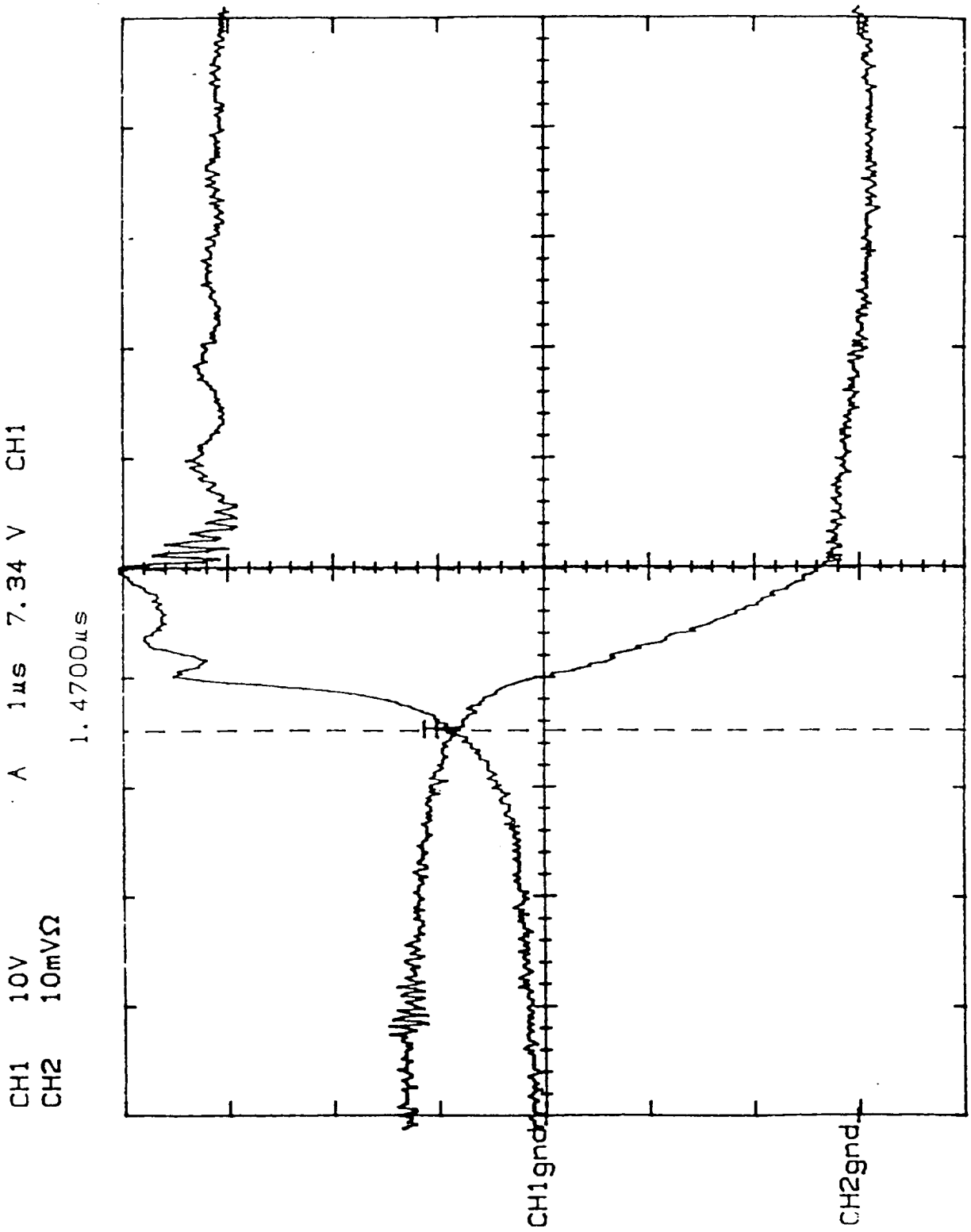

Figure 27. Bipolar Turn-off Waveforms at 200°C. Channel 1 is the Drain-to-Source Voltage Displayed at 10V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 1µs per Division.

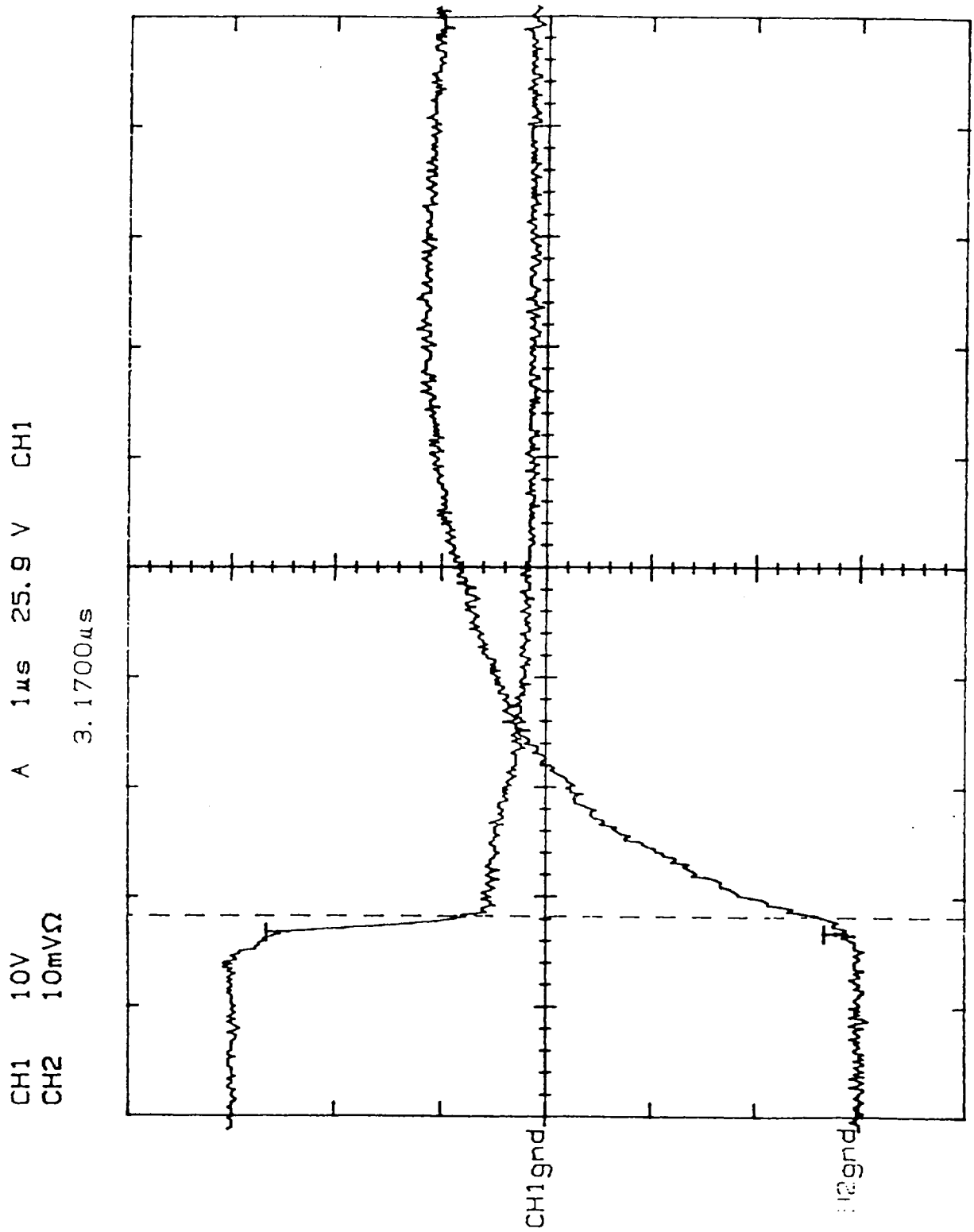

Figure 28. Bipolar Turn-on Waveforms at 200°C. Channel 1 is the Drain-to-Source Voltage Displayed at 10V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 1µs per Division.

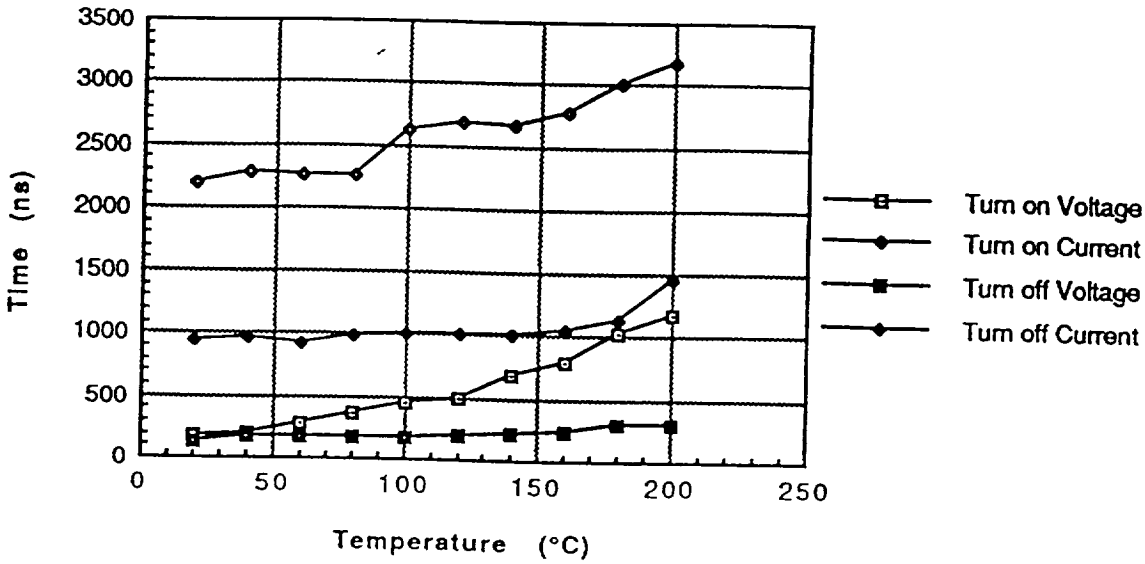

Figure 29. Resistive Switching Times for Bipolar as a Function of Temperature (R_L = 0.67Ω, 0.21μH)

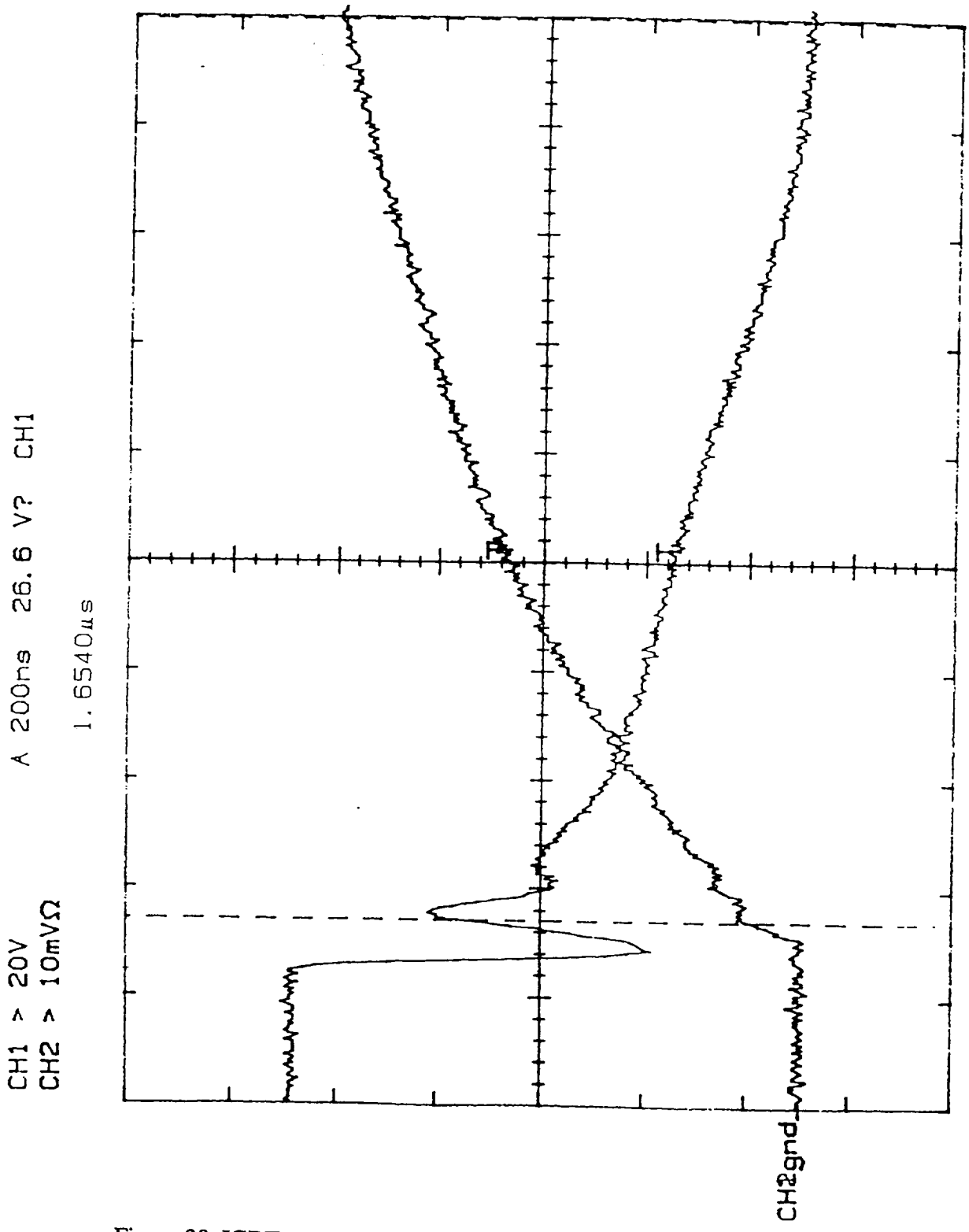

Figure 30. IGBT Turn-off Waveforms at 20°C. Channel 1 is the Drain-to-Source Voltage Displayed at 20V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 200ns per Division.

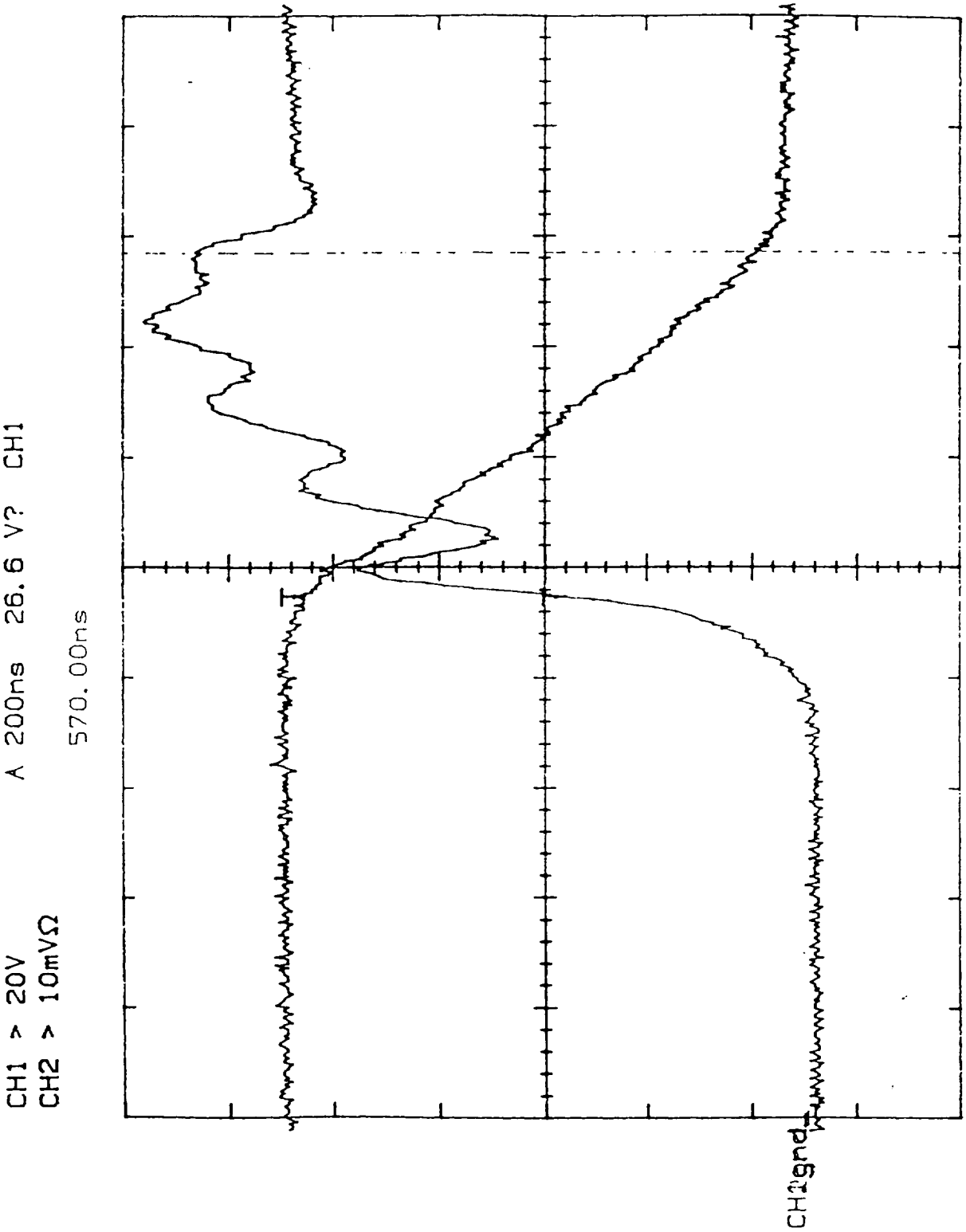

Figure 31. IGBTTurn-on Waveforms at 20°C. Channel 1 is the Drain-to-Source Voltage Displayed at 20V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 200ns per Division.

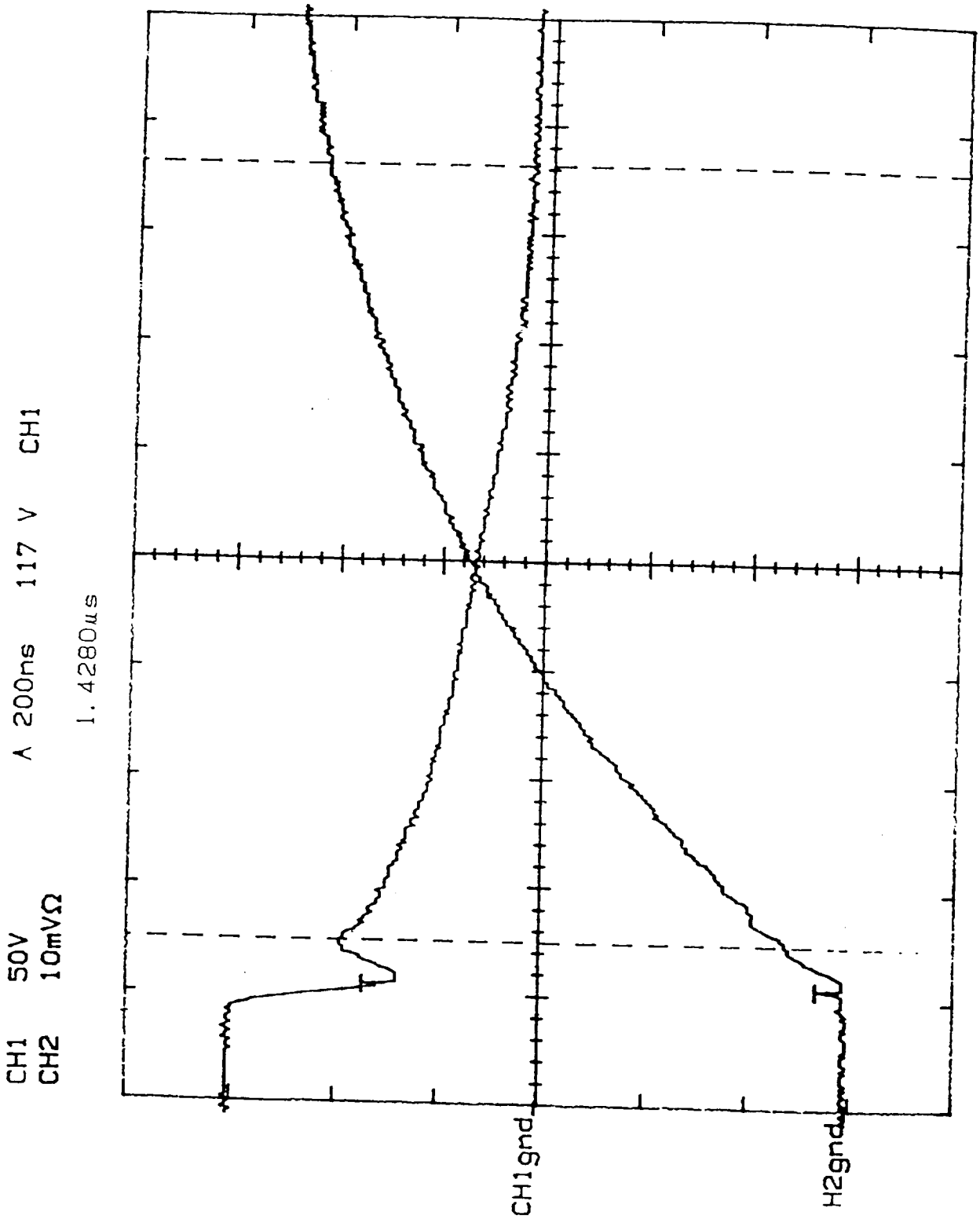

Figure 32. IGBT Turn-off Waveforms at 200°C. Channel 1 is the Drain-to-Source Voltage Displayed at 20V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 200ns per Division.

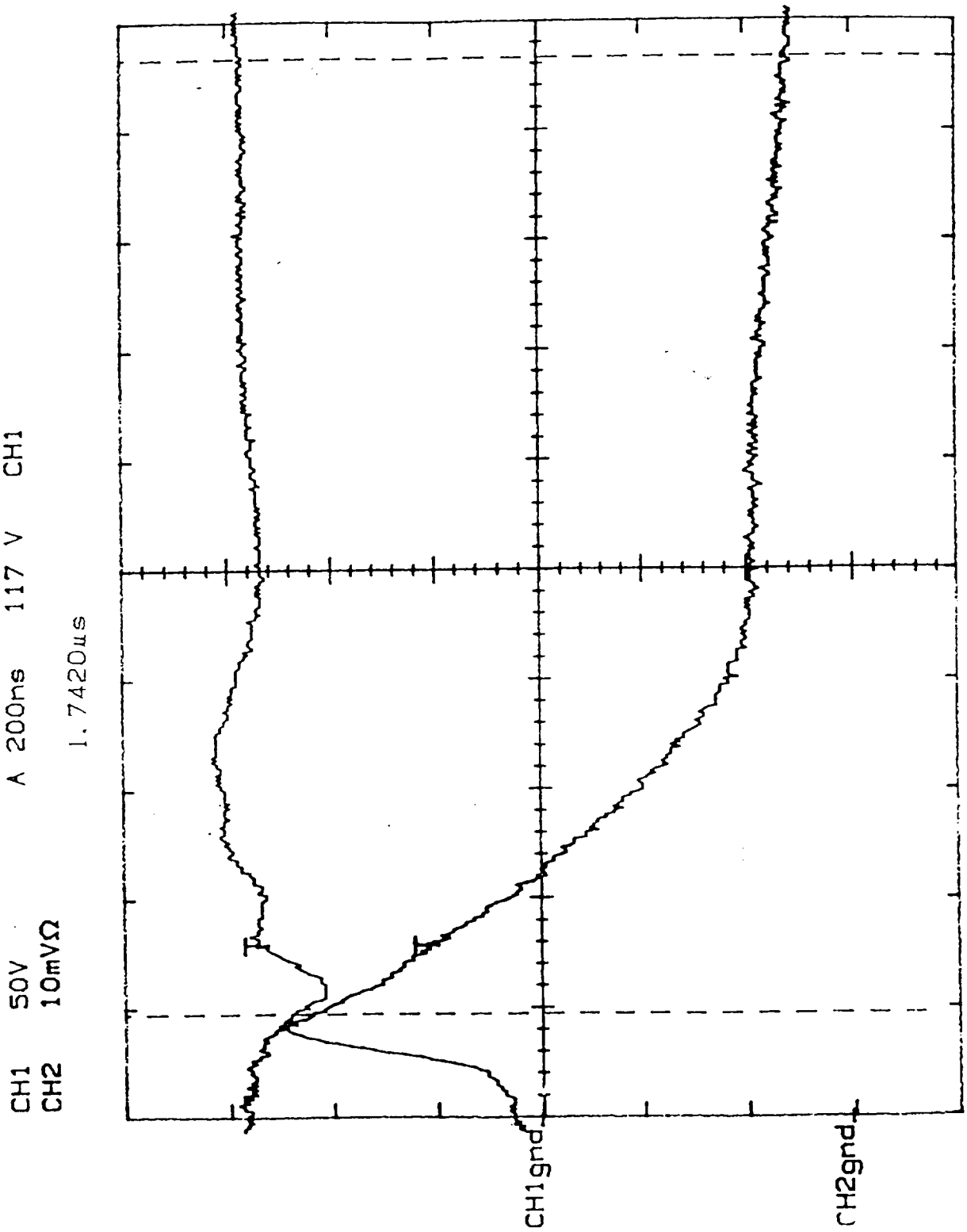

Figure 33. IGBT Turn-on Waveforms at 200°C. Channel 1 is the Drain-to-Source Voltage Displayed at 20V per division. Channel 2 is the Drain Current Displayed at 10A per division. The Time Scale is 200ns per Division.

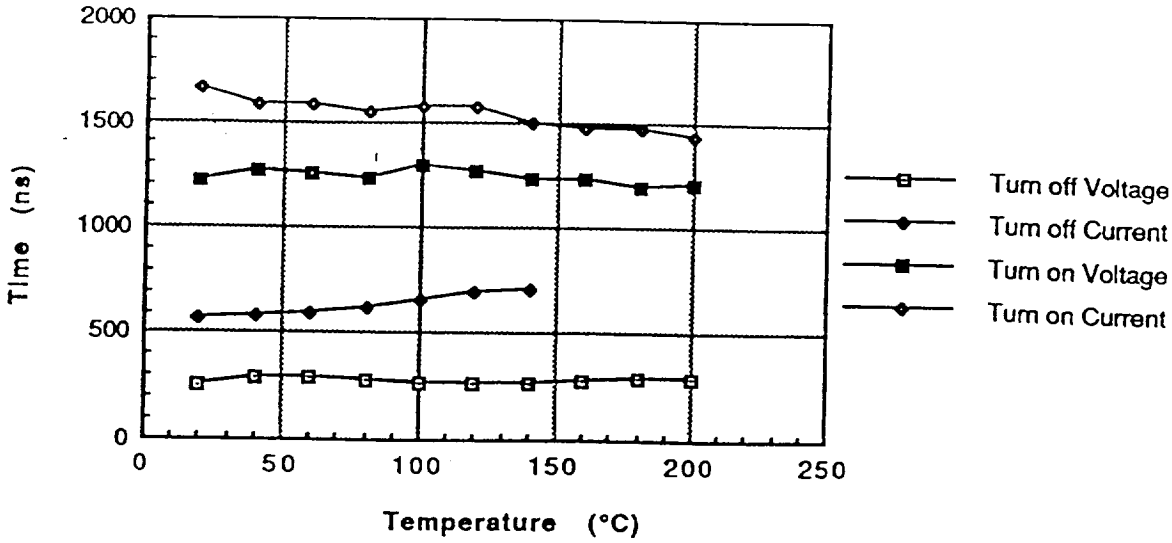

Figure 34. Resistive Switching Times for IGBT as a Function of Temperature (R_L = 5.6Ω, 1.21μH)

IGBT

The BJT drive circuit was used for the IGBT switching tests with the exception that the load resistor was changed to R_L = 5.55Ω, 1.2μH. Figures 30-33 show the IGBT turn-off and turn-on waveforms at 20°C and 200°C, for a V_{CE} =150V and I_C = 30A. Ringing in the turn-off voltage waveforms is again a result of the inductive load. A rise time of 250ns and a fall time of 1.2μs were measured at 20°C. The typical fall time specified by the manufacturer is 1.8μs. The rise and fall times as a function of temperature are presented in Figure 34.

MCT

The test circuit used to measure the MCT switching times is shown in Figure 35. The HP6030 power supply provided a cathode-to-anode voltage of 200V. Two Lambda LLS7060 power supplies provided positive and negative 13V rails for the gate-to-anode drive circuit. An IR2110 gate driver was used to drive the MCT. As in the data sheet test circuit, a diode was used in parallel with the load to protect the MCT. The test conditions used for the data sheet specifications were a 2.5Ω, 50μH load, a gate-to-anode drive of +/- 20V and an anode-to-cathode voltage of 300V. These conditions were not duplicated to reduce stress on the MCT. The data sheet specifications are a current rise time of 0.4μS (typical) and a current fall time of 1.8μS (typical). A resistive load (3.39Ω, 1.040μH) was used for making the switching times versus temperature measurements. This set the on-state current to approximately 60A which corresponds to the maximum average on-state current rating of the MCT. A Tektronix 2440 Oscilloscope was used to measure the anode-to-cathode voltage and to measure the cathode current.

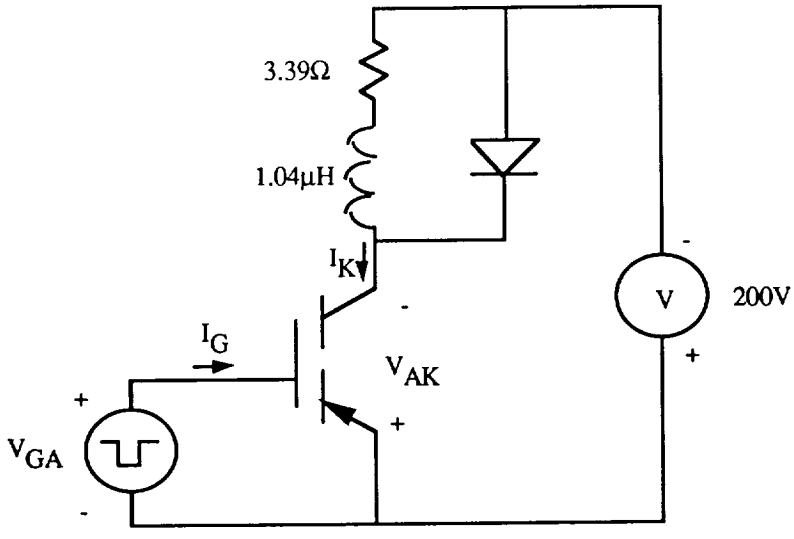

Figure 35. Switching Tme Test Circuit.

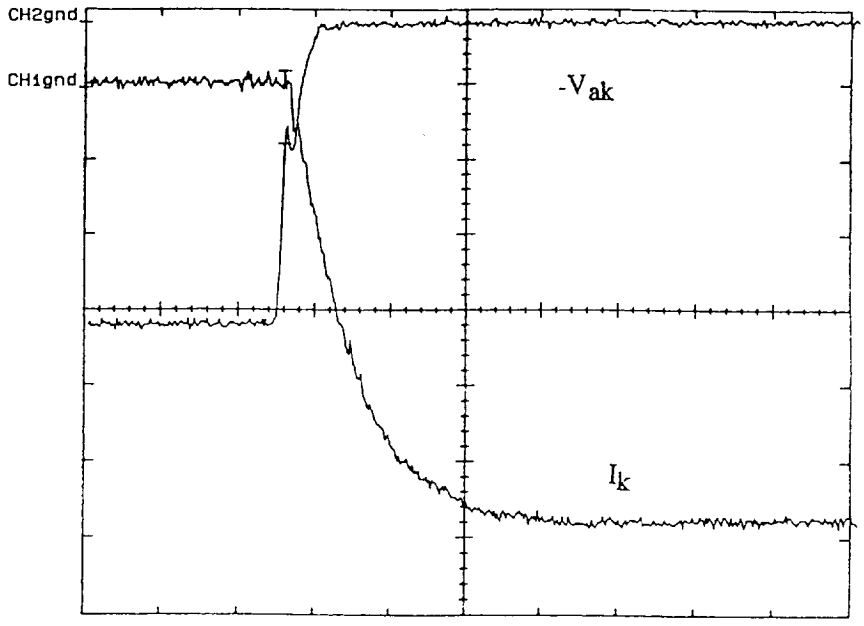

Figure 36. Turn-on waveforms at 30°C. Channel 1 is the current entering the cathode (Ik) displayed at 10A per vertical division. Channel 2 is the cathode-to-anode voltage (-Vak) displayed at 50V per vertical division. The horizontal scale is 500ns per division.

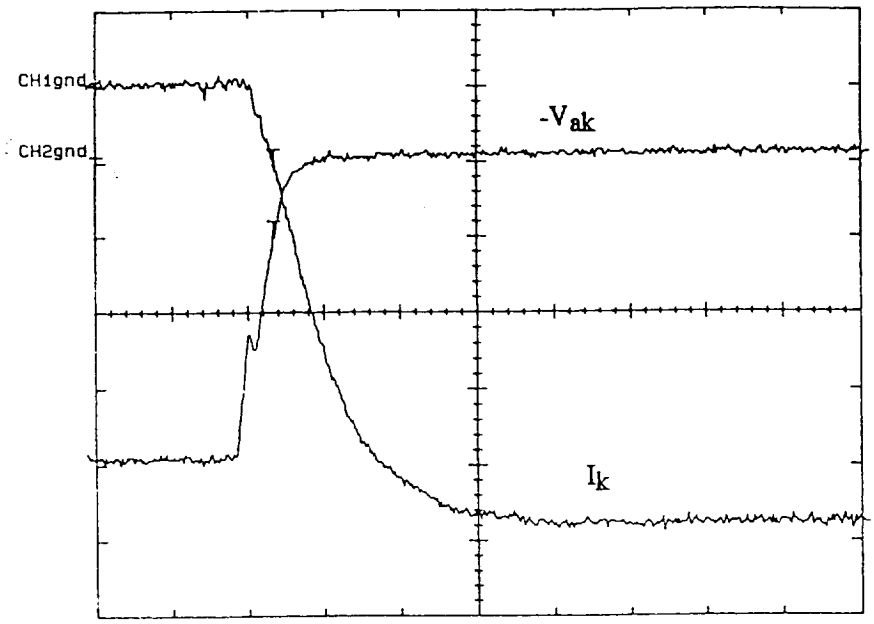

Figure 37. Turn-on waveforms at 200°C. Channel 1 is the current entering the cathode (Ik) displayed at 10A per vertical division. Channel 2 is the cathode-to-anode voltage (-Vak) displayed at 50V per vertical division. The horizontal scale is 500ns per division.

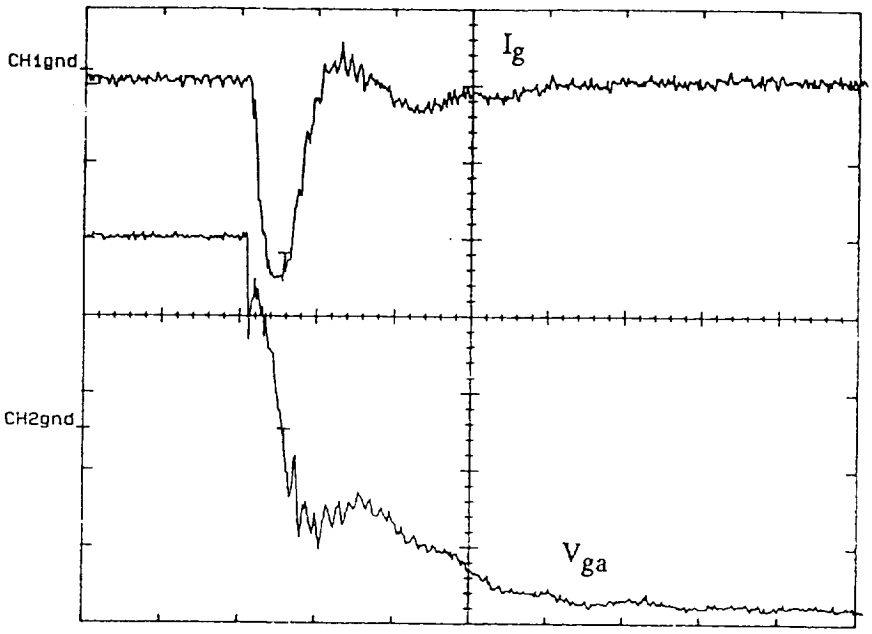

Figure 38. Turn-On Gate Drive Waveforms At 30°C. Channel 1 Is The Current Entering The Gate (Ig) Displayed At 0.5APer Vertical Division. Channel 2 Is The Gate-To-Anode Voltage (Vga) Displayed At 5V Per Vertical Division. The Horizontal Scale Is 500ns Per Division.

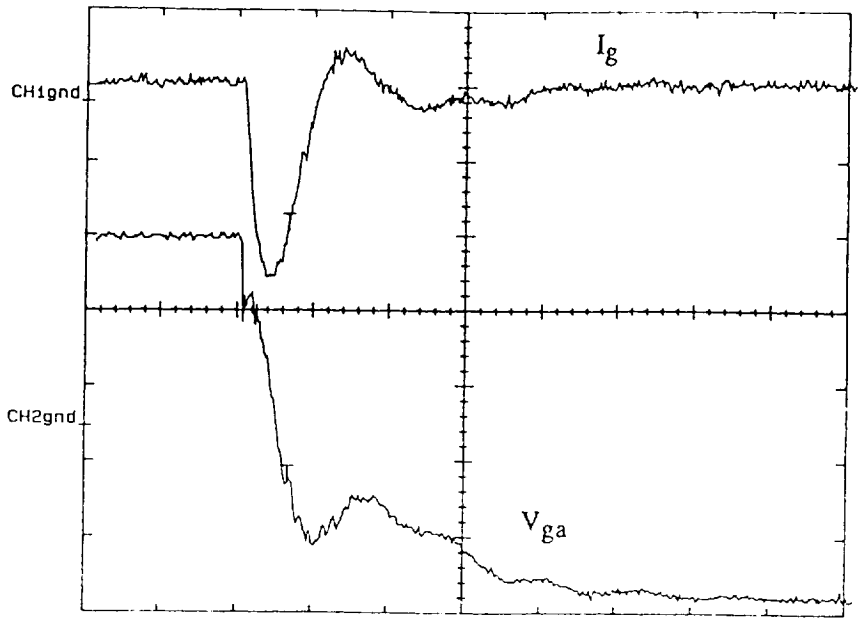

Figure 39. Turn-On Gate Drive Waveforms At 200°C. Channel 1 Is The Current Entering The Gate (Ig) Displayed At 0.5A Per Vertical Division. Channel 2 Is The Gate-To-Anode Voltage (Vga) Displayed At 5V Per Vertical Division. The Horizontal Scale Is 500ns Per Division.

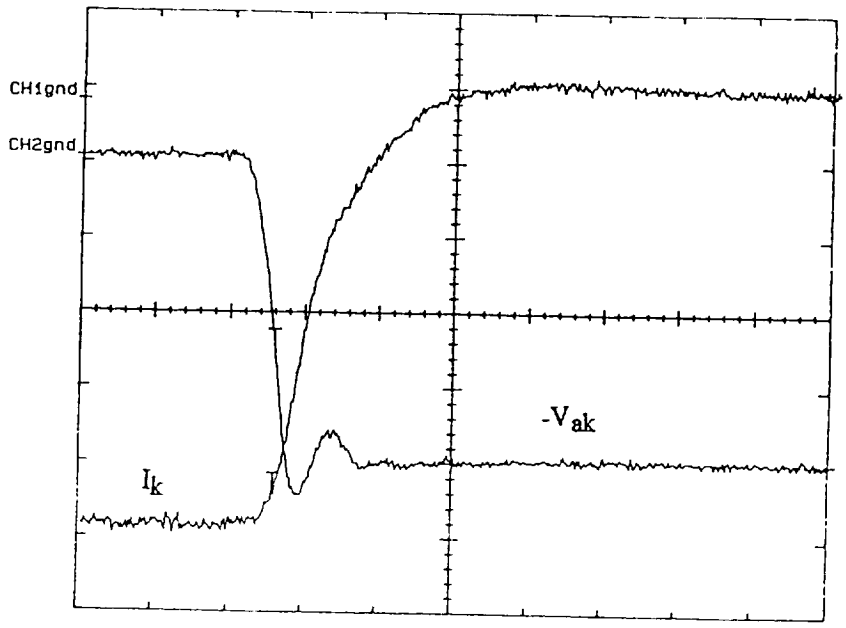

Figure 40. Turn-Off Waveforms At 30°C. Channel 1 Is The Current Entering The Cathode (Ik) Displayed At 10A Per Vertical Division. Channel 2 Is The Cathode-To-Anode Voltage (-Vak) Displayed At 50V Per Vertical Division. The Horizontal Scale Is 500ns Per Division.

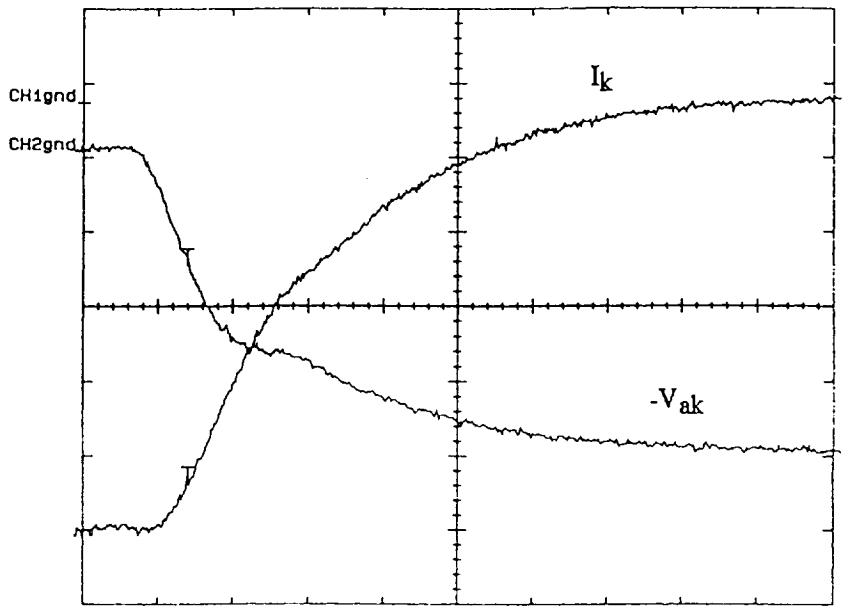

Figure 41. Turn-Off Waveforms At 200°C. Channel 1 Is The Current Entering The Cathode (Ik) Displayed At 10A Per Vertical Division. Channel 2 Is The Cathode-To-Anode Voltage (-Vak) Displayed At 50V Per Vertical Division. The Horizontal Scale Is 500ns Per Division.

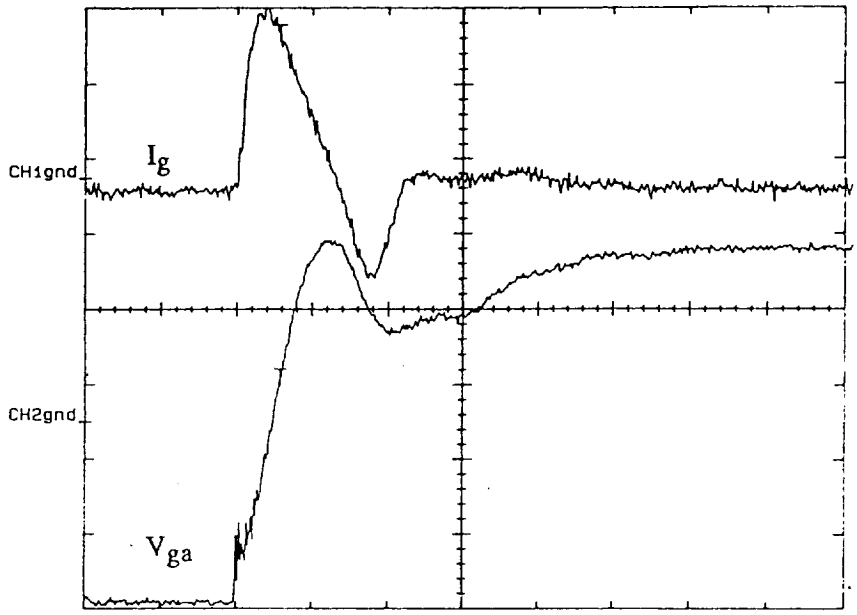

Figure 42. Turn-Off Gate Drive Waveforms At 30°C. Channel 1 Is The Current Entering The Gate (Ig) Displayed At 0.5A Per Vertical Division. Channel 2 Is The Gate-To-Anode Voltage (Vga) Displayed At 5V Per Vertical Division. The Horizontal Scale Is 500ns Per Division.

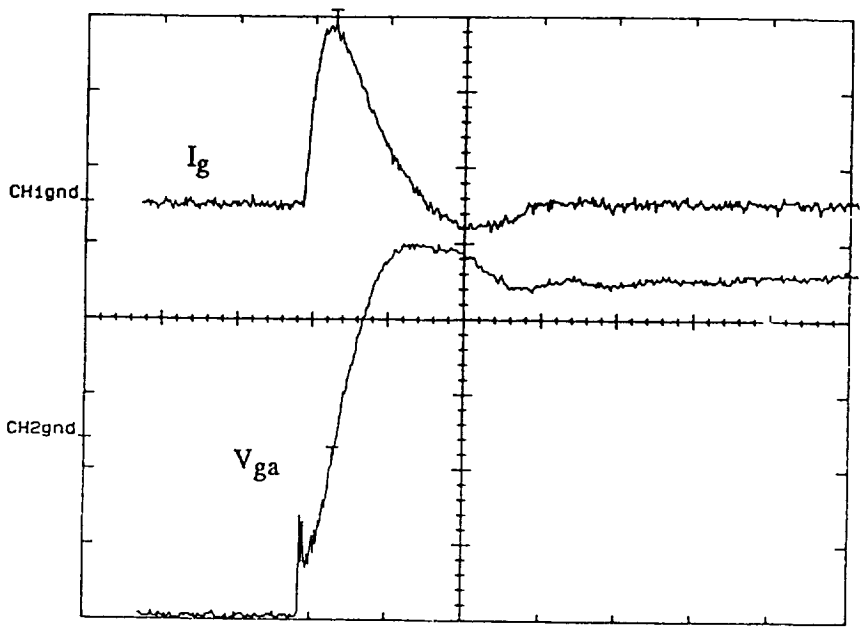

Figure 43. Turn-Off Gate Drive Waveforms At 200°C. Channel 1 Is The Current Entering The Gate (Ig) Displayed At 0.5A Per Vertical Division. Channel 2 Is The Gate-To-Anode Voltage (Vga) Displayed At 5V Per Vertical Division. The Horizontal Scale Is 500ns Per Division.

The MCT turns on very rapidly because of its regenerative thyristor structure. Because of this, the stray inductance in the load serves as a turn-on snubber and may mask the device's true turn-on versus temperature characteristics. Also, the MCT's turn on shown in Figure 36 at 30°C and in Figure 37 at 200°C. may have been slowed by the gate drive. The turn-on gate drive is shown in Figure 38 at 30°C and in Figure 39 at 200°C. The MCT's turn off is a two stage process. First, the regenerative on-state must be broken by turning on the off-FET. Then the excess carriers in the base regions must be recombined. The off-FET supplies charge to the n-base layer for recombination. The excess carriers in the p-base layer, however, must recombine internally. This recombination represents the major portion of the turn-off time. As in the bipolar transistor, this recombination process takes longer at elevated temperatures. Figures 40 and 41 show the MCT turn-off at 30°C and 200°C, respectively. Figures 42 and 43 show the turn-off gate drive at 30°C and at 200°C respectively. The switching times as a function of temperature are shown in Figure 44.

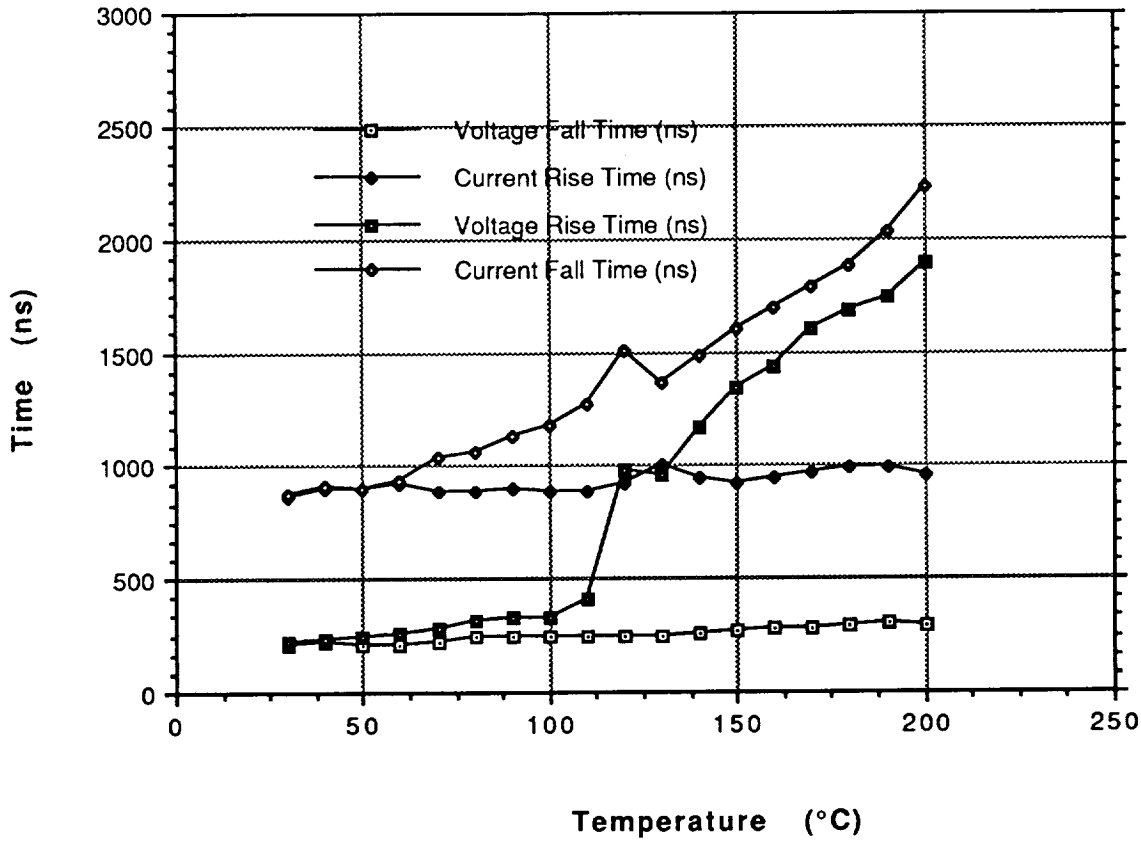

Figure 44. MCT Switching Times as a Function of Frequency

Chapter 4. DEVICE CHARACTERIZATION CONCULSIONS

For the four devices characterized, in general the shift in device parameters above 150°C continued the trend which had developed over the range from 25°C to 150°C. With the exception of the bipolar breakdown voltage, no anomalous measurements were observed. The leakage current which is often considered a major factor at elevated temperatures increased with temperature as expected. However, the leakage current at 200°C was still in the milliamp range. The only other parameter which changed dramatically with temperature was the breakdown voltage of the MCT. This decrease in breakdown voltage with increasing temperature must be included in high temperature MCT designs.

The results of the switching tests are somewhat inconclusive, particularly for the N-MOSFET due to parasitics in the test circuitry and limitations on the drive circuits. The BJT, IGBT and the MCT are slower switching devices and the switching test data is consistent with the manufacturer's specifications for these devices.

Circuits can be designed with the device characteristics measured at 200°C. From the experience of making the measurements, it is recommended that resonant, zero current or zero voltage switching techniques be used in the circuit design. The devices are capable of providing blocking voltages in the off-state or conducting current in the on-state. However, hard switching with both voltage and current present can result in secondary breakdown and destruction of the devices at elevated temperatures.

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12. S. D. Auther, V A. K. Temple, and D. L. Watrous, "Forward Blocking Comparison of P and N MCTs", *Conference Record of the 1992 IEEE IAS Annual Meeting*, October 1992.

Chapter 5. RESONANT CIRCUIT TESTING

From the results of the parameter testing, the IGBT and the N-MOSFET were chosen for testing in power supply circuits. The BJT was rejected because of its high base current needs and the complexity of the base drive circuitry. The MCT was obtained late in the program, too late to be included in circuit design. This chapter contains test information for a parallel-loaded resonant inverter.

Parallel-loaded Resonant Inverter [1]

For demonstration of the devices at 200°C, a circuit was needed that would repetitively stress the devices. The circuit would also need to show a practical application for the devices at 200°C. It was decided that an H-Bridge inverter with a switching frequency of approximately 20kHz and a peak device current of approximately 20A would meet these requirements.

In the search for inverter designs, "hard switching" designs were not considered in order to avoid the stress of both high current and high voltage in the switching device, instead a parallel-loaded resonant inverter was built [1]. This circuit is shown in Figure 45. The drive signals for these devices are generated using a Unitrode UC3860 control chip [2] and an International Rectifier IR2110 [3] driver. The signals from the IR2110 are supplied to bipolar drivers through optocouplers. The inverter is operated in an open loop fashion. A split inductor design for the inverter produces half-wave resonant current in the switches. 1N3891 fast recovery diodes were used as anti-parallel diodes to commutate the second half of this resonant current. Only the power devices and diodes were placed in the oven mounted on an aluminum heat sink. The driver circuitry remained outside the chamber, connected with twisted pairs of 12 gauge silver plated Teflon coated wire.

Figure 46 shows the drain-source voltage and drain current for a low-side N-MOSFET in the inverter at 200°C. Likewise, Figure 47 show the collector-emitter voltage and collector current for a low-side device in the IGBT inverter at 200°C. The transistor case temperatures for the IGBT and MOSFET were measured at 214°C and 208°C, respectively. No degradation in performance was observed at elevated temperature. The IGBT inverter was successfully operated at 40A peak current for 72 hours at 200°C.

References

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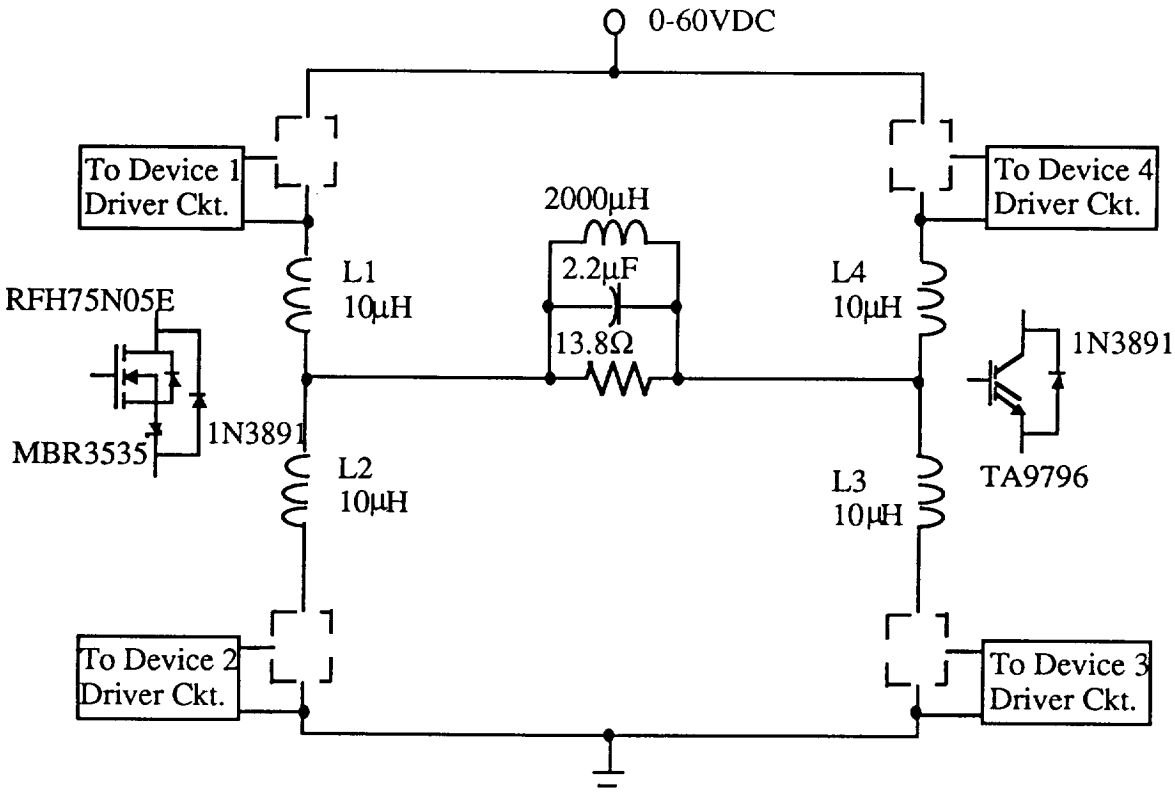

Figure 45. Parallel-loaded resonant inverter

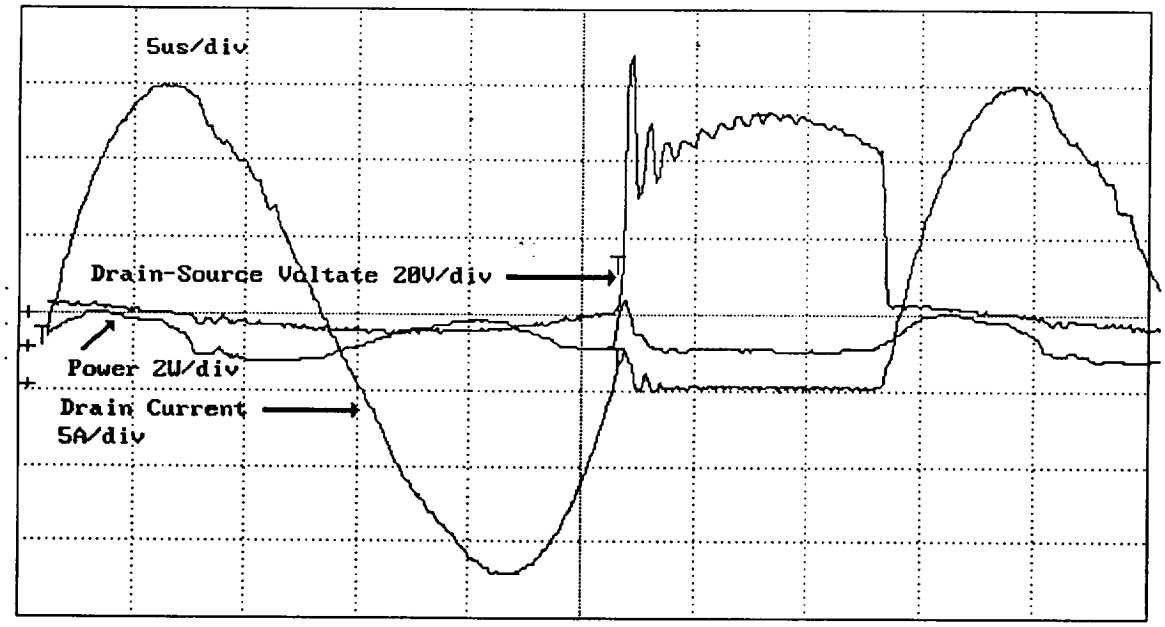

FIGURE 46. Switching waveforms for low-side MOSFET in switching inverter at 200°C.

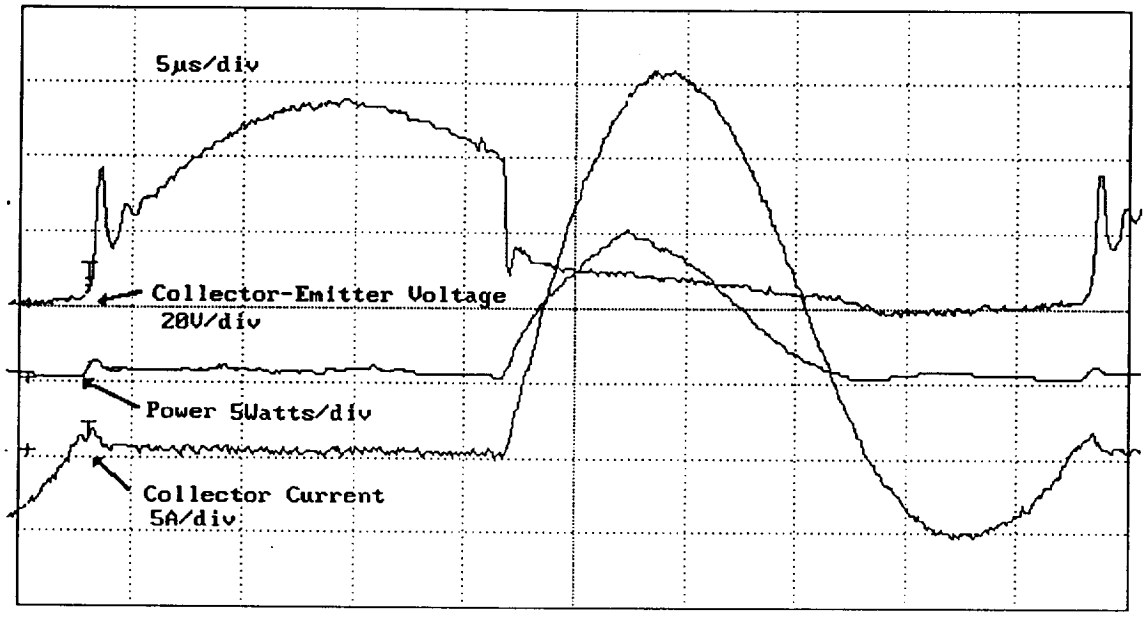

FIGURE 47. Switching waveforms for low-side IGBT in switching inverter at 200°C.

Chapter 6. ZERO-CURRENT-SWITCHED BOOST CONVERTER

The next circuit that was tested at elevated temperatures was a zero-current-switched (ZCS) boost converter [1]. The basic boost converter is modified by replacing the switch with the resonant switch shown in Figure 48.

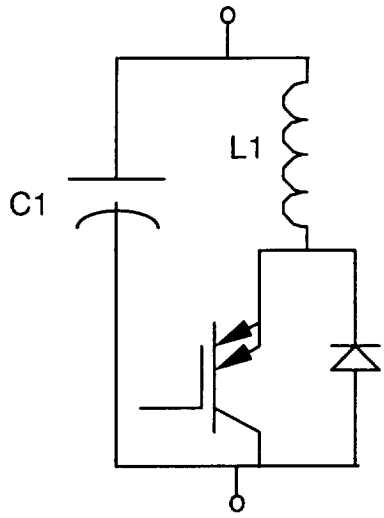

Figure 48. Resonant switch sub-circuit for ZCS boost converter

Non-resonant switching methods subject devices simultaneously to high voltages and high currents during switching transitions which creates large switching losses. The power dissipated in switching transitions becomes excessive at elevated temperatures due to both increased leakage currents and increased switching times. The larger switching losses at elevated temperatures lead to decreased reliability. In an effort to overcome this limitation, the converter was designed using a zero-current switching scheme.

The inductor, L1, and the capacitor, C1, contained in the resonant switch are used to shape the current through the IGBT/diode pair. The bi-directional switch formed by the IGBT/diode pair allows excess energy stored in the resonant elements, L1 and C1, to be fed back to the source. This eliminates the voltage conversion ratio's load sensitivity problem experienced by resonant switching schemes using uni-directional switches [1].

Figure 49 shows a sample IGBT/diode pair current for the sub-circuit above. Figure 50 shows a representative IGBT/diode voltage waveform. At turn on, the IGBT voltage can reach its on-state value quickly while the current slowly rises in a quasi-sinusoidal fashion due to the LC circuit. This reduces losses in a fashion similar to a turn-on snubber. The current then oscillates through the bi-directional switch due to the resonance between L1 and C1. This allows the IGBT to be turned off while the diode is carrying the reverse current. The diode then naturally commutates as the current returns to zero. There is no simultaneous high current, high voltage stress on the IGBT at either turn-on or turn-off as occurs with non-resonant switching schemes. This reduces switching losses and device stress and should lead to increased device reliability, especially at elevated temperatures.

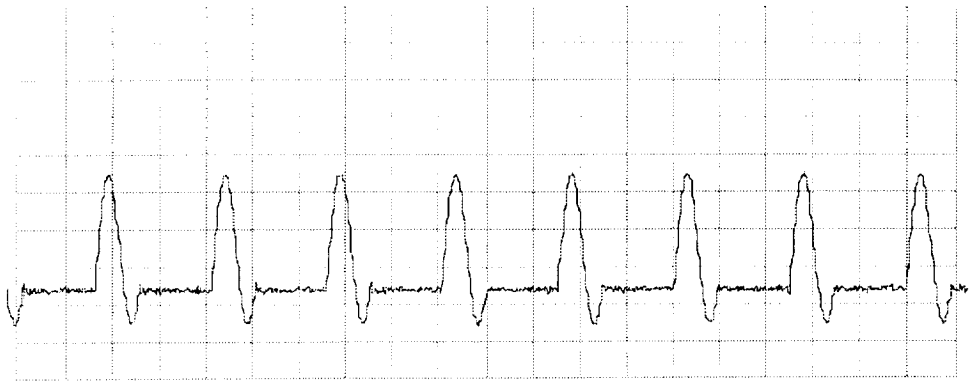

Figure 49. IGBT/diode pair current (10 A/vert. division, 10 μs/horiz. division).

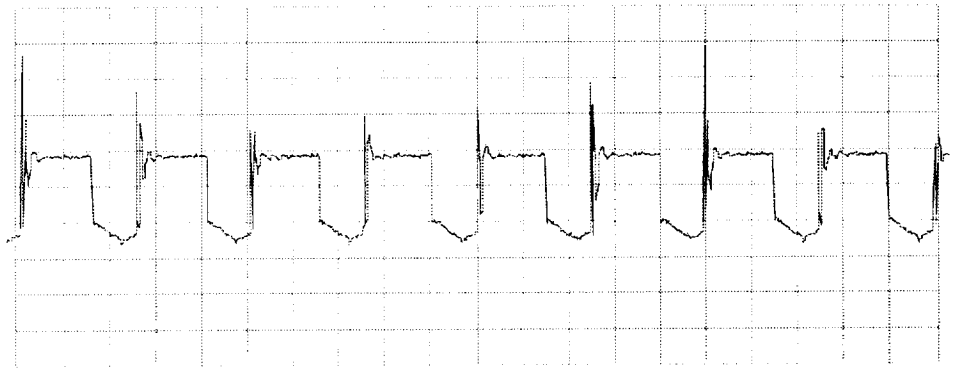

Figure 50. IGBT/diode pair voltage (20 V/vert. division, 10 μs/horiz. division).

A resonant frequency of 100 kHz was selected for the circuit. Equation 33 shows the relationship between L1, C1 and the resonant frequency.

$$f_{res} = \frac{1}{2\pi\sqrt{L_1 C_1}} \qquad \text{eqn. 33}$$

C1 was sized with the goal of subjecting it to the entire range of ambient temperatures in future versions. C1 would be required to have a temperature stable value and to be capable of rapid voltage change. These restrictions would make C1 a very expensive element. C1, therefore, was set to the lowest value which would allow the circuit to operate properly in order to reduce cost. If too small a value was used, not enough energy was stored and the circuit did not oscillate well enough to allow the reverse current flow through the diode. A satisfactory value of 5 μF was experimentally determined.

Once the value of C1 was set, the value of L1 was determined. A Magnetics, Inc. 55717-A2 powdered permalloy torroid core was used for L1. The inductor windings were adjusted to achieve the desired 100 kHz resonant frequency. The necessary value was experimentally determined to be 6.0 μH. It was verified through testing that the inductor value remained relatively stable. This was important, since changes in the value

of L1 would alter the circuit's resonant frequency and make the circuit more difficult to control.

A Harris TA9796 IGBT selected for use in this converter is rated for 34 A and 1000 V. This device has been characterized from 30°C to 200°C and no abnormal behavior was found. The IGBT's breakdown voltage, which was plotted in a previous chapter, is more than sufficient to endure the 80 V oscillations experienced at turn off in this converter. The IGBT's on-state voltage versus temperature was also plotted previously. For a relatively low voltage converter, the 3 - 4 V on-state voltage of the IGBT represents a major source of losses.

The 1N3893 fast recovery diode used to complete the resonant switch is rated to carry 12 A and block 400 V. A fast recovery diode was selected to reduce switching losses and also to minimize the voltage oscillations at turn off.

Figure 51 shows the boost converter schematic including the resonant switch. This converter operates very similarly to the basic boost converter. The inductor, L2, filters the input current and provides a constant current source. The capacitor C2 filters the output waveform to provide a DC voltage.

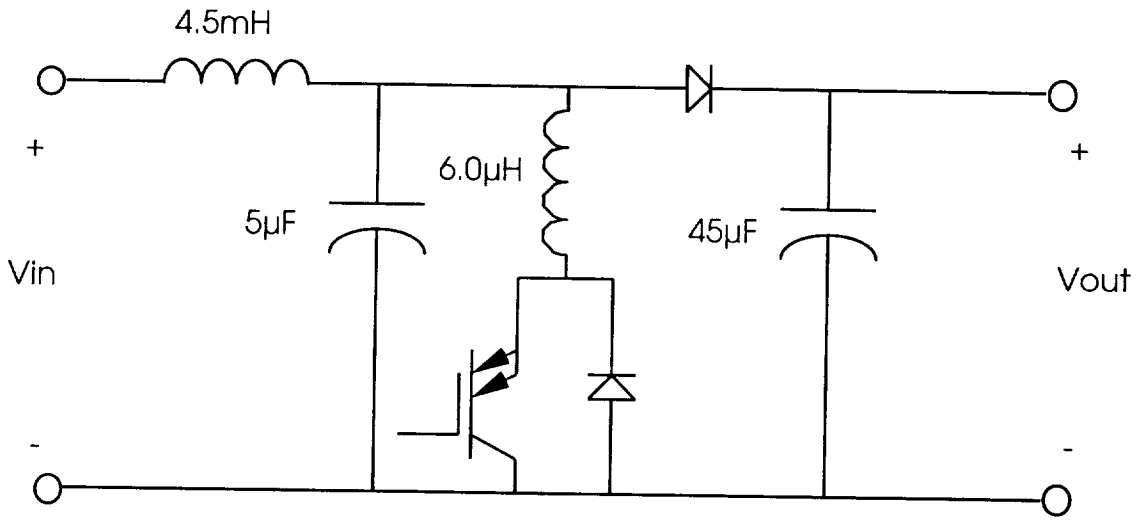

Figure 51. Power supply schematic.

The converter's voltage conversion ratio is governed by equation 34 [1].

$$\frac{x-1}{x}-\frac{1}{2\pi}\left(\frac{f_s}{f_{res}}\right)\left[\frac{x}{2r}+\sin^{-1}\left(\frac{-x}{r}\right)+\frac{r}{x}\left(1-\sqrt{1-\left(\frac{x}{r}\right)^2}\right)\right]=0 \qquad \text{eqn. 34}$$

$$x \equiv \frac{V_o}{V_s}=\frac{42V}{28V}=1.5$$

$f_s \equiv$ switching frequency

$f_{res} \equiv$ resonant frequency

$$Z_n \equiv \sqrt{\frac{L1}{C1}}=\sqrt{\frac{6.1\mu H}{5.0\mu F}}=1.10\ \Omega$$

$$r \equiv \frac{R_{load}}{Z_n}=\frac{17.6\ \Omega}{1.10\ \Omega}=16.0$$

$$\text{and } \frac{3\pi}{2}<\sin^{-1}\left(\frac{-x}{r}\right)<2\pi$$

A simple approximate voltage conversion ratio may be obtained if it is noted that the expression shown in equation 34 is approximately 2π for $0.0 < x/r < 0.99$. This condition is satisfied for all conversion ratios of interest for this converter.

$$\left[\frac{x}{2r}+\sin^{-1}\left(\frac{-x}{r}\right)+\frac{r}{x}\left(1-\sqrt{1-\left(\frac{x}{r}\right)^2}\right)\right]\cong 2\pi \qquad \text{eqn. 35}$$

$$\frac{x-1}{x}-\frac{f_s}{f_{res}}=0 \qquad \text{eqn. 36}$$

By realizing that fs/fres is equivalent to the duty cycle, D, equation 37 may be easily derived. It is of interest that equation 37 is the voltage ratio governing simple boost converters.

$$\frac{V_o}{V_s}=\frac{1}{1-D} \qquad \text{eqn. 37}$$

The input inductor, L2, was chosen to be 4.5mH. A Magnetics Inc. 58867-A2 powdered ferrite torroid core was used for this element. Testing also verified that the inductor value was relatively insensitive to temperature. The value of this inductor was chosen to be large in order to reduce input current fluctuations and to satisfy the analysis assumptions made in [1].

The output capacitor, C2, value was set by the allowable ripple voltage on the output. A maximum allowable ripple voltage of +/-1V was selected. Equation 38 was

then used to determine the minimum value of C2 to be 23.8 μF. A value of 45 μF was selected for the circuit.

$$C \geq \frac{I_{out}(1-D)T}{\Delta V} = \frac{\frac{100W}{42V}(.6667)(30\mu s)}{2V} = 23.8\mu F \qquad \text{eqn. 38}$$

Power Circuit Performance

The power supply, excluding the control circuit and the two capacitors, operated as designed at ambient temperatures between 30°C and 200°C. Although no extensive life testing was done, the circuit was found to be generally reliable. It operated through repeated temperature cycling and at 200°C for periods up to 7 hours without a single failure.

Figure 52 shows the IGBT/diode current at 200°C, and Figure 53 shows the IGBT/diode voltage at 200°C. When compared to the same measurements made at 30°C, Figure 54 and Figure 55, it can be seen that the circuit operated in a consistent fashion across the temperature range. The resonant frequency of the circuit stayed essentially constant as shown by comparing Figure 52 and Figure 5.4.

Figure 52. IGBT/diode pair current at 200°C (10 A/vert. division, 10 μs/horiz. division).

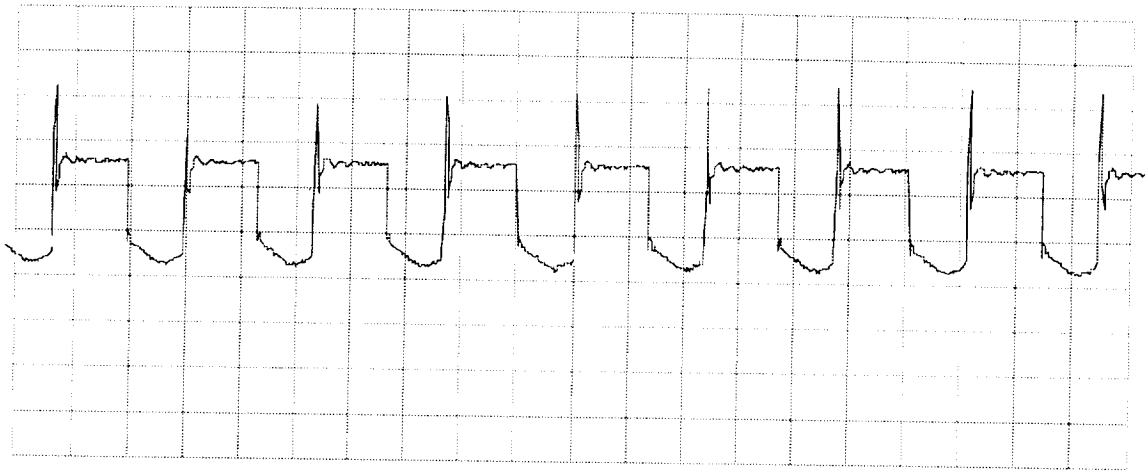

Figure 53. IGBT/diode pair voltage at 200°C (20 V/vert. division, 10 μs/horiz. division).

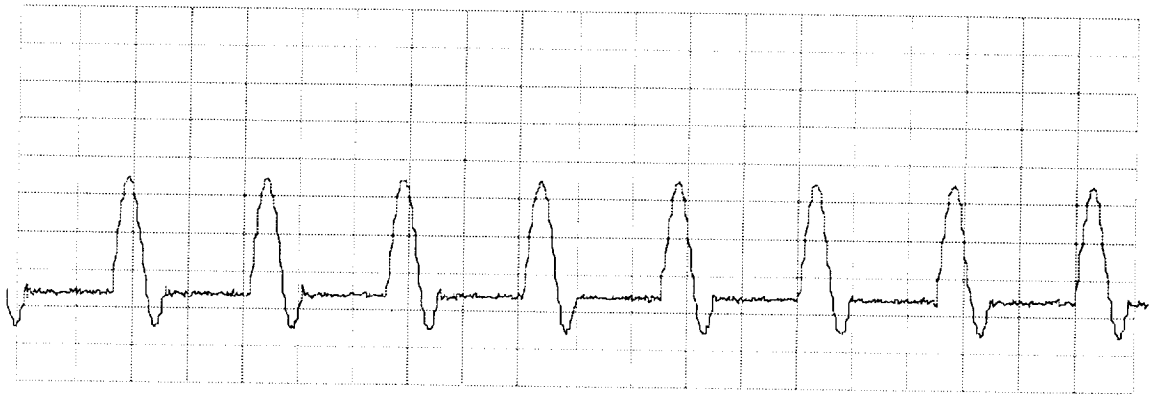

Figure 54. IGBT/diode pair current at 30°C (10 A/vert. division, 10 μs/horiz. division).

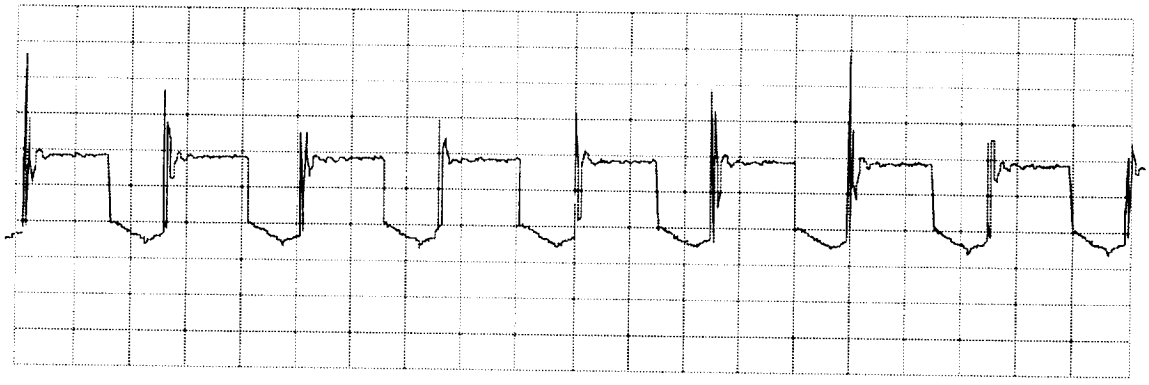

Figure 55. IGBT/diode pair voltage at 30°C (20 V/vert. division, 10 μs/horiz. division).

The output voltage waveform at 200°C in Figure 56, and at 30°C in Figure 57 changed very little over the temperature range. This was as expected since the filter capacitor was not subject to the varying ambient temperatures. The output voltage varied

approximately +/-2V (5%) at all temperatures due to the ripple voltage and to high frequency noise.

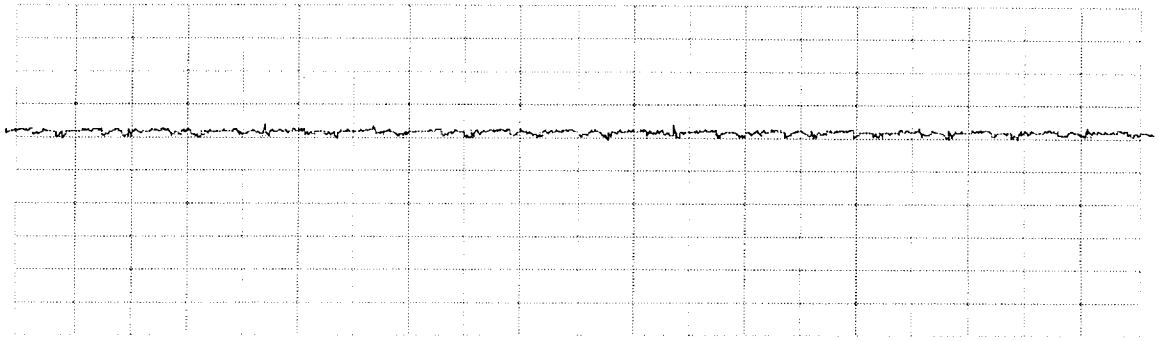

Figure 56. Output voltage at 200°C (10 V/vert. division, 20 µs/horiz. division).

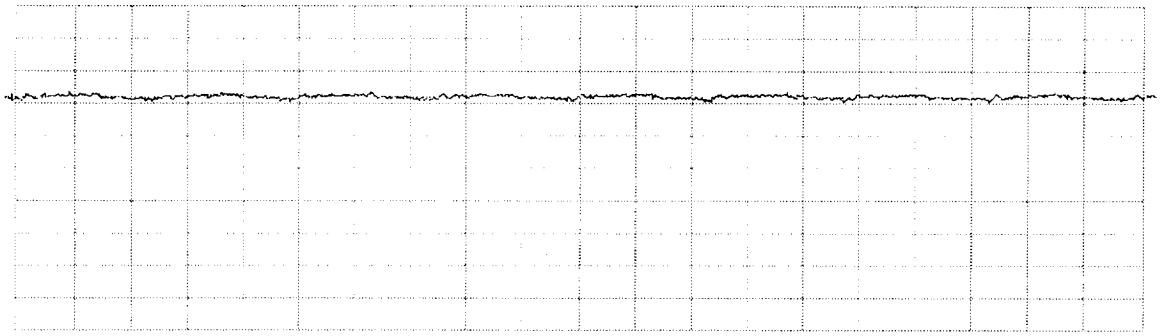

Figure 57. Output voltage at 30°C (10 V/vert. division, 10 µs/horiz. division).

Figure 58 is the overall efficiency of the converter versus temperature. The efficiency of the converter is 79.75% at room temperature and drops to 71.38% at 200°C. While the efficiency of the circuit is reduced at elevated temperatures, this reduction is not great enough to render the circuit unusable.

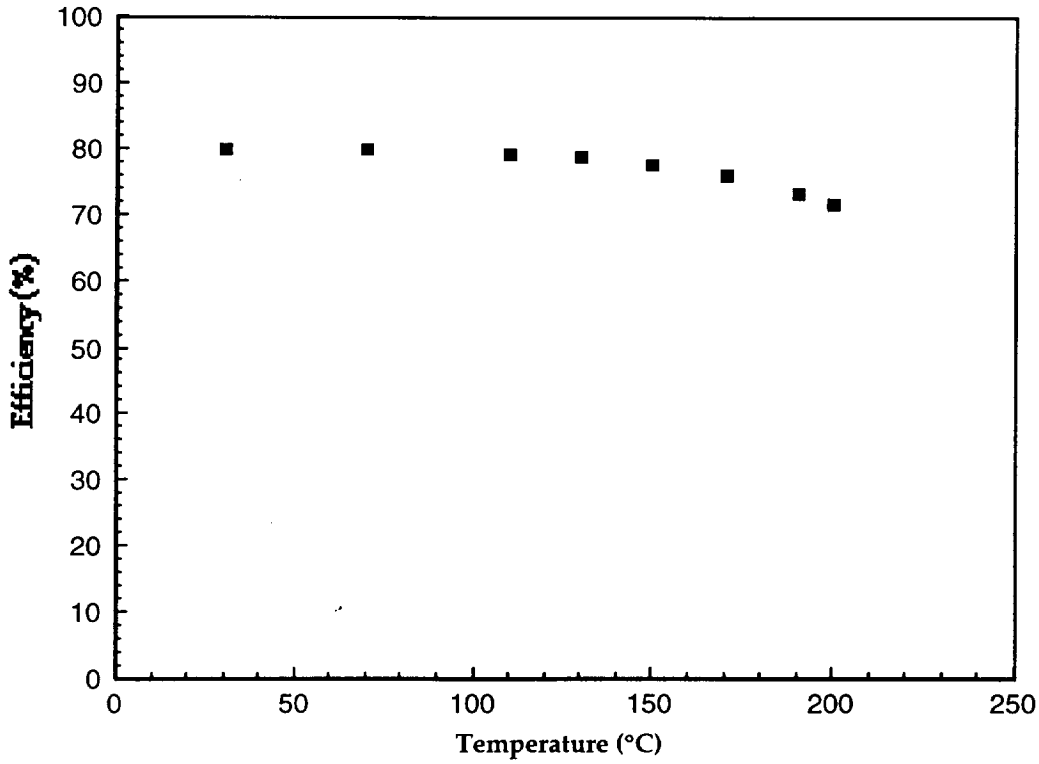

Figure 58. Overall converter efficiency versus temperature.

The IGBT/diode pair and the input inductor are the two elements which dissipate most of the power lost in the power supply. At 200°C, the losses in these elements represent 82% of the total circuit losses

Figure 59 shows the power dissipated in the IGBT/diode pair versus temperature. As can be seen in Figure 60, the on-state losses of the IGBT are the dominant factor at room temperature. Fluctuations in the IGBT's on-state voltage account for most of the changes in power loss to 110°C. Above this temperature, increases in the diode's leakage current and reverse recovery time make the diode's losses significant. Figure 61, the instantaneous IGBT/diode pair losses at 200°C shows a large increase in the dissipated power at the diode turn off due to the increased reverse recovery time.

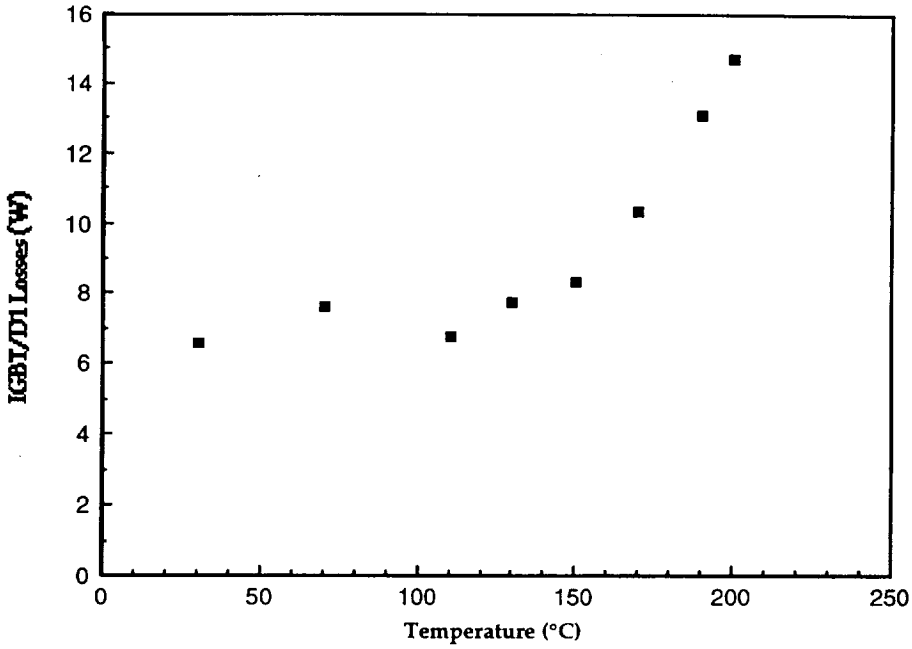

Figure 59. IGBT/diode pair losses versus temperature.

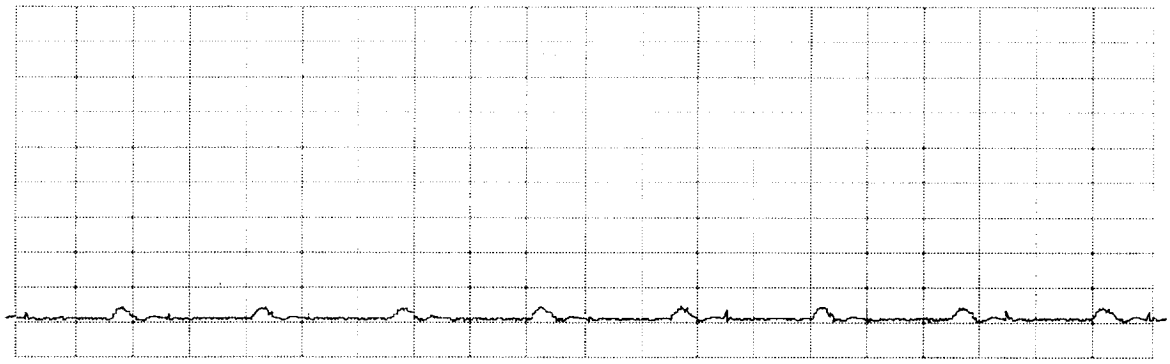

Figure 60. Instantaneous IGBT/diode pair losses at 30°C (50 W/vert. division, 10 μ s/horiz. division).

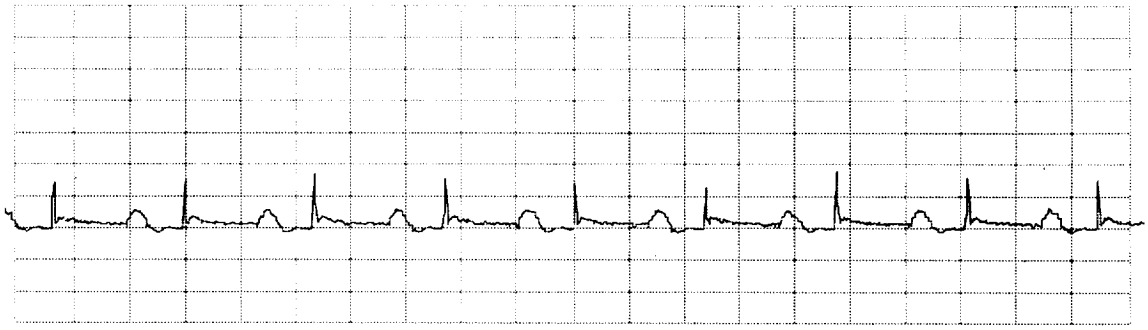

Figure 61. Instantaneous IGBT/diode pair losses at 200°C (50 W/vert. division, 10 μ s/horiz. division).

The power loss due to the input inductor as a function of temperature is shown in Figure 62. Increases in core losses and in copper wire losses both occur as the ambient temperature rises.

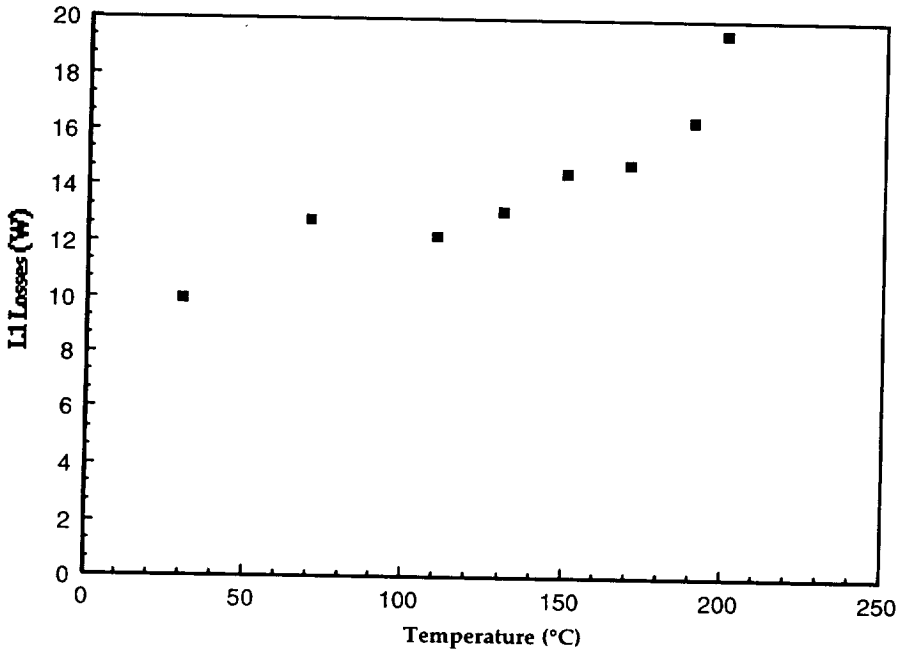

Figure 62. L2 losses versus temperature.

Control Circuit Design

The control circuitry of the power supply was designed using the UC1860 resonant mode power supply controller [2]. This integrated circuit was developed specifically for implementation of frequency-modulated fixed-on-time control schemes and incorporates all the functions required for control of the resonant power supply. Functions utilized in the design of the control circuit and provided by the UC1860 included a precision voltage reference, an error amplifier, a variable frequency oscillator (VFO), and oscillator triggered one shot and an output driver. The UC1860 is contained in a ceramic package and is rated for operation to 125°C. Despite this rating, the control circuit was designed with operation to 200°C in mind.

The control circuit was fabricated as a thick film hybrid with special consideration given to facilitating operation to 200°C. The resistors, both printed and chip, used in this process are temperature stable. Special NPO capacitors were used in the circuit because they were found to be durable and to have constant (+/- 5%) values across the temperature range. High temperature solder paste was used in the process instead of the usual tin-lead mixture which melts at 180°C.

The first step in the control circuit design was to set the on time of the UC1860's one shot timer which controls the output drive pulse width. The on time was selected to

provide zero current turn off of the IGBT at all temperatures. A room temperature on time of 8.4 μs was experimentally determined to meet these needs.

With the on time selected, the values of the resistor and capacitor connected to the UC1860's RC pin (pin 9) could be calculated. The capacitor was selected from the available values to be 1 nF. The necessary resistor value was then calculated to be 42 kΩ using equation 39. In the layout, the printed resistor used for this element was designed as 30 kΩ to allow precision trimming of the resistor to provide the exact on time desired.

$$\text{on time} = 0.2(R*C) \qquad \text{eqn. 39}$$

With the on time set, the minimum and maximum control frequencies could be set. These frequencies determine the maximum and minimum input voltages which the power supply can convert to the desired output voltage. With the Trig and Osc pins (pins 13 and 14) grounded, the frequency of the output waveform is established by the 1860's VFO. Equation 40 is used to approximate the oscillator frequency. C_{VFO} was selected from available values to be 1nF. This equation shows that with C_{VFO} set the oscillator's frequency is directly proportional to I_{VFO}.

$$f_{osc} = \frac{I_{VFO}}{(C_{VFO} \bullet 1V)} \qquad \text{eqn. 40}$$

Using equation 41, the range of necessary oscillator frequencies was determined. It was decided that the power supply should be able to control for 16 V to 36 V. Using 15 V and 37 V as the extremes to allow for a margin of error, the minimum oscillator frequency was calculated to be 11.88 kHz, and the maximum oscillator frequency was calculated to be 64.16 kHz.

$$\frac{V_o}{Vin} = \frac{1}{1 - \frac{f_s}{f_{res}}} \qquad \text{eqn. 41}$$

The minimum oscillator frequency was set by a resistor connected between the 5 V reference and the I_{VFO} pin which sits at approximately 1.4 V. The minimum value of this resistor was calculated to be 303 kΩ using equation 40. The value implemented in the control circuit was 312 kΩ.

The maximum oscillator frequency was then set using a resistor between the error amplifier output and the I_{VFO} pin. The error amplifier's maximum output is 2 V above the I_{VFO} pin. The maximum value of this resistor was calculated as 40 kΩ. The final value of the printed resistor used for this value was 33.2 kΩ in order to provide additional range of controllable voltages.

Figure 63 shows the feedback circuit which is the UC1860's error amplifier. The first stage of the circuit consists of a voltage divider and a low pass filter. R1 and R2 form a voltage divider which reduces the power supply's 42 V output to the 3 V recommended input level for the error amplifier. R2 and C1 form a low pass filter with a -3dB frequency of approximately 1600 Hz ($1/2\pi RC$). The second stage of the feedback

circuit is an integrator which adds stability to the circuit. The transfer function of this stage can be approximated by equation 42.

$$\frac{V_o}{V_{in}} = \frac{-(1+R_3C_2s)}{R_3C_3s} = \frac{-(1+10^{-6}s)}{10^{-4}s} = 10^4\left(\frac{1}{s}\right) + 0.01 \qquad \text{eqn. 42}$$

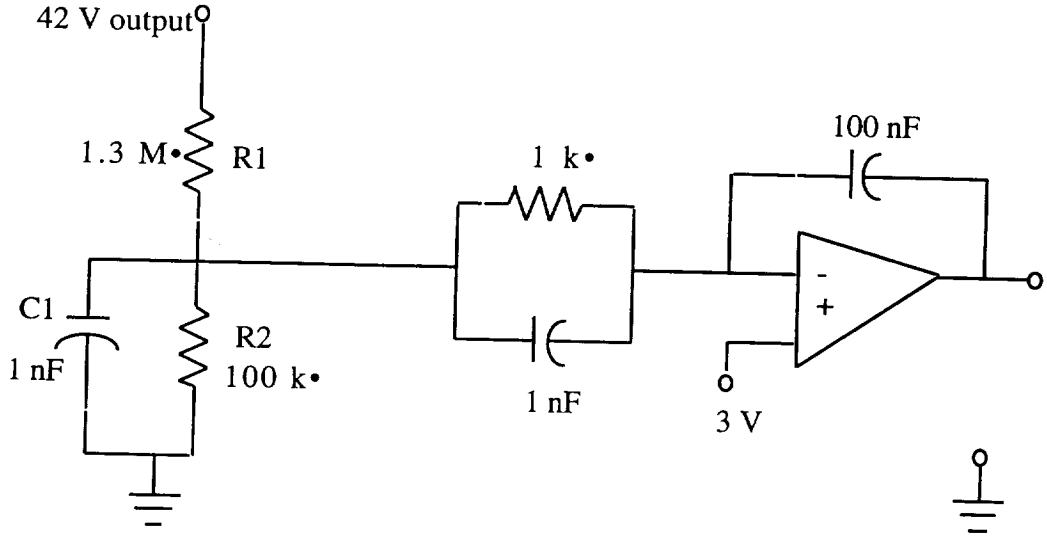

Figure 63. Feedback circuit diagram.

The final portion of the control circuitry design was the output driver. Initial tests of the UC1860 showed that its drive circuitry failed when driving the IGBT at elevated temperatures. To avoid these destructive failures, the output buffer shown in Figure 64 was added. This simple non-inverting bipolar transistor output buffer reduced the current requirements placed on the UC1860's output driver. The 2N2222 and 2N2907 transistors used in this circuit were in TO-18 metal packages. By implementing this circuitry, the failures were eliminated and the UC1860 was able to drive the IGBT at 200°C.

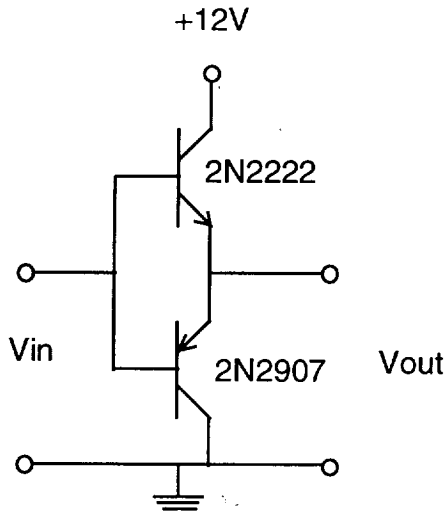

Figure 64. Output buffer schematic.

Control Circuit Performance

The control circuit functioned as designed at room temperature, regulating the power supply's output to 42.9 V. The output voltage could have been fine tuned by trimming resistor values in the feedback circuit. The range of controllable input voltages exceeded the desired 16 V to 36 V range, and the on time was measured to be 8.34 μs, almost exactly the designed value. The feedback circuit was stable and operated at all temperatures up to 170°C.

Table 2 shows the control circuit parameters measured at the temperatures listed. At 170°C, the control frequency dropped to approximately its minimum set value of 11.7 kHz. This was possibly due to drifting in the error amplifier's output voltage. The circuit resumed working when the temperature was lowered.

Temperature (°C)	f (kHz)	Output Voltage (V)	5V Regulator output (V)	On Time (μs)
30	35.09	42.9	4.97	8.34
50	35.09	42.9	4.97	8.34
70	35.09	42.9	4.97	8.34
90	35.09	42.9	4.97	8.34
110	35.09	42.9	4.97	8.34
130	35.81	43.2	4.99	8.34
150	37.38	44.4	5.04	8.26
170	11.71		5.00	

Table 2. Control circuit parameters over temperature range.

The precision 5 V reference did not remain constant. This resulted in temperature variation in the output voltage. In order to provide a temperature invariant output voltage, a voltage reference which was not temperature sensitive would be necessary.

A simple open loop UC1860 circuit was constructed in order to experimentally determine the satisfactory on time for circuit operation from 30°C to 200°C. This process provided not only a satisfactory on time, but also other valuable data from the successful operation of this open loop control circuit to 200°C. The performance of the output drive was verified to 200°C. The satisfactory operation of the UC1860 VFO and one shot to 200°C were also demonstrated by this process. These portions of the UC1860 were shown to be operational across the temperature range and pointed to the other circuitry as the source of the high temperature failures.

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Chapter 7. ZERO-VOLTAGE SWITCHED CONVERTER

The previous two chapters have described testing a parallel-loaded resonant converter and ZCS boost converter. The resonant converter was tested with both IGBTs and MOSFETs. The ZCS boost converter, which converts 28 Vdc to 42 Vdc, utilized an IGBT. Examination of the waveforms in the previous chapter indicates that the voltage across the resonant switch reaches voltages as high as 80 V. This voltage level was not a concern with the 100 V IGBT. However, for the 50 V MOSFETs used in this effort, these voltage spikes are unacceptable. As a result, a different circuit topology was selected so that the MOSFETs could tested at 200 °C. This circuit, which also converts 28 Vdc to 42 Vdc, will be described in this chapter and test results will be given for 100 W and 500 W units.

Figure 65 shows the circuit topology utilized for testing the MOSFETs at 200 °C. As can be seen in this figure, the circuit consists of an H-bridge containing 4 MOSFET switches S1-S4. These devices are controlled using a phase-shifted PWM scheme which allows them to be turned on at zero voltage [1-2]. The diodes D1-D4 may be the intrinsic diodes of the MOSFETs or discrete diodes. The capacitances Cs1 - Cs4 are lossless snubbers. Since this circuit is a buck-derived topology [1-2], a transformer is needed to

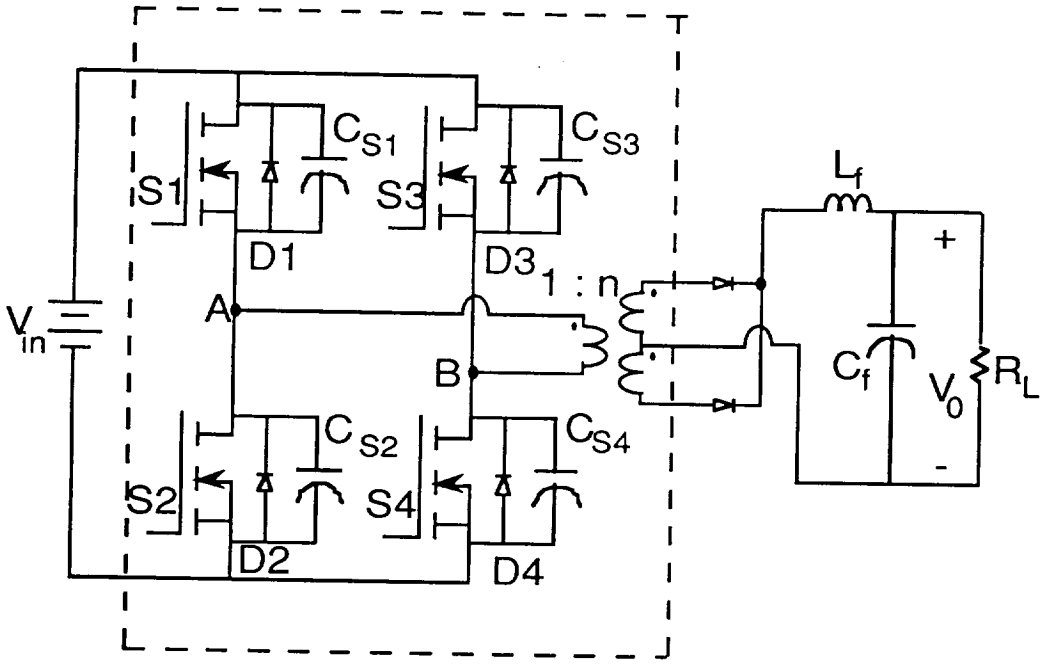

Figure 65. Phase-shifted PWM circuit topology [1-2]

step up the voltage. Components L_f and C_f form a filter. The inductance L_f is needed in this circuit to help achieve zero-voltage switching.

The switching signals for the circuit of Figure 65 are given in Figure 66. Switches S1 and S2 are operated 180 degrees out of phase with respect to one another; S3 and S4 are operated in the same manner. The duty cycle for all switches is slightly less than 50%. Control is achieved by phase-shifting the switches in the right leg from those in the left leg. From t0 - t1, S1 and S4 are conducting. At t1, S1 is turned off, and the current flowing in the leakage inductance of the transformer transfers from S1 to the capacitors Cs1 and Cs2. Capacitor Cs1 begins to charge from zero to the input voltage while Cs2 discharges from

the input voltage to zero. When the voltage across Cs2 reaches zero and goes negative, D2 turns on; switch S2 can now be turned on at zero voltage, thus reducing the switching losses. During the time interval t2-t3, S2 and S4 are conducting and the voltage applied to the transformer is zero. At t3, S4 is turned off. The current in the leakage inductance of the transformer now charges Cs4 and discharges Cs3. When the voltage across Cs3 tries to go negative, D3 turns on so that S3 can now be turned on at zero voltage. Note that only zero voltage turn on of switches S1-S4 is achieved; the switches are not turned off at zero voltage or current.

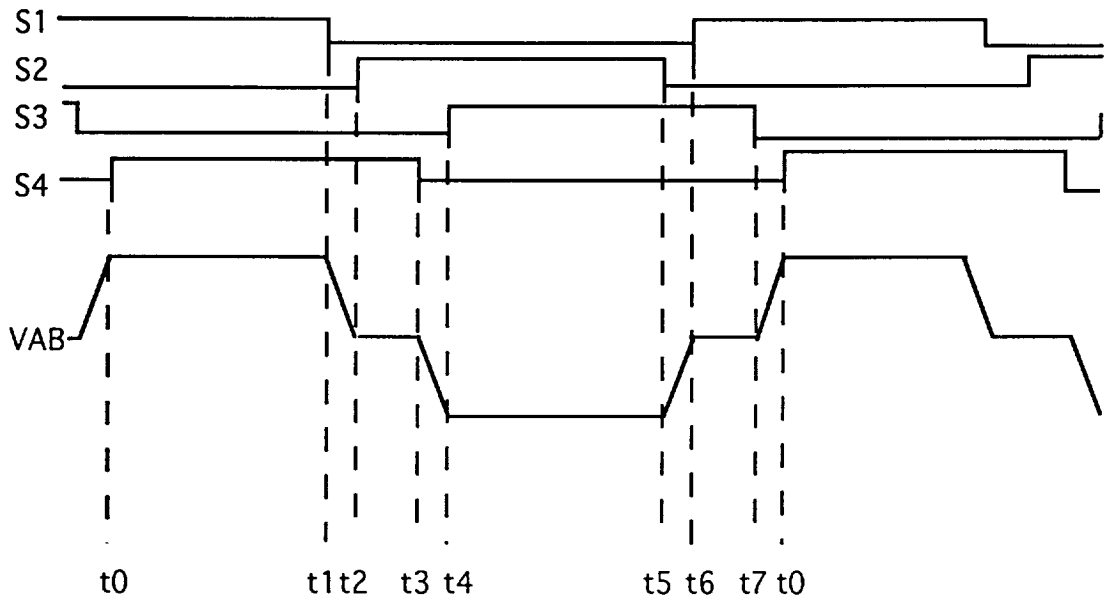

Figure 66. Switching signals for phase-shifted PWM.

The width of the interval from t0 - t1 depends on the amount of phase shift between the switching signals for S1 and S4. The phase shift between S2 and S3 is the same as that for S1 and S4. Control of the output voltage is then achieved by varying the length of intervals t0 - t1 and t4 - t5. In order to prevent a dc bias on the transformer core, the length of these two intervals should be the same. The output voltage is directly proportional to the length of these intervals; as a result, this circuit is referred to as a buck-derived converter.

A resonant converter could have been selected for this application, since it is possible to achieve zero voltage/current switching with this type of converter. Each of these converters contains a network of inductors and capacitors which is connected between the source and the load. One method of control for these converters is frequency control, where the switching frequency is varied in relation to the resonant frequency. The value of capacitance affects the resonant frequency of the circuit. As a result, if the capacitance varies with temperature, then the resonant frequency will also vary making control more difficult. Capacitors with large capacitance values (1 μF and greater) are very sensitive to temperature, decreasing with increasing temperature. On the other hand, capacitors with small values (less than 0.1 μF) are relatively insensitive to temperature variations. Large capacitances would typically be used in resonant converters, whereas small capacitances are suitable for the lossless snubber applications of the circuit of Figure 65. Since it is the goal of this project to place as much of the circuit as possible in the oven, resonant converters were eliminated from consideration because of this capacitance variation.

The dotted box of Figure 65 indicates those components that were tested at elevated temperature. The lossless snubber capacitors have been included in the dotted box but are not currently being utilized because of the difficulty in locating high temperature capacitors with the necessary current rating.

The first prototype constructed was designed for operation at approximately 100 W output. Switches S1-S4 in this prototype are International Rectifier's IRF044 MOSFETs. This device is rated for 60 V and 30 A at a case temperature of 25° C. It is not rated for operation above a case temperature of 175° C. Diodes D1-D4 are Motorola's MUR5015 ultrafast diodes with voltage and current ratings of 50 A and 150 V, respectively, and a maximum junction temperature of 175° C. The intrinsic diodes of the MOSFETs could have been used, but the efficiency of the circuit increased with the addition of external diodes D1-D4. The center-tapped transformer was designed using a Magnetics powdered iron core (part no. 58867-A2-4). It has 22 turns on the primary and 44 turns on each of the secondary windings. The magnetizing inductance of this transformer is 54 μH; this value was relatively insensitive to variations in temperature. The output diodes are also MUR5015 diodes. The inductance in the output filter, which also is necessary to achieve zero-voltage switching, is composed of 45 turns on a Magnetics core (58867-A2-4) and has an inductance of 136 μH. The filter capacitance is 330 μF. A Unitrode UC3875 control chip is utilized to produce the switching signals for S1-S4 [3]. The control chip connections are shown in Figure 67.

With an output voltage of 42 V and a load resistance of 15 Ω, the output power for this prototype is actually 117.5 W. Figure 68 gives a plot of the efficiency versus ambient temperature. This data was recorded in the following manner. The oven temperature was adjusted to the desired value. After thirty minutes at this temperature setting, voltage and current measurements were taken with digital multimeters and then the temperature was moved to the next setting. Note that the efficiency starts at 90.6% for a temperature of 20° C and decreases to 88.7% at 200° C. The efficiency numbers may be improved slightly through the addition of capacitors Cs1 - Cs4. The power required for the control circuitry is also included in calculating the efficiency data.

Life testing of this prototype was undertaken next. This prototype was operated at 117.5 W and at a temperature of 200° C for a period of 1000 hours without failure. The efficiency held constant at 88.7% during this test period. The output voltage remained at 42 Vdc throughout the test.

Figures 69 - 71 show waveforms for this circuit operating at 200° C at the end of the life test. The transformer input voltage is shown in Figure 69. This waveform contains some ringing produced by parasitic capacitances and inductances in the circuit. This ringing could be reduced by the addition of some capacitance across the input to the H-bridge, as was seen in a room temperature version of this prototype. Suitable high temperature capacitors were not available for oven operation. Some of the ringing may also be produced by the test probe which must be inserted into the oven, since the oscilloscope leads are not able to withstand 200° C operation.

Figure 70 and 71 show V_{ds} and I_d versus time for S1 and S3, respectively. The current I_d includes the current flowing through the discrete diode added to the circuit. Note in Figure 70 where the voltage goes to zero and the current begins to increase. This illustrates zero-voltage turn off of switch S1. Switch S3 also turns off at zero voltage as seen in Figure 71. The spike in the voltage waveform for S1 just before the voltage goes high appears during operation at 200° C and is not present for room temperature. Adjustments in the gate drive circuit should eliminate this. Figure 71 shows a negative current pulse which indicates current flow through the discrete MUR5015 diode. S3 is turned on at zero voltage during this interval.

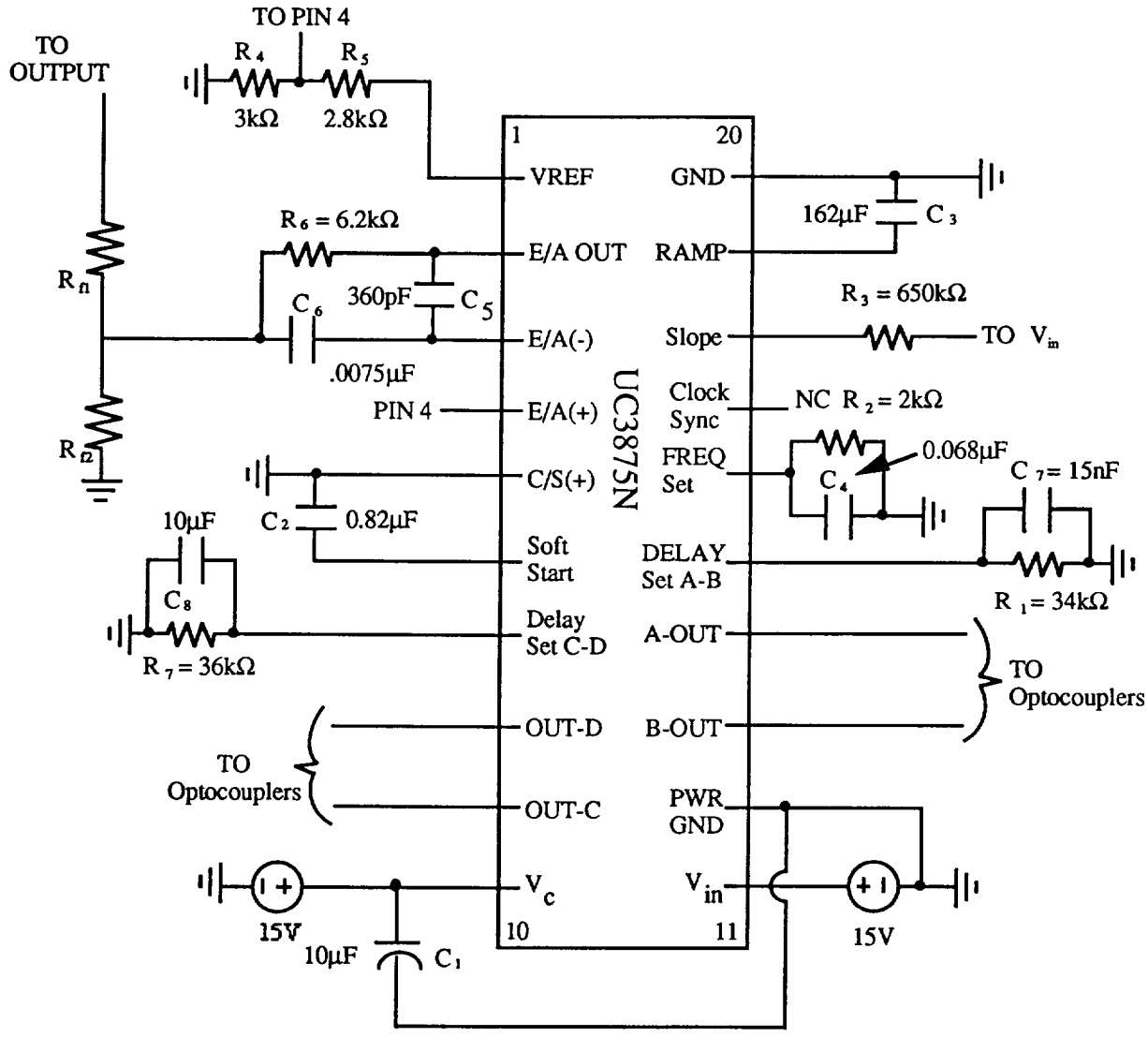

Figure 67. Control chip connections for 100 W unit.

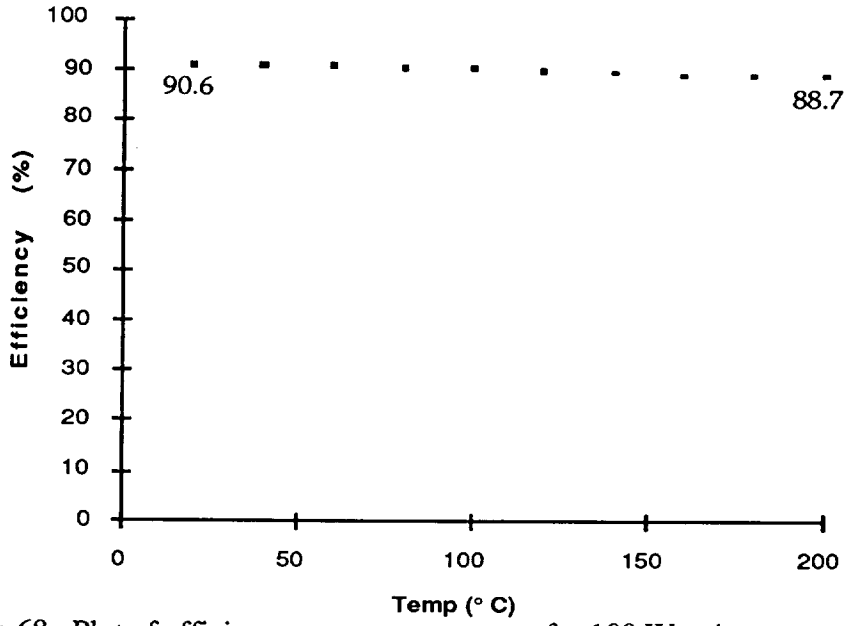

Figure 68. Plot of efficiency versus temperature for 100 W unit.

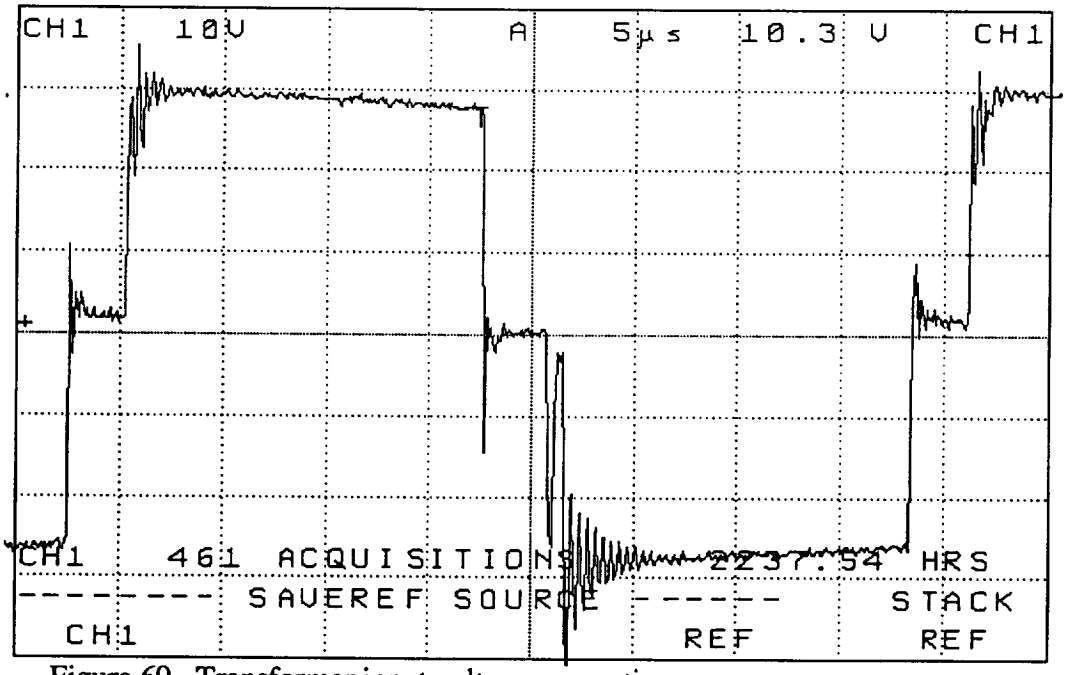

Figure 69. Transformer input voltage versus time.
(10 V/div, 5 µs/div)

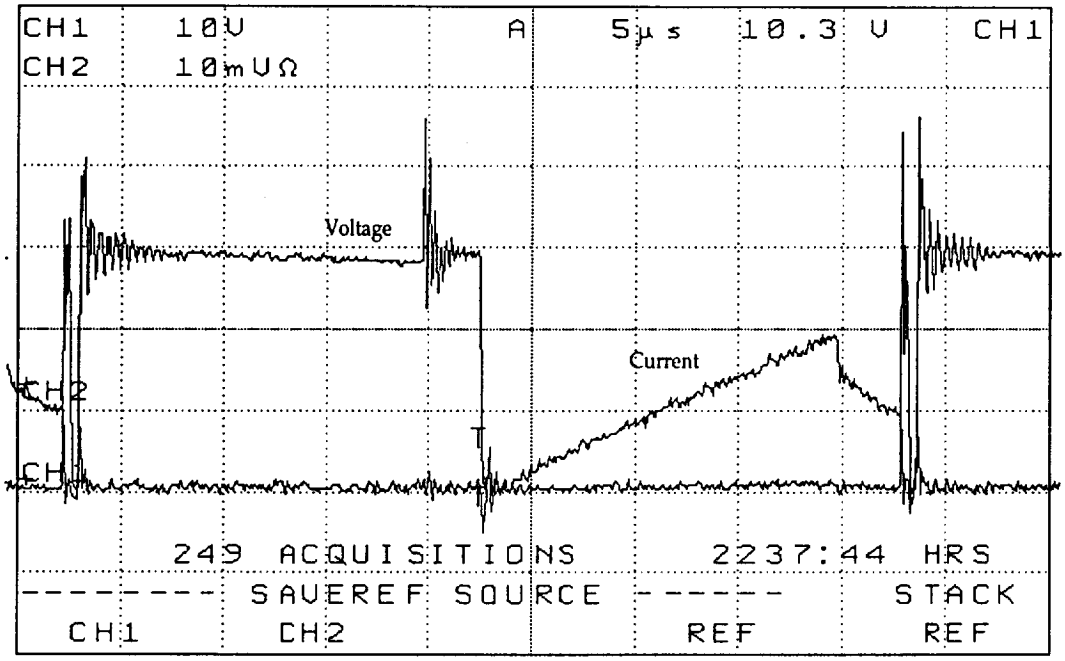

Figure 70. V_{ds} and I_d versus time for S1.
(10 V/div, 5 A/div, 5 µs/div)

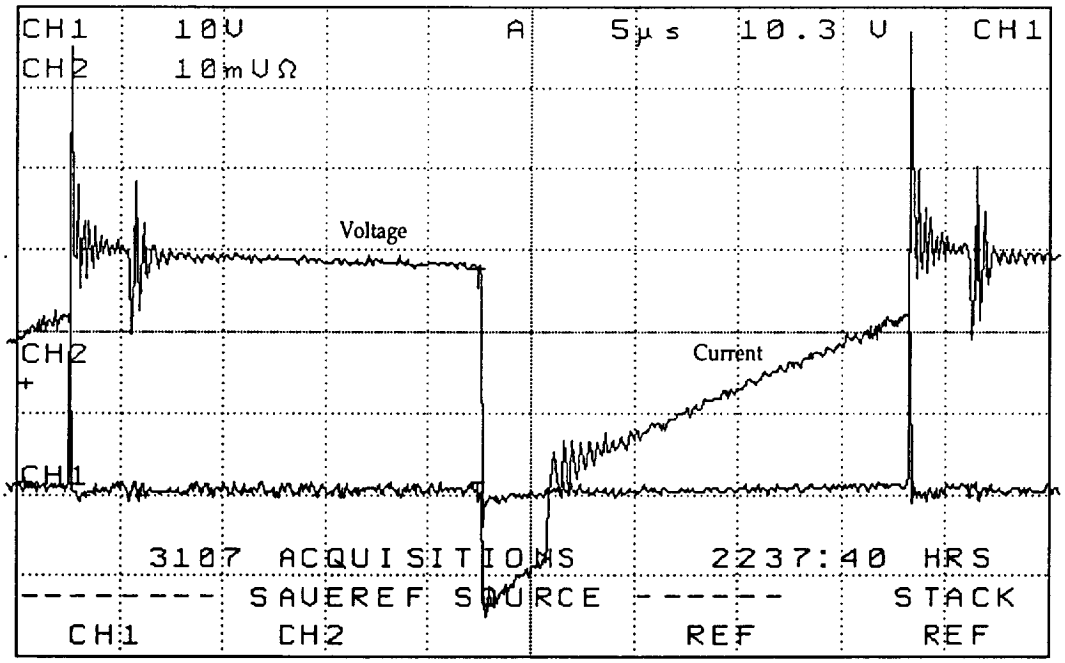

Figure 71. V_{ds} and I_d versus time for S3.
(10 V/div, 5 A/div, 5 µs/div)

A 500 W prototype using the circuit topology in Figure 65 has also been constructed and tested. Each MOSFET shown in Figure 65 is actually composed of 2 IRF044 International Rectifier MOSFETs connected in parallel, which reduces the conduction losses associated with these devices thus improving the efficiency. The control circuit of Figure 67 is modified only slightly for operation at this power level.

The transformer used in the 100 W prototype was not capable of handling the increased power level. A new transformer was designed which used a Magnetics Square Permalloy Tape Wound core housed in an aluminum case. The tape for this core has a thickness of 0.001 in. and a width of 1.0 in. The primary winding is composed of 6 turns of four 10 AWG teflon-coated conductors, while each secondary winding consists of 12 turns of one 12 AWG teflon-coated conductor.

The efficiency of this prototype was also measured as the temperature is varied from 20 °C - 200 °C. Figure 72 is plot of the efficiency versus temperature. The input and output currents of the prototype were measured using 50 A current shunts. The input and output power were then calculated using measurements of the input and output voltage. The power required by the control circuitry is also included in the efficiency calculations. The converter was operated at each temperature level for 30 minutes before any voltage and current measurements were recorded. As can be seen from this plot, the efficiency varied less than 1% over the range of temperatures.

This prototype has also undergone life testing. The unit has operated for more than 1000 hours at 200 °C. The efficiency has held constant at 85.8% while the output voltage has remained at 42 Vdc.

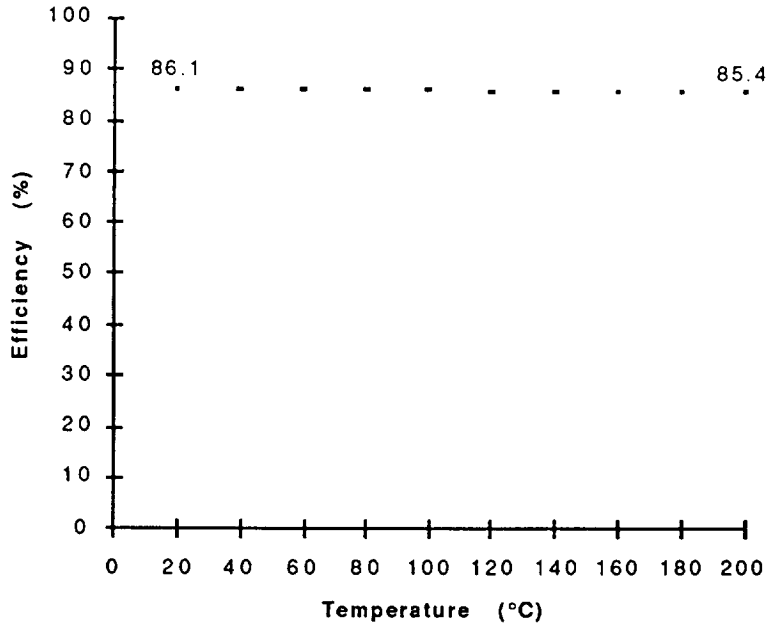

Figure 72. Efficiency versus temperature for the 500 W unit.

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