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## Spacecraft Optical Disk Recorder

### Memory Buffer Control

by

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### Abstract

This paper discusses the research completed under the NASA-ASEE summer faculty fellowship program. The project involves development of an Application Specific Integrated Circuit (ASIC) to be used as a Memory Buffer Controller (MBC) in the Spacecraft Optical Disk System (SODR). The SODR system has demanding capacity and data rate specifications requiring specialized electronics to meet processing demands. The system is being designed to support Gigabit transfer rates with Terabit storage capability. The complete SODR system is design to exceed the capability of all existing mass storage systems today. The ASIC development for SODR consist of developing a 144 pin CMOS device to perform format conversion and data buffering. The final simulations of the MBC were completed during this summer's NASA-ASEE fellowship along with design preparations for fabrication to be performed by an ASIC manufacturer.

### I. Project Goals

The goal of this project is to develop an Application Specific Integrated Circuit (ASIC) for use in the control electronics of the Spacecraft Optical Disk Recorder (SODR). Specifically, this project is to design an extendable memory buffer controller ASIC for rate matching between a system Input/Output port and the SODR's device interface.

The aforementioned goal can be partitioned into the following sub-goals:

- 1) Completion of ASIC design and simulation,
- 2) ASIC Fabrication (@ ASIC manufacturer),
- 3) ASIC Testing (NASA/LaRC, CNU).

### II. Project Description

My research activities during my NASA-ASEE fellowship have been part of the SODR project in the Flight Electronics Division. The SODR project will develop a space qualified optical disk storage system for mass storage and high data rate applications. The system architecture calls for a reconfigurable and extendable optical disk storage system. A multiport system will support terabit capacity and gigabit transfer rates. The disk drive (two devices) requirements call for 10 Gbytes of disk capacity and sustained data rates of 300 Mbps. The high level SODR system architecture is shown in Figure 1.

The specific system being developed in this project is the Memory Buffer Controller (MBC). The function of the MBC is to interface a system I/O port to a SODR device (note each optical disk drive is two devices). Since the instantaneous data rates of the I/O port and the SODR device may vary, a buffer memory is required for data rate matching between these two interfaces.

The current MBC system design calls for an 8-bit data path which is cascadable to support a 32-bit HPPI (High Performance Parallel Interface) data I/O port. The HPPI data port (or multiple HPPI data ports) will be the data I/O path for the SODR system. The MCB's SODR device interface is currently designed to support SCSI II protocol (16-bit, fast). Both interfaces selected have ANSI standards and support the high data rates specified by the SODR system requirements.

Functionally, the MBC ASIC decomposes into the following sections:

- 1) The HPPI source and destination interface,
- 2) The SCSI II interface to the optical disk recorder,
- 3) The Group Controller interface for MBC control and testing,
- 4) The memory buffer interface,
- 5) The MBC system controller.

Figure 2 shows the MBC ASIC with all the major interfaces in a 32-bit I/O port configuration.

### **III. NASA-ASEE Summer Research Activities**

This summer activities are part of my second NASA-ASEE fellowship. The research started last summer with activities which included:

- 1) System architecture development,
- 2) Interface definitions,
- 3) Memory subsystem design & simulation,
- 4) Control algorithm development.

This summer provided the opportunity to simulate the system design. Digital simulations of the MBC system were performed using the Cadence Design Tools and the Verilog-XL simulator. Extensive tests were run to verify correct operation under a variety of conditions. Functional test were performed under minimum/typical/maximum timing conditions. Test vectors for manufacturer testing were also generated. Critical timing issues were resolved and preparation for manufacturer's sign-off were made. In the near future the MBC ASIC will be sent to US2 for fabrication. The final product will be a 144 pin custom CMOS ASIC with a 50 MHz maximum clock frequency.

Post layout simulations and post fabrication testing still remain to be done and are planned for this Fall. This summer's NASA-ASEE fellowship has grown into additional grant work with NASA and has furthered the relationship between NASA and Christopher Newport University.

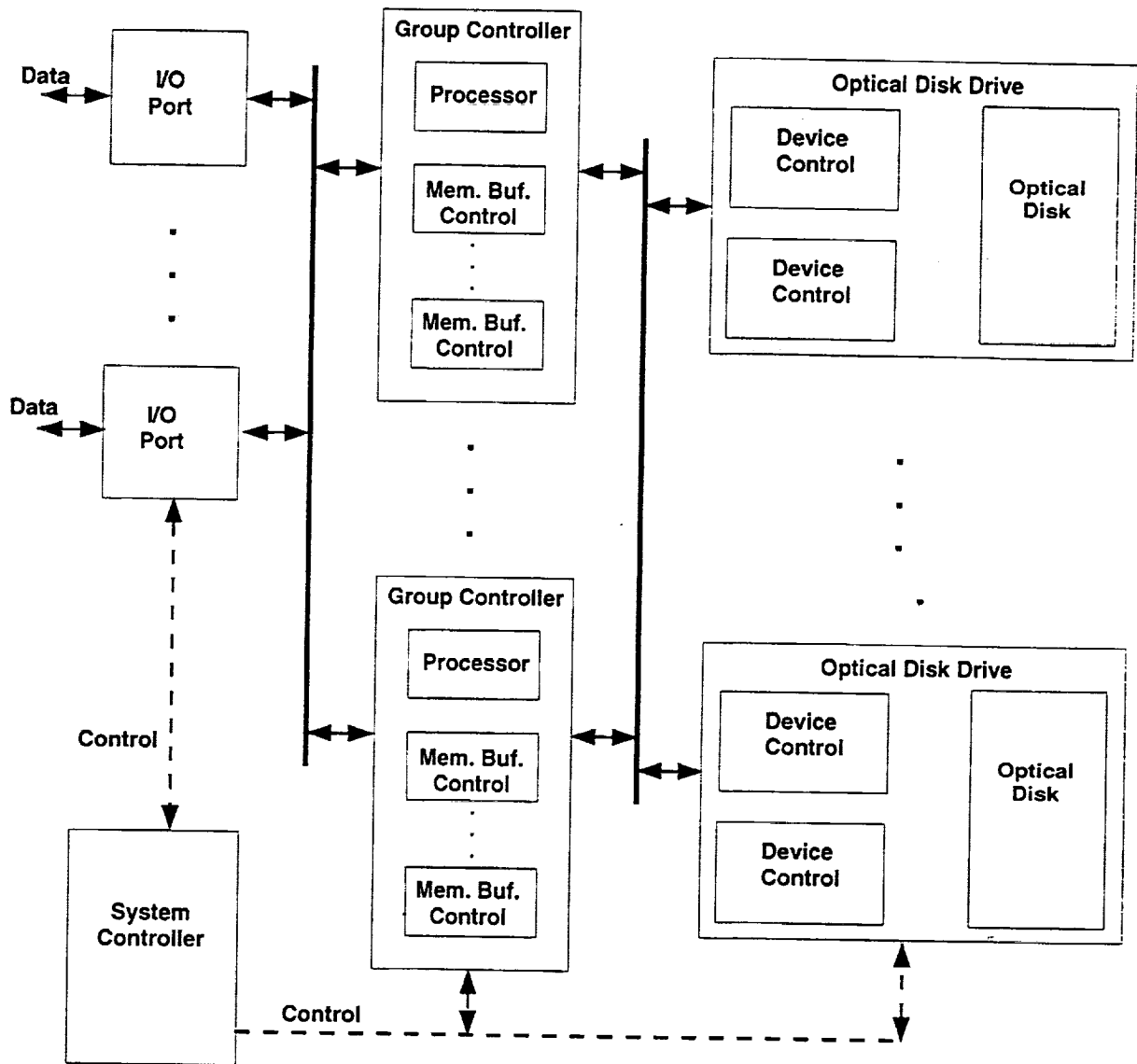
The MBC ASIC is the first custom integrated circuit being developed by the Flight Electronics Division. Therefore almost as important as the device itself, is the process used to design it. Many lessons were learned in the development process which will make future ASIC development much easier. Problems in the design flow have been identified and are being addressed for future projects. Issues of testability, fault coverage and configuration management have been raised by the development of the MBC ASIC. Future projects are sure to benefit from the knowledge gained through the design of this system.

#### **IV. ASEE Related Issues**

In addition to my research activities, I had the opportunity to use a powerful set of design tools for ASIC development. The use of these tools will extend to the classroom for both undergraduate and graduate courses. Contacts made during my NASA-ASEE fellowship have, in-part, made it possible to bring these tools into a university environment.

#### **V. Acknowledgments**

Special thanks to Tom Shull (my associate), Steve Jurczyk, and other members of the SODR team for their help and encouragement.



**Figure 1. SODR System Architecture**

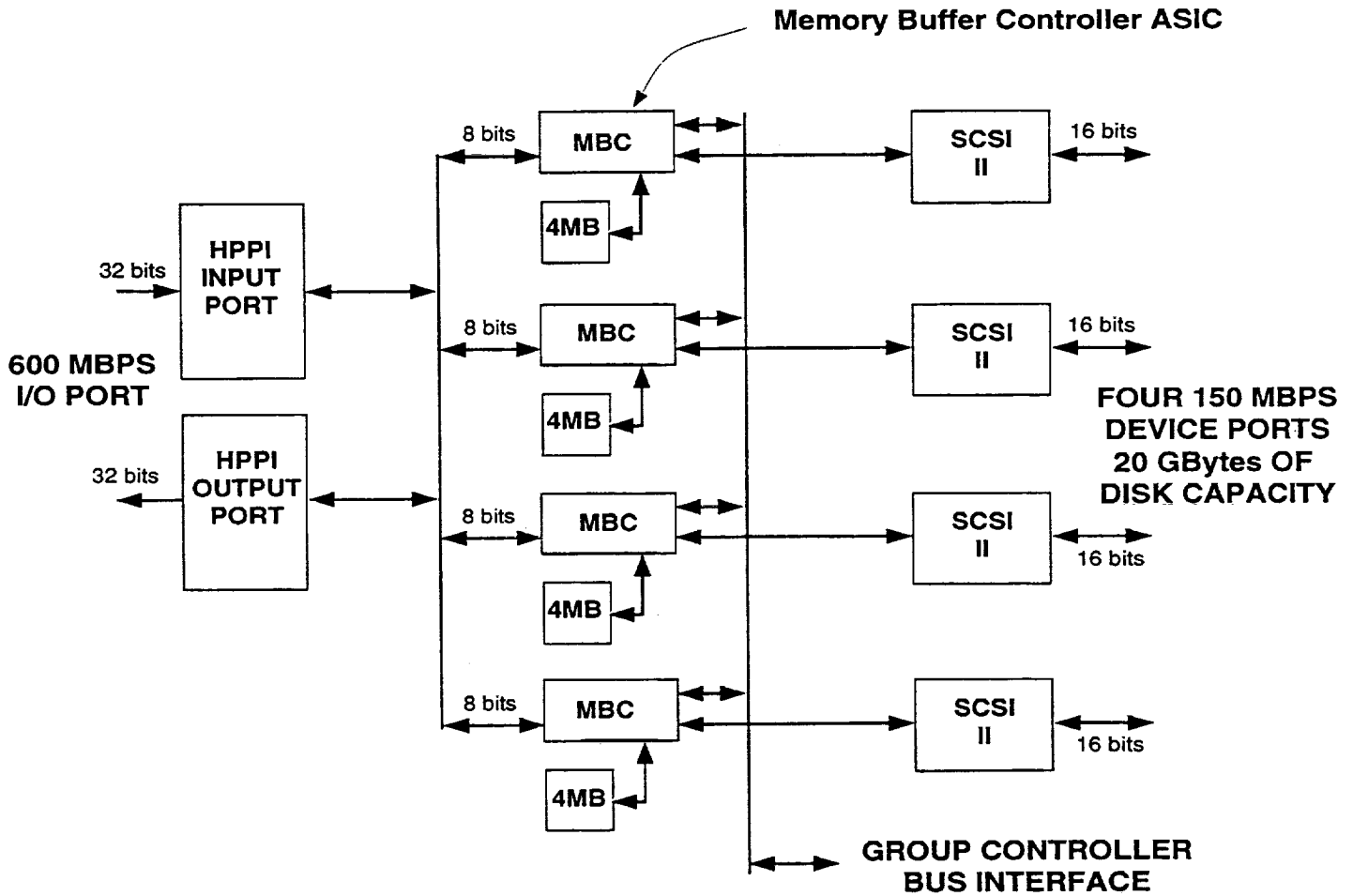


Figure 2. MBC with 32-bit HPPI and 16-bit SCSI