JPL D-1272

Product Evaluation Report

NSC 800, 8-Bit CMOS Microprocessor

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PREFACE

This evaluation has been performed in order to gain a first-hand knowledge of and insight into this product's inherent material structures and its functions; to assess the relative quality of materials, together with pattern design; and to reveal possible flaws. Subsequently, this report should be useful in the establishment of reliability criteria for this process technology, for related device types, and for analysis of failed parts.

The work described in this report was performed by Steve Suszko, JPL Parts Engineering, Section 514.

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SECTION 1
INTRODUCTION

1.1 DEVICE DESCRIPTION

The NSC 800 is an 8-bit CMOS microprocessor manufactured by National Semiconductor Corp., Santa Clara, California. The 8-bit microprocessor chip with 40-pad pin-terminals has eight address buffers (A8-A15), eight data address -- I/O buffers (AD_0-AD_7), six interrupt controls and sixteen timing controls with a chip clock generator and an 8-bit dynamic RAM refresh circuit. The 22 internal registers have the capability of addressing 64K bytes of memory and 256 I/O devices.

The chip is fabricated on N-type <100> silicon using self-aligned polysilicon gates and local oxidation process technology. The chip interconnect consists of four levels: 1) Aluminum; 2) Polysi 2; 3) Polysi 1; and 4) P^+ and N^+ diffusions. The four levels, except for contact interface, are isolated by interlevel oxide. The chip is packaged in a 40-pin dual-in-line (DIP), side-brazed, hermetically sealed, ceramic package with a metal lid.

The operating voltage for the device is 5 V. It is available in three operating temperature ranges: 0 to +70°C, -40 to +85°C, and -55 to +125°C.

1.2 DOCUMENT USES

Two devices were submitted for product evaluation by F. Stott, MTS, JPL Microprocessor Specialist. The devices were pencil-marked and photographed for identification as shown in Figures 2-1 and 2-2.

For detailed information see Section 2, External Examination; Section 3, Electrical Design Analysis; Section 4, Die Materials Evaluation; Section 5, Chip Cross-Sectioning; and Appendix A, Manufacturer's Specification Data Sheets.

SECTION 2

EXTERNAL EXAMINATION

2.1 EXTERNAL VISUAL INSPECTION

The two devices were examined per MIL-STD-883B, Method 2009.1, for integrity of package seal, lead terminals and any evidence of damage. The package markings are identified on metal lids and on the bottom as shown in Figures 2-1, 2-2, and 2-3.

2.2 PACKAGE DIMENSIONS

Package dimensions.	(inch)	(mm)
Length:	2.020	51.308
Width:	0.610	15.49
Thickness with lid:	0.150	3.81
Lead dimensions.		
Length:	0.125	3.175
Width:	0.015	0.381
Thickness:	0.008	0.203
Lead spacing:	0.100	2.540

2.3 HERMETICITY TEST

The devices were placed in a helium pressure container with pressure set at 35 psi (He) for a duration of 18 hours. Thirty minutes after removal of the two devices from the chamber, fine and gross leak tests were performed per MIL-STD-883B, Method 1014.2. The gross leak test was performed in fluorcarbon (FC-43) liquid at +125°C.

Results: No leaks were observed.

2.4 X-RAY RADIOGRAPHY

X-ray photographs of each package are shown in Figure 2-4 and 2-5. Top views display each package lead frame of the ceramic sandwich with a rough outline of a package cavity with a chip, with no detectable signs of voids in the die attach.

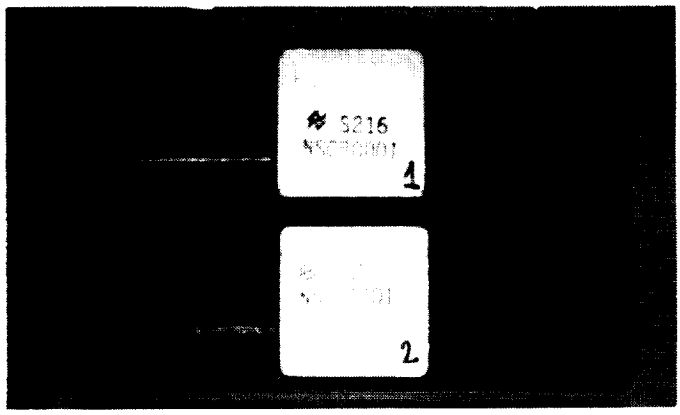


Figure 2-1. 1.4X top view of two devices with markings on metal lids.

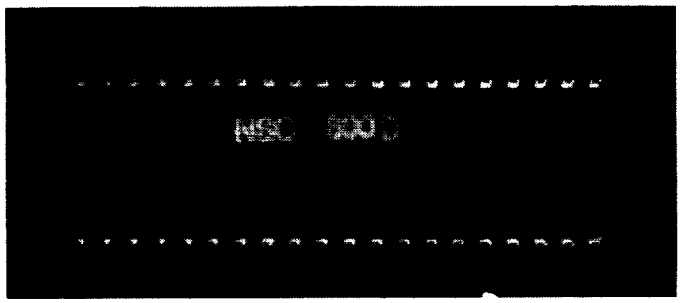


Figure 2-2. 1.4X bottom view of device with markings.

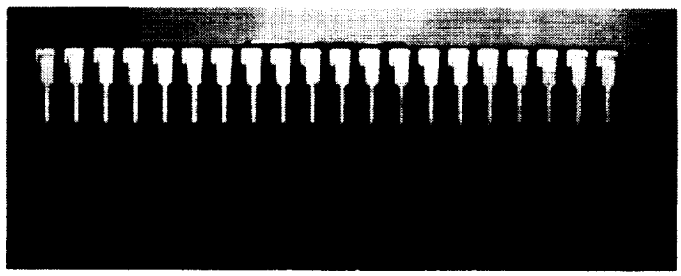


Figure 2-3. Side view of device with side brazed package lead terminations.

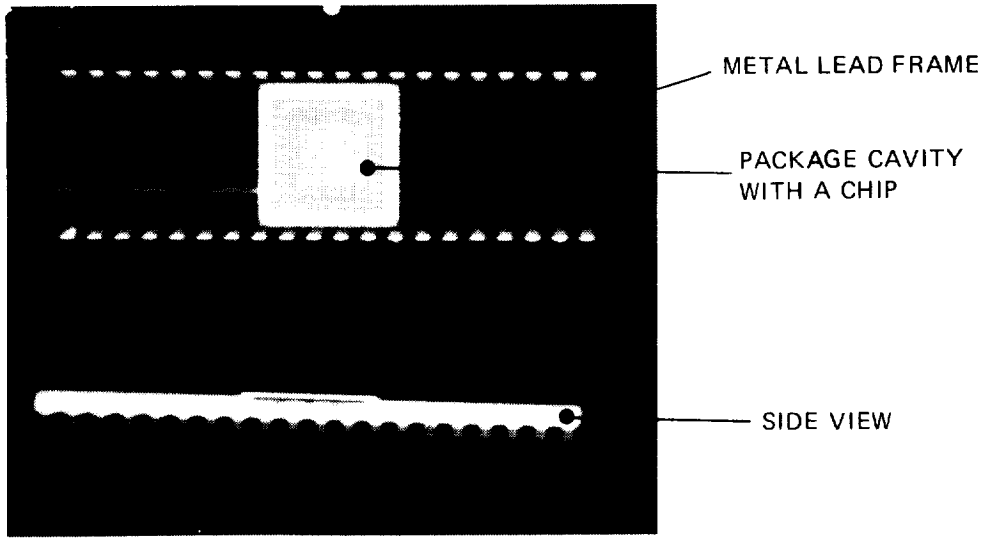


Figure 2-4. 1.4X magnified top and side X-ray view of device No. 1 package lead frame and die cavity.

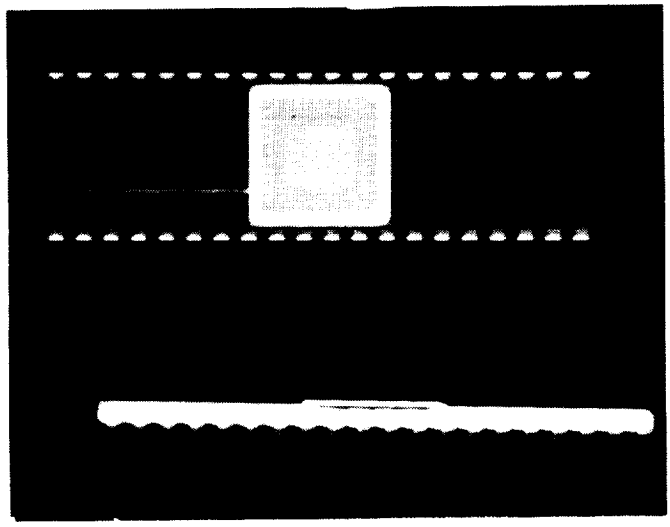


Figure 2-5. 1.4X magnified top and side X-ray view of device No. 2 package lead frame and die cavity.

2.5 INTERNAL EXAMINATION: DELIDDING

The two devices were delidded on a wet sanding disk by grinding off the metal lid to the thickness which made it possible to peel the metal off with an X-Acto knife.

Figure 2-6 displays an example of a delidded package cavity with an exposed silicon chip, outline of a gold-eutectic die attach and wire bonds from die pads to package lead frame.

Figure 2-7 is a 13X optical view of a chip metallization pattern.

2.6 OPTICAL AND SEM EXAMINATION AFTER DELIDDING

(Before protective passivation removal)

The exposed die cavity of each device was examined, both with an optical microscope and with a Scanning Electron Microscope (SEM) in order to determine quality of workmanship, assembly technique and cleanliness, per MIL-STD-883B, Method 2010.3. The die passivation, wires to die pads and package lead frame and die attach fillet were inspected.

Optical Figure 2-8 shows a magnified 29X view of a passivated microprocessor chip with identified (ccw) pads 1, 20, and 40, and the complexity and symmetry of certain circuit patterns.

Figure 2-9 shows only a metallization interconnect mask, roughly identifying V_{SS} and V_{DD} bus distribution from pads 20 and 40. Optically, the chip passivation has a fair amount of transparency for examination to view the underlying metal interconnect, however, it does not help in identifying the cell pattern beneath and the polysi-gates definition.

SEM Figure 2-10 shows a corner of a die with saw and break dicing method and features of die attach, gold eutectic, fillet.

SEM Figure 2-11 shows typical thickness of SiO_2 passivation around perimeter of metal pad. SEM examination of wire bonds on die pads reveal wire bonding with acceptable wedge-type compression.

SEM Figures 2-12, 2-13 and 2-14 show representative examples of typical wire bonding on the die pads with identified perimeter of insulating SiO_2.

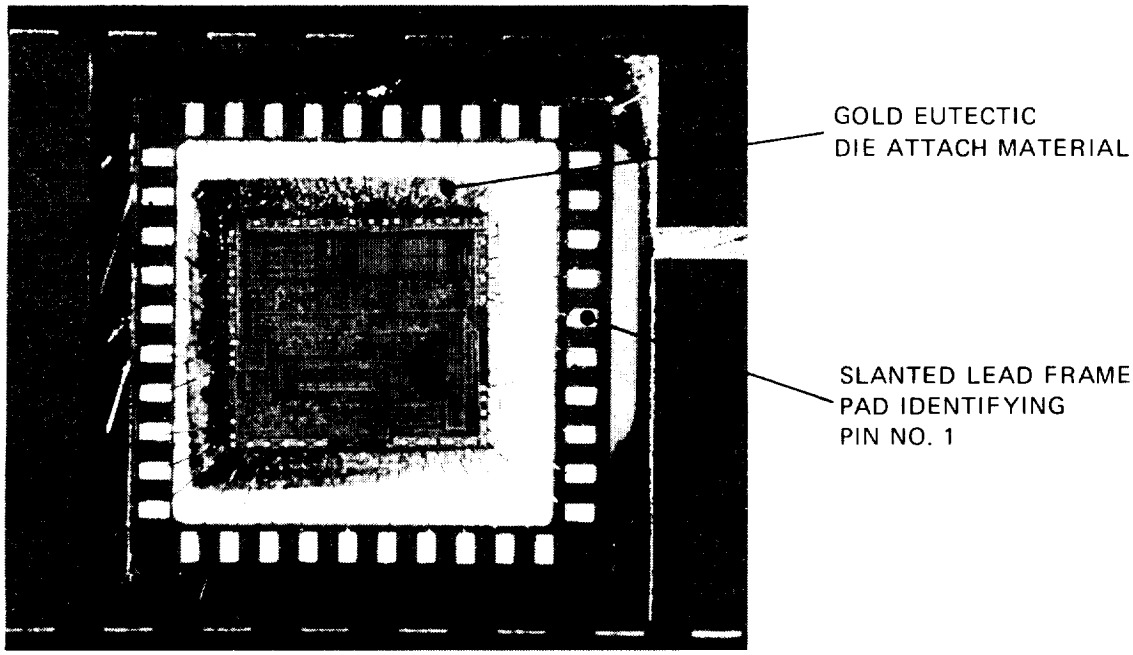


Figure 2-6. 4X optical view of delidded device lead frame cavity with die attach outline, and a die with wire bonds.

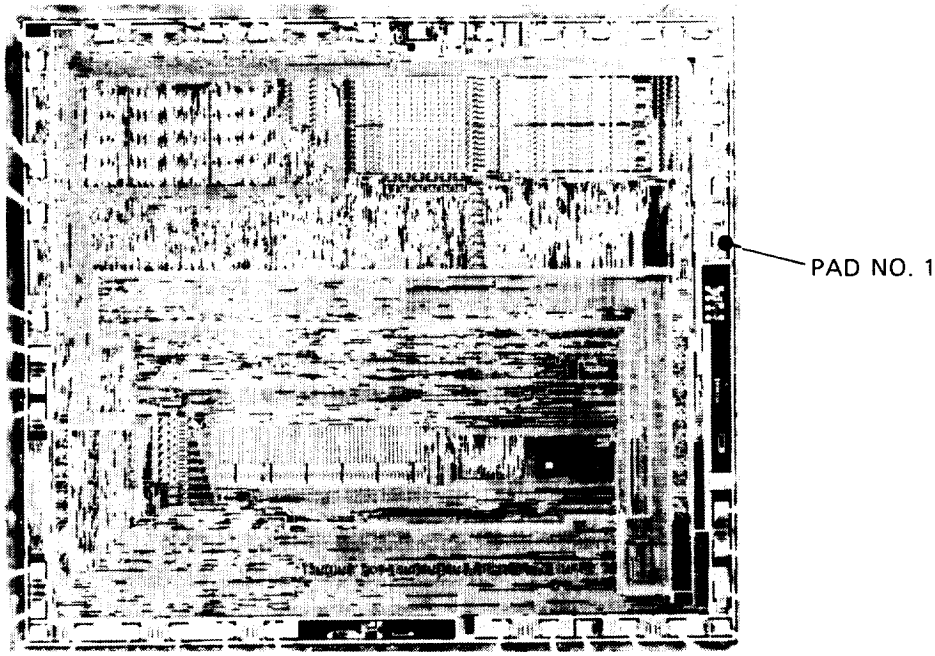


Figure 2-7. 13X optical view of passivated chip metallization interconnect pattern.

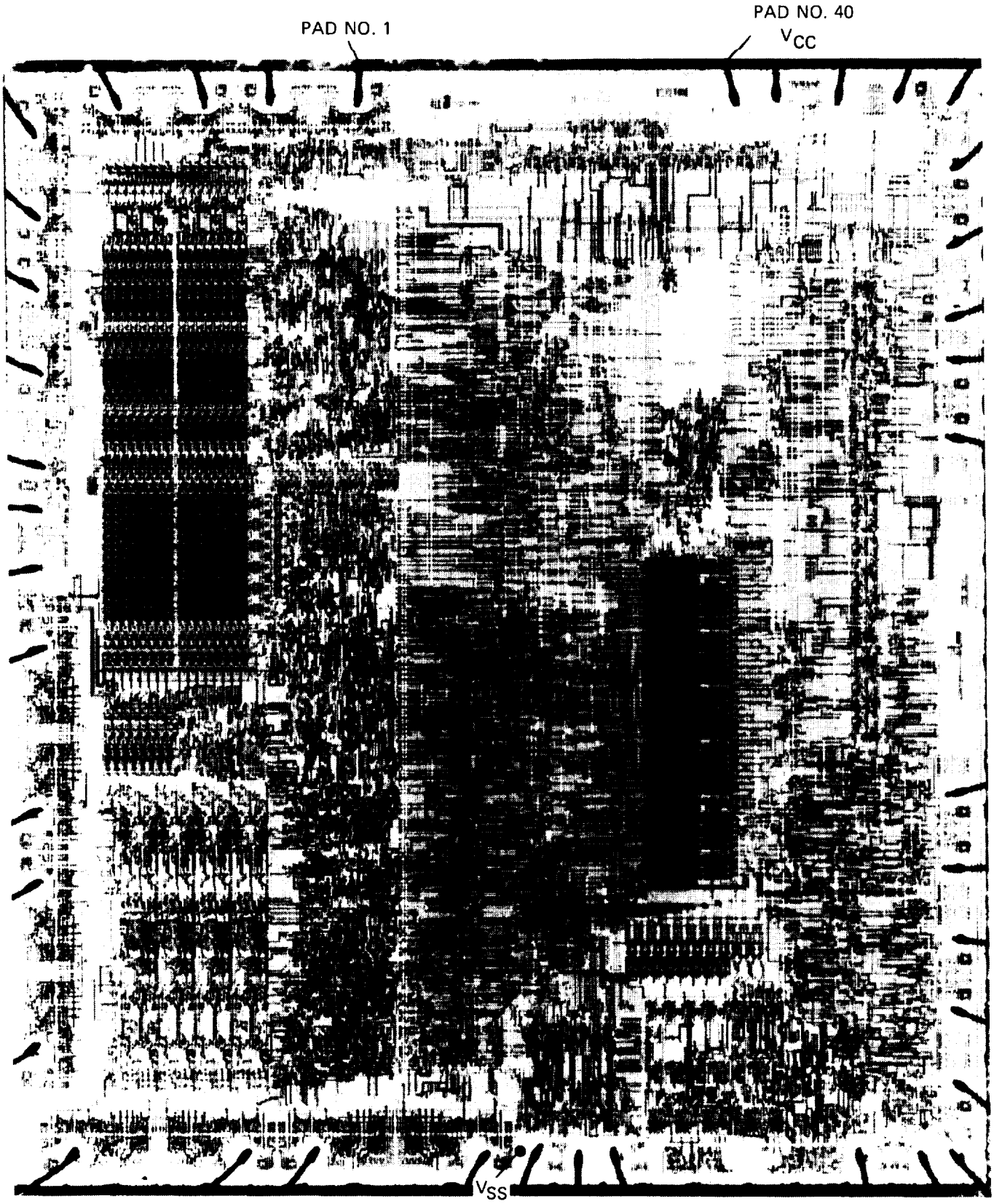


Figure 2-8. 29X magnified optical view of NSC 800 passivated microprocessor chip with patterns of logic cell blocks.

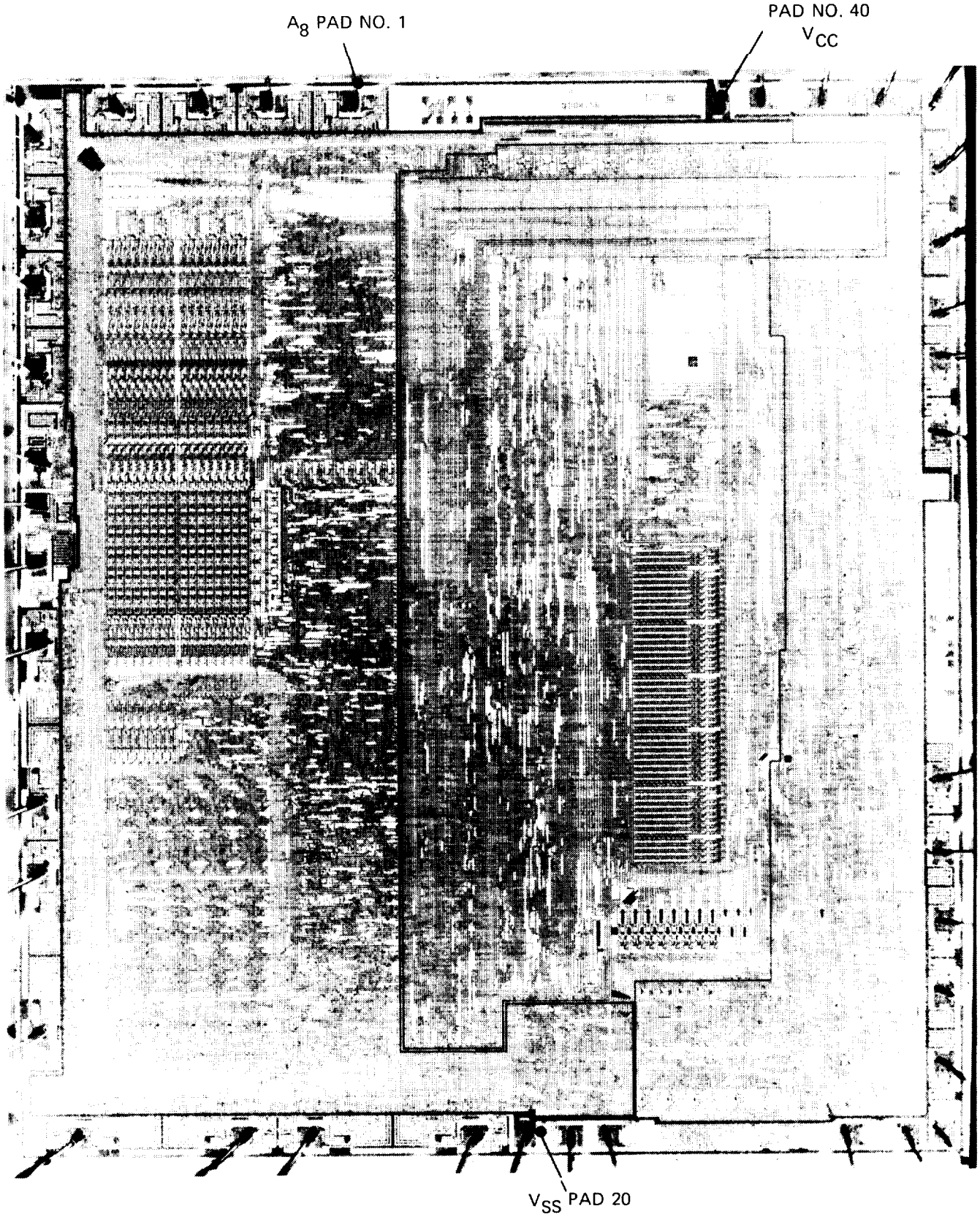


Figure 2-9. 29X optical view of NSC 800 microprocessor chip metallization mask only.

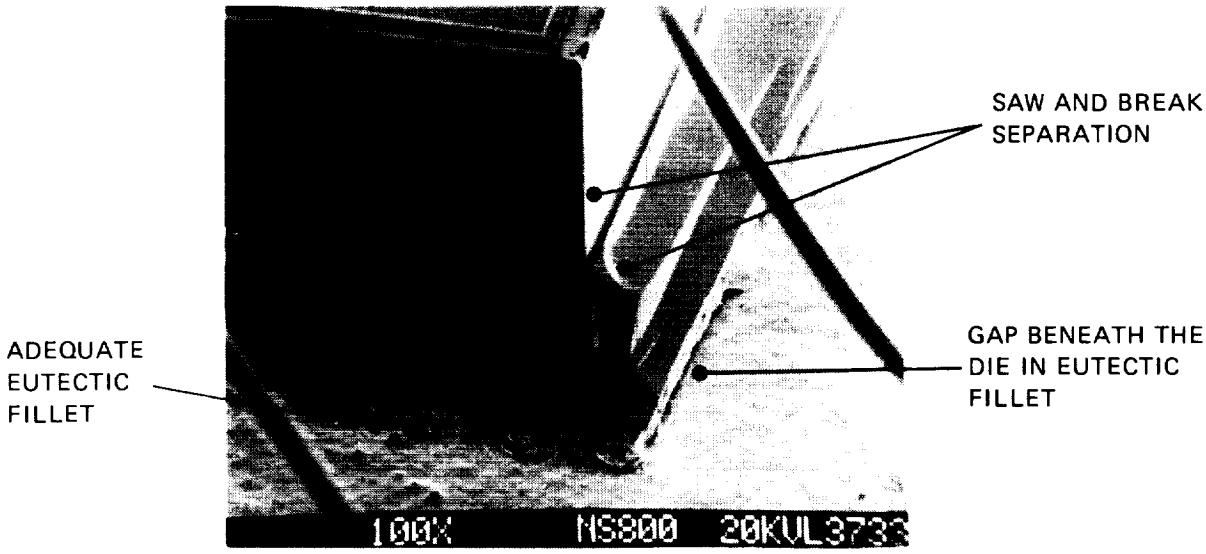


Figure 2-10. SEM view of die corner showing saw and break separation of silicon chip and gold eutectic fillet.

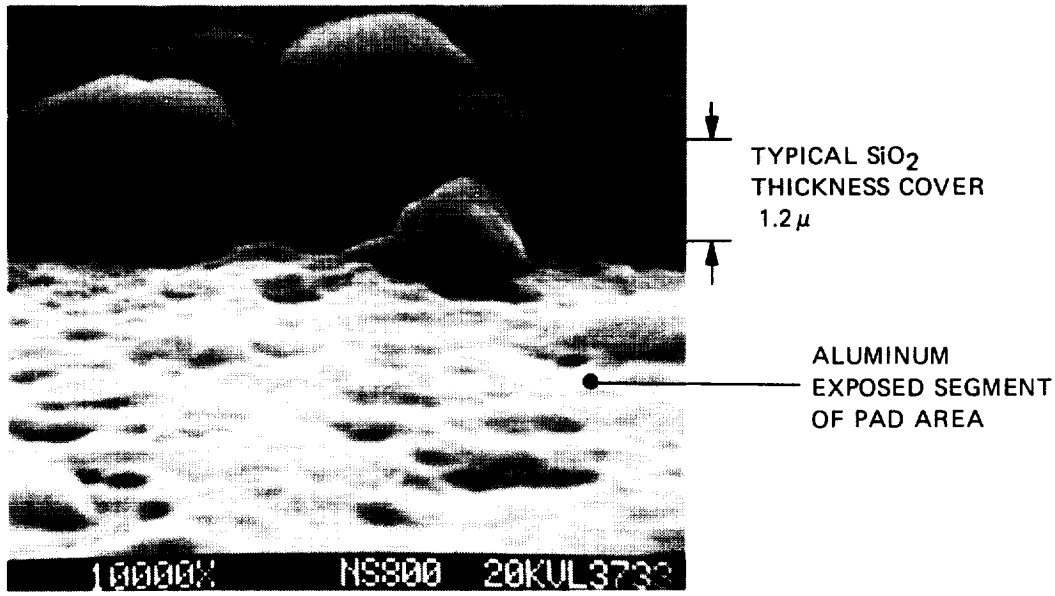


Figure 2-11. 10,000 magnified SEM view at 70^{o} tilt of top SiO_2 passivation thickness the chip.

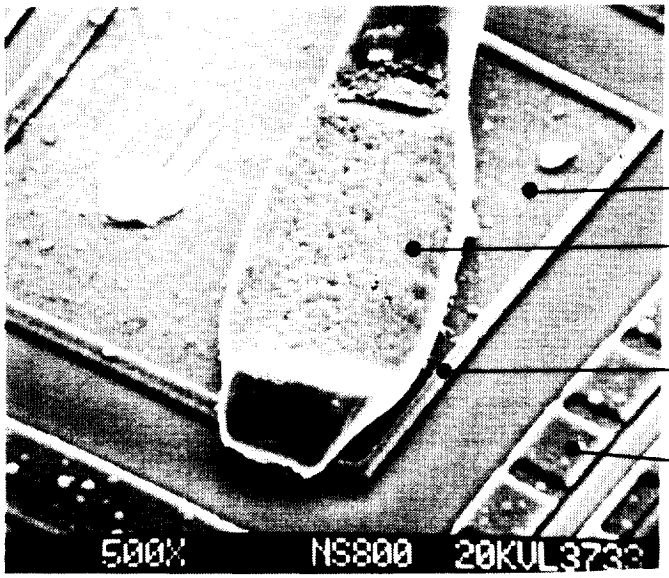


Figure 2-12. SEM view of aluminum die pad with glassivation perimeter and aluminum wire band.

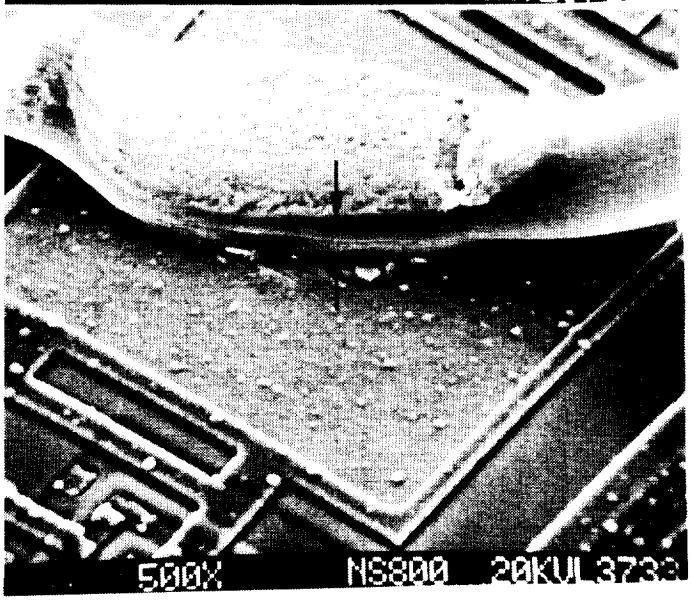


Figure 2-13. SEM side view of wire bond showing acceptable compression thickness.

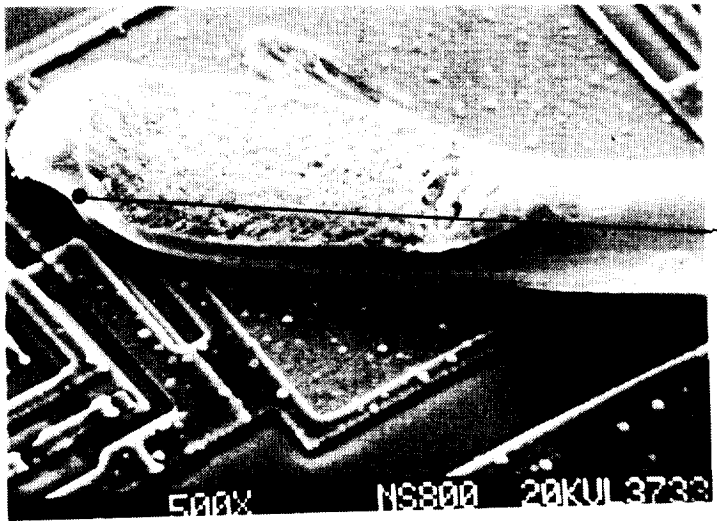


Figure 2-14. SEM view of a wire bond.

2.7 WIRE BOND PULL TEST

The wire bond pull test was performed per MIL-STD-883B, Method 2011.2 (prior to passivation removal). A strip chart recorder with a bond pull test setup calibrated in grams was used for the wire break test. The breaking stress for each bond is shown in Table I.

Table I. Wire Bond Pull Test (in Grams)

Pin No.	Device SN-1	Device SN-2		Pin No.	Device SN-1	Device SN-2
1	2.3	2.8		21	3.3	2.9
2	2.8	2.5		22	2.9	2.7
3	3.1	2.9		23	2.7	2.4
4	3.	3.1		24	3.4	3.1
5	2.7	2.5		25	3.2	2.9
6	2.2	2.6		26	3.7	3.2
7	2.6	2.9		27	3.	2.6
8	2.9	3.		28	2.8	3.
9	2.5	2.2		29	2.4	2.6
10	3.4	2.9		30	2.9	2.7
11	3.1	3.		31	3.2	3.
12	3.1	2.4		32	2.7	2.9
13	3.	2.7		33	2.3	2.5
14	2.6	2.2		34	2.8	2.9
15	2.9	3.1		35	2.9	3.6
16	2.7	2.9		36	3.1	3.4
17	3.1	3.		37	3.4	2.9
18	3.	2.8		38	3.	2.7
19	3.6	2.9		39	2.6	2.9
20	3.4	2.7		40	2.9	3.2

Note: Minimum acceptable breaking force for 1 mil aluminum wire is 2. grams.

2.8 SUMMARY AND CONCLUSIONS: PACKAGE ASSEMBLY AND BONDING INTEGRITY

The X-ray pattern of each package cavity with a die does not reveal any voids beneath each die. However, a SEM view of one die corner shows a small gap in die fillet (Figure 2-10). The wire bonding, both on the package lead frame and on the die pads, appears clean, with acceptable centering on pads and the thickness of compressed wire bonds.

The wire pull test of all wires in both packages appears to meet required pull strength above 2 grams.

SECTION 3

ELECTRICAL DESIGN ANALYSIS

3.1 INTRODUCTION

The overall pattern of an NSC 800 8-bit microprocessor chip with identified functional blocks is shown in Figure 3-1. A corresponding floor map is shown in Figure 3-2.

A functional block diagram, Figure 3-3, identifies the timing and interrupt control functions, chip internal data bus to arithmetic logic, instruction decoders and register arrays, and the address buffer block (A_8-A_{15}) and data address I/O block (AD_0-AD_7).

The NSC 800 microprocessor (P^2CMOS) utilizes a local oxidation process with two-level polysi and a metal interconnect. The chip contains approximately 11000 active components on N-type silicon. (See Section IV, Materials Analysis.) A complete description of the NSC 800 microprocessor pin-out functions and program instructions is in the manufacturer electrical specifications, Section VII.

NOTE: Due to very minimal circuit design information received from the manufacturer, only several circuit segments on the chip are shown together with diagrams and captions, without the benefit of a complete and detailed logic diagram.

3.2 DESIGN PATTERN AND FUNCTION

The first purpose of this design evaluation was to develop a simplified method of approach for physical circuit pattern identification and subsequent logic definition.

Several analyzed circuits are presented as an example to show the usefulness, if need arises, for evaluating the entire physical design of the NSC 800 P^2CMOS (VLSI) microprocessor and for other NSC family of devices using P^2CMOS process technology. For a circuit analyst, the advantages of using such a method in the evaluation of VLSI-type chips are:

a. Being able to identify, and define in detail, segments of complex circuit patterns and translate them to functional logic regardless of availability of circuit information from the manufacturer.

b. When a selected circuit segment is defined, it is then possible to understand its function and the interface with other circuits on the chip.

c. In product qualification assurance for the VLSI chips, a working method is a necessary tool used in evaluation steps. The subsequent examples of reverse engineering methods used in (any) circuit design evaluation are well suited to define and identify complex VLSI circuit patterns.

Because the P^2CMOS process has a four-level interconnect (e.g., metallization, Poly 1, Poly 2, and P^+ and N^+ diffusions) the design analysis follows a sequence of steps with the exposure of separate materials pattern levels on down to P^+ and N^+ diffusions in silicon substrate for identification and validation of transistor patterns, contact interface and interconnect.

3.3 DARKFIELD MICROPHOTOGRAPHY PROCESS

The photographic examples of identified circuit segments were developed using darkfield microphotography and the photo results were processed from positive contacts. This method lends itself more precisely to identification and definition of very small, VLSI-type, microcircuit patterns. Thus, the several selected circuits in photo figures together with captions and diagrams present, in part, the complexity of identified circuit patterns, and a method for a complete circuit design analysis, together with materials level interface definition.

Specifically, using this approach helps when there is no available logic design information from the manufacturer.

The seven circuit patterns selected on the chip are referenced in Figure 3-4. These circuits magnified and identified in detail, together with captions and diagrams, are shown in Figures 3-5a through 3-13d as follows:

a. Circuit No. 1; POWER SAVE ($\overline{PS}$) function pad 39 is a typical CMOS input protection with a buffer and represents a pattern used in other 10 input functions on the chip. (Figures 3-5a thru 3-6c.)

b. Circuit No. 2; RESET OUT function pad 37 is a control buffer circuit pattern used in other 9 control functions on the chip. (Figures 3-7a thru 3-7d.)

c. Circuit No. 3; A_{11} address buffer, pad 4 is 1 of 8 address buffer logic patterns of (A_8-A_{15}) eight address buffers. (Figures 3-8a thru 3-8d.)

d. Circuit No. 4; AD_3 Data I/O buffer pad 15 is 1 of 8 I/O buffer patterns AD_0-AD_7. (Figures 3-9a thru 3-9d.)

e. Circuit No. 5; A register latch segment of 2 bistable latches of an 8-bit register. (Figures 3-10a thru 3-10e.)

f. Circuit No. 6; A register latch segment with read/write data enable gates of an 8-bit register. (Figures 3-11a and b.)

g. Circuit No. 7; Very small segment of a programmable logic array (PLA) with product buffers. (Figures 3-12a thru 3-12d.)

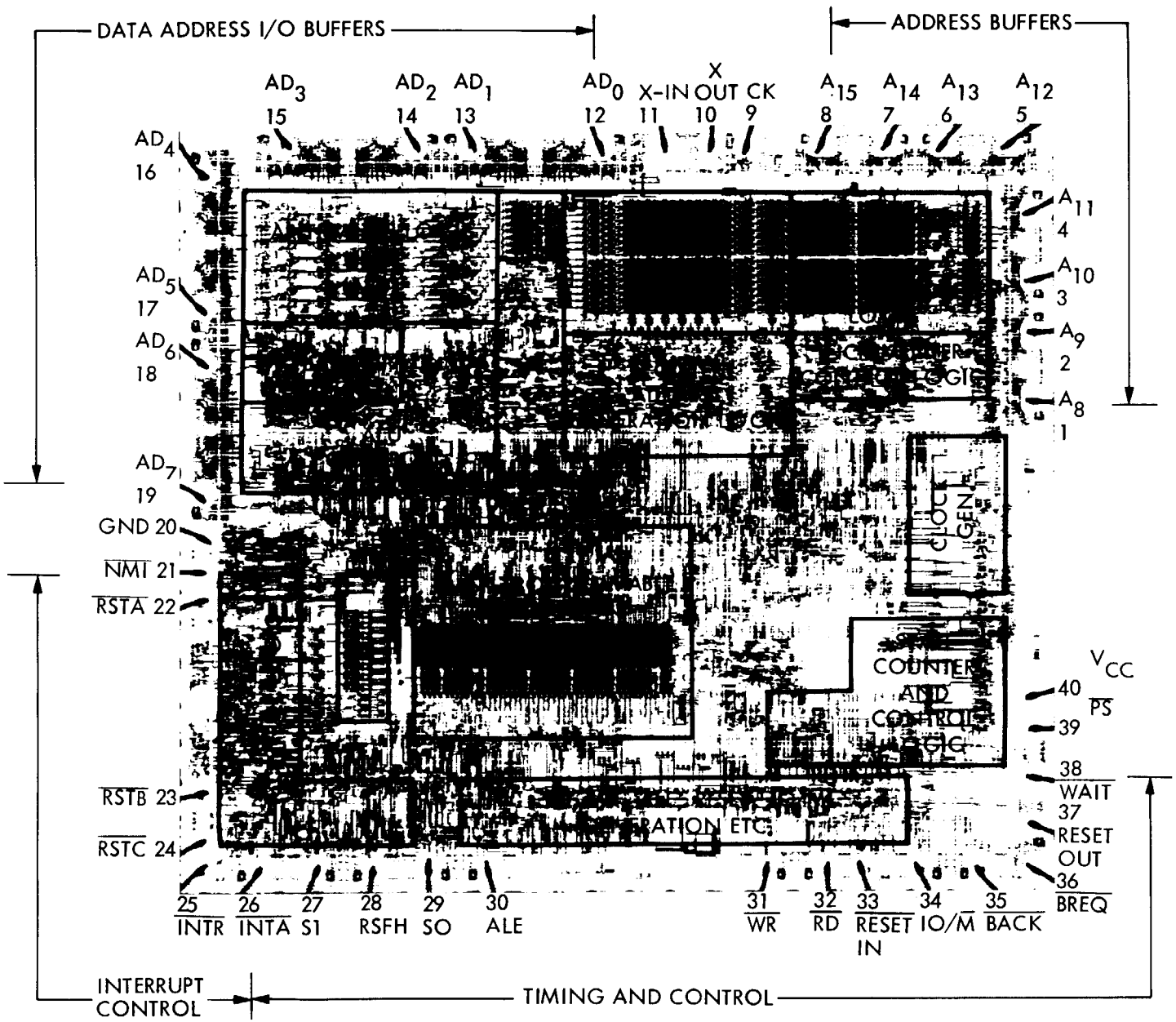


Figure 3-1. Optical figure of NSC 800 $\overline{G}$ 8-bit microprocessor chip with identified logic block functions.

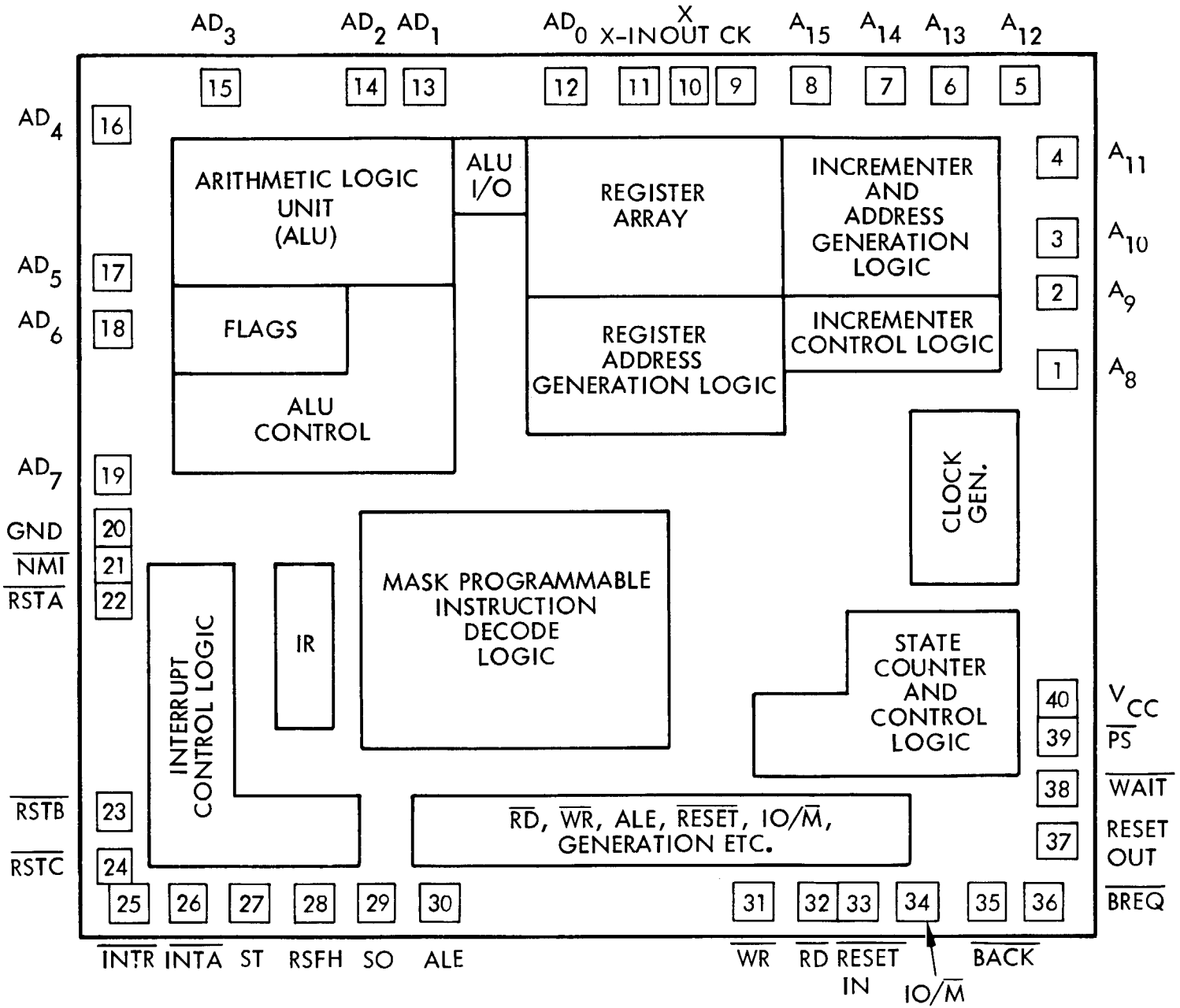


Figure 3-2. Floor map of NSC 800 microprocessor chip.

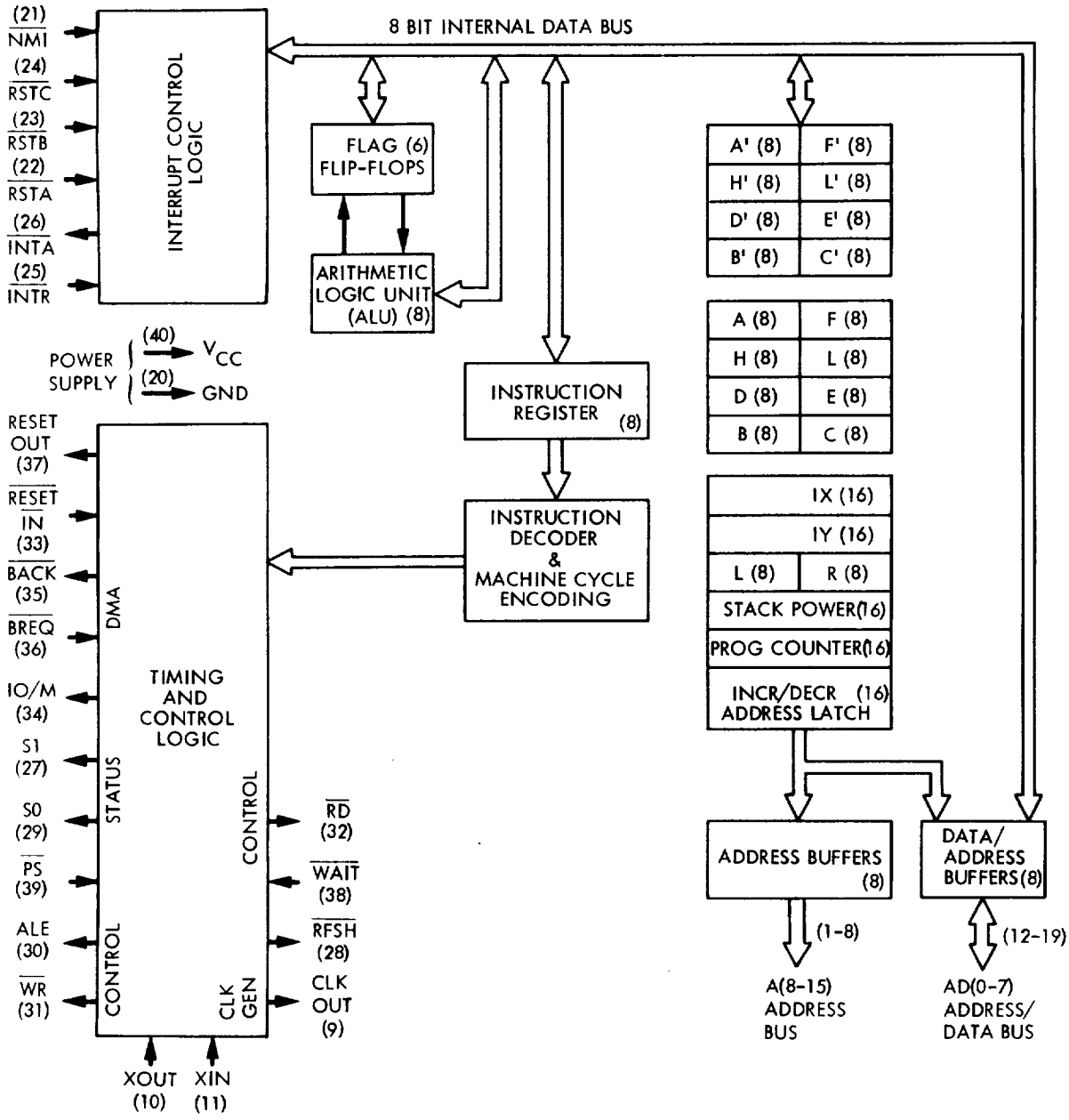


Figure 3-3. NSC 800 8-bit microprocessor functional block diagram.

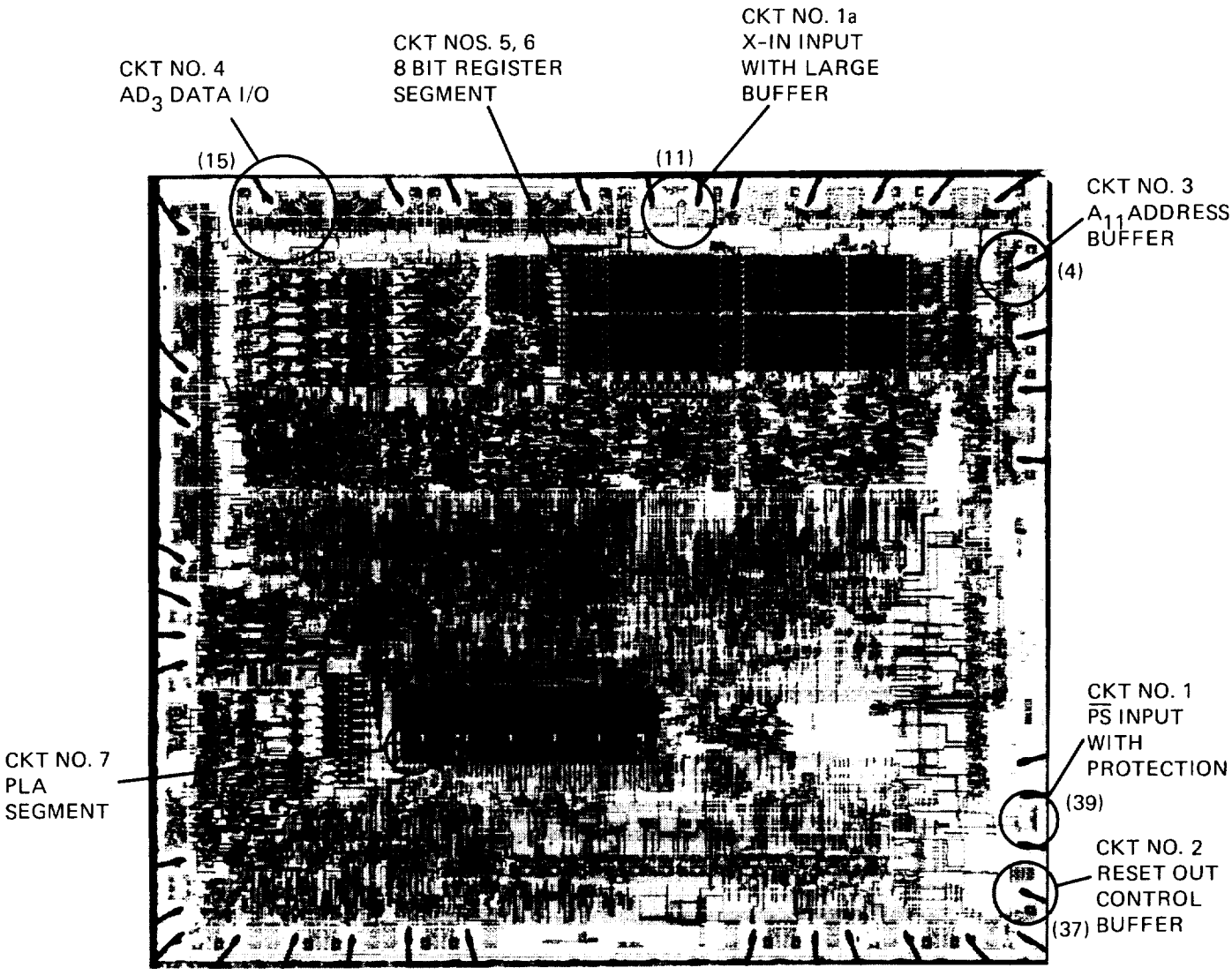


Figure 3-4. NSC 800 chip with selected and identified locations of seven circuits for subsequent electrical design and pattern validation presented in Figures 3-5 thru 3-13d.

Figures 3-5a thru 3-5e display type No. 1 circuit pattern (for 10 input circuits on the chip) comprised of an input protection resistor, two diodes (D_1, D_2) and an inverting buffer used in the following chip input functions:

Pad		Function	Pad		Function
11	—	X-IN	25	—	$\overline{\text{INTR}}$
21	—	$\overline{\text{NMI}}$	33	—	$\overline{\text{RESET IN}}$
22	—	$\overline{\text{RSTA}}$	36	—	$\overline{\text{WAIT}}$
23	—	$\overline{\text{RSTB}}$	38	—	PS
24	—	$\overline{\text{RSTC}}$	39	—	BREQ

Note: 11 — X-IN input function differs from other ten inputs, in that it has a large inverting buffer pattern identified in Figures 3-6a thru 3-6c and in reference Figure 3-4.

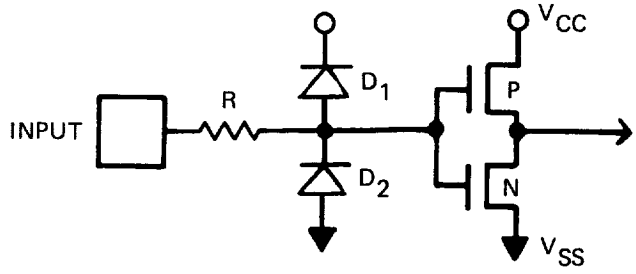


Figure 3-5a. Typical input protection circuit with a buffer (1 of 11).

Figure 3-5b. Logic equivalent.

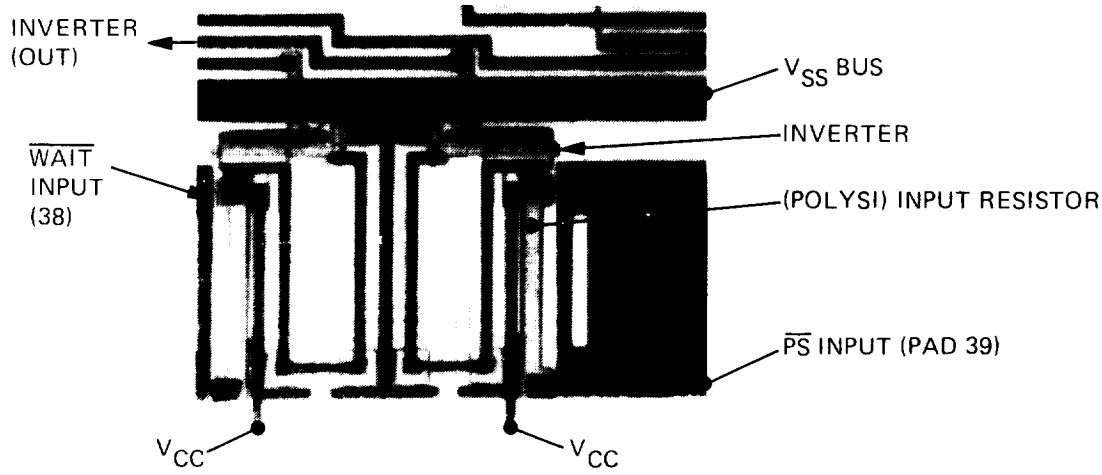


Figure 3-5c. Metallization interface of two input protection circuits [WAIT (38) and PS (39)] with inverting buffers. (Two of 10 similar input patterns).

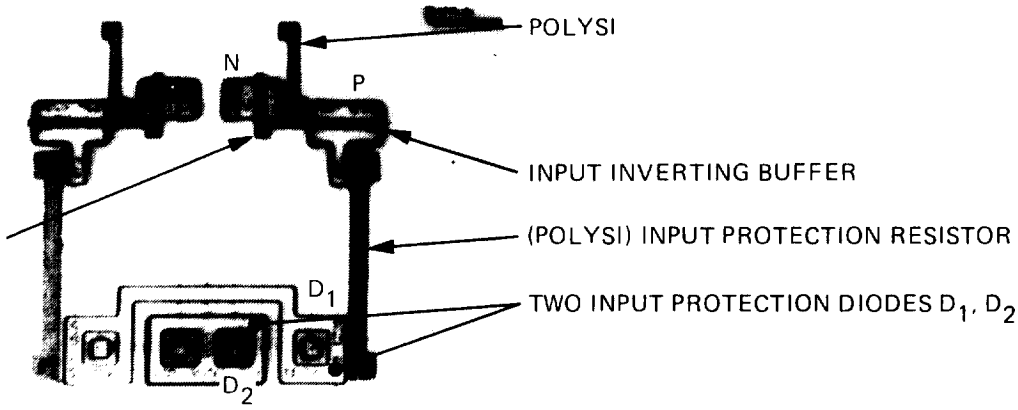


Figure 3-5d. Exposed (polysi) resistors and gates with diffusion patterns of two input protection circuits [WAIT (38) and PS (39)].

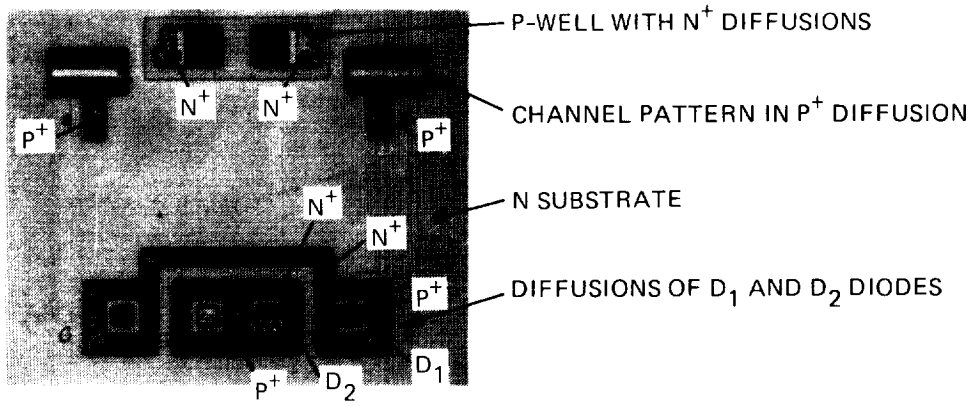


Figure 3-5e. Exposed P-well with N^+ and P^+ diffusions in silicon substrate of two input protection circuits [WAIT (38) and PS (39)]. (Two of ten similar input patterns).

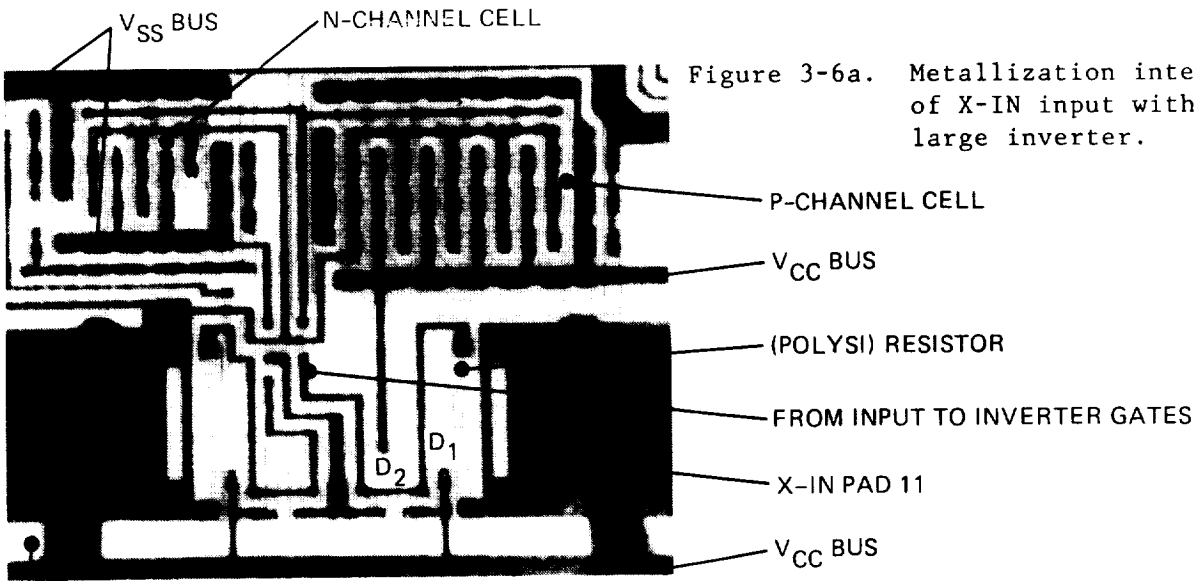


Figure 3-6a. Metallization interface of X-IN input with a large inverter.

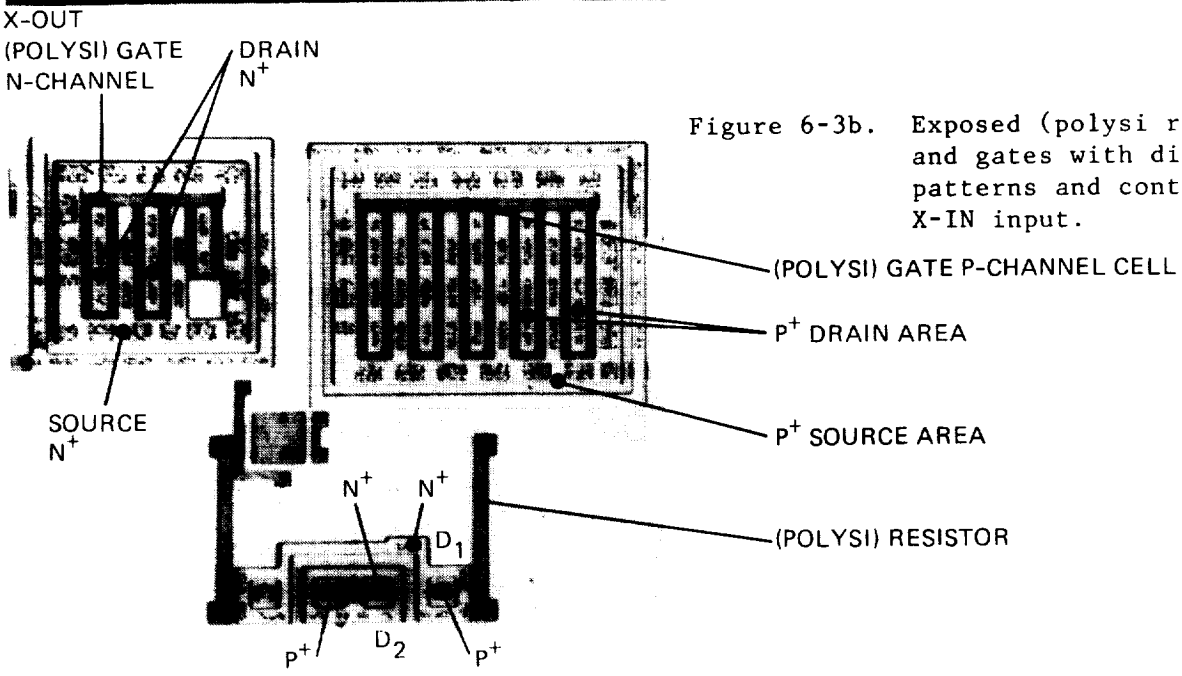


Figure 6-3b. Exposed (polysi resistor and gates with diffusion patterns and contacts of X-IN input.

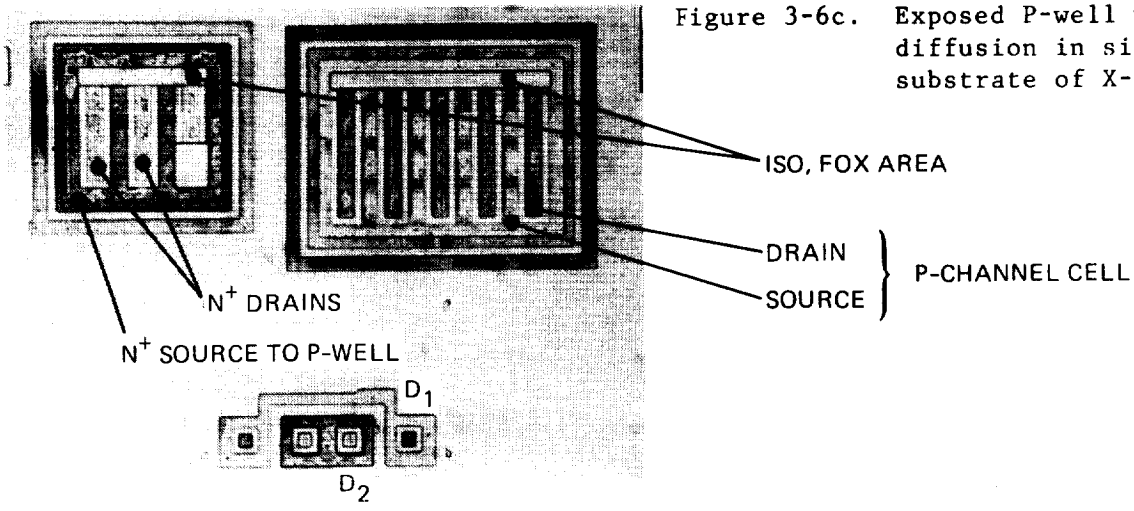


Figure 3-6c. Exposed P-well with N^+ diffusion in silicon substrate of X-IN input.

Figures 3-7a thru 3-7d display type No. 2 circuit patterns (for 10 control circuit buffers on the chip). The RESET OUT control buffer is of pull-up/pull-down configuration using N-MOS and NPN bipolar transistor in the output. This circuit pattern is used by the chip in the following control functions with the identified pads:

Pad		Function	Pad		Function
26	—	$\overline{\text{INTA}}$	31	—	$\overline{\text{WR}}$
27	—	S1	32	—	$\overline{\text{RD}}$
28	—	$\overline{\text{RFSH}}$	34	—	IO/$\overline{\text{M}}$
29	—	SO	35	—	$\overline{\text{BACK}}$
30	—	ALE	37	—	RESET OUT

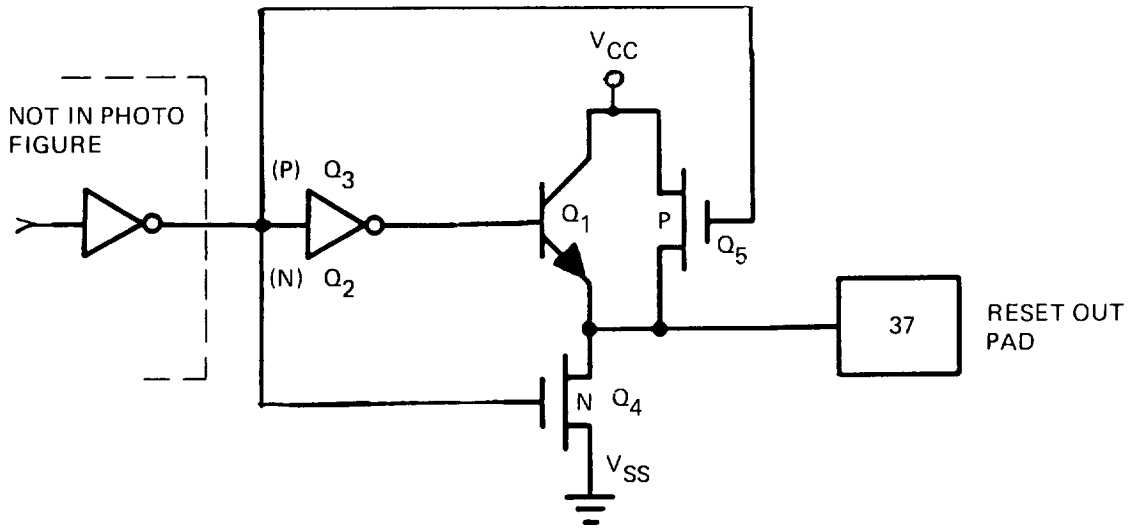


Figure 3-7a. Circuit schematic of RESET OUT control function with pull-up bi-polar output and N-MOS transistor.

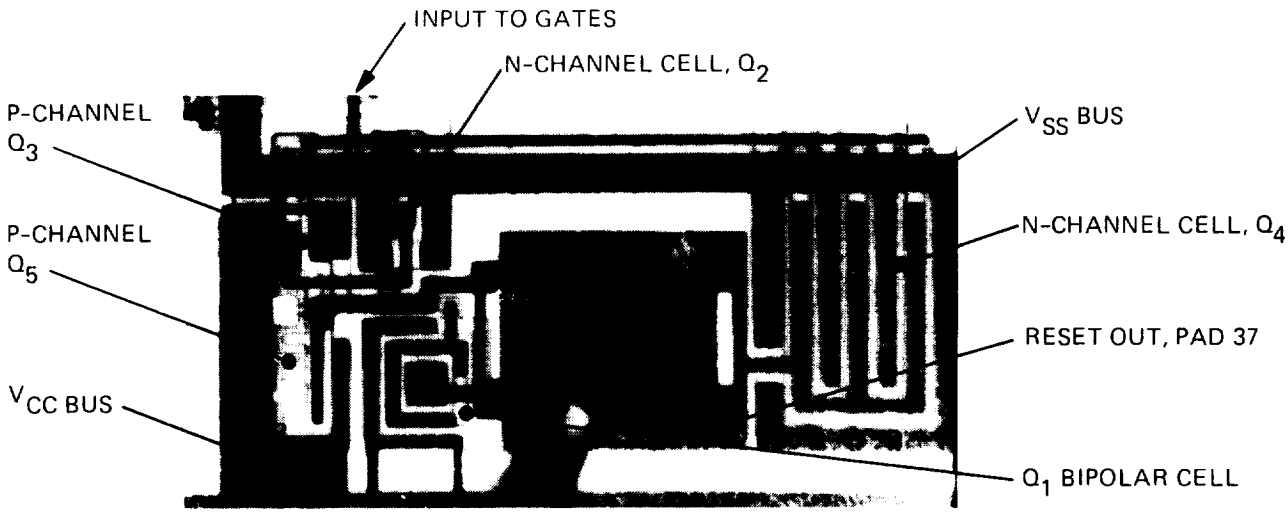


Figure 3-7b. Metallization interface over RESET OUT control circuit (1 of 10 similar circuit patterns of other control circuits).

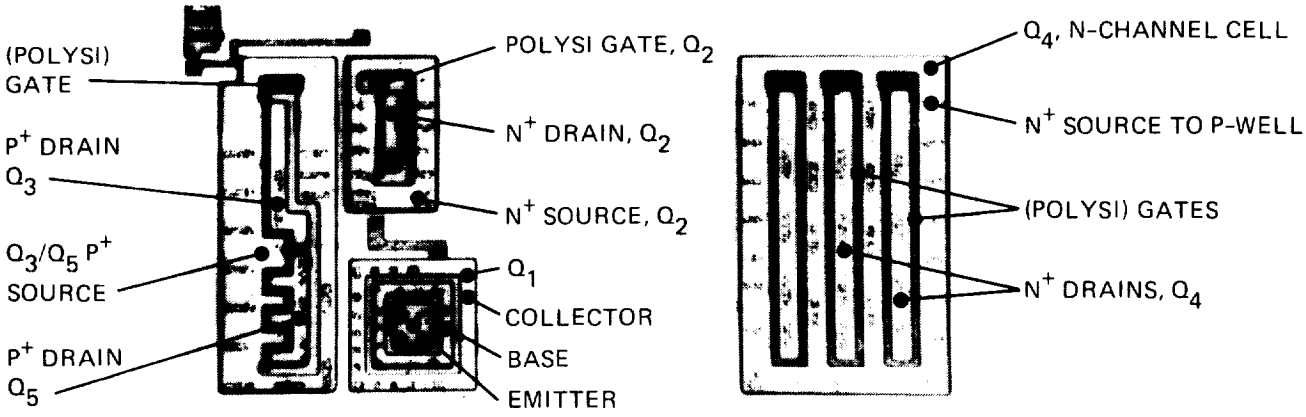


Figure 3-7c. Exposed (polysi) gates and cell diffusion patterns of RESET OUT control circuit (1 of 10 circuit patterns of other control circuits).

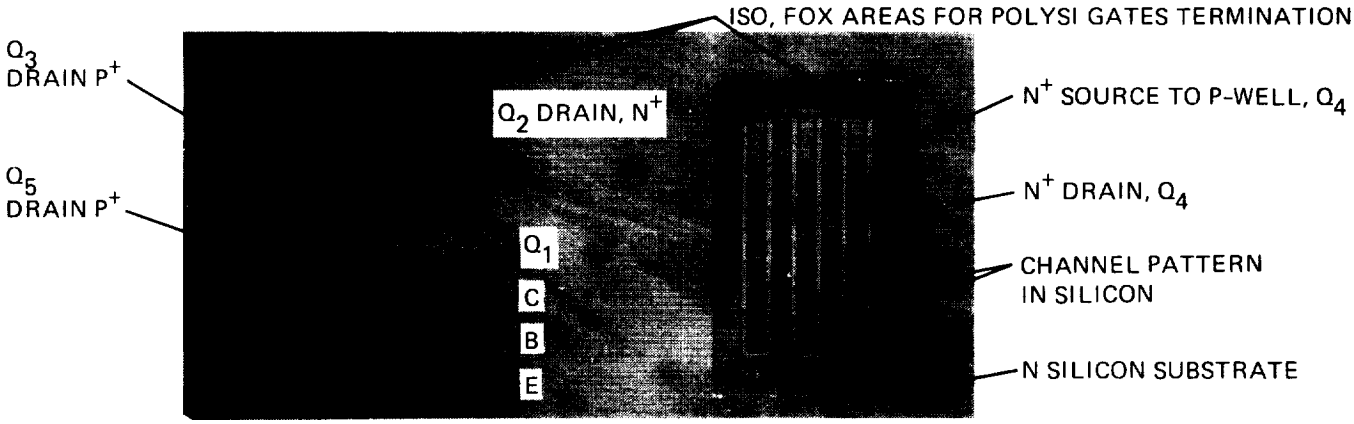


Figure 3-7d. Exposed P-well with N^+ and P^+ diffusions and NPN bipolar cell of RESET OUT control circuit (1 of 10 circuit patterns of other control circuits).

Figures 3-8a thru 3-8d, together with captions and circuit diagram, display type No. 3 circuit pattern (A_{11} address buffer) for eight data address buffers A_8-A_{15}, chip pads 1 through 8.

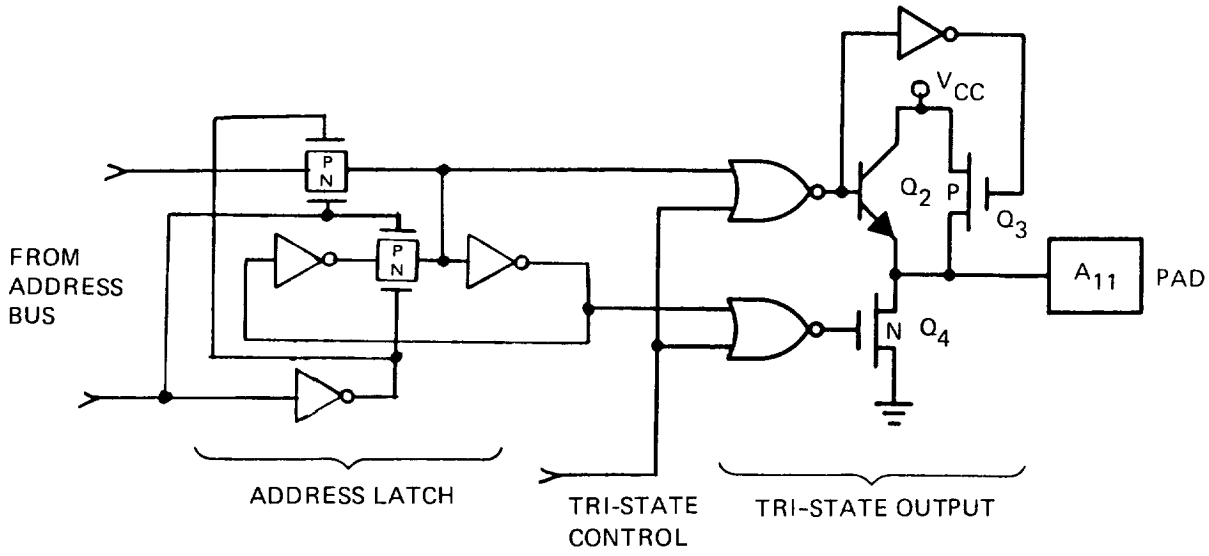


Figure 3-8a. Circuit schematic of address buffer A_{11}. (1 of 8).

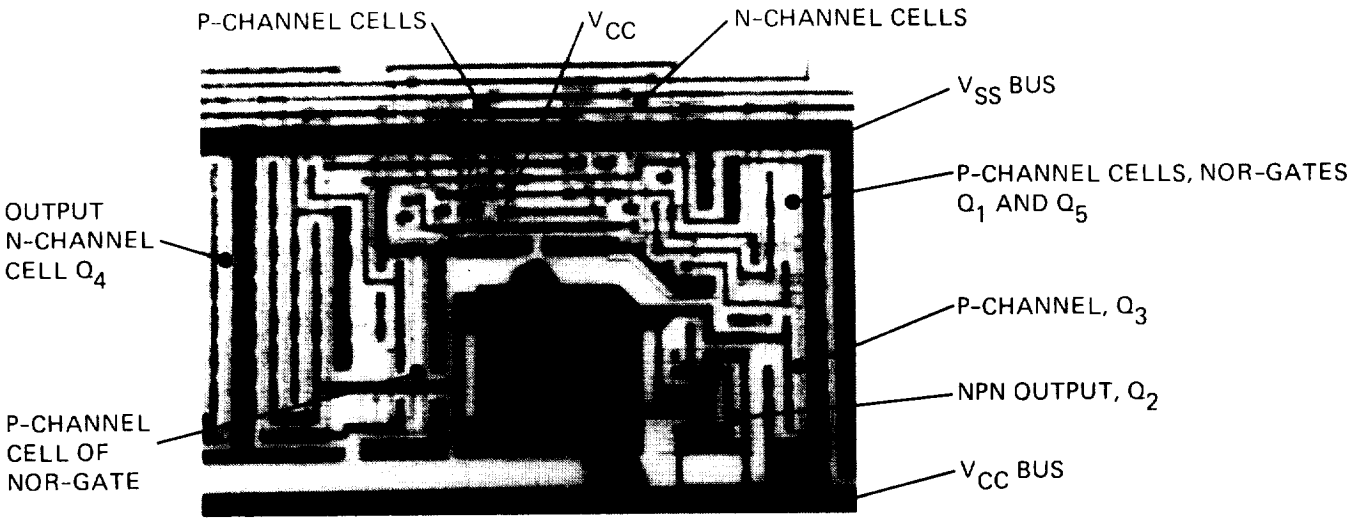


Figure 3-8b. Metallization interface of A_{11} address latch and buffer circuit (1 of 8 circuit patterns).

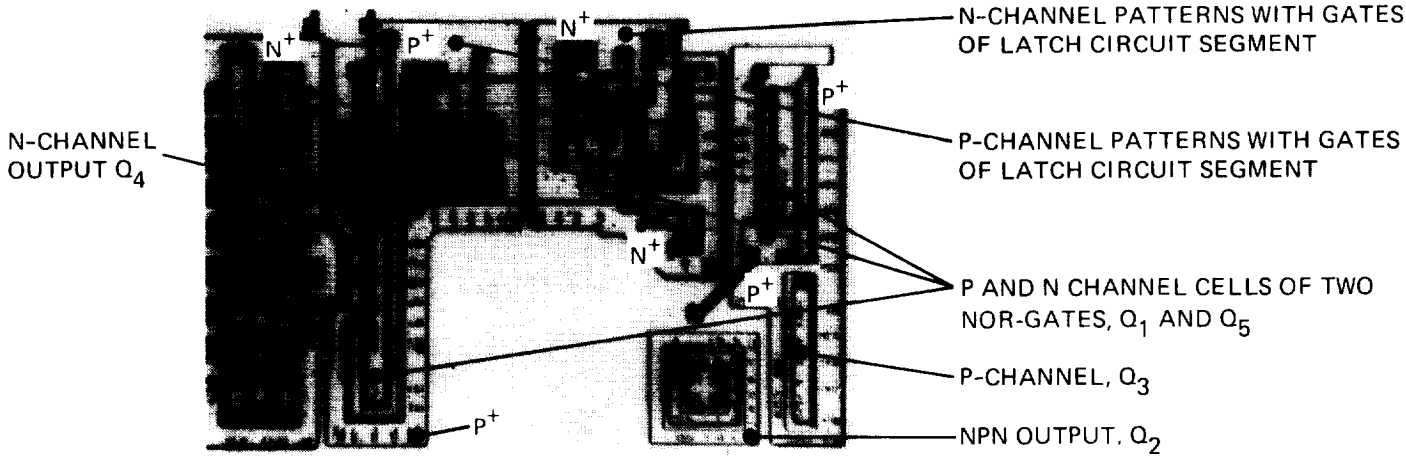


Figure 3-8c. Exposed polysi gates and cell diffusion patterns of A_{11} address latch and buffer circuit.

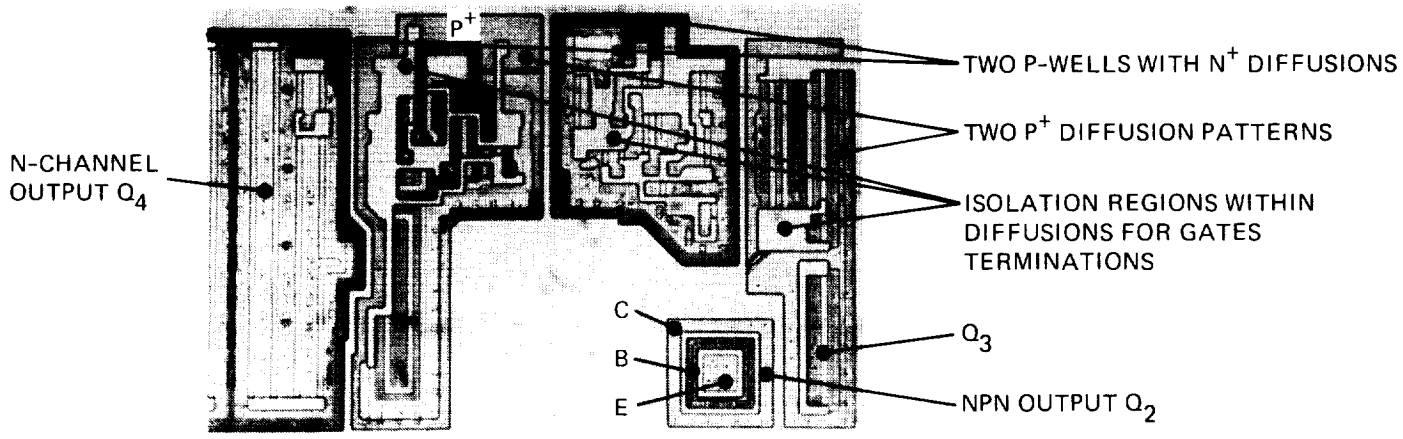


Figure 3-8d. Exposed two P-wells with N^+ diffusions and two P^+ diffusions patterns of A_{11} address buffer (1 of 8 circuit patterns).

Figures 3-9a thru 3-9d, together with captions and circuit diagram, display group No. 4 circuit pattern of AD_3 Data I/O buffer (a pattern for 8 data I/O buffers AD_0-AD_7, chips pads 12 thru 19).

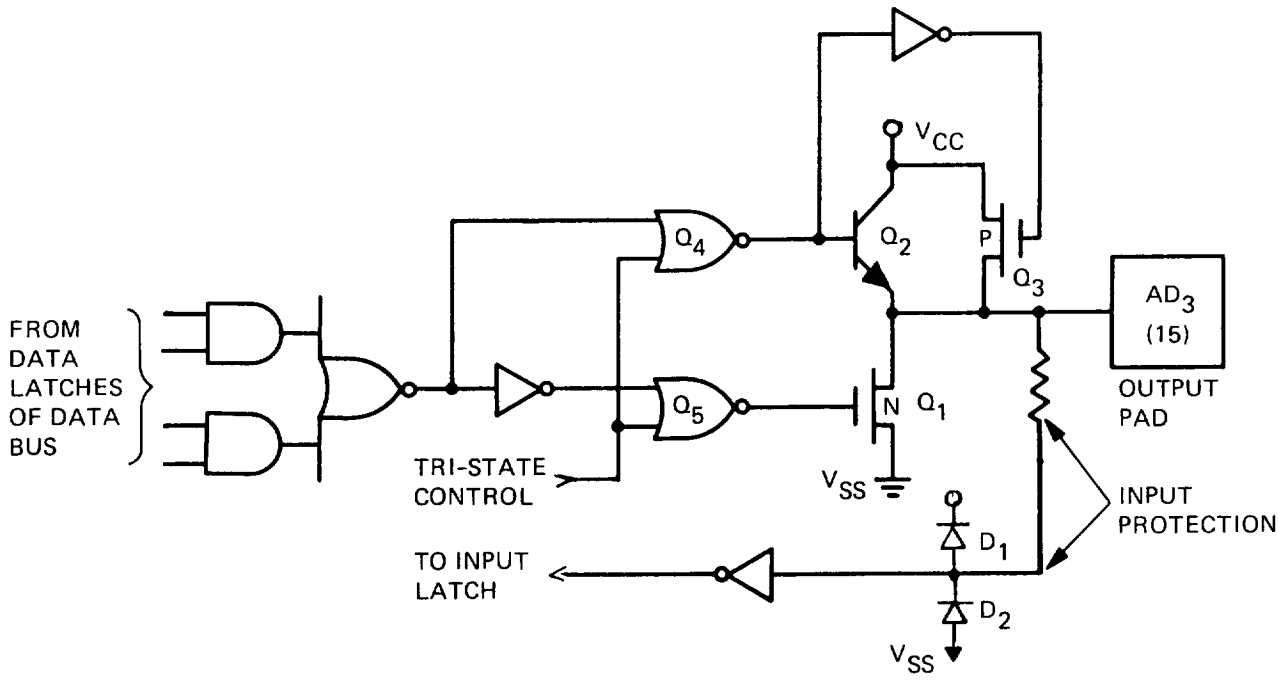


Figure 3-9d. Logic/circuit schematic of tri-state Data I/O buffer output (1 of 8 patterns).

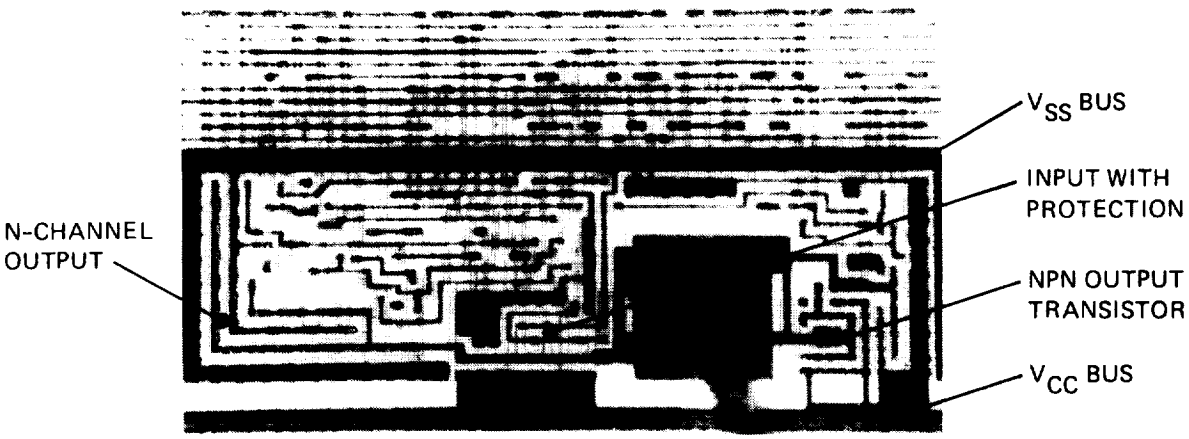


Figure 3-9b. Metallization interface of AD_3 Data I/O buffer (1 of 8 circuit patterns).

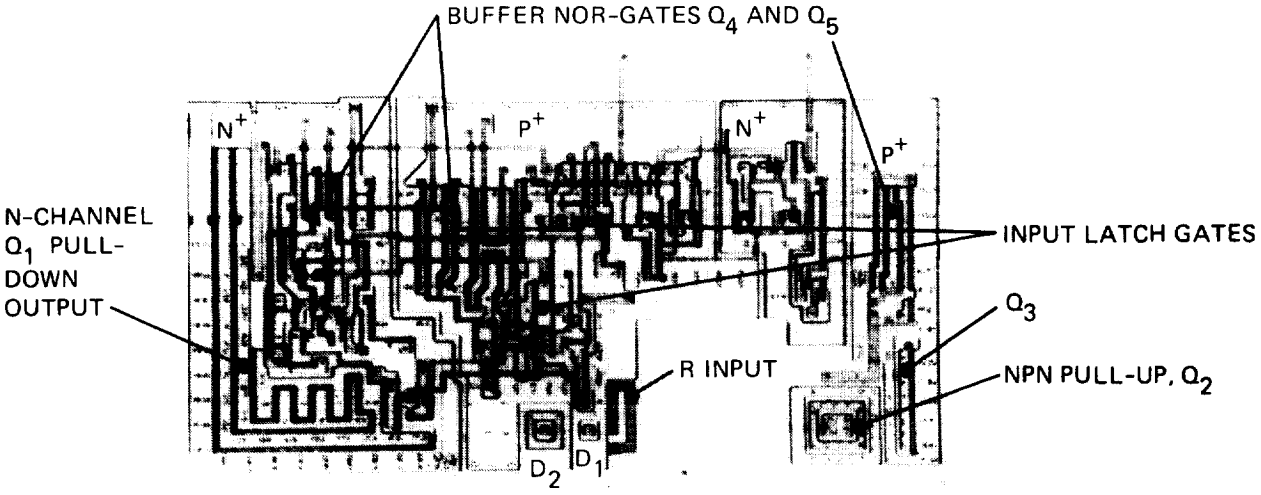


Figure 3-9c. Exposed polysi gates and diffusion patterns of AD_3 Data I/O buffer (1 of 8 circuit patterns).

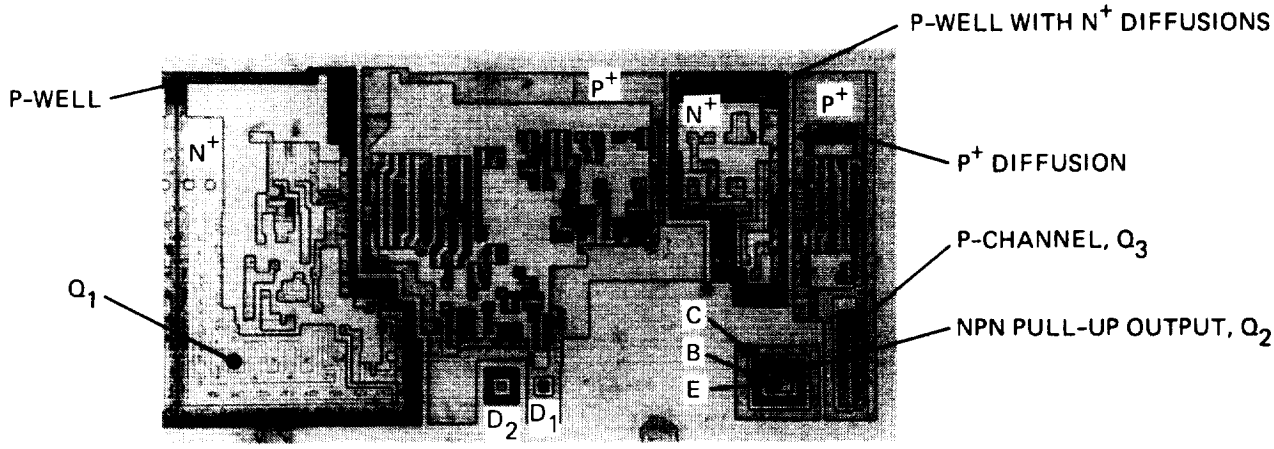


Figure 3-9d. Exposed P^+ and N^+ diffusion patterns in silicon substrate of AD_3 Data I/O Buffer (1 of 8 circuit patterns).

Figures 3-10a thru 3-10e, and circuit diagrams, display a six-transistor register latch pattern and a segment of 4 bistable latches of an 8-bit register. This is a typical 6-T CMOS latch used in Random Access Memories (RAMs) and registers. The register's data, $\overline{data}$ lines are the Polysi 2 interface to pass-transistor outputs N_1 and N_3.

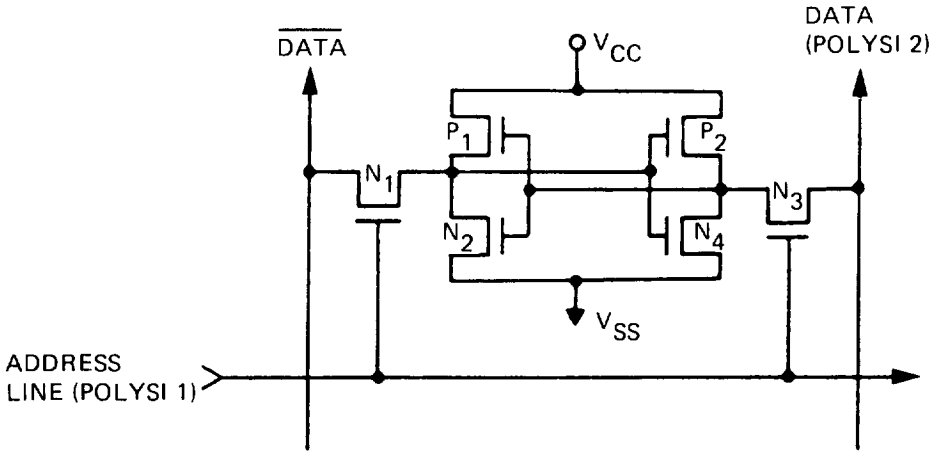


Figure 3-10a. Circuit schematic of 6-T bistable register latch.

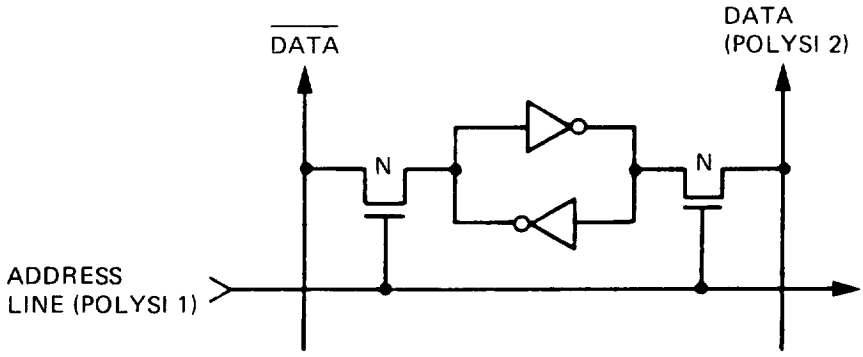


Figure 3-10b. Logic equivalent.

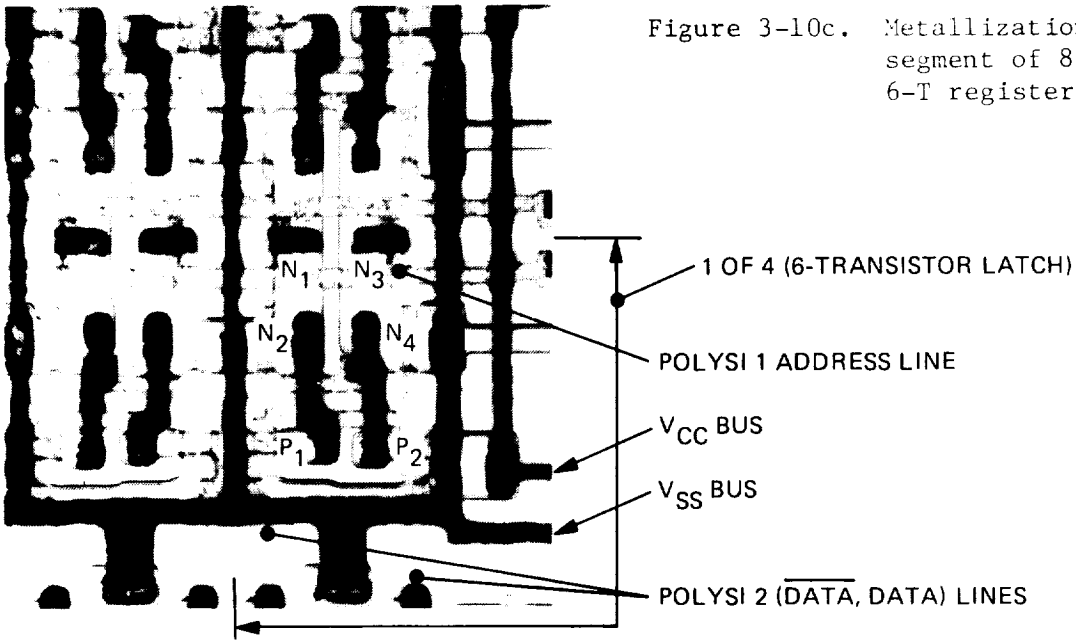


Figure 3-10c. Metallization interface segment of 8-bit, four 6-T register batches.

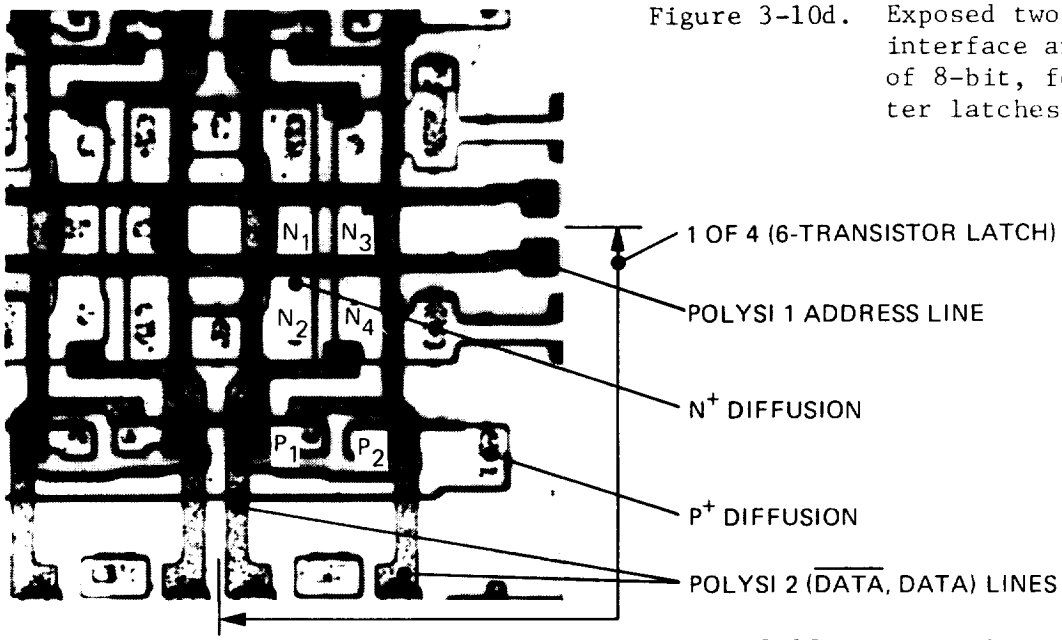


Figure 3-10d. Exposed two level polysi interface and diffusions of 8-bit, four 6-T register latches.

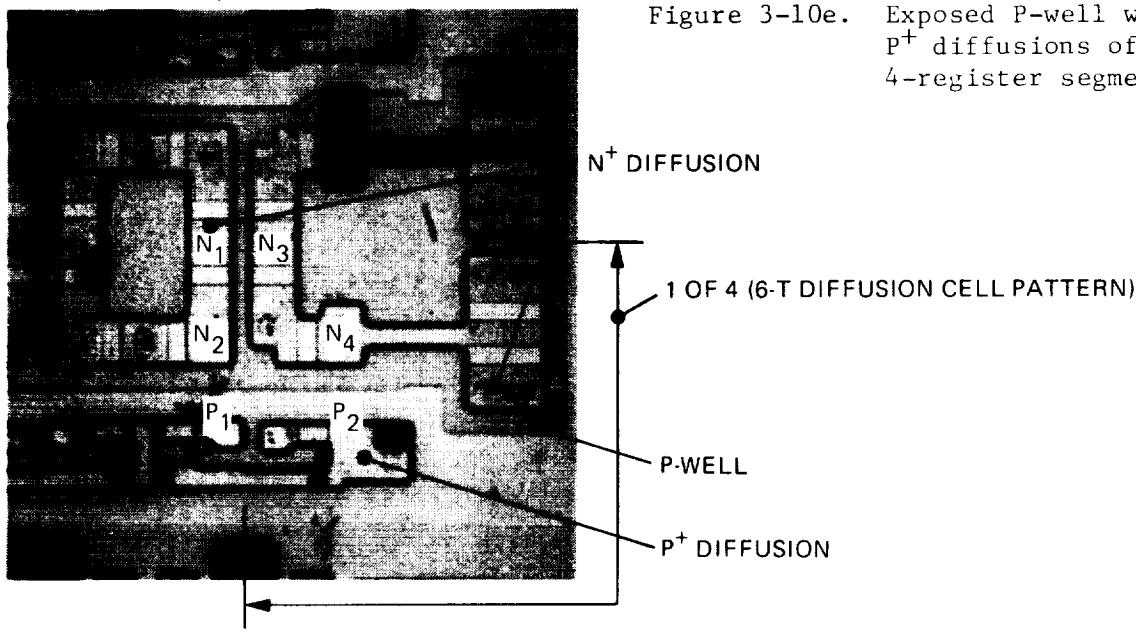


Figure 3-10e. Exposed P-well with N^+ and P^+ diffusions of an 8-bit 4-register segment.

Figures 3-11a and 3-11b display a register latch segment with read/write control gates with a data bus, and a segment of an 8-bit register.

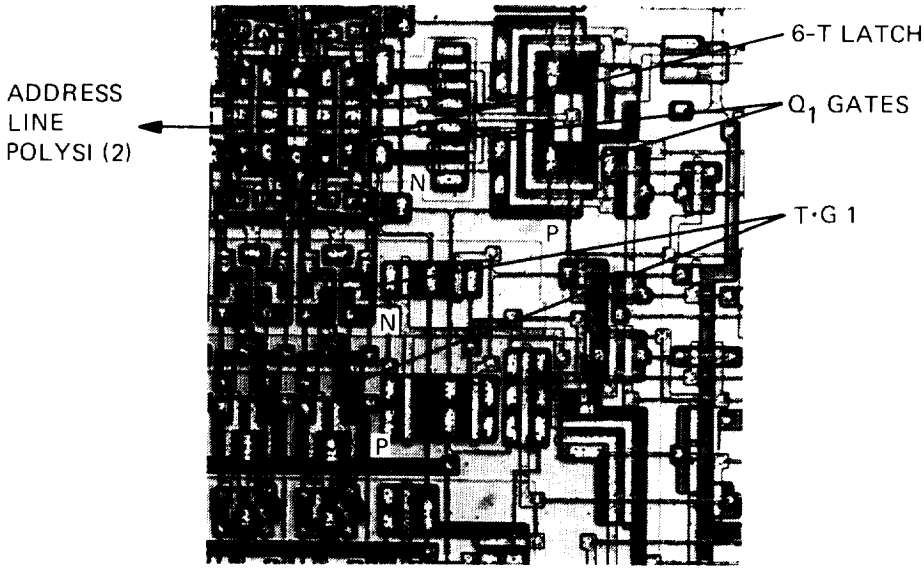


Figure 3-11a. Register latch 2-bit segment of 8-bit register with control gates.

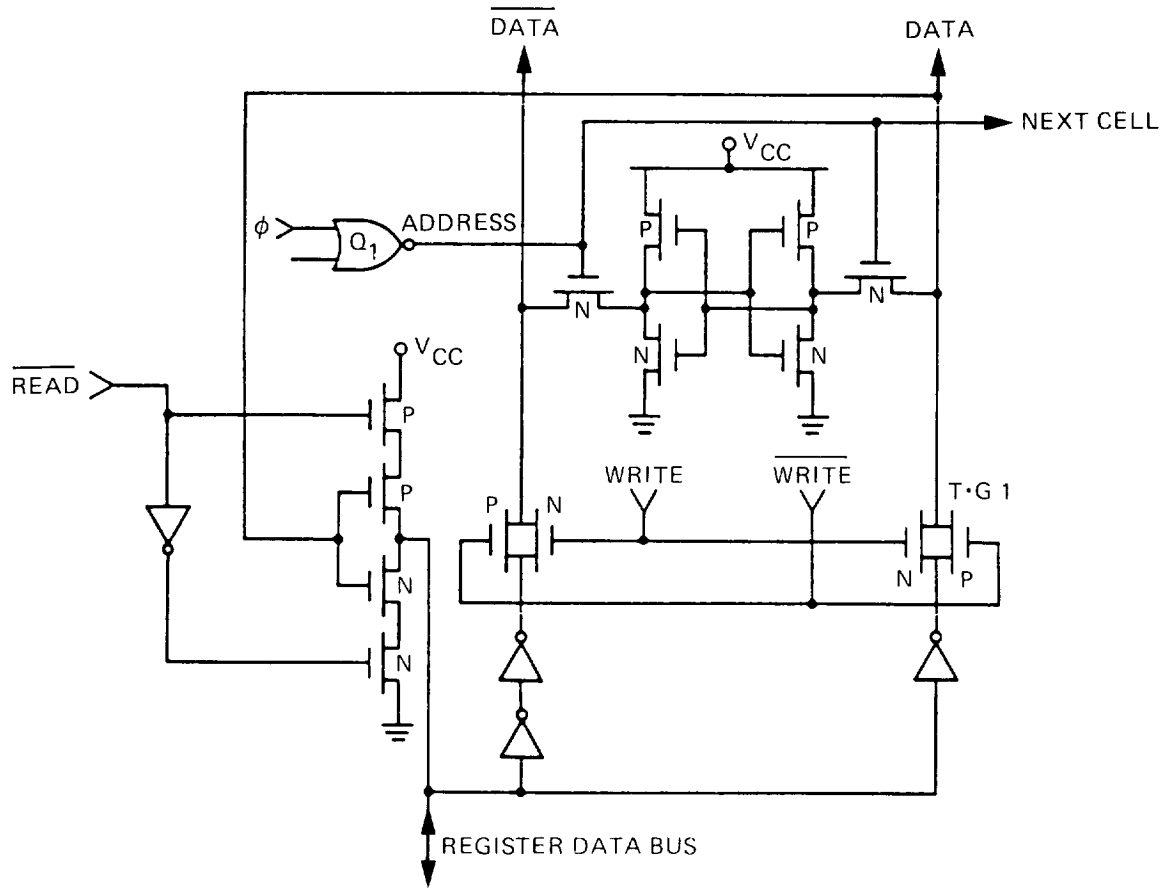


Figure 3-11b. Circuit schematic of a register latch with I/O logic.

Figures 3-12a thru 3-12d, and a circuit diagram, present a circuit of PLA with branch product buffers. This is a very small segment of PLA showing density of cells and gates pattern of reference area in Figure 3-4.

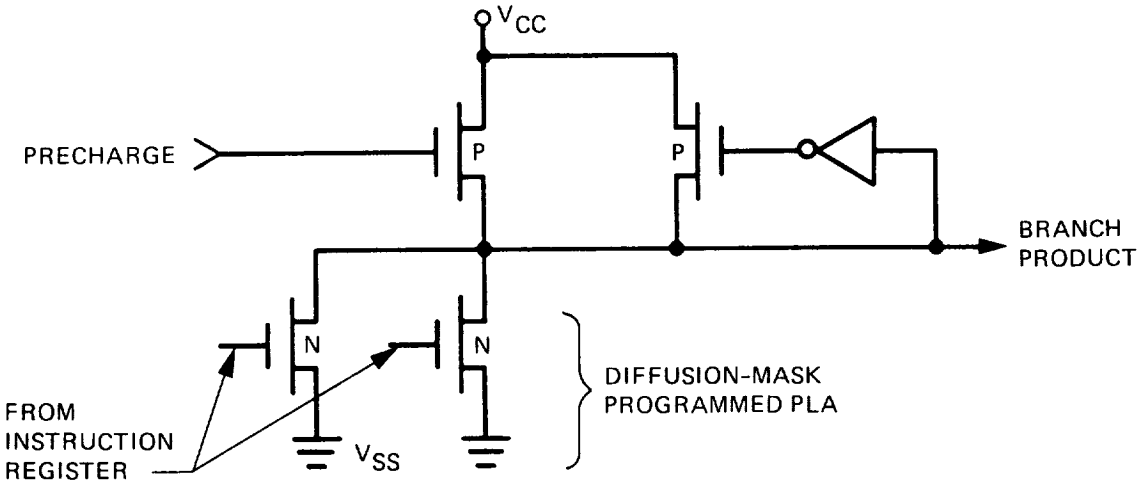


Figure 3-12a. Circuit schematic segment of PLA.

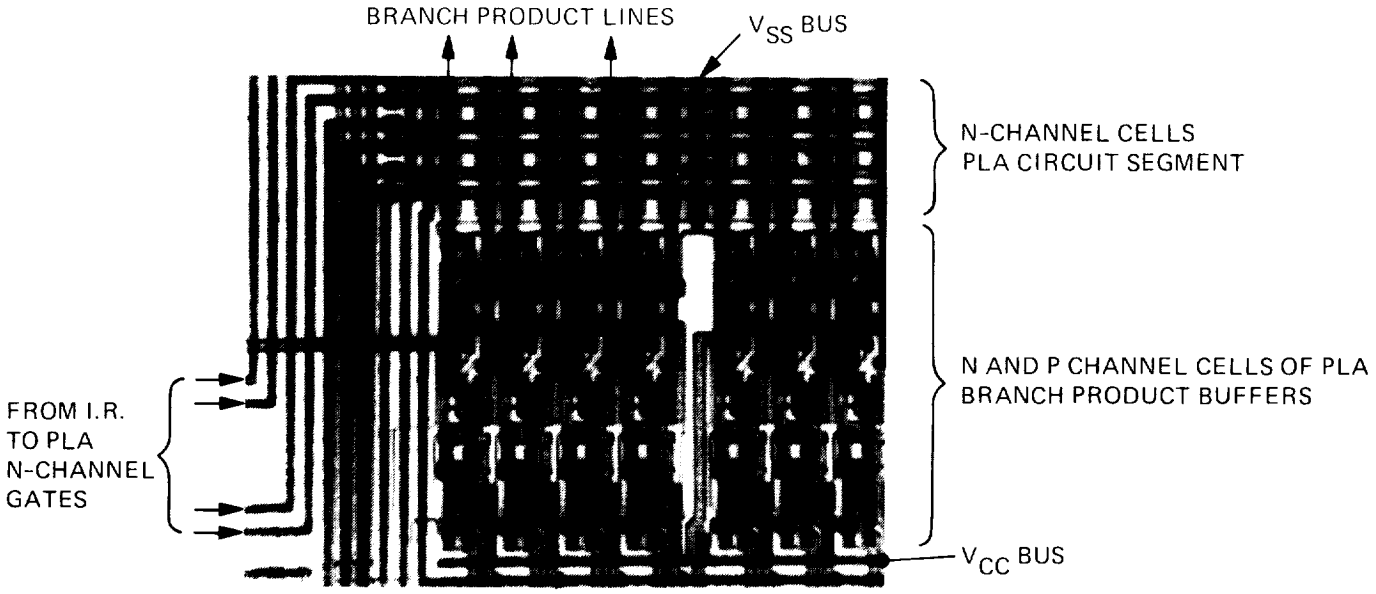


Figure 3-12b. Metallization interface of PLA circuit segment.

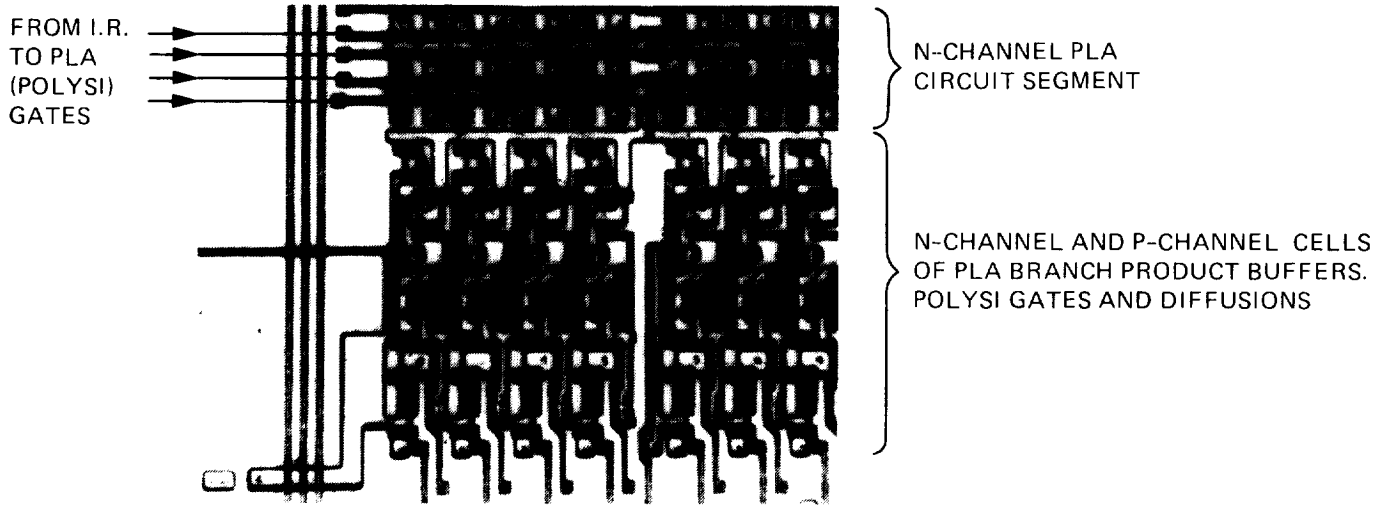


Figure 3-12c. Exposed (polysi) gates and diffusion pattern of PLA circuit segment.

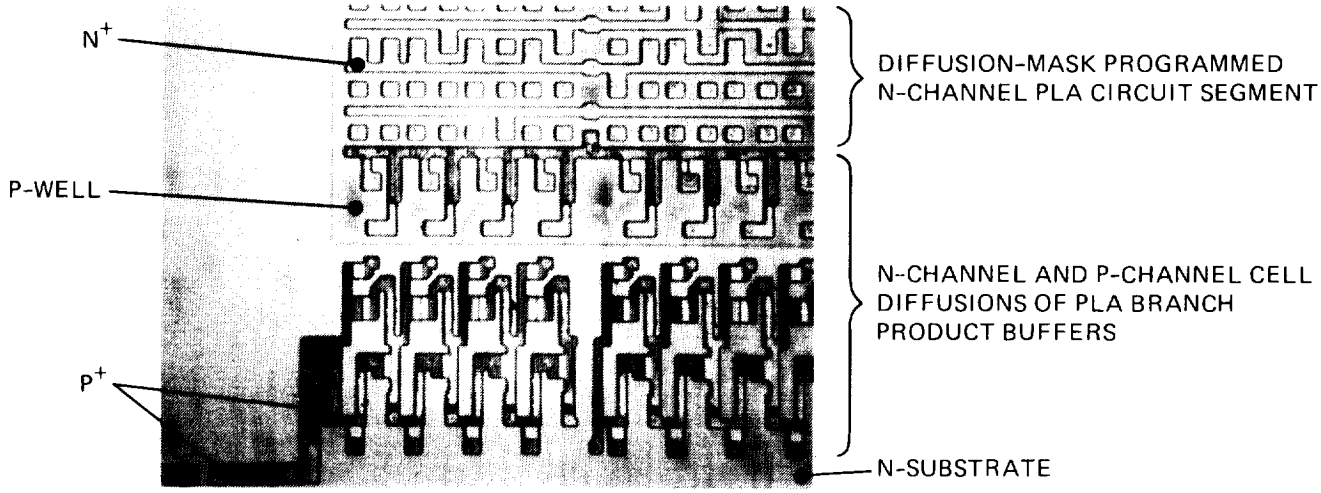


Figure 3-12d. Exposed pattern of N-channel diffusion programmed PLA circuit segment.

3.4 SUMMARY AND CONCLUSIONS

Three different date-coded NSC 800 devices were examined to ascertain if any comparative changes exist on each chip and its size related to the package date code. In each instance, each date-coded package contained a chip with a different code letter. Further examination of each chip has revealed changes in design and in chip size and material.

The three package date-codes related to the chip mask-codes are as follows:

a. Device date-code 1980 has chip code NSC 800 $\overline{F}$.

b. Device date-code 1982 has chip code NSC 800 $\overline{G}$.

c. Device date-code 1983 has chip code NSC 801 $\overline{A}$.

The segments of chip code masks are shown in photo-Figures 3-13a thru 3-13c.

The two chips, NSC 800 $\overline{F}$ and NSC 800 $\overline{G}$, are of the same area but differ in design pattern and use SiO_2 protective passivation. The NSC 801A uses a thick nitride protective passivation.

The NSC 801A chip is 10 percent smaller in size; the polysi and diffusion level geometry appears to be correspondingly scaled-down compared to the $\overline{F}$ and $\overline{G}$ chips.

The maturity of the NSC 800 8-bit microprocessor is fairly recent, about 2-1/2 years. In that time the manufacturer has instituted changes in chip design, size and materials process, most likely to improve the function of the chip.

Note: Of three date-coded lots inspected, only two devices with NSC 800 $\overline{G}$ type chips were evaluated in depth on all materials levels. This information is the purpose of this report.

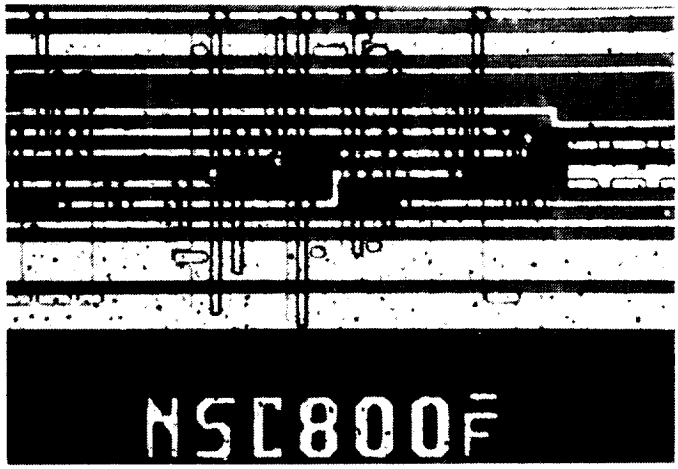


Figure 3-13a. A magnified segment of a chip with ID No. NSC 800-$\overline{F}$ of a 1980 date-coded device.

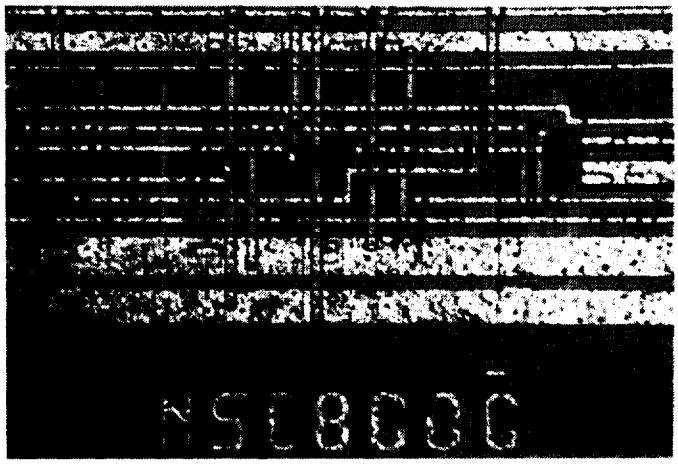


Figure 3-13b. A magnified segment of a chip with ID No. NSC 800-$\overline{G}$ of a 1982 date-coded device.

Figure 3-13c. A magnified segment of chip with ID No. NSC 801-$\overline{A}$ of a 1983 date-coded device.

SECTION 4

NSC 800 — DIE MATERIALS EVALUATION

4.1 APPROACH

The materials analysis was performed in four steps, chemically removing each layer of surface material on the chip (wet chemical etch), and to reveal subsequent levels of materials with minimal structure degradation.

At each step, the exposed level of chip materials was examined optically and with a Scanning Electron Microscope (SEM). X-ray spectroscopy was also utilized for materials identification and contaminants. The visual evidence as presented in the optical and SEM photo figures (4-1 through 4-18c), together with detailed captions and comparisons provided thereby, offers insight into the exposed materials and design structures.

The four etching steps are correlated with figures in Table II.

Table II. Four-Step Wet Chemical Etch Materials Removal on the Chip.

Step	Description
1.	Top SiO_2 passivation removed; aluminum metallization exposed. (SEM Figures 4-3 through 4-9a.)
2.	Aluminum metallization removed; interlevel insulating SiO_2 exposed with contact apertures to polysi and silicon diffusions. (SEM Figure 4-11a.)
3.	Interlevel insulating SiO_2 removed; exposed Polysi 2- and Polysi 1-gates, field oxide (SiO_2) and thin oxide. (SEM Figures 4-13a through 4-16b.)
4.	Polysi 2, Polysi 1-gates, field oxide (SiO_2) and thin oxide (SiO_2) removed; exposed silicon substrate, P^+ and N^+ diffusions, P-well definition and isolation regions where grown field oxide was present. (SEM Figures 4-18a through 18-c.)

The emphasis at each level of materials exposure and through the SEM figures is to visually establish comparisons of these materials and in the replicating patterns after these materials have been removed, as well as in the definition of process anomalies and ultimately by a reliable assessment of chip materials patterns.

Note: However carefully the multiple etching steps are performed in the removal of chip materials, the effect of lateral etch cannot be avoided. It can, however, be controlled, minimized and fully explained.

4.2 SEM EXAMINATION PRIOR TO PASSIVATION REMOVAL

The entire chip protective SiO_2 passivation was examined. The surface morphology of SiO_2 is more granular over metal interconnect and roughly identifiable from other materials patterns. The two level polysi, Polysi 2 and Polysi 1 are barely defined beneath SiO_2 passivation.

SEM Figure 4-1 at 500X displays a segment of a register four bistable latches with typical passivation coverage.

SEM Figure 4-2 at 1000X magnification shows a pattern of one bistable latch circuit with detailed definition of passivation features covering the metal and two-level polysi. There were no signs of surface contaminants nor pinholes in the two chips examined.

4.3 STEP 1: SEM EXAMINATION AFTER TOP PASSIVATION REMOVAL

The protective SiO_2 passivation was removed from the chip surface, to expose intact metallization interconnect and leaving partially passivated the two-level polysi and field oxide.

The metallization was subsequently examined optically and in the SEM for metal step coverage over oxide and polysi steps. The contact interface of metal to the two-level polysi and silicon diffusion was also inspected. SEM Figures 4-3 and 4-4 show typical input protection, two diodes and a polysi resistor with exposed metal. SEM Figure 4-5 at 475X shows (AD) address buffer segment and exposed aluminum pad with an interconnect.

SEM Figure 4-6 with four bistable latches of register array (each latch a

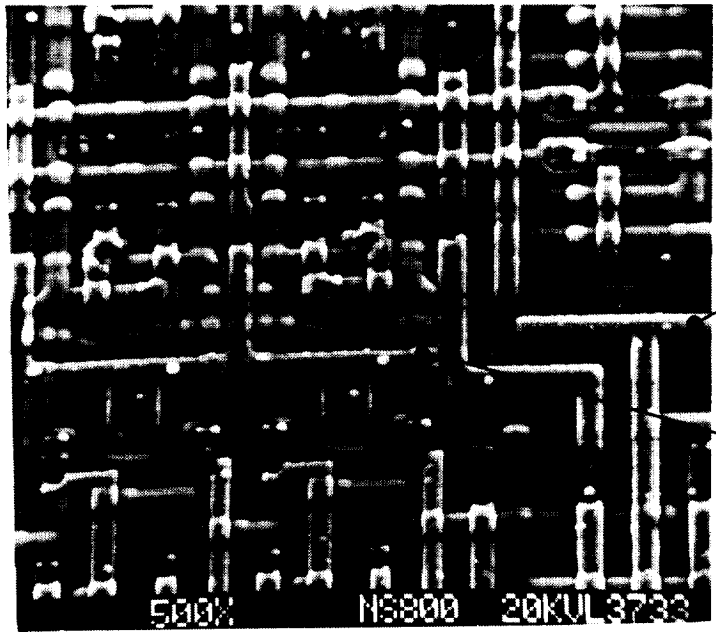


Figure 4-1. (With SiO_2 passivation.) 500X SEM view of chip segment RAM register circuit cells. Note: With the exception of metal interconnect, the gate polysi pattern cannot be identified with SiO_2 coverage.

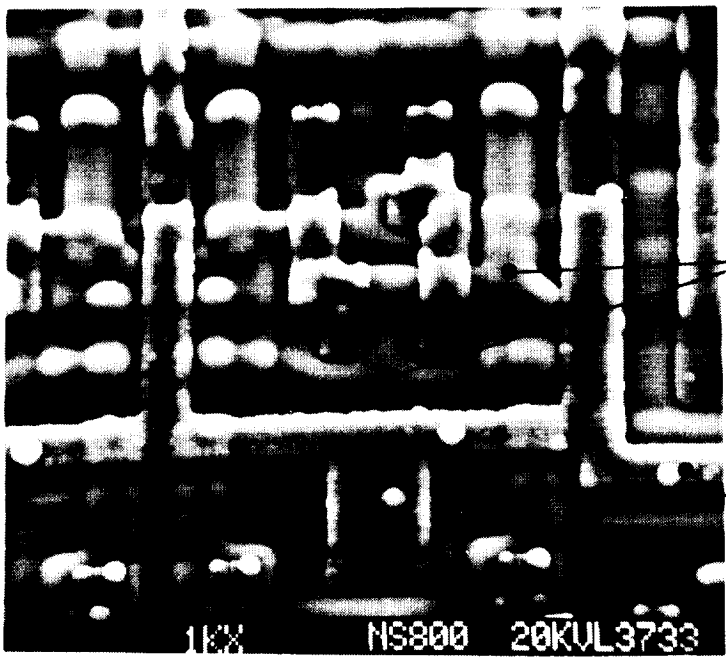


Figure 4-2. 1000X SEM view of magnified one RAM register cell with sharper definition of SiO_2 passivation morphology over metal as compared to areas over polysi and field oxide.

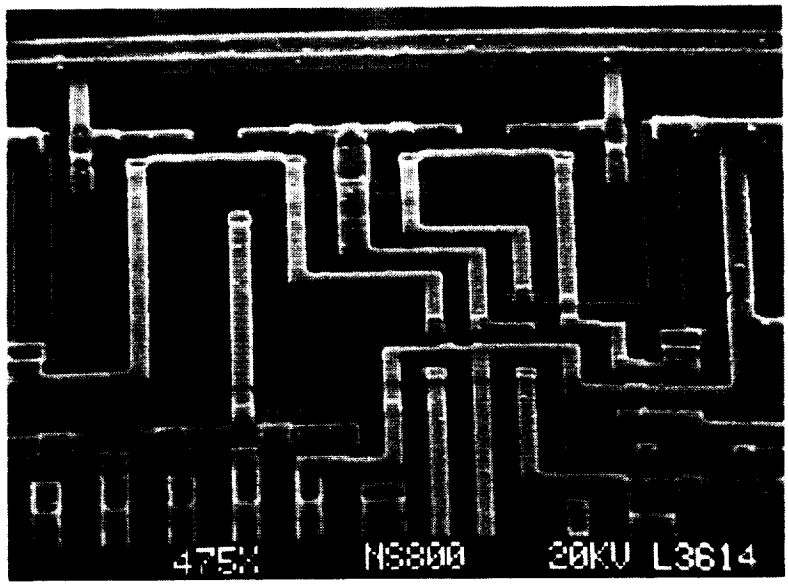


Figure 4-3. (Top passivation removed.) 475X SEM view of two separate input protection circuits, each comprised of two diodes and an input resistor and exposed metal interconnect.

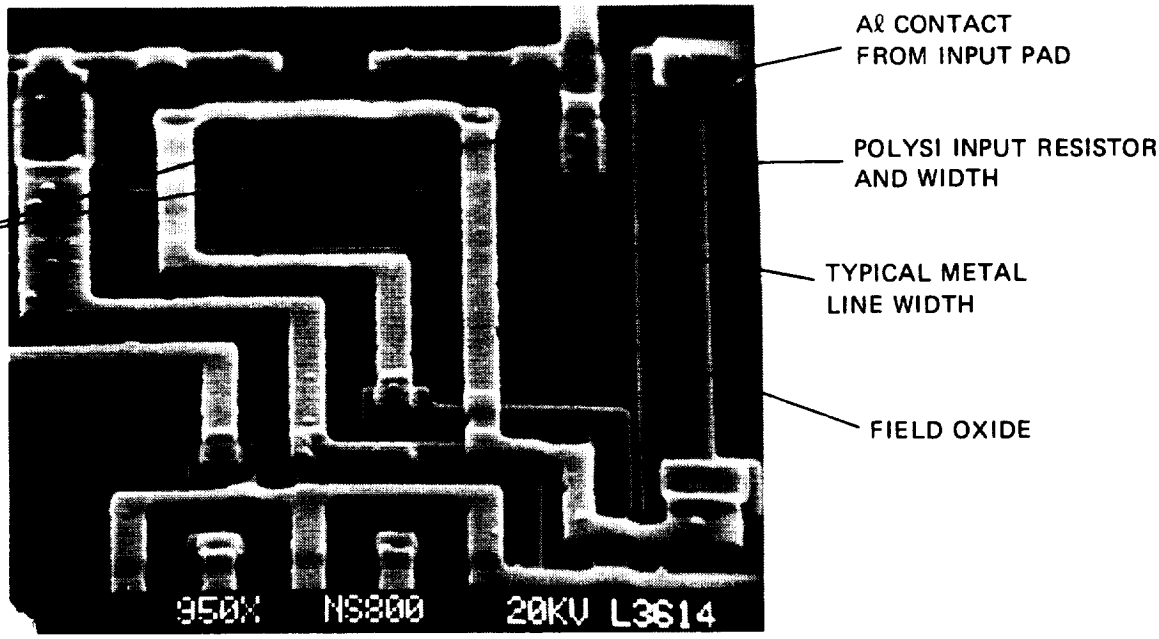


Figure 4-4. 950X SEM view of input protection diodes (two) and a polysi resistor (Ref. Figure 4-3 above). Note metal contact interface, typical metal line width and step coverage.

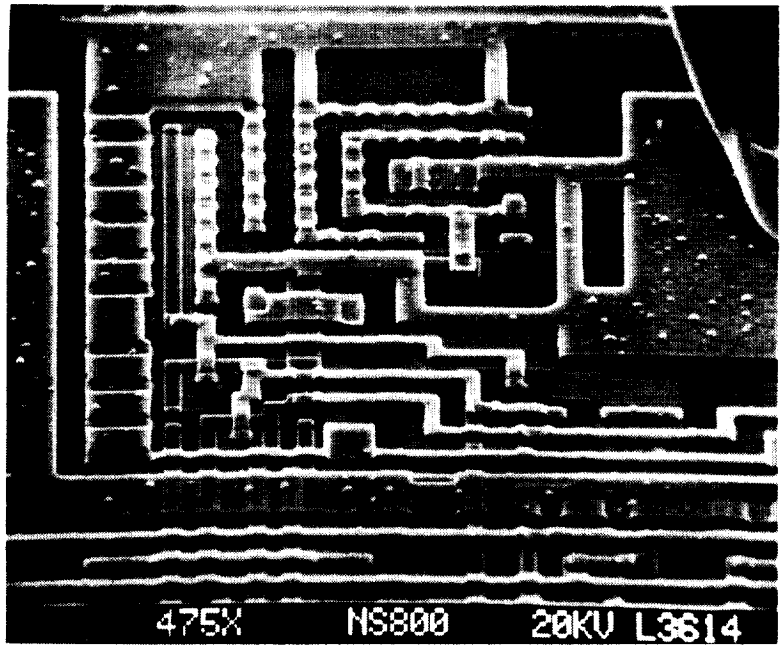


Figure 4-5. (Passivation removed.) 475X SEM view of chip segment with exposed aluminum interconnect.

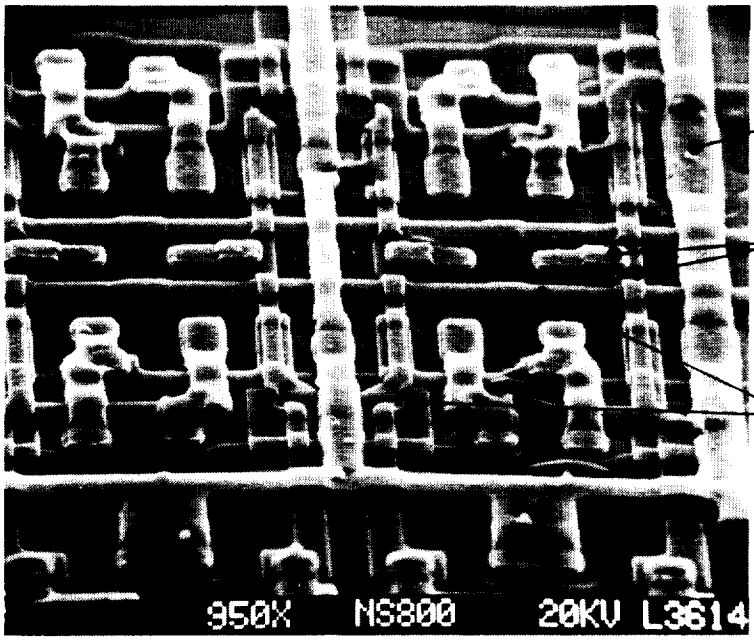


Figure 4-6. (Passivation removed.) 950X SEM view at 55^{o} tilt of four 6-transistor RAM cells in a register array. Note metal interconnect, metal butting contacts to polysi and diffusions and the two-level polysi. (See Figures 4-1 and 4-2.)

6-transistor cell), together with subsequent SEM magnifications (Figures 4-7 through 4-9a with descriptive captions in various positions), show typical examples of metal line widths, step coverage, thickness and contact interface to Polysi 2 and Polysi 1-gate, and help to identify the field oxide isolation regions and thin oxide in P^+ and N^+ diffusions. The metal patterns in these segments represent the average quality of metal interconnect in the two devices examined.

4.3.1 Summary And Conclusions

The metal step coverage shows uniform thickness over oxide and polysi steps, because of the grown oxide process depleting the silicon in isolation regions which makes the overall insulated surface of the chip reasonably level compared to deposited oxide which typically has higher steps around the active diffusions with thin oxide pattern. The data line butting the metal contact to polysi in Figure 4-9a (top-right) shows a partial void at the step to pass-transistor diffusion. Most metal contacts on the chip were of acceptable interface.

The patterns of register latch circuits appear to contain highest overlay of materials levels found on the chip.

4.4 STEP 2: SEM EXAMINATION AFTER REMOVAL OF ALUMINUM INTERCONNECT, EXPOSING INTERLEVEL OXIDE, CONTACT APERTURES TO POLYSI 2 AND POLYSI 1 (GATES) AND DIFFUSIONS

Magnified optical photo Figure 4-10 reveals the chip with exposed interlevel oxide, contact apertures to Polysi 2 and Polysi 1 and diffusions. Certain similarity of symmetry defines the blocks and similar circuit patterns on this level of materials exposed. A circled area in that figure is displayed in a magnified SEM Figure 4-11a. A similar latch circuit pattern, now with metal removed, is shown in Figure 4-9a. The narrow path of residual interlevel oxide identifies the paths where metal was present as well as the effect of wet chemical etching showing this pattern, with an undercut in interlevel oxide compared with an untouched surface of grown field oxide in silicon. The Polysi 2 data line, with an exposed butting contact aperture in Polysi 2 and silicon, is fairly well outlined in thin residue of interlevel oxide. Other contacts in the diffusions show perimeter outlines in thin oxide. Both data lines of Polysi 2 overlap the Polysi 1 gates P-channel and N-channel widths with Polysi 1 cross-terminations resting on field oxide. The P-channel Polysi 1, gate length beneath Polysi 2 appears to be

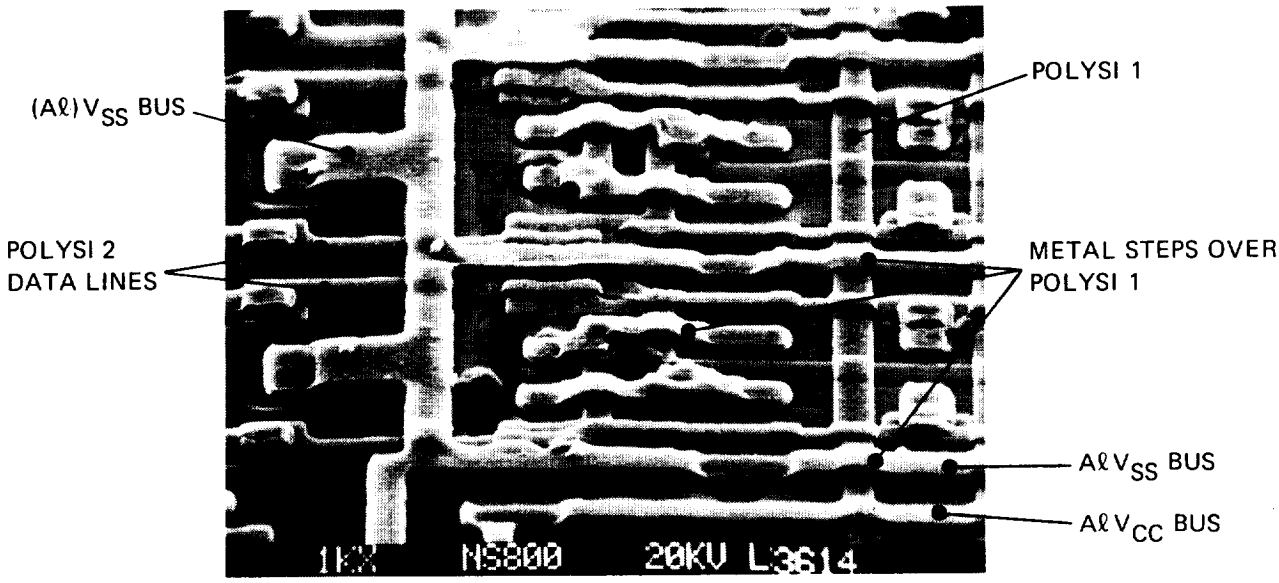


Figure 4-7. (Passivation removed.) 1000X SEM side view at 60° tilt and 90° turn cw (ref. Figure 4-6), showing exposed features of metal step coverage over polysi and oxide steps.

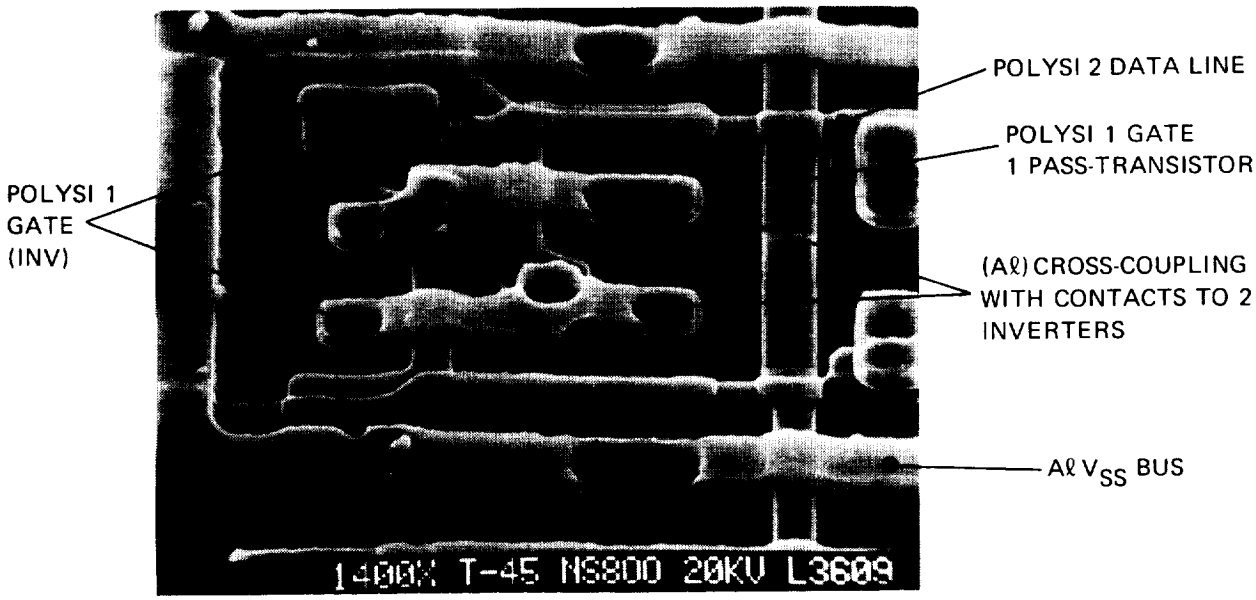


Figure 4-8. 1400X magnified SEM view of a 6-transistor cell pattern two level polysi, metal step coverage and contacts. (Ref. Figure 4-7 above).

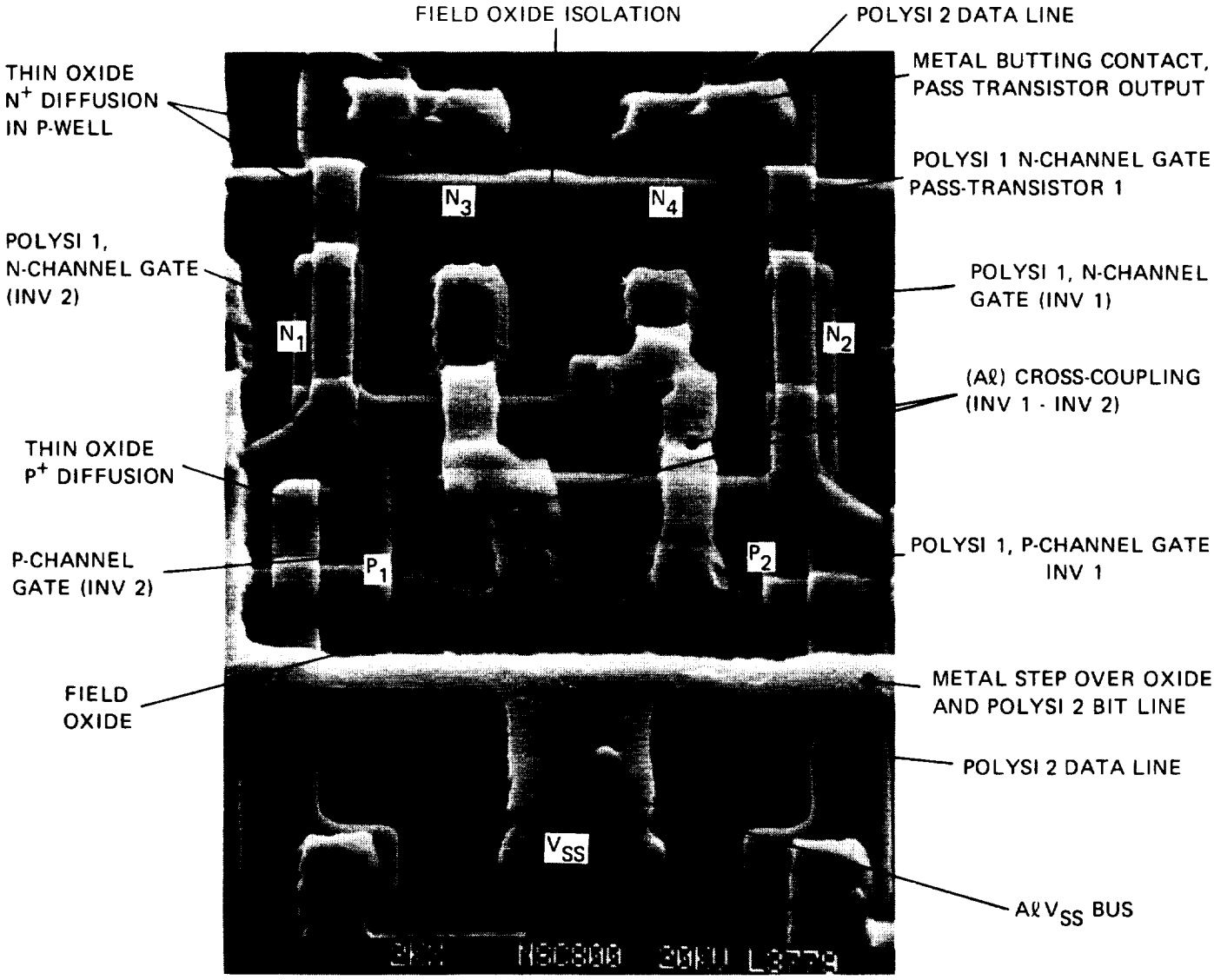


Figure 4-9a. (Passivation removed.) 200X SEM view of 6-transistor complementary CMOS RAM cell with definition of exposed metal step coverage, two-level polysi (Polysi 1 and Polysi 2), field oxide and thin oxide and P-channel and N-channel gate pattern. (Also see Figure 4-11).

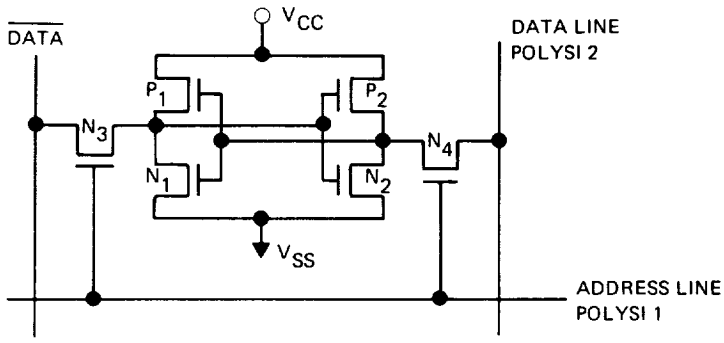


Figure 4-9b. Circuit diagram of CMOS 6-transistor RAM register cell, see physical pattern above.

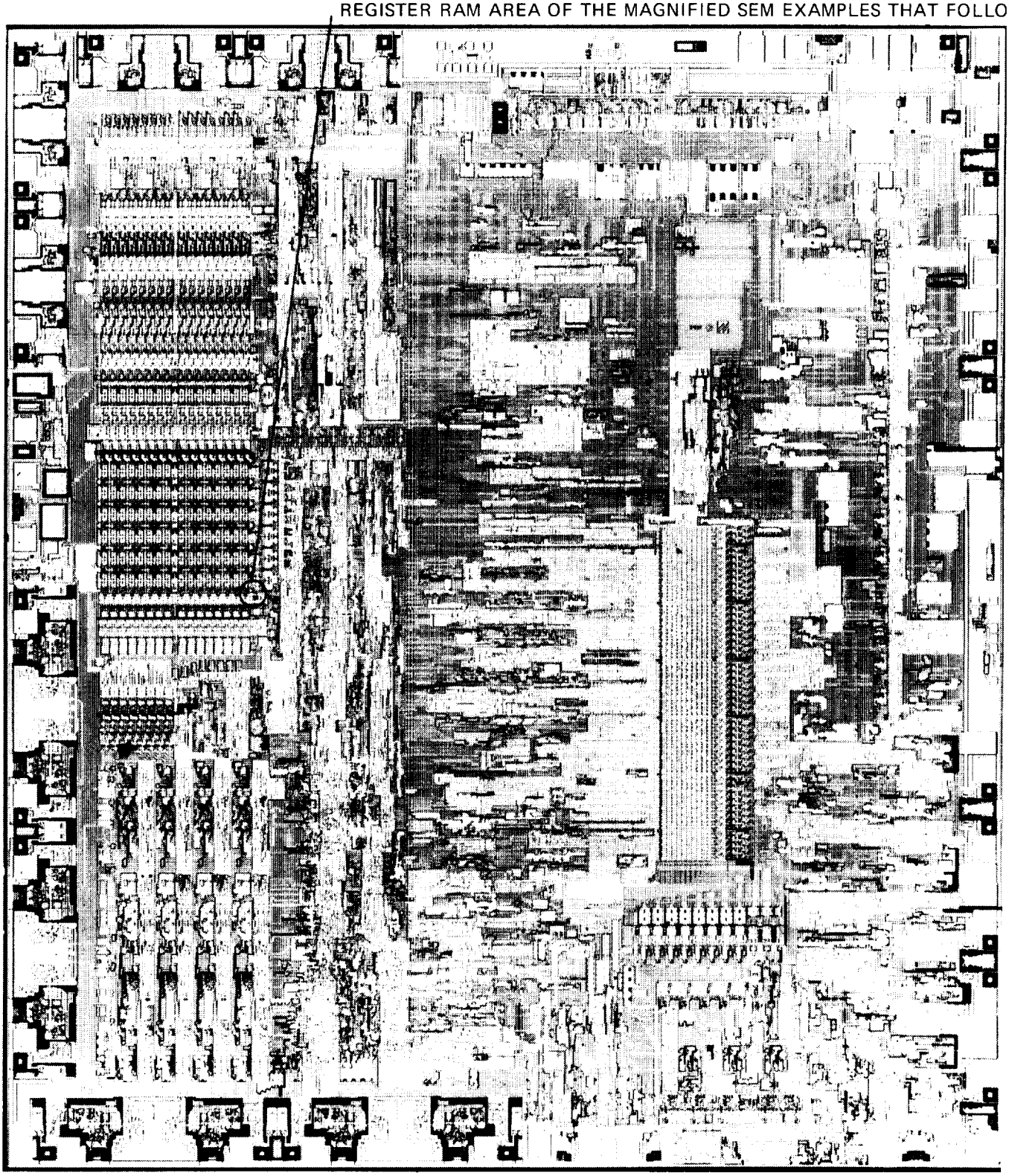


Figure 4-10. 29X magnified optical view of NSC 800 microchip after removal of top passivation and metallization. Exposed pattern of interlevel oxide, field oxide, contact apertures to polysi, (Polysi 1 and Polysi 2 pattern) and diffusion contacts in thin oxide are shown. (Ref. Figure 2-8).

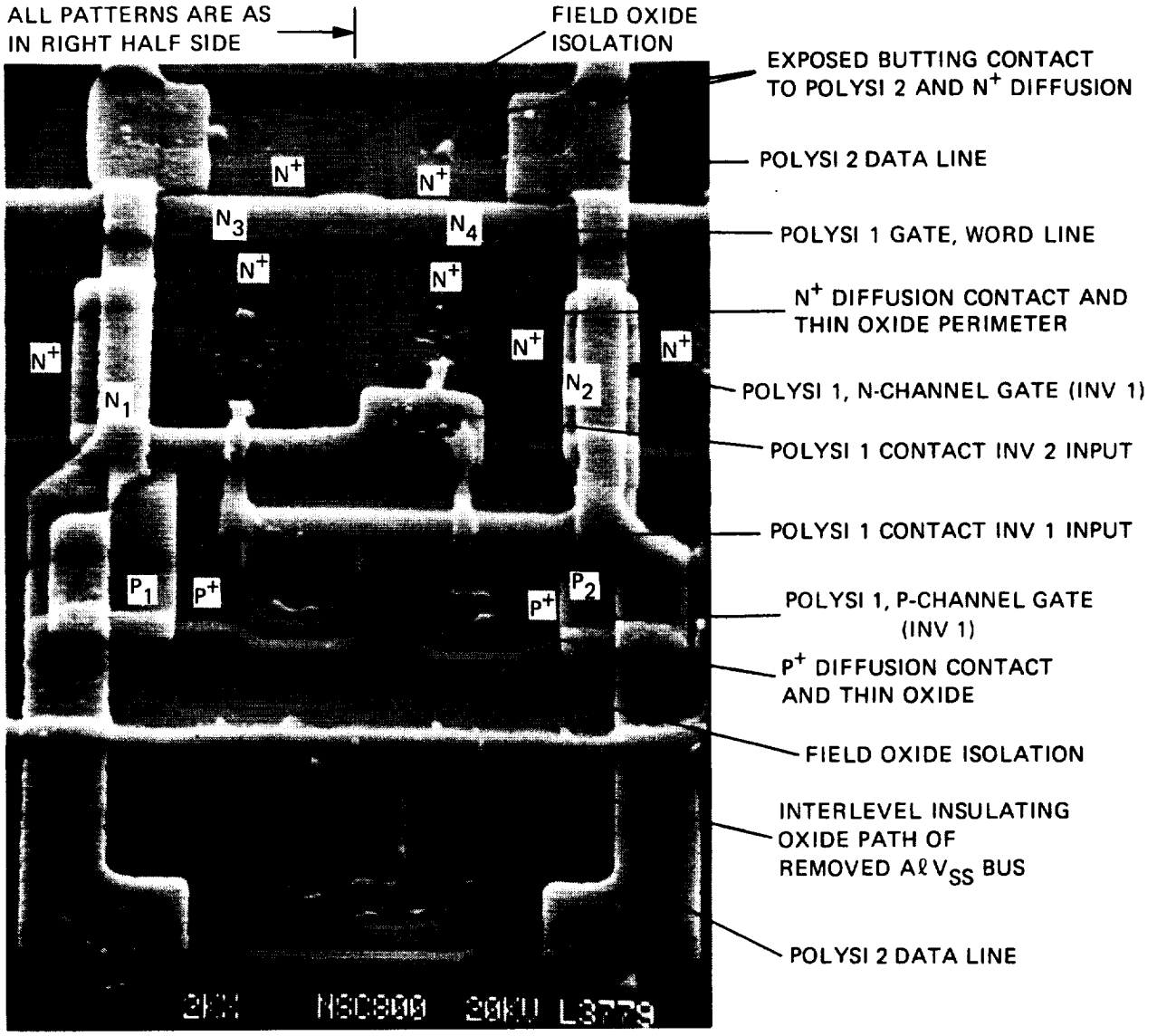


Figure 4-11a. (Metallization removed.) 2000X magnified SEM view of 6-transistor, complementary CMOS RAM cell. Exposed interlevel insulating oxide two-level polysi, contact apertures to Polysi 1 and Polysi 2, P^+ and N^+ diffusions with thin oxide and local isolation with field oxide are shown. (See Figure 4-9.)

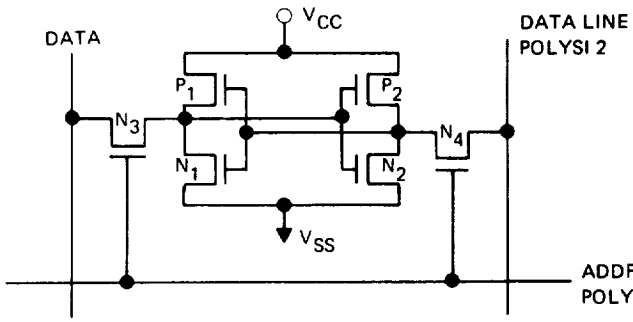


Figure 4-11b. Circuit diagram of CMOS 6-transistor RAM register cell, (See physical pattern above.)

almost twice as wide as the N-channel gate length. The perimeters of P^+ and N^+ diffusions with thin oxide are identified by borderlines of field oxide in isolation regions.

4.4.1 Summary and Conclusions

This level of materials exposure provides important insight into the features of the contacts interface in polysi and silicon diffusion and effect of preferential alloying due to sintering step of the metal interconnect. The residual paths of interlevel oxide of the polysi steps, typically, will show the thickness of separating insulation at metal crossover path.

The exposed definition of field oxide patterns surrounding the active regions of P^+ and N^+ diffusions with thin oxide can be examined.

The silicon contacts do not exhibit pitting effects of sintering.

4.5 STEP 3: SEM EXAMINATION AFTER REMOVAL OF INTERLEVEL OXIDE AND PARTIALLY FIELD OXIDE, EXPOSING POLYSI 2 AND POLYSI 1, AND DIFFUSIONS.

The removal of interlevel oxide exposes bare the two-levels of polysi, Polysi 2 and Polysi 1. Magnified optical photo Figure 4-12 of the chip shows the entire pattern density of the polysi interconnect and polysi-gates only. (These two polysi levels can be compared with the metal mask in Figure 2-9 for interconnect level density.)

Magnified SEM examples which follow in Figures 4-13b through 4-16c display the patterns of exposed two-level polysi of one bistable - latch circuit; referenced to Figure 4-13a (a circuit which is also shown in previous step, Figure 4-11a, with interlevel oxide). These figures together with captions, in this level of materials exposure, present detailed identification and definition of an overlapping two-level polysi pattern, its intra-level SiO_2 insulating separation and polysi-gate channel lengths and widths in P-channel and N-channel transistors. Also, identified are polysi-gate terminations and Polysi 1 crossover patterns with sloping step coverage over field oxide birds beak termination; a lateral perimeter of local oxidation in silicon regions.

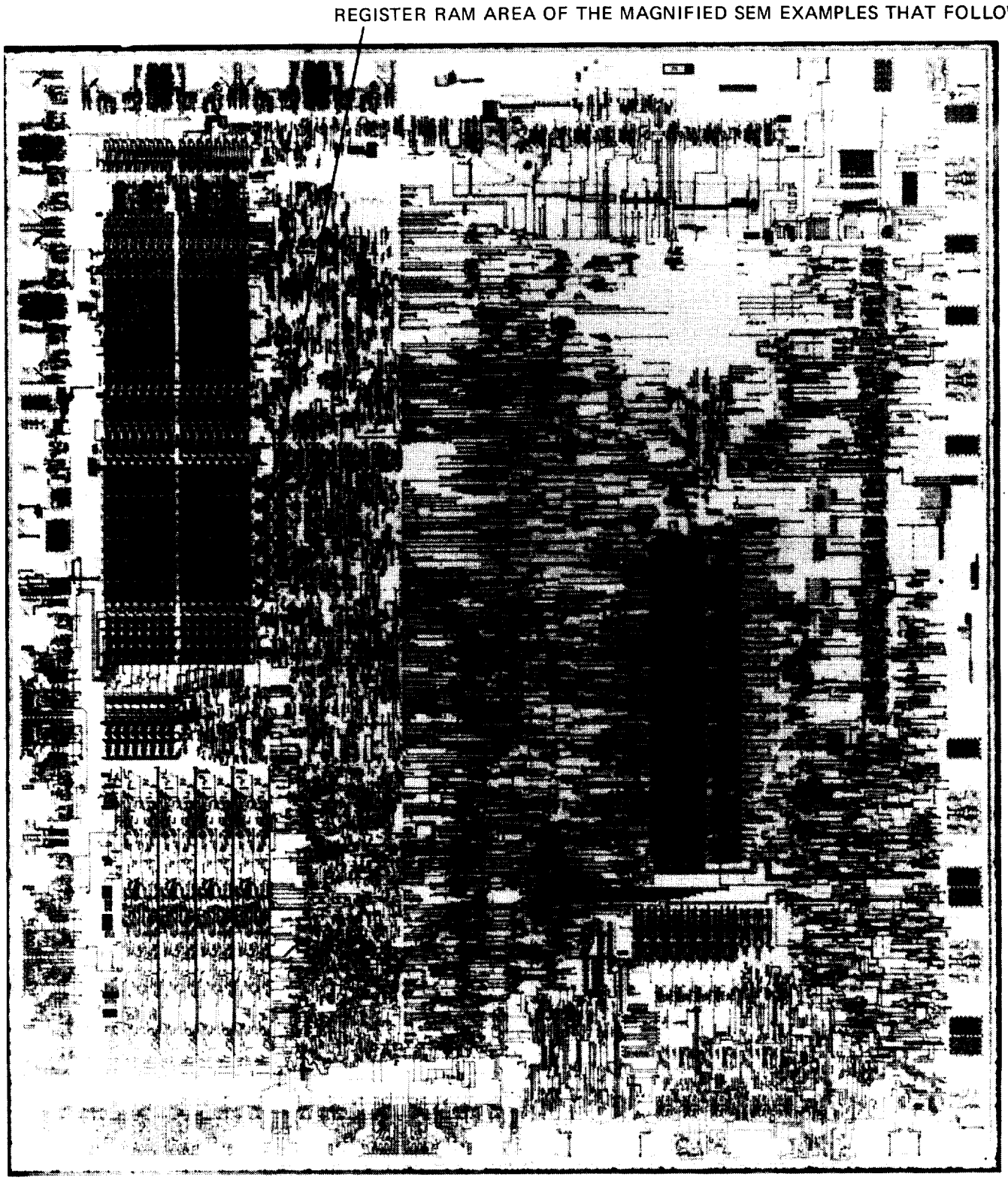
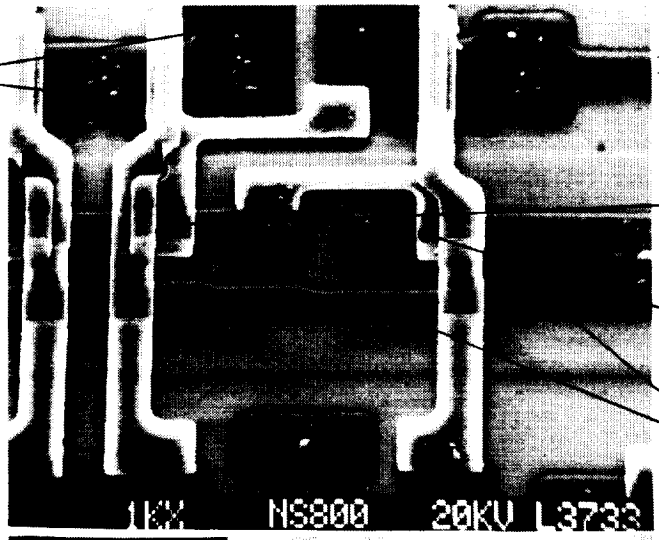


Figure 4-12. (Interlevel oxide removed and partially field oxide). 29X magnified optical view of NSC 800 micro chip with exposed polysi interconnect and gate pattern mask (Polysi 1 and Polysi 2) and contacts in silicon diffusions. (See Figures 2-8 and 4-10.)

REMOVED INTERLEVEL OXIDE AND PARTIALLY FIELD OXIDE (REF. FIGURE 4-11)
EXPOSED TWO-LEVEL POLYSI, POLYSI 1 AND POLYSI 2, P^+ AND N^+ DIFFUSION PATTERNS



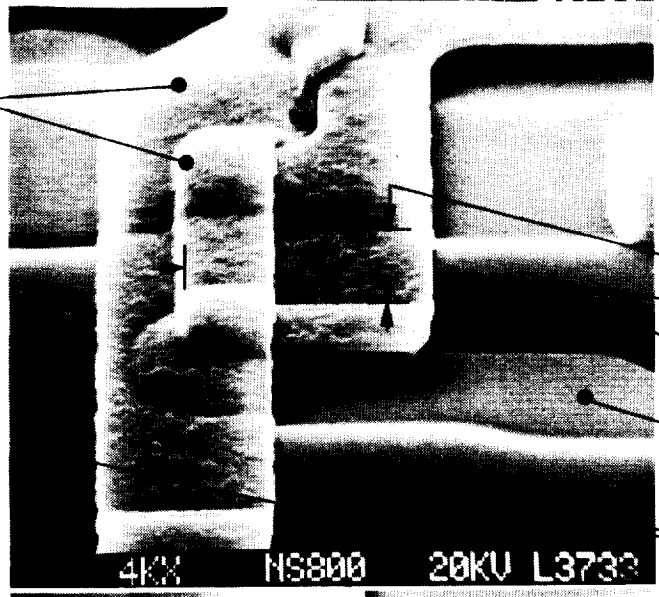
N^+ DIFFUSION

REF AREA MAGNIFIED IN FIGURE 4-13b
POLYSI 1 GATE, P-CHANNEL SOURCE/DRAIN PATTERN

REF AREA MAGNIFIED IN FIGURE 4-13c
POLYSI 1 GATE P-CHANNEL SOURCE/DRAIN PATTERN

P^+ DIFFUSION (SOURCE, V_{CC})

Figure 4-13a. 1000X SEM view of 6-transistor complementary pattern.



POLYSI 2 OVERLAPPING POLYSI 1

POLYSI 1 GATE, P-CHANNEL WIDTH

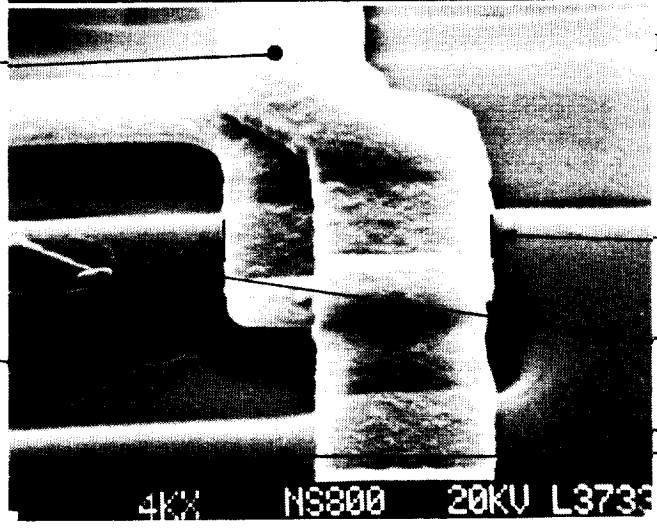
POLYSI 1 P-CHANNEL LENGTH PATTERN

P^+ DIFFUSION, DRAIN SIDE

OXIDE ISOLATION AREA

P^+ DIFFUSION' SOURCE SIDE (V_{CC})

Figure 4-13b. 4000X SEM view of left side Polysi 1 gate P-channel pattern with overlapping Polysi 2 bit line. (Ref. Figure 4-12a.)



POLYSI 2

POLYSI 1 GATE, P-CHANNEL LENGTH PATTERN

FIELD ISOLATION

P^+ DIFFUSION, DRAIN SIDE

P^+ DIFFUSION, SOURCE SIDE (V_{CC})

Figure 4-13c. 4000X SEM view of right side Polysi 1 gate P-channel pattern and Polysi 2. (Ref. Figure 4-13a.)

REMOVED INTERLEVEL OXIDE AND PARTIALLY FIELD OXIDE (Ref. Figure 4-11) EXPOSED TWO-LEVEL POLYSI, POLYSI 1 AND POLYSI 2, P^+ AND N^+ DIFFUSION PATTERNS

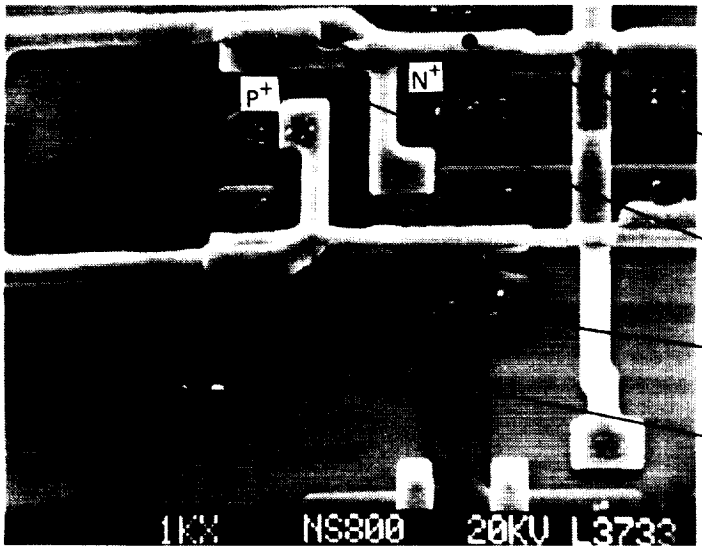


Figure 4-14a. 1000X SEM view of 6-transistor cell at 90° cw turn. (Ref. Figure 4-13.)

REF AREA MAGNIFIED IN FIGURE 4-14b OF POLYSI 1 GATE N-CHANNEL WIDTH

REF AREA MAGNIFIED IN FIGURE 4-14c OF POLYSI 1 GATE P-CHANNEL WIDTH

N^+ DIFFUSION PATTERN

P^+ DIFFUSION PATTERN

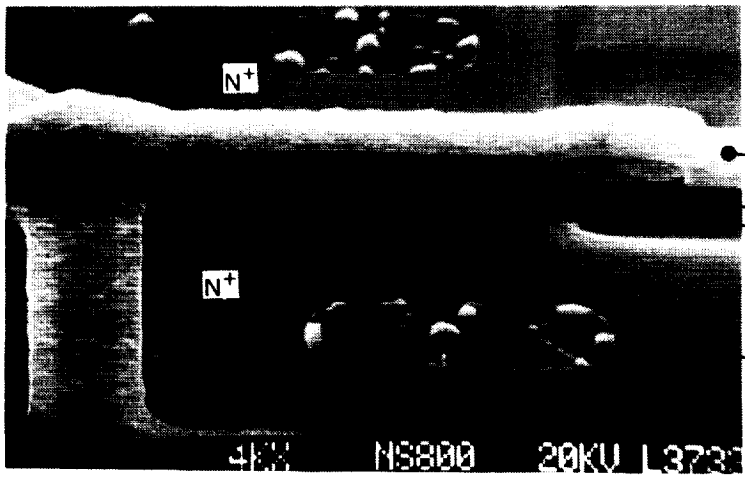


Figure 4-14b. 4000X SEM view at 60° of Polysi 1 gate N-channel width.

POLY 2 BIT LINE OVERLAP AND STEP

SLOPING STEP OF POLYSI 1 GATE TERMINATION OVER FIELD OXIDE BIRDS BEAK

ACTUAL N-CHANNEL WIDTH DEFINED BY POLYSI 1 OUTLINE

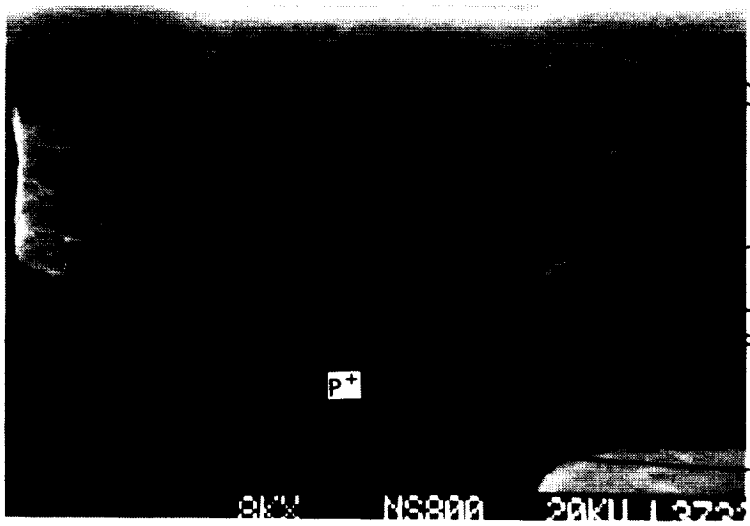


Figure 4-14c. 4000X SEM view at 60° of Polysi 1 gate P-channel width.

POLYSI 2 LEVEL OVER POLYSI 1 AND THICKNESS

POLYSI 1 GATE, ACTUAL P-CHANNEL WIDTH DEFINITION

POLYSI 1 SLOPING STEPS OVER FIELD OXIDE BIRDS BEAK, AND GATE TERMINATION ON LEFT SIDE

FIELD OXIDE

REMOVED INTERLEVEL OXIDE AND PARTIALLY FIELD OXIDE (Ref. Figure 4-11) EXPOSED TWO-LEVEL POLYSI, POLYSI 1 AND POLYSI 2, P^+ AND N^+ DIFFUSION PATTERNS

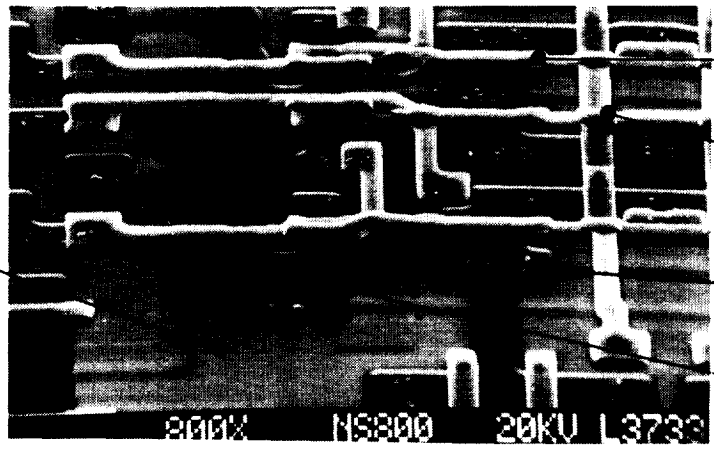


Figure 4-15a. 800X SEM view of 6-transistor cell at 90° cw turn. (See Figure 4-13a.)

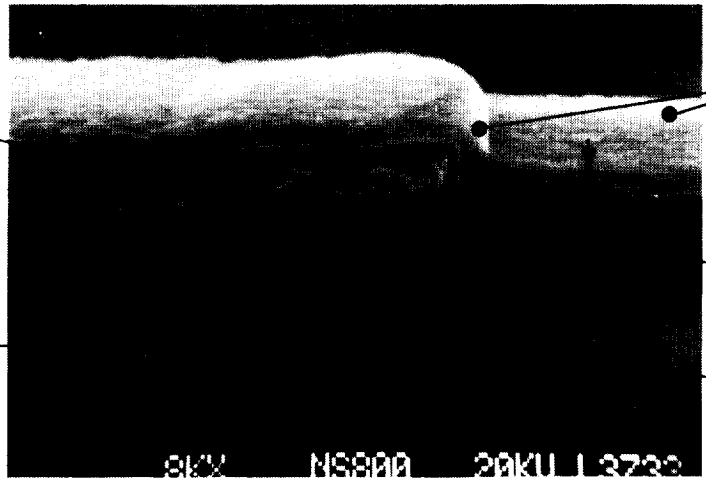


Figure 4-15b. 8000X SEM side view at 70° (Ref. Figure 4-15a.) of Polysi 1 gate termination over field oxide and Polysi 2 step.

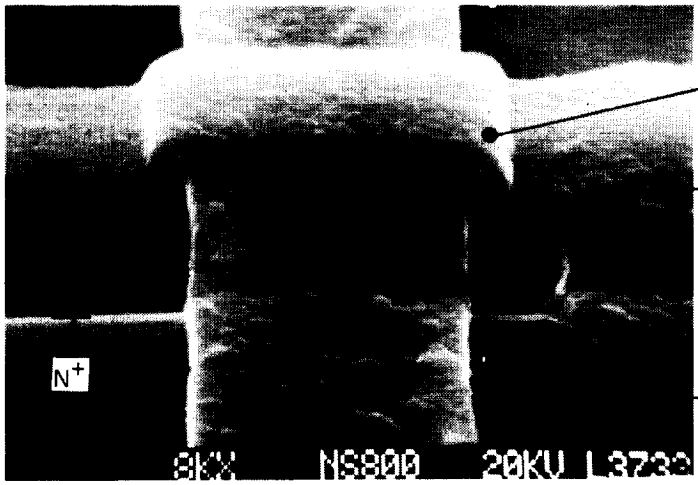
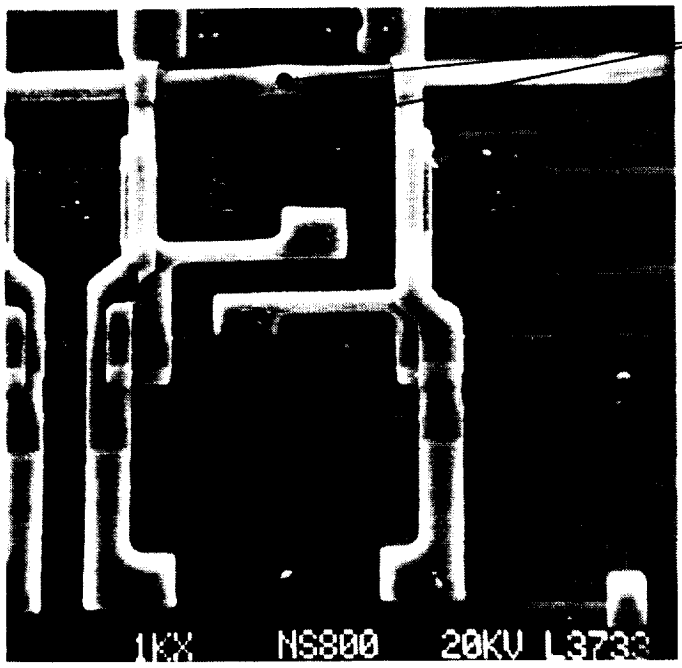


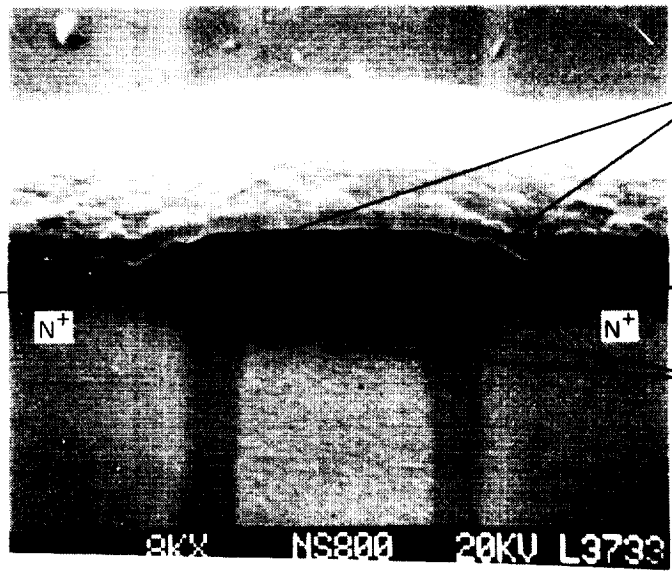
Figure 4-15c. 8000X magnified SEM side view at 70°, (Ref. Figure 4-15a.) of Polysi 2 step and thickness with isolation over Polysi 1.

REMOVED INTERLEVEL OXIDE AND PARTIALLY FIELD OXIDE (Ref. Figure 4-11) EXPOSED TWO-LEVEL POLYSI, POLYSI 1 AND POLYSI 2, P^+ AND N^+ DIFFUSION PATTERNS



REF AREA MAGNIFIED IN FIGURE 4-16b BELOW, IDENTIFYING NARROW OXIDE ISOLATION SEPARATING THE TWO N^+ DIFFUSIONS AND POLYSI 1 BRIDGING PATTERN AND GATES OF TWO N-CHANNEL PASS-TRANSISTORS

Figure 4-16a. 1000X SEM view of complementary 6-transistor cell pattern exposed Polysi 1 and Polysi 2.



RESIDUAL FIELD OXIDE WITH BIRDS BEAKS

OTHER EDGE OF N-CHANNEL WIDTH

EDGE OF N-CHANNEL WIDTH

SLOPING TROUGH OF ISOLATION REGION IN SILICON WITH PARTIALLY REMOVED FIELD OXIDE

Figure 4-16b. 8000X magnified SEM side view at 60^o of Polysi 1 bridge with sloping steps over narrow oxide isolation region separating and defining two N^+ diffusions.

4.5.1 Summary and Conclusions

Only at this level of materials exposure is it possible to examine and define any anomalies in P^+ and N^+ diffusions, as well as the interface of two-level polysi relative to photo mask steps and the materials definition. Also, by completely removing interlevel oxide insulation, the effect of a wet chemical etch on the exposed contacts in silicon interface would define more sharply the existence of pitting features in these contacts if there are any (an effect of metal sintering step). These contacts, however, appear clean and relatively smooth.

The insulating SiO_2 between the two polysi levels at the oxide and Polysi 1 step shows acceptable isolation in Figures 4-15b and 4-15c.

Examples of birds-beak field oxide definition are in Figures 4-14b, 4-15b and 4-16b.

The SEM examination on this level did not uncover any significant anomalies.

4.6 STEP 4: SEM EXAMINATION AFTER REMOVAL OF POLYSI 1 AND POLYSI 2, FIELD OXIDE AND THIN GATE OXIDE

The removal of the two-level polysi, field oxide and thin gate-oxide exposed bare the silicon chip substrate with N^+ and P^+ diffusion patterns.

Magnified optical photo Figure 4-17 of the chip shows the exposed P^+ and N^+ diffusions (cell patterns) density only. The exposed cell diffusions in N-silicon substrate in this figure, combined with two-level polysi interconnect in Figure 4-12, together with the metal mask in Figure 2-9 typifies the active interface of this microprocessor chip.

SEM Figures 4-18a through 4-18c are again the referenced examples of a bistable latch circuit pattern now in exposed silicon diffusions.

SEM Figure 4-18b compares these silicon patterns with polysi-gates in SEM Figure 4-16a of previous step.

The outlines of channel paths in P^+ and N^+ silicon where Polysi 1 was present are quite distinct.

The implanted N^+ and P^+ patterns of silicon appear higher than the lateral silicon isolation regions of N-substrate and P-well. In fact, the outline of P-well perimeters appears to be the most deeply recessed region in silicon which

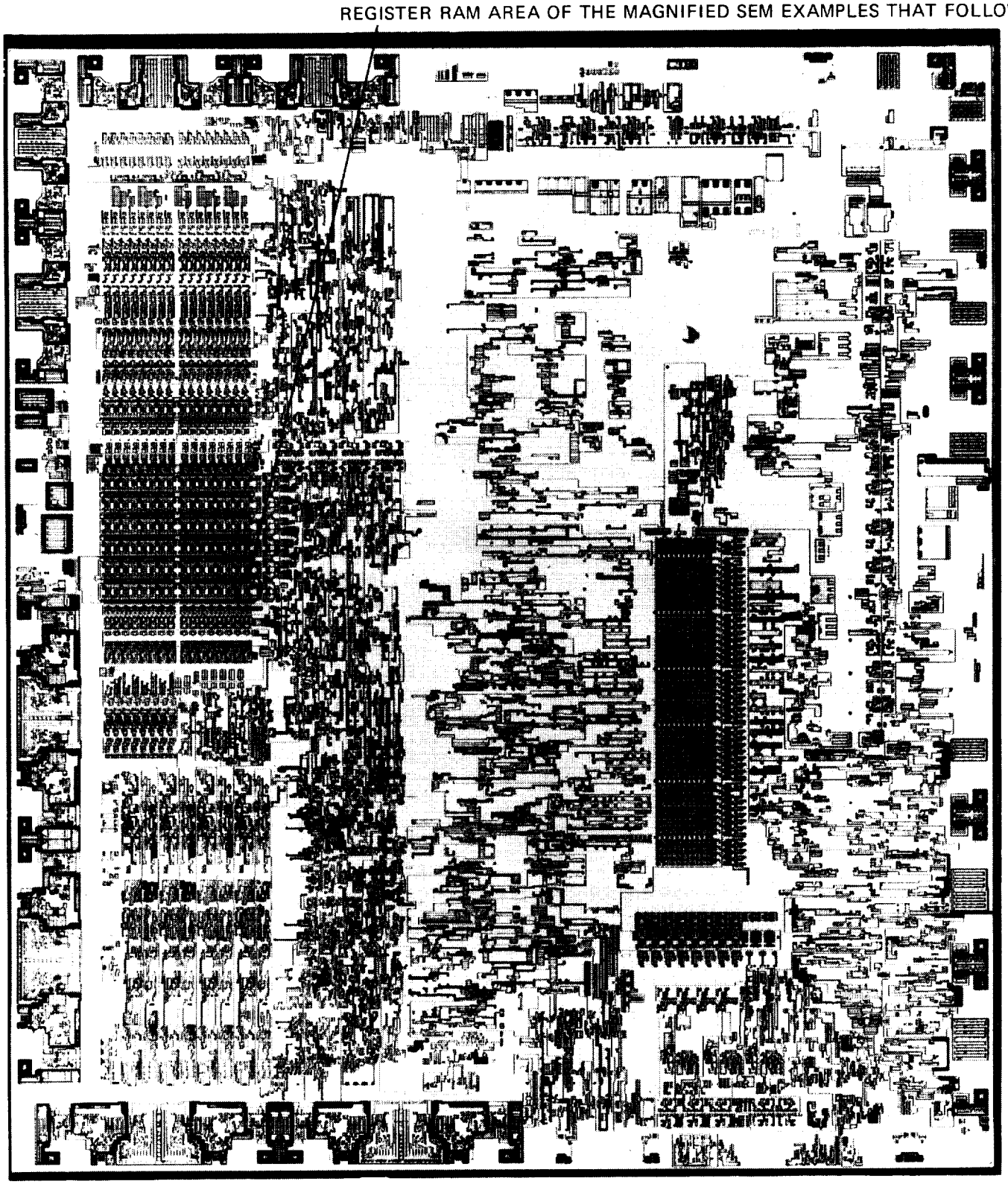


Figure 4-17. (Removed two-level polysi and field oxide.) 29X magnified optical view of chip exposed P^+ and N^+ cell diffusions in silicon substrate, and contacts.

REMOVED TWO-LEVEL POLYSI, FIELD OXIDE AND THIN OXIDE (Ref. Fig. 4-13a) EXPOSED P^+ AND N^+ CELL DIFFUSIONS IN SILICON SUBSTRATE AND P-WELL DEFINITION

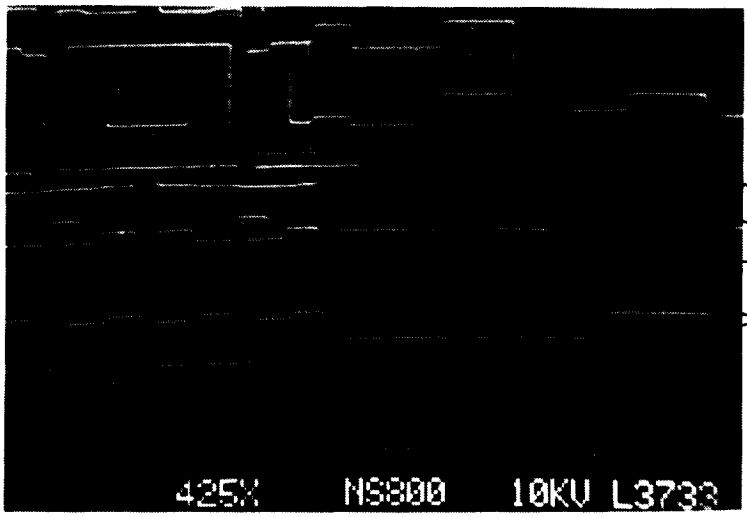


Figure 4-18a. 425X SEM view of register segment P^+ and N^+ cell diffusion patterns defined in silicon substrate.

N^+ CELL DIFFUSIONS

P-WELL OUTLINE

P^+ CELL DIFFUSIONS

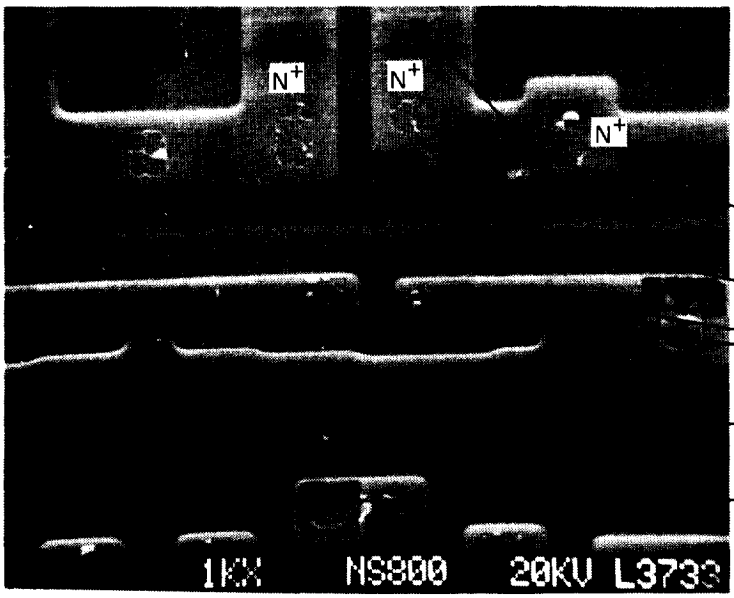


Figure 4-18b. 1000X SEM view of exposed P^+ and N^+ (6-transistor) cell diffusion patterns and P-well outlines. (Ref. Figures 4-13a and 4-18a.)

N-CHANNEL PATTERN IN SILICON AND N^+ DIFFUSION

P-WELL AND P-WELL LINE

P-CHANNEL PATTERN IN SILICON AND P^+ DIFFUSION

N-SUBSTRATE

P-WELL WITH CONTACT IN SILICON

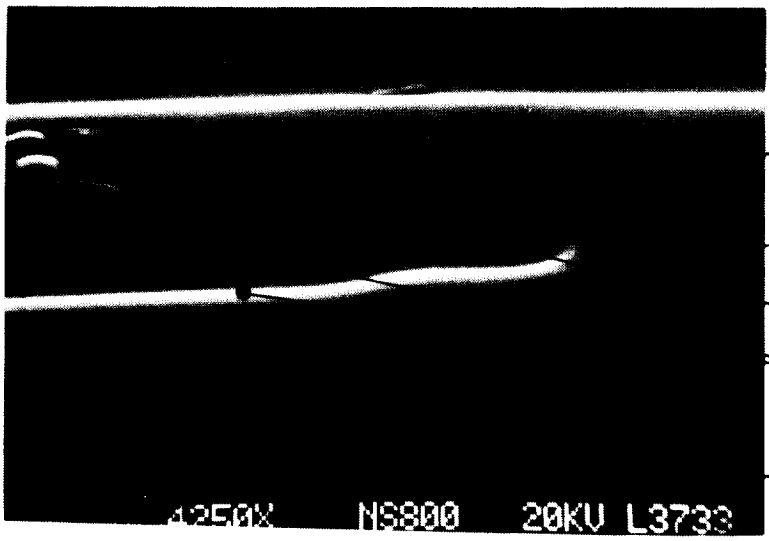


Figure 4-18c. 4250X magnified SEM view of P^+ diffusion segment. (Ref. Figure 4-18b.)

EDGE OF CHANNEL OUTLINE IN SILICON

P^+ SILICON DIFFUSION, SOURCE SIDE

CONTACT IN P^+ SILICON DRAIN SIDE

ISOLATION TROUGH IN SILICON AND SLOPING EDGE AFTER FIELD OXIDE REMOVAL

SILICON SUBSTRATE

(ALSO SEE FIGURES 13a THROUGH 16c AND COMPARE)

resulted from the initial masking step of P-well patterns definition and the subsequent local oxidation step.

SEM Figure 4-18c shows a magnified segment of an elevated P^+ silicon diffusion pattern, in N-substrate, with a rounded sloping edge due to the effect of the local oxidation process step. This edge defines the field oxide perimeter (now removed) terminated in birds-beaks beneath Polysi 1 interfacing patterns with the active diffusion regions.

The cross-sectioned definition of some of these patterns are shown in certain details in SEM Figures 5-2a through 5-5, which follow in Section V.

4.6.1 Summary and Conclusions

The SEM photo examples of chip exposed silicon provide an insight into the formation of lateral patterns in terms of photo masks and process steps on silicon substrate.

The added etching step, with a wet chemical solution, to expose this level did not adversely affect the silicon surface or its contacts.

Figure 4-18b shows a typical P-well buried contact which the metal interface overlaps on a source side to N^+ diffusion in V_{SS} bus (see Figures 4-9a and 4-11a). The P^+ diffusions (on source side) in certain areas are similarly strapped to N-substrate in V_{DD} bus pattern.

Figure 4-18c shows, in a channel path outline, two very small pinholes on the inside edge of the isolation region.

SECTION 5

CHIP CROSS-SECTIONING

5.1 PHYSICAL CROSS-SECTIONING OF NSC 800 CHIP

A cross-sectioning of a chip was performed using a standard polishing and lapping system in two steps, A and B.

Step A, Figures 5-1a, b and c, shows approximations of vertical definition (thickness) of chip surface materials interfacing with silicon substrate (e.g., top SiO_2 passivation, metallization, interlevel oxides and the two-level polysi, Polysi 1 and Polysi 2).

Examples in Step B, SEM Figures 5-2a through 5-5, display in detail the definitions (by staining the cross-section) of junction depths, effective channel length in silicon, Polysi 1 gate-length, together with gate oxide isolation in the channel path, and the two-level polysi with intra-level oxide insulation.

These figures, together with captions, provide an insight into cross-sectioned materials and their approximate dimensions.

5.1.1 Summary and Conclusions

The cross-section examples are from a single device and are not an extended cross-section sampling of several chips. The significant patterns appear to be in the overlapping features of Polysi 1 and Polysi 2 in Figures 5-1c and 5-5.

Figure 5-2 does not appear to show a channel stop implant guard band at the edge of P-well which indicates that the implanted guard band isolations are not used in this design and process.

CROSS SECTION SEGMENT OF NSC 800 MICROPROCESSOR CHIP WITH OXIDE LEVELS ALUMINUM METAL AND TWO LEVEL POLYSI, POLYSI 1 AND POLYSI 2

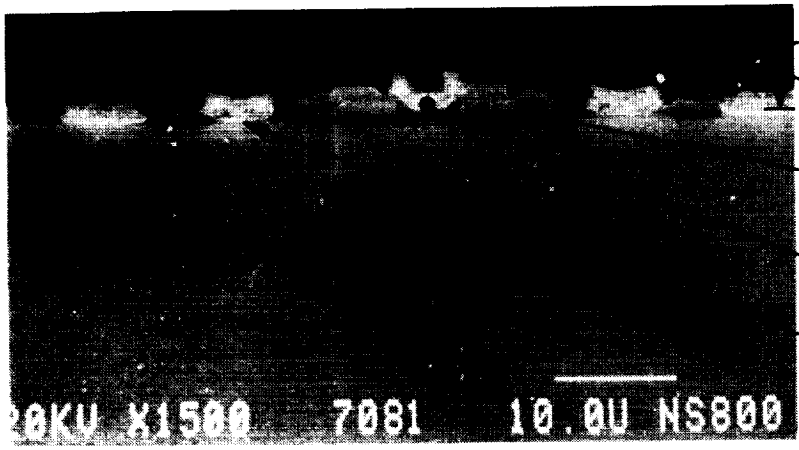


Figure 5-1a. 1500X SEM view of silicon cross section segment reference and magnified patterns in Figures 5-1b and 5-1c below.

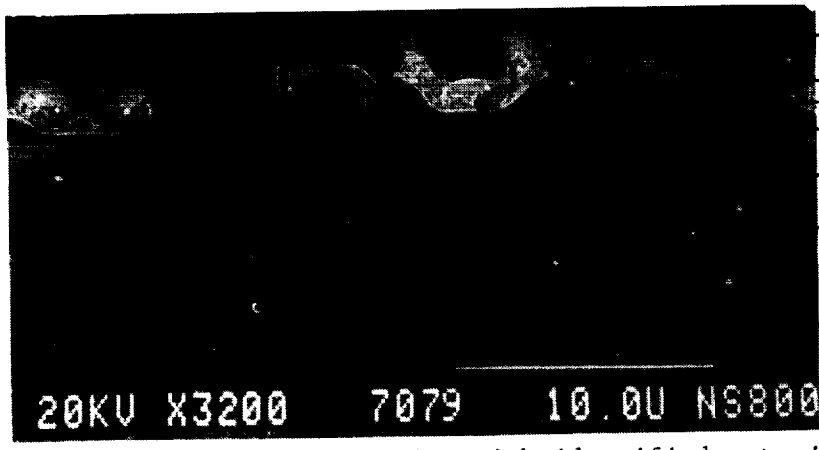


Figure 5-1b. 3200X SEM view with identified materials patterns. (Ref. Figure 5-1a.)

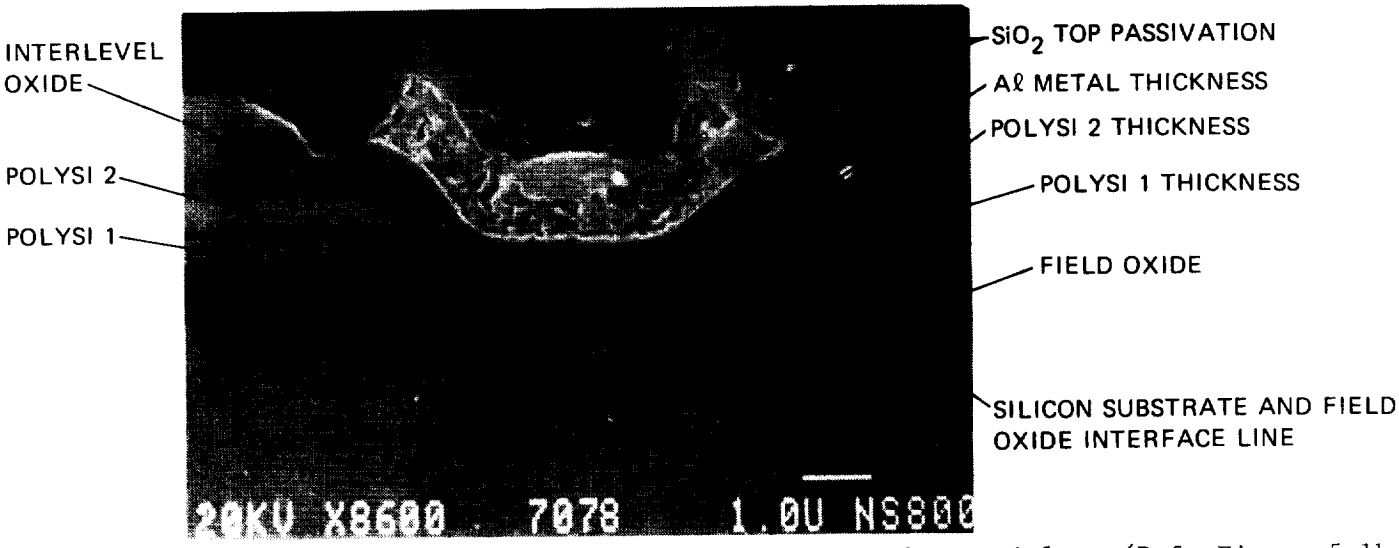


Figure 5-1c. 8600X magnified SEM view of cross sectioned materials. (Ref. Figure 5-1b.)

CROSS SECTION SEGMENT OF NSC 800 MICROPROCESSOR CHIP, AFTER STAINING, WITH DELINEATED DEPTH OF A P-WELL WITH N^+ DIFFUSIONS AND POLYSI-GATES WITH CHANNEL PATTERNS

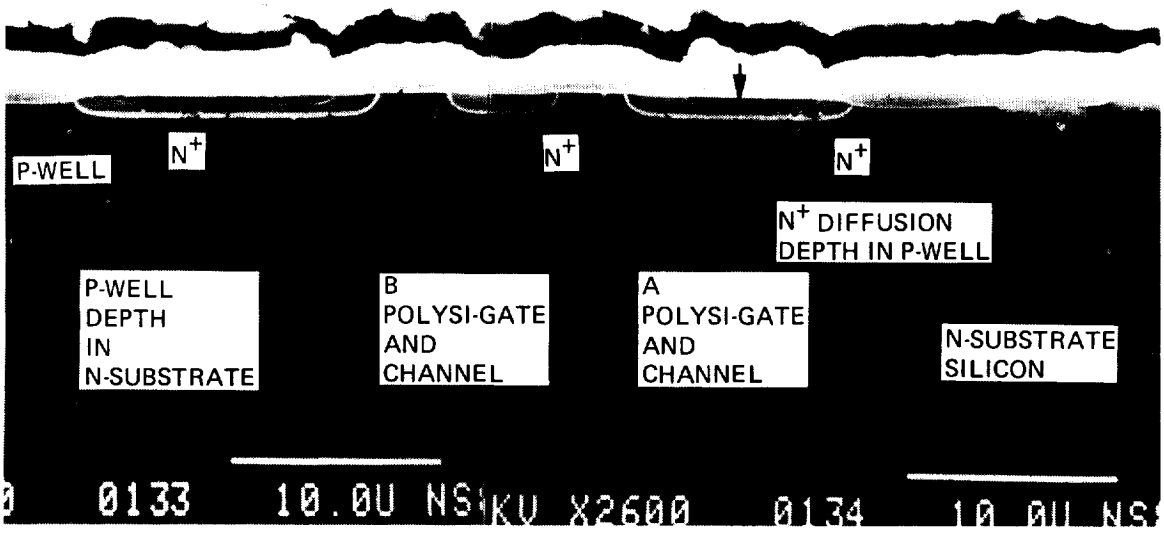


Figure 5-2a. 2600X SEM view of cross section segment reference and magnified functions with channel patterns in Figure 5-2b and 5-2c below.

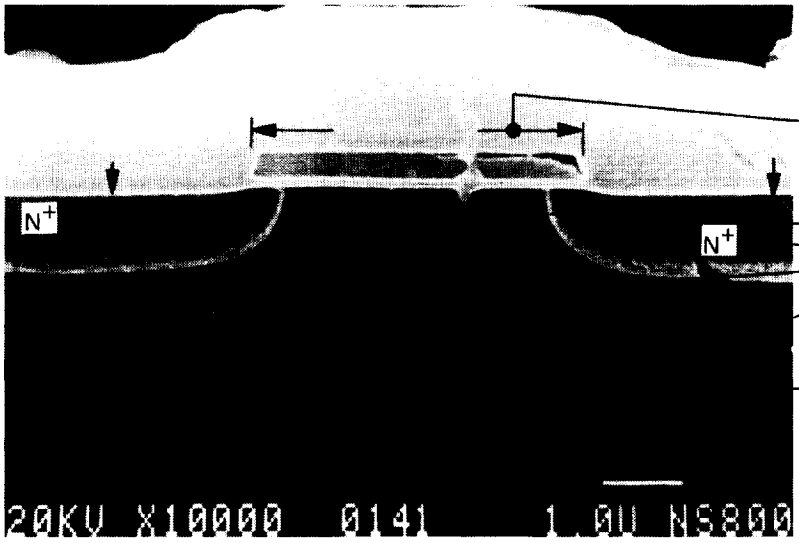


Figure 5-2b. Channel A and Polysi 1 gate pattern.

A POLYSI-GATE LENGTH OVER CHANNEL LENGTH IN SILICON

CHANNEL LENGTH IN SILICON

N^+ DIFFUSION DEPTH

P-WELL

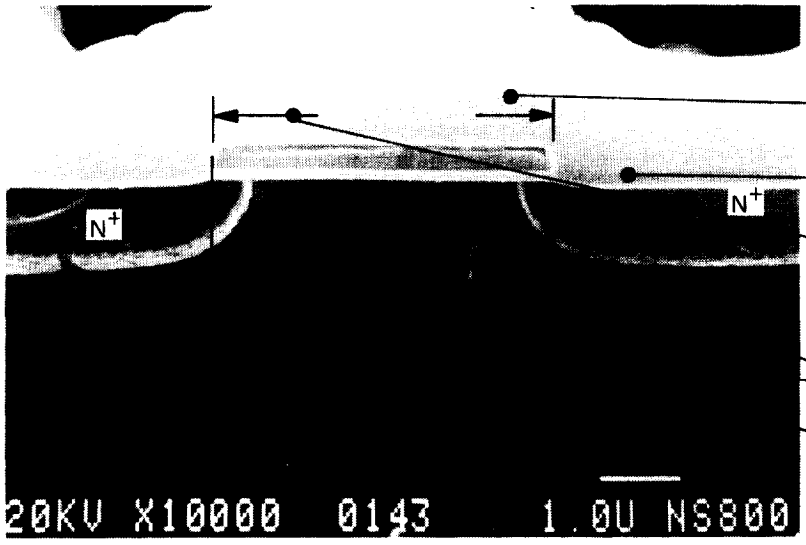


Figure 5-2c. Channel B and Polysi 1 gate pattern.

DEPOSITED INTERLEVEL OXIDE

FIELD OXIDE (LOCAL OXIDATION)

B POLYSI-GATE LENGTH OVER N-CHANNEL LENGTH

TYPICAL POLYSI-GATE CHANNEL OVERLAP IN SILICON WITH N^+ DIFFUSION SPREAD BENEATH (TWO SIDES OF CHANNEL LENGTH)

CROSS SECTION SEGMENT OF NSC 800 MICROPROCESSOR CHIP, AFTER STAINING, N-CHANNEL CELL WITH DELINEATED OXIDES, POLYSI 1-GATE AND CHANNEL-LENGTH, P-WELL DEPTH AND N^+ DIFFUSION DEPTH

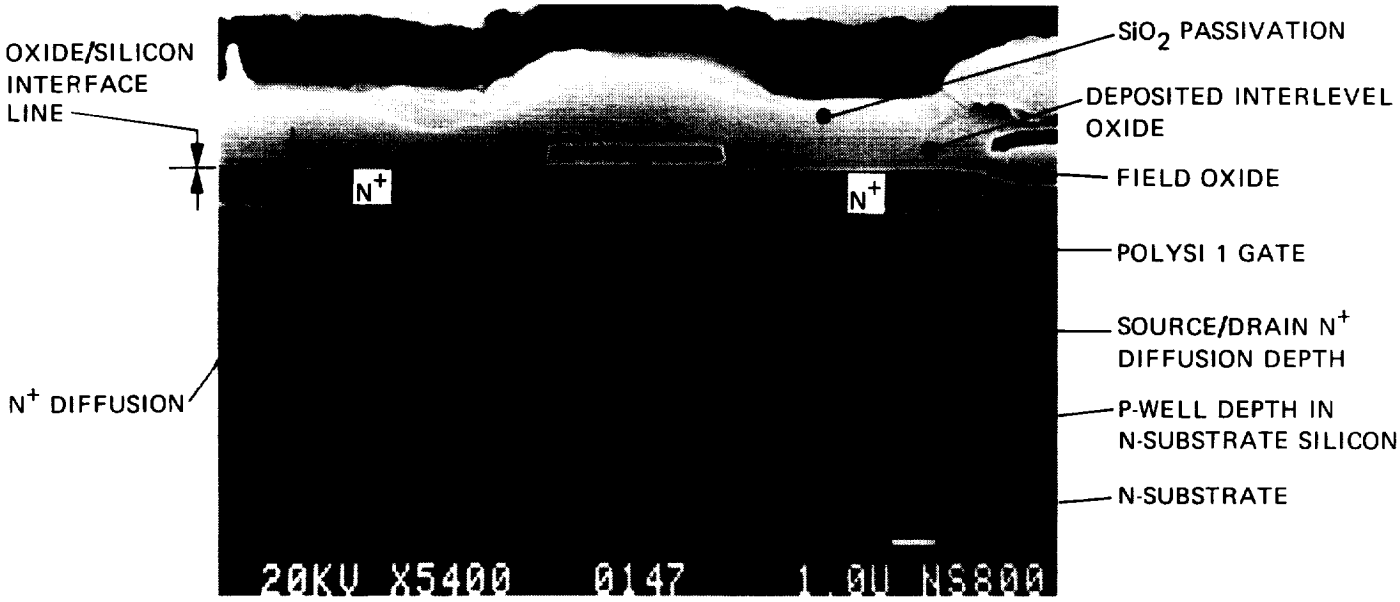


Figure 5-3a. 5400X SEM view of N-channel transistor materials cross section with Polysi 1-gate, N^+ diffusions and P-well depth in silicon.

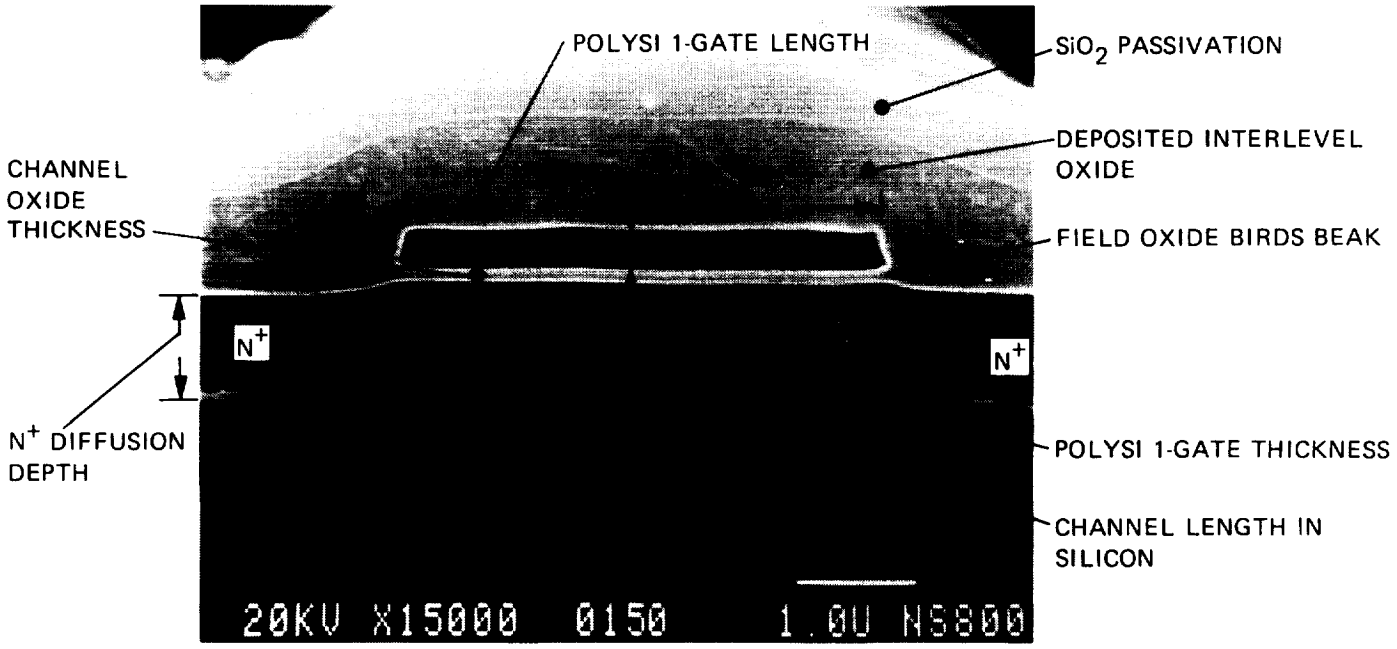


Figure 5-3b. 15,000X magnified SEM view (Ref. Figure 5-3a) of channel length in silicon versus Polysi 1-gate length and channel oxide.

ANOTHER CROSS SECTION SEGMENT OF NSC 800 MICROPROCESSOR CHIP, AFTER STAINING, OF DELINEATED TWO-LEVEL POLYSI PATTERN, POLYSI 1 AND POLYSI 2 THICKNESS WITH INTERLEVEL OXIDE INSULATION ON TOP OF FIELD OXIDE

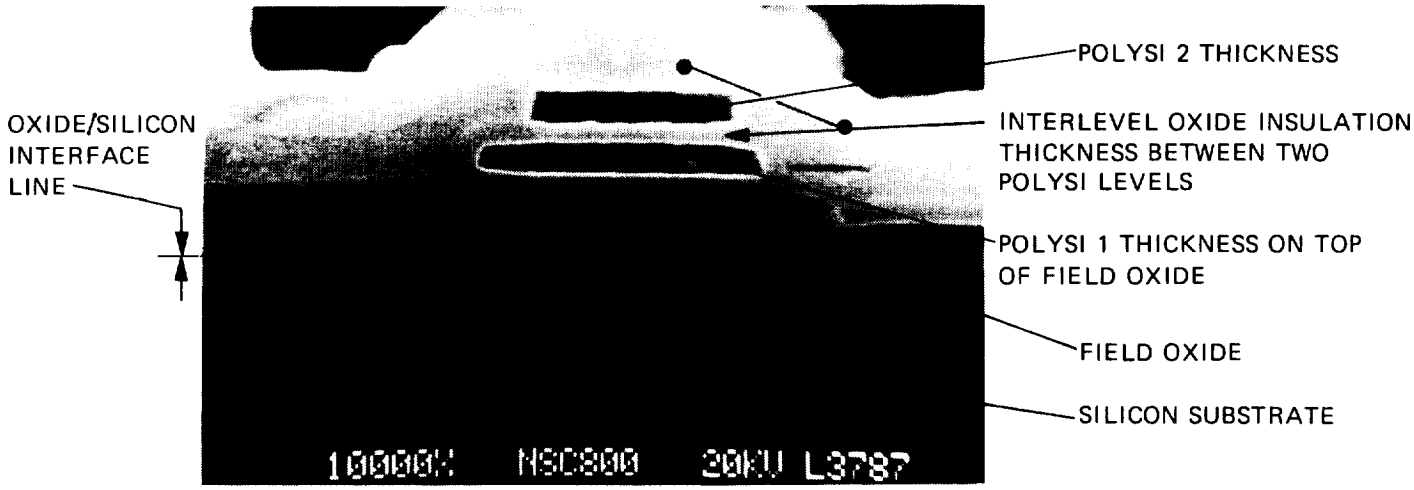


Figure 5-4. 10,000X magnified SEM view of cross sectioned two-polysi levels within insulating oxide levels.

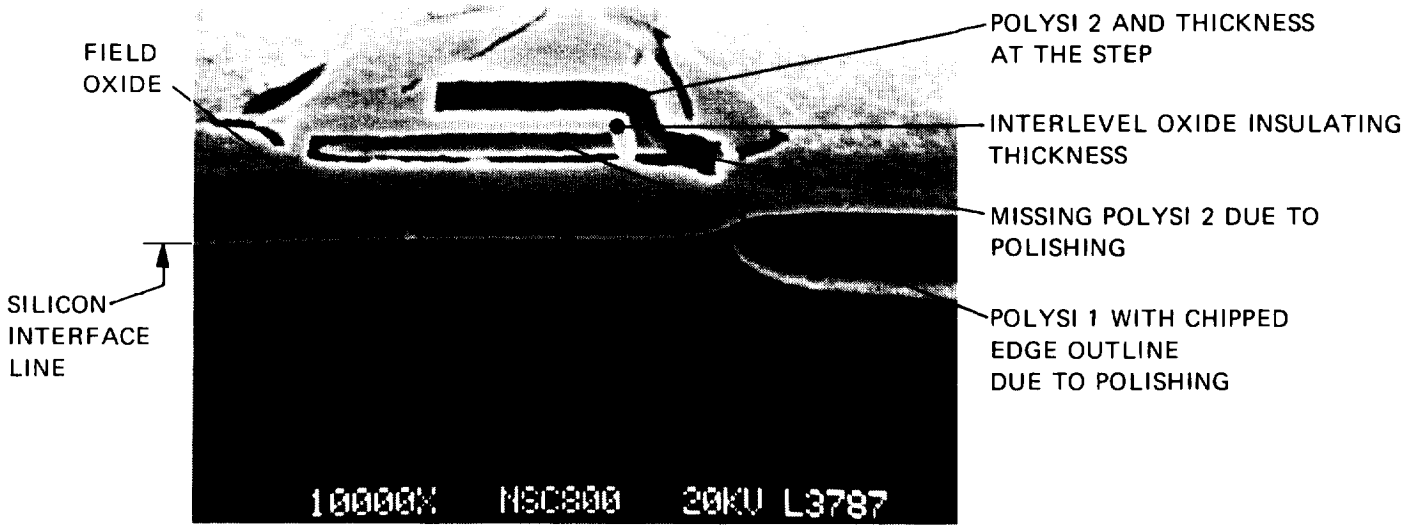


Figure 5-5. 10,000X magnified SEM view of cross sectioned two-polysi levels within insulating oxide levels. Note Polysi 2 overlapping step and interpoly oxide insulation at the step between Polysi 2 and Polysi 1. (Also see Figures 5-1b and 5-1c.)

SECTION 6

PROCESS FABRICATION

6.1 FABRICATION MATERIALS AND PATTERNS

The NSC 800 8-bit CMOS microprocessor chip is fabricated on an N-type <100> silicon wafer, using P^2CMOS Process Technology.

The sequence of fabrication, derived from observations made through this evaluation, approximates the photo mask and process steps shown in Figures 6-1 through 6-6.

The chip has four levels of interconnect. The top level is silicon doped aluminum, beneath it are two levels of polysi (Polysi 1 and Polysi 2). Polysi 1 is used as a gate polysi and Polysi 2 is used as an interconnect. The diffusions are the fourth level. The P-wells with (N^+) source terminations form V_{SS} bus with interconnect to V_{SS} pad. The (P^+) source terminations with N-substrate form V_{DD} bus with an interconnect to a V_{DD} pad. Except for contacts interface, all 4 levels of interconnect are isolated by interlevel insulating (SiO_2) oxides.

The chip process uses selective local oxidation on silicon substrate. This localized oxidation of silicon regions in reactive oxide growth, generated from the silicon surface, provides for markedly more planar surface with recessed patterns of N-substrate regions and P-well areas beneath grown thick field oxide. The local oxidation step is initiated right after the P-well patterns are defined, using nitride and a photo resist mask.

This nitride/resist masking forms a protection from selective local oxidation encroachment of mask defined silicon patterns within each P-well as well as on N-substrate designated for N-channel and P-channel transistor circuit areas; afterwards, the nitride with resist is removed. Thus, these defined silicon patterns, which will subsequently form N^+ regions in P-wells and P^+ regions in N-substrate, remain intact and well above the recessed silicon patterns of isolation regions beneath the grown thick field oxide. Laterally they may be almost equal in planar features with the outlined perimeters of surrounding field oxide (See Figures 4-9a and 4-11a).

The standard steps which follow are gate oxide and Polysi 1 deposition followed by polysi-gate pattern definition. Subsequent masking steps and

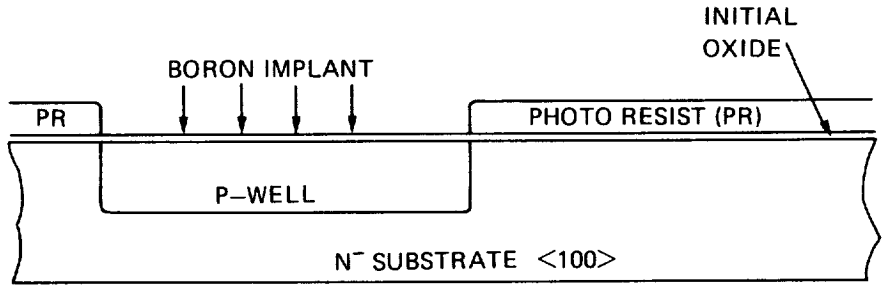


Figure 6-1. Three-step example for: 1) Initial wafer oxidation; 2) Photo-resist mask for P-well outlines; 3) Boron implant for P-well depth definition in silicon.

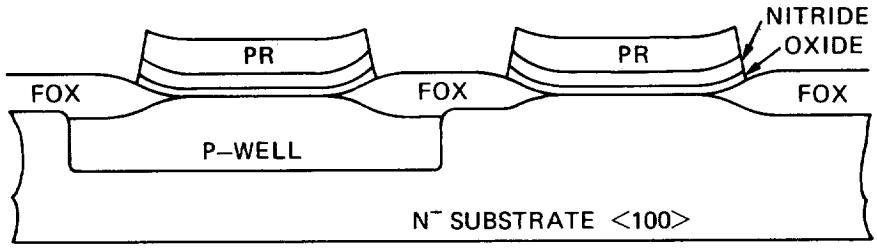


Figure 6-2. Four-step example for: 1) Photo-resist and initial oxide removed; 2) New oxide/nitride and resist mask deposition; 3) Photo mask pattern, with etchback of oxide/nitride and photo resist for silicon substrate isolation region; 4) Reactive process of field oxide growth depleting exposed silicon and recessing the surface of silicon substrate. (See Figures 4-18a, 5-2a.)

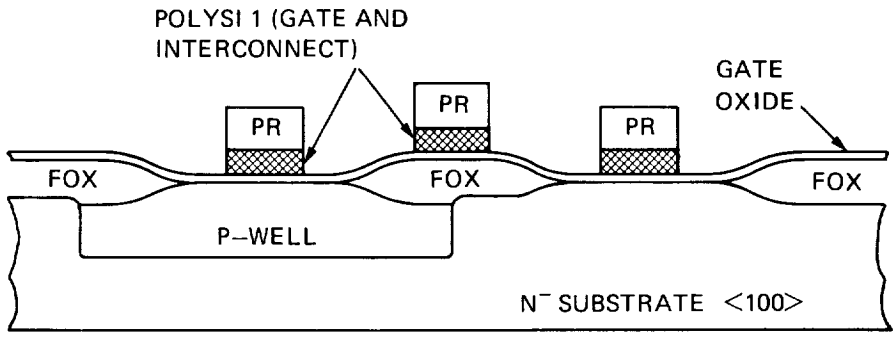


Figure 6-3. Four-step example for: 1) Photo-resist, oxide/nitride mask removed; 2) Thin gate oxide deposition; 3) Polysi 1 deposition; 4) Photo-resist mask pattern, with etchback of Polysi 1, for gates and interconnect definition.

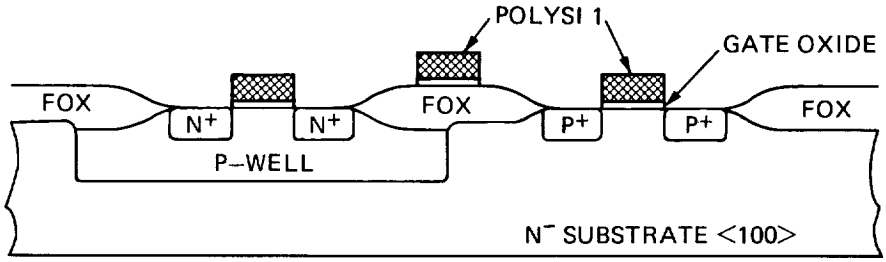


Figure 6-4. Three-step example with substeps, showing: 1) Photo-resist and thin oxide removed; 2) Photo-resist mask pattern over P-well areas, with etch-back step, for P^+ areas in N-substrate, followed by boron implant defining P-channel transistors; 3) Photo-resist removed and redeposited with etchback in P-well areas for N^+ phosphorous implant defining N-channel transistors.

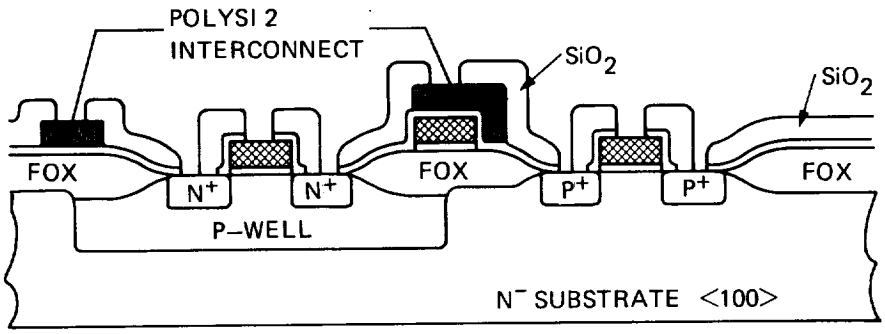


Figure 6-5. Four-step example with substep, showing: 1) SiO_2 deposition for intra-polysi insulation; 2) Deposition of Polysi 2 and photo-mask pattern with etchback of Polysi 2 for interconnect; 3) Deposition of SiO_2 (an insulator for subsequent metallization); 4) Photo-resist mask with etchback for contact apertures in SiO_2 levels to Polysi 1 and Polysi 2 and silicon diffusions. (See Figure 4-11a.)

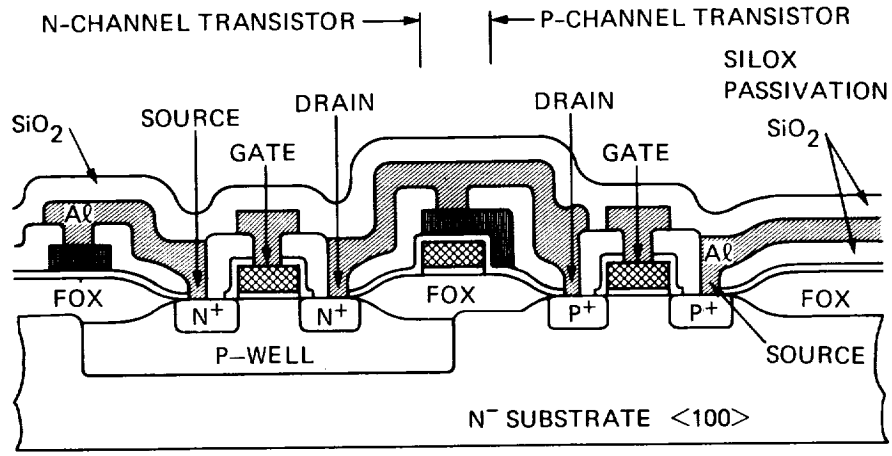


Figure 6-6. Three-step example with substeps, showing: 1) Deposition of silicon doped aluminum metallization and sintering step; 2) Photo-resist mask pattern and etchback for metallization interconnect mask; 3) Deposition of protective SiO_S (Silox) passivation followed by photo-resist mask pattern and etchback for die pads and test patterns. (See Figure 2-12.)

NOTE: In subsequent steps the wafer back-plane is prepared with conductive interface, and the wafer chips are ready to be tested for slicing and packaging and testing in assembled package.

implantations define self-aligned channel patterns with source and drain areas for P-channel and N-channel transistor circuits.

In addition (this device having a two-level polysi), after P-channel and N-channel transistors are defined, a thin insulating film of SiO_2 is deposited (2500 to 3000 Å thick) followed by deposition step of Polysi 2; a photo mask pattern forms Polysi 2 interconnect.

Note: In this device process, Polysi 2 does not interface directly with contacts in silicon diffusions or Polysi 1 gates, but is linked only with butting type metal contacts or straight links.

The next step which follows is another deposition of insulating SiO_2 with a subsequent photo-mask step and etchback for opening of contact apertures in the deposited oxides to silicon diffusions, Polysi 1-gates and Polysi 2 interconnect. An aluminum metal deposition, which follows, interfaces with these contacts in Polysi 1 and 2 and silicon. After the sintering step of aluminum, a photo-mask step and etchback defines the aluminum interconnect mask on the chip. Last, a protective cover of insulating SiO_2 is deposited on the entire chip/wafer followed by a photo mask and etchback to expose the die pads. The wafer back plane is then conductively prepared and the chips are tested, with the wafer (chips) ready for slicing.

6.2 DIE INTERNAL MATERIALS AND DIMENSIONS

Most of these dimensions were derived from approximations from SEM photos, taking into account the SEM magnification factor and the position of specimen in the SEM.

Table III. Physical Dimensions and Materials

1.	Die attach material		Gold eutectic
2.	Die size		6 x 6.75 mm
3.	Silicon substrate		<100> N-type
4.	Die passivation (Silox)		SiO_2
5.	Passivation thickness		1.1 μ
6.	Die wire bond		Aluminum
7.	Wire bonding technique (wedge)		Ultrasonic compression
8.	Die metallization		Aluminum Si
9.	Typical metallization thickness		1.2 μ
10.	Minimum metal thickness at oxide and polysi steps		1.0 μ
11.	Minimum metal line width		4.5 μ
12.	Minimum metal line separation		5.0 μ
13.	Typical field oxide thickness		0.9 μ
14.	Typical SiO_2 insulation between Polysi 1 and Polysi 2		0.25 μ
15.	Polysi 1 thickness (gate-polysi)		0.5 μ
16.	Polysi 2 thickness (interconnect)		0.4 μ
17.	Polysi-gate (N-channel length)	6-T Register cell Ref. Figures 4-13a thru 4-14	4.7 μ
18.	Polysi-gate (N-channel width)		12.0 μ
19.	Polysi-gate (P-channel length)		8.7 μ
20.	Polysi-gate (P-channel width)		4.8 μ
21.	Polysi-gate (P-channel width)		0.9 μ
22.	Typical P-well depth in N substrate		9.0 μ
23.	Approximate gate oxide thickness		700 Å

National Semiconductor

July 1983

NSC800™ High-Performance Low-Power Microprocessor

General Description

The NSC800 is an 8-bit microprocessor that functions as the central processing unit (CPU) in National Semiconductor's NSC800 microcomputer family. The device is fabricated using National's P^2CMOS^{TM} technology. This technology provides the system designer with devices equaling the performance levels of comparable NMOS products, combined with the low-power advantages of CMOS. Many system functions are incorporated on the device, such as: vectored priority interrupts, refresh control, power-save feature and interrupt acknowledge. The NSC800 is housed in dual-in-line and chip carrier packages.

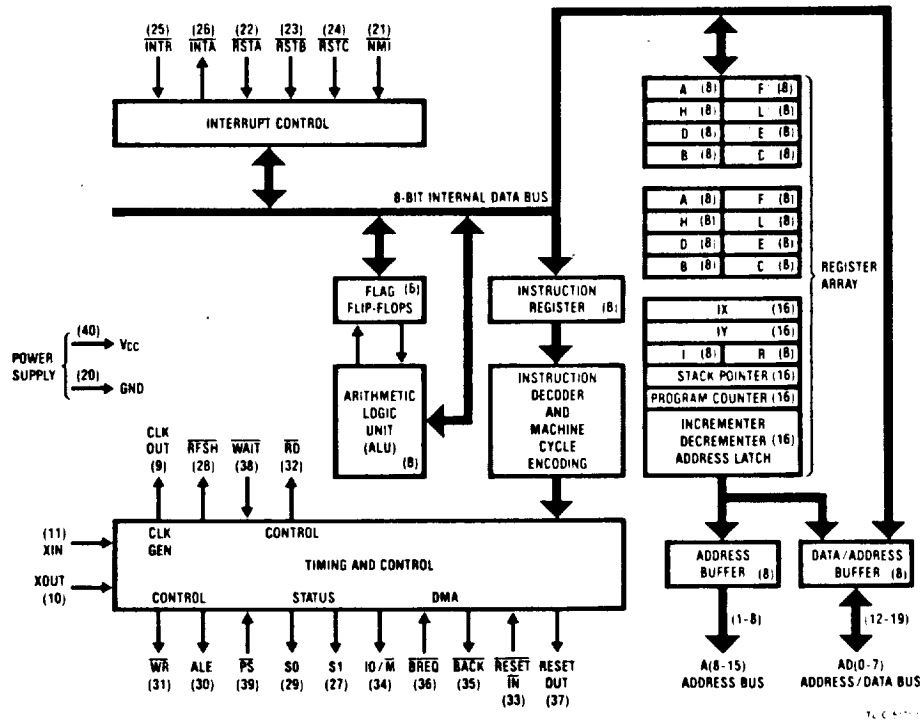
Dedicated peripherals (NSC810 RAM I/O Timer, NSC831 I/O and NSC858 UART) have on-chip logic for direct interface to the NSC800. In addition, National also offers a full line of CMOS components to allow a full low-power solution to system designs.

For military applications, the NSC800 is available with class B screening in accordance with Method 5004 of MIL-STD-883.

Features

- Variable power supply 2.4V – 6.0V
- Fully compatible with Z80 instruction set
- Powerful set of 158 instructions
- 10 addressing modes
- 22 internal registers
- Low power: 50 mW at 5V V_{CC}
- Multiplexed bus structure
- On-chip bus controller and clock generator
- On-chip 8-bit dynamic RAM refresh circuitry
- Speed: 1.0 μs instruction cycle at 4.0 MHz
  - NSC800-4 4.0 MHz
  - NSC800 2.5 MHz
  - NSC800-1 1.0 MHz
- Capable of addressing 64k bytes of memory and 256 I/O devices
- Five interrupt request lines on-chip
- Schmitt trigger input on reset
- Unique standby-current (power-save) feature

CPU Functional Block Diagram



NSC800™ and P^2CMOS^{TM} are trademarks of National Semiconductor Corp
TRI-STATE® is a registered trademark of National Semiconductor Corp
Z80® is a registered trademark of Zilog Corp

Absolute Maximum Ratings (Note 1)

Storage Temperature	− 65°C to + 150°C
Voltage on Any Pin with Respect to Ground	− 0.3V to V_{CC} + 0.3V
Maximum V_{CC}	7V
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions V_{CC} = 5V ± 10%

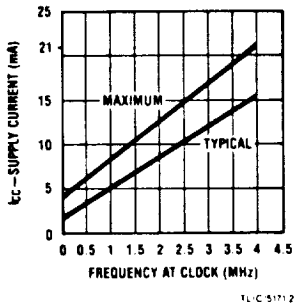
Ambient Temperature	
Military	− 55°C to + 125°C
Industrial	− 40°C to + 85°C
Commercial	0°C to + 70°C

DC Electrical Characteristics T_A = − 55°C to + 125°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{HY}	Hysteresis at RESET IN input	V_{CC} = 5V	0.25	0.5		V
V_{OH1}	Logical 1 Output Voltage	I_{OUT} = − 1.0 mA	2.4			V
V_{OH2}	Logical 1 Output Voltage	I_{OUT} = − 10 μA	V_{CC} − 0.5			V
V_{OL1}	Logical 0 Output Voltage	I_{OL} = 2 mA	0		0.4	V
V_{OL2}	Logical 0 Output Voltage	I_{OUT} = 10 μA	0		0.1	V
I_{IL}	Input Leakage Current	0 ≤ V_{IN} ≤ V_{CC}	− 10.0		10.0	μA
I_{OL}	Output Leakage Current	0 ≤ V_{IN} ≤ V_{CC}	− 10.0		10.0	μA
I_{CCA}	Active Supply Current	I_{OUT} = 0, $f_{(XIN)}$ = 5 MHz		10	15	mA
I_{CCA}	Active Supply Current	I_{OUT} = 0, $f_{(XIN)}$ = 8 MHz		15	21	mA
I_{CCQ}	Quiescent Current	$f_{(XIN)}$ = 0 MHz		2	4	mA
I_{CPS}	Power-Save Current	$f_{(XIN)}$ = 5.0 MHz		5		mA
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			8	12	pF
V_{CC}	Power Supply Voltage		2.4	5	6	V

Note 1: Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

I_{CC} vs System Speed



TL/C/5171-2

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, GND = 0V

NSC800-1 → $T_A = -40°C$ to $+85°C$
NSC800 → $T_A = -55°C$ to $+125°C$
NSC800-4 → $T_A = 0°C$ to $+70°C$

Symbol	Parameter	NSC800-1		NSC800		NSC800-4		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_X	Period at XIN and XOUT Pins	500	31250	200	31250	125	31250	ns	
T	Period at Clock Output ($= 2\,t_X$)	1000	62500	400	62500	250	62500	ns	
t_R	Clock Rise Time		110		110		75	ns	Measured from 10%-90% of signal
t_F	Clock Fall Time		60		60		40	ns	Measured from 10%-90% of signal
t_L	Clock Low Time	490		190		95		ns	50% duty cycle, square wave input on XIN
t_H	Clock High Time	450		150		80		ns	50% duty cycle, square wave input on XIN
$t_{ACC(RD)}$	ALE to Valid Data		1375		500		300	ns	Add t for each $\overline{WAIT}$ STATE Add t/2 for memory read cycles
t_{AFR}	AD(0-7) Float after $\overline{RD}$ Falling		0		0		0	ns	
t_{BABE}	$\overline{BACK}$ Rising to Bus Enable		1000		400		250	ns	
t_{BABF}	$\overline{BACK}$ Falling to Bus Float		50		50		50	ns	
t_{BACL}	$\overline{BACK}$ Falling to CLK Falling	425		125		55		ns	
t_{BRH}	$\overline{BREQ}$ Hold Time	0		0		0		ns	
t_{BRS}	$\overline{BREQ}$ Set-Up Time	100		50		35		ns	
t_{CAF}	Clock Falling to ALE Falling	0	30	0	30	0	35	ns	
t_{CAR}	Clock Rising to ALE Rising	0	100	0	100	0	75	ns	
t_{DAI}	ALE Falling to $\overline{INTA}$ Falling	530		230		100		ns	
t_{DAR}	ALE Falling to $\overline{RD}$ Falling	525	575	225	250	125	160	ns	
t_{DAW}	ALE Falling to $\overline{WR}$ Falling	990	1010	390	410	220	250	ns	
$t_{D(BACK)1}$	ALE Falling to $\overline{BACK}$ Falling	2500		1000		600		ns	Add t for each $\overline{WAIT}$ state Add t for opcode fetch cycles
$t_{D(BACK)2}$	$\overline{BREQ}$ Rising to $\overline{BACK}$ Rising	500	1600	200	700	125	475	ns	
$t_{D(I)}$	ALE Falling to $\overline{INTR}$, $\overline{NMI}$, $\overline{RSTA\text{-}C}$, $\overline{PS}$, $\overline{BREQ}$, Inputs Valid		1375		475		250	ns	Add t for each $\overline{WAIT}$ state Add t for opcode fetch cycles
t_{DPA}	Rising $\overline{PS}$ to Falling ALE	500	1550	200	650	125	475	ns	See *Figure 12* also
$t_{D(RFSH)}$	Falling ALE to Falling $\overline{RFSH}$	1500		600		325		ns	Add t for each $\overline{WAIT}$ state
$t_{D(WAIT)}$	ALE Falling to $\overline{WAIT}$ Input Valid		550		250		125	ns	

AC Electrical Characteristics (Continued) V_{CC} = 5V ± 10%, GND = 0V

NSC800-1 — T_A = −40°C to +85°C
NSC800 — T_A = −55°C to +125°C
NSC800-4 — T_A = 0°C to +70°C

Symbol	Parameter	NSC800-1		NSC800		NSC800-4		Units	Notes
		Min	Max	Min	Max	Min	Max		
$t_{H(ADH)1}$	A(8-15) Hold Time During Opcode Fetch	0		0		0		ns	
$t_{H(ADH)2}$	A(8-15) Hold Time During Memory or IO, $\overline{RD}$ and $\overline{WR}$	400		100		60		ns	
$t_{H(ADL)}$	AD(0-7) Hold Time	400		100		50		ns	
$t_{H(WD)}$	Write Data Hold Time	400		100		75		ns	
t_{INH}	Interrupt Hold Time	0		0		0		ns	
t_{INS}	Interrupt Set-Up Time	100		50		35		ns	
t_{NMI}	Width of NMI Input	50		30		20		ns	
t_{RDH}	Data Hold after Read	0		0		0		ns	
t_{RFL}	$\overline{RFSH}$ Rising to ALE Rising		−100		−100		−70	ns	Negative number means ALE occurs first
$t_{RL(MR)}$	$\overline{RD}$ Rising to ALE Rising (Memory Read)	450		150		85		ns	
$t_{RL(OP)}$	$\overline{RD}$ Rising to ALE Rising (Opcode)		−75		−65		−55	ns	Negative number means ALE occurs first
$t_{S(AD)}$	AD(0-7) Set-Up Time	300		80		40		ns	
$t_{S(ALE)}$	A(8-15), SO, SI, IO/$\overline{M}$ Set-Up Time	350		100		50		ns	
$t_{S(WD)}$	Write Data Set-Up Time	385		85		50		ns	
$t_{W(ALE)}$	ALE Width	430		130		75		ns	
t_{WH}	$\overline{WAIT}$ Hold Time	0		0		0		ns	
$t_{W(I)}$	Width of $\overline{INTR}$, $\overline{RSTA-C}$, $\overline{PS}$, $\overline{BREQ}$	500		200		125		ns	
$t_{W(INTA)}$	$\overline{INTA}$ Strobe Width	1000		400		200		ns	Add two t states for first $\overline{INTA}$ of each interrupt response string Add t for each $\overline{WAIT}$ state
t_{WL}	$\overline{WR}$ Rising to ALE Rising	450		150		90		ns	
$t_{W(RD)}$	Read Strobe Width During Opcode Fetch	1000		400		225		ns	Add t for each $\overline{WAIT}$ State Add t/2 for Memory Read Cycles
$t_{W(RFSH)}$	Refresh Strobe Width	1925		725		400		ns	
t_{WS}	$\overline{WAIT}$ Set-Up Time	100		50		35		ns	
$t_{W(WAIT)}$	$\overline{WAIT}$ Input Width	550		250		175		ns	
$t_{W(WR)}$	Write Strobe Width	1000		400		220		ns	Add t for each $\overline{WAIT}$ state
t_{XCF}	XIN to Clock Falling	25	55	25	55	25	55	ns	
t_{XCR}	XIN to Clock Rising	45	75	45	75	45	75	ns	

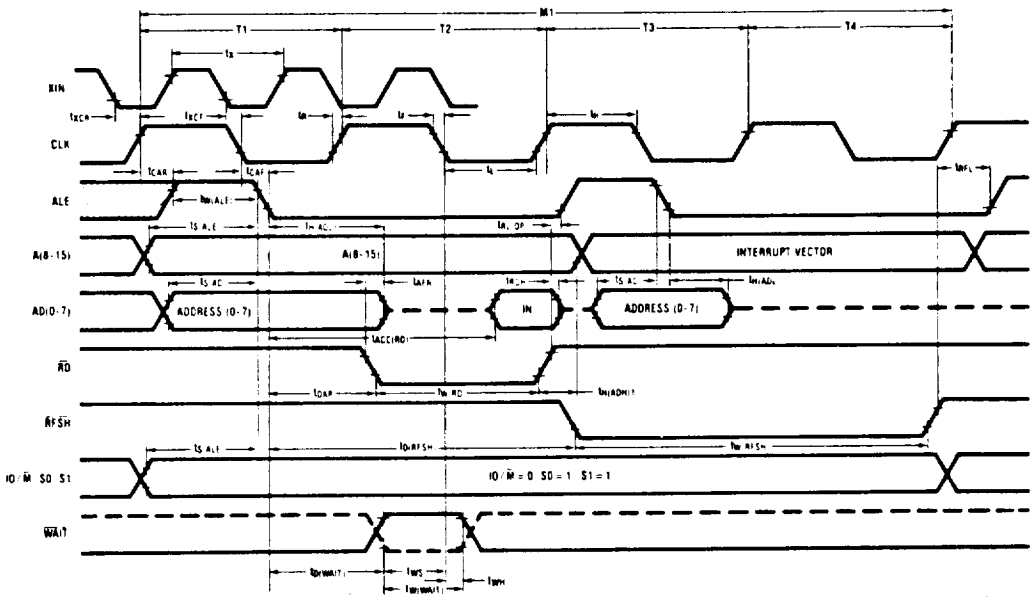
Note 1: Test conditions: t = 1000 ns for NSC800-1, 400 ns for NSC800, 250 ns for NSC800-4

Note 2: Output timings are measured with a purely capacitive load of 150 pF. The following correction factor can be used for other loads:
150 pF < C_L ≤ 300 pF: +0.25 ns/pF
50 pF ≤ C_L < 150 pF: −0.15 ns/pF

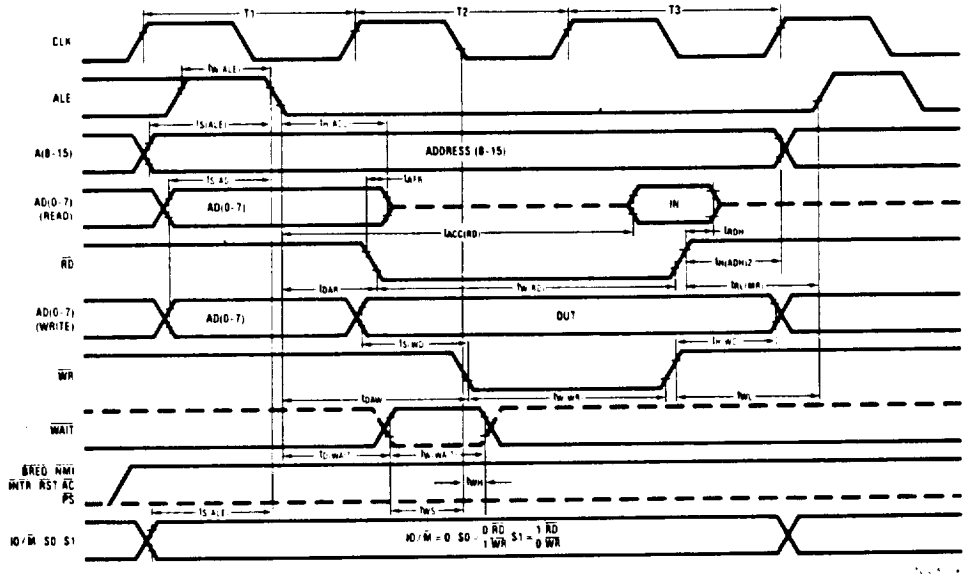
Note 3: To calculate timing specifications at other values of t use Table I.

Timing Waveforms

Opcode Fetch Cycle

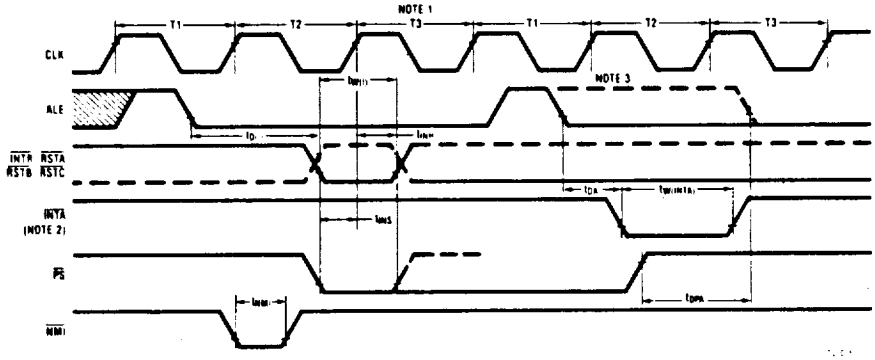


Memory Read and Write Cycle



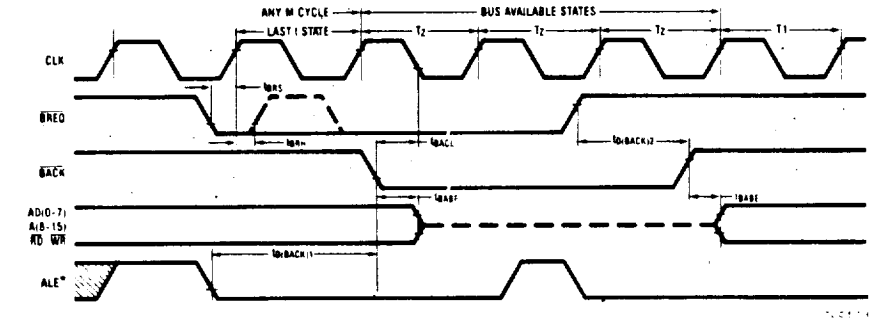
Timing Reference

Interrupt—Power-Save Cycle



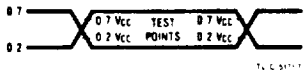
Note 1: This t state is the last t state of the last M cycle of any instruction.
Note 2: Response to INTR input.
Note 3: Response to PS input.

Bus Acknowledge Cycle



*Waveform not drawn to proportion. Use only for specifying test points.

AC Testing Input/Output Waveform



AC Testing Load Circuit

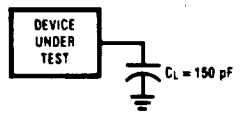


TABLE I. BUS TIMING AS t_X DEPENDENT

Symbol	$t_X < 2.5$ MHz	2.5 MHz $< t_X <$ 4.0 MHz		Symbol	$t_X < 2.5$ MHz	2.5 MHz $< t_X <$ 4.0 MHz	
t_L	(1/2)T − 10	(1/2)T − 30	Min	$t_{D(RFSH)}$	(3/2 + N)T	(3/2 + N)T − 50	Min
t_H	(1/2)T − 50	(1/2)T − 45	Min	$t_{D(WAIT)}$	(1/2)T + 50	(1/2)T	Max
$t_{ACC(RD)}$	(1 + N)T + 100	(1 + N)T + 50	Max	$t_{H(ADH)2}$	(1/2)T − 100	(1/2)T − 65	Min
t_{BABE}	T	T	Max	$t_{H(ADL)}$	(1/2)T − 100	(1/2)T − 75	Min
t_{BACL}	(1/2)T − 75	(1/2)T − 70	Min	$t_{H(WD)}$	(1/2)T − 100	(1/2)T − 50	Min
t_{DAI}	(1/2)T + 30	(1/2)T − 25	Min	$t_{RL(MR)}$	(1/2)T − 50	(1/2)T − 40	Min
t_{DAR}	(1/2)T + 25	(1/2)T	Min	$t_{S(AD)}$	(1/2)T − 120	(1/2)T − 85	Min
t_{DAR}	(1/2)T + 50	(1/2)T + 35	Max	$t_{S(ALE)}$	(1/2)T − 100	(1/2)T − 75	Min
t_{DAW}	T − 10	T − 30	Min	$t_{S(WD)}$	(1/2)T − 115	(1/2)T − 75	Min
t_{DAW}	T + 10	T	Max	$t_{W(ALE)}$	(1/2)T − 70	(1/2)T − 50	Min
$t_{D(BACK)1}$	(5/2 + N)T	(5/2 + N)T − 25	Min	$t_{W(INTA)}$	(1 + N)T	(1 + N)T − 50	Min
$t_{D(BACK)2}$	(1/2)T	(1/2)T	Min	t_{WL}	(1/2)T − 50	(1/2)T − 35	Min
$t_{D(BACK)2}$	(3/2)T + 100	(3/2)T + 100	Max	$t_{W(RD)}$	(1 + N)T	(1 + N)T − 25	Min
t_{DI}	(3/2 + N)T − 125	(3/2 + N)T − 125	Max	$t_{W(RFSH)}$	2T − 75	2T − 100	Min
t_{DPA}	(1/2)T	(1/2)T	Min	$t_{W(WR)}$	(1 + N)T	(1 + N)T − 30	Min
t_{DPA}	(3/2)T + 50	(3/2)T + 100	Max				

Note N is equal to number of WAIT states

Functional Pin Descriptions

The following describes the function of all NSC800 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Reset Input ($\overline{\text{RESET IN}}$): Active low. Sets A (8-15) and AD (0-7) to TRI-STATE[1] (high impedance). Clears the contents of PC, I and R registers, disables interrupts, and causes a reset output to be activated.

Bus Request ($\overline{\text{BREQ}}$): Active low. Used when another device is requesting the system bus. $\overline{\text{BREQ}}$ is recognized at the end of the current machine cycle, then A(8-15), AD(0-7), IO/$\overline{\text{M}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ are set to the high impedance mode and the request is acknowledged via the $\overline{\text{BACK}}$ output signal.

Non-Maskable Interrupt ($\overline{\text{NMI}}$): Active low. The non-maskable interrupt, generated by the peripheral device(s), is the highest priority interrupt request line. The interrupt is edge sensitive and only a pulse is required to set an internal flip-flop which generates the internal interrupt request. Since the $\overline{\text{NMI}}$ flip-flop is monitored on the same clock edge as the other interrupts, it must also meet the minimum set-up time spec for the interrupt to be accepted in the current machine instruction. Once the interrupt is accepted the flip-flop is reset automatically. Its execution is independent of the interrupt enable flip-flop. $\overline{\text{NMI}}$ execution involves saving the PC on the stack and automatic branching to restart address X'0066 in memory.

Restart Interrupts A, B, C ($\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, $\overline{\text{RSTC}}$): Active low level sensitive. Restarts generated by the peripherals are recognized at the end of the current instruction if their respective interrupt enable bits and master enable bit are set. Execution is identical to $\overline{\text{NMI}}$ except interrupts are enabled for the following restart addresses:

Name	Restart Address (X')
$\overline{\text{NMI}}$	0066
$\overline{\text{RSTA}}$	003C
$\overline{\text{RSTB}}$	0034
$\overline{\text{RSTC}}$	002C
$\overline{\text{INTR}}$ (Mode 1)	0038

The order of priority is fixed (highest first) as follows:

1) $\overline{\text{NMI}}$ 2) $\overline{\text{RSTA}}$ 3) $\overline{\text{RSTB}}$ 4) $\overline{\text{RSTC}}$ 5) $\overline{\text{INTR}}$

Interrupt Request ($\overline{\text{INTR}}$): Active low level sensitive. An interrupt request input generated by a peripheral device is recognized at the end of the current instruction provided that the interrupt enable and master interrupt enable bits are set. $\overline{\text{INTR}}$ is the lowest priority interrupt request input. Under program control, $\overline{\text{INTR}}$ can be executed in three distinct modes in conjunction with the $\overline{\text{INTA}}$ output.

Wait ($\overline{\text{WAIT}}$): Active low. When set low during $\overline{\text{RD}}$, $\overline{\text{WR}}$ or $\overline{\text{INTA}}$, the CPU extends its machine cycle in increments of t (wait) states. The wait machine cycle continues until the $\overline{\text{WAIT}}$ input returns high.

The wait strobe input will be accepted only during machine cycles that have $\overline{\text{RD}}$, $\overline{\text{WR}}$ or $\overline{\text{INTA}}$ strobes and during the machine cycle immediately after an interrupt has been accepted by the CPU. The later cycle has its RD strobe suppressed but it will still accept the wait.

Power-Save ($\overline{\text{PS}}$): Active low. $\overline{\text{PS}}$ is sampled at the end of the current instruction cycle. When $\overline{\text{PS}}$ is low, the CPU stops executing at the end of current instruction and keeps itself in the low-power mode. Normal operation resumes when $\overline{\text{PS}}$ is returned high.

Functional Pin Descriptions (Continued)

OUTPUT SIGNALS

Bus Acknowledge ($\overline{BACK}$): Active low. $\overline{BACK}$ indicates to the bus requesting device that the CPU bus and its control signals are in the TRI-STATE mode. The requesting device may then take control of the bus and its control signals.

Address Bits 8-15 [A(8-15)]: Active high. These are the most significant 8 bits of the memory address during a memory instruction. During an I/O instruction, the port address on the lower 8 bits of address get duplicated onto these 8 bits. During a BREQ/BACK cycle, the A (8-15) bus is in the TRI-STATE mode.

Reset Out (RESET OUT): Active high. When RESET OUT is high, it indicates the CPU is being reset. The signal is normally used to reset the peripheral devices.

Input/Output/Memory (IO/$\overline{M}$): An active high on the IO/$\overline{M}$ output signifies that the current machine cycle is relative to an input/output device. An active low on the IO/$\overline{M}$ output signifies that the current machine cycle is relative to memory. It is TRI-STATE during $\overline{BREQ}$/$\overline{BACK}$ cycles.

Refresh ($\overline{RFSH}$): Active low. The refresh output indicates that the dynamic RAM refresh cycle is in progress. $\overline{RFSH}$ goes low during T3 and T4 states of all M1 cycles. During the refresh cycle, AD(0-7) has the refresh address and A(8-15) indicates the interrupt vector register I.

Address Latch Enable (ALE): ALE is active only during the T1 state of any M cycle and also T3 state of M1 cycle. The high to low transition of ALE indicates that a valid memory/I-O/refresh address is available on the AD(0-7) lines.

Read Strobe ($\overline{RD}$): Active low. On the trailing edge of the $\overline{RD}$ strobe, data is input to the CPU via the AD(0-7) lines. The $\overline{RD}$ line is in the TRI-STATE mode during $\overline{BREQ}$/$\overline{BACK}$ cycles.

Write Strobe ($\overline{WR}$): While the $\overline{WR}$ line is low, valid data is output by the CPU on the AD(0-7) lines. The $\overline{WR}$ line is in the TRI-STATE mode during $\overline{BREQ}$/$\overline{BACK}$ cycles.

Clock (CLK): CLK is an output provided for use as a system clock. The CLK output is a square wave at one half the input frequency.

Interrupt Acknowledge ($\overline{INTA}$): Active low. The interrupt acknowledge output is activated in the M1 cycle (S) immediately following the t state in which the $\overline{INTR}$ input is recognized. [Output is normally used to gate the interrupt response vector from the peripheral controller onto the AD(0-7) lines.] It is used in two of the three interrupt modes. In mode 0, an instruction is gated onto the AD(0-7) line during $\overline{INTA}$. There will be from 1 to 4 $\overline{INTA}$ strobes issued for each mode 0 interrupt. The amount of $\overline{INTA}$ strobes issued is instruction dependent. In mode 2, a single interrupt response vector is gated onto the data bus. In mode 1, $\overline{INTA}$ is not used. In this mode, $\overline{INTR}$ functions like the restart interrupts.

Status (S0, S1): Bus status outputs indicate encoded information regarding the ensuing M cycle as follows:

Machine Cycle	Status			Control	
	S0	S1	IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$
Opcode Fetch	1	1	0	0	1
Memory Read	0	1	0	0	1
Memory Write	1	0	0	1	0
I/O Read	0	1	1	0	1
I/O Write	1	0	1	1	0
Halt*	0	0	0	0	1
Internal Operation*	0	1	0	1	1
Acknowledge of Int**	1	1	0	1	1

* ALE is not suppressed in this cycle.

** This is the cycle that occurs immediately after the CPU accepts an interrupt ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, $\overline{INTR}$, $\overline{NMI}$).

Note 1: During halt, CPU continues to do dummy opcode fetch from location following the halt instruction with a halt status. This is so CPU can continue to do its dynamic RAM refresh.

Note 2: No early status is provided for interrupt or hardware restarts.

INPUT/OUTPUT SIGNALS

Power (V_{CC}): +5V supply.

Ground (GND): 0V reference.

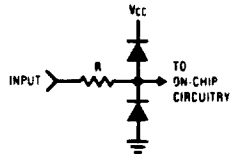
Crystal (XIN, XOUT): XIN may be used as an external clock input.

Multiplexed Address/Data [AD(0-7)]: Active high

At $\overline{RD}$ Time:	Input data to CPU.
At $\overline{WR}$ Time:	Output data from CPU.
At Falling Edge of ALE Time:	Least significant byte of address during memory reference cycle. 8-bit port address during I/O reference cycle.
During $\overline{BREQ}$/$\overline{BACK}$ Cycle:	High impedance.

Input Protection

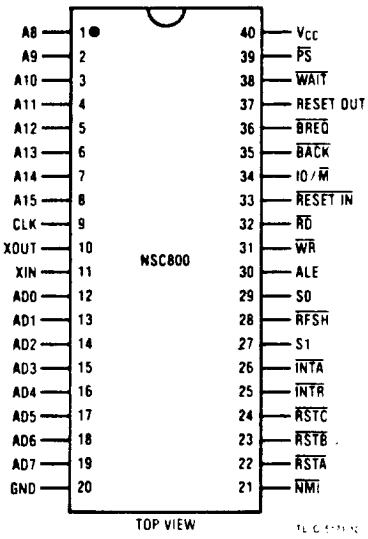
All inputs are protected from static charge with diode clamps to both V_{CC} and GND. Normal precautions taken with MOS devices are recommended.



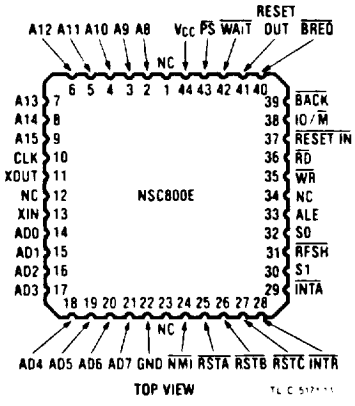
$100\Omega < R < 300\Omega$

Connection Diagrams

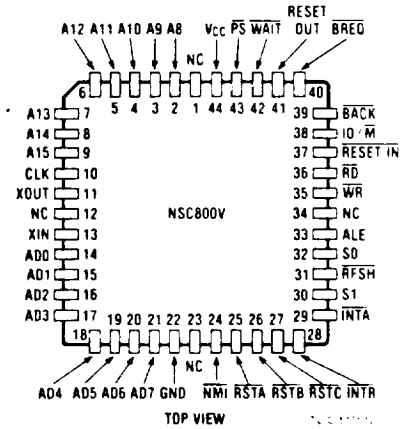
Dual-In-Line Package



E Package



V Package



Timing Control

All necessary timing signals are provided by a single state inverter oscillator contained on the NSC800 chip. The chip operation frequency is equal to one half of the frequency of this oscillator. The oscillator frequency can be controlled by one of the following methods:

1. Leaving the XOUT pin unterminated and driving the XIN pin with an externally generated clock as shown in *Figure 1a*. When driving XIN with a square wave, the minimum duty cycle is 30%-70%, either high or low.
2. Connecting a crystal with the proper biasing network between XIN and XOUT as shown in *Figure 1b*. Recommended crystal is a parallel resonance AT cut crystal.

Resistor capacitor feedback network described in earlier data sheets will not oscillate due to gain of internal inverter circuit. A modification of this circuit by adding two inverters in series between the RC network and XIN will work.

The CPU has a minimum clock frequency input (@ XIN) of 32 kHz, which results in 16 kHz system clock speed. All registers internal to the chip are static, however there is dynamic logic which limits the minimum clock speed. The Input clock can be stopped without fear of losing any data or damaging the part. You stop it in the phase of the clock that has XIN low and CLK OUT high. When restarting the CPU, precautions must be taken so that the input clock meets minimum specification. Once started, the CPU will continue operation from the same location at which it was stopped. During DC operation of the CPU, typical current drain will be 2 mA. This current drain can be reduced by placing the CPU in a wait state during an opcode fetch cycle then stopping the clock.

Functional Description

The NSC800 is an 8-bit general purpose microprocessor designed for stand-alone and DMA (direct memory access) applications. A minimum system can be constructed with an NSC800, an NSC810 (RAM I/O Timer) and an NMC27C16 (EPROM).

NSC800 uses a multiplexed bus for data and addresses. The 16-bit address bus is divided into a high-order 8-bit address bus that handles bits 8-15 of the address, and a low-order 8-bit multiplexed address/data bus that handles bits 0-7 of the address and bits 0-7 of the data. Strobe outputs from the NSC800 (ALE, $\overline{RD}$ and $\overline{WR}$) indicate when a valid address or data is present on the bus. IO/$\overline{M}$ indicates whether the ensuing cycle accesses memory or I/O.

During an input or output instruction, the CPU duplicates the lower half of the address [AD(0-7)] onto the upper half [A(8-15)]. The eight bits of address will stay on A(8-15) for the entire machine cycle.

Figure 2 illustrates the timing relationship for opcode fetch cycles with and without a wait state. *Figure 3* illustrates the timing relationship for memory read and write cycles with and without a wait state. Input/output cycles with and without a wait state are shown in *Figure 4*. One wait state is automatically inserted into each I/O instruction.

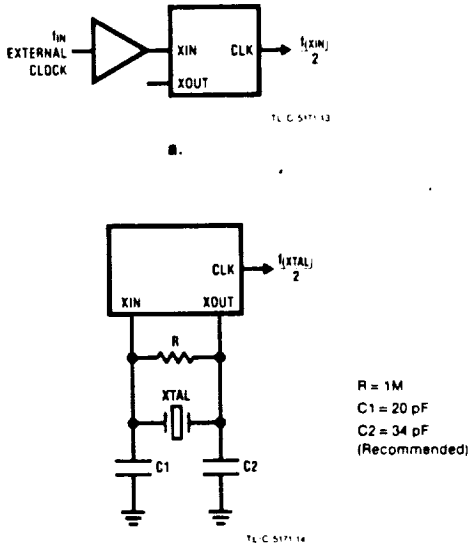


FIGURE 1. Timing Control Configurations

Functional Description (Continued)

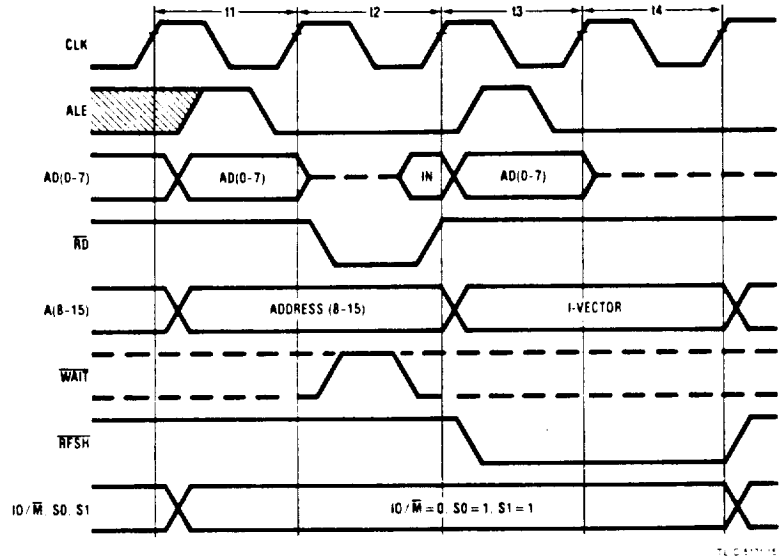


FIGURE 2a. Opcode Fetch Cycles without $\overline{\text{WAIT}}$ States

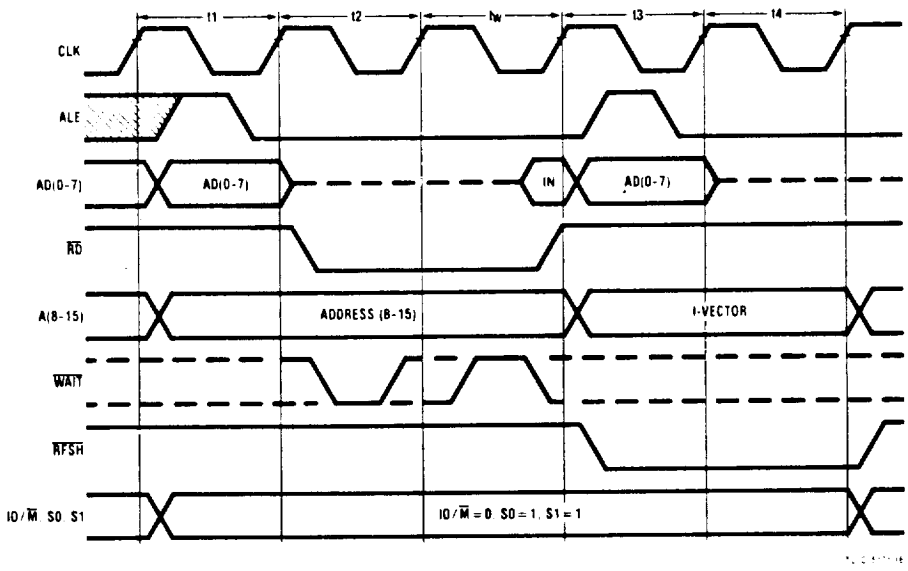


FIGURE 2b. Opcode Fetch Cycles with $\overline{\text{WAIT}}$ States

Functional Description (Continued)

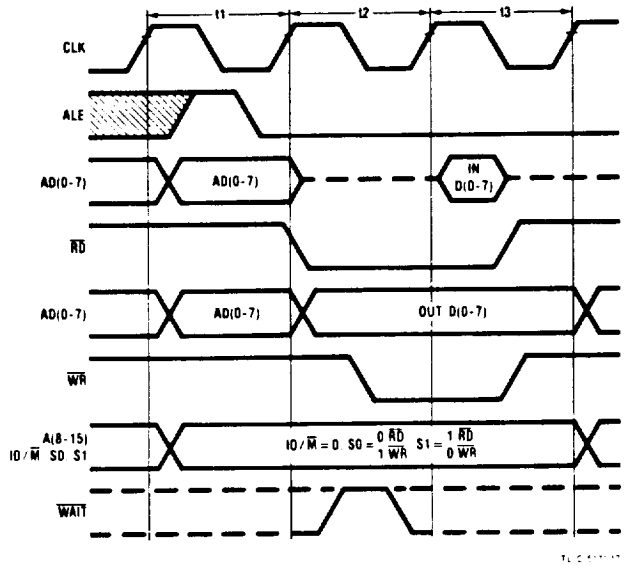


FIGURE 3a. Memory Read/Write Cycles without $\overline{\text{WAIT}}$ States

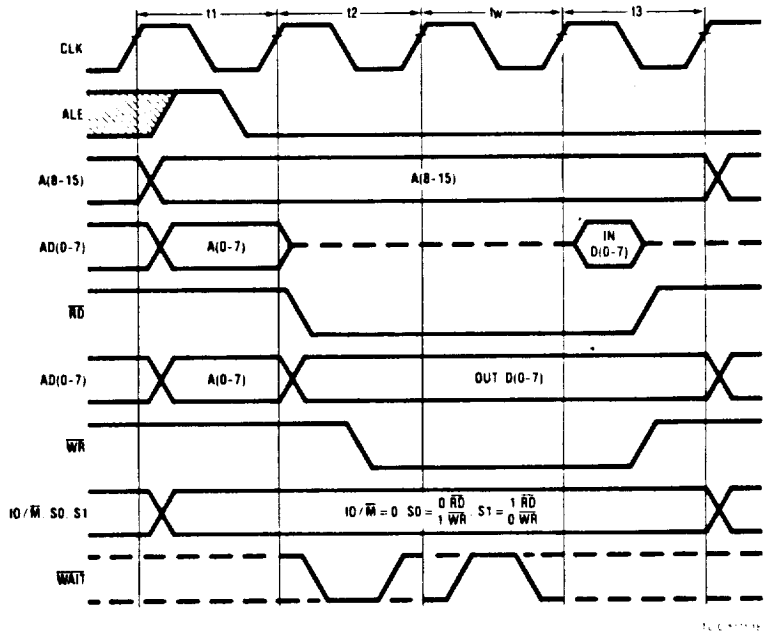


FIGURE 3b. Memory Read and Write with $\overline{\text{WAIT}}$ States

Functional Description (Continued)

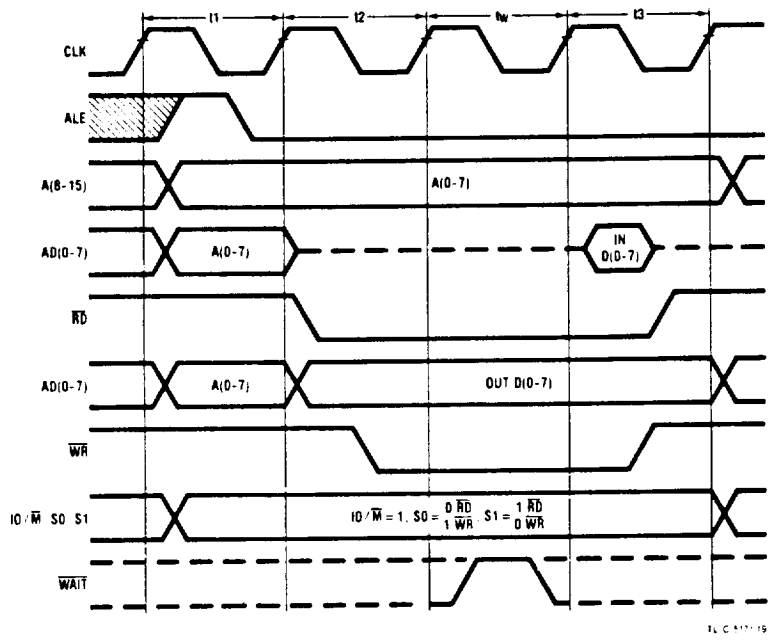
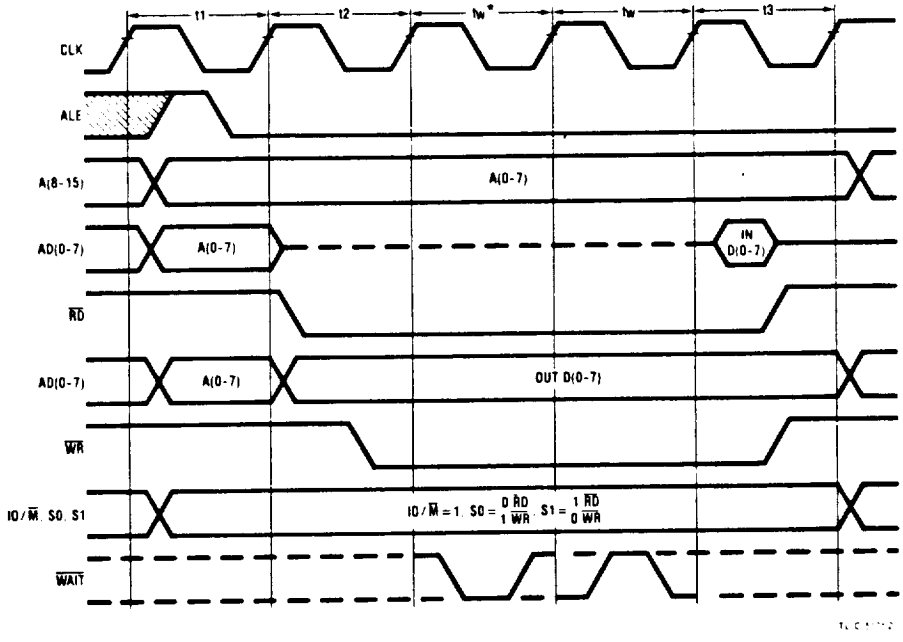


FIGURE 4a. Input and Output Cycles without $\overline{\text{WAIT}}$ States



* $\overline{\text{WAIT}}$ state automatically inserted during IO operation.

FIGURE 4b. Input and Output Cycles with $\overline{\text{WAIT}}$ States

Functional Description (Continued)

INITIALIZATION

The NSC800 and its peripheral components are initialized by $\overline{\text{RESET IN}}$ and RESET OUT. $\overline{\text{RESET IN}}$ input is associated with an on-chip Schmitt trigger that facilitates using an R-C network power-on reset scheme (*Figure 5*).

To ensure proper power-up conditions for the NSC800, the following power-up and initialization procedure is recommended:

1. Apply power (V_{CC} and GND) and set $\overline{\text{RESET IN}}$ active (low). Allow sufficient time (approximately 100 ms if crystal used) for the oscillator and internal clocks to stabilize. $\overline{\text{RESET IN}}$ must remain low for at least 3t state (CLK) times. RESET OUT, following the clock stabilization period, responds by going high, indicating to the system that the NSC800 is being reset. RESET OUT signal becomes available to reset the peripherals.
2. Set $\overline{\text{RESET IN}}$ high, following which the RESET OUT goes low and the CPU initiates the first opcode fetch cycle.

NOTE: *The NSC800 initialization includes: Clear PC to X'0000 (the first opcode fetch, therefore, is from memory location X'0000). Clear registers I (Interrupt Vector Base) and R (Refresh Counter) to X'00. Clear interrupt control register bits IEA, IEB and IEC. The interrupt control bit IEI is set to 1 to maintain INS8080A/Z80A compatibility (see INTERRUPTS for more details). Maskable interrupts are disabled and the CPU enters Interrupt Mode 0. While $\overline{\text{RESET IN}}$ is active (low), the A(8-15) and AD(0-7) lines go to high impedance (TRI-STATE) and all CPU strobes go to the inactive state.*

BUS ACCESS CONTROL

Figure 6 illustrates bus access control in the NSC800. The external device controller produces an active $\overline{\text{BREQ}}$ signal that requests the bus. When the CPU responds with $\overline{\text{BACK}}$ then the bus and related control strobes go to high impedance (TRI-STATE). It should be noted that (1) $\overline{\text{BREQ}}$ is sampled at the last t state of any M machine cycle only. (2) The NSC800 will not acknowledge any interrupt/restart requests, and will not perform any dynamic RAM refresh functions until after $\overline{\text{BREQ}}$ input signal is inactive high. (3) $\overline{\text{BREQ}}$ signal has priority over all interrupt request signals, should $\overline{\text{BREQ}}$ and interrupt request become active simultaneously.

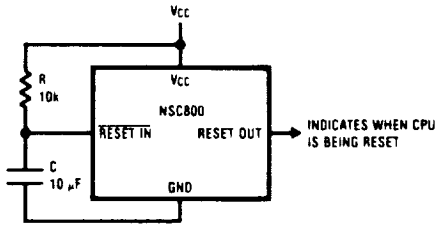
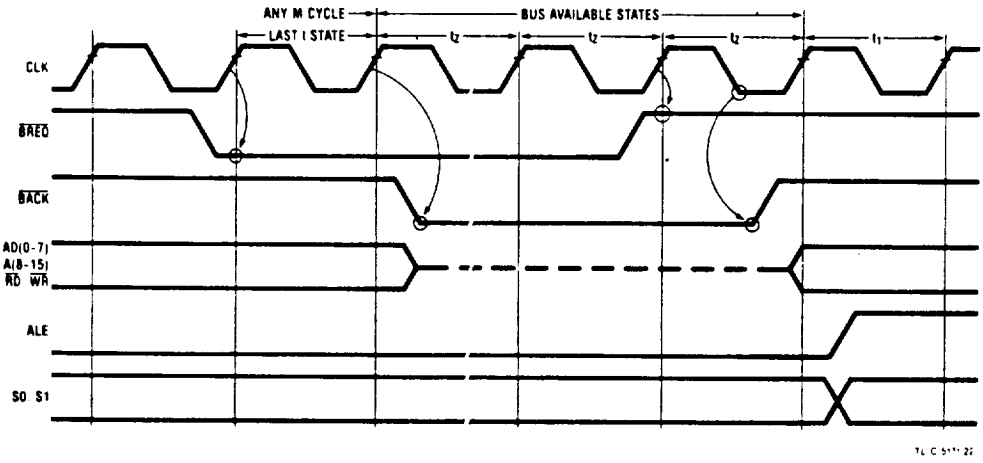


FIGURE 5. Power-On Reset



*S0, S1 during $\overline{\text{BREQ}}$ will indicate same machine cycle as during cycle when $\overline{\text{BREQ}}$ was accepted
tz = time states bus and control signals are in high impedance mode.

FIGURE 6. Bus Acknowledge Cycle

Functional Description (Continued)

REGISTER CONFIGURATION

The NSC800 contains 22 programmable registers as shown in *Figure 7*. The CPU working registers are arranged in two 8-register configurations, each of which includes an 8-bit accumulator, a flag register, and six general purpose 8-bit registers. Only one 8-bit register set may be active at any given moment. However, simple instructions exist that allow the programmer to exchange the active and alternate register sets.

It should also be noted that the six 8-bit general purpose registers (B, C, D, E, H, and L) can be accessed as 16-bit registers (BC, DE, and HL). The functions of these become apparent in the instruction set description.

CPU Main Working Register Set

Accumulator	(8)	Flags F	(8)
Register B	(8)	Register C	(8)
Register D	(8)	Register E	(8)
Register H	(8)	Register L	(8)

CPU Alternate Working Register Set

Accumulator A'	(8)	Flags F'	(8)
Register B'	(8)	Register C'	(8)
Register D'	(8)	Register E'	(8)
Register H'	(8)	Register L'	(8)

CPU Dedicated Registers

Index Register IX	(16)
Index Register IY	(16)
Interrupt Vector Register I	(8)
Memory Refresh Register R	(8)
Stack Pointer SP	(16)
Program Counter PC	(16)

FIGURE 7. Register Configuration

DEDICATED REGISTERS

Program Counter (PC): The program counter contains the 16-bit address of the current instruction being fetched from memory. The PC is incremented after its contents have been transferred to the address lines. When a program jump occurs, the new address is placed in the PC, overriding the incrementer.

Stack Pointer (SP): The stack pointer contains the 16-bit address of the current top of a stack located in external system RAM memory. The external stack memory is organized as a last-in, first-out (LIFO) file. The stack allows simple implementation of multiple level interrupts, virtually unlimited subroutine nesting and simplification of many types of data manipulation.

Index Registers (IX and IY): The two 16-bit index registers hold a 16-bit base address used in indexed addressing modes. In this mode, an index register is used as a base to point to a region in memory from which data is to be stored or retrieved. An additional byte is included in indexed instructions to specify a displacement from this base. This displacement is specified as a two's complement signed integer.

Interrupt Page Address Register (I): The NSC800 CPU can indirectly call any memory location in response to a mode 2 interrupt. The I register is used to store the high-order 8 bits of the address. The low-order 8 bits are supplied by the interrupting peripheral. This feature allows interrupt routines to be dynamically located anywhere in memory with minimal access time to the routine.

Memory Refresh Register (R): The NSC800 CPU contains a memory refresh counter to enable dynamic memories to be used with the same ease as static memories. This 8-bit register is automatically incremented after each instruction fetch. The data in the refresh counter is sent out on the lower portion of the address bus along with a refresh control signal while the CPU is decoding and executing the fetched instruction. This mode of refresh is totally transparent to the programmer and does not slow down CPU operation. The programmer can load the R register for testing purposes, but this register is normally not used by the programmer.

ACCUMULATORS AND FLAG REGISTERS

The CPU includes two 8-bit accumulators and two associated 8-bit flag registers. The accumulator holds the results of 8-bit arithmetic or logical operation. The flag register indicates specific conditions for 8-bit or 16-bit operations.

FLAG REGISTERS (F,F')

The two NSC800 flag registers each contain six status bits that are set or reset (cleared) by various CPU operations (*Figure 8*). Four of these bits (carry, zero, sign, and parity/overflow flags) can be tested by the programmer. The descriptions of the flags follow.

Carry Flag (C): This flag is set by the carry from the highest order bit of the accumulator during an add instruction or a borrow generated during a subtraction instruction. Specific shift and rotate instructions also affect this bit.

Zero Flag (Z): This flag is set when a zero is loaded into the accumulator as a result of an operation. Otherwise it remains clear.

Sign Flag (S): This flag stores the state of bit 7 (the sign bit) in the accumulator after an arithmetic operation. This flag is intended to be used with signed numbers.

Parity/Overflow Flag (P/V): During logical operations this flag is set when the parity of the result is even and reset when it is odd. It represents overflow when signed two's complement arithmetic operations are performed. An overflow occurs when the resultant of a two's complement operation (in the accumulator) is out of range.

The two non-testable flag register bits used for BCD arithmetic are:

Half Carry (H): This flag indicates a BCD carry or borrow result from the least significant four bits of an operation; when using the DAA (Decimal Adjust Accumulator Instruction), it is used to correct the result of a previously packed decimal add or subtract.

Functional Description (Continued)

Add/Subtract Flag (N): Since the algorithm for correcting BCD operations is different for addition or subtraction, this flag specifies what type of instruction was executed last in order that the DAA operation will be correct for either operation.

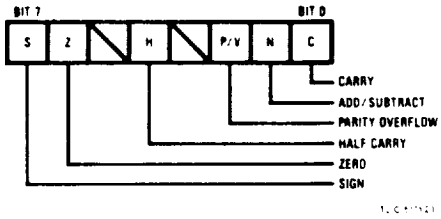


FIGURE 8. Flag Register

INTERRUPTS

The NSC800 has five interrupt/restart inputs, four are maskable ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, and $\overline{INTR}$) and one is non-maskable ($\overline{NMI}$). $\overline{NMI}$, having the highest priority of all interrupts, is always serviced and cannot be disabled by the user. After recognizing an active input on $\overline{NMI}$, the CPU stops before the next instruction, pushes the PC onto the stack, and jumps to address X'0066, where the user's interrupt service routine is located (i.e., restart to memory location X'0066). $\overline{NMI}$ is intended for interrupts requiring immediate attention, such as power-down, control panel, etc.

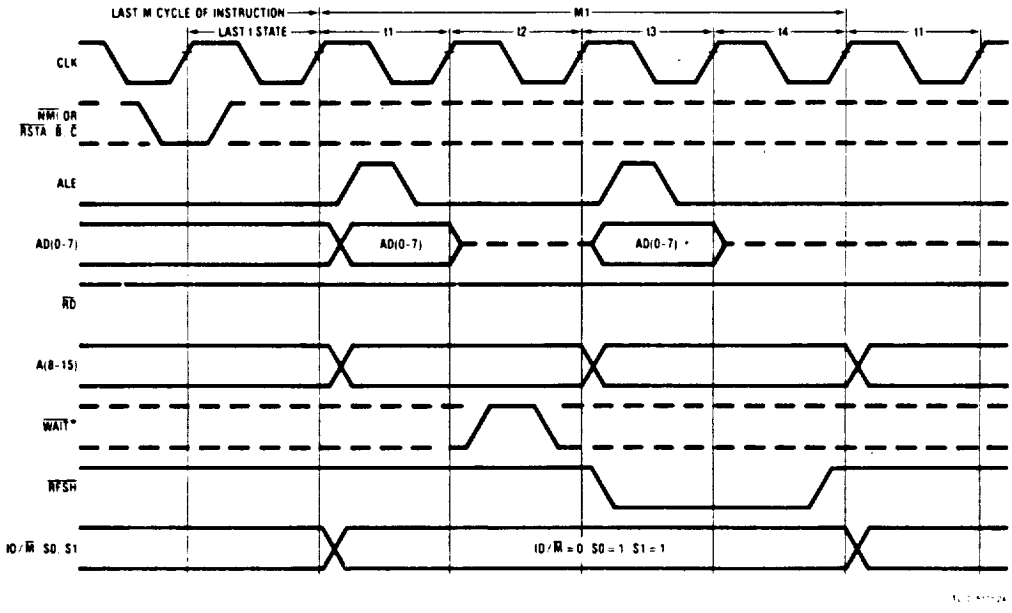
$\overline{RSTA}$, $\overline{RSTB}$ and $\overline{RSTC}$ are restart inputs, which, if enabled, execute a restart to memory location X'003C, X'0034, and X'002C, respectively. Note that the CPU response to the $\overline{NMI}$ and $\overline{RST}$ ($\overline{A}$, $\overline{B}$, $\overline{C}$) request input is basically identical. Unlike $\overline{NMI}$, however, restart request inputs must be enabled.

Figure 9 illustrates $\overline{NMI}$ and $\overline{RST}$ interrupt machine cycles. M1 cycle will be a dummy opcode fetch cycle followed by M2 and M3 which are stack push operations. The following instruction will then start from the interrupts restart location.

The NSC800 also provides one more general purpose interrupt request input, $\overline{INTR}$. When enabled, the CPU responds to $\overline{INTR}$ in one of the three modes defined by instruction IM0, IM1, and IM2 for modes 0, 1, and 2, respectively. Following reset, the CPU automatically sets itself in mode 0.

Interrupt ($\overline{INTR}$) Mode 0: Similar to INS8080A mode. The CPU responds to an interrupt request by providing an INTA (interrupt acknowledge) strobe, which can be used to gate an instruction from a peripheral onto the data bus. Two wait states are automatically inserted by the CPU during the first $\overline{INTA}$ cycle to allow the interrupting device (or its controller) ample time to gate the instruction and determine external priorities. (*Figure 10*). This can be any instruction from one to four bytes. The most popular instruction would be a one-byte call (restart instruction) or a three-byte call (CALL NN instruction). If it is a three-byte call, the CPU issues a total of three $\overline{INTA}$ strobes. The last two read NN (which do not include wait states).

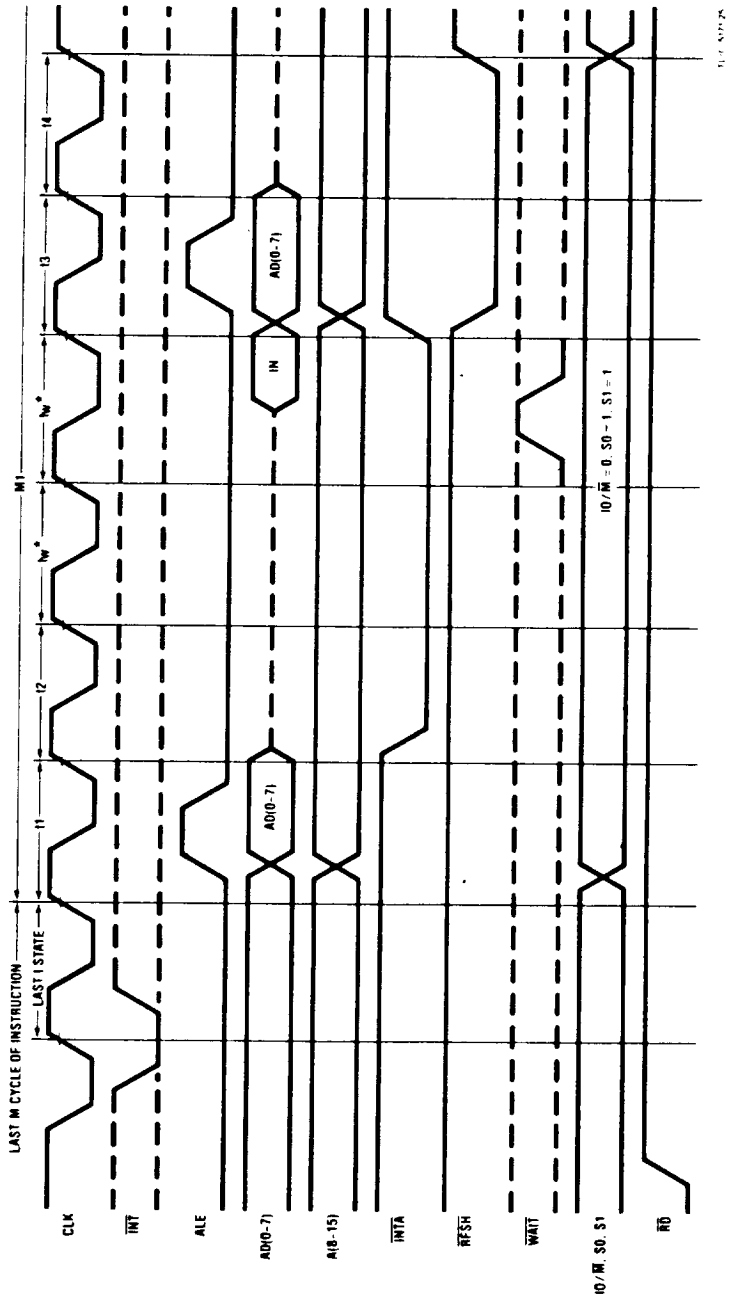
Interrupt ($\overline{INTR}$) Mode 1: Similar to the restart interrupts except the restart location is X'0038 (*Figure 9*).



* This is the only machine cycle that does not have an $\overline{RD}$, $\overline{WR}$, or $\overline{INTA}$ strobe but will accept a wait strobe

FIGURE 9. Non-Maskable and Restart Interrupt Machine Cycle

Timing Waveforms (Continued)



*Tw is the CPU generated WAIT state in response to an interrupt request

FIGURE 10. Interrupt Acknowledge Machine Cycle

Functional Description (Continued)

Interrupt ($\overline{INTR}$) Mode 2: With this mode, the programmer maintains a table that contains the 16-bit starting address of every interrupt service routine. This table may be located anywhere in memory. When the mode 2 interrupt is accepted (*Figure 11*), a 16-bit pointer must be formed to obtain the desired interrupt service routine starting address from the table. The upper 8 bits of this pointer are from the contents of the I register, which has been previously loaded with the desired value by the programmer. The lower 8 bits of the pointer are supplied by the interrupting device with the low-order bit forced to zero. The pointer is used to get two adjacent bytes from the interrupt service routine starting address table to complete 16-bit service routine starting address. The first byte of each entry in the table is the least significant (low-order) portion of the address. The programmer must obviously fill this table with the desired addresses before any interrupts are to be accepted.

Note that this table can be changed at any time to allow peripherals to be serviced by different service routines. Once the interrupting device supplies the lower portion of the pointer, the CPU automatically pushes the program counter onto the stack, obtains the starting address from the table and does a jump to this address.

The interrupts have fixed priorities built into the NSC800 as:

$\overline{NMI}$	(Highest Priority)
$\overline{RSTA}$	
$\overline{RSTB}$	
$\overline{RSTC}$	
$\overline{INTR}$	(Lowest Priority)

ENABLING INTERRUPTS

$\overline{NMI}$, being a non-maskable interrupt request, is executed as it occurs and can never be disabled.

The maskable interrupt inputs ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, and $\overline{INTR}$) are enabled under program control through the use of the interrupt control register and enable/disable interrupt instruction.

The appropriate interrupt control bits in 4-bit interrupt control register (IEA, IEB, IEC, and IEI) must be enabled in conjunction with IFF1 and IFF2, before the maskable $\overline{INTR}$ and $\overline{RST}$ A, B, C can be accepted by the CPU.

The interrupt control register is an on-chip write only output port located at port address X'BB. It can only be written to by either the OUT (C), r or OUT (N), A instructions (for example OUTI instruction will not affect Interrupt Control Register). Its contents are:

Bit	Name	Function
0	IEI	Interrupt Enable for $\overline{INTR}$
1	IEC	" " " $\overline{RSTC}$
2	IEB	" " " $\overline{RSTB}$
3	IEA	" " " $\overline{RSTA}$

For example: In order to enable $\overline{RSTB}$, CPU interrupts must be enabled and IEB must be set.

At reset, IEI bit is set and other mask bits, IEA, IEB, IEC are cleared. This maintains the software compatibility between NSC800 and INS8080A (or Z80A).

Execution of an IO block move instruction will not affect the state of the interrupt control bits. The only two instructions that will modify this write only register are OUT (C), r and OUT (N), A.

POWER-SAVE FEATURE

The NSC800 provides a unique power-save mode by the means of the $\overline{PS}$ pin. $\overline{PS}$ input is sampled at the last t state of the last M cycle of an instruction. After recognizing an active (low) level on $\overline{PS}$, the NSC800 stops its internal clocks, thereby reducing its power dissipation to one half of operating power, yet maintaining all register values and internal control status. The NSC800 keeps its oscillator running, and makes the CLK signal available to the system. When in power-save the ALE strobe will be stopped high and the address lines [AD(0-7), A(8-15)] will indicate the next machine address. When $\overline{PS}$ is returned high, the opcode fetch (or M1 cycle) of the CPU begins in a normal manner. Note this M1 cycle could also be an interrupt acknowledge cycle if the NSC800 was interrupted simultaneously with $\overline{PS}$. *Figure 12* illustrates the power-save feature.

In the event $\overline{BREQ}$ is asserted (low) at the end of an instruction cycle and $\overline{PS}$ is active simultaneously, the following occurs:

1. The NSC800 will go into $\overline{BACK}$ cycle
2. Upon completion of $\overline{BACK}$ cycle if $\overline{PS}$ is still active the CPU will go into power-save mode.

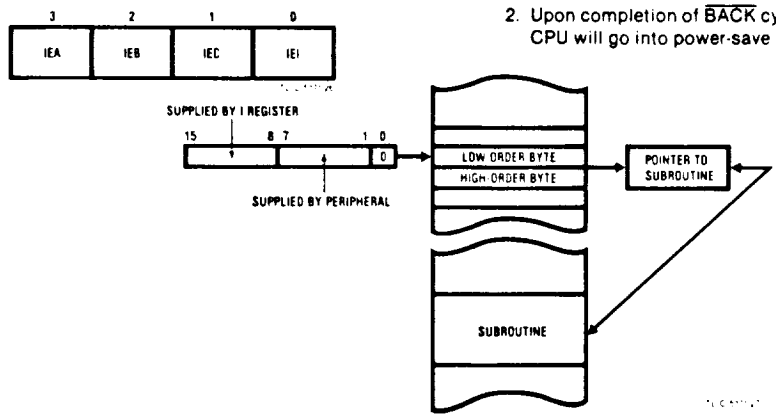


FIGURE 11. Interrupt Mode 2

Timing Waveforms (Continued)

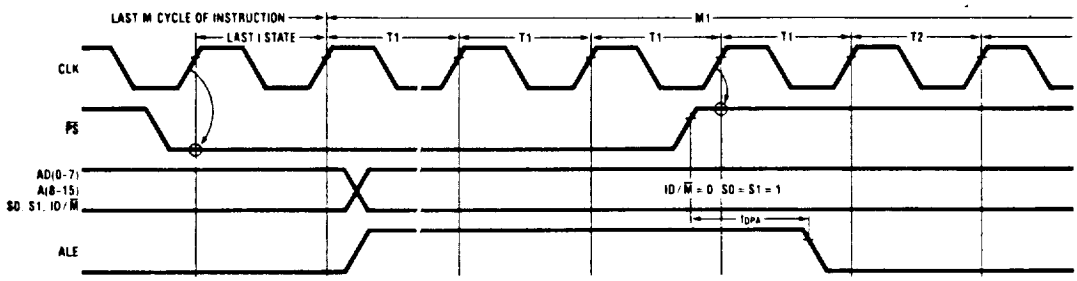


FIGURE 12. NSC800 Power-Save

Instruction Set

In the following instruction set listing, the notation used is shown below.

b: Used in instructions employing bit mode addressing to designate one bit in a register or memory location.

cc: Designates condition codes used in conditional Jumps, Calls, and Return instructions; may be

NZ = Non Zero (Z Flag = 0)
Z = Zero (Z Flag = 1)
NC = Non Carry (C Flag = 0)
C = Carry (C Flag = 1)

PO = Parity Odd or No Overflow (P/V = 0)
PE = Parity Even or Overflow (P/V = 1)
P = Positive (S = 0)
M = Negative (S = 1)

d: Used in instructions employing relative or indexed modes of addressing to designate 8-bit signed 2's complement displacement.

kk: Subset of cc condition codes used in conjunction with conditional relative jumps; may be NZ, Z, NC or C.

m1: Used in instructions employing register indirect or indexed modes of addressing; may be (HL), (IX + d), or (IY + d).

m2: Used in instructions employing register indirect or direct modes of addressing; may be (BC), (DE), or (nn).

n: Any 8-bit binary number.

nn: Any 16-bit binary number.

pp: Used in 16-bit arithmetic instructions employing register modes of addressing; may be BC, DE, SP, or register designated as destination operand.

qq: Used in instructions employing register modes of addressing; may be BC, DE, HL, AF, IX, or IY.

r: Used in instructions employing register mode of addressing; may be A, B, C, D, E, H, or L.

rr: Used in instructions employing register mode of addressing; may be BC, DE, HL, SP, IX, or IY.

ss: Used in instructions employing register mode of addressing; may be HL, IX, or IY.

T: Used in restart instructions employing modified page zero addressing mode; may take on hex values of 0, 8, 10, 18, 20, 28, 30, or 38.

X_L: Subscript L indicates the low-order byte of a 16-bit register.

X_H: Subscript H indicates the high-order byte of a 16-bit register.

( ): Parentheses indicate the contents are considered a pointer to a memory or I/O location.

8-Bit Loads

REGISTER TO REGISTER

Mnemonic	Description	Operation
LD r_d, r_s	Load register r_d with r_s	$r_d \leftarrow r_s$
LD A, I	Load ACC with register I	A ← I
LD I, A	Load register I with ACC	I ← A
LD A, r	Load ACC with register R	A ← r
LD r, A	Load register R with ACC	r ← A
LD r, n	Load register r with immediate data n	r ← n

REGISTER TO MEMORY

Mnemonic	Description	Operation
LD m1, r	Load memory from register r	m1 ← r
LD m2, A	Load memory from ACC	m2 ← A
LD m1, n	Load memory with immediate data n	m1 ← n

MEMORY TO REGISTER

Mnemonic	Description	Operation
LD r, m1	Load register r from memory	r ← m1
LD A, m2	Load ACC from memory	A ← m2

16-Bit Loads

REGISTER TO REGISTER

Mnemonic	Description	Operation
LD rr, nn	Load register rr with immediate data nn	rr←nn
LD SP, ss	Load SP register with register ss	SP←ss

REGISTER TO MEMORY

Mnemonic	Description	Operation
LD (nn), rr	Load memory location nn with 16 bit register rr	$(nn)\leftarrow rr_L$ $(nn+1)\leftarrow rr_H$
PUSH qq	Push contents of 16-bit register qq onto memory stack	$(SP-1)\leftarrow qq_H$ $(SP-2)\leftarrow qq_L$ SP←SP−2

MEMORY TO REGISTER

Mnemonic	Description	Operation
LD rr, (nn)	Load 16-bit register rr from memory location nn	$rr_L\leftarrow(nn)$ $rr_H\leftarrow(nn+1)$
POP qq	Pop contents of stack to register qq	$qq_L\leftarrow(SP)$ $qq_H\leftarrow(SP+1)$ SP←SP+2

8-Bit Arithmetic

REGISTER ADDRESSED ARITHMETIC

Mnemonic	Description	Operation
ADD A, r	Add contents of register r to ACC	A←A+r
ADC A, r	Add with carry contents of register r to ACC	A←A+r+CY
SUB r	Subtract contents of register r from ACC	A←A−r
SBC A, r	Subtract with carry contents of register r from ACC	A←A−r−CY
AND r	Logically AND contents of register r with ACC	A←A ∧ r
OR r	Logically OR contents of register r with ACC	A←A ∨ r
XOR r	Exclusive OR contents of register r with ACC	A←A ∀ r
CP r	Compare contents of register r to ACC	A:r Z flag←1 If A=r else Z Flag←0
INC r	Increment contents of register r	r←r+1
DEC r	Decrement contents of register r	r←r−1
DAA	Decimal adjust ACC	(ACC adjust for BCD)
CPL	Complement ACC (1's complement)	A←Ā
NEG	Negate ACC (2's complement)	A←0−A
CCF	Complement carry flag	CY←CY
SCF	Set carry flag	CY←1

IMMEDIATE ADDRESSING MODE ARITHMETIC

Mnemonic	Description	Operation
ADD A, n	Add number n to ACC	A←A+n
ADC A, n	Add with carry number n to ACC	A←A+n+CY
SUB n	Subtract number n from ACC	A←A−n
SBC A, n	Subtract with carry number n from ACC	A←A−n−CY
AND n	AND number n with ACC	A←A ∧ n
OR n	OR number n with ACC	A←A ∨ n
XOR n	Exclusive OR number n with ACC	A←A ∀ n
CP n	Compare number n to ACC	A: n Z flag←1 if A=n else Z Flag←0

MEMORY ADDRESSED ARITHMETIC

Mnemonic	Description	Operation
ADD A, m1	Add memory to ACC	A←A+m1
ADC A, m1	Add with carry memory to ACC	A←A+m1+CY
SUB m1	Subtract memory from ACC	A←A−m1
SBC A, m1	Subtract with carry memory from ACC	A←A−m1−CY
AND m1	AND memory with ACC	A←A ∧ m1
OR m1	OR memory with ACC	A←A ∨ m1
XOR m1	Exclusive OR memory with ACC	A←A ∀ m1
CP m1	Compare memory with ACC	A: m1 Z flag←1 if A=r else Z Flag←0
INC m1	Increment memory	m1←m1+1
DEC m1	Decrement memory	m1←m1−1

16-Bit Arithmetic

REGISTER ADDRESSED ARITHMETIC

Mnemonic	Description	Operation
ADD ss, pp	Add 16-bit register pp to 16-bit register ss	ss←ss+pp
ADC HL, pp	Add with carry 16-bit register pp to HL	HL←HL+pp+CY
SBC HL, pp	Subtract with carry 16-bit register pp from HL	HL←HL−pp−CY
INC rr	Increment 16-bit register rr	rr←rr+1
DEC rr	Decrement 16-bit register rr	rr←rr−1

Bit Set, Reset, and Test

REGISTER

Mnemonic	Description	Operation
SET b, r	Set bit b in register r	$r_b \leftarrow 1$
RES b, r	Reset bit b in register r	$r_b \leftarrow 0$
BIT b, r	Test bit b in register r	$Z \leftarrow r_b$

MEMORY

Mnemonic	Description	Operation
Set b, m1	Set bit b in memory location m1	m1b←1
RES b, m1	Reset bit b in memory location m1	m1b←0
BIT b, m1	Test bit b in memory location m1	Z←m1b

Exchanges

REGISTER/REGISTER

Mnemonic	Description	Operation
EX DE, HL	Exchange contents of DE and HL register	DE↔HL
EX AF, AF1	Exchange contents of A and F registers with A1 and F1 registers	AF↔AF'
EXX	Exchange contents of BC, DE and HL registers with corresponding alternate registers	BC↔BC' DE↔DE' HL↔HL'

REGISTER/MEMORY

Mnemonic	Description	Operation
EX (SP), ss	Exchange top of stack with 16-bit register ss	$(SP) \leftarrow ss_L$ $(SP+1) \leftarrow ss_H$

Memory Block Moves and Searches

Block move and search instructions (such as LDIR and INIR) insert a dummy instruction fetch after each cycle to keep refresh going.

SINGLE OPERATIONS

Mnemonic	Description	Operation
LDI	Move data from memory location (HL) to memory location (DE), increment memory pointers, and decrement byte counter BC.	(DE)←(HL) DE←DE+1 HL←HL+1 BC←BC−1
LDD	Move data from memory location (HL) to memory location (DE), and decrement memory pointer and byte counter BC.	(DE)←(HL) DE←DE−1 HL←HL−1 BC←HL−1
CPI	Compare data in memory location (HL) to ACC, increment memory pointer and decrement byte counter BC.	A−(HL) HL←HL+1 BC←BC−1
CPD	Compare data in memory location (HL) to ACC and decrement memory pointer and byte counter BC.	A−(HL) HL←HL−1 BC←BC−1

REPEAT OPERATIONS

Mnemonic	Description	Operation
LDIR	Move data from memory location (HL) to memory location (DE), increment memory pointers, decrement byte counter BC, repeat until BC = 0	(DE)←(HL) DE←DE+1 HL←HL+1 BC←BC−1 Repeat until BC = 0
LDDR	Move data from memory location (HL) to memory location (DE), decrement memory pointers and byte counter BC, repeat until BC = 0	(DE)←(HL) DE←DE−1 HL←HL−1 BC←BC−1 Repeat until BC = 0
CPIR	Compare data in memory location (HL) to ACC, increment memory pointer, decrement byte counter BC, repeat until BC = 0 or (HL) = A	A−(HL) HL←HL+1 BC←BC−1 Repeat until BC = 0 or (HL) = A
CPDR	Compare data in memory location (HL) to ACC, decrement memory pointer and byte counter BC, repeat until BC = 0 or (HL) = A	A−(HL) HL←HL−1 BC←BC−1 Repeat until BC = 0 or (HL) = A

Input/Output

Due to the multiplexed bus structure, the NSC800 handles the address bus differently than the Z80 during input and output instructions. The NSC800 duplicates the port address on the upper and lower halves of the address.

Mnemonic	Description	Operation
IN A, (n)	Input from I/O device at address n to ACC	A←(n)
OUT (n), A	Output to I/O device at address n from ACC	(n)←A
IN r, (C)	Input from I/O device at address (C) to register	r←(C)
OUT (C), r	Output to I/O device at address (C) from register	(C)←r
INI	Input from I/O device at address (C) to memory location (HL), increment pointer, and decrement B counter	(HL)←(C) HL←HL+1 B←B−1

Input/Output (Continued)

Mnemonic	Description	Operation
OUTI	Output to I/O at address (C) from memory location (HL), increment pointer, and decrement B counter	(C)←(HL) HL←HL + 1 B←B − 1
IND	Input from I/O device at address (C) to memory location (HL) and decrement pointer, and B counter	(HL)←(C) HL←HL − 1 B←B − 1
OUTD	Output to I/O device at address (C) from memory location (HL) and decrement pointer and B counter	(C)←(HL) HL←HL − 1 B←B − 1
INIR	Input from I/O device at address (C) to memory location (HL), increment pointer, decrement B counter, and repeat until B = 0	(HL)←C HL←HL + 1 B←B − 1 Repeat until B = 0
OUTIR	Output to I/O device at address (C) from memory location (HL), increment pointer, decrement B counter, and repeat until B = 0	(C)←(HL) HL←HL + 1 B←B − 1 Repeat until B = 0
INDR	Input from I/O device at address (C) to memory location (HL), decrement pointer and B counter, and repeat until B = 0	(HL)←(C) HL←HL − 1 B←B − 1 Repeat until B = 0
OUTDR	Output to I/O device at address (C) from memory location (HL), decrement pointer and B counter, and repeat until B = 0	(C)←(HL) HL←HL − 1 B←B − 1 Repeat until B = 0

CPU Control

Mnemonic	Description	Operation
NOP	No operation	
HALT*	Halt processor	
DI	Disable Interrupts	
EI	Enable Interrupts	
IM 0	Set Interrupt Mode 0	
IM 1	Set Interrupt Mode 1	
IM 2	Set Interrupt Mode 2	

*Halt instruction locks CPU into an endless cycle of instruction fetches until CPU is reset or interrupted. Therefore dynamic memory refresh continues to run.

Program Control

JUMPS

Mnemonic	Description	Operation
JP nn	Unconditional jump direct to nn	PC←nn
JP (ss)	Unconditional jump indirect via ss register	PC←ss
JP cc, nn	Conditionally jump direct to nn if cc is true	If cc true, PC←nn, else continue
JR d	Unconditional jump to PC + d	PC←PC + d
JR kk, d	Conditionally jump PC + d if kk is true	If kk true, PC←PC + d
DJNZ, d	Decrement B register and jump to PC + d if B ≠ 0, otherwise continue	B←B − 1 if B = 0 PC←PC + d

CALLS

Mnemonic	Description	Operation
CALL nn	Unconditional call to subroutine at location nn	(SP − 1)←PC_H (SP − 2)←PC_L PC←nn
CALL cc, nn	Conditional call to subroutine at location nn if cc true	If cc true, (SP − 1)←PC_H (SP − 2)←PC_L PC←nn, else continue

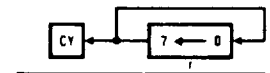
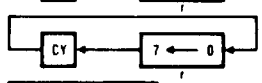
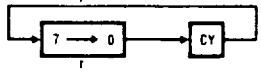
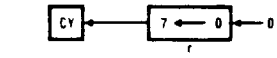
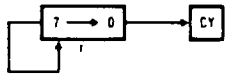
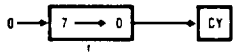
RETURNS

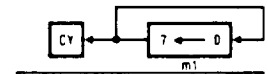
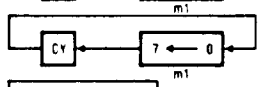
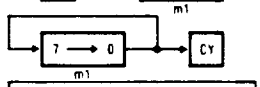
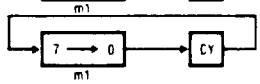
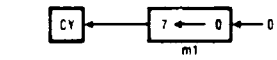
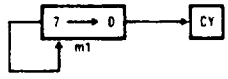
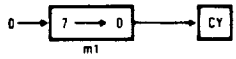
Mnemonic	Description	Operation
RET	Unconditonal return from subroutine	PC_L←(SP) PC_H←(SP + 1)
RET cc	Conditional return from subroutine	If cc true: PC_L←(SP) PC_H←(SP + 1) else continue
RETI	Return from interrupt	PC_L←(SP) PC_H←(SP + 1)
RETN	Return from non-maskable interrupt	PC_L←(SP) PC_H←(SP + 1) Restore interrupt enable status

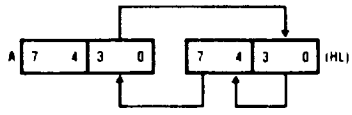
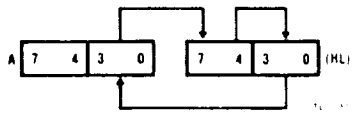
RESTARTS

Mnemonic	Description	Operation
RST T	Interrupt to location T	(SP − 1)←PC_H (SP − 2)←PC_L PC←T

Rotate and Shift

REGISTER MNEMONIC	DESCRIPTION	OPERATION
RLC r	ROTATE REGISTER r LEFT CIRCULAR	
RL r	ROTATE REGISTER r LEFT THROUGH CARRY	
RRC r	ROTATE REGISTER r RIGHT CIRCULAR	
RR r	ROTATE REGISTER r RIGHT THROUGH CARRY	
SLA r	SHIFT REGISTER r LEFT ARITHMETIC	
SRA r	SHIFT REGISTER r RIGHT ARITHMETIC	
SRL r	SHIFT REGISTER r RIGHT LOGICAL	

MEMORY MNEMONIC	DESCRIPTION	OPERATION
RLC m1	ROTATE MEMORY LEFT CIRCULAR	
RL m1	ROTATE MEMORY LEFT THROUGH CARRY	
RRC m1	ROTATE MEMORY RIGHT CIRCULAR	
RR m1	ROTATE MEMORY RIGHT THROUGH CIRCULAR	
SLA m1	SHIFT MEMORY LEFT ARITHMETIC	
SRA m1	SHIFT MEMORY RIGHT ARITHMETIC	
SRL m1	SHIFT MEMORY RIGHT LOGICAL	

REGISTER/MEMORY MNENONIC	DESCRIPTION	OPERATION
RLD	ROTATE DIGIT LEFT AND RIGHT BETWEEN ACC AND MEMORY (HL)	
RRD	ROTATE DIGIT RIGHT AND LEFT BETWEEN ACC AND MEMORY (HL)	

NSC800M/883B MIL-STD-883 Class B Screening

National Semiconductor offers the NSC800DM and NSC800EM with full class B screening per MIL-STD-883B for Military/Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

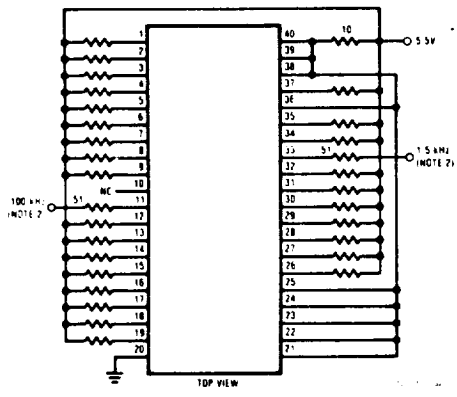
Electrical testing is performed in accordance with RETS800X, which tests or guarantees all of the electrical performance characteristics of the NSC800M data sheet. A copy of the current revision of RETS800X is available upon request.

100% SCREENING FLOW

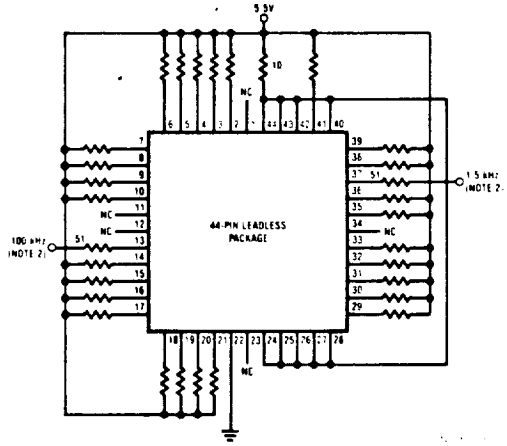
Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010B	100%
Stabilization Bake	1008 C 24 Hrs. @ + 150°C	100%
Temperature Cycling	1010 C 10 Cycles − 65°C/ + 150°C	100%
Constant Acceleration	2001 E 30,000 G's, Y1 Axis	100%
Fine Leak	1014 B 5×10^{-8}	100%
Gross Leak	1014C	100%
Burn-In	1015 160 Hrs. @ + 125°C (using burn-in circuits shown below)	100%
Final Electrical	+ 25°C DC per RETS800X	100%
PDA	10% Max	
	+ 125°C AC and DC per RETS800X	100%
	− 55°C AC and DC per RETS800X	100%
	+ 25°C AC per RETS800X	100%
QA Acceptance	Group A (sample, each lot)	
Quality Conformance	Group B (sample, each inspection lot)	
	Group C (sample every 90 days per microcircuit group)	
	Group D (sample every 6 months per package type)	
External Visual	2009	100%

Burn-In Circuits

5240HR
NSC800D/883B (Dual-In-Line)



5241HR
NSC800E/883B (Leadless Chip Carrier)



All resistors 2.7 kΩ unless marked otherwise.

Note 1: All resistors are 1/4W ± 5% unless otherwise specified.

Note 2: All clocks 0V to 3V, 50% duty cycle, in phase with < 1 μs rise and fall time.

Note 3: Device to be cooled down under power after burn-in.

Ordering Information

NSC800 X X X X

/A + = A + Reliability Screening
/883 = MIL-STD-883B Screening (Note 1)

I = Industrial Temperature (– 40°C to + 85°C)
M = Military Temperature (– 55°C to + 125°C)
No Designation = Commercial Temperature (0°C to 70°C)

– 1 = 1 MHz Clock Output (Note 2)
– 4 = 4 MHz Clock Output
No Designation = 2.5 MHz Clock Output

D = Ceramic Package
J = CERDIP Package (availability to be announced)
N = Plastic Package
E = Ceramic Leadless Chip Carrier (LCC)
V = Plastic Leaded Chip Carrier (PCC) (availability to be announced)

Note 1: Do not specify a temperature option, all parts are screened to military temperature

Note 2: – 1 part only available in D-1, N-1, D 1I, N 1I, V-1, V 1I

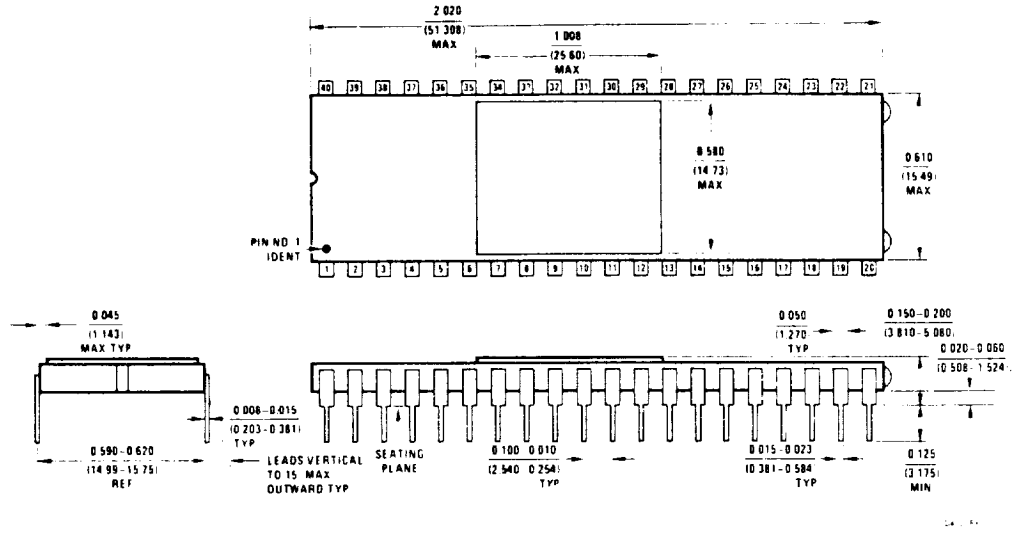
EXAMPLES

NSC800E-4/883
NSC800N
NSC800D-1I/A +

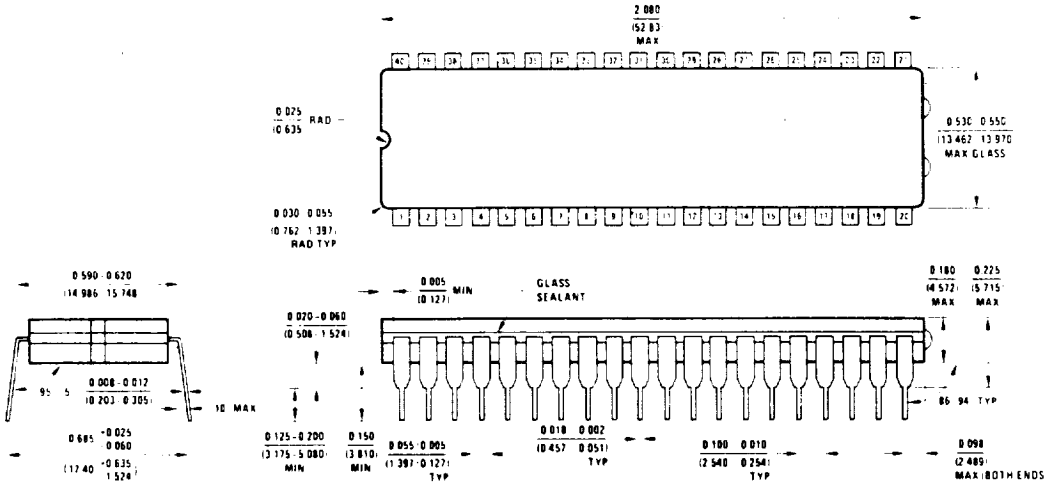
Reliability Information

Gate Count 2750
Transistor Count 11,000

Physical Dimensions inches (millimeters)



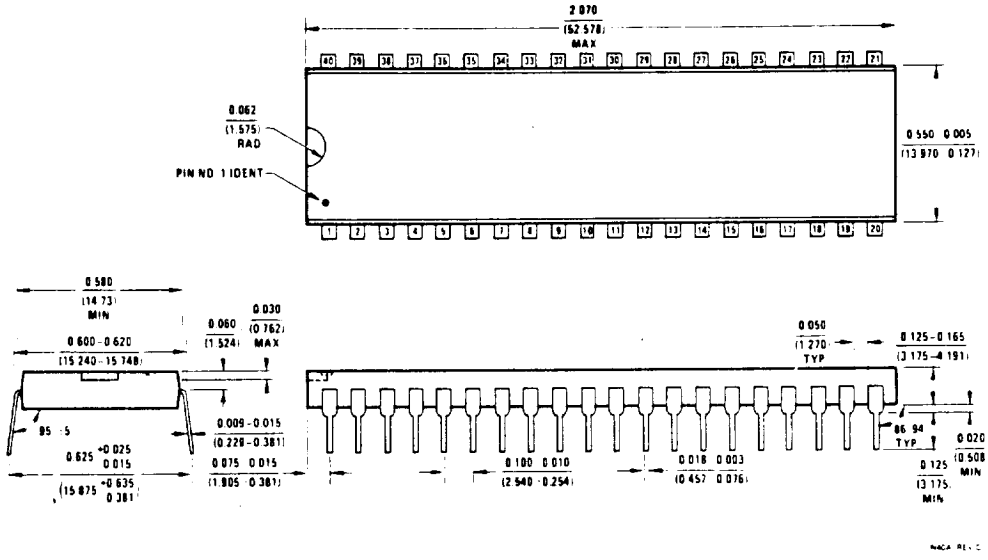
Ceramic Dual-In-Line Package (D)
NS Package Number D40C



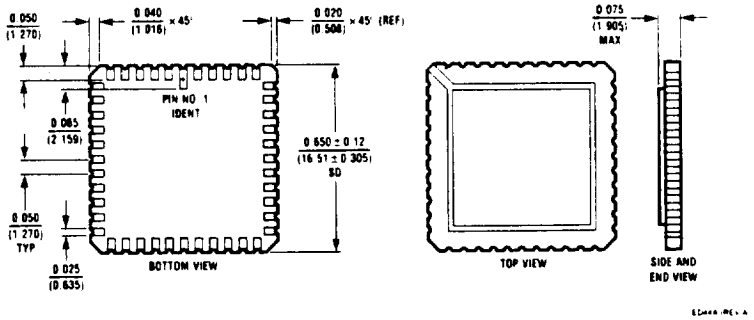
Ceramic Dual-In-Line Package (J)
NS Package Number J40A

C-2.

Physical Dimensions (Continued) inches (millimeters)

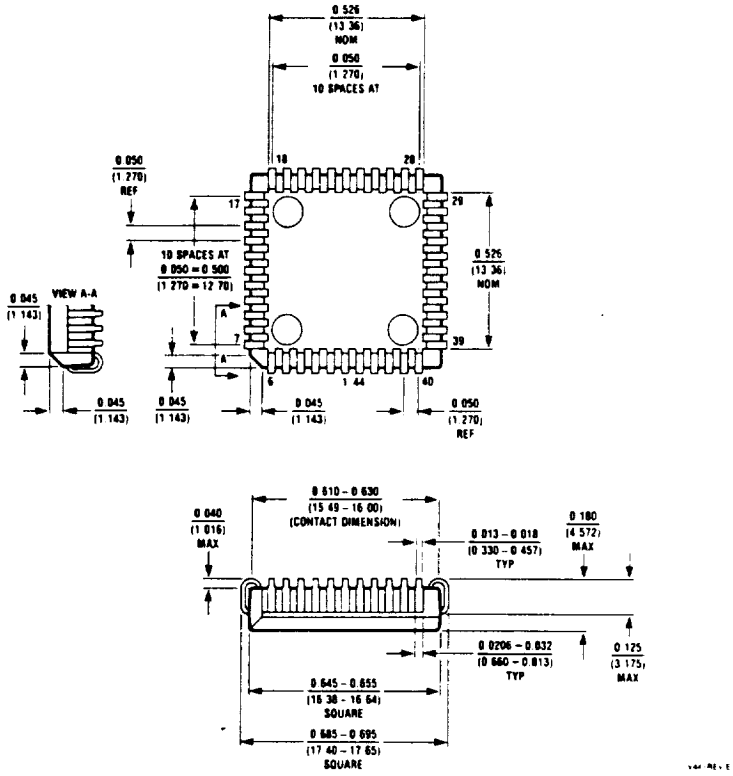


Plastic Dual-In-Line Package (N)
NS Package Number N40A



44-Pin Hermetic Leadless Package (E)
NS Package Number ED44A

Physical Dimensions inches (millimeters) (Continued)



44-Lead Plastic Chip Carrier (V)
NS Package Number V44

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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