A COMBINED ELECTRON BEAM/OPTICAL LITHOGRAPHY PROCESS STEP FOR THE FABRICATION OF SUB-HALF-MICRON-GATE-LENGTH MMIC CHIPS

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ABSTRACT

Advanced radar and communication systems rely heavily on state-of-the-art microelectronics. Systems such as the phased-array radar require many transmit/receive (T/R) modules which are made up of many millimeter wave - microwave integrated circuits (MMICs). The heart of a MMIC chip is the Gallium Arsenide (GaAs) field-effect transistor (FET). The transistor gate length is the critical feature that determines the operating frequency of the radar system. A smaller gate length will typically result in a higher frequency. In order to make a phased array radar system economically feasible, manufacturers must be capable of producing very large quantities of small-gate-length MMIC chips at a relatively low cost per chip. This requires the processing of a large number of wafers with a large number of chips per wafer, minimum processing time, and a very high chip yield.

One of the bottlenecks in the fabrication of MIMIC chips is the transistor gate definition. The definition of sub-half-micron gates for GaAs-based field-effect transistors is generally performed by direct-write electron beam lithography (EBL). Because of the throughput limitations of EBL, the gate-layer fabrication is conventionally divided into two lithographic processes where EBL is used to generate the gate fingers and optical lithography is used to generate the large-area gate pads and interconnects. As a result, two complete sequences of resist application, exposure, development, metallization and lift-off are required for the entire gate structure. We have baselined a hybrid process, referred to as EBOL (electron beam/optical lithography), in which a single application of a multi-level resist is used for both exposures. The entire gate structure, (gate fingers, interconnects and pads), is then formed with a single metallization and lift-off process. The EBOL process thus retains the advantages of the high-resolution E-beam lithography and the high throughput of optical lithography while essentially eliminating an entire lithography/metallization/lift-off process sequence. This technique has been proven to be reliable for both trapezoidal and mushroom gates and has been successfully applied to metal-semiconductor and high-electron-mobility field-effect transistor (MESFET and HEMT) wafers containing devices with gate lengths down to 0.10 micron and 75 x 75 micron gate pads. The yields and throughput of these wafers have been very high with no loss in device performance. We will discuss the entire EBOL process technology including the multilayer resist structure, exposure conditions, process sensitivities, metal edge definition, device results, comparison to the standard gate-layer process, and its suitability for manufacturing.

INTRODUCTION

Fabrication of solid-state electronic devices and circuits is accomplished through a series of processing cycles. One of these consists of a lithography, a metal deposition, and a metal lift-off step. This particular cycle of steps may be repeated many times before fabrication is complete. Much work has been done in making this cycle faster and more reliable to decrease the semiconductor processing time.

Many variations of this cycle are used. The most common form of lithography is photolithography in which a wafer is coated with a thin film of a material that is sensitive to light (photoresist). The photoresist is then exposed by a pattern of light via a patterned quartz mask. After exposure the photoresist is developed and the exposed photoresist or unexposed photoresist (depending on the type of photoresist and developer used) is rinsed away. The next step of the cycle is to evaporate metal onto the wafer. Finally, a lift-off technique is used to remove the remaining unexposed photoresist and the metal on top of it. Thus,

only the desired pattern of metal remains. Photolithography is generally limited to geometries down to 0.6 microns with possible placement errors up to a micron.

For smaller geometries (< 0.6 µm) and/or geometries which require highly accurate placement, electron beam lithography (EBL) is commonly used. EBL is similar to photolithography except that an EBL resist (which is sensitive to an electron beam rather than UV light) is used in place of photoresist and the pattern is drawn onto the wafer with an electron beam rather than exposed through a mask. EBL can write both large geometries and small geometries (less than a tenth of a micron) with accurate placement.

Modern solid-state electronic devices or circuits require small-geometry structures (such as transistor gates) be connected to large-geometry structures (such as probe pads or interconnects) for continuity. To make these connections, the entire layer (small geometries and large geometries) could be fabricated by EBL/metal deposition/lift-off cycle. Although this technique produces good results, it is usually extremely time consuming. When an e-beam machine is set up to define smaller-geometry patterns, the beam spot size is small and larger geometries can take an extremely long time to write. When the machine is optimized for large-geometry writes, the beam spot size is large and ultra-fine features are very difficult to write. The write times in conjunction with lengthy switch-over times required to change the machine from "large-geometry mode" to "small-geometry mode" (i.e. change the accelerating voltage, switch the aperture selection, re-align the column, etc.) make this technique impractical for combination large geometry and fine geometry fabrication. More commonly, the large-and-small-geometry fabrication method is to use photolithography/metal deposition/lift-off cycle to form the large-geometry structures and EBL/metal deposition/lift-off cycle to overlap the small-geometry structures. Again, this method is time consuming because two cycles are required, and it also introduces a metal-to-metal coverage problem. If the overlapping metal is not thick enough, good electrical contact will not be made and a device failure mechanism is introduced. A third method is to use a deep ultraviolet (UV) light mask aligner to image the large-geometry patterns, EBL to image the small-geometry patterns, and a single metal deposition/liftoff for both geometry patterns[1]. This method is excellent; however, it requires a deep UV mask aligner or stepper. Deep UV mask aligners are not found in every integrated circuit lab. We present an alternative fabrication process that combines optical photolithography and EBL into one process step with one metal deposition and one metal lift-off which can be used for high-throughput, fine-geometry device fabrication.

EBOL PROCESS

The EBOL process is as follows. The wafer is coated with standard e-beam resist scheme (1 to 3 layers), followed by a layer of optical photoresist. The wafer is then aligned and exposed to the gate pad mask using an optical mask aligner. The top photoresist is then developed. The resulting pattern is used as a mask for a deep UV exposure of the e-beam resists. The large patterns are now exposed. The top layer photoresist is then removed without damaging the underlying e-beam resists. Next, The gates are written by e-beam. Once the exposed resists are developed, metal is deposited. The resulting metal layer consists of very large gate pads and 0.25 µm gate fingers. The turn-around time is very fast compared to our standard 2 cycle process, and no step coverage problem exists of the gate fingers onto the gate pads.

The major obstacle in developing this process was to remove the top-layer photoresist after the deep UV exposure without affecting the underlying e-beam resists. It was first believed the optical photoresist could be developed out after the deep UV exposure if it was flood exposed by light. Poly-(methyl methacrylate) (PMMA)[2] was used for the initial process development. The optical photoresist used was 1400-27[3]. When 351 developer[4] was used to remove the exposed 1400-27, a thin film formed between the PMMA and the 1400-27 resists which could not be removed by realistic methods (i.e. solvent clean, microposit remover 1165[5], or oxygen plasma stripper). SAL 110-PLI[6] (PMGI) was tried in place of PMMA and a similar film formed. After unsuccessful attempts to try to develop the photoresist away, dissolving it was tried. PMGI can be dissolved by 1165, PMMA by 1165 or by acetone, and 1400-27 by acetone. Fortunately, the dissolution rate of PMMA in acetone is much slower than 1400-27 in acetone. A short blast of acetone was shown to remove the 1400-27 without significantly affecting PMMA or PMGI resists. After the photoresist was removed the e-beam write, development, gate recess etch, gate deposition and liftoff were routine.

C-2.

The following is an example of our EBOL process for a 0.25 μm mushroom gate[7].

1. Solvent clean.
   Spin e-beam resist - PMMA 496K 4% (60 seconds at 3000 rpm), P(MMA-MAA)[8] Type I 9% (60 seconds at 3000 rpm), PMMA 496K 4%:chlorobenzene [2:1] (60 seconds at 3000 rpm).
   Bake - 5 minutes on a 200 °C hot plate.
   Spin optical photoresist - 1400-27 (30 seconds at 4000 rpm).
   Bake - 5 minutes on a 100 °C hot plate.

1400-27
PMMA496K4%:Chlorobenzene (2:1)
P(MMA-MAA)
PMMA 496K4%
Substrate

Figure 1. Schematic of resist scheme after coating

2. Align and expose optical resist using gate pad/interconnect mask - 12 mW/cm^2 for 42 seconds. Develop 1400-27 photoresist - 351:de-ionized water [1:5] (30 seconds at 500 rpm), de-ionized water (30 seconds at 500 rpm).
   Deep-UV exposure - 240 nm at 10 mW/cm^2 for 600 seconds.

1400-27
PMMA496K4%:Chlorobenzene (2:1)
P(MMA-MAA)
PMMA 496K4%
Substrate

Figure 2. Schematic of resist after deep UV exposure of large patterns.

3. 1400-27 removal - acetone spray (15 seconds at 500 rpm), isopropyl alcohol (15 seconds at 500 rpm).

PMMA496K4%:Chlorobenzene (2:1)
P(MMA-MAA)
PMMA 496K4%
Substrate

Figure 3. Schematic of resist after the optical resist is stripped away.

4. E-beam direct write - JEOL JBX5DII(U), 5th lens, 50 kV, 50 pA, (A,10), center single-pass-lines (dose: 3.5 nC/μm), 0.1 μm offset wing areas (0.25 μm wide) (dose: 150 μC/μm^2).

PMMA496K4%:Chlorobenzene (2:1)
P(MMA-MAA)
PMMA 496K4%
Substrate

Figure 4. Schematic of resist after e-beam write.

5. Develop e-beam resists - chlorobenzene 15 seconds at 500 rpm), isopropyl alcohol (30 seconds at 500 rpm), methyl-isobutyl-ketone (MIBK):isopropyl alcohol [1:1] (90 seconds at 500 rpm), isopropyl alcohol (30 seconds at 500 rpm).

PMMA496K4%:Chlorobenzene (2:1)
P(MMA-MAA)
PMMA 496K4%
Substrate

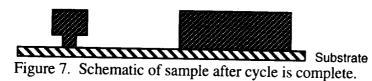Figure 5. Schematic of resist after e-beam resist development.

6. Oxygen plasma .
   Gate recess - standard.
   Pre-metal dip - standard
   Gate metal deposition - approximately 6000 Å (standard gate metal).

PMMA496K4%:Chlorobenzene (2:1)
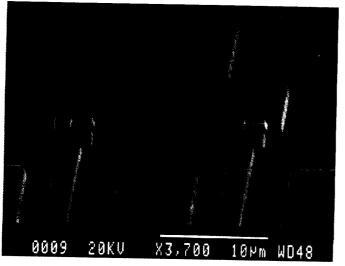P(MMA-MAA)
PMMA 496K4%
Substrate

Figure 6. Schematic of sample after metal deposition.

7. Gate metal lift-off.
   Solvent clean.

Substrate

Figure 7. Schematic of sample after cycle is complete.

RESULTS

Figure 8 shows a conventional gate layer formation. This process fabricates the gate layer in two cycles. First the gate pads are formed by optical lithography/metal deposition/lift-off cycle and then the gate fingers are formed by a EBL/metal deposition/lift-off cycle. Aside from being time-consuming due to the two cycles, this process introduces a possible failure mechanism due to the gate finger metal overlap and adhesion to the gate pad metal. Figure 10 shows a typical EBOL device.
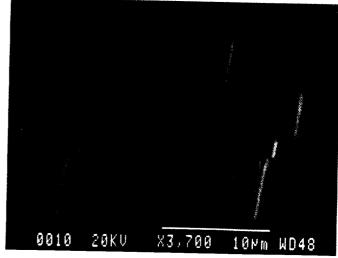

Figure 8. A conventional gate layer showing gate finger/pad step coverage

Figure 9. An EBOL gate layer showing the elimination of gate finger/pad step coverage.

This process has been used to fabricate various device types such as metal-semiconductor field effect transistors (MESFETs), high electron mobility transistors (HEMTs), and heterojunction bipolar transistors (HBTs). In addition, this process has been used to fabricate Low Noise Amplifier MMIC circuits. However, most of the device data has been taken from MESFET devices. The following are some of the results using the EBOL process for MESFET device fabrication. Figure 10 shows a wafermap and histogram of DC transconductance (gm) at zero gate voltage for 0.25 µm x 50 µm gate MESFETs on a 2-inch semi-insulating GaAs substrate with a 1µm undoped GaAs buffer followed by a 1000 Å layer of

7×10^{17} doped GaAs capped by a 500 Å layer of 2.5×10^{18} doped GaAs (MBE grown). The average value is 306 mS/mm with a standard deviation of 45 mS/mm. The median value is 323 mS/mm with a lower quartile value of 278 mS/mm and an upper quartile value of 333 mS/mm. The plots show that the device performance is extremely uniform across the wafer. Note that the majority of the poor devices are around the edge of the wafer.

Binned/Total Data Points : 199/224

Mean ± Standard Deviation (binned);
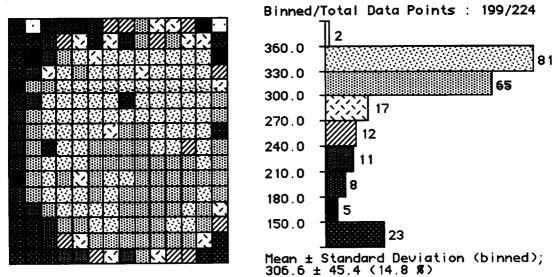306.6 ± 45.4 (14.8 %)

Figure 10. A wafermap and histogram of DC transconductance (gm) for MESFETs with an EBOL fabricated gate layer.

Figure 11 shows the RF transconductance wafermap and histogram from the same wafer as in figure 10. These devices have 2 x 0.25 µm x 75 µm gates. The average RF gm value is 374 mS/mm with a standard deviation of 90 mS/mm.

Binned/Total Data Points : 174/186

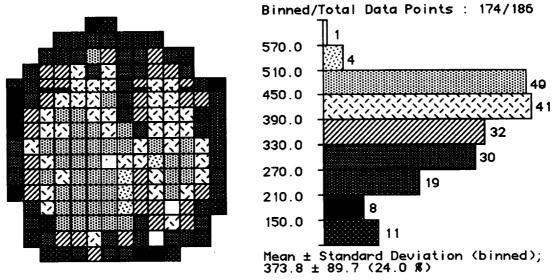Mean ± Standard Deviation (binned);
373.8 ± 89.7 (24.0 %)

Figure 11. A wafermap and histogram of RF transconductance (gm) for MESFETs with an EBOL fabricated gate layer.

Figure 12 shows the cutoff frequency (F_t) wafermap and histograms for the same devices as in figure 11. The average F_t value is 42 GHz with a standard deviation of 4 GHz. The corresponding measured noise figure for a representative device was 0.3 dB at 12.6 mA at 10 GHz.
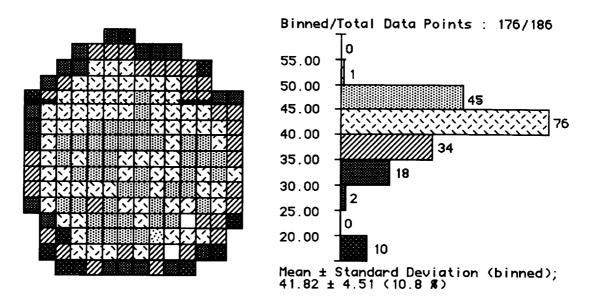
Figure 12. A wafermap and histogram of cut-off frequency (Ft) for MESFETs with an EBOL fabricated gate layer.

CONCLUSION

We have demonstrated that the EBOL process not only saves processing time due to a reduced number of metal and liftoff steps, but it is also capable of producing devices at least comparable to (if not better than) devices fabricated with a conventionally fabricated gate layer. The process has been proven successful and does not require any processing "tricks" to get acceptable results. Moreover, the yields have been exceptional most likely due to the elimination of step coverage problems. Finally, this process is quite flexible. Both a 2-layer (PMMA/P(MMA-MAA)) trapezoidal resist scheme and a 3-layer (PMMA/P(MMA-MAA)/PMGI) mushroom resist scheme have been used successfully. This process should be able to be combined with any existing e-beam process without any problems. These qualities make this process ideally suited for the manufacturing of sub-half-micron-gate-length microwave devices and circuits.

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REFERENCES

1) Y. Todokoro et al., "A Hybrid E-beam/Deep-UV Lithography for GaAs FET's",SPIE Electron-Beam, X-Ray and Ion-Beam Lithographies VI, Vol. 773, pp 54-60, 1987.
2) KTI Chemicals Incorporated, 1170 Sonora Ct., Sunnyvale CA 94086.
3) Shipley Company Incorporated, 2300 Washington St., Newton MA 02162.
4) Shipley Company Incorporated, 2300 Washington St., Newton MA 02162.
5) Shipley Company Incorporated, 2300 Washington St., Newton MA 02162.
6) Shipley Company Incorporated, 2300 Washington St., Newton MA 02162.
7) R.C. Tiberio et al., "Electron Beam Lithography and Resist Processing for the Fabrication of T-gate Structures", Proc. SPIE, 1089, 124, 1989.
8) KTI Chemicals Incorporated, 1170 Sonora Ct., Sunnyvale CA 94086.