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Multichannel Demultiplexer-Demodulator

Final Report

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National Aeronautics and
Space Administration

1.0 INTRODUCTION

This Final Design Report satisfies the last remaining requirement specified in Section 2.5, "Task V - Testing, Verification, Analyses and Delivery" in the MCDD Statement of Work.

This report is not a stand-alone document. It is intended to be an update to the "MCDD Detailed Design Report".

There are 6 sections to this report:

1.0 Introduction
2.0 Changes since DDR
3.0 Lessons Learned
4.0 Recommendations/Enhancements
5.0 Sample BER plots
6.0 List of Acronyms

Section 2 discusses changes to the POC since the Detailed Design Review. A number of small adjustments to the design were made.

Section 3 discusses issues and discoveries which will help future designers do a better job.

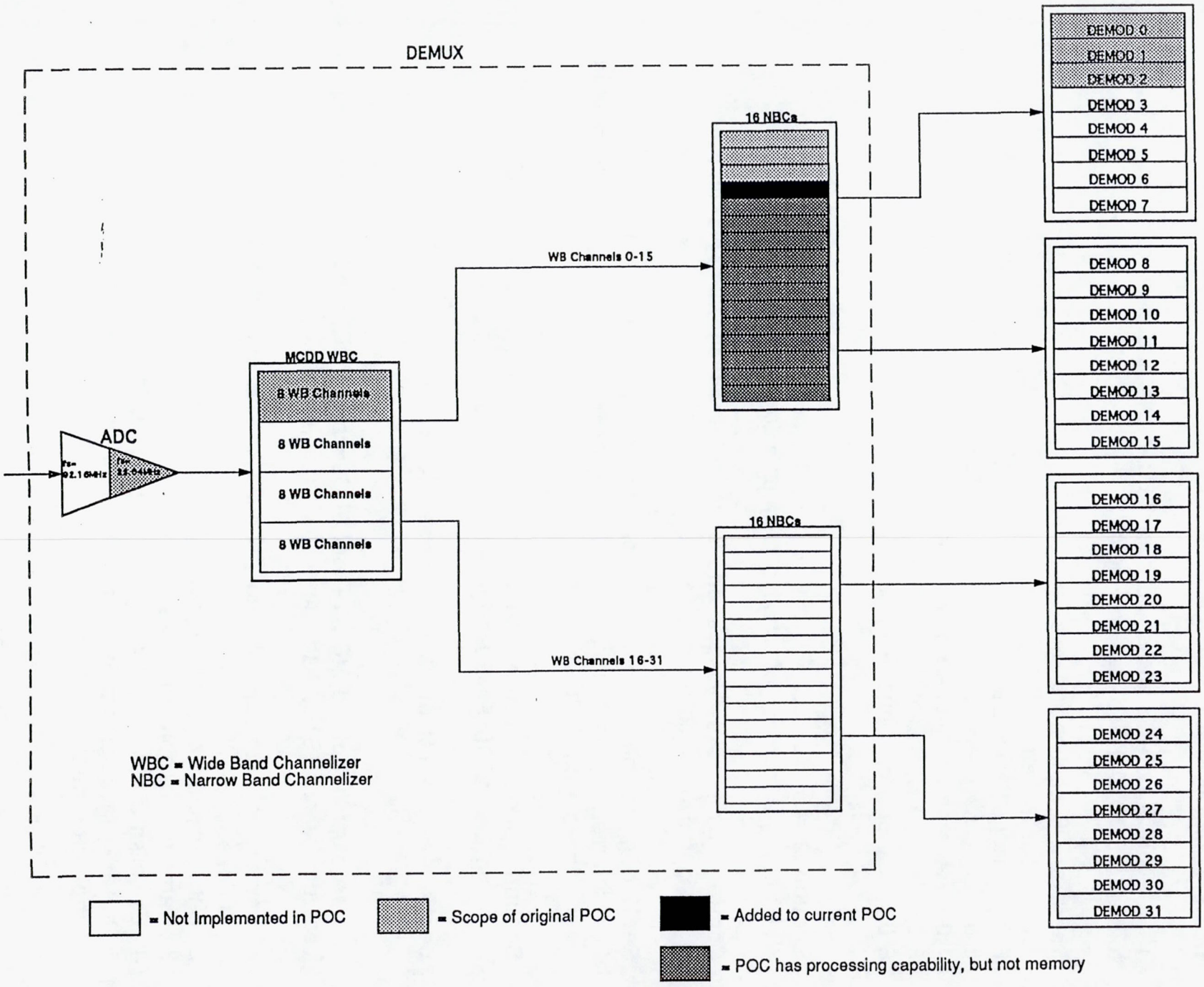
Section 4 includes recommendations for future designs. These recommendations are ideas which originated too late to be incorporated into the current POC.

Section 5 includes two samples of BER plots produced by the POC and STE during the MCDD Final Design Review.

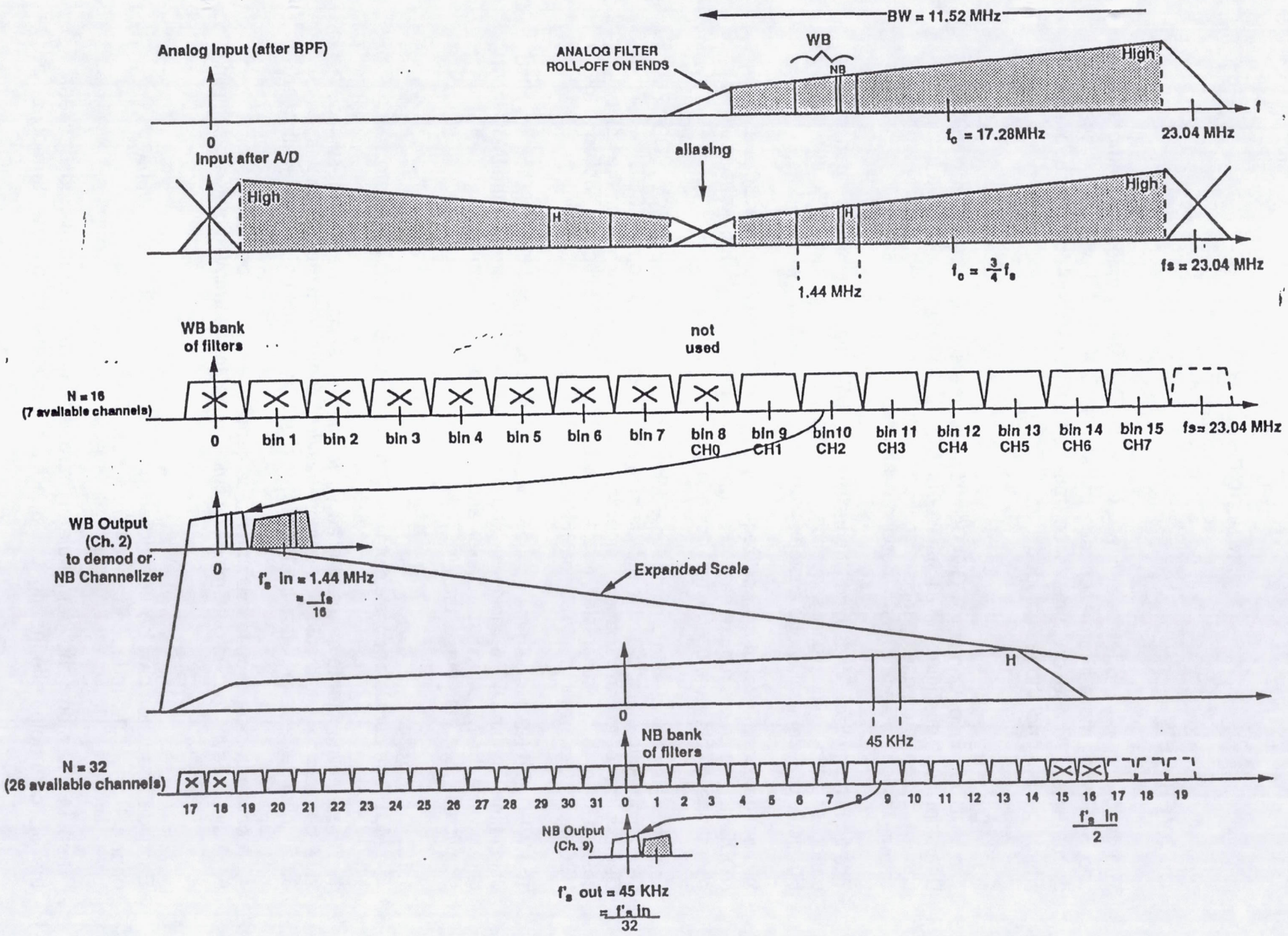
Section 6 is a list of commonly used Acronyms.

The development of the MCDD Proof of Concept (POC) model and the Special Test Equipment (STE) had the following objectives:

1. Demonstrate its capability to demultiplex and demodulate FDMA uplinks.
2. Show expandability to thousands of channels.
3. Carry out performance tests.
4. Establish a database for the next phase of MCDD.
5. Initiate development of components critical to a future flight implementation.



POC SUBSET OF MCDD



MCDD POC FREQUENCY PLAN

1.1 OVERVIEW

The following is a brief overview of the MCDD Demultiplexer, Demodulator and STE. For more information, see the MCDD DDR and the MCDD Closeout documents. Those documents contain textual and graphical descriptions which go beyond those included here.

1.1.1 Demux

The MCDD Proof of Concept (POC) Demultiplexer is a subset of the full size MCDD Demultiplexer (see Figure "POC Subset of MCDD"). It performs wideband (course) channelization of an analog input signal and, optionally, narrowband (fine) channelization on each of the wideband channels.

The first channelizer (Wideband Channelizer or WBC) applies a set of sixteen complex bandpass filters to the digital sequence out of the ADC. These sixteen equally spaced FIR filters are identical to one another except in center frequency.

Since the second level of channelizers (Narrowband Channelizers or NBCs) and the MCDD demodulators require baseband inputs, the WBC also performs the required operations to shift each filter output down to dc.

Each NBC is dedicated to a particular wideband channel out of the WBC. A NBC may be configured to either pass the data from the WBC, unaltered, to an MCDD Demodulator or to narrowband channelize the data before sending it. In the latter case, a set of thirtytwo complex, equally spaced bandpass FIR filters is applied to the NBC input data. As in the WBC, each NBC output is shifted to baseband.

The WBC and NBC requirements are very similar and both are efficiently implemented using time domain DFT techniques. Some notable differences are that the WBC input is real while the NBC input is complex and that the input sampling rate to a NBC is significantly less than that of the WBC.

1.1.2 Demod

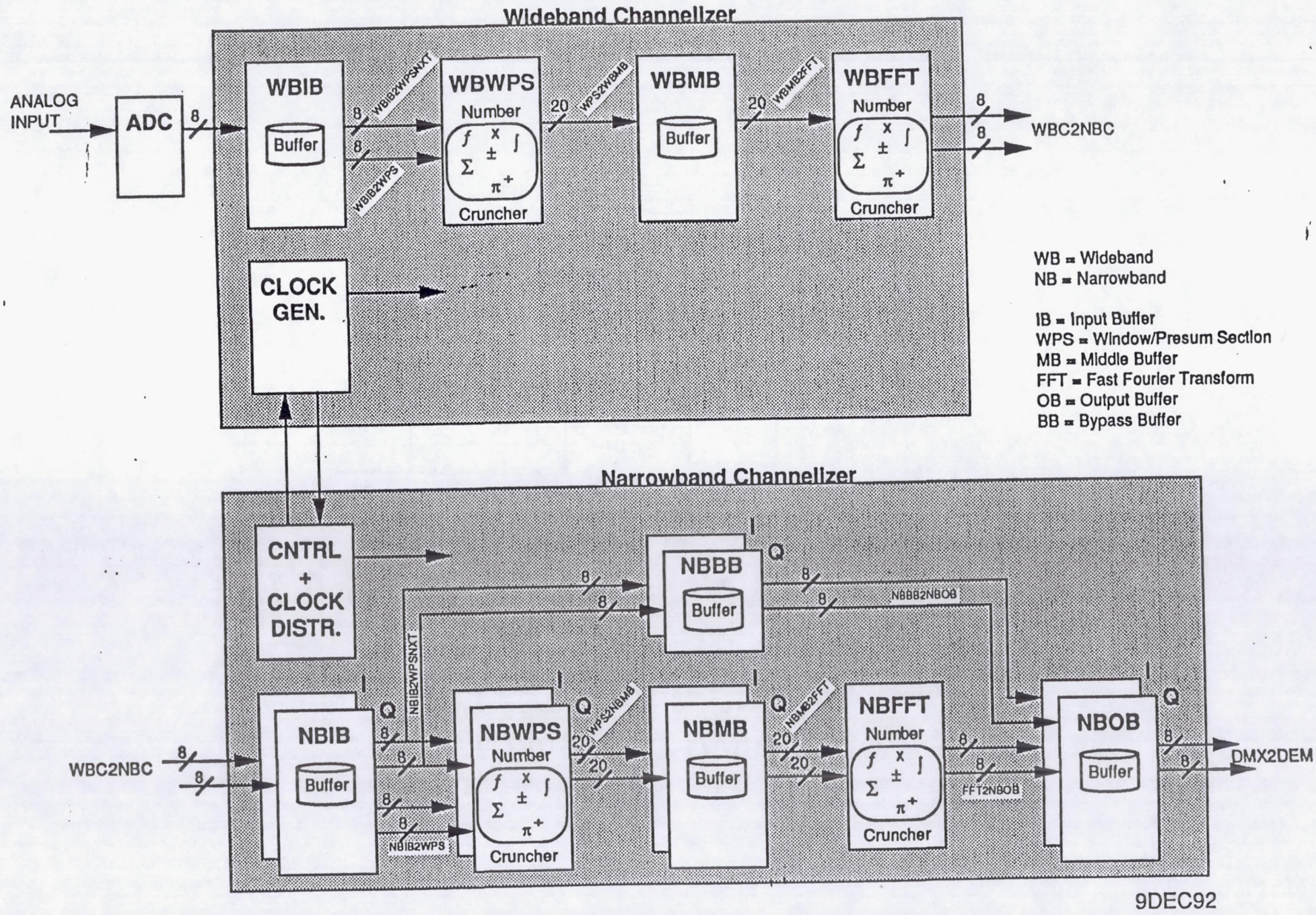
The MCDD demodulator consists of five major functional blocks. These are:

1. A resampling filter to generate exactly two complex signal samples per symbol.
2. A derotate complex multiply to remove residual carrier from these samples.
3. Symbol decision to determine the received two-bit symbol (differentially encoded OQPSK).
4. A carrier tracking loop to estimate the carrier phase offset to be derotated.
5. A symbol sync loop to determine any timing offset to be removed by the resampling filter.

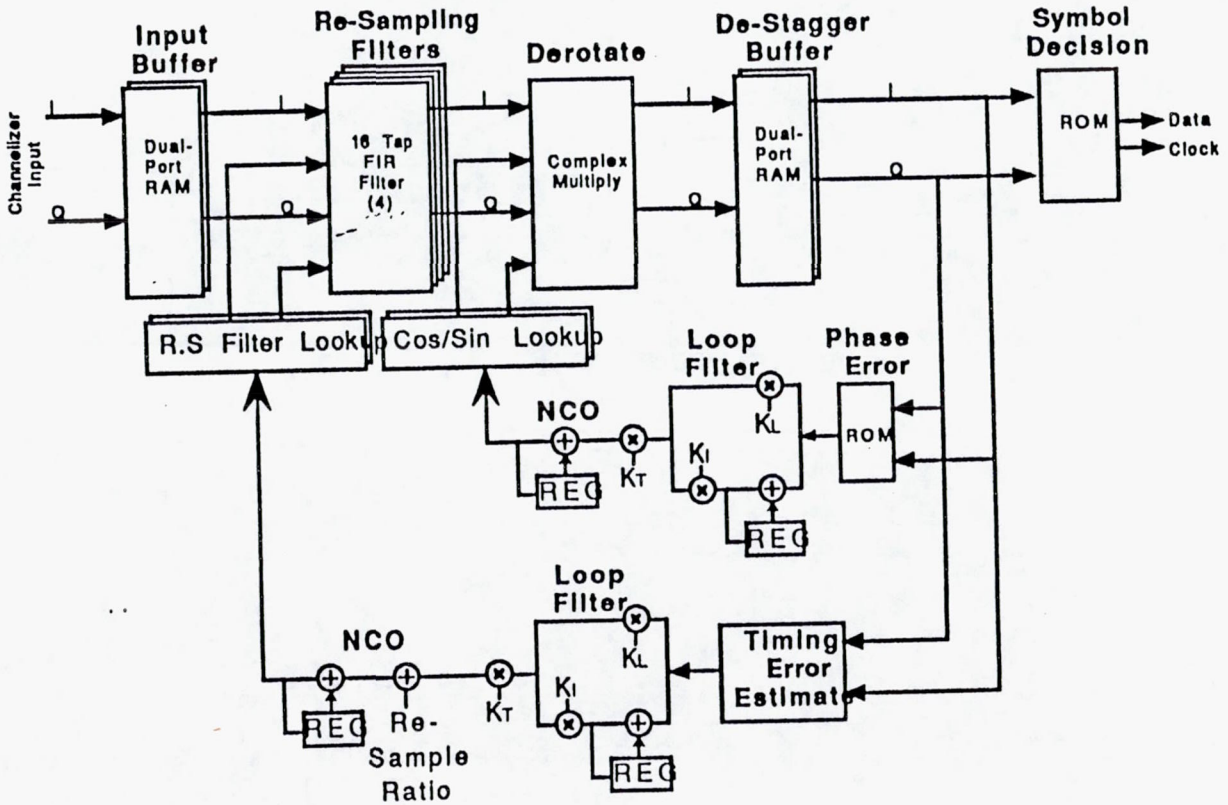
Each demodulator can be configured as a single 2.048Mbps wideband channel or as 32 independent 64Kbps narrowband channels.

When in NB mode the demodulator hardware is time multiplexed between the 32 channels, eliminating the need for duplicate hardware running at a

MCDD DEMUX BLOCK DIAGRAM



Multi-Rate Demodulator

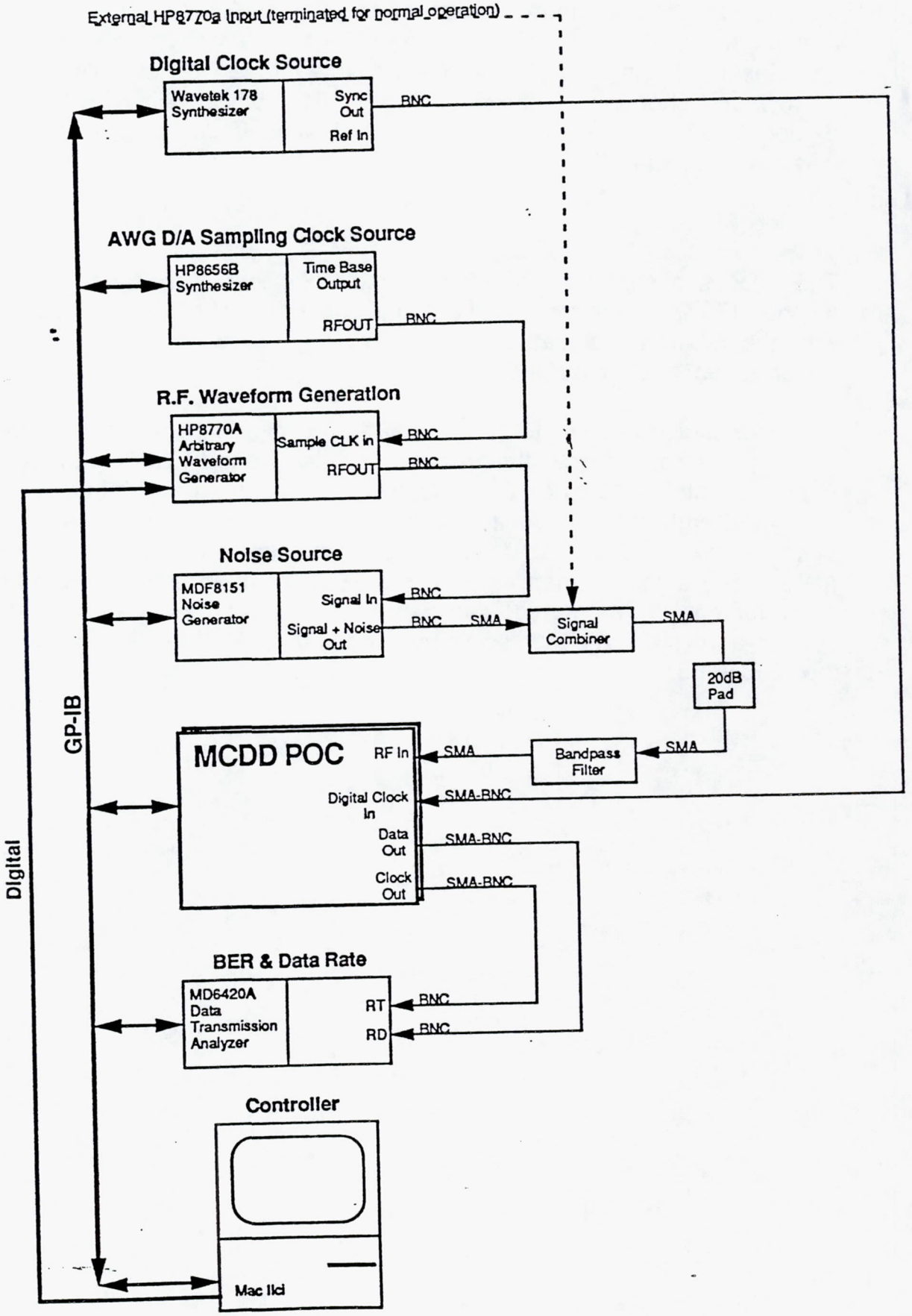


slow rate. Data is input to each of the demodulators from the demultiplexer at a rate of 1.44Msps. This data will be consecutive time samples for a single WB channel, or time interleaved samples from 32 narrowband channels. The output of the POC will be either a 2.048 Mbps demodulated data stream from the WB channel under test or any one of the thirtytwo 64Kbps NB channels.

1.1.3 STE

The STE is composed entirely of commercial test equipment. It is based on the HP8770A Arbitrary Waveform Generator. The AWG is downloaded with the desired digitized waveforms which are run through a DAC to generate an analog output signal.

The STE includes a white noise source and signal combiner (included in the noise generator) to give the necessary noise added to our generated signal. A coupler also is provided to allow an optional external input to be combined with the composite FDM signal. This combined waveform will then be low-pass filtered to eliminate any aliasing effects induced by the AWG. The signal is then input to the POC for channelization and demodulation. The demodulated output is input to a bit-error-rate test set for analysis. All test equipment contained in the STE is controlled via the IEEE-488.



Special Test Equipment Interface Diagram

2.0 Changes

2.1 Demux

The demux had three minor changes since DDR. First, the Kaiser-Bessel windows in the WB and NB channelizers were replaced with equiripple designs. This change merely consisted of burning new coefficient PROMs for each of the channelizers.

The second and third changes to the Demux were changes in gain. Originally, each channelizer had a gain of 1. The gain in the WB channelizer was changed to 2 while that of the NB channelizer was changed to 8. These changes were required to preserve sufficient loading at the output of the Demux (input to the Demod). Incorporating these changes only involved moving DIP Switch settings to the LSI Logic FFT chips.

2.2 Demod

The demod also had three changes since DDR. First, the resample filter control sequencing was modified to save the NCO value used to determine overflow. Second, the polarity of the timing estimate (symbol sync loop) was reversed. And finally, the loop filter accumulators were limited to prevent overflow wrap-around.

2.3 STE

The Special Test Equipment had a number of minor changes and additions. These are listed below:

1. Eb/No calibration was automated with LabVIEW software.

2. A digital interface card was added to the Macintosh to speed waveform loading to the HP8770 AWG.

3. An amplifier was inserted in front of the ADC.

4. Acceptance test parameters were made dynamically definable using LabVIEW software or a text editor.

5. The POC clock source is no longer phase locked to the waveform generator synthesizer.

3.0 Lessons Learned

3.1 Degradation to Narrowband Channel 0 in the POC

Truncation of a binary number (two's complement representation is assumed) will either (1) cause the original number to migrate in the direction of negative infinity (i.e. closer to zero for positive numbers and away from zero for negative numbers) or (2) leave the original number unchanged. Case number two occurs when the truncated bits all happened to be zero.

The discussion above implies that if the samples of a digitized waveform are truncated, a negative dc offset (with respect to the original signal) will necessarily result. The magnitude of the offset depends on the number of bits truncated as follows:

$$\text{DC Offset} = -0.5\,[LSB_T - LSB_O]$$

where,

LSB_O = The magnitude value a 1 would contribute in the least significant bit position in the original (non - truncated) number.

LSB_T = The magnitude value a 1 would contribute in the least significant bit position in the new (truncated) number.

Data at the output of the WBC is truncated down from 20 to 8 bits. For the WBC output, $LSB_O = 2^{-19}$ and $LSB_T = 2^{-7}$. This results in a DC offset value of approximately -2^{-8}. The effect on WB channels is empirically seen to be negligible.

Similarly, data at the output of the NBC is truncated down from 20 to 8 bits. Again, the effect on NB channels is empirically seen to be negligible.

However, note that the dc offset in each particular WB channel falls in the frequency band belonging to NB channel 0 for that particular WB channel (see figure, "MCDD POC Frequency Plan"). Thus, NB channel 0 will not only have an offset due to truncation at the NBC output, but will also carry the effect due to truncation at the WBC output. Furthermore, the NBC applies a gain of 8 as it processes its data. This gain applies equally to any dc offset present in the input.

The end result of truncation at the WBC and NBC outputs is a degradation in performance for NB channel 0 in each WB channel.

The simplest solution to avoid the phenomenon discussed above is to apply rounding instead of truncation at each channelizer's output. The simplest rounding technique will still add a small dc offset, however the magnitude of this offset will be much less than that of truncation (assuming a significant number of bits are truncated). The magnitude of the offset induced by simple rounding is as follows:

DC Offset = + 0.5 LSB_O

where,

LSB_O = The magnitude value a 1 would contribute in the least significant bit position in the original (non - truncated) number.

Simple truncation is performed simply by adding + 0.5 LSB_T to the original number and then truncating.

The analysis and conclusions provided above should be treated as unverified hypotheses on any future MCDD activity. Schedule and budget did not allow thorough determination of the cause and effect of the degraded performance in NB channel 0.

For additional "lessons learned", see the MCDD Final review package.

4.0 Recommendations/Enhancements

4.1 Demux

Removing the NB Channelizer output buffer can save 16K bytes of DPRAM. The result is a channelizer output which bursts 512 samples of a particular WB channel before switching to the next one. The MCDD closeout documentation has a complete discussion of this reduction.

Additionally, an enhanced corner-turning approach was discovered which halves the required memory depth of corner turning buffers. As a result, the NBC input buffer can be reduced from 24K bytes of DPRAM to 16K bytes with very little extra control logic.

4.2 Demod

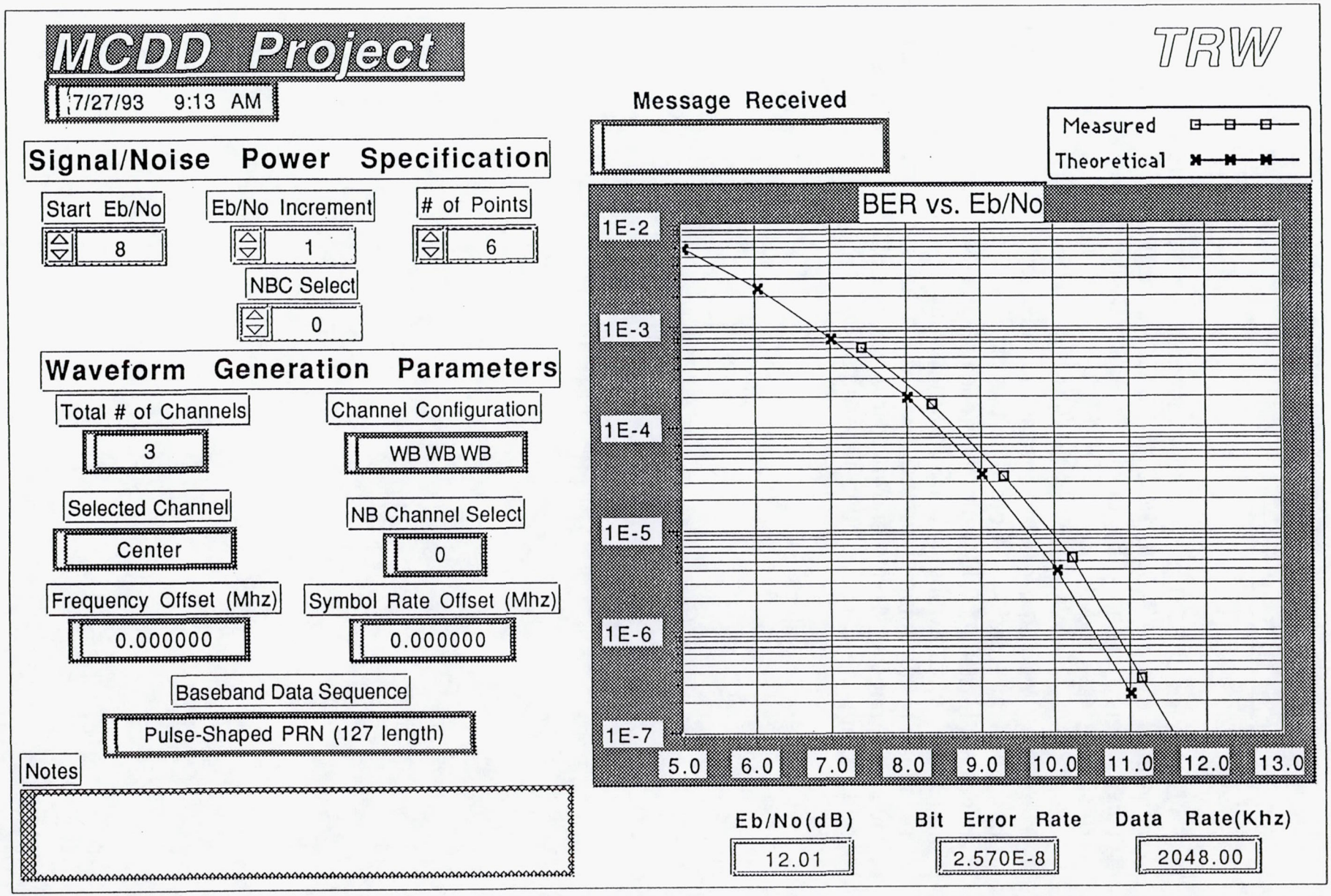
The inability of the demod to lock up on carrier frequency offsets > 1.5 times the loop bandwidth can be overcome by using a swept acquisition scheme in the carrier tracking loop. This would be accomplished by muxing in a constant into the CT NCO periodically if the loop was not locked. This would sweep the CT NCO through its possible range of values. The sweep mechanism would be disabled when the loop achieved lock.

5.0 Sample BER Plots

Two samples of BER plots (one Wideband and one Narrowband) which were generated with the MCDD POC and STE are included in this section. These curves were run at NASA Lewis Research Center during the MCDD Final Design Review and demo.

The case (Wideband or Narrowband) is indicated on the plot in the "channel configuration" window. Note that the plot for the WB channel is consistently about .3dB from theoretical. The NB plot starts out at about .4dB and ends at about .75dB from theoretical. While .75dB is a reasonable implementation loss, we would have expected closer tracking over the range of Eb/No shown. However, we did not have time to explore and isolate the cause of this flare out.

Front Panel


MCDD Project
7/27/93 9:13 AM
TRW
Message Received
Signal/Noise Power Specification
Start Eb/No
8
Eb/No Increment
1
# of Points
6
NBC Select
0
Waveform Generation Parameters
Total # of Channels
3
Channel Configuration
WB WB WB
Selected Channel
Center
NB Channel Select
0
Frequency Offset (Mhz)
0.000000
Symbol Rate Offset (Mhz)
0.000000
Baseband Data Sequence
Pulse-Shaped PRN (127 length)
Notes
Measured
Theoretical
BER vs. Eb/No
1E-2
1E-3
1E-4
1E-5
1E-6
1E-7
5.0
6.0
7.0
8.0
9.0
10.0
11.0
12.0
13.0
Eb/No(dB)
12.01
Bit Error Rate
2.570E-8
Data Rate(Khz)
2048.00

MCDD Project

7/27/93 6:03 AM

TRW

Signal/Noise Power Specification

Start Eb/No: 8

Eb/No Increment: 1

# of Points: 6

NBC Select: 1

Waveform Generation Parameters

Total # of Channels: 3

Channel Configuration: NB NB NB

Selected Channel: Center

NB Channel Select: 1

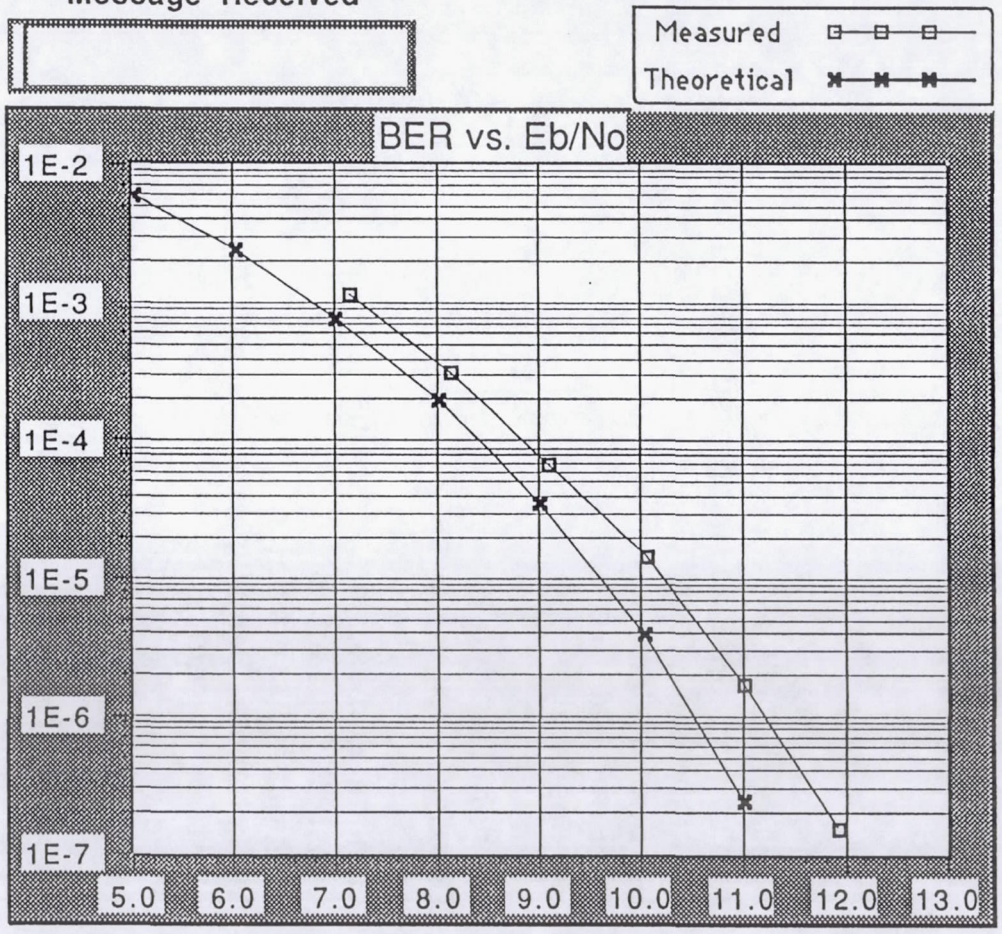
Frequency Offset (Mhz): 0.000000

Symbol Rate Offset (Mhz): 0.000000

Baseband Data Sequence: Pulse-Shaped PRN (127 length)

Notes

Message Received



Eb/No(dB): 11.93

Bit Error Rate: 1.540E-7

Data Rate(Khz): 64.00

6.0 ACRONYMS

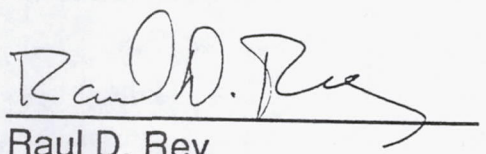
A/D	Same as ADC.
ADC	Analog to Digital Converter.
ASIC	Application Specific Integrated Circuit.
AWG	Arbitrary Waveform Generator.
BER	Bit Error Rate.
BERT	Bit Error Rate Tester.
BPF	Bandpass filter.
BW	Bandwidth.
CT	Carrier Tracking
DDR	Detailed Design Review.
FTP	File Transfer Protocol.
GPIB	General Purpose Interface Bus.
LSB	Least Significant Bit.
MAC	Multiplier Accumulator.
MCDD	Multichannel Demultiplexer Demodulator.
MSB	Most Significant Bit.
NBC	Narrowband Channelizer.
NB	Narrowband.
NCO	Numerically Controlled Oscillator.
PDR	Preliminary Design Review.
POC	Proof of Concept.
PRN	Pseudo Random Noise
RF	Radio Frequency.
SS	Symbol Synchronization
STE	Special Test Equipment.
WBC	Wideband Channelizer.
WB	Wideband.
WPA	Window/Presum ASIC.

MCDD Project

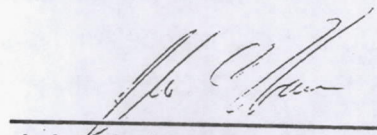
TRW

DETAILED DESIGN REPORT

12 June 1991



Raul D. Rey
SCD Review Board



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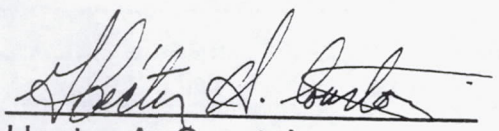
Advanced Processor
Technology Department Manager



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Ron Smith
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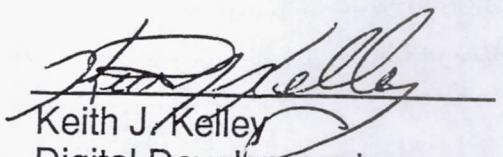
Synthesis Department Manager



Keith J. Kelley
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Laboratory Manager

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1.0 INTRODUCTION

1.1 Overview

This Detailed Design Report satisfies the requirements specified in Section 2.3 of the MCDD Statement of Work with the following exceptions:

a) RAM for the Demultiplexer Channelizers has not yet been selected.
b) Pinout for the WPA ASIC is not yet know.
c) Due to a) and b) above, layout of the Demultiplexer has not been completed.

The completed Demux Detailed Design will be presented and submitted as an addendum to this document at the ASIC Critical Design Review.

The MCDD project is partitioned into two major subtasks, a System Engineering task and a Hardware Development task.

The aim of the System Engineering effort is to:

- Validate the MCDD proposal assumptions
- Define performance parameters
- Define system requirements and constraints

The development of the MCDD Proof of Concept (POC) model and the Special Test Equipment (STE) has as its objectives:

- Demonstrate its capability to demultiplex and demodulate FDMA uplinks
- Show expandability to thousands of channels
- Carry out performance tests
- Establish a database for the next phase of MCDD
- Initiate development of components critical to a future flight implementation

Section 2 of this report summarizes the results of MCDD's System Engineering phase including Concept Development and POC Performance Specification. Section 3 provides an overview of both the POC and STE. Sections 4, 5 and 6 cover the

Demultiplexer, Demodulator and STE respectively. Section 7 covers the Test Plan and Procedures and Section 8 covers the MCDD Work Plan.

1.2 Requirements Flowdown Approach

Requirements as specified in the MCDD Statement of Work (SOW) have been mapped to MCDD derived requirements.

Concept and Performance MCDD requirements are derived solely from the SOW and the remaining MCDD requirements were derived both from the SOW and System Engineering results.

Table 1.2-1 lists the mapping of MCDD SOW vs. MCDD derived requirements.

All MCDD derived requirements are flowed down to one or more of the following:

- Concept Development/Performance Specification (Section 2)
- POC/STE Design and Performance (Section 3)
- MCDD Demultiplexer (Section 4)
- MCDD Demodulator (Section 5)
- MCDD STE (Section 6)

Each MCDD derived requirement is in turn addressed in each of the above sections in a Requirement vs. Capabilities table.

Table 1.2-1 SOW vs. MCDD Derived Requirements

SOW Sect	SOW REQUIREMENT	REQID	MCDD DERIVED REQUIREMENT	DDR Sect
	Concept General Requirements			
3.1.1 (a)	Simultaneously demultiplex and demodulate an FDM composite input signal	1	Simultaneously demultiplex and demodulate an FDM composite input signal	System Eng
3.1.1 (a)	Composite input signal shall consist of hundreds to thousands of narrow band (NB) channels and tens of wideband (WB) channels	2	Composite input signal shall consist of hundreds to thousands of narrowband (NB) channels and tens of wideband (WB) channels	System Eng
3.1.1 (b)	The NB input channels shall have a data throughput rate of 64 Kbps	3	The NB input channels shall have a data throughput rate of 64 Kbps	System Eng
3.1.1 (c)	The WB channels shall have a data throughput rate of at least 24 times that of the NB channels	4	The WB channels shall have a data throughput rate of at least 24 times that of the NB channels	System Eng
3.1.1 (d)	Individual input channels shall have a maximum dynamic range of 8 dB	5	Individual input channels shall have a maximum dynamic range of 8 dB	System Eng
3.1.1 (e)	Concept shall take into consideration future technology availability, and size, mass, and power tradeoffs for a flight model for year 2000	6	Concept shall take into consideration future technology availability, and size, mass, and power tradeoffs for a flight model for year 2000	System Eng
3.1.1 (f)	Techniques of POC shall not preclude future flight model	7	Techniques of POC shall not preclude future flight model	System Eng

Table 1.2-1 SOW vs. MCDD Derived Requirements (Cont'd)

SOW Sect	SOW REQUIREMENT	REQID	MCDD DERIVED REQUIREMENT	DDR Sect.
	Performance Parameters			
	Supply optimized performance goals for:			
3.1.2 (a)	Modulation scheme	8	Modulation scheme	System Eng
3.1.2 (a)	Implementation loss from theory of proposed modulation scheme	9	Implementation loss from theory of proposed modulation scheme	System Eng
3.1.2 (b)	Composite signal bandwidth efficiency	10	Composite signal bandwidth efficiency	System Eng
3.1.2 (c)	The required Eb/No to achieve a BER of 5x10 -7for both NB and WB channels with no adjacent channel interference (ACI)	11	The required Eb/No to achieve a BER of 5x10 -7for both NB and WB channels with no adjacent channel interference (ACI)	System Eng
3.1.2 (d)	The BER vs Eb/No with and without ACI for both NB and WB channels	12	The BER vs Eb/No with and without ACI for both NB and WB channels	Systems Eng
3.1.2 (e)	The minimum carrier, and symbol clock stabilities for both NB and WB channels	13	The minimum carrier, and symbol clock stabilities for both NB and WB channels	System Eng
3.1.2 (f)	The mechanism for acquisition and synchronization of newly activated NB and WB users	14	The mechanism for acquisition and synchronization of newly activated NB and WB users	System Eng
3.1.2 (g)	The grouping (distribution) of active NB and WB channels across the composite signal bandwidth	15	The grouping (distribution) of active NB and WB channels across the composite signal bandwidth	System Eng

Table 1.2-1 SOW vs. MCDD Derived Requirements (Cont'd)

SOW Sect	SOW REQUIREMENT	REQID	MCDD DERIVED REQUIREMENT	DDR Sect.
	POC and STE Requirements			
3.2.1 (a)	The POC model shall implement those enabling technologies deemed essential and critical to the MCDD concept and configured to allow testing and validation of critical components	16	The MCDD POC model shall implement and demonstrate the Time Domain FFT concept and its ability to perform wideband and narrowband channelization	Demux
		17	The MCDD POC model shall implement an SQPSK multirate demodulator	Demod
		18	The POC model shall be configured to allow testing and validation of its critical components	STE,POC Design & Performance
3.2.1 (b)	POC model and its design shall permit expanded designs for the MCDD concept	19	POC model shall fully demonstrate the MCDD concept and its architecture shall be expandable to a full MCDD	Demux, POC Design & Performance
3.2.1 (c)	POC model shall simultaneously demultiplex and demodulate a single FDM composite signal consisting of at least 2 WB and 4 NB input channels	20	The POC model FDM composite signal shall consist of 8 WB channels	Demux
		21	The POC model shall demultiplex and demodulate 3 WB channels, any of which can be further subdivided into 28 NB channels.	Demux, Demod
3.2.1 (c)	Provide mechanism which clearly indicates the correlation between the individual input channels and the output	22	The STE shall provide the capability of measuring BER on any of the demodulated channels	STE

Table 1.2-1 SOW vs. MCDD Derived Requirements (Cont'd)

SOW Sect	SOW REQUIREMENT	REQID	MCDD DERIVED REQUIREMENT	DDR Sect.
	POC and STE Requirements (Cont'd)			
3.2.1 (d)	The NB channels shall have a data throughput rate of 64 Kbps	23	The NB channels shall have a data throughput rate of 64 Kbps	Demux, Demod STE
3.2.1 (e)	The WB channels shall have a data throughput rate of at least 24 times that of the NB channels	24	The POC shall implement WB channels at 2.048 Mbps	Demux, Demod, STE
3.2.1 (f)	Individual input channels shall have a maximum dynamic range of 8 dB	25	STE shall provide a minimum dynamic range of 8 dB	STE
3.2.1 (g)	The POC and STE shall be housed in chassis or racks and include all necessary power supplies	26	The POC and STE shall be housed in a double bay rack and will include all necessary power supplies	POC design, STE
3.2.1 (h)	The interface between the POC model and the STE shall be clearly defined	27	The interface between the POC model and the STE shall be clearly defined	Demux, Demod, STE
3.2.1 (i)	The STE shall emulate the fully populated POC FDM composite signal	28	The STE shall emulate the fully populated POC FDM composite signal	STE
3.2.1 (j)	The STE shall provide BER measurements on individual NB and WB channels within the fully populated composite FDM signal	29	The STE shall provide BER measurements on individual NB and WB channels within the fully populated composite FDM signal	STE

Table 1.2-1 SOW vs. MCDD Derived Requirements (Cont'd)

SOW Sect	SOW REQUIREMENT	REQID	MCDD DERIVED REQUIREMENT	DDR Sect.
	Environmental Design Requirement			
3.2.2	The POC shall be designed for operation in a laboratory environment. Operating temperature range shall be 0 to 70 degrees centigrade	30	The POC model shall be fabricated with commercial grade components. Operating temperature range shall be 0 to 70 degrees centigrade	Demux, Demod
3.2.2	For any custom components designed for use in the POC model, best commercial design and fabrication practices shall apply	31	Best commercial design and fabrication practices will be used in the development of both the POC model and STE	Demux, Demod

Table 1.2-1 SOW vs. MCDD Derived Requirements

SOW Sect	SOW REQUIREMENT	REQID	MCDD DERIVED REQUIREMENT	DDR Sect.
	Testing ,Verification and Analysis			
3.3.1	Testing and analyses shall be sufficiently detailed to demonstrate the POC model performance and the ability of the POC model to meet the requirements of 3.2.1	32	The STE and Demodulator shall implement a linearly amplified SQPSK system	Demod, STE
		33	The POC Demux shall be designed with the following parameters: Presum ratio: 16 Decimation ratio: 16(WB), 32 (NB) Window length: 256 (WB), 512 (NB), Window type: Kaiser Window quantization: 16 bits Sampling frequency: 23.04MHz (WB), 1.44 MHz (NB) A/D resolution: 8 bits A/D loading factor: 1/4	Demux
		34	The full size MCDD Demux shall be designed with the following parameters: Presum ratio: 16 Decimation ratio: 64 (WB), 32 (NB) Window length: 1024 (WB), 512 (NB), Window type: Kaiser Window quantization: 16 bits Sampling frequency: 92.16 MHz (WB), 1.44 Mhz (NB) A/D resolution: 8 bits A/D loading factor: 1/4	

Table 1.2-1 SOW vs. MCDD Derived Requirements (Cont'd)

SOW Sect	SOW REQUIREMENT	REQID	MCDD DERIVED REQUIREMENT	DDR Sect.
	Testing ,Verification and Analysis			
3.3.1	Continued	35	The POC Demod shall be designed with the following parameters: Number of resampling filter taps: 16 Carrier track loop BW x symbol period: 10^{-2} Carrier track loop parameters: $K_L = 2^5, K_I = 2^{-1}, K_T = 2^4$ Sym sync loop BW x symbol period: 5×10^{-3} Sym sync loop parameters: $K_L = 2^7, K_I = 20, K_T = 2^8$ The POC performance shall be compared to the results of the simulation as follows:	Demod, STE
		36	The required Eb/No to achieve a BER of $5x\ 10^{-7}$ for NB and WB channels with no adjacent channel interference (ACI)	POC Design and Performance
		37	The BER vs Eb/No with ACI (8 dB dynamic range) for both NB and WB channels	POC Design and Performance

Table 1.2-1 SOW vs. MCDD Derived Requirements (Cont'd)

SOW Sect	SOW REQUIREMENT	REQID	MCDD DERIVED REQUIREMENT	DDR Sect.
	Testing ,Verification and Analysis			
3.3.1	Continued		The POC performance shall be compared to the results of the simulation as follows:	Demod, STE
		38	POC shall demonstrate its ability to acquire frequency offsets of 102.4 KHz for WB and 3.2 KHz for NB channels	POC Design and Performance
		39	POC shall demonstrate its ability to acquire clock rate offsets of 51.2 Kbps for WB and 1.6 Kbps for NB channels	POC Design and Performance
3.3.2	POC model performance analyses shall be sufficient to verify or deny the continued candidacy of the POC model for the MCDD concept	40	POC model performance analyses shall be sufficient to verify or deny the continued candidacy of the POC model for the MCDD concept	POC Design and Performance

2.0 CONCEPT DEVELOPMENT/PERFORMANCE ANALYSES REPORT

2.1 Introduction

This report covers details of the MCDD system engineering analysis carried out to confirm that the theoretical and practical performance estimates meet or exceed the original MCDD requirements as specified in TRW's technical proposal, 'Advanced Technology for a Satellite Multichannel Demultiplexer/Demodulator.' We have utilized our extensive BOSS (Block Oriented System Simulation Software Package) capability to perform functional simulations at the system level for MCDD concept refinement and hardware simulations at the logic level for POC design. This activity provided us with early design verification of the POC architecture as well as final selection of the MCDD POC operational parameters.

The MCDD concept uses time domain FFT channelization processing in a wideband/narrowband cascade for demultiplexing and a multirate demodulator which can process one wideband data stream or thirty-two narrowband data streams. This approach best fits the needs of frequency demultiplexing and most efficiently matches the processing capabilities of both current and future signal processing hardware.

TRW's POC (Proof of Concept) model fully demonstrates the signal processing functions of MCDD. The relationship of the POC model to the MCDD design is shown in Figure 2-1. The input bandwidth of the POC model is one-fourth that of the MCDD. Correspondingly, the A/D converter operates at one-fourth the sampling rate, and the wideband channelizer outputs eight channels rather than thirty-two. Any three of these channelizer outputs (rather than twenty-six as in the MCDD) are subsequently demodulated. Each narrowband channelizer can demultiplex a single wideband channelizer output into its twenty-eight usable 64 Kbps channels prior to demodulation. Thus, the POC model has the capability to process either three 2.048 Mbps channels or two 2.048 Mbps channels and twenty-eight 64 Kbps channels.

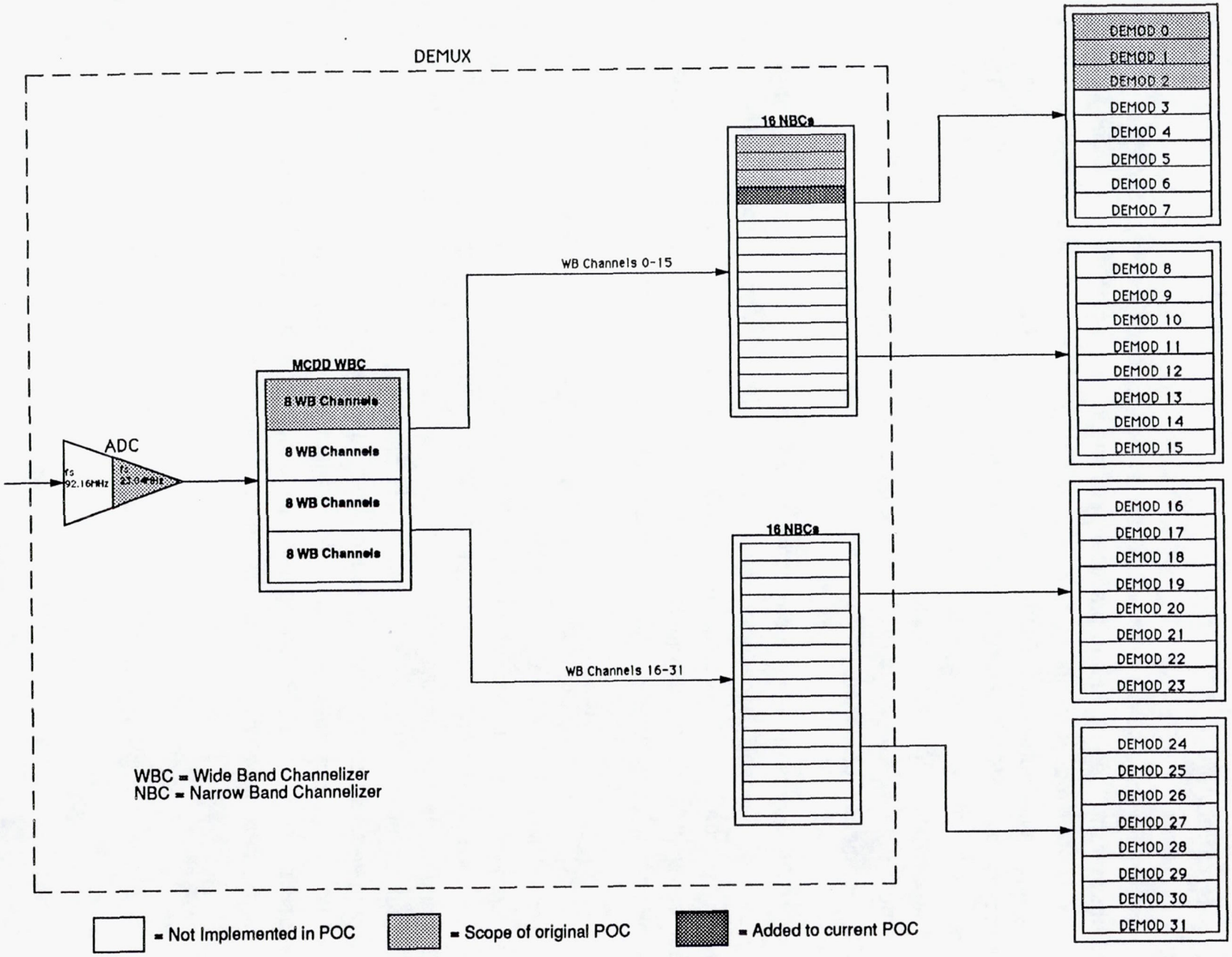


FIGURE 2-1: POC SUBSET OF MCDD

Our system engineering analysis of the POC model confirmed that the TRW MCDD concepts are not only achievable but also balance the joint goals of minimizing on-board complexity and cost of ground equipments while retaining the flexibility needed to meet a wide range of system requirements. An overview of important MCDD system engineering issues is presented in Sections 2.1 through 2.4. Section 2.5 discusses some of the BOSS simulation analyses performed for design verification as well as for selecting operational parameters of the POC model. Summary of the selected parameters and capabilities of the MCDD POC model with respect to the overall MCDD concept requirements is shown in Section 2.6. Section 2.6 also considers the issue of system synchronization and the modulation trade study for future MCDD.

2.2 MCDD Requirements

Specific requirements for the MCDD are listed below.

- Host satellite bus shall be in geostationary orbit.
- Ground terminals shall be stationary.
- Frequency division multiplex (FDM) composite uplink input signal shall consist of hundreds to thousands of narrowband (NB) data channels and/or tens of wideband data (WB) channels.
- Downlink signal shall be time division multiplexed (TDM).
- Narrowband channel data rate shall be 64 Kbps.
- Wideband channel data rate shall be at least 24 times greater than the narrowband data rate (i.e., 1536 Kbps minimum).
- Dynamic range variation between individual channels shall be at most 8 dB.
- Bit error rate (BER) shall be 5×10^{-7} or better per channel.
- Design/build readiness for a flight model shall be reached by the year 2000.

In addition, the MCDD is subject to the three following general requirements:

- Ground terminal complexity and costs shall be minimized, particularly narrowband user terminals, considering the large number of such terminals.

- Satellite communication system constraints shall be minimized.
- System performance shall be maximized with regard to measures such as demodulation implementation loss from theory, FDM composite signal bandwidth efficiency, BER vs Eb/No with and without adjacent channel interference, carrier and symbol clock stabilities, and complexity of new user initialization schemes.

2.3 MCDD Configuration within a VSAT Communication Systems

The TRW MCDD configuration is summarized in Table 2-1. The flexible and bandwidth-efficient FDM composite signal structure, differentially encoded/ coherent demodulated QPSK data modulation type, and synchronous system operation were chosen based on our space communication system engineering experience and trade studies, e.g., TDRSS, MILSTAR, etc.

The flexibility and performance of our MCDD concept result from extensive work in advanced digital signal processing for spacecraft payloads. Virtually no constraints are imposed by our FDM composite signal structure, which is feasibly implementable on board due to our efficient wideband/narrowband channelization cascade.

Our coherent QPSK demodulator, implementable on-board in advanced VLSI, offers robust operation with imperfect user synchronization.

Synchronous network operation greatly simplifies data routing and TDM modulation operation with the possible elimination of requirements for elastic buffers and bit stuffing. The MCDD hardware itself is economized by enabling time division multiplexing of hardware and data lines and the elimination of separate clock interfaces for every demodulated channel.

Ground terminal complexity is also reduced with synchronous network operation by the elimination of costly frequency sources with very tight absolute accuracy at each ground terminal.

ITEM	SELECTED CONFIGURATION	FEATURE
• FDM COMPOSITE SIGNAL	• NB CHANNELS - 64 KBPS - 45 KHZ SPACING • WB CHANNELS - 2.048 KBPS - 1.44 MHZ SPACING • INPUT BW PER MCDD - 37.4 MHZ (1995) - 149.6 MHZ (2005)	• BW-EFFICIENT STANDARD RATES & SPACINGS • EXTREME FLEXIBILITY OF CHANEL ASSIGNMENTS - NB CHANNELS ANYWHERE ON 45 KHZ CENTERS - WB CHANNELS ANYWHERE ON 1.44 MHZ CENTERS
• MODULATION	• DIFF ENCODED COHERENTLY DEMODULATED QPSK	• 2.0 dB Eb/No GAIN RELATIVE TO DIFF COHERENT QPSK • DIFFERENTIAL ENCODING TO RESOLVE CARRIER PHASE AMBIGUITY
• ASYNCHRONOUS/ SYNCHRONOUS SYSTEM	• SYNCHRONIZED VSATS	• ELIMINATES ELASTIC BUFFERS & BIT STUFFING FOR TDMA DOWNLINK • REDUCES MCDD HARDWARE • TDM DOWNLINK DISTRIBUTES FREQ & TIME REFERENCES TO VSATS • ELIMINATES COSTLY REFS FOR EACH VSAT

Table 2-1 MCDD Selected Configuration

The TRW MCDD configuration within an overall VSAT communication system is shown in Figure 2-2. The FDM composite uplink structure, differentially encoded/coherent QPSK modulation and network synchronization schemes are described. In addition, the operational system will employ forward error correction. (Not shown here.)

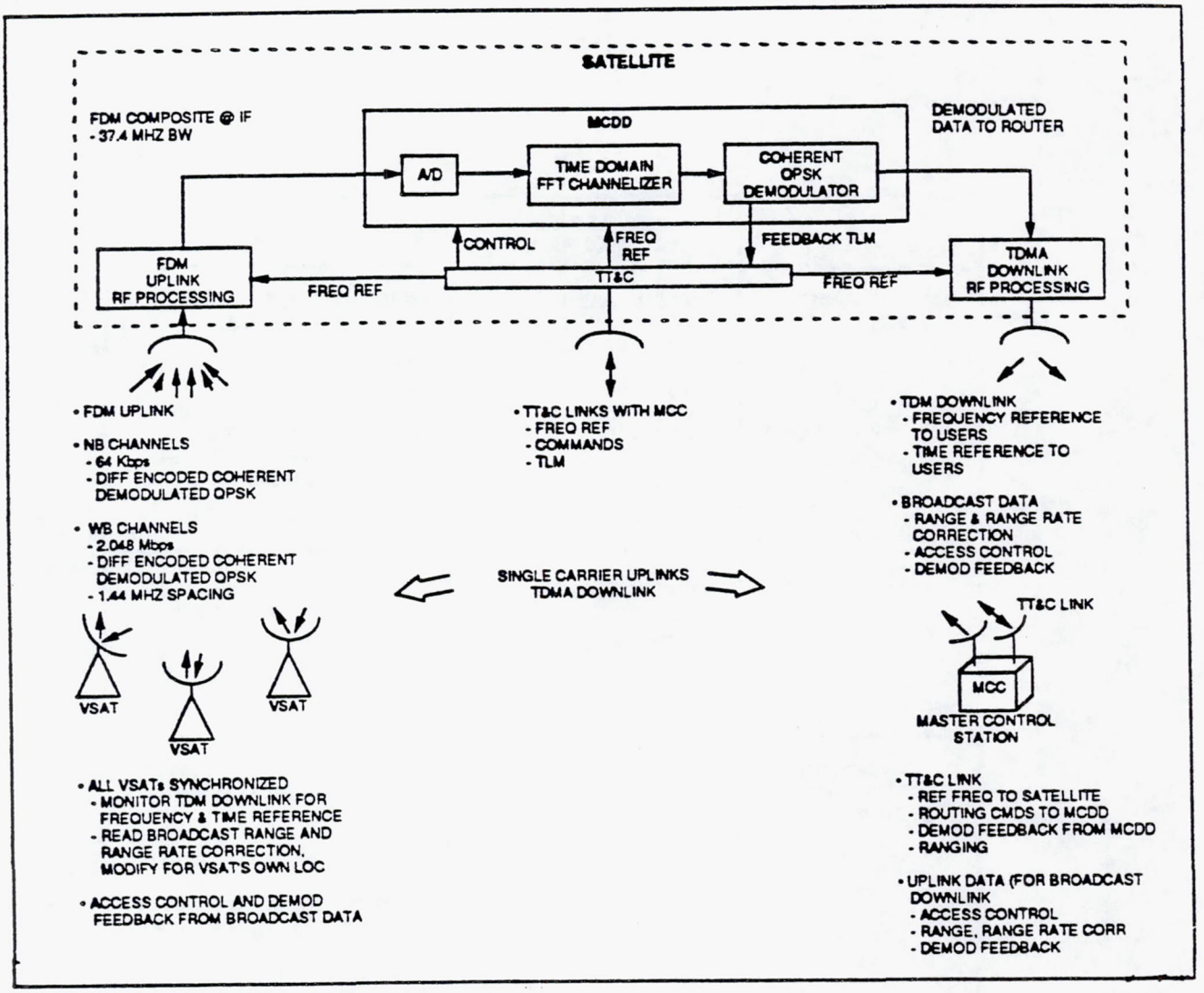


Figure 2-2 MCDD Configuration within a VSAT Communication System

2.4 MCDD Concepts and Architecture

The TRW MCDD, as shown in Figure 2-3, operates on a 37.4 MHz composite input signal. Individual channel data rates are either 64 Kbps or 2.048 Mbps. The demultiplexer divides the input signal into segments containing either a single 2.048 Mbps channel or thirty-two 64 Kbps channels. In the latter case, the narrowband channelizer further divides a wideband channel into its 64 Kbps components. Identical multirate demodulators are used to recover either the single 2.048 Mbps data stream or twenty eight 64 Kbps data streams (data from the four outer guard channels are discarded).

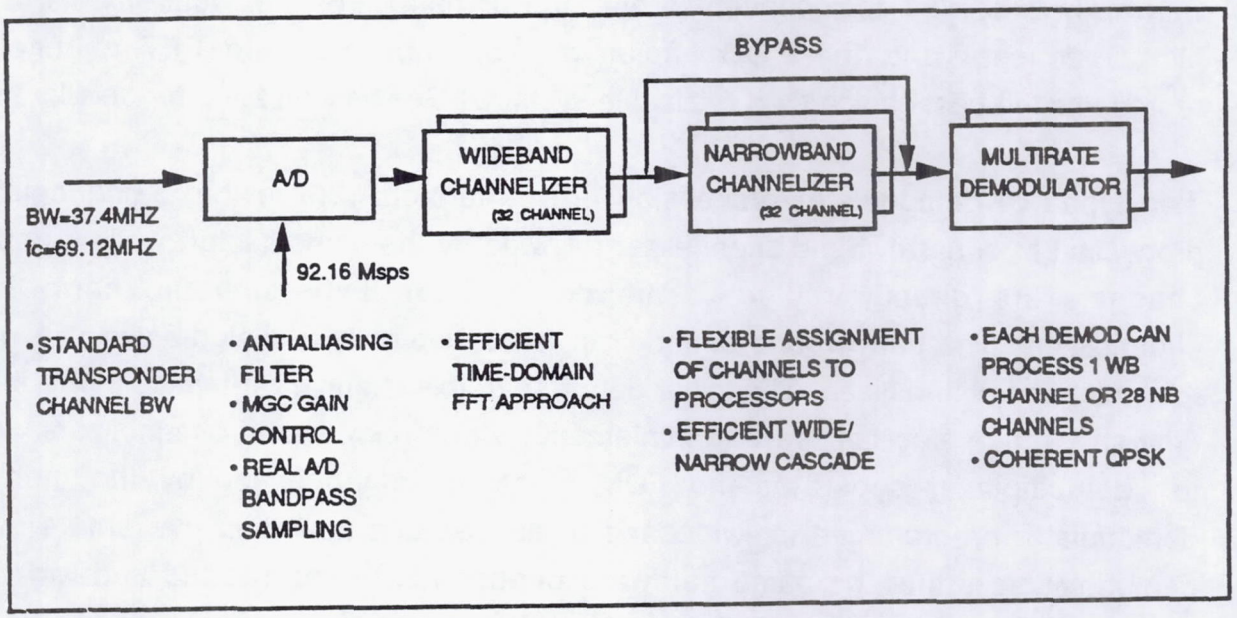


Figure 2-3 MCDD Block Diagram

With this approach the FFT processing capacity is matched well to the bandwidth and number of channels to be demultiplexed. By using a multirate demodulator, fewer demodulators are required while achieving greater flexibility. Each demodulator can process a wideband channel or twenty eight narrowband channels. We can demodulate all wideband channels, a mixture of wideband and narrowband channels, or all narrowband channels. A satellite implementation requires half the numbers of multirate demodulators than would be required if separate wideband and narrowband demodulators were used.

The MCDD concept proposed by TRW uses time domain FFT channelizing in a wideband/narrowband cascade. This algorithm processes the data in the time domain by performing window/presum followed by a single FFT to perform heterodyning of the signal. The FFT channelizer algorithm is important for its efficient use of FFT hardware to realize a parallel bank of filters. The alternative approach is based on a large FFT fast convolution which converts the input signal to the frequency domain through an FFT algorithm, performs window filtering on the frequency samples and follows this

with an inverse FFT to reconvert to the time domain. For the requirements of the MCDD concept and the POC implementation, however, the FFT channelizer represents the best choice for a realizable system. See section 2.4.2 for details.

Two types of demodulator processing are performed. Narrowband channels are processed by a narrowband channelizer followed by the demodulator, while wideband channels are directly routed to the demodulator, bypassing the narrowband channelizer. The narrowband channelizer is conceptually a scaled-down version of the wideband channelizer. The lower data rate of this channelizer makes it possible to time-share the same hardware to implement sixteen narrowband channelizers. After the demultiplexer separates the FDM signal, it is processed by the multirate demodulator programmed for wideband or narrowband operation. A feature of the demodulation is that the same hardware performs both narrowband and wideband functions, with a programmable control word determining the operating mode.

The demodulator consists of five functional blocks. The resampling filter takes data that is input with a sampling rate of 1.406 times the symbol rate and increases this to two complex samples per symbol to make the demodulator processing straightforward. With feedback from the symbol sync circuit, these two samples per symbol are timed so that they occur at mid-symbol and at the symbol transition. Following the resampling filter, the derotate circuit corrects for any residual uplink channel frequency and phase error.

Derotation is performed with a quadrature multiply of the oversampled data by a phase error estimate value. The phase error estimate is obtained by averaging the residual phase in a second order type II loop after a symbol decision in the carrier tracking circuit. The derotated signal is passed through a symbol decision circuit that outputs two binary bits. In this manner, a single wideband or twenty eight interleaved narrowband channels are demodulated to recover the binary data. Details now follow.

2.4.1 MCDD Frequency Plan

The TRW MCDD concept embodies a multistage approach to accommodate different channel bandwidths. (See Figure 2-4.) Each MCDD operates on a digitized 37.4 MHz bandwidth segment. The initial stage provides channelization into thirty two wideband 1.44 MHz channels corresponding to the wideband data rate, which has been set at 2.048 Mbps. The signal at this point is either demodulated directly or fed to a second channelizer which subdivides the signal into thirty two 45 KHz channels corresponding to the 64 Kbps narrowband channel rate. In the latter case, the output of the second channelizer is fed to a demodulator which is identical to that used for the wideband channel. This single demodulator recovers all of the 64 Kbps data streams. Thus, only a single demodulator needs to be provided for each 1.44 MHz subsegment of the input spectrum, regardless whether the subsegment contains a single 2.048 Mbps channel or thirty two 64 kbps channels.

The narrowband channel spacing is chosen to be 45 KHz to satisfy the evolutionary system concept and maximum FDM composite signal bandwidth efficiency requirements. Smaller channel spacings place undue frequency and doppler compensation requirements on the user ground terminals. Larger channel spacings are not only inefficient, but make the typical frequency generation components in the ground terminals unusable. The wideband channel data rate is constrained to be at least 24 times the narrowband channel rate of 64 Kbps for a minimum rate of 1.536Mbps. Satisfying this requirement, the chosen WB channel data rate is 2.048 Mbps. The wideband channel spacing is chosen to be 1.44 MHz to maximize the composite FDM signal bandwidth efficiency. The same ratio of maximum bit rate to channel spacing is maintained for the wideband channels as for the narrowband channels (2.048 Mbps/1.44 MHz = 64 Kbps/45 KHz). The rate and channel spacing enables a very efficient algorithm to be used within the MCDD for demultiplexing.

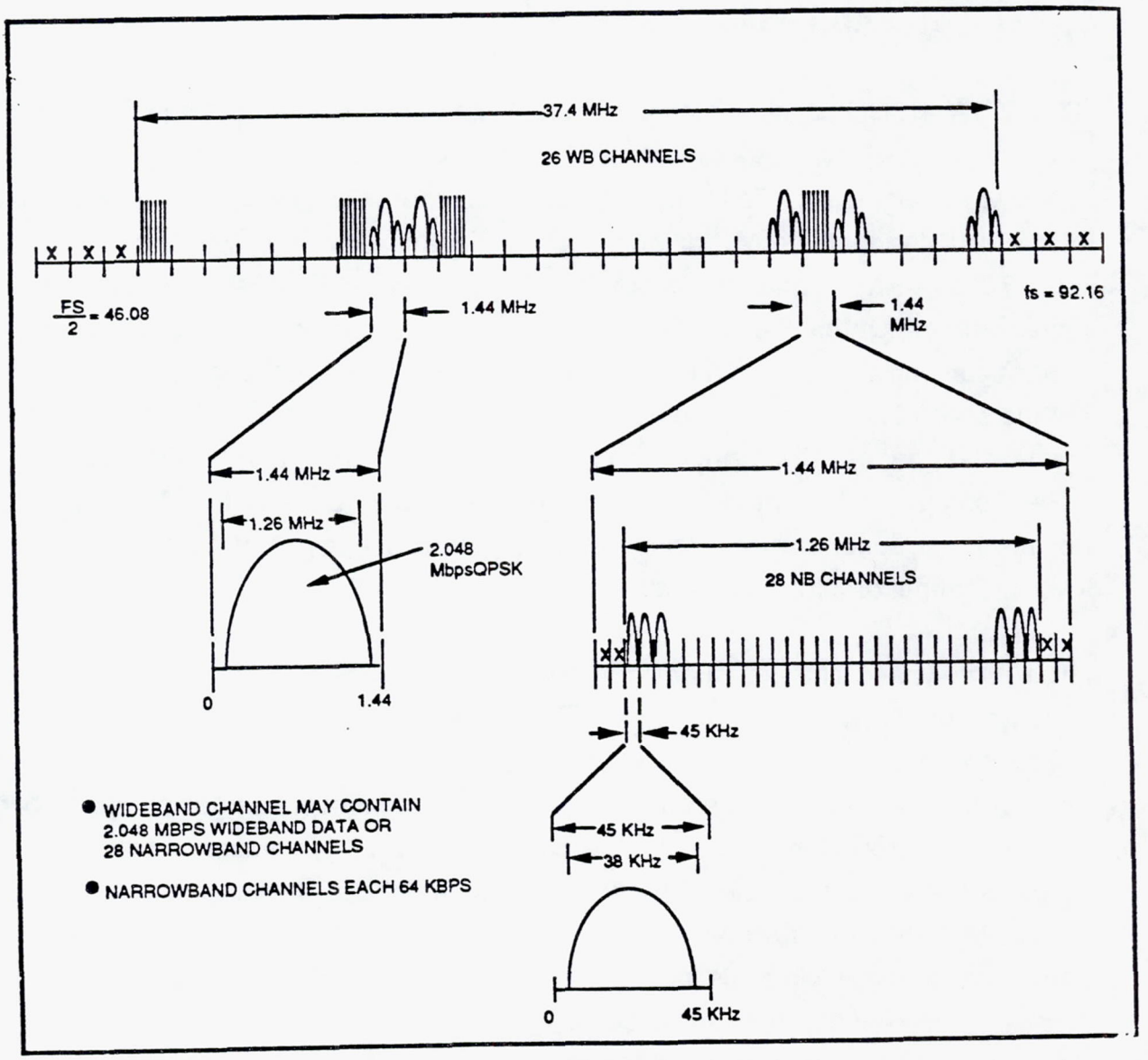


Figure 2-4 MCDD Frequency Plan

2.4.2 The Channelizer Design

Suppose we require a bank of N complex bandpass filters with equally spaced center frequencies from [DC to f_S), the impulse response of the *k*th filter, $h_k(n)$, can be written in terms of a complex modulated lowpass filter w(n)

$$h_k(n) = w(n)e^{-j\left(\frac{2\pi}{N}\right)kn} \qquad ; k=0,..N-1 \qquad (2.4.1)$$

The Fourier transform shows that the frequency response of the *k*th filter is a frequency shifted version of lowpass filter's frequency response.

$$H_k(e^{j\omega}) = W\left(e^{j\left(\omega+\frac{2\pi}{N}k\right)}\right) \qquad ; k=0,...,N-1 \qquad (2.4.2)$$

Thus, the *k*th output $y_k(n)$ is given by the convolution

$$y_k(n) = x(n) * h_k(n) \qquad ; k=0,...,N-1$$

or

$$y_k(n) = \sum_{m=-\infty}^{\infty} x(n-m)w(m)e^{-j(\frac{2\pi}{N}km)} \qquad ;k=0,...,N-1 \qquad (2.4.3)$$

By making substitution : m=Nr+q with q=0,...,N-1 and $-\infty \le r \le \infty$, we can express equation (2.4.3) as a double sum

$$y_k(n) = \sum_{q=0}^{N-1}\left[\sum_{r=\infty}^{\infty} x(n-Nr-q)w(Nr+q)\right]e^{-j\frac{2\pi}{N}kq}$$

since

$$e^{-j\left(\frac{2\pi}{N}kq\right)} = e^{-j\left(\frac{2\pi}{N}k(Nr+q)\right)} \qquad ;k=0,...,N$$

or equivalently,

$$y_k(n) = \sum_{q=0}^{N-1} [U_n(q)]e^{-j\frac{2\pi}{N}kq} \qquad ;k=0,...,N-1 \qquad (2.4.4)$$

where

$$u_n(q) = \sum_{r=-\infty}^{\infty} x(n - Nr - q)w(Nr + q) \qquad ;q=0,...,N-1 \qquad (2.4.5)$$

Equation (2.4.5) is called the presum operation and becomes a finite sum for finite window length. Figure 2-5 shows a block diagram of the time domain FFT channelizer which represents the above derivation.

Channelizer performance depends principally on the following factors: window type, presum ratio, and quantization effects, etc. During our system engineering analysis, we have utilized the BOSS simulation tools in choosing the type of window and presum ratio which provide the desired channel shape. We have chosen the Kaiser window for its flat passband response as well as the stopband attenuation satisfying the ACI rejection when the interfering signal power at both adjacent channels are 8 dB higher than that of the desired signal.

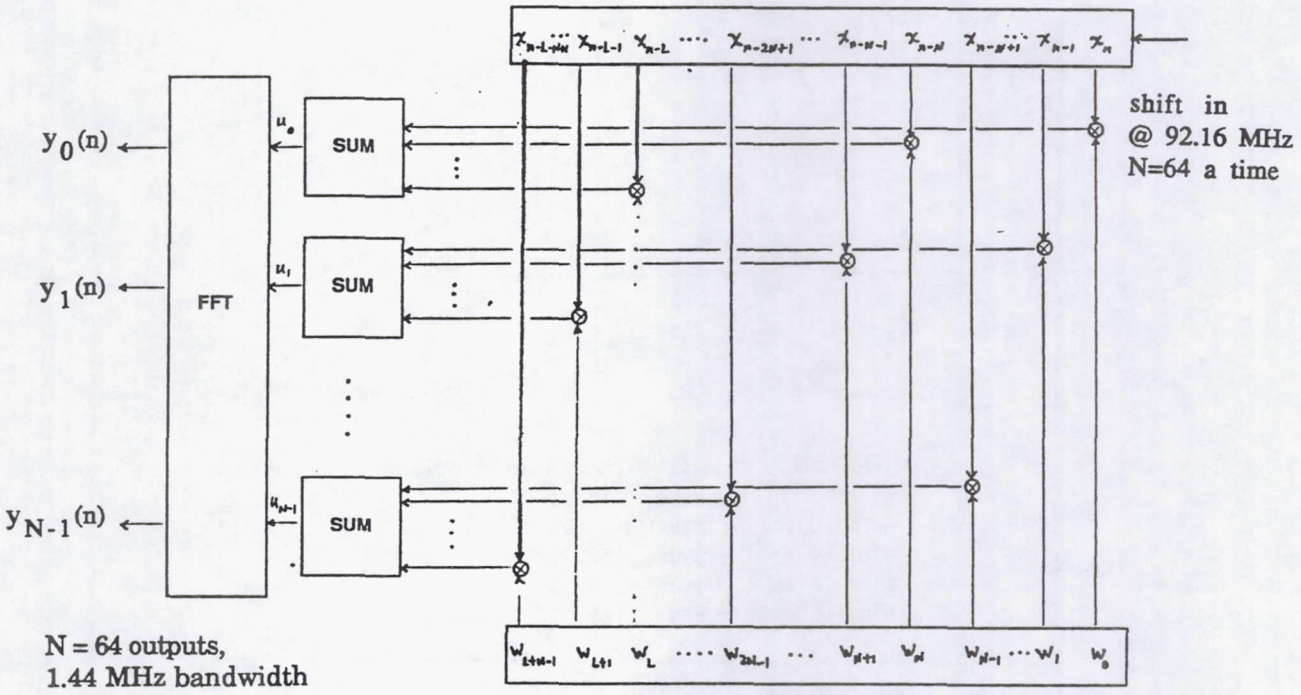


Figure 2-5 Time Domain FFT Channelizer

Figure 2-6 shows the percentage of mainlobe that can go through the narrowband channelizer (3 dB bandwidth of the filter divided by that of the mainlobe) using Kaiser window with different presum ratios. An example of the channel shape vs. presum ratio using Kaiser window is also shown in Figure 2-7. Furthermore, the number of bits for presum window coefficients should be chosen so that an acceptable quantization level can be obtained without sacrificing computational efficiency. Details of the BOSS simulation analysis are shown in Section 2.5.

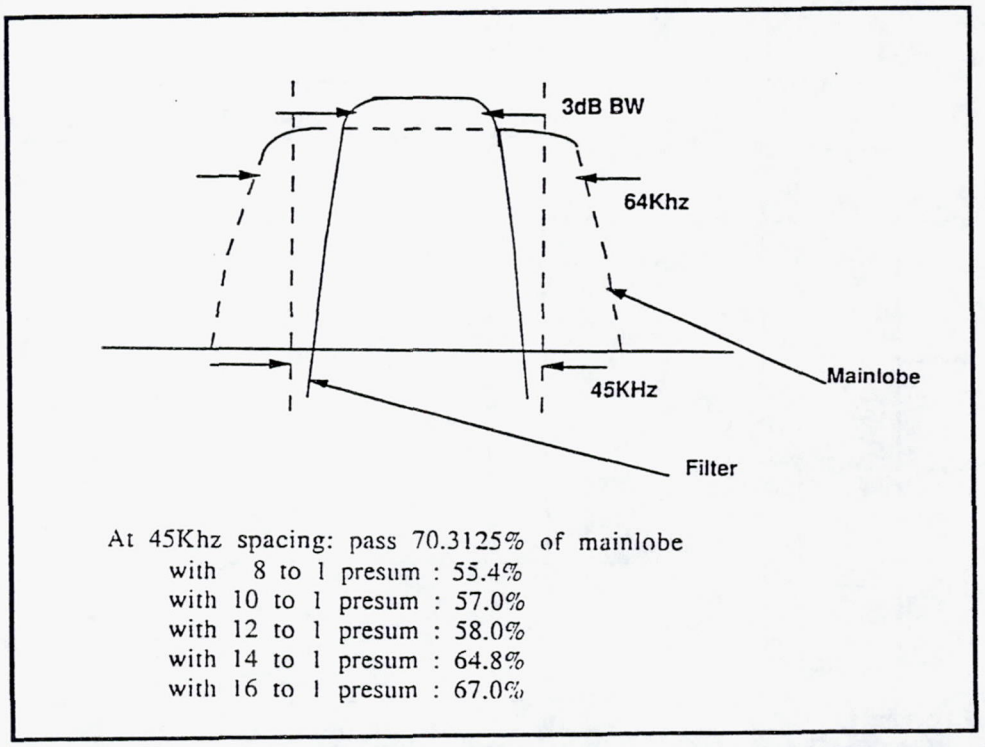
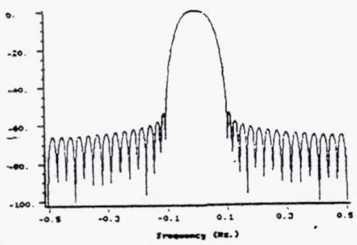
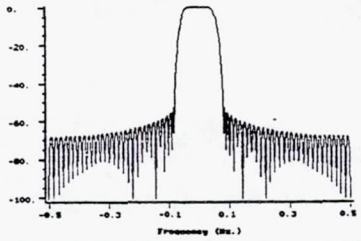


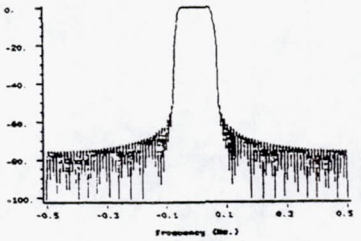
Figure 2-6 Percentage of the Passing Mainlobe vs. Presum Ratio



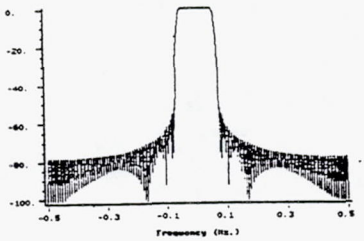
(a) 4 to 1 Presum



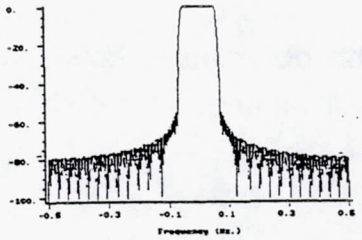
(b) 8 to 1 Presum



(c) 12 to 1 Presum



(d) 16 to 1 Presum



(e) 20 to 1 Presum

Figure 2-7. Channel Shape vs. Presum Ratio

2.4.3 Channel Modulation & Pulse Shaping

Bandwidth constraint is an important consideration in communication satellite designs. The MCDD design is intended to accommodate data rates up to 2.048 Mbps and 64 Kbps in the wideband and narrowband channels, respectively. The wideband channel has a channel center to center separation of 1.44 MHz. With the allocation of guard bands between channels, the usable communication bandwidth for each wideband channel is only 1.26 MHz. The center to center separation for the narrowband channels is 45 KHz. The usable communication bandwidth is 38 KHz for each narrowband channel. The allocations require a modulation scheme with a bandwidth efficiency exceeding 1.625 bits per sec per Hz. A bandwidth efficient modulation or combined modulation/coding technique is thus necessary for the MCDD application which will also be power efficient and will create minimal ACI and ISI degradations.

QPSK is frequently used in TDMA single channel per carrier digital satellite systems. It has a 2 bits per second per Hz theoretical bandwidth efficiency (1.5 to 1.8 bits/sec/Hz practical), low Eb/No requirements for good BER performance and relatively simple implementation. In a multiple carrier FDMA application, however, QPSK is not desirable because the power spectrum of a QPSK signal exhibits side lobes that may interfere with adjacent channels. Transmit filtering for side lobe control at the high power amplifier (HPA) output is usually not practical because the channel bandwidth is usually very small compared to the RF frequency, and requires the bandpass filter to have an exceedingly high Q which is not achievable. Filtering at the IF would create envelope fluctuations which results in spectral spreading at the HPA output due to AM/AM and AM/PM effects of the HPA nonlinearity.

Staggered QPSK (SQPSK) has relatively lower side lobes after undergoing nonlinear amplification. The main difference between conventional QPSK and SQPSK is in the alignment in the I and Q baseband symbols in the modulated signal. This difference in time alignment does not change the power spectral density of the modulated signal, and hence in linear channels both QPSK and OQPSK spectra have the same shape. However, the two modulated signals respond differently when they undergo bandlimiting and then nonlinear amplification. Because of the coincident alignment of

the two baseband components in QPSK, an instantaneous phase transition of 180 degrees can take place; hence the bandlimited QPSK signal exhibits 100 percent envelope fluctuation. In SQPSK, on the other hand, the two baseband signals cannot change their states simultaneously. This eliminates the possibility of instantaneous phase transitions of 180 degrees. Thus the bandlimited SQPSK signal has a much smaller envelope fluctuation than the QPSK signal. Consequently, the HPA nonlinear amplification will not regenerate the undesired high frequency components originally removed by the bandlimiting filter.

SQPSK modulation was thus considered in the initial phase of the MCDD POC development. Figures 2-8(a) and 2-8(b) shows the spectra of a single SQPSK signal, and the same signal with two adjacent channel signals 8 dB stronger than the desired signal. Figures 2-9(a) and 2-9(b) compare the matched filter output spectra of the same channel with and without the presence of adjacent channel interference (ACI). Distortion due to ACI at the matched filter output is clearly present. The degradation on BER due to ACI is significant with either QPSK or SQPSK. (See Figure 2-10.)

To mitigate the effects of intersymbol interference (ISI), and simultaneously, the effects of ACI due to bandlimiting in the channelizer, baseband pulse shaping is applied to the SQPSK I and Q symbol pulses. In particular, the pulse shaping function is a raised cosine response equally split between the transmitter and the receiver matched filter, i.e., square root raised cosine response for each. The roll-off factor α is chosen to be 0.3.

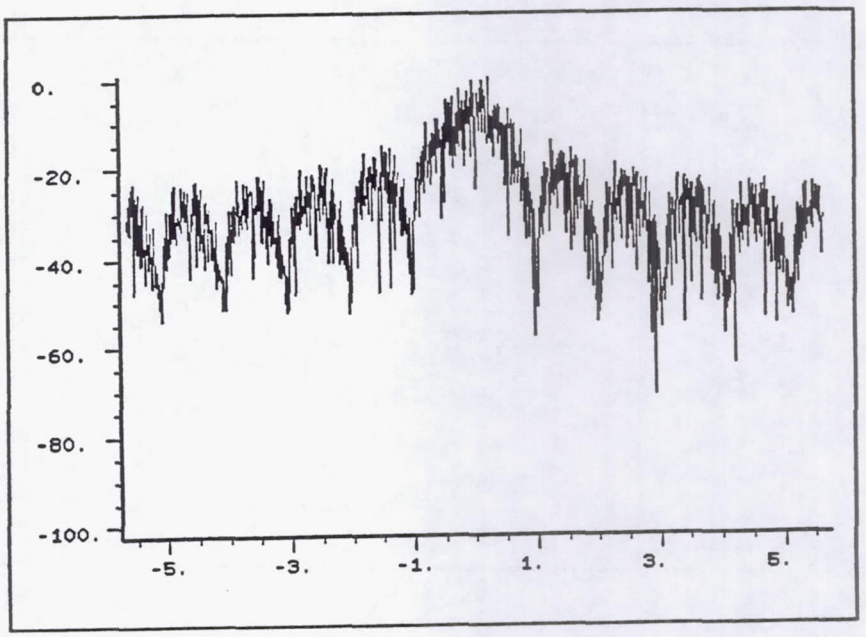


Figure 2-8(a) Power Spectrum of SQPSK without Adjacent Channel Interference

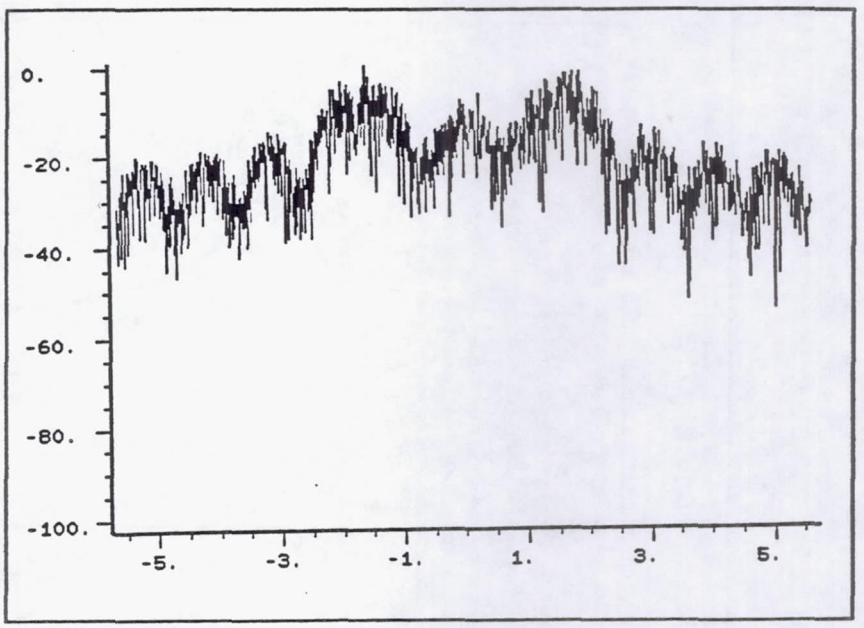


Figure 2-8(b) Power Spectrum of SQPSK with Two Adjacent Channel Signals 8 dB Higher in Power than the Desired Signal.

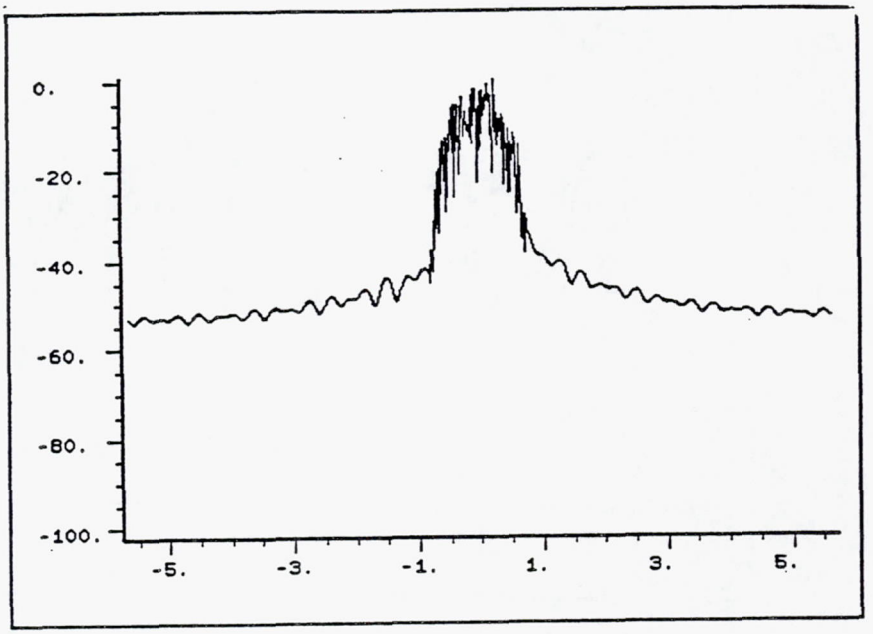


Figure 2-9(a) Power Spectrum of Matched Filter Output: without Adjacent Channel Interference

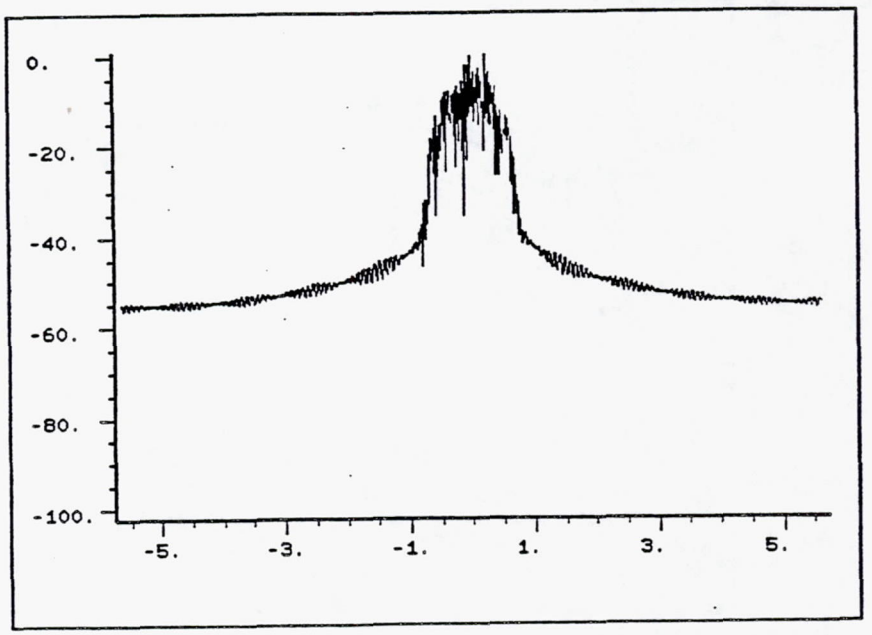


Figure 2-9(b). Power Spectrum of Matched Filter Output: with Two Adjacent Channel Signals 8 dB Higher in Power than the Desired Signal.

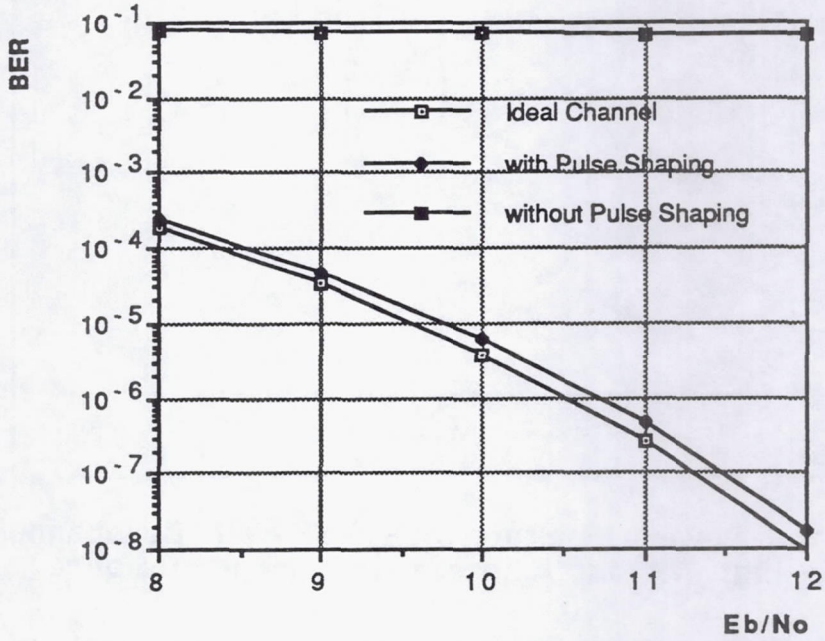


Figure 2-10. BER Degradation due to ACI with and without Pulse Shaping

Figures 2-11(a) and 2-11(b) show the spectra of a SQPSK signal with pulse shaping, and the same with two pulse-shaped adjacent channel signals with 8 dB higher in power, respectively. Figures 2-12(a) and 2-12(b) show the spectra of the matched filter outputs of the desired channel without and with the presence of ACI. The effect of ACI is evidently reduced as compared to that of the SQPSK without pulse shaping as illustrated in Figure 2-9(b). With pulse shaping, the Eb/No degradation of the MCDD is less than 0.25 dB at 5×10^{-7} BER, as illustrated in Figure 2-10, and the effect of ACI is completely mitigated by baseband pulse shaping.

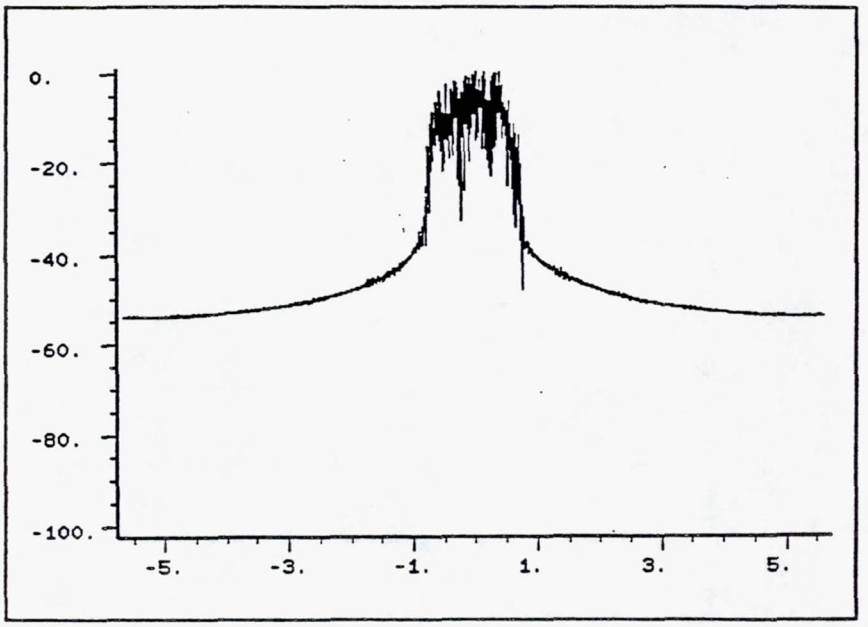


Figure 2-11(a) Power Spectrum of SQPSK with Baseband Pulse Shaping: Without Adjacent Channel Interference

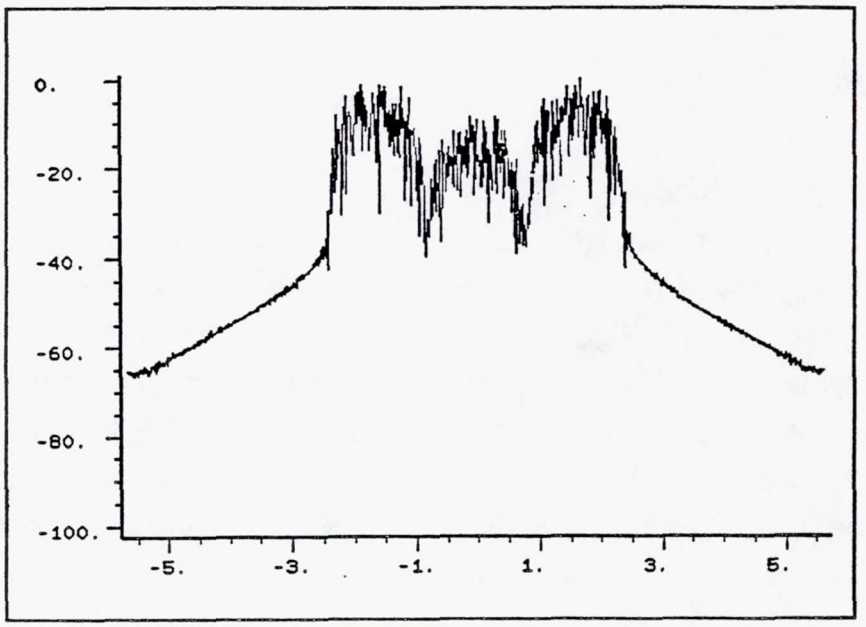


Figure 2-11(b) Power Spectrum of SQPSK with Baseband Pulse Shaping: With Two Adjacent Channel Signals 8 dB Higher than the Desired Signal.

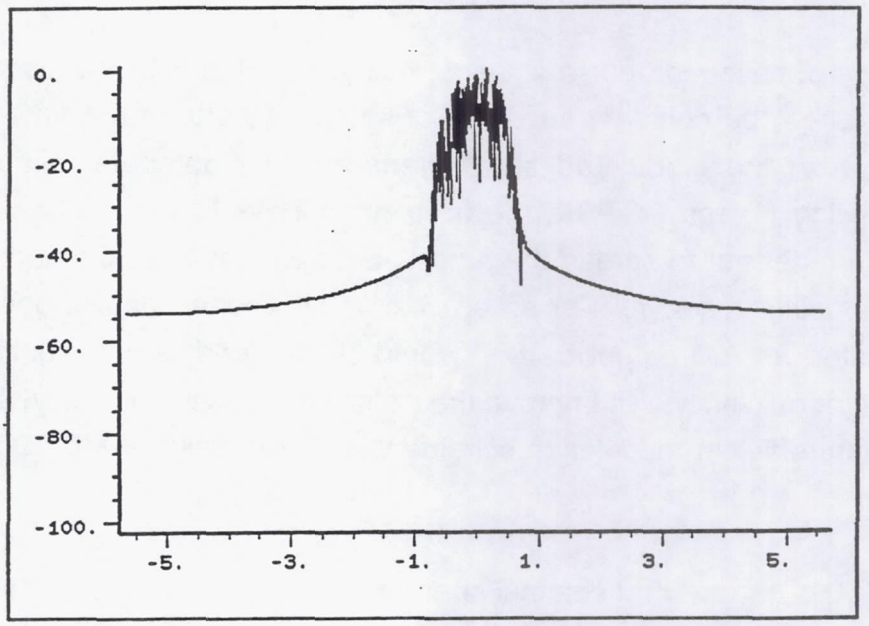


Figure 2-12(a). Power Spectrum of Matched Filter Output with Baseband Pulse Shaping: without Adjacent Channel Interference

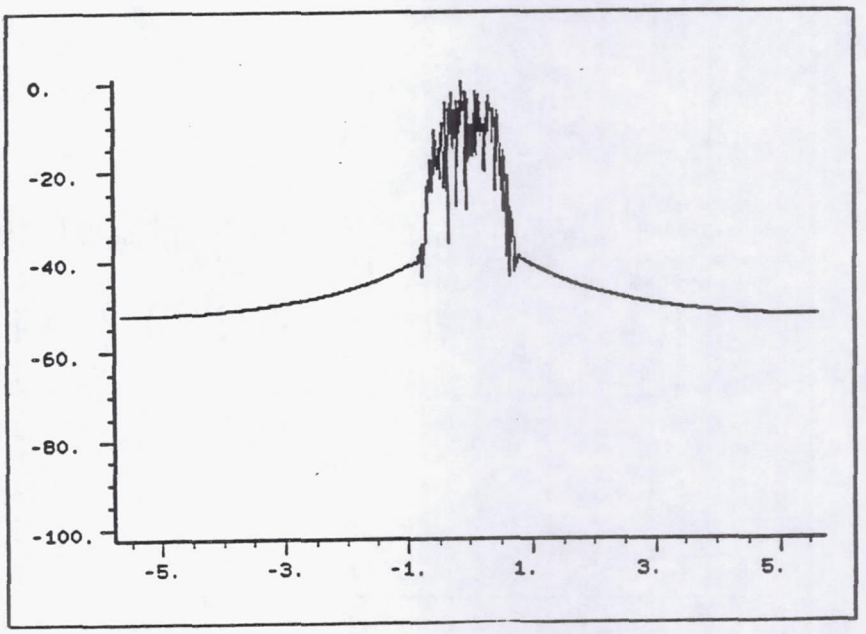


Figure 2-12(b). Power Spectrum of Matched Filter Output with Baseband Pulse Shaping: with Two Adjacent Channel Signals 8 dB Higher Power

This type of baseband pulse shaping, however, will result in a modulated signal which will no longer be constant-envelope. Figure 2-13 shows the time domain plot of the envelope of the modulated signal generated by computer simulation. Similar to bandlimiting filtered SQPSK, the transmitter HPA has to be backed off to its linear range in order not to spread the amplified output spectra. Sidelobe level is a function of the amplifier backoff. For an approximately linear mode of operation of a SQPSK transmitter, a 5 dB output backoff would be required, which significantly reduces the transmitter efficiency. To improve the transmitter power efficiency, a constant envelope bandwidth efficient modulation scheme will be required for MCDD in the future. (See Section 2.6.1.2.)

Our 45 KHz narrowband channel spacing matches that of one of the INTELSAT single-channel-per-carrier services which utilize linearly amplified QPSK. The current choice of SQPSK modulation is also related to the fact that all constant envelope bandwidth efficient modulation type, e.g., TFM, MSK, GMSK, are similar to pulse shaped SQPSK with differential encoding, so our demodulator can easily be used to demodulate with only a change to the resampling filter impulse response.

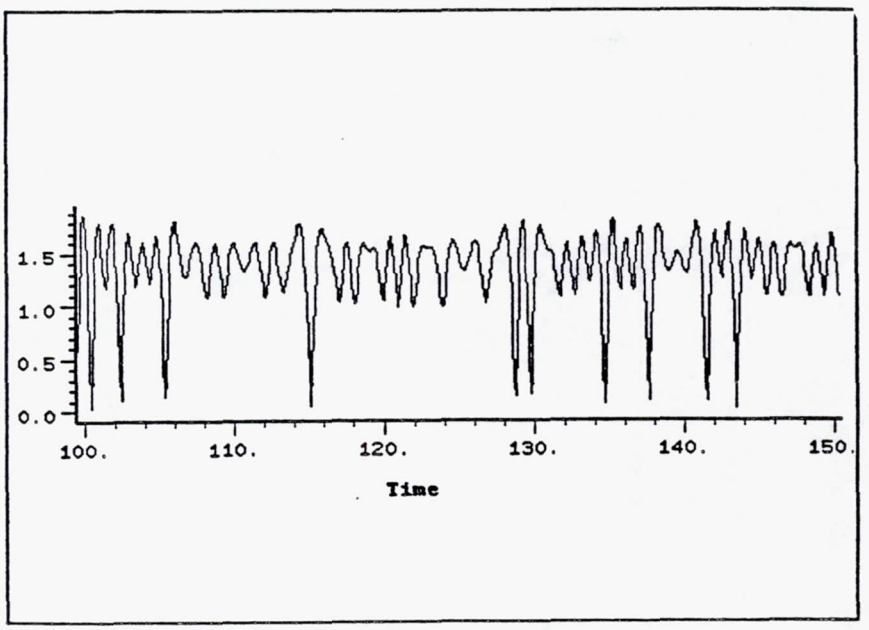


Figure 2-13. Normalized Envelope of Transmit Signal: SQPSK with Raised Cosine Pulse Shaping

2.4.4. The Demodulator Design

The multirate demodulator consists of five major functional blocks shown in Figure 2-14. These blocks are: a resampling filter to generate exactly two complex signal samples per symbol from the channelizer output of 1.406 samples per symbol and also matched filter the transmitted signal, a derotate complex multiply to remove residual carrier phase error from these samples, a symbol decision to determine the received two-bit symbol, a carrier tracking loop to estimate the carrier offset to be derotated, and a symbol sync loop to determine any timing offset to be removed by the resampling filter. A more detailed block diagram of the Demodulator is shown in Figure 2-15.

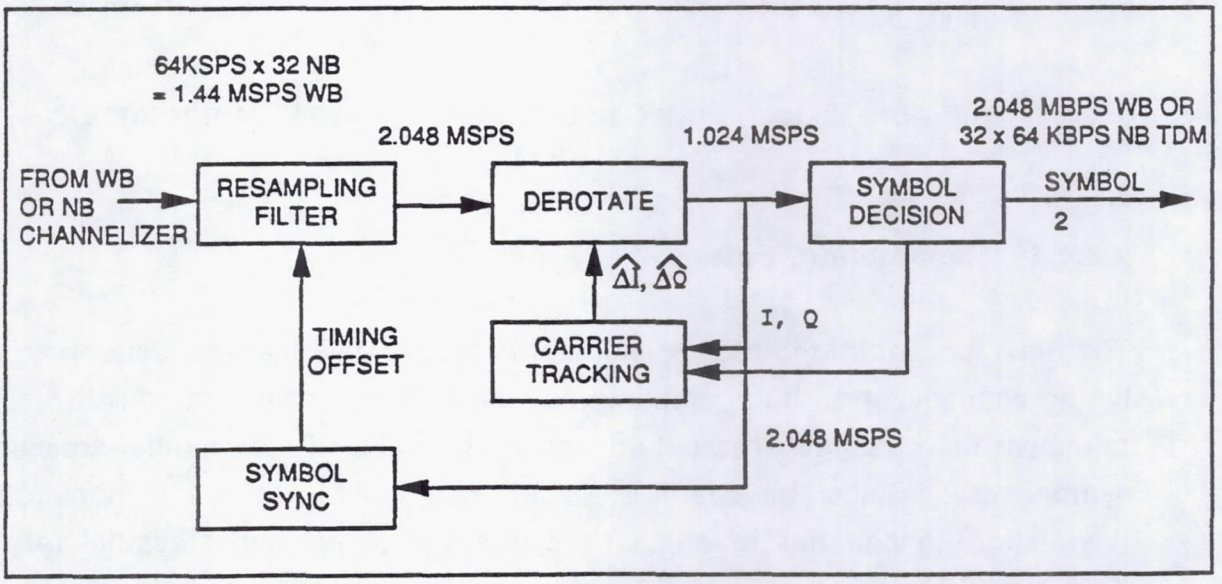


Figure 2-14. The Coherent Demodulator Block Diagram

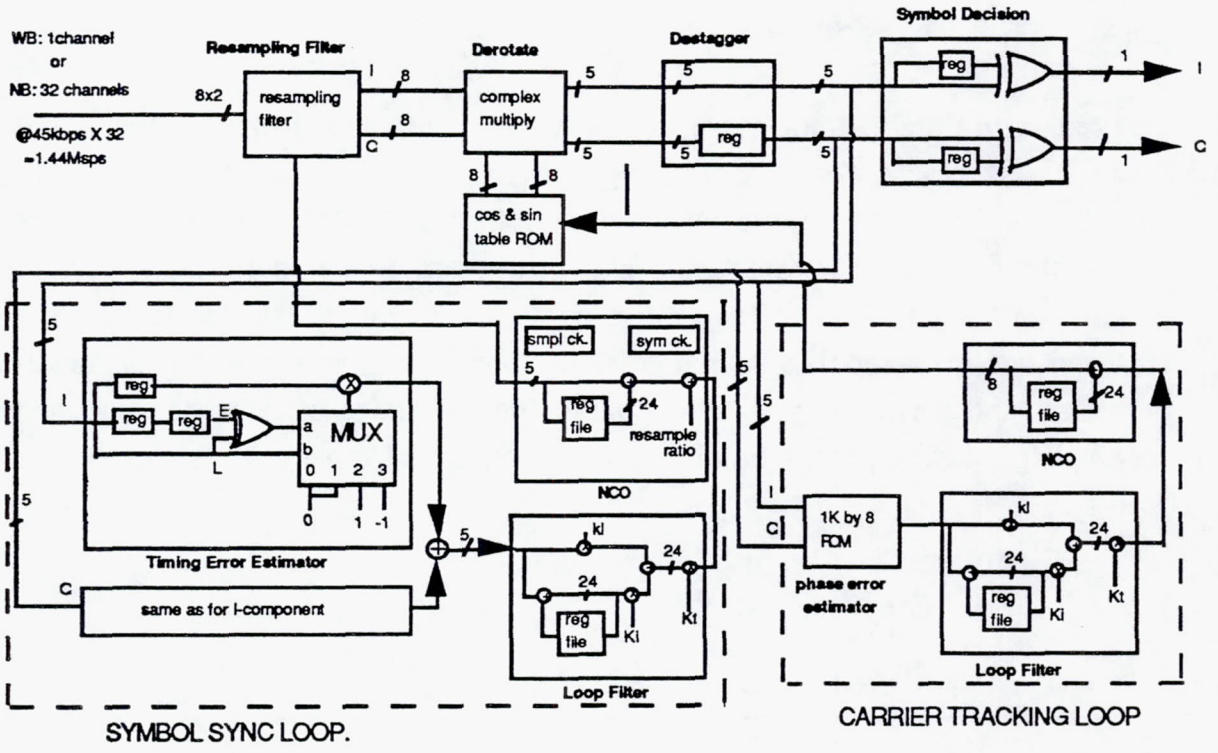


Figure 2-15. Functional Diagram of the Demodulator

2.4.4.1 Resampling Filter

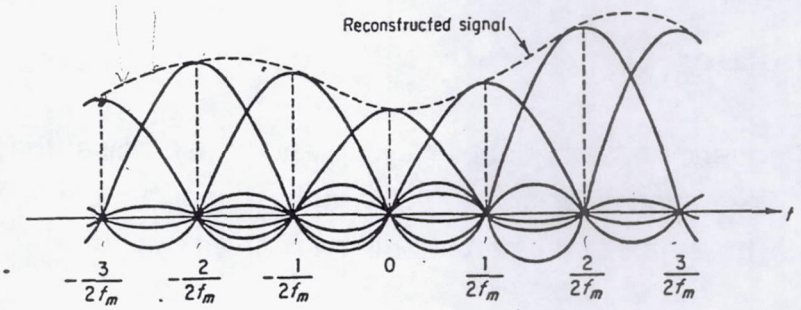
The main function of the resampling filter is to resample the data sequence provided by the channelizer at the appropriate sample epochs for the demodulator. The data rate from the channelizer is determined by the ratio of the channel spacing to the symbol rate. Since the channel spacing is 45 KHz and the symbol rate is 32 Ksym/sec, the channelizer output rate is 1.406 samples per symbol (45 KHz/32 Ksym/sec). However, the demodulator operation requires 2 samples per symbol for proper timing recovery. Thus the resampler must provide 1.422 samples (2./1.406) to the demodulator for every sample provided by the channelizer on the average.

The resampling filter in the MCDD demodulator utilizes the principle of sampling theorem, namely, that a real band-limited function is completely determined by its sample values taken at or faster than the Nyquist sampling rate. The reconstructed

signal is a summation of appropriately delayed *(sin x)/x* functions whose amplitude at the associated sampling instant is exactly the sample value and at every other sampling instant is exactly zero. Furthermore, at all intermediate points in time, the entire collection of terms combines to yield exactly the original continuous waveform everywhere. This is illustrated in Figure 2-16.

$$T \leq 1/2f_m$$

$$\sum_{l=-\infty}^{\infty} g(lT)\ \frac{\sin[2\pi(t - lT)/2T]}{2\pi(t - lT)/2T}$$



Reconstruction of a signal from its Nyquist samples by low-pass filtering.

Figure 2-16 Resampling Filter Concept

In order to do this, the resampler works in conjunction with the NCO of the timing recovery loop to interpolate the samples at the correct timing epochs.

In order to reduce complexity, the interpolator range is restricted to span only one channelizer sample. Sometimes the resampler will compute two output samples for demodulator from a single input sample from the channelizer, and sometimes it will compute only one. (In order for the resampler to compute either zero or three samples from a single input sample would require the symbol rate to be off by a degenerate amount.)

On the average, the resampling ratio will be 1.422 samples per sample. In the worst case, each of the resamplers for the thirty two channels computes two output samples from a single channelizer sample. Therefore, the system master clock must provide two execution slots for each demodulator to operate per channelizer cycle. During each execution of the demodulator for a specific channel, the NCO computes the required sample epoch for the next execution of the demodulator for that channel. The resampling filter then selects the closest of the given time slots stored in RAM containing the interpolation impulse response. If the epoch is past the one sample range of the interpolator, the NCO sets a flag to disable further executions of the demodulator for that channel until the next sample has been provided by the channelizer.

2.4.4.2 Derotator

Because of frequency offsets, doppler shifts, and phase noise, the complex signal at the output of the channelizer and the resampler is not be a true SQPSK baseband signal. That is, the signal at the derotator input is given by

$$\tilde{x}_r(k) = \tilde{x}_b(k)e^{j\theta(k)} \tag{2.4.6}$$

where $\tilde{x}_b(k)$ is the true QPSK baseband signal, and $\theta(k)$ is extraneous phase modulation. Because of this extraneous phase modulation, the signal is best described as being a pseudo-baseband signal. The function of the carrier recovery loop is to track the extraneous phase modulation and provide a phase estimate to the derotator for each sample out of the resampler. The function of the derotator is to use the phase estimate to translate the pseudo-baseband signal to baseband. In order to do this, the derotator multiplies the each input sample by the unit-valued phasor which has a phase in the opposite direction of the phase estimate.

$$\begin{aligned}
\tilde{x}_d(k) &= \tilde{x}_r(k)e^{-j\hat{\theta}(k)} \\
&= \left[\{\tilde{x}_r(k)\}_i + j\{\tilde{x}_r(k)\}_q\right]\left[\cos\hat{\theta}(k) - j\sin\hat{\theta}(k)\right] \\
&= \left[\{\tilde{x}_r(k)\}_i\omega_c(k) + \{\tilde{x}_r(k)\}_q\omega_s(k)\right] + j\left[\{\tilde{x}_r(k)\}_q\omega_c(k) - \{\tilde{x}_r(k)\}_i\omega_s(k)\right]
\end{aligned} \tag{2.4.7}$$

where

$$\omega_c(\mathbf{k}) = \cos\hat{\theta}(\mathbf{k})$$
$$\omega_s(\mathbf{k}) = \sin\hat{\theta}(\mathbf{k}) \qquad (2.4.8)$$

The derotator output at time k is thus given by

$$\tilde{x}_d(\mathbf{k}) = \tilde{x}_r(\mathbf{k})e^{-j\hat{\theta}(\mathbf{k})} = \tilde{x}_b(\mathbf{k})e^{j(\theta(\mathbf{k})-\hat{\theta}(\mathbf{k}))} \qquad (2.4.9)$$

where $\hat{\theta}$ is the phase estimate provided by the carrier tracking loop at time k, and $\theta(\mathbf{k})-\hat{\theta}(\mathbf{k})$ is the residual phase noise. Because of thermal noise and self-noise, the phase estimate is not exact and therefore $\theta(\mathbf{k})-\hat{\theta}(\mathbf{k}) \neq 0$. However, appropriate design of the carrier tracking loop produces a residual phase noise process with an acceptable RMS value.

The implementation of the derotator in integer arithmetic is straight forward. The phase estimate is provided to the derotator in an 8-bit two's complement. The phase in radians which the integer word, z(k), represents is given by

$$\hat{\theta}(\mathbf{k}) = \frac{2\pi z(\mathbf{k})}{256} \qquad (2.4.10)$$

Thus z(k)=-128 corresponds to

$$\hat{\theta}(\mathbf{k}) = -\pi,$$

and z(k)=127 corresponds to

$$\hat{\theta}(\mathbf{k}) = \frac{127}{128}\pi.$$

The w_c and w_s values are each 8-bits. The values are stored in ROM tables, and z(k) is used an an address into these tables. The table values as a function of z(k) are given by

$$\omega_c(\mathbf{k}) = \mathbf{Rnd}\left\{127\cos\frac{2\pi z(\mathbf{k})}{256}\right\}$$
$$\omega_s(\mathbf{k}) = \mathbf{Rnd}\left\{127\sin\frac{2\pi z(\mathbf{k})}{256}\right\} \qquad (2.4.11)$$

where Rnd{•} denotes rounding to the nearest integer value. The complex samples out of the resampler are quantized to 8-bit per rail. Thus, each multiplication produces a 16-bit product. The two products for each rail are added or subtracted accordingly to produce 16-bit words on each rail. The carry bit may be discarded since overflow is not possible. The 16-bit words are each truncated to 5-bits by dropping the 11 LSB's to form the derotator output.

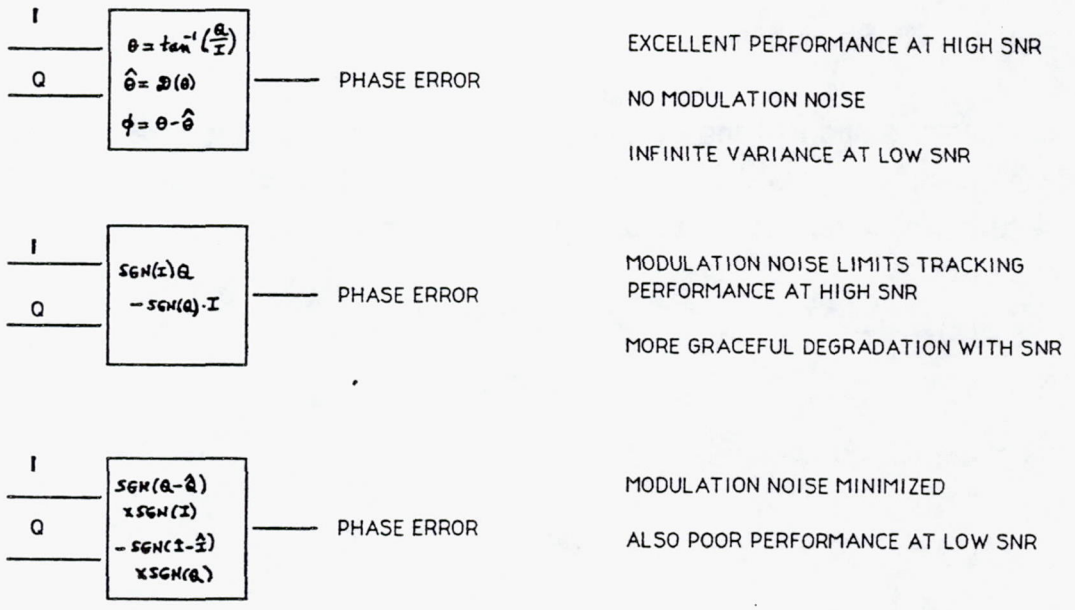


Figure 2-17. Carrier Tracking Considerations (Ideal Case)

2.4.4.3. Carrier Tracking Loop

Figure 2-17 roughly summarizes the three well known phase error detection methods that have been considered during the MCDD system engineering analysis, where I and Q stands for in-phase and quadra-phase components of the received signal and θ

and $\hat{\theta}$ refers to the measured and the corresponding reference phase of the received carrier. We have chosen the first method for its simplicity of hardware implementation and no modulation noise in the absence of either ISI or timing error. Even though this type of estimator exhibit infinite variance at low SNR, the normal operating conditions provided for the MCDD demodulation should not allow any havoc.

The carrier phase error estimate taken after the destagger module is low-pass filtered and used to cancel the carrier phase offset. For computing the loop parameters as shown in Figure 2-15, the following equations are used:

$$K_l = \frac{2\xi\omega_n T}{AK_v K_t T} \tag{2.4.12}$$

and

$$K_i = \frac{(\omega_n T)^2}{AK_v K_t T} \tag{2.4.13}$$

where A is the gain of carrier phase estimator module, and K_t is the remaining loop filter parameter. K_v is the NCO gain computed by

$$K_v = \frac{2\pi R}{2^L}. \tag{2.4.14}$$

R is the symbol rate and L is the number of NCO bits, T is the symbol period (T=1/R), ξ is the damping factor ($0.5<\xi<1$), w_n is the loop resonance frequency given by

$$\omega_n = 1.89B_L, \tag{2.4.15}$$

and B_L is the loop bandwidth we desire.

Narrower loop bandwidth decreases RMS jitter due to thermal noise, however, this results in slow pull-in time and poorer phase noise performance due to oscillator instability. On the other hand, setting the loop bandwidth too large would allow too much RMS jitter due to thermal noise which results in substantial BER performance degradation. The loop bandwidth in MCDD POC model is selected to be one hundredth of the data rate which results in phase jitter due to thermal noise less than

six degrees and pull in time of less than 0.05 second. Given the desired loop bandwidth, one can determine the loop filter parameters using equations (2.4.12)-(2.4.15).

2.4.4.4. Bit Synchronization Loop

The derotated complex samples are processed, I and Q separately, to determine timing error. If the two mid-symbol samples are of opposite signs, they will cancel and the transition sample will be near zero (DTTL). The resulting sum of the two mid-symbol samples is therefore zero if the resampling filter is precisely locked to the symbols, and any timing error will be proportional to the non-zero sum. The difference in sign of the two mid-symbol samples indicates the direction of timing error. If the signs are equal, the above sum is ignored since no transition occurred. The measured timing errors for the I and Q samples are summed to give the resulting timing error estimate.

The timing error estimate is low-pass filtered and used to control the direction of an up/down counter which generates the step size of the timing offset. The step size is a function of the fixed ratio of the resampling filter input and output sample rates and the variable timing drift. The timing offset is output to the resampling filter to select the next filter to be used. The number of resampling filter taps should chosen to provide good interpolation precision while minimizing the size of the hardware. The loop parameters can be obtained using the equations (2.4.12) to (2.4.15) as well.

2.4.4.5. Symbol Decision

The symbol decision block decides on the I & Q estimates by taking the most significant bit of the sample taken at the center of each symbol.

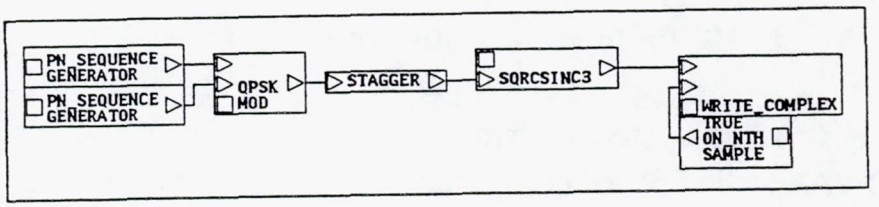
2.5. MCDD Performance Analysis Using BOSS

The Block Oriented Systems Simulator (BOSS) run under VMS operating system on the DEC VAX station provides a complete iterative environment for simulation-based analysis and design of any system signal processing operation. Whereas BOSS can perform a time domain (waveform level) simulation of any system, the current model library contains functional blocks most suitable for communication systems simulation.

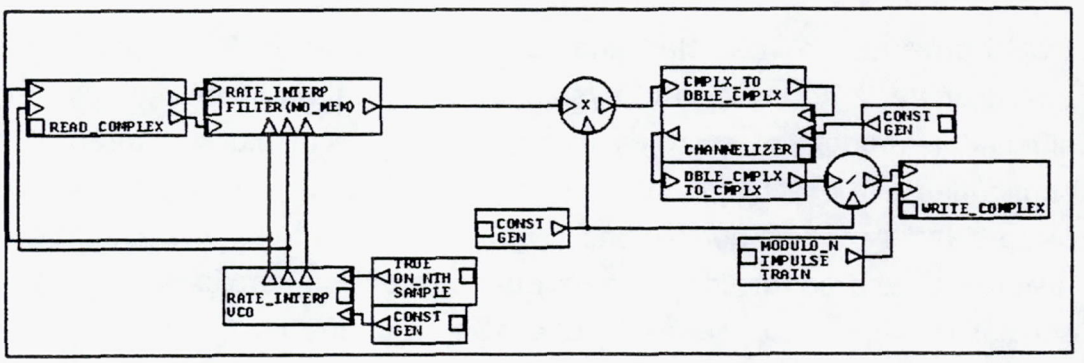
BOSS provides an integrated and iterative environment for all phases of simulation based analysis and design of systems including the capabilities for (i) constructing simulation models of systems using a hierarchical block diagram approach, (ii) configuring and executing time domain simulations, (iii) viewing the simulation results using a variety of time domain and frequency domain plots, and other displays such as histograms and correlation plots, (iv) perform design iterations, and (v) documenting simulation models and the results of analysis and design.

Performance of the total MCDD as well as each of the individual blocks have been analyzed using BOSS. Three major BOSS simulation system modules for the MCDD POC model analysis are shown in Figure 2-18. The simulations were run at three consecutive modes, i.e., (a) modulation & pulse shaping, (b) channelization, and (c) demodulation & BER estimation. Performance of the MCDD can be analyzed in the most efficient manner using this setup since the number of samples per symbol is different at the channelizer input and at the demodulator input.

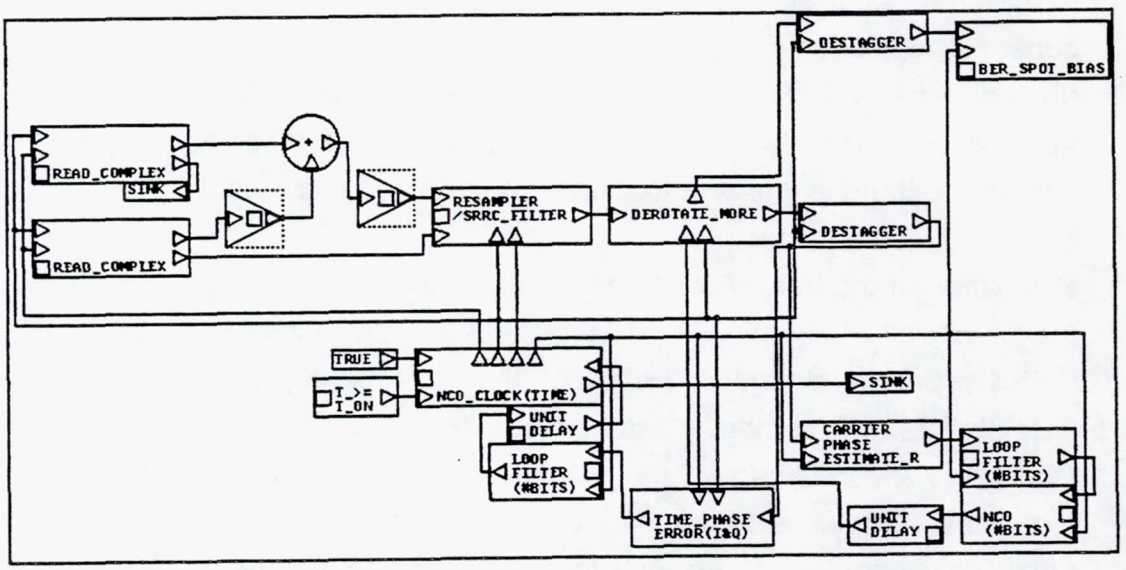
Simulation of the total MCDD has been performed in the following manner. First, run the simulation of Figure 2-18(a) with QPSK sources and two samples per symbol. The QPSK source is staggered (SQPSK), then baseband pulse shaping is applied to the SQPSK I and Q symbol pulses before its samples are written to an external file. During the second phase of the simulation as shown in Figure 2-18(b), the channelizer reads the samples stored in three external files, i.e., at the center channel and two adjacent channels, i.e., the ACI (adjacent channel interference) effect can be added right here. Each ACI input needs to be read in from separate external files then amplified by proper factor, i.e., 2.51 (8dB higher power), the worst case ACI.



(a) BOSS System for Modulation & Pulse Shaping



(b) BOSS System for Channelization



(c) BOSS System for Demodulation & BER estimation

Figure 2-18. BOSS Block Diagram for Bit Error Rate Estimation

The number of samples per symbol is two when the samples are read in by the channelizer simulation. At the output of the channelizer, however, we get 1.406 samples per symbol to be stored in another external file. White Gaussian noise samples can also be added to the input during the channelizer simulation so that the input to the channelizer is the transmitted signal plus noise. An alternative method, which we have utilized here for substantial savings in simulation time, processes the signal and the noise samples separately then mix them right before the demodulation. Though not exactly the same as the true POC hardware set up, independent simulation of the two methods in various cases confirmed that the two methods provide almost identical BER estimates.

The third step of the MCDD simulation involves demodulation and the BER (bit error rate) estimation. The signal and noise are added together with proper SNR set up (noise samples are multiplied by a proper constant to provide desired Eb/No) then demodulated. The BER_SPOT_BIAS module estimates the BER semi-analytically. Details of the simulation now follow.

2.5.1 MCDD Channelizer Analysis

Analysis of the channelizer involves BOSS simulation of the Figure 2-18(a), Figure 2-18(b), and Figure 2-18(c) in sequence then estimating the BER curves with different sets of parameters. Important parameters to be selected are window type and presum ratio of the windowed input data for the channelizer. The criterion to be used here is Eb/No required to obtain the BER of $5x10^{-7}$ while keeping the size and complexity of the hardware to the minimum.

We have chosen the Kaiser window because of its smooth flat passband response at the expense of stopband ripple since the current modulation choice with baseband pulse shaping have already mitigated the effects of ACI successfully. Availability of proven window design softwares helped us to choose and simulate all available windows with different presum ratio. In order to choose the presum ratio and the channelizer window type, the effects of ACI (adjacent channel interference) have been carefully looked at. It turns out that the BER performance improvement from

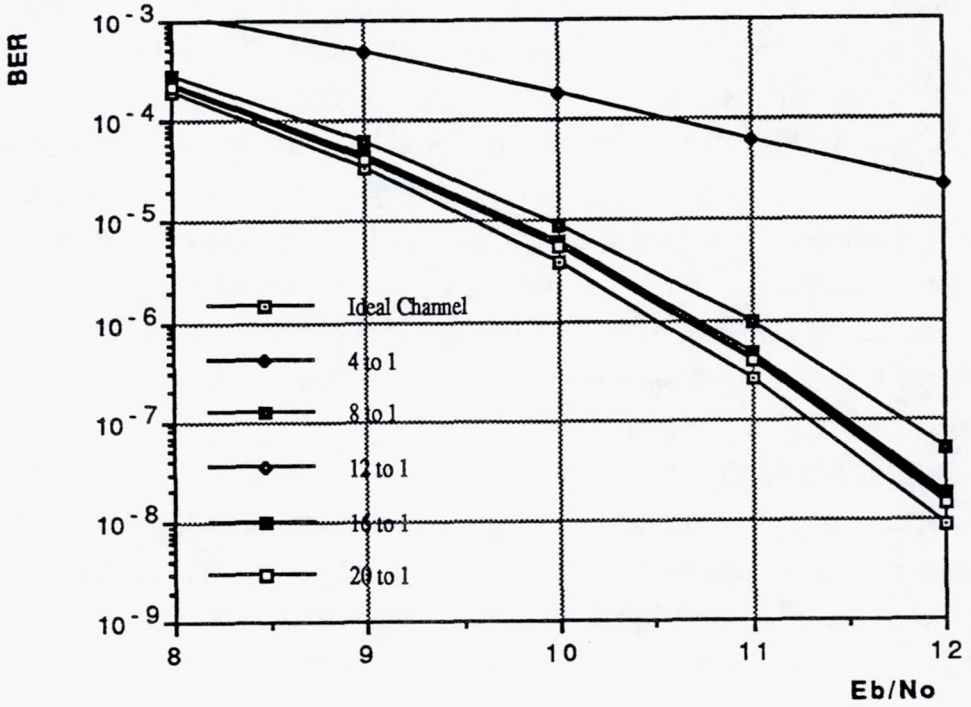


Figure 2-19. BER vs. Presum Ratio

increasing presum, i.e., wider 3 dB bandwidth and steeper cutoff, reaches the point of diminishing return at around the presum ratio of twelve. (See Figure 2-19.) Our choice of presum ratio for the MCDD is sixteen, which allows room for additional implementation losses as well as the possibility of implementing constant envelope bandwidth efficient type modulation later.

Simulation of the channelizer without and with ACI showed that the ACI, where the adjacent channel signal with 8dB higher signal power than the signal at the center channel, did not degrade the BER performance much, i.e., less than one percent BER increase due to the ACI. (See Figure 2-10.) In the same manner, we have also chosen the window tap quantization to be sixteen bits after observing significant degradation of BER performance with less than twelve bits.

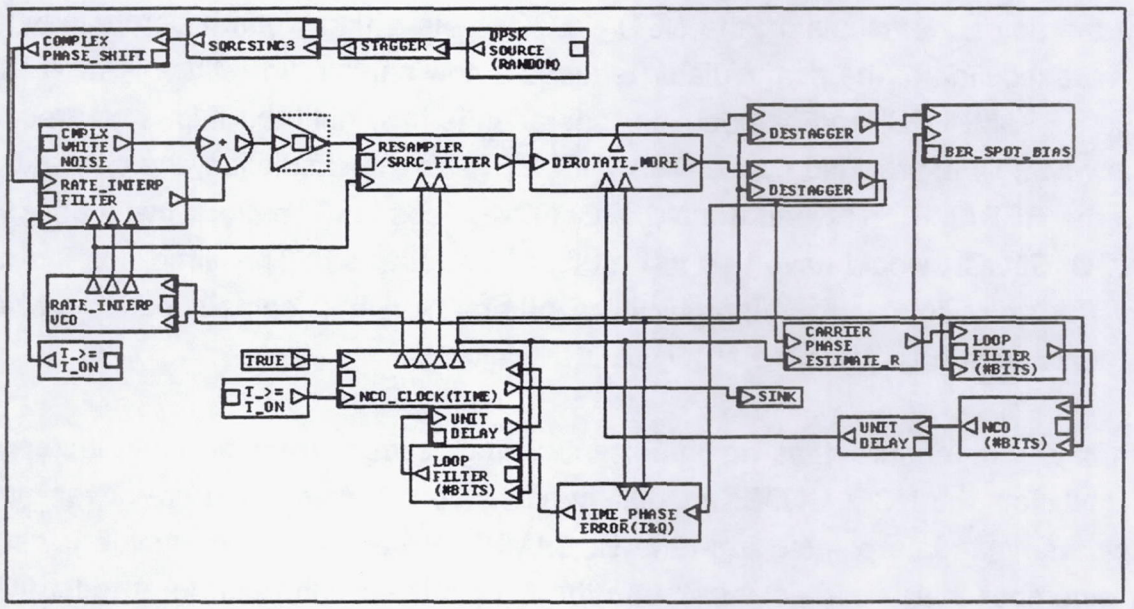


Figure 2-20. BOSS Block Diagram for the Simulation of Demodulator Only

2.5.2 MCDD Demodulator Analysis

A BOSS system module to test only the demodulator is shown in Figure 2-20. Note the absence of the channelizer in the system. Using this test module, any arbitrary carrier phase error, carrier frequency shift, and timing offset can be added to the SQPSK source signal to verify each of the demodulator modules.

Two additional modules, which are not required in the actual demodulator, have been added to aid in the simulation of the MCDD demodulator with ideal channelizer : RATE_INTERP VCO and RATE_INTERP FILTER. The RATE-INTERP FILTER module accepts samples from a pulse-shaped SQPSK source which operates at a sample rate of two samples per symbol, and buffers these samples in a circular buffer. Samples are interpolated upon request from the RATE_INTERP VCO at a rate of 45/64 per sample. RATE_INTERP VCO requests a new sample when the NCO_CLOCK module determines that it needs a new sample in the RESAMPLER.

In the actual demodulator, the NCO_CLOCK sets a flag when it determines that the next execution of the demodulator requires a new sample from the CHANNELIZER in the RESAMPLER, and demodulator operation is held until the flag is cleared when a new sample is provided by the CHANNELIZER. In the simulation, the data is provided to the RESAMPLER when the NCO_CLOCK needs it. The clock cycle on which the NCO_CLOCK would have had to wait is thus swallowed. This simplifies the analysis of the demodulator waveforms, which otherwise would contain periods where the signals were held while the NCO_CLOCK waited.

In order to ensure that no important timing issues are being neglected by the simulation, the NCO_CLOCK module contains code to verify that are never more than two samples interpolated from the RESAMPLER before a new sample is requested (remember that in the actual system the demodulator can operate at most two times before the channelizer writes a new sample to the RESAMPLER). With this code in place, the simulation is capable of fully verifying the operation of the demodulator. Details of the simulation now follow.

2.5.2.1 Resampling filter

We have observed the input and output of the resampling filter to confirm that the output samples are coming out at the rate of two samples per symbol when the input sample rate is 1.406 samples per symbol.

2.5.2.2 Carrier Tracking Loop

A BOSS system module similar to the one shown in Figure 2-20, but without closing the carrier tracking loop, is utilized when computing the carrier phase error estimator gain. The carrier phase error estimator module gain is a required parameter for computing necessary loop parameters of the carrier tracking loop as illustrated by equations (2.4.12) through (2.4.15). Furthermore, we have deliberately introduced carrier phase errors ranging from -1/4 Π to 1/4 Π, and measured the corresponding outputs of the module. Figure 2-21 shows the carrier phase estimate obtained from

the carrier phase error estimator module vs. the actual phase error entered as simulation parameters. For computing the module gain, only the linear portion of the plot is taken into account.

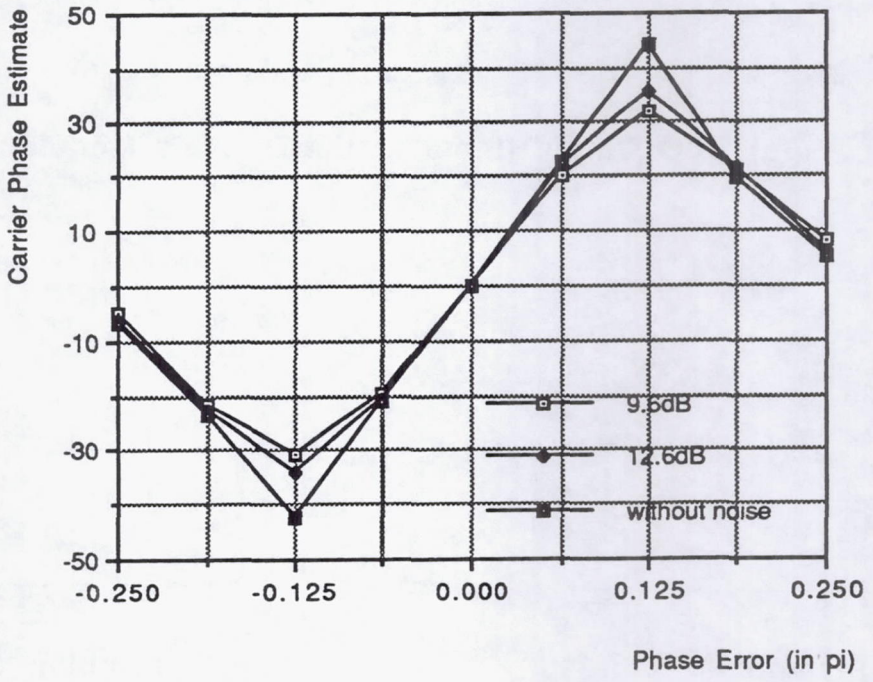
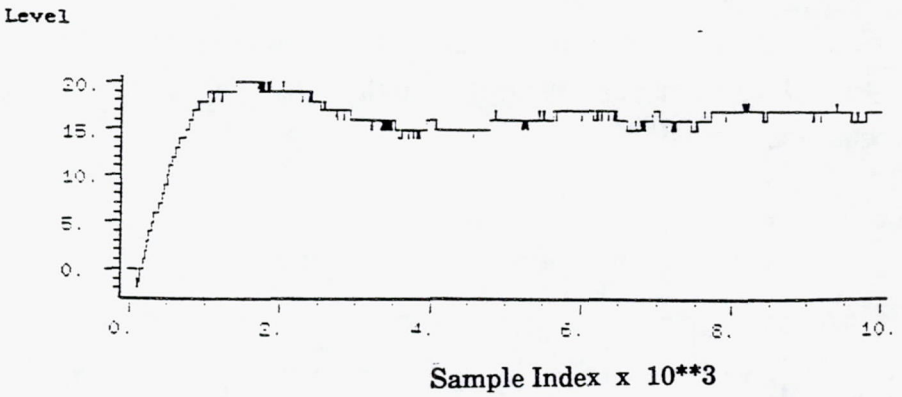
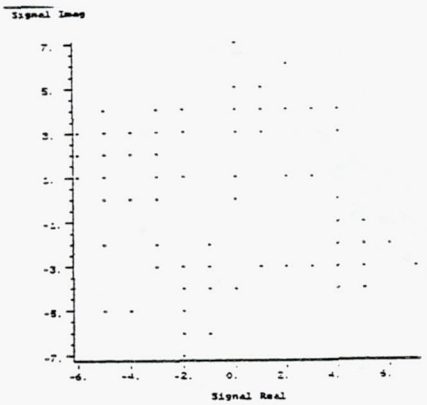


Figure 2-21. Carrier Phase Estimate vs. Carrier Phase Error

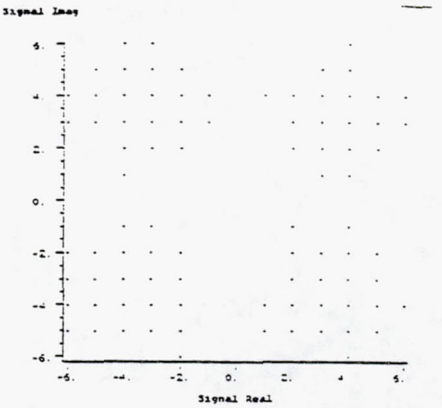
The demodulator's ability to track carrier phase error can be verified by running simulations with its loop closed, and Figure 2-22(a) shows time plot of the carrier tracking loop NCO output when the true carrier phase error is 22.5^{o} in the absence of timing errors. The NCO output converges to 16, and it can be easily shown using equation (2.4.10) that the corresponding phase error is indeed 22.5^{o}. Figures 2-22(b1) to 2-22(b4) then shows the I-Q plots of the destaggered output at the sample indices of (b1) 111 to 310, (b2) 3001 to 4000, (b3) 6001 to 7000, and (b4) 9001 to 10000. The tracking capability of the carrier phase loop is evident.



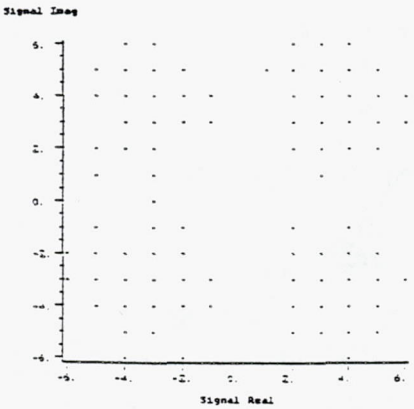
(a) NCO Output (Input to the Derotate Module)



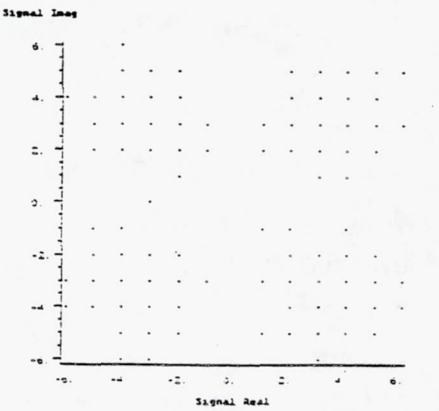
(b1) samples. 111-310



(b2) samples 3001-4000



(b3) samples 6001-7000



(b4) samples 9001-10000

Figure 2-22. Demonstration of Carrier Phase Tracking Ability

Furthermore, the carrier phase estimate jitters are measured and compared to those obtained analytically for our choice of the carrier phase error estimator:

$$\sigma_{ph}^{\ 2} = \frac{2B_L T}{(E_b / N_o)} \qquad (2.5.1)$$

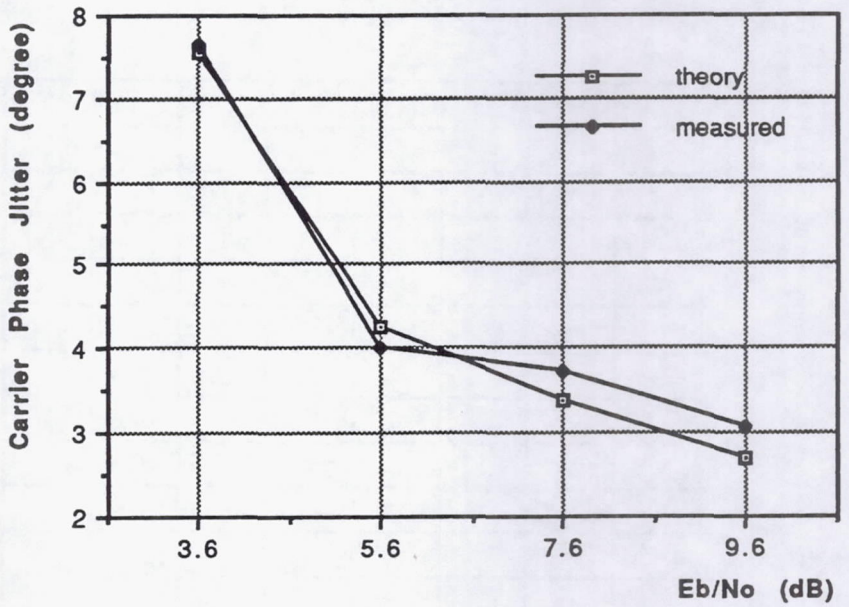


Figure 2-23. Carrier Phase Jitter (Theory vs. Actual)

Phase jitter estimate obtained by equation (2.5.1) is valid at moderately high Eb/No, and Figure 2-23 shows the theoretical phase jitter (obtained from the above equation) and the measured phase jitter for $B_L T$ of 10^{-2}. Note the consistency of measured phase jitter and theoretical phase jitter. The loop bandwidth in MCDD POC model is selected to be one hundredth of the data rate which results in phase jitter due to thermal noise less than six degrees and pull in time of less than 0.05 second.

With the loop bandwidth selection of 10^{-2} times the symbol rate ($B_L T=10^{-2}$), the carrier loop will be able to acquire frequency offsets of 102.4 KHz for the wideband channel,

and 3.2 KHz for the narrowband channel, both assuming K-band (14 GHz) uplinks. This implies oscillator instabilities of approximately 7.3×10^{-6} and 2.3×10^{-7} for the wideband and narrowband transmitters, respectively. Thus for wideband channels, it is not necessary to provide any special acquisition mechanism, but we may need to provide a acquisition tool for narrowband channels. (See section 2.6.1.1 for details.)

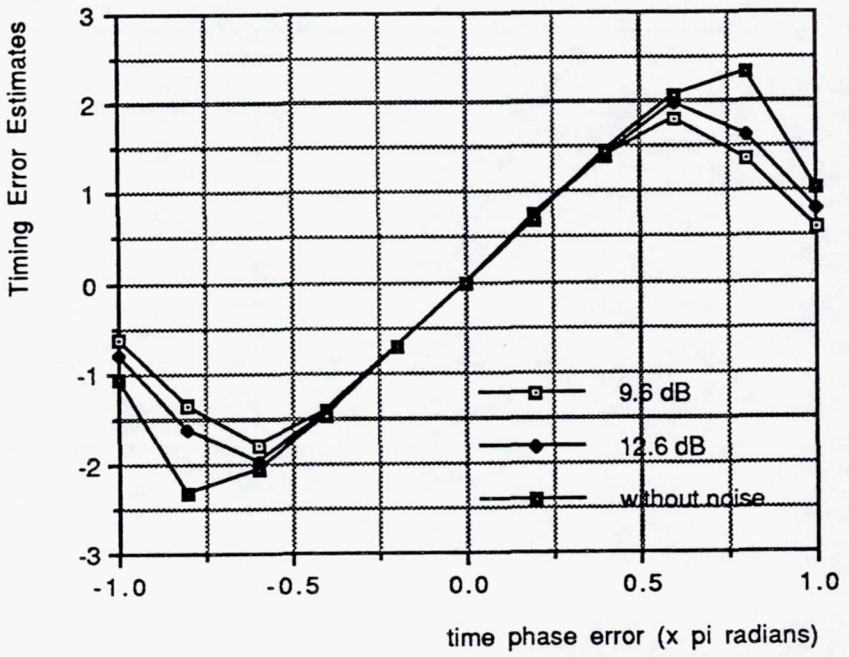


Figure 2-24. Timing Error Estimates vs. Timing Error

2.5.2.3 Bit Synchronization Loop

Likewise, the demodulator's ability to track timing error has been verified by running simulations with its loop closed. Figure 2-24 shows the timing error estimator module gain which is used to compute the timing loop parameters. With the loop bandwidth selection of 5×10^{-3} times the symbol rate ($B_L T = 5 \times 10^{-3}$), the bit synchronization loop will be able to acquire clock rate offsets of 51.2 Kbps for the wideband channel, and

1.6 Kbps for the narrowband channel. This implies symbol clock instabilities of 2.5×10^{-2} for both the wideband and narrowband transmitters, thus it is not necessary to provide any special acquisition mechanism in either the wideband or the narrowband case.

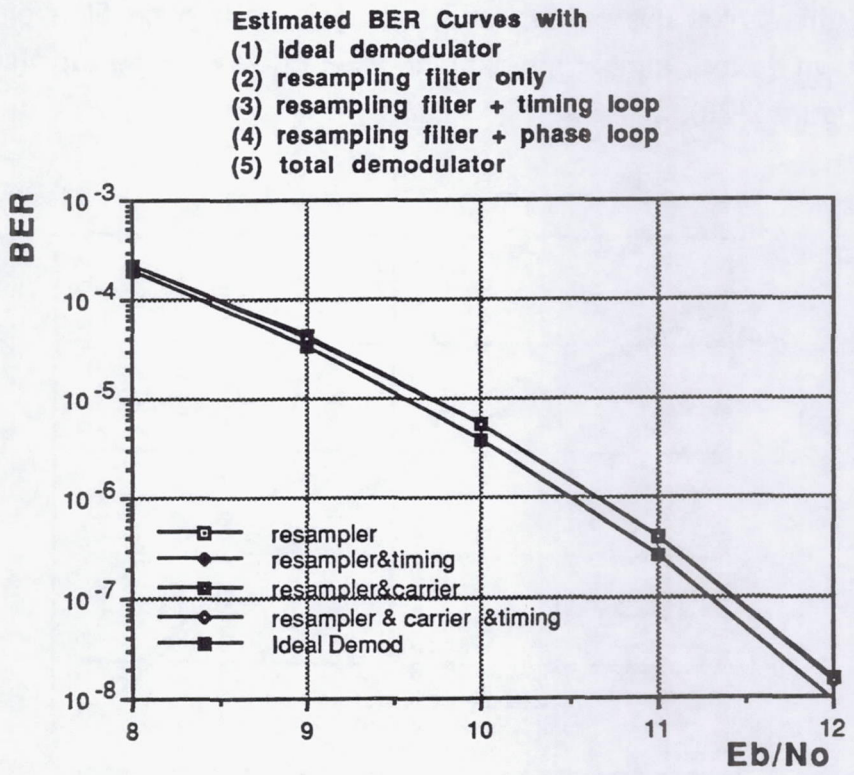


Figure 2-25. BER Estimates with Ideal Channelizer (without Channelizer Losses)

2.5.3 MCDD Parameter Trade

Using the BOSS Spot Check Variance Semi-Analytic BER estimation module, we have quantified the demodulator losses due to resampling filter, carrier tracking loop, and bit synchronization loop, as well as A/D effects in terms of the required Eb/No to achieve 5×10^{-7} BER. Losses due to the demodulator only (without any channelizer

losses) are shown in Figure 2-25, and it can be clearly seen that major portion of the losses came from the resampling filter, i.e., timing loop and carrier phase loop did not introduce any significant degradation.

The bottom BER curve corresponds to the ideal demodulator without loss, while the BER curves due to (i) resampling filter only, (ii) resampling filter plus the timing loop, (iii) resampling filter plus the carrier loop, and (iv) resampling filter plus both loop closed, are shown as four almost overlapping BER curves on the top (seen as a top BER curve in Figure 2-25).

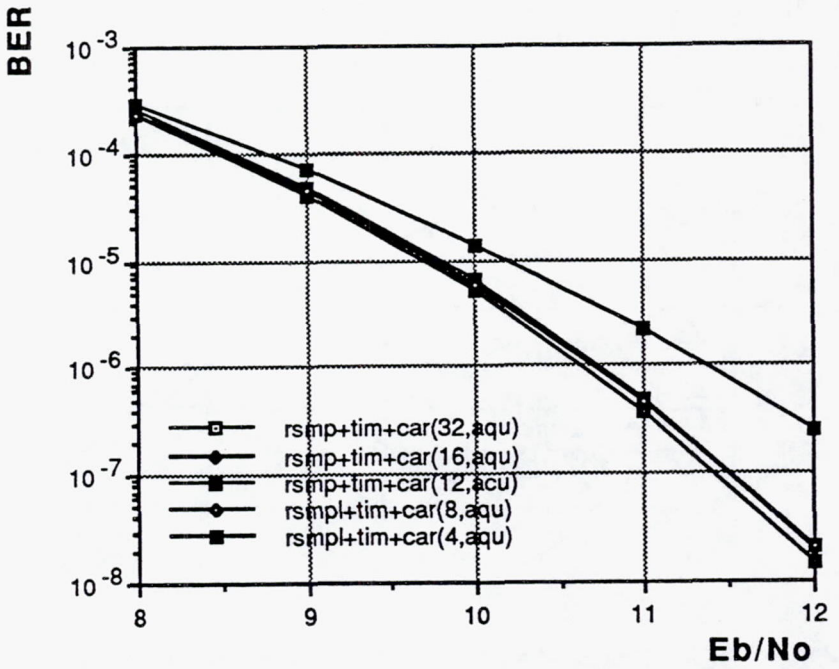


Figure 2-26. BER vs. Number of Resampling Filter Taps

Losses due to the resampling filter were then examined to see what the most significant factors are in determining the BER performance. Among those considered, number of resampling filter taps was found to be the most critical. Figure 2-26 shows the BER curves with ideal channelizer and varying number of resampling filter taps. (The BER results shown in Figure 2-25 uses sixteen resampling filter taps.) Even though eight seems to be a point of diminishing return, our choice for the number of

resampling filter taps is sixteen in order to allow enough room for other possible degradations, i.e., implementation losses. Future pulse shaping choices such as TFM may require more number of quantization bits.

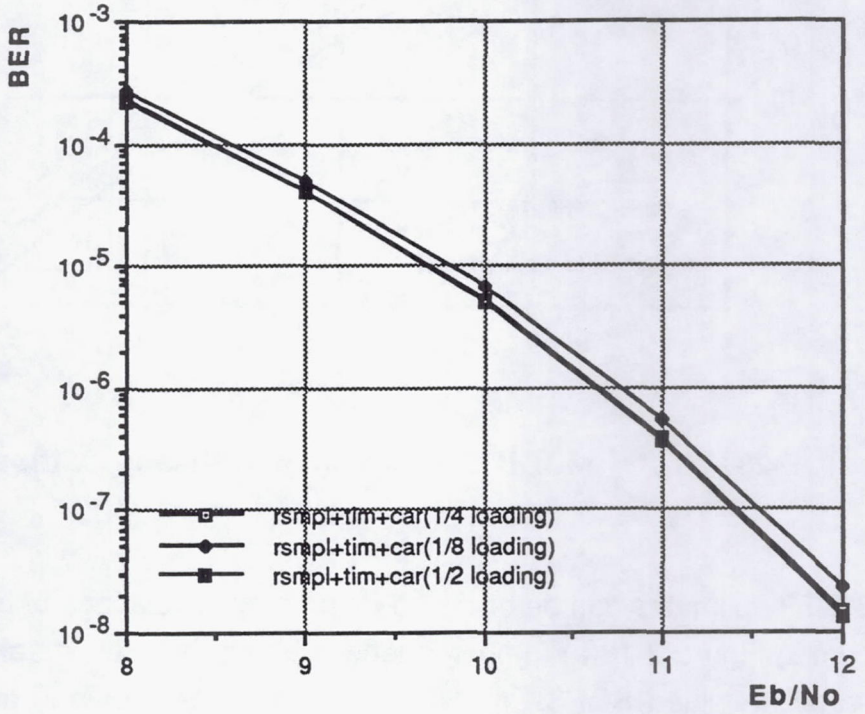


Figure 2-27. BER vs. A/D Loading Factor in the Demodulator

While fixing the demodulator parameters as before, BER performance of the demodulator with different A/D loading factors are examined over the dynamic range of 8 dB, i.e., half loading means that the maximum value of a sample is only half the maximum value the given number of bits can handle, etc. Figure 2-27 shows the BER vs. A/D loading factor; 1/8, 1/4, and 1/2. Our choice of the loading factor is 1/4 since it allows enough room to avoid overflow while providing sufficient precision.

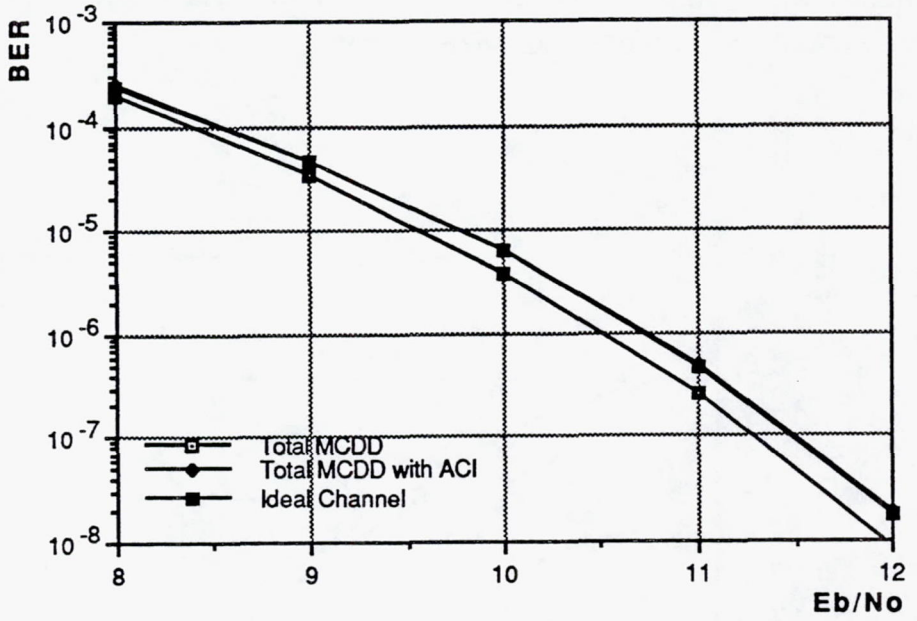


Figure 2-28. Total MCDD Performance with and without ACI

Total MCDD BER estimates can be obtained by running simulations of the three BOSS systems shown in Figure 2-18(a)-(c) in sequence. Using the presum ratio of sixteen to one and linearly amplified SQPSK modulation, BER plots shown in the Figure 2-28 were generated. Note the 0.25 dB Eb/No degradation at the BER of $5x10^{-7}$. This compares with about 0.1 dB Eb/No degradation due to the demodulator alone.

Also plotted is the case of ACI, where the signal powers at the two adjacent channels are 8 dB higher than that of the desired signal. As mentioned before, the current modulation approach is SQPSK with baseband pulse shaping. The pulse shape is a raised cosine (square root raised cosine at the transmitter and another square root raised cosine matched filter implemented at the resampling filter). This approach indeed mitigated the effects of ACI and ISI, i.e., the effects of ACI on the BER performance is less than one percent additional BER degradation over the case without ACI.

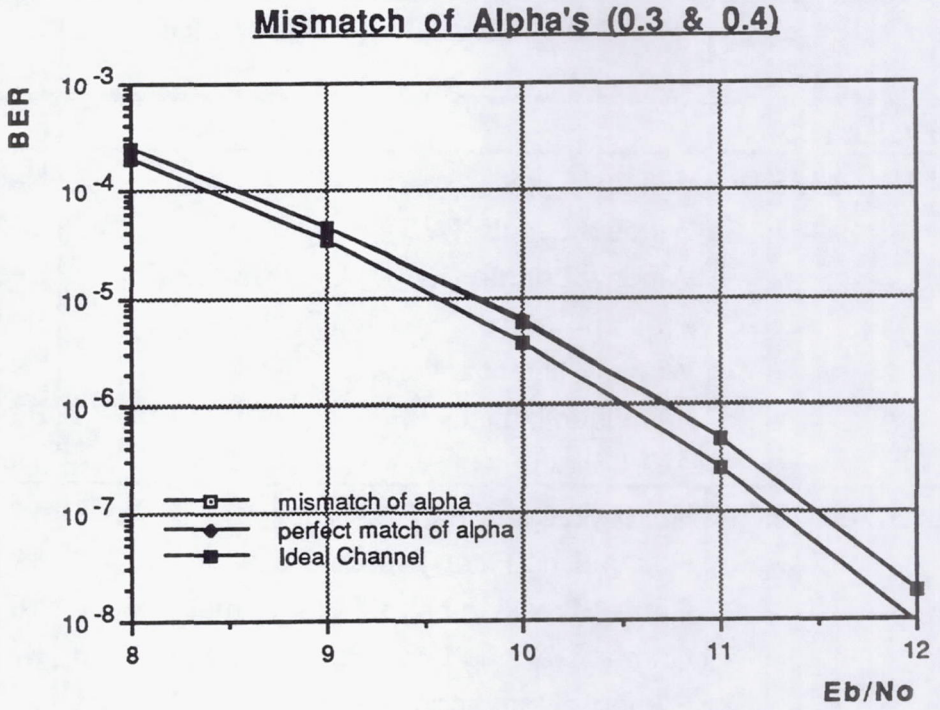


Figure 2-29. Total MCDD Performance with Mismatch of Alpha's

We have also looked at the effects of mismatch in the transmitter square root raised cosine filter rolloff constants and that of the receiver (within the resampling filter), both of which are designed to be square root raised cosine filters with identical rolloff constant. Due to aging or manufacturing tolerance limits, the roll-off constant of the transmitter and the receiver may not match exactly. Figure 2-29 shows the BER plots with perfect match and with a slight mismatch, i.e., rolloff constant of 0.3 and 0.4, respectively. Degradation due to the mismatch seems almost negligible from the BER plot shown in Figure 2-29.

	POC DESIGN PARAMETER	CHOICE
MODULATION		Linear Amp. **SQPSK**
CHANNELIZER	Window Type	Kaiser
	Window Length (**WB**)	L=256
	Window Length (**NB**)	L=512
	Presum Ratio	P=16
	Window Quantization	16 bits
	A/D Quantization	8 bits
	A/D Loading	1/4
DEMODULATOR	No. of Resampling Filter Taps	16
	Resampling Filter Tap Quantization	16 bits
	Carrier Tracking Loop **BW** x Symbol Period	10^{-2}
	Carrier Tracking Loop Parameters	$K_L=2^5$, $K_I=2^{-1}$, $K_T=2^{-4}$
	Symbol Sync. Loop **BW** x Symbol Period	$5x10^{-3}$
	Symbol Sync. Loop Parameters	$K_L=2^7$, $K_I=2^0$, $K_T=2^{-8}$
	No. of Bits in Loop NCO Register Files	24

Table 2-2 Summary of MCDD POC Design Parameters

2.6 Summary and MCDD POC Requirements vs. Capabilities

Various issues of the MCDD have been discussed and analyzed using the BOSS simulation results, and Table 2-2 summarizes outcome of the system engineering tasks regarding the choice of channelizer and demodulator parameters. The overall MCDD concept requirements and a set of POC model performance parameters are summarized in the left column of Table 2-3. Shown in the right hand side column are the corresponding capabilities of the MCDD POC model as verified by BOSS analysis, assuming that the satellite is in geosynchronous orbit and the ground terminals are stationary.

Table 2-3 Requirements vs. Capabilities

REQID	MCDD REQ/SYSTEMS ENGINEERING	CAPABILITY	VERIFIED BY
1	Simultaneously demultiplex and demodulate an FDM composite input signal	Comply	Design
2	Composite input signal shall consist of hundreds to thousands of narrowband (NB) channels and tens of wideband (WB) channels	784 NB & 26 WB (MCDD Concept) 3 WB or 2 WB & 26 NB channels (POC)	Design
3	The NB input channels shall have a data throughput rate of 64 KBPS	Comply	Design
4	The WB channels shall have a data throughput rate of at least 24 times that of the NB channels	WB data rate is 32 times NB data rate	Design
5	Individual input channels shall have a maximum dynamic range of 8 db	Maximum dynamic range of more than 8 dB	Design
6	Concept shall take into consideration future technology availability, and size, mass, and power tradeoffs for a flight model for year 2000	Expected GaAs technology (MISFETS) Flight-ready 4.5 lbs and 18 W by 1995 Flight-ready 1.0 lbs and 5 W by 2000	Design
7	Techniques of POC shall not preclude future flight model	The POC model does not preclude any future application (fully demonstrates the signal processing functions of MCDD)	Design

Table 2-3 Requirements vs. Capabilities (Cont'd)

REQID	MCDD REQ/SYSTEMS ENGINEERING	CAPABILITY	VERIFIED BY
	Supply optimized performance goals for:		
8	Modulation scheme	Linearly amplified SQPSK (w/option to choose constant envelope BW efficient modulation with minor design change)	Simulation
9	Implementation loss from theory of proposed modulation scheme	.1 dB loss due to demodulator alone	Simulation
10	Composite signal bandwidth efficiency	1.42 bps/Hz (WB) & 1.25 bps/Hz (NB)	Simulation
11	The required Eb/No to achieve a BER of $5x10^{-7}$ for both NB and WB channels with no adjacent channel interference (ACI)	10.8 dB (WB) & 10.9 dB (NB) without ACI	Simulation
12	The BER vs Eb/No with and without ACI for both NB and WB channels	10.8 dB (WB) & 10.9 dB (NB) (almost no degradation due to ACI)	Simulation
13	The minimum carrier, and symbol clock stabilities for both NB and WB channels	Carrier: WB: 7.3x10E(-6); NB: 2.3x10E (-7) Symbol: WB: 2.5x10E(-2); NB: 2.5x10E (-2)	Simulation
14	The mechanism for acquisition and synchronization of newly activated NB and WB users	Cooperative interrelation of the VSAT users through MCS *or* by utilizing probing channels shared by users	Analysis
15	The grouping (distribution) of active NB and WB channels across the composite signal bandwidth	26 WB channels with 28 NB each	Design

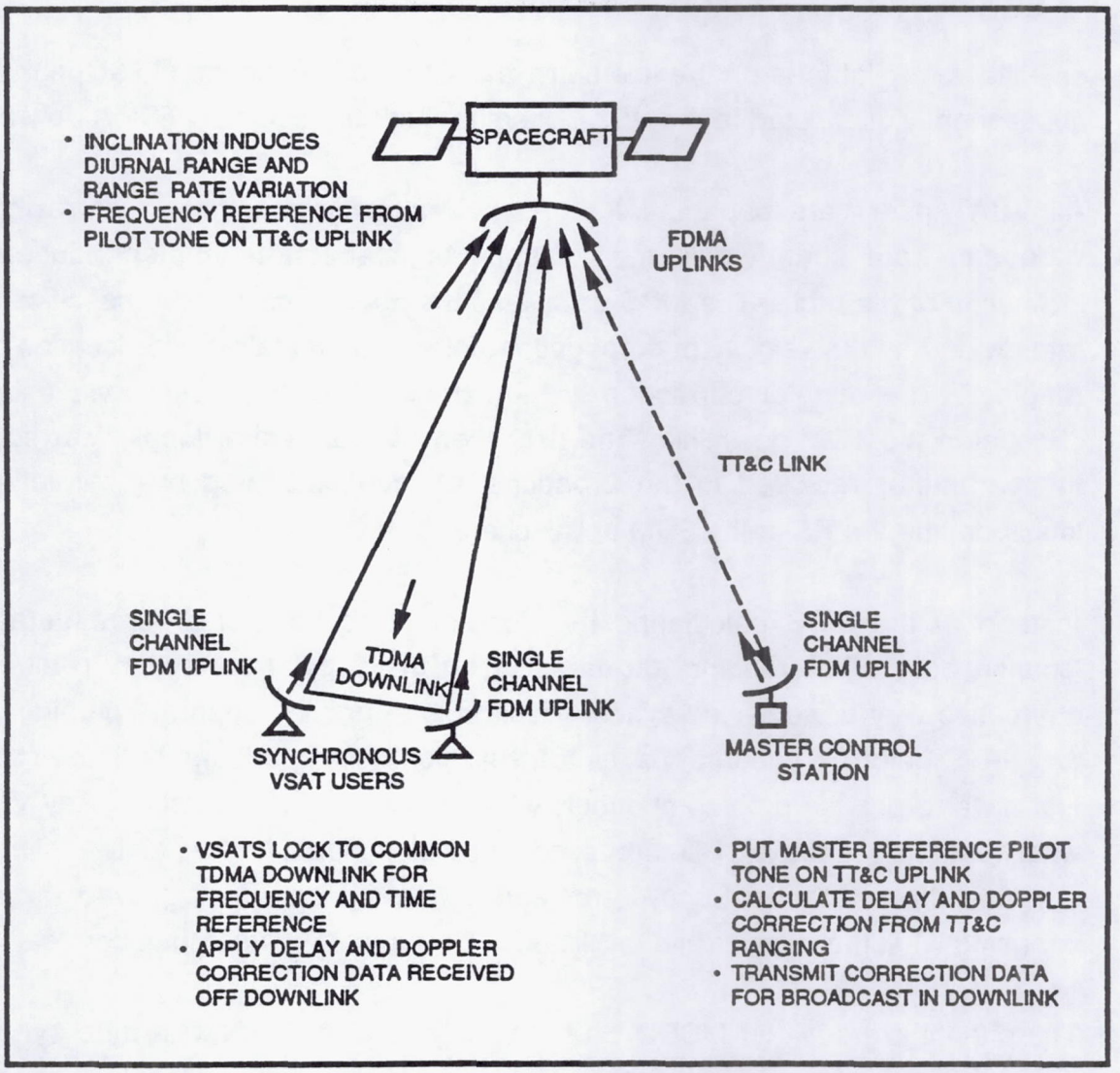


Figure 2-30 MCDD Synchronous System Operation

2.6.1 Further Considerations

2.6.1.1 System Synchronization Methods

It may be necessary to provide a special synchronization mechanism for the reasons discussed in MCDD demodulator carrier tracking loop analysis. System synchronization can be achieved through the cooperative interrelation of the VSAT users through the master control station (MCS) as shown in Figure 2-30. All operation is coherent with the master frequency reference at the MCS which is uplinked to the

satellite as a pilot tone on the telemetry, tracking, and command (TT&C) link and then subsequently distributed to the VSAT users through the common TDMA downlink.

All VSAT users are capable of rate-synchronously transmitting narrowband and wideband data channels in the absence of spacecraft doppler induced by the inclination of the orbit. The MCS calculates the doppler correction (specifically, range rate divided by the velocity of propagation) for a representative user location by TT&C ranging. The doppler correction is then transmitted to all users via a broadcast channel in the TDM downlink. The user then calculates the doppler correction from the parameter received in the broadcast channel, modified by user latitude and longitude and the RF of the FDM uplink channel.

Instead of the MCS calculating the doppler correction for a representative user location from TT&C ranging and transmitting the doppler correction to all users, an alternative way of achieving synchronization is to provide separate probing channels to VSATS before initiation of uplink transmission. Using this method, the satellite will first have to provide probing channels which are shared by all users. Any VSAT user who wants to use the MCDD then sends a probing signal to the satellite. The satellite estimate the user's frequency error and sends a response signal to the downlink informing what the doppler and oscillator drift error is. The user then corrects its error.

The channelizers within MCDD do not strictly require the precise rate synchronism, i.e., doppler correction, provided by the above procedure. The only requirement for proper operation of the channelizer is that the modulation be placed within the channel filters. Demodulator performance is, however, improved by the more accurate placement of the modulation within the assigned channels, i.e., adjacent channel interference (ACI) and intersymbol interference (ISI) from unmatched channel filtering is reduced.

2.6.1.2 Modulation Choice for Future MCDD

The type of baseband pulse shaping we are using, as mentioned in section 2.4.3, will result in a modulated signal which will no longer be constant-envelope. (See Figure 2-13.) To improve the transmitter power efficiency, a constant envelope bandwidth efficient modulation scheme will be required for MCDD. We need to identify the best modulation/coding technique which will provide the required bandwidth efficiency and side lobe characteristics for MCDD and will be relatively simple with low risk. A tradeoff study should then be performed with respect to bandwidth efficiency, power efficiency, hardware complexity and weight, development risks, and speed/power requirements. From these tradeoffs a preferred modulation or combined modulation/coding technique can be selected.

In our demodulator design, we have a resampling filter which does matched filtering as well, and the filter coefficients reside in programmable RAM. It is straightforward to revise the resampling filter coefficients to cover other types of modulation schemes, e.g., TFM, MSK, GMSK, etc. Symbol decision output can also be input to decoder in the event we utilize combined modulation/coding.

3.0 POC STE DESIGN AND PERFORMANCE

3.1 Design Description

The POC model fully demonstrates the MCDD concept. Figure 3.1-1 shows a block diagram of the POC model and its relationship to the full MCDD.

The POC model design has been partitioned into the Demultiplexer (DEMUX) which includes the ADC, the Wideband (WB) Channelizer and the Narrowband (NB) channelizer and the Multirate Demodulator (DEMOD).

The DEMUX as presented in this report incorporates two major refinements with respect to the originally proposed design:

- A very efficient Window/Presum approach
- An NB channelizer design which processes 16 WB channels or 1/2 the full MCDD

The DEMOD concept has also been improved with respect to the proposal with:

- A simplified design
- A design adaptable to a future constant envelope modulation scheme

In addition to the above, both designs have been approached with a future ASIC implementation in mind.

Our versatile, low cost STE has also been improved with:

- MAC IIs as a controller
- LABVIEW for custom screen generation
- "C" for waveform generation
- Automated test procedure
- Full configurability for generation of new tests

Figure 3.1-2 shows an interface diagram of the POC model and STE.

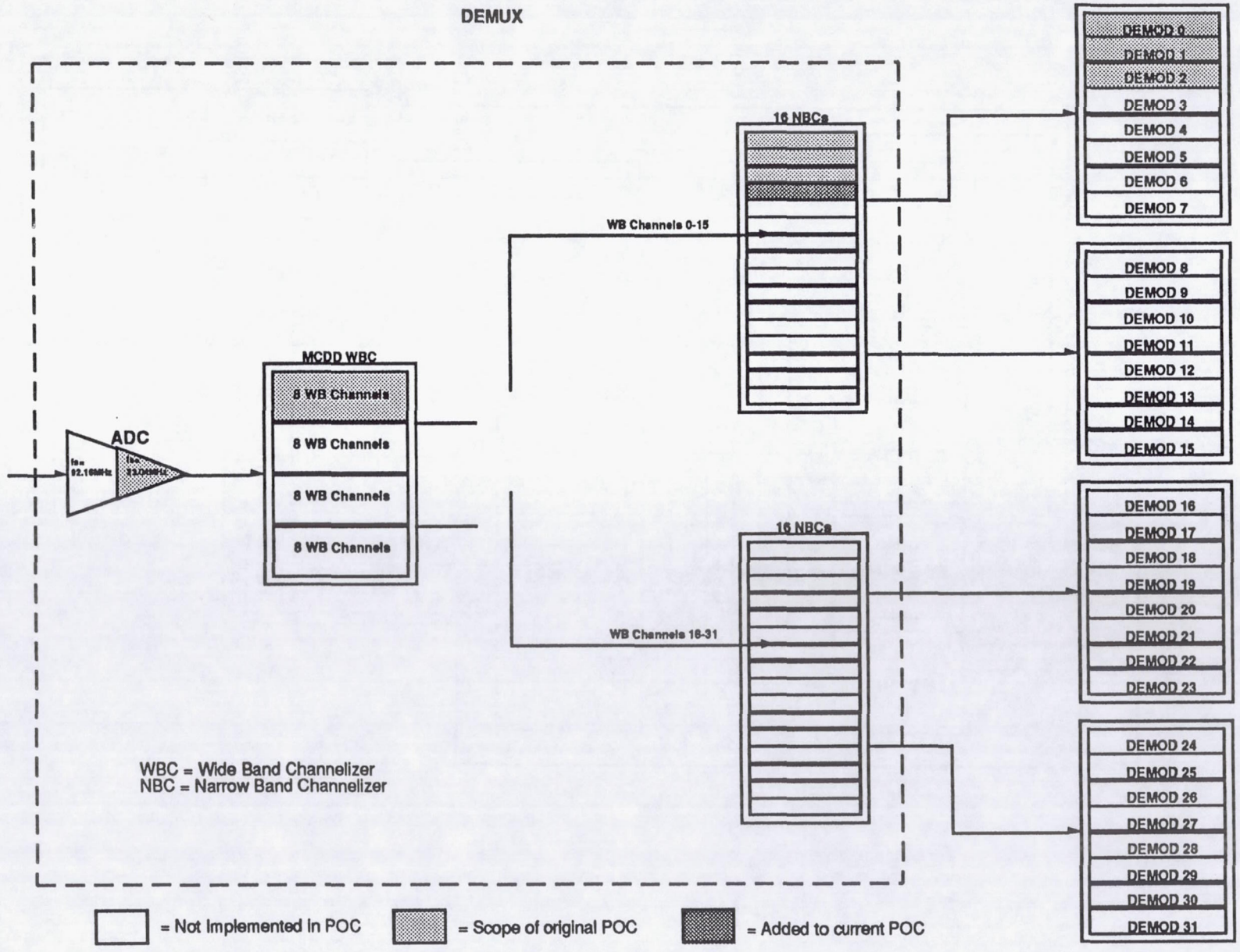


Figure 3.1-1 POC Model Block Diagram

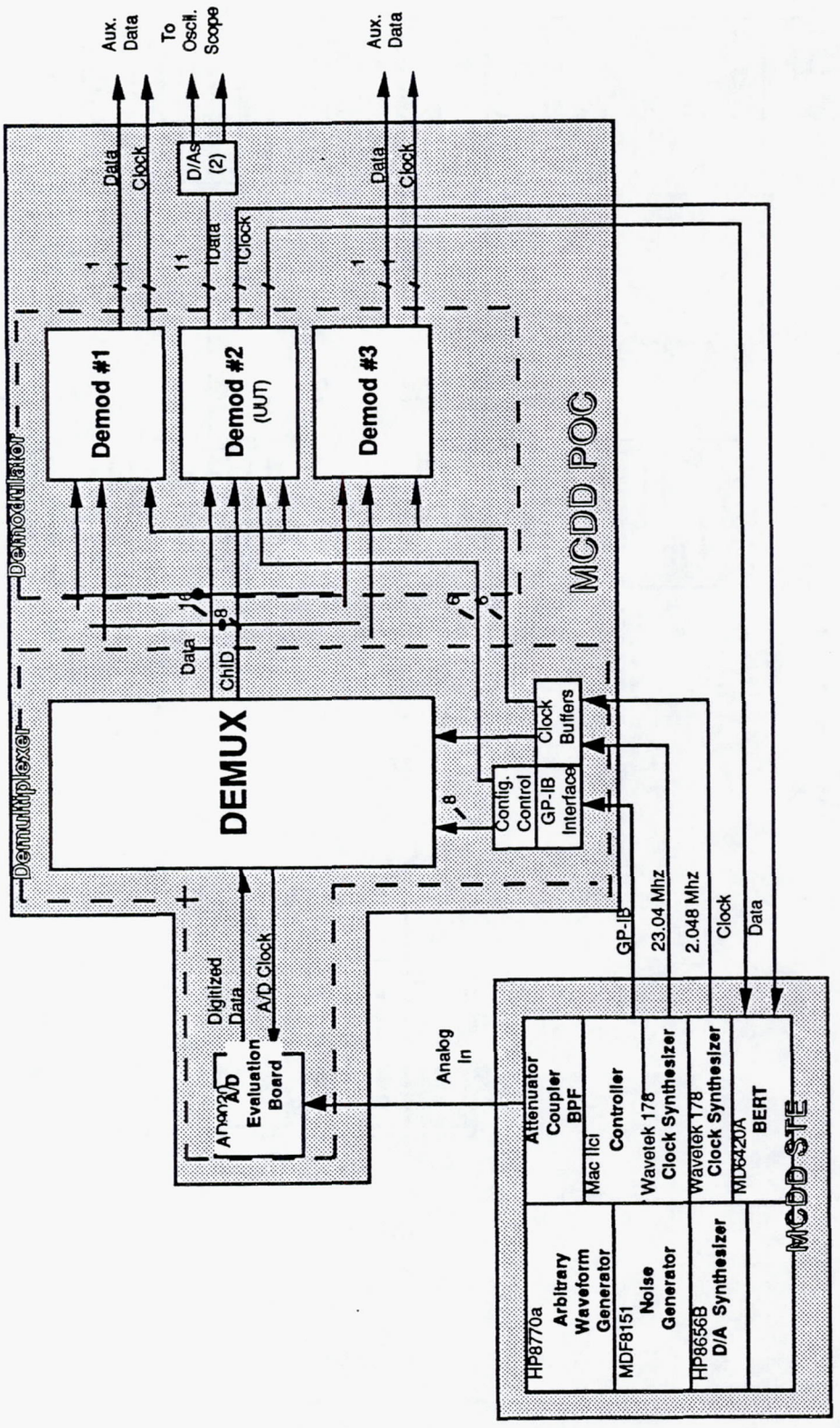


Figure 3.1-2 Interface Diagram of POC Model and STE

3.2 Requirements vs. Capabilities

See Table 3.2-1 below.

3.3 Derating Guidelines

No special derating guidelines will be applied in the design of the POC model. All detail design to follow will abide by the DDL Logic Design Guidelines, IOC 89-V125-01-88, dated 12 June 1989.

3.4 Packaging Approach

The MCDD POC model, as shown in Figure 3.4-1, will be enclosed in a 6 ft. double bay rack. All cables will be commercial, therefore eliminating any custom cables or harnesses.

The MCDD POC hardware will be enclosed in a MUPAC 13 slot card cage (see Figure 3.4-2). The wirewrap panels for both the DEMUX and DEMOD units will be the MUPAC 3466089-01 (6U; High Density Universal). The MCDD components are summarized below:

- STE Test Equipment (See Section 6)
- POC Hardware:

QTY	Description
1	MUPAC 3316625-03; 13 slot cage with high speed backplane
TBD	MUPAC TBD; DEMUX wirewrap panels
3	MUPAC 3476088-01; DEMOD wirewrap panels
1	ERBTEK EPI • 488; GPIB card
1	Brooktree BT101 EVM; D/A evaluation board
1	A/D 9020; analog devices A/D board

REQID	MCDD REQ POC DESIGN AND PERFORMANCE	CAPABILITY	VERIFIED BY
18	The POC model shall be configured to allow testing and validation of its critical components	Comply	Design
19	POC model shall fully demonstrate the MCDD concept and its architecture shall be expandable to a full MCDD	Comply	Design
26	The POC and STE shall be housed in a double bay rack and will include all necessary power supplies	Comply	Design
	The POC performance shall be compared to the results of the simulation as follows:		
36	The required Eb/No to achieve a BER of 5×10^{-7} for NB and WB channels with no adjacent channel interference (ACI)	Comply	Test
37	The BER vs Eb/No with ACI (8 dB dynamic range) for both NB and WB channels	Comply	Test
38	POC shall demonstrate its ability to acquire frequency offsets of 102.4 KHz for WB and 3.2 KHz for NB channels	Comply	Test
39	POC shall demonstrate its ability to acquire clock rate offsets of 51.2 Kbps for WB and 1.6 KBps for NB channels	Comply	Test
40	POC model model performance analyses shall be sufficient to verify or deny the continued candidacy of the POC model for the MCDD concept	Comply	Analysis

Table 3.2-1 Requirements vs. Capabilities

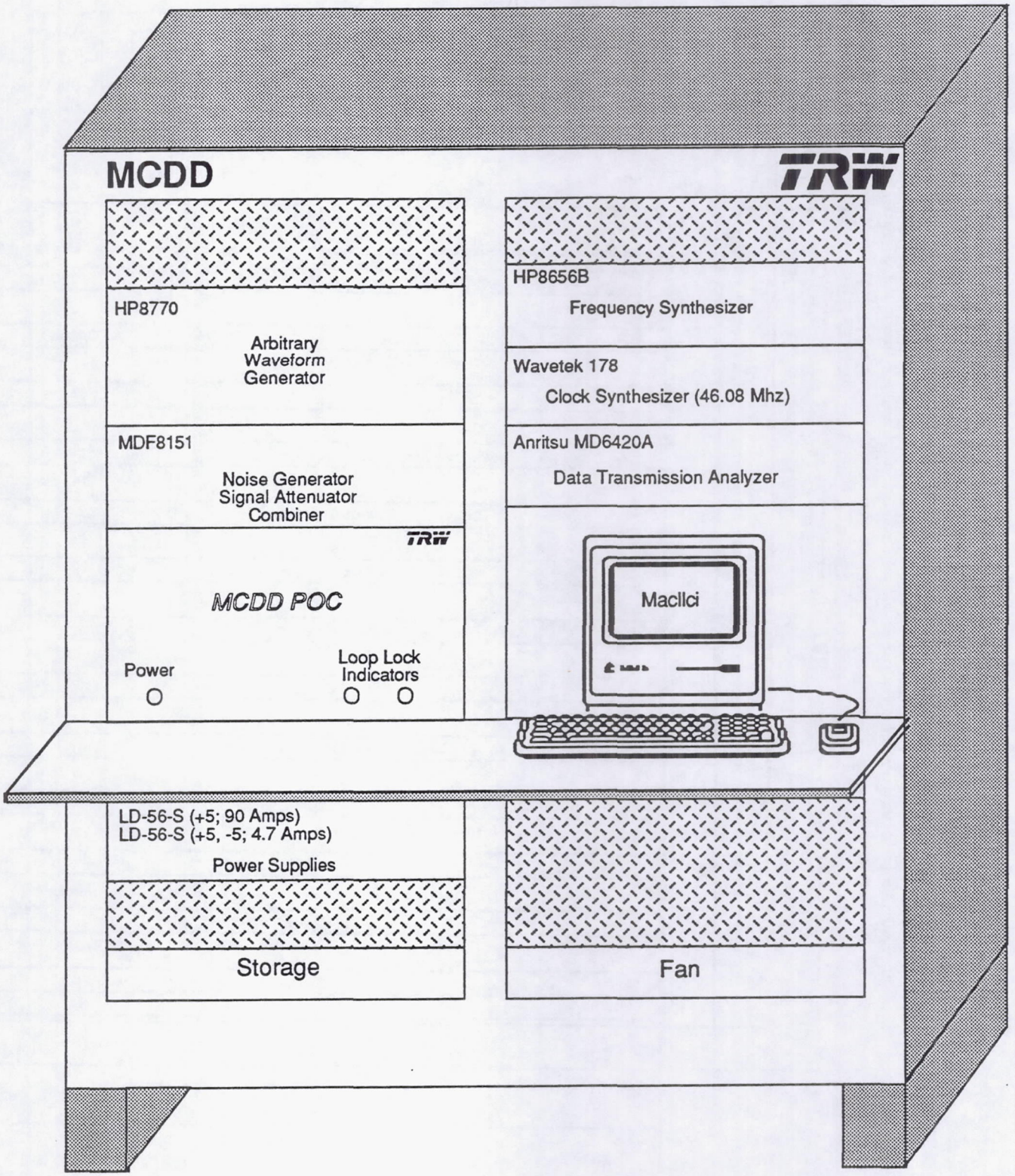


Figure 3.4-1 MCDD STE

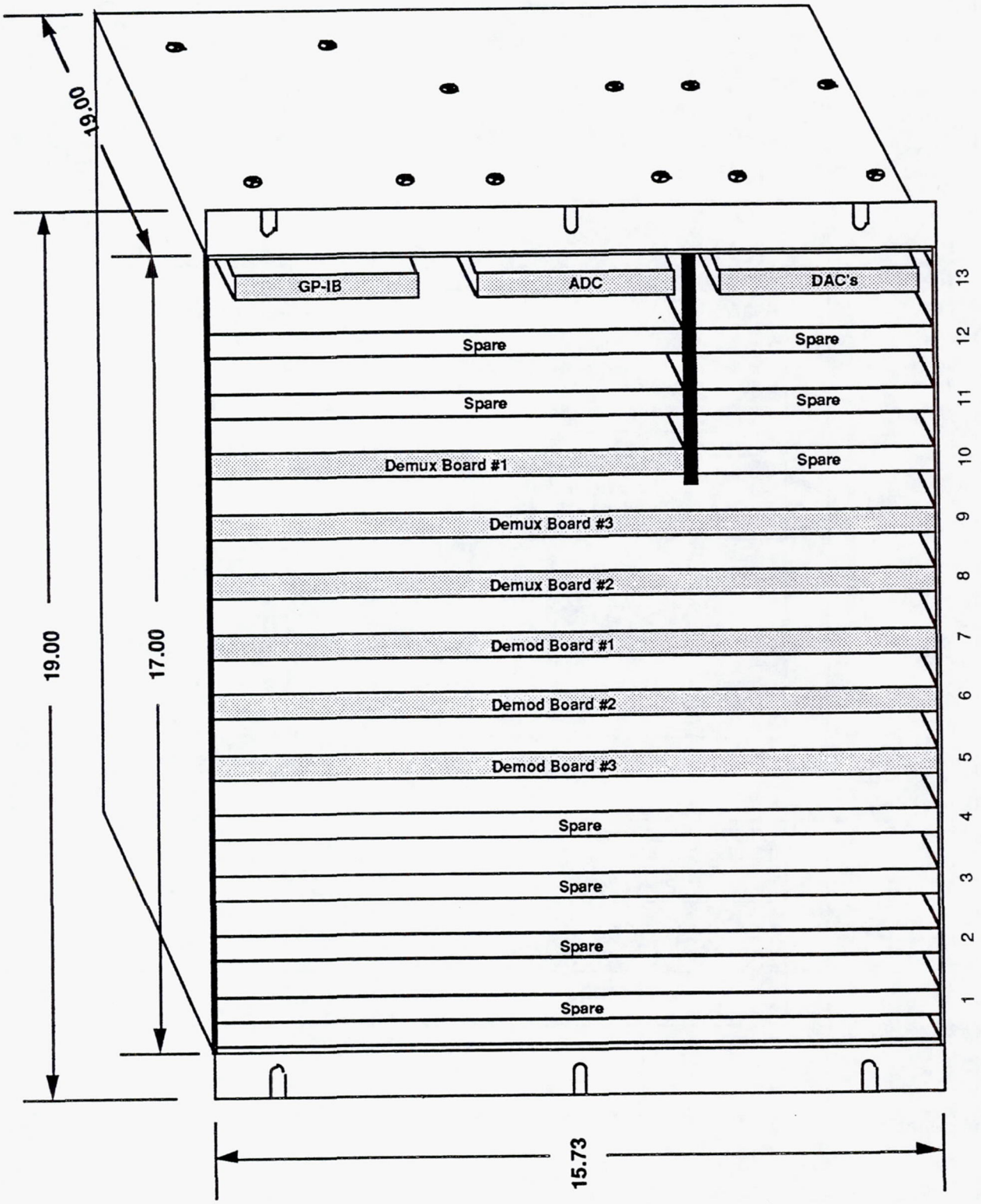


Figure 3.4-2 MCDD POC Drawer

3.5 Parts and Power Summary

See Table 3.5-1 below.

FUNCTION	PARTS	POWER
DEMUX	156*	68 W*
DEMOD	302	93 W

*Worst case (assumes 2K x 8 RAM)

Table 3.5-1 Power and Parts Summary

4.0 MCDD DEMULTIPLEXER

4.1 Functional Overview

The MCDD Proof of Concept (POC) Demultiplexer is a subset of the full size MCDD Demultiplexer (see Figure 4.1-1). It performs wideband (course) channelization of an analog input signal and, optionally, narrowband (fine) channelization on each of the wideband channels.

The first channelizer (WideBand Channelizer or WBC) applies a set of sixteen complex bandpass filters to the digital sequence out of the ADC. These sixteen equally spaced FIR filters are identical to one another except in center frequency.

Since the second level of channelizers (NarrowBand Channelizers or NBCs) and the MCDD demodulators require baseband inputs, the WBC also performs the required operations to shift each filter output down to dc.

Each NBC is dedicated to a particular wideband channel out of the WBC. A NBC may be configured to either pass the data from the WBC, unaltered, to an MCDD Demodulator or to narrowband channelize the data before sending it. In the latter case, a set of thirty-two complex, equally spaced bandpass FIR filters is applied to the NBC input data. As in the WBC, each NBC output is shifted to baseband.

The WBC and NBC requirements are very similar and both are efficiently implemented using time domain DFT techniques. Some notable differences are that the WBC input is real while the NBC input is complex and that the input sampling rate to a NBC is significantly less than that of the WBC.

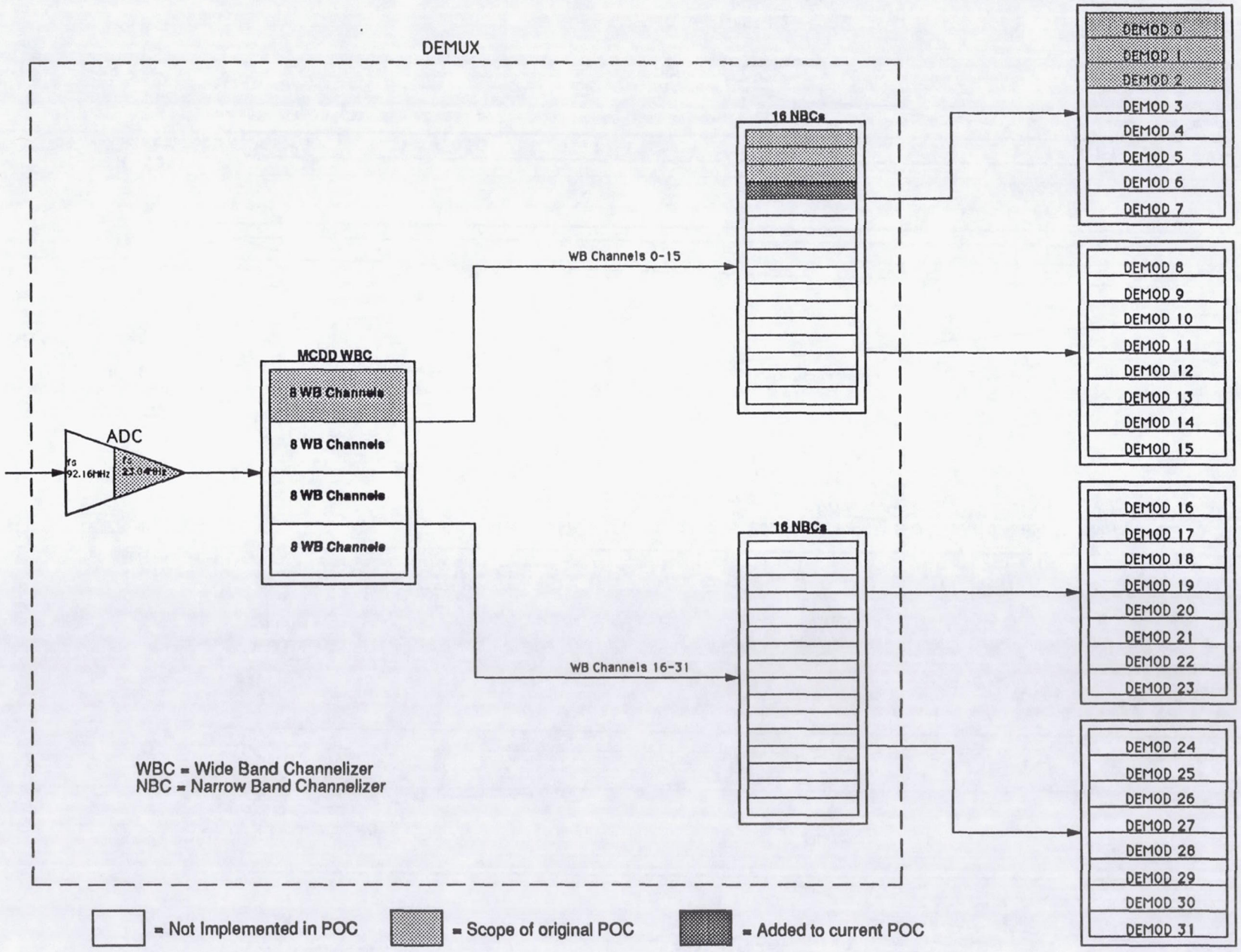


FIGURE 4.1-1: POC SUBSET OF MCDD

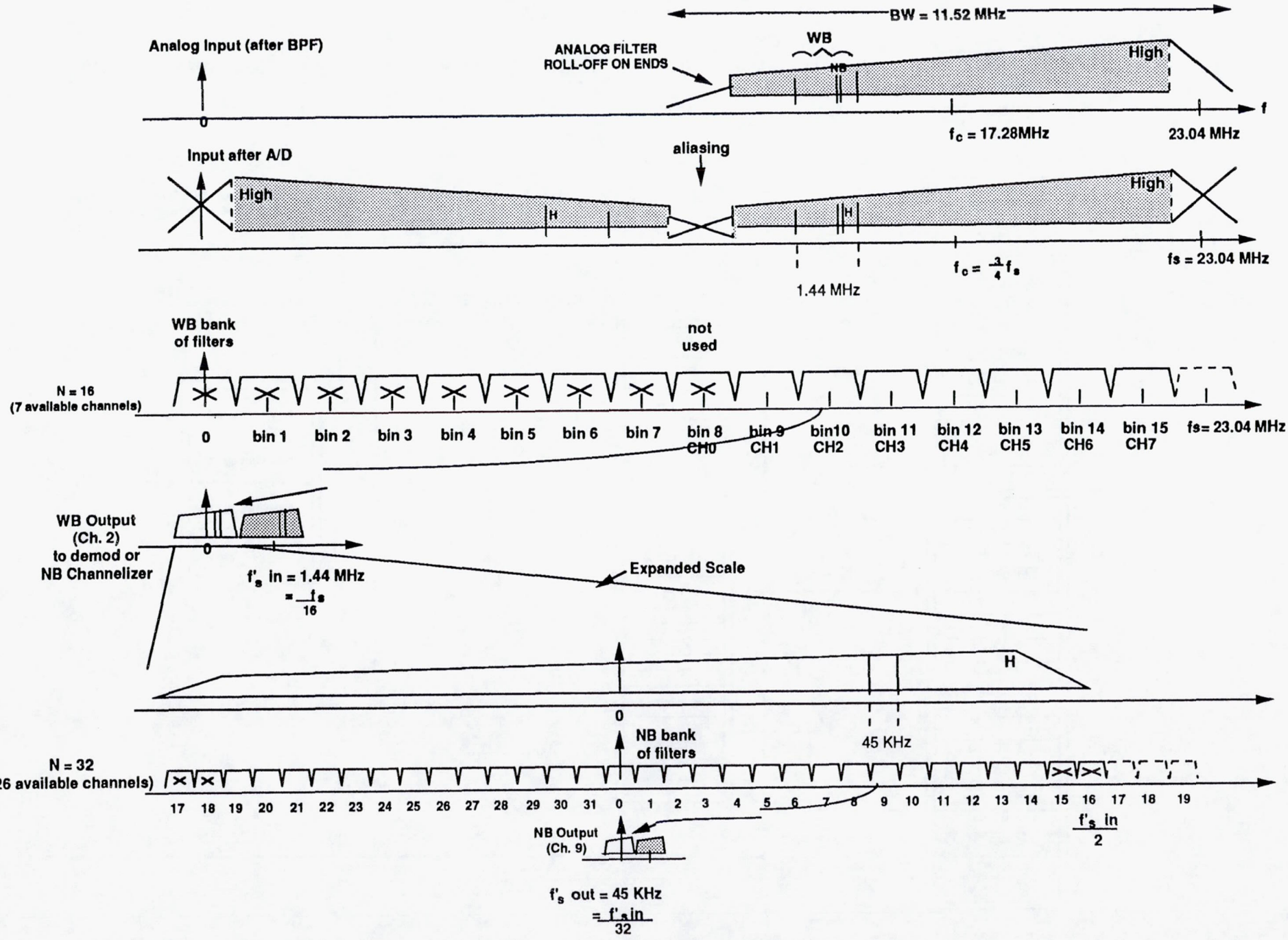


Figure 4.1-2: MCDD POC FREQUENCY PLAN

Table 4.2-1 Requirements vs. Capabilities

REQID	MCDD REQ DEMULTIPLEXER	CAPABILITY	VERIFIED BY
16	The MCDD POC model shall implement and demonstrate the Time Domain FFT concept and its ability to perform wideband and narrowband channelization	Comply	Design
19	POC model shall fully demonstrate the MCDD concept and its architecture shall be expandable to a full MCDD	Comply	Design
20	The POC model FDM composite signal shall consist of 8 WB channels	Comply	Design
21	The POC model shall demultiplex and demodulate 3 WB channels, any of which can be further subdivided into 28 NB channels	Comply	Design
23	The NB channels shall have a data throughput rate of 64 Kpbs	Comply	Design
24	The POC shall implement WB channels at 2.048 Mbps	Comply	Design
27	The interface between the POC and the STE shall be clearly defined	Comply	Design
30	The POC Model shall be fabricated with commercial grade components. Operating temperature range shall be 0 to 70 degrees centigrade	Comply	Design

Table 4.2-1 Requirements vs. Capabilities (Cont'd)

REQID	MCDD REQ DEMULTIPLEXER	CAPABILITY	VERIFIED BY
31	Best commercial design and fabrication practices shall be used in the development of both the POC model and the STE	Comply	Design
33	The POC Demux shall be designed with the following parameters: Presum ratio = 16 Decimation ratio = 16 (WB), 32 (NB) Window length = 256 (WB), 512 (NB) Window type = Kaiser Window quantization = 16 bits Sampling frequency = 23.04 MHz (WB), 1.44 MHz (NB) A/D resolution = 8 bits A/D loading factor = 1/4	Comply	Design
34	The full size MCDD Demux shall be designed with the following parameters: Presum ratio = 16 Decimation ratio = 64 (WB), 32 (NB) Window length = 1024 (WB), 512 (NB) Window type = Kaiser Window quantization = 16 bits Sampling frequency = 92.16 MHz (WB), 1.44 MHz (NB) A/D resolution = 8 bits A/D loading factor = 1/4	Comply	Design

* Pages 75-114 Proprietary information. Permission to publish not received at time of printing.

5.0 MCDD DEMODULATOR

5.1 Functional Overview

The MCDD POC, shown in Figure 5.1-1, will contain three identical digital demodulator boards, one board for each channel being processed. The demodulator consists of five major functional blocks as shown below. These blocks are:

1. A resampling filter to generate exactly two complex signal samples per symbol;
2. A derotate complex multiply to remove residual carrier from these samples;
3. Symbol decision to determine the received two-bit symbol (Differentially encoded OQPSK),
4. A carrier tracking loop to estimate the carrier phase offset to be derotated; and
5. A symbol sync loop to determine any timing offset to be removed by the resampling filter.

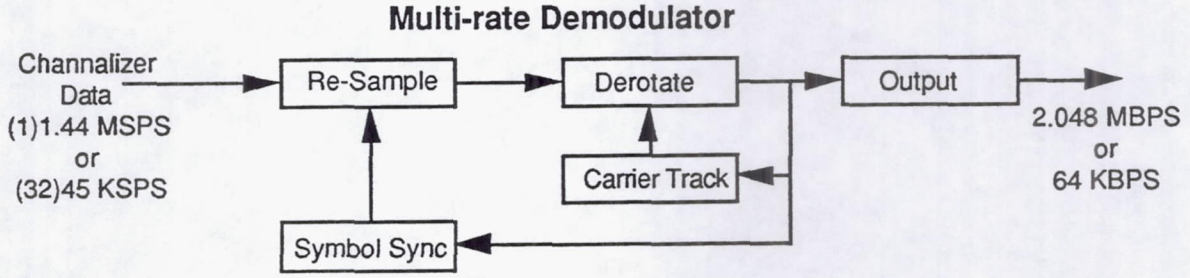


Figure 5.1-2

Each demodulator can be configured as a single 2.048 Mbit/sec wideband (WB) channel, or as 32 independent 64 Kbit/sec narrowband (NB) channels.

For the POC, the three demodulators can be configured as either a WB or NB channel. When in NB mode the demodulator hardware is time multiplexed between the 32 channels, eliminating the need for duplicate hardware running at a slow rate. Data is input to each of the demodulators from the demultiplexer at a rate of 1.44 MSPS. This data will be consecutive time samples for a single wideband channel, and time multiplexed samples from 32 narrowband channels. The output of the POC will be either a 2.048 Mbit/sec demodulated data stream from the wideband channel under

test, or any one of the thirty-two 64 Kbit/sec narrowband channels. Data from the other wideband channels will be available.

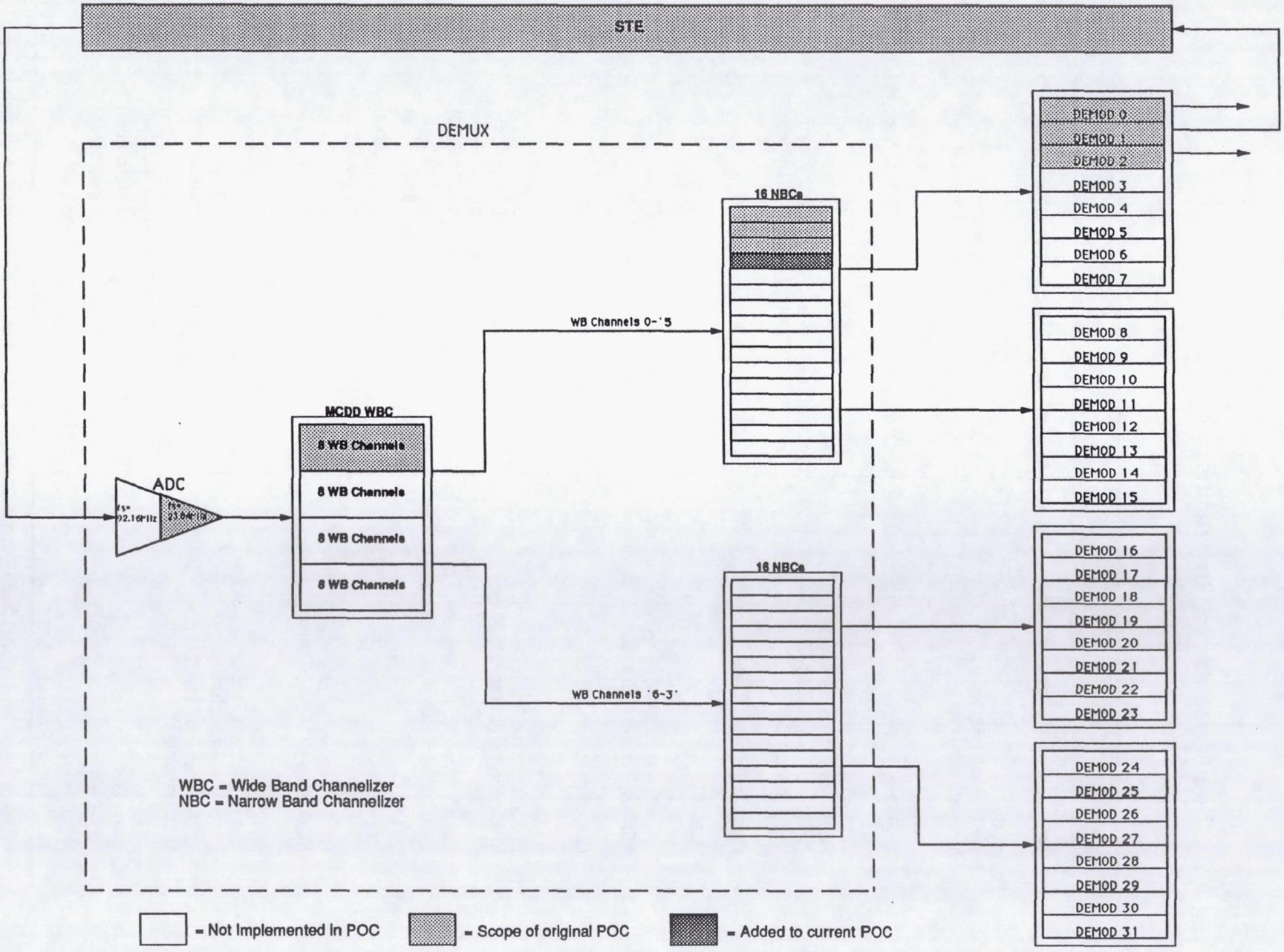


FIGURE 5.1-1: POC SUBSET OF MCDD

5.2 Requirements vs. Capabilities

Requirement	Capability
Modulation Format	
Differentially Encoded S-QPSK	Comply; Can accommodate other formats w/o HW mod.
Data Rate	
Wideband 2.048 Mbit/S	Comply
Narrowband 64 Kbit/S	Comply
Resampling Filter	
Filter Size: 16 Taps	Comply; Could accommodate less than 16 w/o HW mod.
Time offsets: 32 Possible	Comply
Filter Types (STE Selectable)	
Square-Root-Raised-Cosine-Interpolation	Comply (PROM defined)
Interpolation	Comply (PROM defined)
Output Precision: 8 bits	Comply
Derotate	
Function	
$I = X_i \cdot \cos[\varnothing(\text{error})] + X_q \cdot \sin[\varnothing(\text{error})]$	Comply
$Q = X_q \cdot \cos[\varnothing(\text{error})] - X_i \cdot \sin[\varnothing(\text{error})]$	Comply
Output Precision: 5 bits	Comply
Carrier Tracking Loop	
Phase Estimate Precision: 8 bits	Comply
Phase Error = ArcTan(Q/I) - θ(opt)	Comply (PROM defined)
Loop Filter Precision: 24 bits	Comply
Loop Bandwidth: (symbol rate) • 10^{-2}	Comply (switch selectable)
Loop Parameters:	
$K_L = 2^5$	Comply (switch selectable)
$K_i = 2^{-1}$,	Comply (switch selectable)
$K_T = 2^4$	Comply (switch selectable)
NCO Precision: 24 bits	Comply
NCO Output Precision: 8 bits	Comply
Symbol Sync Loop	
Phase Estimate Precision: 5 bits	Comply
Loop Filter Precision: 24 bits	Comply
Loop Bandwidth: (symbol rate) • 5×10^{-3}	Comply (switch selectable)
Loop Parameters:	
$K_L = 2^7$	Comply (switch selectable)
$K_i = 2^0$	Comply (switch selectable)
$K_T = 2^8$	Comply (switch selectable)
NCO Precision: 24 bits	Comply
NCO Output Precision: 5 bits	Comply

Table 5.2-1 Requirements vs. Capabilities

Multi-Rate Demodulator

TRW

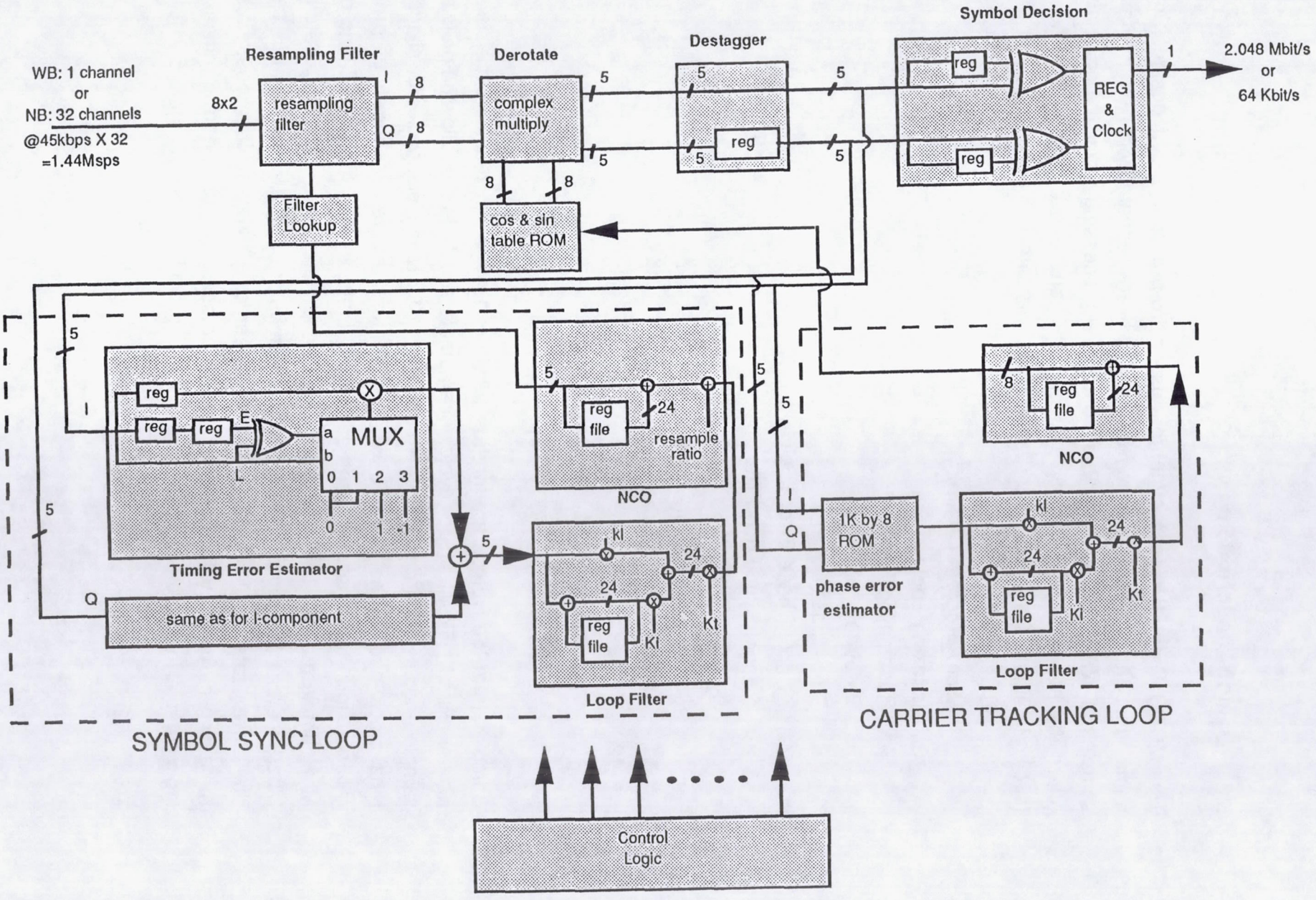


Figure 5.3 Multi-Rate Demodulator

5.3 Design Description

The MCDD Demod uses a synchronous, micro-program based design. Since the same functions will be performed by the hardware repeatedly for each channel (or samples in WB mode) with minimal conditional processing, a micro-coded approach offers the necessary complexity with minimal parts and control logic. The Demod (shown in Figure 5.3) consists of the following functional components :

1. Clock Logic
2. Micro-program Control
3. Indexing Logic
4. Resampling Filters
5. Derotate
6. De-Stagger Buffer
7. Symbol Phase Error Logic
8. Symbol Sync Loop Filter
9. Symbol Sync NCO
10. Carrier Phase Error Lookup
11. Carrier Tracking Loop Filter
12. Carrier Tracking NCO
13. Output Buffer / Channel Mux
14. Lock Detect

Samples from the Demux are input at a rate of 1.44 MSPS resulting in sixteen 23.04 Mhz or eight 11.52 Mhz clock cycles in a sample epoch. In the following descriptions a sample epoch will be defined as either eight 11.52 Mhz clock cycles or sixteen 23.04 Mhz clock cycles.These rates were driven by the resampling filter processing requirements, which are two separate 16 tap filters, for both I and Q, during one 1.44 Mhz sample period. The Resampling Filter, and Derotate run at a clock rate of 23.04 Mhz, whereas the remaining processing elements run at a clock rate of 11.52 Mhz. The slower rate of 11.52 Mhz rate was chosen to alleviate timing constraints on the remaining hardware with providing enough processing cycles, and to minimize clock logic complexity. A detailed hardware block diagram is shown in Figure 5.3-1.

Interpolation Process

Data samples are input to the Demod at 45KSPS (NB) and 1.44MSPS (WB), with the ideal sample rate being 64KSPS (NB) and 2.048MSPS (WB). The input waveform has a sample period of T_{IN} = 1/45KSPS, and we want the output of the Resampling Filter to have a sample period of T_{OUT} = 1/64KSPS (2 samples per symbol). The relative time location that each R.S. Filter output will occupy is determined by the symbol sync NCO. To get the desired R.S. Filter output rate with $T_{IN} \cdot T_{NCO} = T_{OUT}$, we see that we need $T_{NCO} = T_{OUT}/T_{IN} = (1/64)/(1/45) = 45/64$.

By updating the NCO and monitoring the overflow status, it can be determined if the current input data samples are sufficient to calculate one or two data points out of the R.S. Filters. Each sample epoch (1.44 Mhz) the NCO will be updated, if it overflows, only one R.S Filter output will be valid the following sample period. If the NCO does not overflow on the first update, it is updated again and two R.S. Filter outputs will be valid the next sample period. Although the instantaneous data rate out of the R.S. Filter varies, the average data rate, in absence of offset, will be 64 Ksamples/sec NB, and 2.048 Msamples/sec WB.

Destagger

Due to both the rate interpolation, and the staggering of the I and Q arms, a de-stagger buffer is needed. The symbol sync loop needs a current midpoint, previous transition, and previous midpoint samples for determining the timing error. The carrier tracking loop needs the current midpoint sample to determine the phase error estimate. The output decision logic needs a current and previous midpoint samples to make a symbol decision. The requirement of needing three samples, along with the staggering and rate interpolation results in eight memory locations to handle the worst case scenario.

Processing for the aforementioned processing elements is conditional on there being sufficient valid data points in the de-stagger buffer.

5.3.1 Clock Logic

For the POC, the Demux will send two clocks to the Demod; 23.04 Mhz and 11.52 Mhz. For Demod stand-alone operation a 46.08 Mhz TTL level clock will be input and the

two system clocks (23.04 and 11.52 Mhz) will be generated via a down-counter. For RAM/FIFO writes, an inverse 11.52 Mhz clock will be generated to allow NAND gating a write enable control signal to generate the write strobe. This write enable clock will have one less buffering level than the distributed system clocks so that the NAND gating required will not cause unnecessary clock/write strobe skew. Clocks will be buffered and distributed via 244 drivers.

MCDD Demodulator Hardware Block Diagram

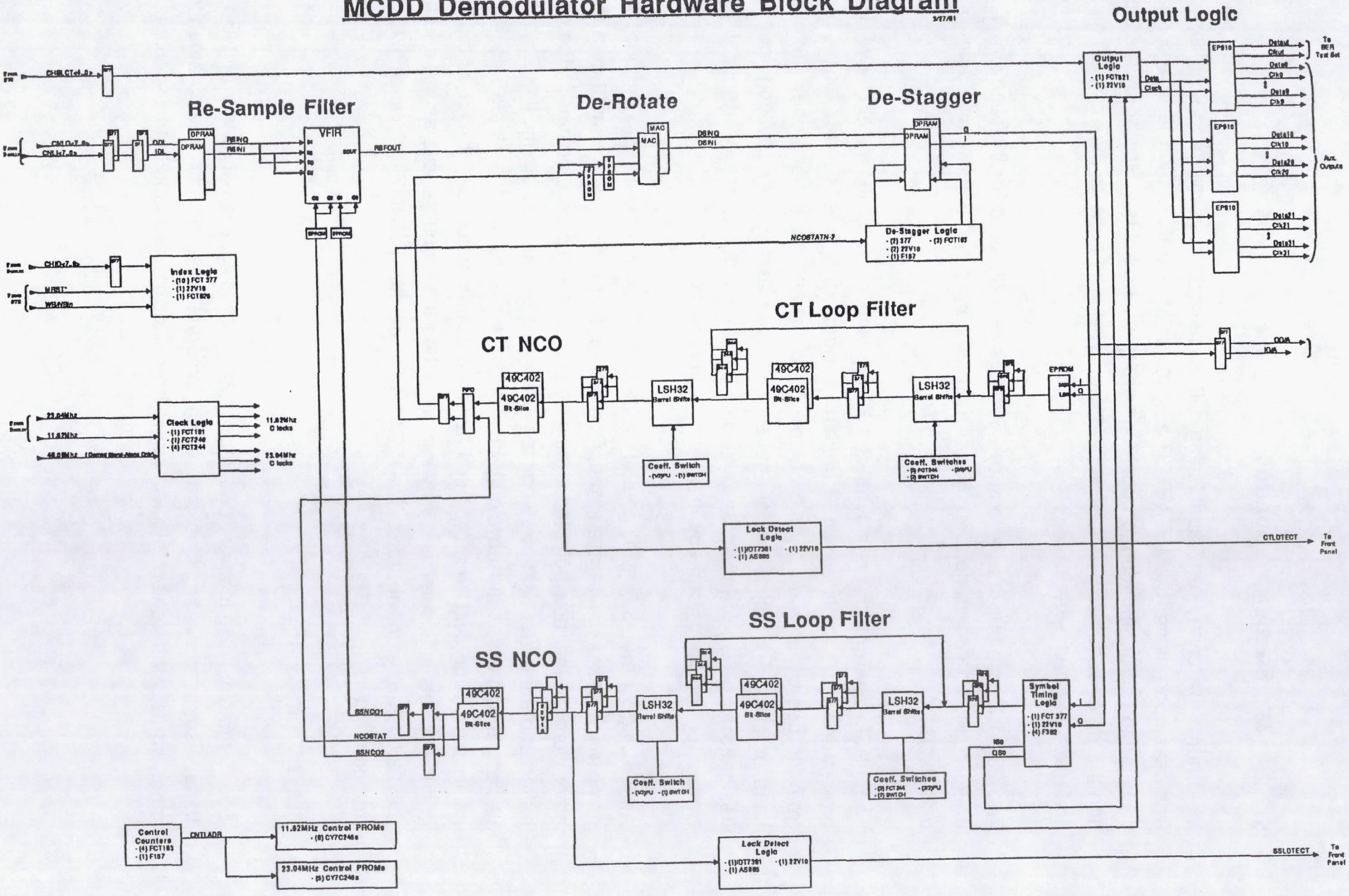


Figure 5.3-1

5.3.2 Micro-Program Control

Most hardware control and addressing will be performed in micro-code. Micro-code was developed using the METASTEP assembler on a VAX Station II. The code was divided into two independent groups. One group controls 23.04 Mhz hardware blocks, and the other controls the 11.52 Mhz blocks. This was done to minimize complexity and micro-program stores.

The 23.04 Mhz group has a total of 256 lines with 66 lines for initialization. This is broken up as 16 re-sample addresses in 16 different sequences for a total of 256 unique states.

The 11.52 Mhz group has a total of 16 lines with no lines for initialization. This is broken up as 1 sample epoch (8 cycles) for when valid data is ready for processing from the destagger buffer, and 1 sample epoch when data is not ready. (total of 16 lines or cycles) Processing for the symbol sync and carrier tracking loops was designed to be as identical as possible, this enabled the use of identical control signals for both loops, thereby minimizing parts and complexity.

Addressing for the 23.04 Mhz control PROMS is mode dependent. If WB mode, the re-sample addresses must cycle thru the circular buffer at the 1.44Mhz input data rate. In other words, every new point input must be placed in the oldest location in the circular buffer, and the current set of 16 points must be accessed accordingly. If NB mode, the re-sample addresses must cycle thru the buffer at the 45 Khz input data rate, with the same addressing sequence repeated 32 times. (same sequence for each of the 32 NB channels) This is accomplished by selecting the proper counter bits as the address to the 23.04 Mhz control store. The 11.52 Mhz control PROMS addressing is mode independent.

5.3.3 Indexing Logic

Due to the pipelining inherent to demodulator processing, it is necessary (in NB mode) to have some processing blocks accessing different channels data at the same time. In other words, all hardware blocks cannot be using the same index to access its local

memory at the same time. This requires the generation of time delayed versions of the same index with the proper time synchronization.

The channel ID word sent from the Demux is comprised of a 3 bit WB channel index (used as a demod board select) and a 5 bit NB channel index (channel index if in NB mode). If in NB mode, the 5 bit NB channel ID is registered in as the channel index. Versions of this 5 bit index are delayed and synchronized to give the proper timing relationships with the various hardware blocks.

If in WB mode, the channel index is forced to zero (00000) since only one channels memories will be accessed.

5.3.4 Resampling Filters

The resampling filters perform the necessary interpolation to create the midpoint and transition samples, they also perform the pulse shaping matched filters. The symbol rate is compensated by either generating one or two points through interpolation in the resampling/pulse shaping filters. Even though only one point is valid from the R.S. Filters, both will be calculated. The first point (I and Q) out will always be valid, with the second complex pair being valid conditional on the symbol sync NCO status.

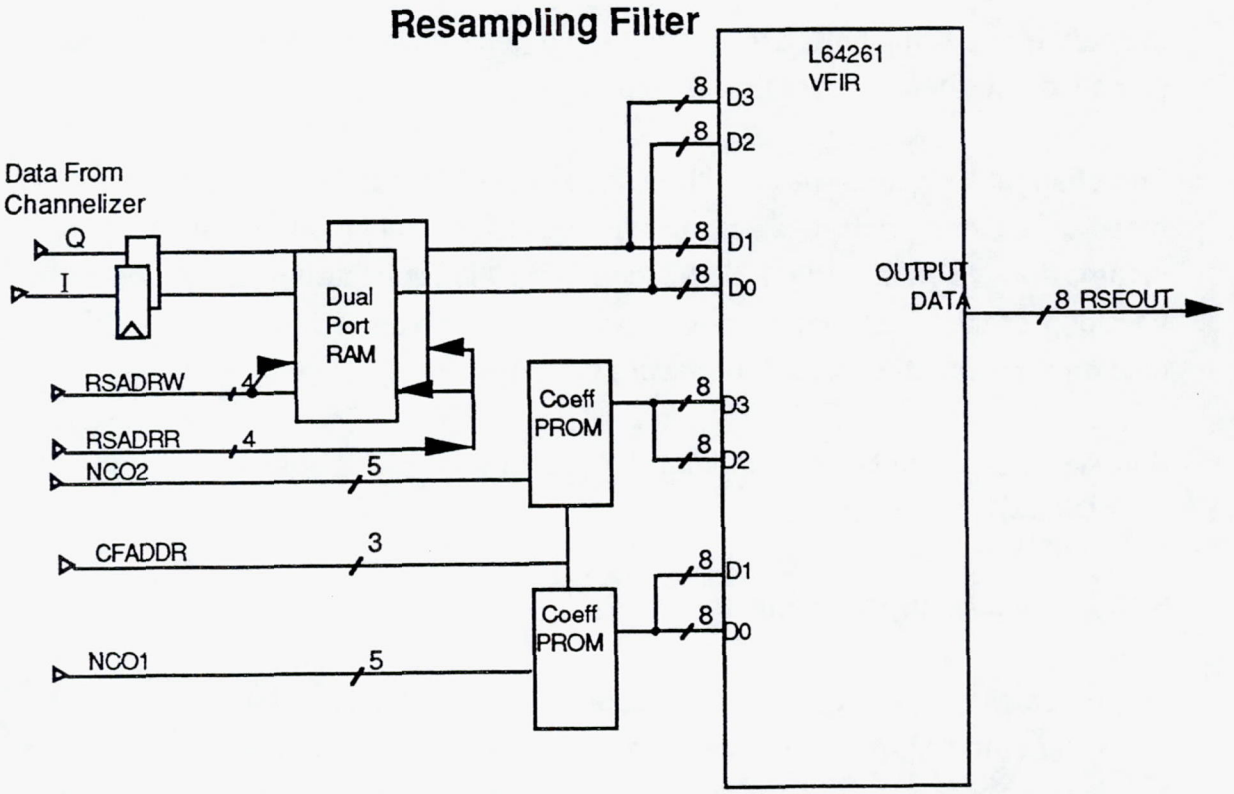


Figure 5.3.4-1

The hardware block is shown in Figure 5.3.4-1. The input data is buffered in a Dual-Port RAM to allow circular buffering of the incoming data samples. The channel ID is decoded to determine which data samples are selected from the shared data bus. This data bus, from the demultiplexer, is shared among the three demodulators. In NB mode the Dual-Port RAM is configured as 32 independent circular buffers, in WB mode the RAM is configured as one buffer.

The 16 consecutive complex data points are accessed from RAM at a rate of 23.04 Mhz and input to a LSI Logic L64261 VFIR. During one sample epic, the resample filters will interpolate either one or two complex samples (4 filters total). The VFIR chip, which is configured as four independent 16-bit multiplier/accumulators (MAC), performs the necessary interpolation/matched filtering for both I and Q paths. Both I and Q are input to two data inputs of the VFIR. Each filter requires 16 taps, and there are 32 sets of these coefficients (one for each timing offset) resulting in a 512 word coefficient memory. In addition there is another 32 sets of 16 tap filters that were generated without the square-root-raised-cosine pulse shaping filter to allow the the

channel to operate without the benefit of pulse shaping. The filter set is switch selectable. Window coefficients are stored in EPROM. The interpolation filter with the appropriate timing offset, or which of the 32 sets of coefficients, is selected by the 5-bit symbol sync NCO value. Each coefficient is 8 bits wide. The 8-bit output, from both I and Q, of the resampling filters is input to the derotate.

Therefore it was determined, by systems engineering BOSS simulation, that with a 8x8 multiply (resulting in 16 bits:<15..0>) and the 16 accumulates performed by the resampling filters, bits <14..7> should be selected as the final output of the resampling filter. This corresponds to bits <12..5> (unshifted) output from the VFIR.

5.3.5 Derotate

The derotate is performed by two 8x8 Multiply-Accumulators (TMC2208) as shown in Figure 5.3.5-1. These have a 25 Mhz speed rating.

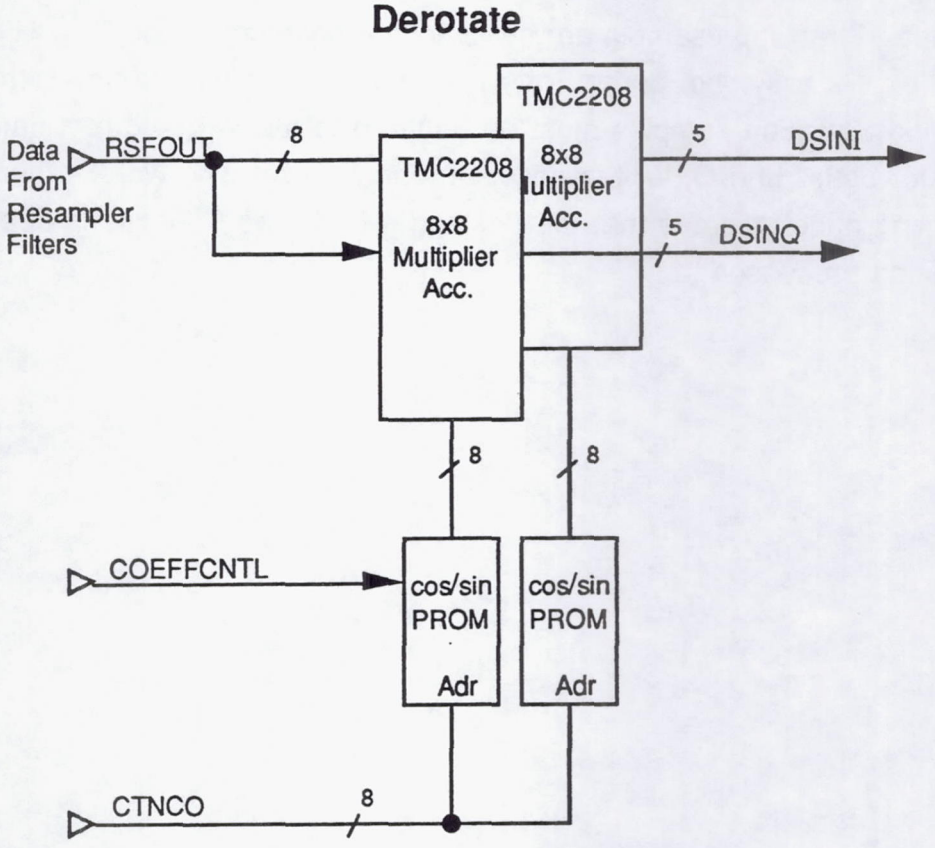


Figure 5.3.5-1

The math function desired is:

$$[Xi(n) + jXq(n)]*[\cos(err) - j\sin(err)] \Rightarrow$$

$$DSINI(n) = Xi(n)*\cos(err) + Xq(n)*\sin(err) \quad ; \text{"I"}$$
$$DSINQ(n) = Xq(n)*\cos(err) - Xi(n)*\sin(err) \quad ; \text{"Q"}$$

The lookup table is configured such that cos(err) is in the lower 256 locations and sin(err) is in the upper 256 locations. The "Q" MAC is configured to subtract the second product from the first, whereas the "I" MAC is configured to add the second product from the first. The worst case overflow scenario can never happen during the accumulates, (due to the multiplication of sin/cos) therefore bits <15..11> are selected as the output of the derotate. The choice of output bits was verified through BOSS simulation. The five bit result, both I and Q, are input to the destagger buffer.

5.3.6 Destagger

A midpoint and transition sample are not output every sample epoch, and I and Q are staggered by 1/2 a symbol period (one midpoint or transition sample), therefore the midpoint and transition samples must be buffered to allow the correct samples to be available, for both I and Q, for the necessary processing. The worst case scenario of symbol timing offset dictates that the destagger buffer be 8 locations deep (for each channel being processed).

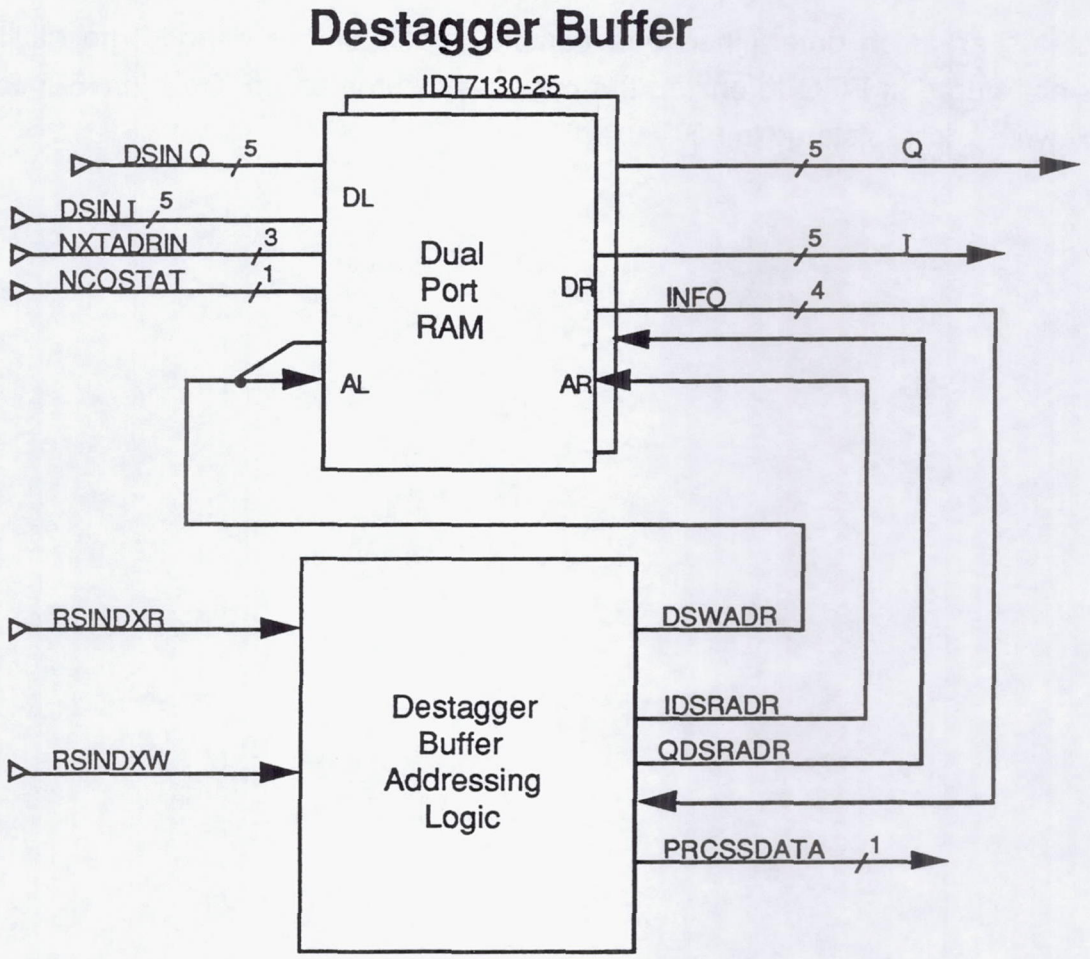


Figure 5.3.6-1

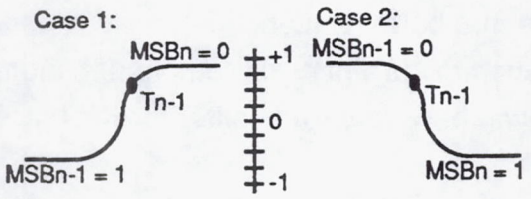
Also stored in the de-stagger buffer (shown in Figure 5.3.6-1) is addressing and NCO status information necessary to maintain buffer and processing control. This information is stored at the end of the data buffer locations (one information memory location for each channel). The information consists of a three bit address that determines the next data address to be written, and a symbol sync NCO status bit. The read addresses for the data points are determined logically from the next write address and NCO status.

In WB mode it is necessary to use the next write address during the following sample epoch since all operations are on only one channel. However in narrowband mode, the next write address is determined one sample epoch before it is used, due to pipeline delays in the data path. The carrier tracking NCO values and symbol sync

NCO status are also determined one sample epoch before needed, so all three entities are stored in FIFO to ensure the correct synchronization. Only in NB mode is the next write address stored in FIFO used.

5.3.7 Symbol Timing Error Logic

Timing error or symbol sync phase error is calculated for both I and Q independently and the result added (shown in Figure 5.3.7-1). The MSBs of two consecutive midpoint samples are compared and determines if 0, +1, or -1 is multiplied with the transition sample as shown below.



MSBn	MSBn-1	Err
0	0	0
0	1	+Tn-1
1	0	-Tn-1
1	1	0

The case of no symbol timing error will result in a transition sample equal to zero. When the transition sample is behind the zero crossing point the NCO needs to be sped up or a positive error estimate should be generated. When the transition sample is in front of the zero crossing point the NCO needs to be slowed or a negative error estimate should be generated. The most significant four bits is used as a timing estimate, with the sign adjusted error for both I and Q being summed to form a composite 5 bit error estimate. This 5 bit error estimate is placed in the least significant 5 bits and sign extended to 24 bits for input to the loop filter.

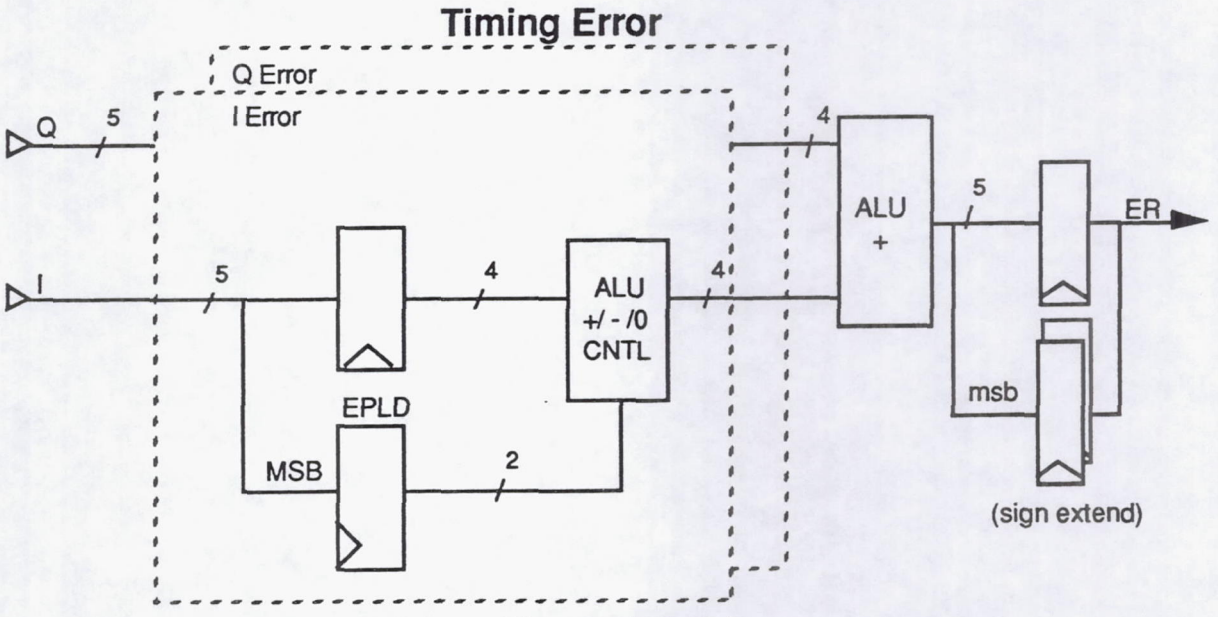


Figure 5.3.7-1

5.3.8 Symbol Sync Loop Filter

The loop filter operations are performed for each channel during a single sample epoch. (shown in Figure 5.3.8-1) The processing is as follows:

1) Pass previous loop filter result to NCO while shifting the error estimate by Kl. (2 cycles)
2) Place the shifted error estimate in a temporary register.
3) Pass unshifted error estimate thru barrel shifter.
4) Add previous error accumulation to current error sample and store.
5) Send current error accumulation back to barrel shifter for Ki shift. (2 cycles)
6) Add Kl*Err to Ki*Sum(Errs) and store.

Processing requires two register locations for each channels loop filter. All accumulations are 24 bits wide. It should be noted that all memory/register locations mentioned in the symbol sync and carrier tracking loop descriptions are referencing the register files located in the IDT49C402B Bit-Slice. It should also be noted that all shifts performed require two clock cycles. This is necessary since the 32 bit barrel shifter can only output 16 bits during one cycle. All K's are switch selectable to allow the use of different loop bandwidths.

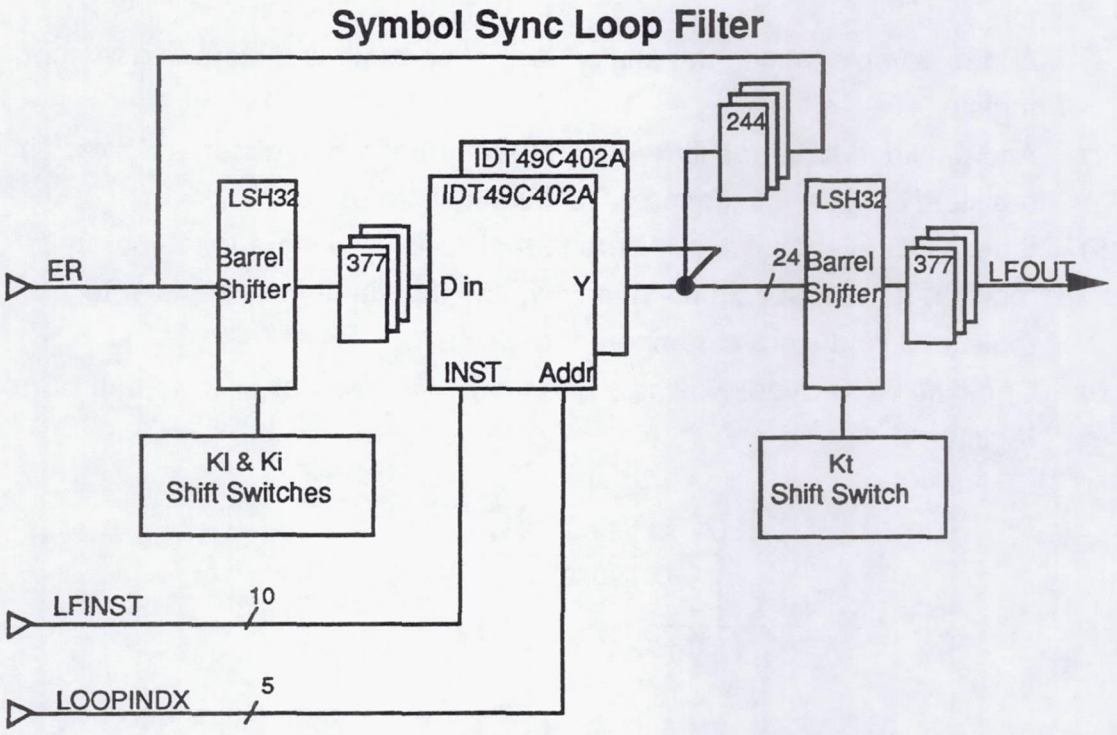


Figure 5.3.8-1

5.3.9 Symbol Sync NCO

The NCO operations are performed for each channel during a single sample epoch (eight 11.52 Mhz cycles). The NCO, shown in Figure 5.3.9-1, must create at most two NCO results for each channel. If the NCO overflows on the calculation of the first result, then that first result is stored in both NCO register locations for that channel. If however the NCO does not overflow, two unique NCO results will be stored in the two register locations. This reduces control complexity when generating the next NCO result, for the previous valid result will always be stored in the second register location. Stored in an unused bit of the second register location will be the NCO overflow status. The input to the NCO Bit-Slice is passed thru a set of 22V10 PLDs to enable the input of the re-sample ratio.

Processing is as follows:

1) Pass previous NCO results to the Re-Sampling filter coefficient PROMs, while shifting the previous loop filter result by Kt.(2 cycles)
2) Place the shifted loop filter result in a temporary register.

3) Add re-sample ratio to the shifted loop filter result and store in a temporary register.
4) Add previous NCO result (register#2) to temporary register and store in register#1, while monitoring NCO overflow status.
5) If the NCO overflowed, add zero to register#1 and store in temporary register. If the NCO did not overflow, add the temporary register to register#1 and store in temporary register.
6) Combine NCO overflow status and temporary register and store in register#2.

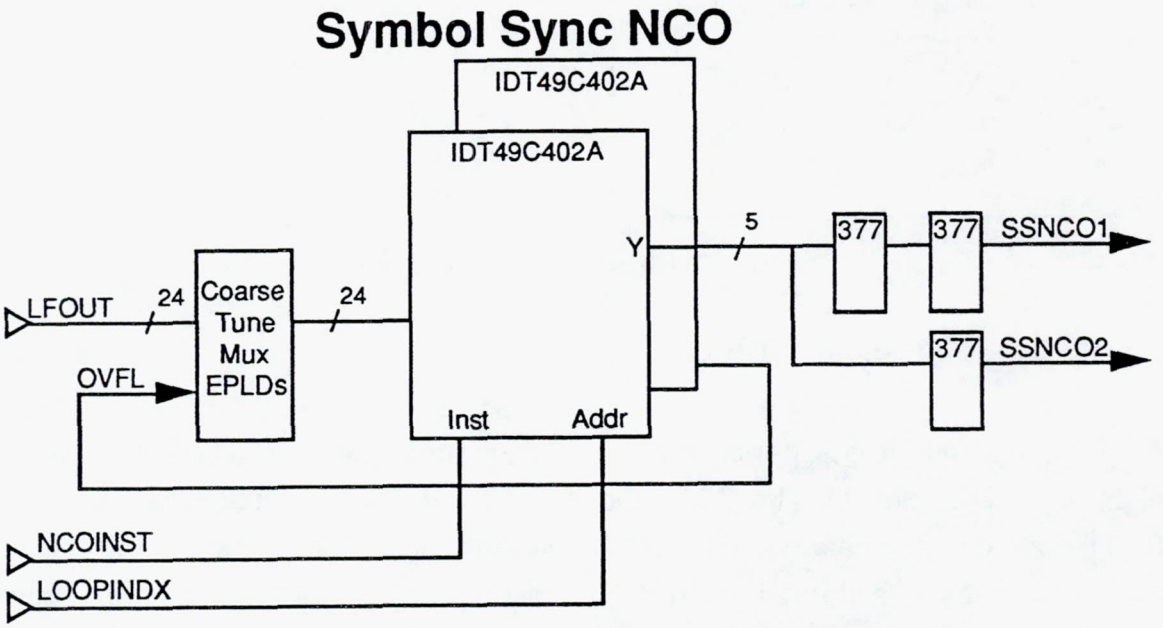


Figure 5.3.9-1

The conditional processing is performed by modifying the instruction word sent to the NCO. This modified instruction word is also sent to the carrier tracking NCO since it has to produce the same number of NCO results. It is through the NCO overflow status that the desired sample rate is achieved. Processing requires two register locations for each channels NCO and all accumulations are 24 bits wide.

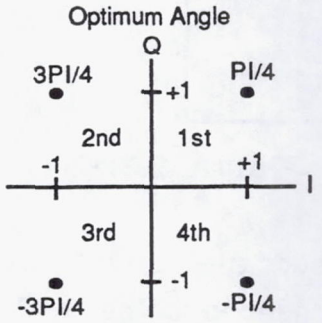
5.3.10 Carrier Phase Error

Carrier phase error is estimated by using the current midpoint samples, from both I and Q, as a 10-bit address to an 8 bit phase error lookup table (EPROM). Q is used as the

least significant address bits and I is used as the most significant. The lookup table is calculated as follows:

Phase Error = ArcTan[Q/I] - AngleOptimum[I,Q]

where AngleOptimum[I,Q] = [PI/4] : First Quadrant
[3PI/4] : Second Quadrant
[-3PI/4] : Third Quadrant
[- PI/4] : Fourth Quadrant



The result of this lookup is placed in the least significant 8 bits and sign extended to 24 bits for input to the loop filter.

5.3.11 Carrier Tracking Loop Filter

The carrier tracking loop filter operations are exactly the same as the symbol sync loop filter as is the hardware block. All dynamic control signal are shared by both loop filters. All K's are switch selectable to allow the use of different loop bandwidths.

5.3.12 Carrier Tracking NCO

The carrier tracking NCO (shown in Figure 5.3.12-1) operations are exactly the same as the symbol sync loop filter, except that when the re-sample ratio is added to the shifted loop filter result in the symbol sync NCO, the carrier tracking NCO adds zero. This enables the control signals of both NCOs to be as identical as possible.

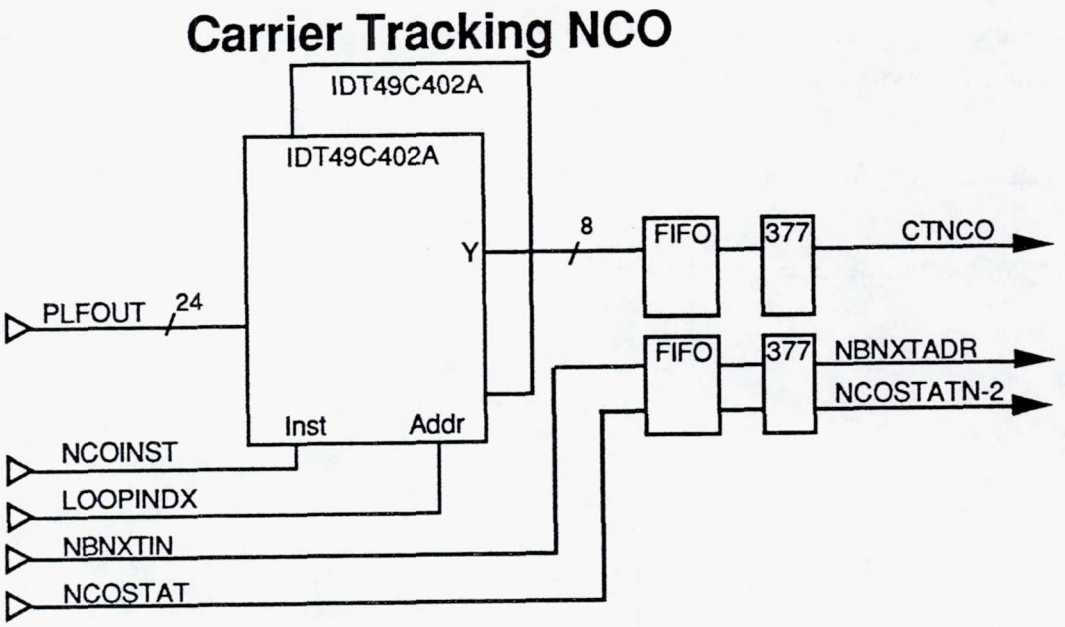


Figure 5.3.12-1

Since the symbol sync NCO results are needed for the Resampling Filters, and the carrier tracking NCO results are needed for the derotate, there exists a time disparity between when the data is available from the carrier tracking NCO and when that data is needed. This delay is one symbol epoch. To induce the necessary delay in the carrier tracking NCO results, a FIFO is used to provide the buffering. So whereas the symbol sync NCO results are output directly to the re-sample filter block, the carrier tracking NCO results are stored in FIFO and read one symbol epoch later to compensate for the pipeline delays in going through the resampling filters to the derotator. As mentioned previously, the symbol sync NCO status and de-stagger buffer next write address are also stored in this FIFO to allow proper synchronization.

(NB) rate will be output. These two signals (DATA and CLOCK) are shared by all channels as their respective data bit and clock strobe, with that data being sent out when the proper channel index is accessed. This is illustrated in Figure 5.3.13-1.

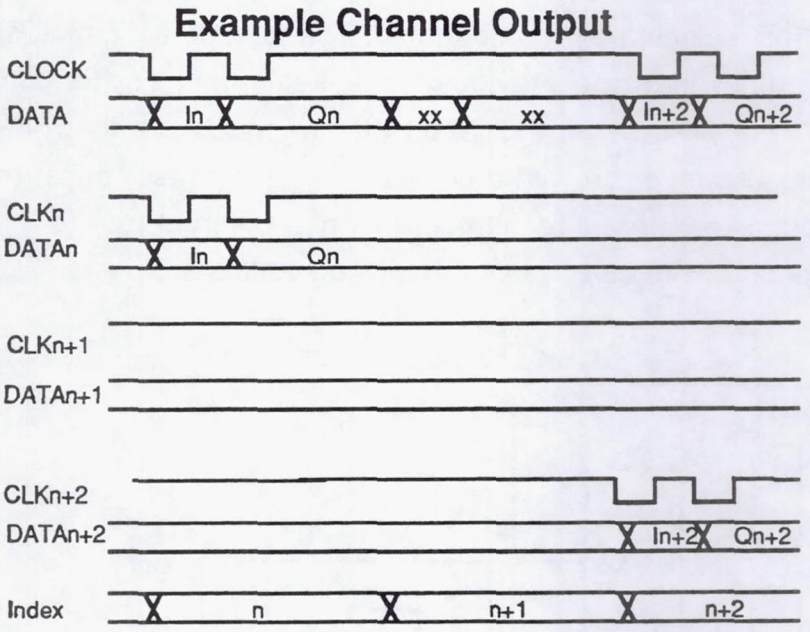


Figure 5.3.13-1

The selection of the channel under test will be determined by the controller. It is this channel that will be sent to the BER test set. The other channels (if in NB mode) will be available for observation.

5.3.14 Lock Detect

Lock detect circuitry, shown in Figure 5.3.15-1, exists to monitor the loop filter outputs of both the symbol sync and carrier tracking loops. Lock detect is performed only on the channel under test selected by the controller. The lock detect circuit subtracts the current loop filter output from the previous loop filter output and is compared to a known threshold. This will give an indication of how much the loop filter output is changing. This is necessary since with a constant rate (or phase) offset the loop filter will on average produce a different result than that of a different rate (or phase) offset, therefore the difference has to be observed to give an estimate of lock.

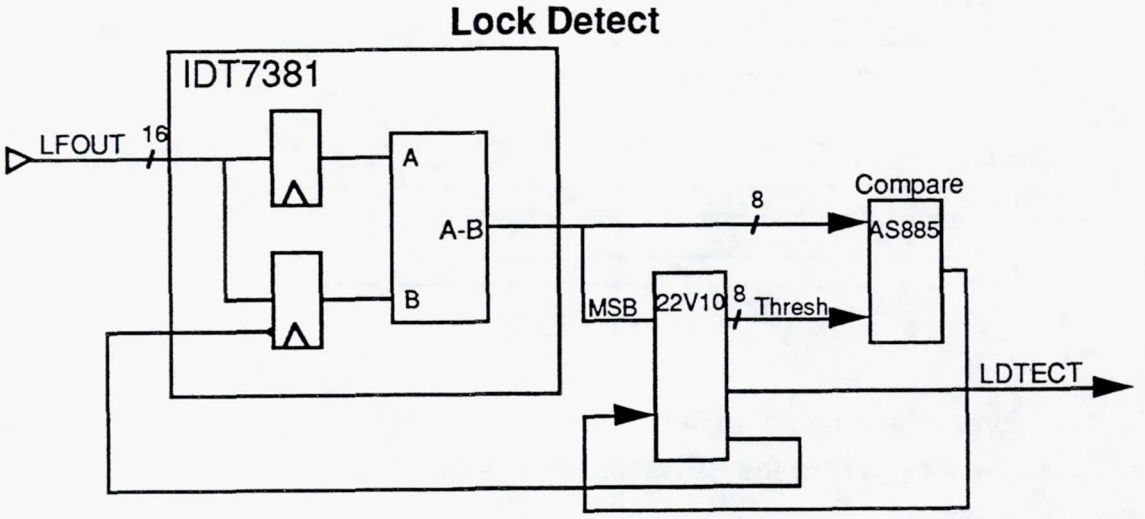


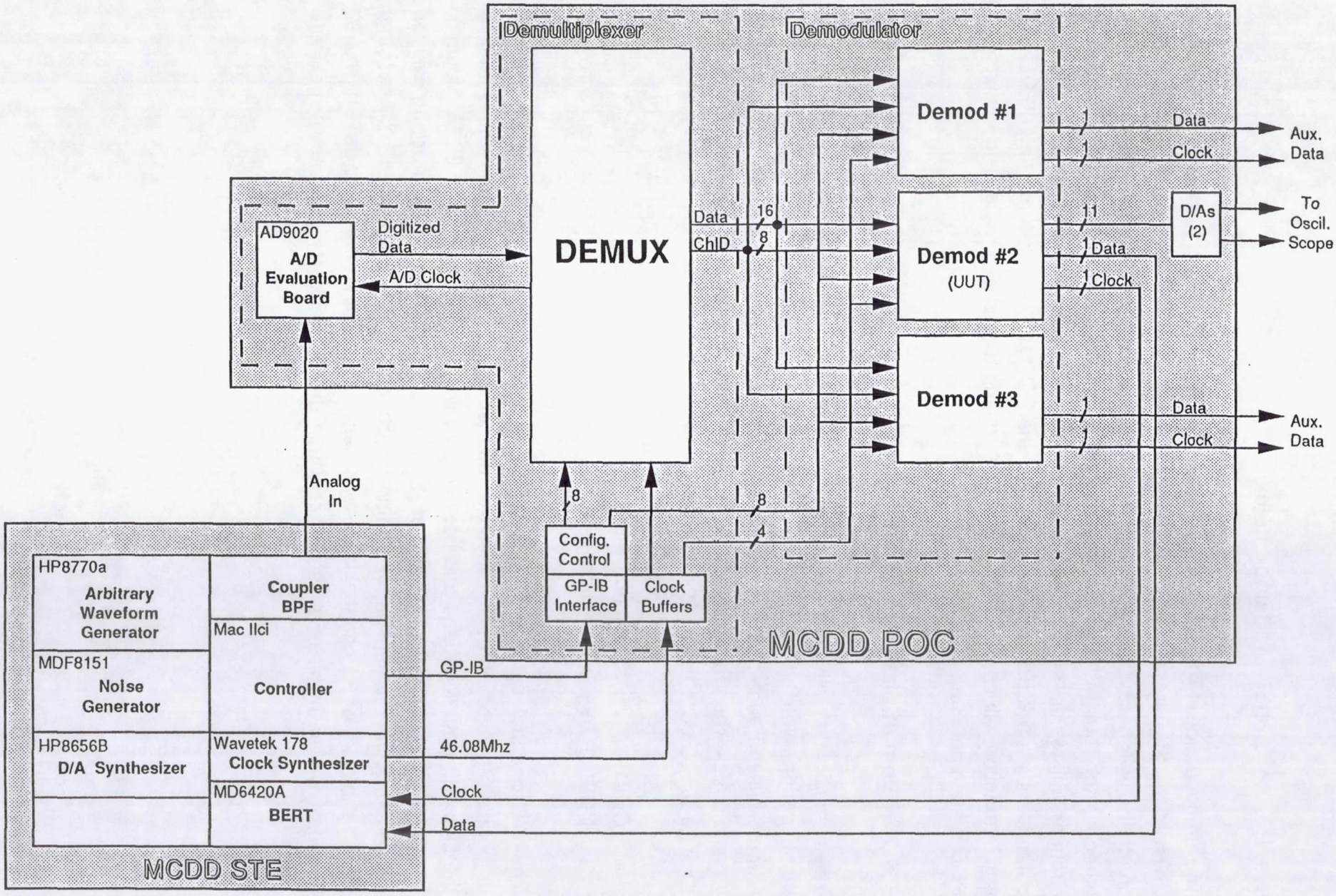
Figure 5.3.15-1

5.4 Critical Design Parameters

By far the most critical design parameter is the number of resampling filter taps. This is the driving factor in determining the system clock rates. Another factor is the word lengths specified by system engineering.

5.5 Critical Interfaces

There are three interfaces for the MCDD POC demodulator (shown in Figure 5.5-1), they are outlined below.



MCDD POC Interface Diagram

Figure 5.5.1

5.5.1 Controller to Demodulator

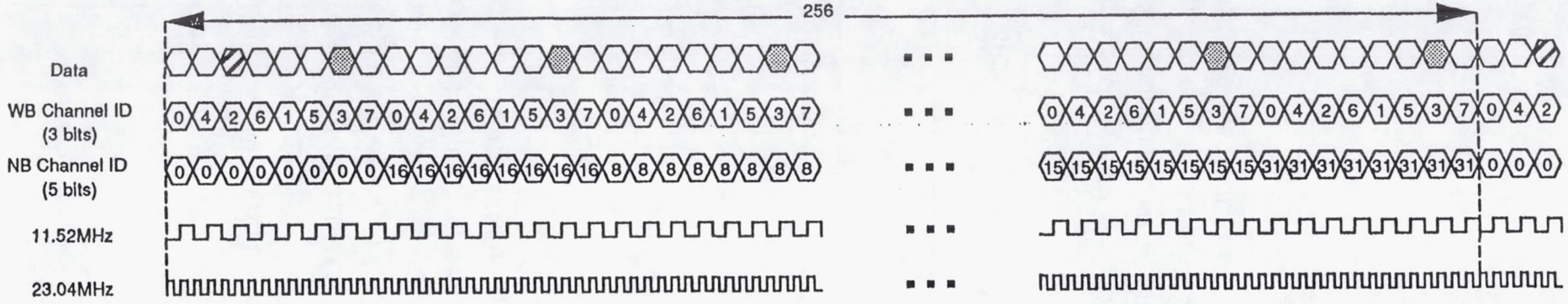
The demodulator is expecting 1 bit for NB/WB mode selection, and 5 bits to select which of the 32 narrowband channels is to be output to the STE. In wideband mode channel 0 will always be selected. The controller will not interface directly to the demodulator, but will communicate through the demultiplexer, for the IEEE-488 circuitry will reside at the demultiplexer. The controller will change POC system parameters via a IEEE-488 bus, on which the POC will be a listener only. IEEE-488 bus interaction will consist of the controller writing to a status register to change the POC system parameters.

5.5.2 Demultiplexer to Demodulator

The demultiplexer will send 16 bits of data (8 I and 8 Q) along with a 8-bit channel identification word, that will be common to all demodulator inputs. It is the responsibility of each of the demodulators to decode the channel ID word and write in its data points when they are active on the time-division-multiplexed bus. The channel ID word will be decoded as follows:

CHID<4..0> = NB channel index;
CHID<7..5> = WB channel index;

The WB channel index will be used as a board select, with each of the three demodulators selecting their respective channels data. Data output from the Demux to the Demod, both wideband and narrowband, will be valid for one 11.52 Mhz period, but have an average data rate of 1.44 MSPS. Effective data ordering will be consecutive time samples for wideband channels. For narrowband processing, adjacent blocks of 32 channels will represent consecutive time samples, but the 32 channels will be in bit reversed order within these blocks. This is shown in Figure 5.5-2.



EXAMPLE

WB Channel 3

WB Channel 2, NB Channel 0

DEMUX - DEMOD INTERFACE DESCRIPTION

Eight WB channels are output, time multiplexed over a single bus. The WB channel output order is bit reverse.

If NB channelized, the consecutive samples of a WB channel become a time multiplexed stream of thirtytwo NB channels. Within the WB channel, the NB channel order is bit reverse.

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MCDD Demod RDE

Date

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Date

MCDD POC DEMUX-DEMOD INTERFACE

5.5.3 Demodulator to STE

Output to the STE will be two TTL level signals:

1) Demodulated Data
2) Data Clock

Data transitions will be centered about the rising edge of the data clock to ensure setup and hold requirements of the STE (Bit-Error-Rate Test Set). The data clock will be 2.048 Mhz for the wideband channel data, and 64 Khz for the narrowband channel data in the absence of symbol rate error. The clock signal will not have a 50% duty cycle. This timing relationship is shown in Figure 5.5.3-1.

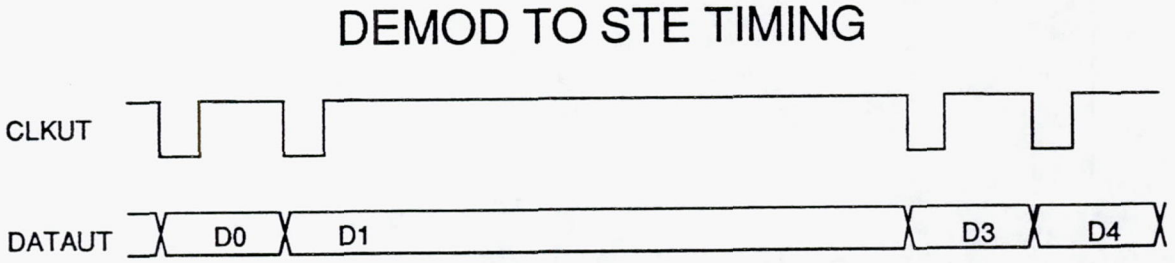


Figure 5.5.3-1

5.6 Design Trade-offs Summary and Conclusions

5.6.1 Derotate

It was first proposed to use a Plessy complex multiplier for the derotate function. Upon investigation, an 8 Bit Multiplier/Accumulator (MAC) was found and used instead. The Plessy chip had a max clock rate of 20 Mhz, which required the registering of data input to the chip to slow down the data rate. The plessy chip also has a pipeline delay of 9 clock cycles. This pipeline delay would have made the indexing more complicated. The MAC approach allows the data to be output from the VFIR directly, with the complex multiply function being performed in two cycles at the 23.04 Mhz rate.

5.7 Parts and Power Summary

5.7.1 Parts Summary

A parts summary compiled by functional hardware blocks is shown in Table 5.7.1. The estimated number of parts is 143 for a single demodulator, 15 of the these are PGAs with 68 pins or more. At the time of the PDR it was estimated that the part count would be approximately 65. The significant increase in parts is attributed to the following factors:

a) Addition of switches to control loop coefficients resulted in the addition of 13 components.

b) Addition of lock detect circuitry resulted in addition of 6 components.

c) Indexing circuitry not accounted for (14 components).

d) Barrel shifter output of 16 bits/cycle (when 24 is required) resulted in the addition of barrel shifter in both loops, and 3 registers after every barrel shifter to hold data. Also propagational timing restrictions required the addition of 244 buffers instead of using the component output enables for one of the shifts performed (total of 26 components).

The main contribution of parts increase came from the addition of registers (from 8 registers at PDR to 44 registers). The majority of the parts added will not be necessary in an ASIC implementation, for many were necessary to accommodate the 24 bit data path being comprised of two 16 bit data paths. It should be noted that the number major demodulator building blocks (Bit-Slice, Dual-Port RAM, & VFIR) did not increase.

5.7.2 Power Summary

A power summary is shown in Table 5.7.2. The total estimated power for one demodulator is 31.13 watts, and 93.39 watts for the three demodulators contained in the POC. The increase in power from 19.39 watts to 31.13 watts is a direct consequence of the increased parts count.

Demod Parts Summary 5/23/91

	Part #:	163a	22v10	7C245	F157	7032	377a	L64261	2208	49C402	F382	LSH32	244a	FCT825	EP910	L381	8bit cmpr	240	Dip Swtch	191	F00	Pullup	7201
Module Name:																							
Control Logic		4	1	11	1		10						2	1									
Resampling Filters				2		2		1											1		1		
Derotate				2					2														
Destagger Buffer		3	2		1	2	4														1		
Symbol Sync LF			1				7			2	4	2	6	3					3			1	
Symbol Sync NCO			3				3			2													
CT LF				1			6			2		2	6	3					3			1	
CTNCO							2			2				2							1		1
Symbol Decision			1				3								3		1						
Lock Detect			2													2	2						
Clock Logic													4					1		1			
Parts Totals:		7	10	16	2	4	35	1	2	8	4	4	18	9	3	2	3	1	7	1	3	2	1
Total Parts =	143																						

Table 5.7.1

Demodulator Parts/Power 5/23/91

PART #	DESCRIPTION		QTY	POWER/PART	POWER/TYPE
FCT163A	4 BIT COUNTER		7	0.025	0.175
22V10B	PRGRAMMABLE LOGIC DEVICE		10	0.45	4.5
CY7C245A	2K x 8 EEPROM		16	0.6	9.6
F157	4 BIT MUX		2	0.075	0.15
IDT7032-25	1K x 8 DUAL PORT RAM		4	0.4	1.6
FCT377A	OCTAL REGISTER		35	0.03	1.05
TMC2208	8 x 8 MAC		2	0.175	0.35
IDT7381-40	16 BIT ALU		2	0.225	0.45
FCT825A	8 BIT REGISTER		9	0.03	0.27
IDT49C402B	16-BIT SLICE		8	0.675	5.4
F382	4 BIT ALU		4	0.27	1.08
LSH32	32 BIT BARREL SHIFTER		4	0.05	0.2
FCT244a	CLOCK BUFFER		18	0.075	1.35
L64261-40	VFIR		1	1.55	1.55
EP910-35	Big EPLD		3	0.5	1.5
FCT240a	Inverting Buffer		1	0.075	0.075
FCT191	Up/Down Counter		1	0.025	0.025
F00	Nand Gate		3	0.075	0.225
BD05	5 pos. Dip Switch		7	0	0
IDT7201	512x9 FIFO		1	0.25	0.25
Pullup Pack	1k Pullup Network		2	0	0
FCT521	8 Bit Compare		1	0.03	0.03
AS885	8 Bit Compare		2	0.65	1.3
		TOTAL QTY	143	TOTAL POWER	31.13

Table 5.7.2

5.8 TEST APPROACH

5.8.1 Demodulator Test Approach

Check-out will focus initially on basic functionality of the demodulator components. At this time proper timing relationships, control signals, and arithmetic functions will be verified. When this functional test is completed, test vectors obtained from BOSS simulation will be injected into the demodulator, via a pattern generator to check loop dynamics and proper demodulator operation. BOSS models have the same exact word widths as the hardware implementation. The BOSS simulation will be modified to induce the same processing delays from input all the way thru the loops and back to alter the incoming data, that exist in the hardware. Obtained from the modified simulation will be an input vector set, along with various probe sets that will be placed at significant locations in the demodulator processing path. Injecting the BOSS demodulator vectors into the demod will allow a bit by bit comparison of the simulation results and hardware output. Granted the number of unique vectors compared is limited (around 200), but this will verify that the hardware is implementing the correct algorithm.

Vectors will be downloaded via the MacIIci controller to a HP16500 Logic Analysis System. The HP16500 has a 4096 deep, 60 bit wide pattern generator. Data will be collected by the HP16500's Logic Analyzer, and uploaded to the MacIIci controller for comparison to the simulation results. Zero's will be input to the demod prior to the BOSS vectors input to clear all loop filters, buffers, and data registers. The only non-zero value, and hence unknown will be the symbol sync NCO.

Synchronization is necessary due to the fact that the symbol sync NCO will be running with the resampling ratio (zero out of the loop filter) being input to the NCO. This will result in the NCO being in an unknown state, which in turn will alter all values output from the resampling filters. If the input vectors from the BOSS simulation are input to the demodulator with the NCO in an unknown state, then the demod results and simulation results will not match. This problem can be alleviated by triggering the pattern generator to input the BOSS vectors when the demod's NCO is in the state that matches the simulation.

5.8.2 Test Equipment

The following test equipment will be obtained from EMC for testing:

1. Logic Analysis System HP16500
2. Power Supplies (+5V,40A)
3. Oscilloscope (TEK 2445B)
4. DVM

The following items will be obtained for the STE, and will be used for checkout of demodulator hardware:

1. Mac IIci, with GP-IB interface card. (STE controller)
2. One Wavetek 178 Clock Synthesizer
3. Anritsu MD6420 BERT

5.8.3 Test Points

The following test points will be available:

1. Soft Decision Data (I and Q)
2. Micro-code program address
3. Miscellaneous control signals and syncs

Two D/A converters will be included in the POC to observe the I and Q soft decision data samples. This will enable the observation of both the signal constellation and eye diagram (of either I or Q).

5.9 ANALYSIS

5.9.1 Worst Case Timing

Worst case timing analysis for critical paths is given in Table 5.9.

Demodulator Worst Case Timing Paths 5/23/91

Control Counters						
~~						
cp -> tc		FCT163a		9.8		
cet -> tc		FCT163a		5.5		
cet -> tc		FCT163a		5.5		
Tsetup		FCT163a		11		
			Path =	31.8	Margin =	11.6
Re-Sample Data Read						
~~						
cp -> RSADDR		CY7C245a-15		10		
RSADDR -> RSINI/Q		IDT7032-25		25		
Tsetup		L64261-40		6		
			Path =	41	Margin =	2.4
VFIR to De-Rotate						
~~						
cp -> RSFOUT		L64261-40		18		
Tsetup		TMC2208		10		
			Path =	28	Margin =	15.4
De-Rotate to De-Stagger						
~~						
cp -> RSINI/Q		TMC2208		18		
Tsetup		IDT7032-25		12		
			Path =	30	Margin =	13.4

Table 5.9 Page 1

De-Stagger Read Address						
~~						
cp -> INFORD		22V10-20		12		
addr -> data		IDT7032-25		25		
INF0<2> -> RPE2		22V10-20		20		
Tsetup		FCT163a		4.5		
			Path =	61.5	Margin =	25.3
Output Logic Data (IS0 & QS0)						
~~						
cp -> I/Q<4..0>		FCT377a		7.2		
I/Q<4> -> IS0/QS0		22V10-20		20		
Tsetup		22V10-20		12		
			Path =	39.2	Margin =	47.6
Symbol Timing Error						
~~						
cp -> I/Q<4..0>		FCT377a		7.2		
I/Q<4> -> IS0/QS0		22V10-20		20		
IS0/QS0 -> Fout		F382		20.5		
a,b -> Cn+4		F382		9		
Cn -> Fout		F382		12		
Tsetup		FCT825a		4		
			Path =	72.7	Margin =	14.1

Table 5.9 Page 2

Ki Shift Timing (SS and CT)						
~~						
cp -> LFINST		CY7C245a-15		10		
LFINST -> ALU		49C402B		28		
ALU -> ER		FCT244a		4.3		
ER -> SHOUT		LSH32A		34		
Tsetup		FCT377a		2		
			Path =	78.3	Margin =	8.5
Kt Shift Timing (SS and CT)						
~~						
cp -> LFINST		CY7C245a-15		10		
LFINST -> ALU		49C402B		28		
ALU -> T0_PLF...		LSH32A		34		
Tsetup		FCT377a		2		
			Path =	74	Margin =	12.8
Loop Filter to SSNCO						
~~						
cp -> LFOUT		FCT377a		7.2		
LFOUT -> NCOIN		22V10-20		20		
Tsetup		49C402B		20		
			Path =	47.2	Margin =	39.6
NCO 24 bit Add						
~~						
cp -> NCOINST		CY7C245a-15		10		
NCOINST -> I2		22V10-20		20		
a,b -> Cn+16		49C402B		26		
Tsetup		49C402B		14		
			Path =	70	Margin =	16.8

Overflow Setup						
~~						
cp -> NCOINST		CY7C245a-15		10		
NCOINST -> I2		22V10-20		20		
a,b -> Cn+16		49C402B		26		
Cn -> OVFL		49C402B		17		
Tsetup		22V10-20		12		
			Path =	85	Margin =	1.8
CT NCO and NCOSTAT to FIFO						
~~						
cp -> NCOINST		CY7C245a-15		10		
NCOINST -> I2		22V10-20		20		
a,b -> y		49C402B		28		
Tsetup		IDT7201-25		15		
			Path =	73	Margin =	13.8
Note: Names in all capital letters denote actual signal names (ie. NCOINST),						
whereas names in lower case letters (ie. a,b, and Cn) denote device pins.						

5.10 MECHANICAL

5.10.1 Board Type/Size

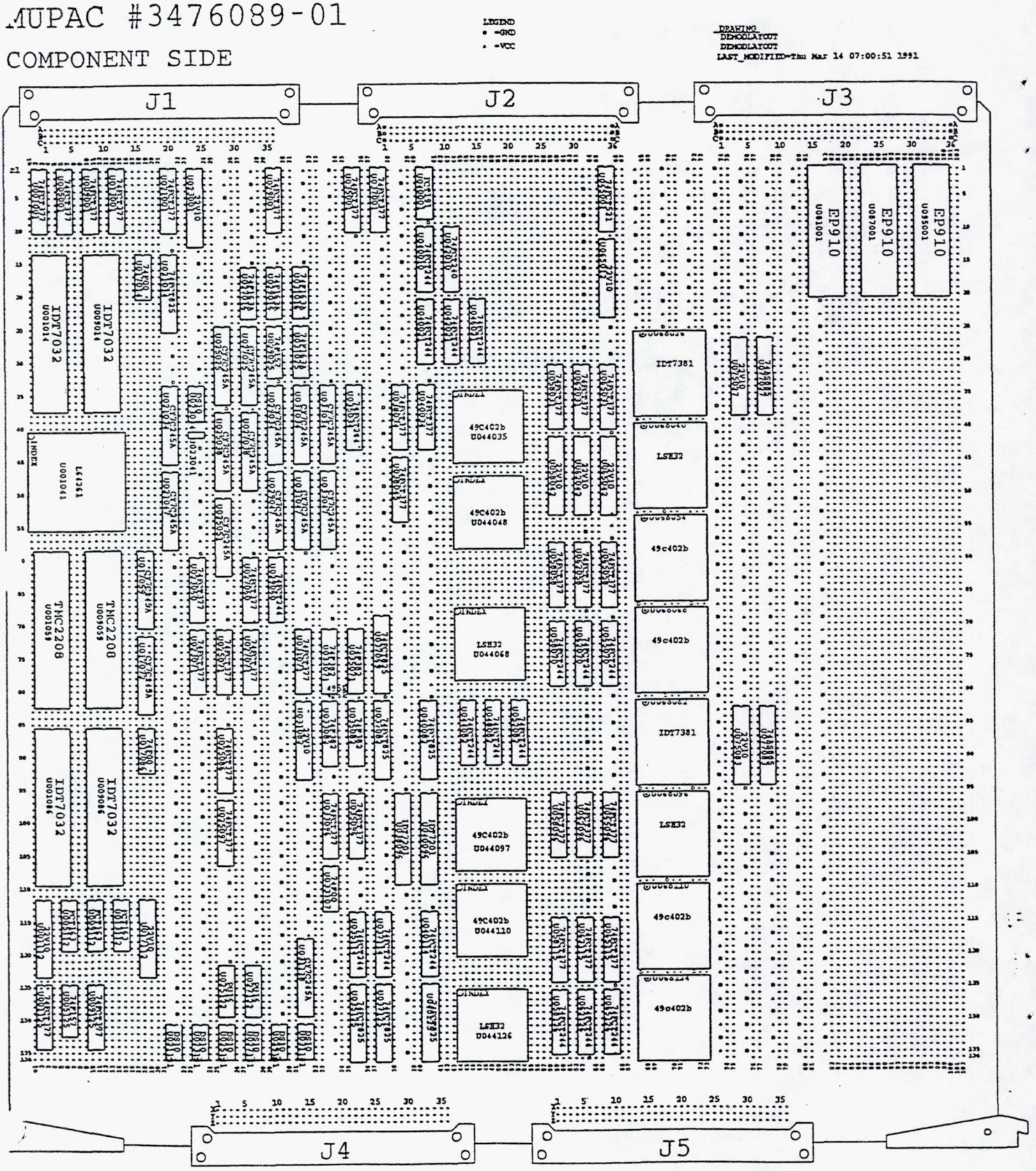
Board type for the Demodulator is a Mupac 3476089. Dimensions are as follows: Length = 16.90 inches, Width = 14.90 inches. A layout for the MCDD demodulator with IC's placed is shown in Figure 5.10.1-1

5.10.2 Inter-Connect

An overall signal interface is shown in Figure 5.11-1 with backplane interconnections are as shown in Table 5.11-2

MUPAC #3476089-01

COMPONENT SIDE



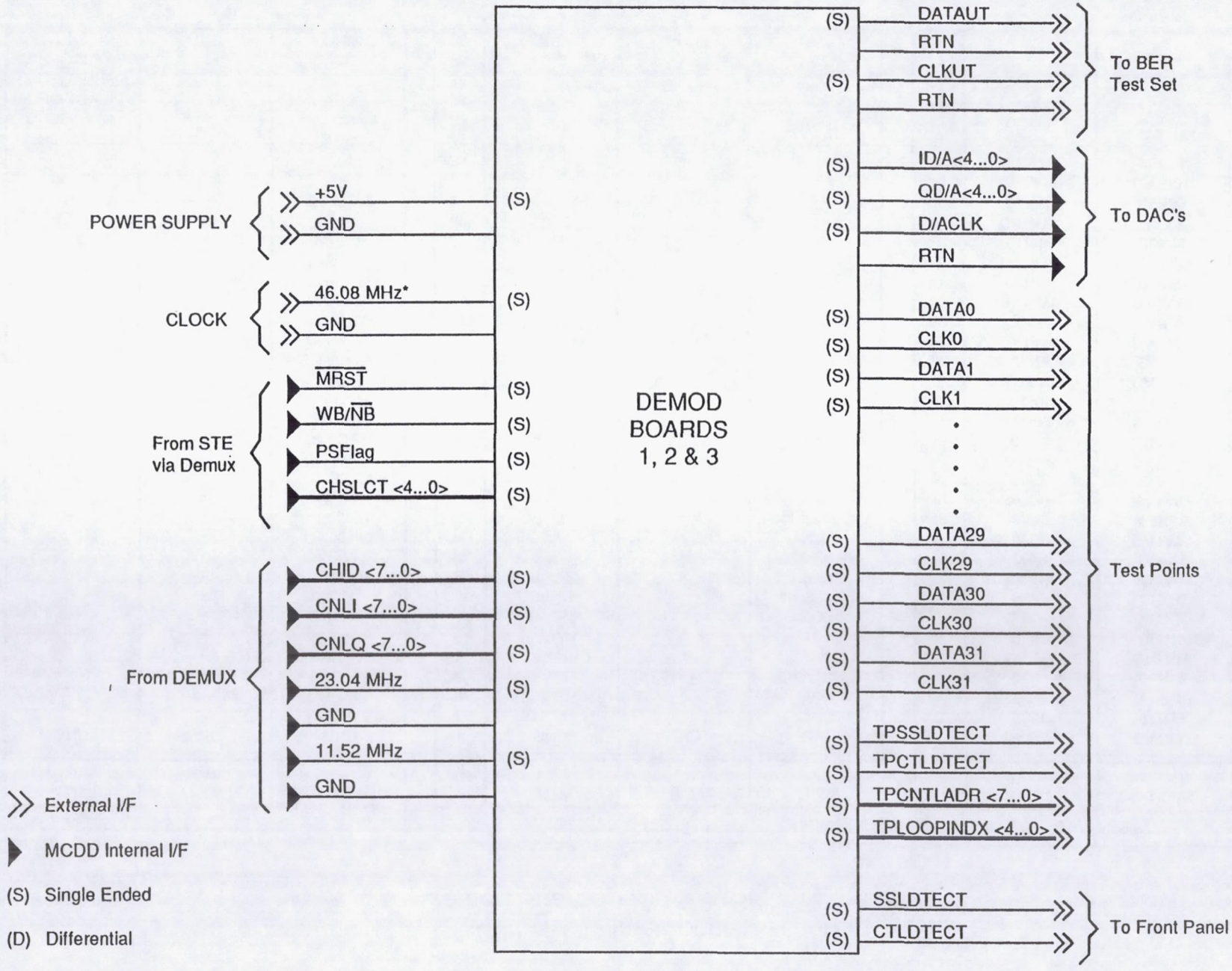


Figure 5.11-1 DEMOD I/F DIAGRAM

MCDD POC Interconnect Diagram
Demod Boards 1, 2, & 3 (Slots 7, 8 & 9)

P1			
	ROW A	ROW B	ROW C
1	GND	GND	GND
2	-	-	CNLI<7>
3	-	-	CNLI<6>
4	-	-	CNLI<5>
5	-	-	CNLI<4>
6	-	-	CNLI<3>
7	-	-	CNLI<2>
8	-	-	CNLI<1>
9	-	-	CNLI<0>
10	-	-	CNLQ<7>
11	-	-	CNLQ<6>
12	-	-	CNLQ<5>
13	-	-	CNLQ<4>
14	-	-	CNLQ<3>
15	-	-	CNLQ<2>
16	-	-	CNLQ<1>
17	-	-	CNLQ<0>
18	-	-	CHID<7>
19	-	-	CHID<6>
20	-	-	CHID<5>
21	-	-	CHID<4>
22	-	-	CHID<3>
23	-	-	CHID<2>
24	-	-	CHID<1>
25	-	-	CHID<0>
26	-	-	WB/NB
27	-	-	MRST
28	-	-	PS FLAG
29	-	-	-
30	-	-	-
31	CHSLCT<4>	-	VCC
32	CHSLCT<3>	-	VCC
33	CHSLCT<2>	-	VCC
34	CHSLCT<1>	-	VCC
35	CHSLCT<0>	-	VCC
36	GND	GND	GND

P2			
	ROW A	ROW B	ROW C
1	GND	GND	GND
2	ID/A<4>	-	VCC
3	ID/A<3>	-	VCC
4	ID/A<2>	-	VCC
5	ID/A<1>	-	VCC
6	ID/A<0>	-	VCC
7	QD/A<4>	-	VCC
8	QD/A<3>	-	46.08MHz*
9	QD/A<2>	-	RTN
10	QD/A<1>	-	23.04 MHz
11	QD/A<0>	-	RTN
12	D/ACLK	-	11.52 MHZ
13	-	-	RTN
14	-	-	-
15	-	-	-
16	-	-	-
17	-	-	-
18	-	-	-
19	-	-	-
20	-	-	-
21	-	-	-
22	-	-	-
23	-	-	-
24	-	-	-
25	-	-	-
26	-	-	-
27	-	-	-
28	-	-	-
29	-	-	-
30	-	-	-
31	-	-	VCC
32	-	-	VCC
33	-	-	VCC
34	-	-	VCC
35	-	-	VCC
36	GND	GND	GND

P3			
	ROW A	ROW B	ROW C
1	DATAO	DATA17	DATAUT
2	CLK0	CLK17	RTN
3	DATA1	DATA18	CLKUT
4	CLK1	CLK18	RTN
5	DATA2	DATA19	SSLDTECT
6	CLK2	CLK19	CTLDTECT
7	DATA2	DATA20	-
8	CLK3	CLK20	-
9	DATA4	DATA21	-
10	CLK4	CLK21	-
11	DATA5	DATA22	-
12	CLK5	CLK22	-
13	DATA6	DATA23	-
14	CLK6	CLK23	-
15	DATA7	DATA24	-
16	CLK7	CLK24	-
17	DATA8	DATA25	-
18	CLK8	CLK25	-
19	DATA9	DATA26	-
20	CLK9	CLK26	-
21	DATA10	DATA27	-
22	CLK10	CLK27	-
23	DATA11	DATA28	-
24	CLK11	CLK28	-
25	DATA12	DATA29	-
26	CLK12	CLK29	-
27	DATA13	DATA30	-
28	CLK13	CLK30	-
29	DATA14	DATA31	-
30	CLK14	CLK31	-
31	DATA15	-	-
32	CLK15	-	-
33	DATA16	-	-
34	CLK16	-	-
35	-	-	-
36	-	-	-

* For stand-alone only

Table 5.11-2

MCDD POC Interconnect Diagram
Demod Boards 1, 2, & 3 (Slots 7, 8 & 9)

P4			
	ROW X	ROW Y	ROW Z
1	TPCNTLADR<7>	-	-
2	TPCNTLADR<6>	-	-
3	TPCNTLADR<5>	-	-
4	TPCNTLADR<4>	-	-
5	TPCNTLADR<3>	-	-
6	TPCNTLADR<2>	-	-
7	TPCNTLADR<1>	-	-
8	TPCNTLADR<0>	-	-
9	TPLOOPINDX<4>	-	-
10	TPLOOPINDX<3>	-	-
11	TPLOOPINDX<2>	-	-
12	TPLOOPINDX<1>	-	-
13	TPLOOPINDX<0>	-	-
14	-	-	-
15	-	-	-
16	-	-	-
17	-	-	-
18	-	-	-
19	-	-	-
20	-	-	-
21	-	-	-
22	-	-	-
23	-	-	-
24	-	-	-
25	-	-	-
26	-	-	-
27	-	-	-
28	-	-	-
29	-	-	-
30	-	-	-
31	-	-	-
32	-	-	-
33	-	-	-
34	-	-	-
35	-	-	-
36	-	-	-

P5			
	ROW X	ROW Y	ROW Z
1	TPSSLDTECT	-	-
2	TPCTLDTECT	-	-
3	-	-	-
4	-	-	-
5	-	-	-
6	-	-	-
7	-	-	-
8	-	-	-
9	-	-	-
10	-	-	-
11	-	-	-
12	-	-	-
13	-	-	-
14	-	-	-
15	-	-	-
16	-	-	-
17	-	-	-
18	-	-	-
19	-	-	-
20	-	-	-
21	-	-	-
22	-	-	-
23	-	-	-
24	-	-	-
25	-	-	-
26	-	-	-
27	-	-	-
28	-	-	-
29	-	-	-
30	-	-	-
31	-	-	-
32	-	-	-
33	-	-	-
34	-	-	-
35	-	-	-
36	-	-	-

Table 5.11-2 (Cont'd)

6.0 MCDD STE

6.1 Functional Overview

The STE is shown in Figure 6.1-1 in its relative position in the MCDD POC. The STE will be comprised entirely of off-the-shelf commercial test equipment. The STE is responsible for performance testing of the MCDD POC under various operating conditions. The POC drawer will be mounted in the STE rack along with the other commercial test equipment. The primary component for signal generation is the Hewlett Packard 8770 Arbitrary Waveform Generator (AWG). The AWG can fully load the input and generate data patterns with rate and timing offsets, multiple IF frequencies with offsets and interference. The STE has the flexibility to generate analog signals that can closely simulate the entire communication channel. The STE will be able to simulate a fully loaded MCDD POC spectrum with at least 256 individual narrowband channels (8 wideband channels). All signal parameters will be varied in software before up-loading to the AWG. Also, changes to the modulation format can be accommodated without modification to the STE hardware. A commercial software package will be used to interface with the test equipment and to provide a user friendly interface for operation.

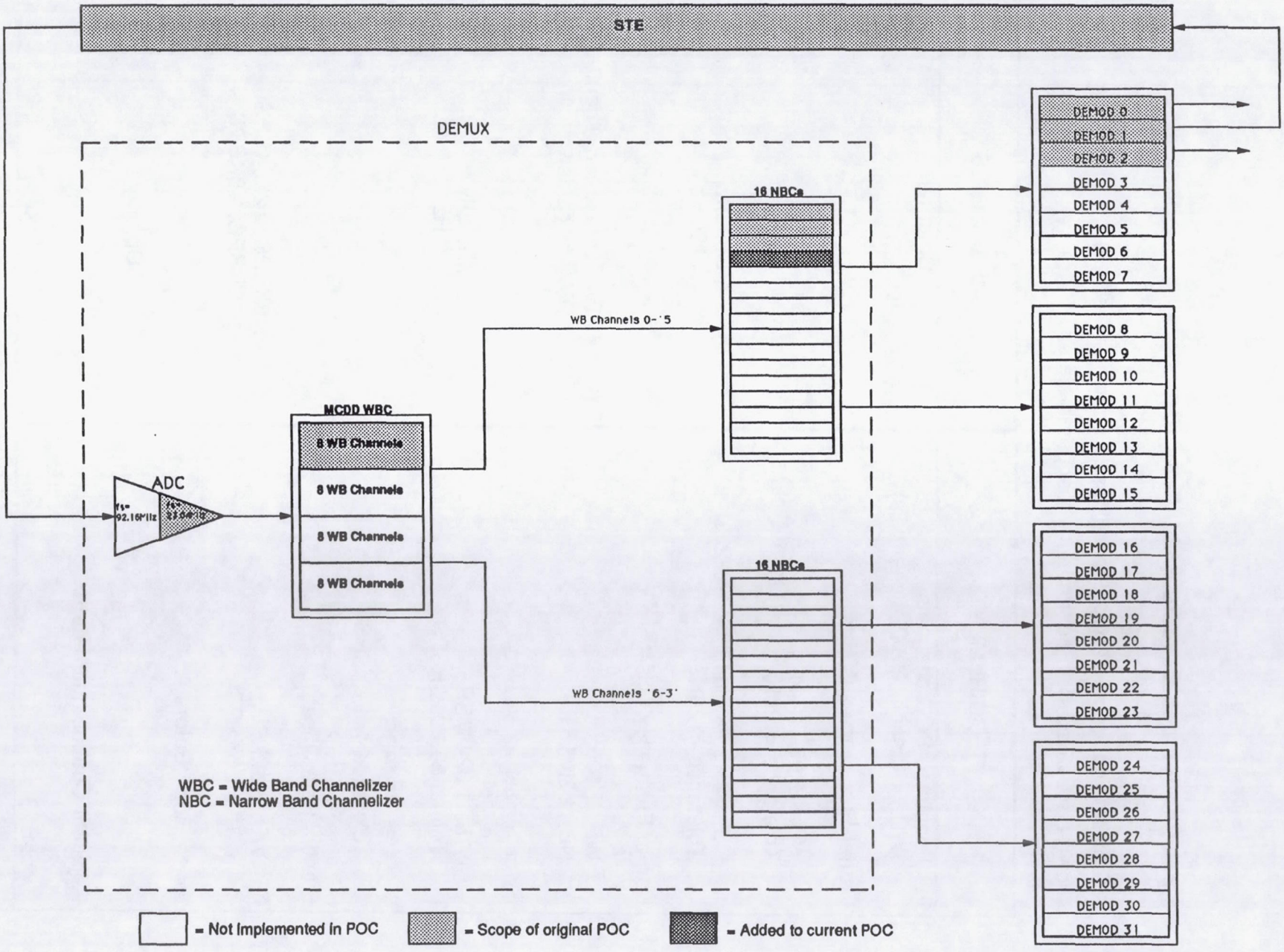


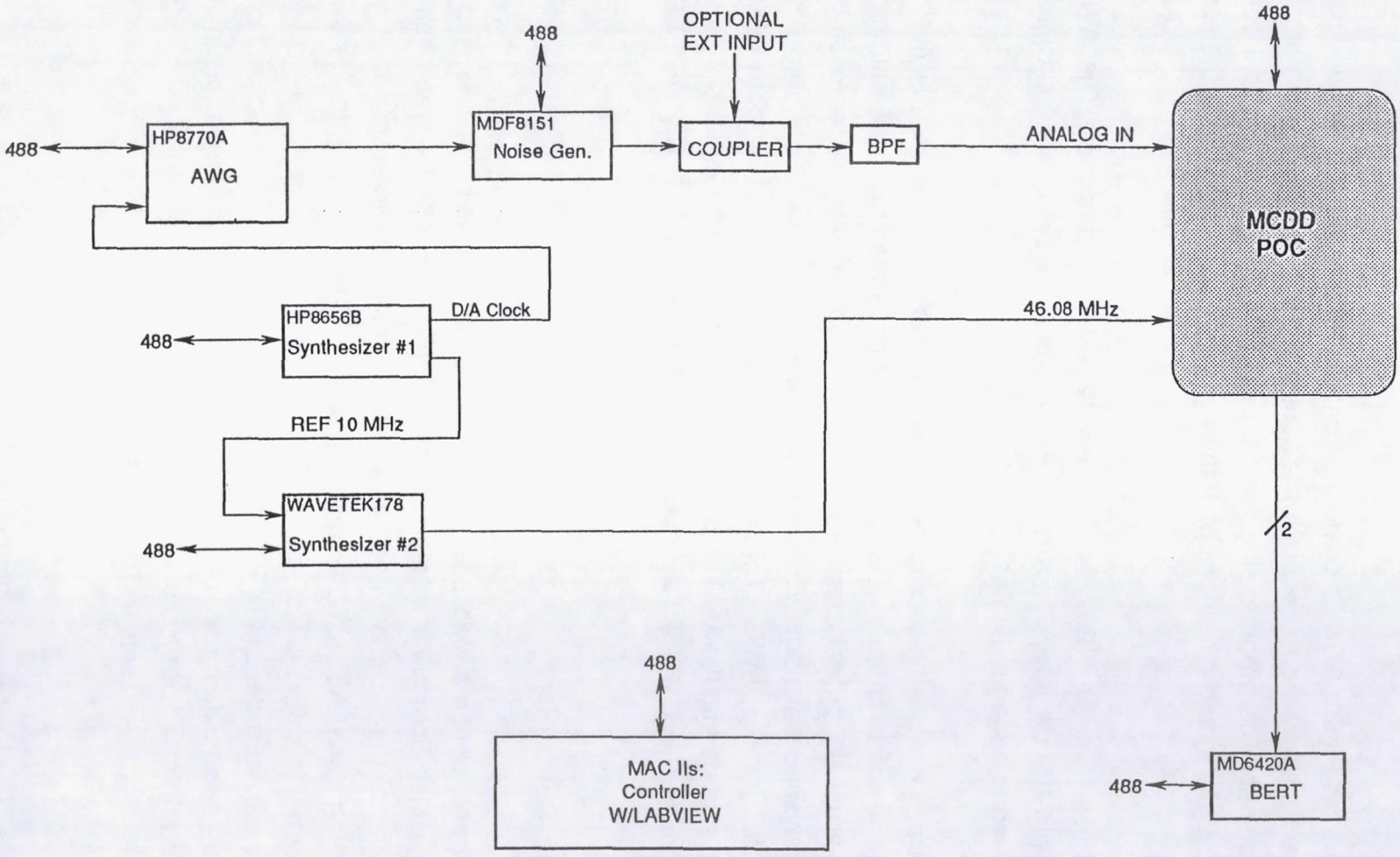
FIGURE 6.1-1: POC SUBSET OF MCDD

6.2 Requirements vs. Capabilities

A table of requirements vs. capabilities is shown in Table 6.2-1. The requirements shown are derived from performance test parameters.

REQUIREMENTS	CAPABILITIES
Fully populate POC channels (WB 7 channels, NB 224 channels)	Comply
Carrier Frequencies (MHz)	
WB: 12.96 + 1.44i ($0 \leq i \leq 6$) Tolerance <120Hz	Comply 0 Hz
NB: 12.285 + 0.045i ($0 \leq i \leq 223$) Tolerance <120Hz	Comply <120Hz
Carrier Frequency Offset	
WB: ± 100KHz NB: ± 3KHz	WB: + $F_{D/A}/2$ - $F_{carrier}$, -$F_{carrier}$ NB: + $F_{D/A}/2$ - $F_{carrier}$, -$F_{carrier}$
Symbol Rate	
WB: 1.024 MSPS Tolerance < ±20KSPS	Comply 0 Hz
NB: 32KSPS Tolerance < 1.0KSPS	Comply 0 Hz
Symbol Rate Offset	
WB: ± 50KSPS NB: ± 1.5KSPS	-533KSPS, +256KSPS -16.7KSPS, +8KSPS
Noise Floor (Before A/D)	
< - 50dB	Comply
Adjacent Channel Interference	
± 8dB	±20dB

Table 6.2-1 Requirements vs. Capabilities



STE FUNCTIONAL BLOCK DIAGRAM

Figure 6.3-1

6.3 Design Description

The STE, shown in Figure 6.3-1 is composed entirely of commercial test equipment; the development task will be to generate the necessary software and to integrate the various components. The programming required will be limited to instrument control, via IEEE-488 interface, and development of the composite FDM signals for the various tests cases.

The STE is based on the HP8770a Arbitrary Waveform Generator. The AWG is downloaded with the desired digitized waveforms, these waveforms are Digital-to-Analog converted to generate an analog signal.

The STE includes a white noise source and signal combiner (included in the noise generator) to give the necessary noise added to our generated signal. A coupler also is provided to allow an optional external input to be combined with the composite FDM signal. This combined waveform will then be low-pass filtered to eliminate any aliasing effects induced by the AWG. The signal will then be input to the POC for channelization and demodulation. The demodulated output will be input to a bit-error-rate test set for analysis. All test equipment contained in the STE will be IEEE-488 controlled.

6.3.1 STE Controller

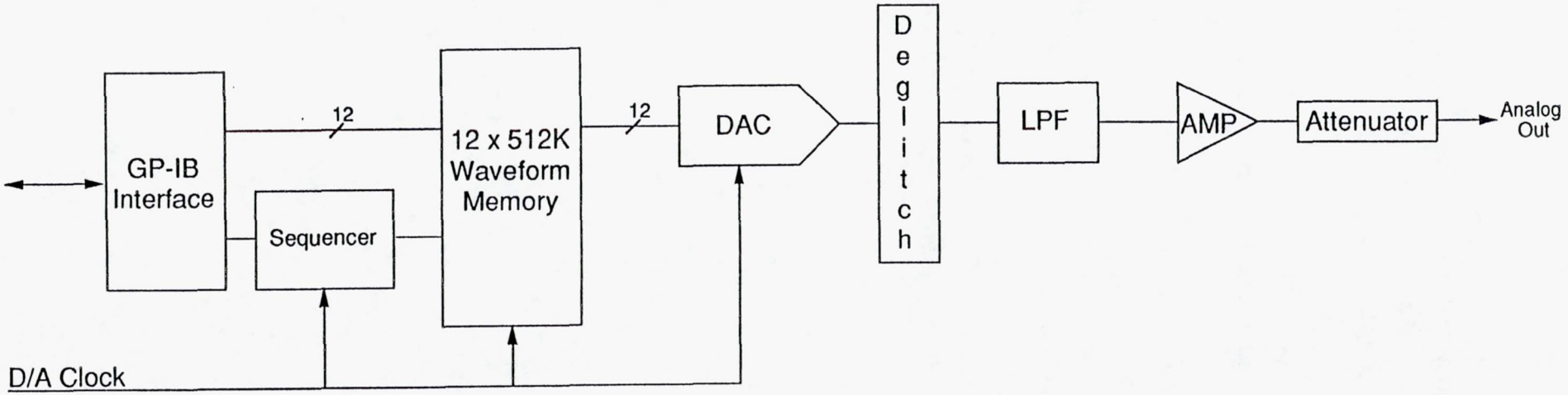
The STE controller will be a Macintosh IIci with 8 MB of RAM and a 80 MB hard disk. Installed in the Mac IIci will be a National Instruments IEEE-488 interface board, to allow controlling of the various pieces of test equipment. The user interface will be generated using the LABVIEW software package. The STE controller will be responsible for the following tasks:

1. Differentially encodes either PRN sequence, or user entered message.
2. Generates sampled composite FDM QPSK modulated sequence for uploading the AWG. Induces desired channel degradations.
3. Loads the AWG and sets up its necessary parameters.
4. Adjusts the signal power.
5. Adjusts the noise power.
6. Controls POC for desired channel configuration.

7. Controls frequency of AWG D/A clock synthesizer (HP8656B).
8. Controls frequency of 46.08Mhz clock to the POC synthesizer (Wavetek 178).
9. Monitors output of BER test set.

6.3.2 Arbitrary Waveform Generator

The HP8770a, shown in Figure 6.3-2, is the principal building block of the STE. It enables us to generate waveforms with frequency components (non-aliased) of up to 50 Mhz. The AWG has an internal attenuator which has a range of 120 dB in 10 dB steps. In addition to this, an external programmable attenuator will be provided to give the necessary precision
to obtain desired Eb/No values. The various signal parameters will be induced on the symbol waveforms, in software, then up-loaded to the AWG for output.



HP8770 Functional Block Diagram

Figure 6.3-2

6.3.3 Programmable Attenuator

To get the necessary precision in signal power output from the AWG an additional programmable attenuator is necessary. The HP programmable attenuator was eliminated by installing a signal attenuator (GPIB controlled) in the noise generator.

6.3.4 White Noise Source

The noise source is an MDF8151 (MDF Products Inc.) with a bandwidth of 40 Mhz. The noise source has a maximum output power level of +13 dBm, and a programmable attenuator of 120 dB in 1 dB steps. The signal input also has the same attenuator. Included in the noise source is a combiner, this will enable us to add noise to the signal output from the HP8770. A coupler will be added to the output of the power combiner to allow the summing of an arbitrary external input with our composite FDM signal. A power splitter at the output of the combined signal plus noise provides an analog monitoring point.

6.3.5 Frequency Synthesizers

The STE includes three frequency synthesizers controlled by the STE controller via a IEEE-488 interface. These synthesizers will be phase referenced with the HP8656B being the reference source.

- Frequency Synthesizer #1 (HP8656B) provides the D/A clock to the AWG.
- Frequency Synthesizer #2 (Wavetek 178) provides the 46.08Mhz digital clock to the POC. (will be divided down to provide 23.04 and 11.52Mhz)

6.3.6 Bit-Error-Rate Test Set

The BER test set will be an Anritsu MD6420 with a MD0620A GP-IB module. This will receive as input the demodulated data stream and corresponding data clock. The BER test set is expecting a known PRN sequence to which it will synchronize. The AWG will be loaded with this PRN sequence properly encoded and modulated. The STE will read the BER figure calculated by the MD6420 periodically, and display it to the Controller screen. Also available from the BERT will be the output data rate, (ie 64KBPS or 2.048MBPS) and ASCII characters formed from the input data stream.

6.3.7 Software

Two software packages will be used on the Mac IIci, LABVIEW and Think C. LABVIEW will control all test equipment along with providing a user interface, and Think C will be used to generate the C modules that will create digitized waveforms to be uploaded to the AWG.

LABVIEW is a software package that allows us to computer generate a functional "front panel" for the entire STE. Only pertinent parameters of the various pieces of test equipment will be available for manipulation and display. Waveform parameters will also be available in the same fashion. The user interface is a computer generated "front panel" with knobs, switches, and other easily identified control symbols that can be manipulated with the computer mouse. An example "front panel" for the HP8770 , as seen from the computer screen, is shown in Figure 6.3-3. LABVIEW enables the programmer to easily generate the necessary GP-IB (IEEE-488) commands such that they are transparent to the user. It also enables easy modification of the generated "front panel".

Think C is a C compiler, debugger, and text editor package. It is compatible with LABVIEW such that modules written in C can be easily interfaced with LABVIEW. LABVIEW will pass signal generation parameters to modules written in C. The module will create the necessary waveform files that will be passed back to LABVIEW and uploaded to the AWG. Waveforms created in the C modules will have the various signal variations (ie. carrier frequency and phase offsets), including pulse shaping.

Front Panel

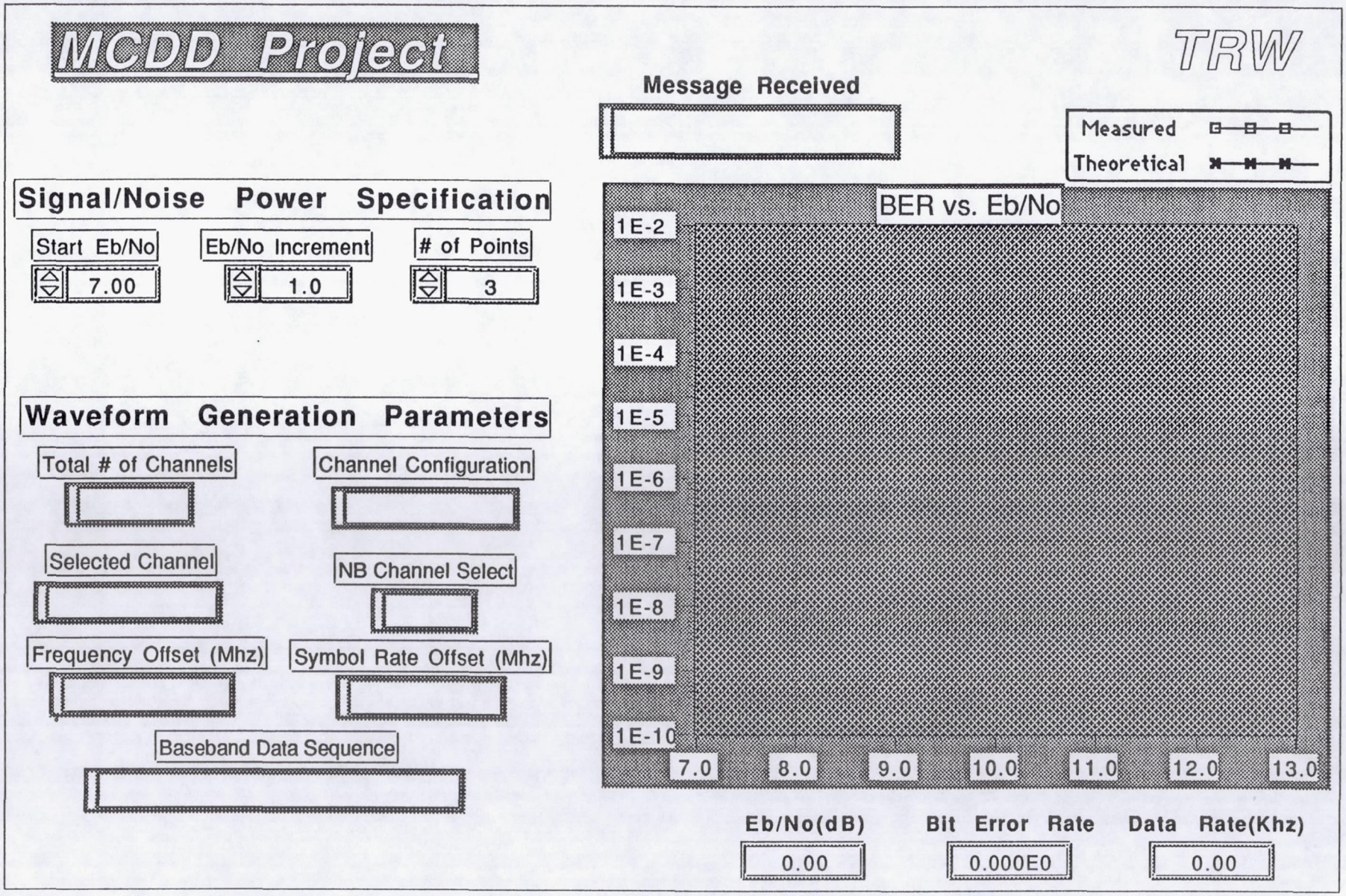


Figure 6.3-3 LABVIEW Front Panel

6.3.8 Typical BER Measurement Sequence

Given below is a typical sequence of events for a BER measurement.

1. User will select desired test, or can vary a specific signal parameter.
2. PRN sequence will be differentially encoded, and modulated onto the symbol waveforms. This is done in C modules on the Mac IIci controller.
3. The digital waveforms created are up-loaded to the AWG waveform memory.
4. The AWG 125 MSPS D/A converter creates analog signal from stored symbol waveforms. Signal is coarse attenuated in AWG.
5. Signal is fine attenuated by programmable attenuator located in the noise generator.
6. Signal is combined with appropriately attenuated noise to give desired Eb/No.
7. Signal is Band-Pass filtered and input to MCDD POC for processing.
8. Demodulated data symbols are output form MCDD POC to the BERT for BER measurement.
9. BER measurements are read by controller, via GP-IB, and displayed as a BER curve on LABVIEW "front panel" display.

6.4 Critical Design Parameters

The design parameters of the STE are a direct consequence of the tests to be performed. Since the design is mainly software driven, then as long as the individual components of the STE can vary their operating parameters over a reasonable range, there should be enough flexibility to generate all desired test conditions.

One constraint on the STE is the memory size of the HP8770. The RAM internal to the HP8770 is 512K words, therefore any signal sequence sent must be constrained to 512K samples. For the MCDD POC spectrum requirements we have the following:

$$F_{max} = 34.56 \text{ Mhz}$$

$$F_{sample} = 2\ (F_{max}) = 69.12 \text{ Mhz (Nyquist)}$$

$$F_{symbol} = 32 \text{ KSPS (minimum)}$$

$$\text{\# of AWG samples per symbol} = F_{sample} / F_{symbol} = 2160$$

$$512 \text{ K} / 2160 = 242 = \text{Maximum \# of unique symbols created}$$

A 2^7 - 1 (127) length sequence will be used to give enough flexibility in signal characteristics.

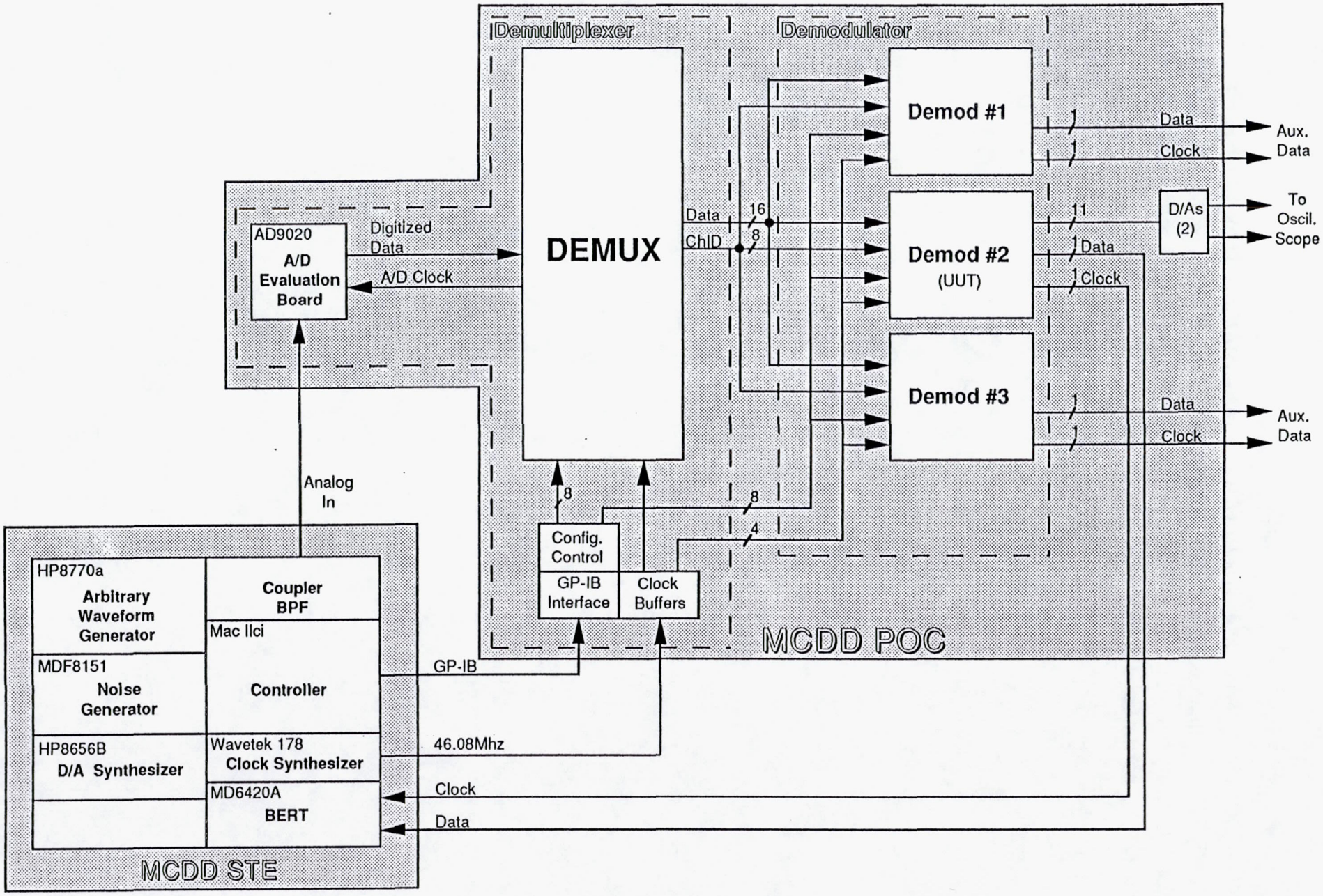
Another constraint is the maximum number of users that can be accommodated without clipping both the AWG D/A converter and the MCDD POC A/D converter. The AWG has a data width of 12 bits (+/- 2047), a conservative number for the maximum total signal amplitude would be 2000. A conservative minimum for each channel amplitude, to eliminate quantization effects from the AWGs D/A, would be 10. This would allow 2000 / 10 = 200 users to be loaded into the AWG. This maximum of 2000 would only be obtained if all signals reached their maximum value at the same time. If we take into account that each channel will have signals with various phase and frequency relationships, we can use the power of each user to estimate the maximum number of users. With a maximum power of $2000^2 / 2$, and an individual user power of $10^2 / 2$, we get a total of $2000^2 / 10^2 = 40{,}000$ users. With individual signal amplitude of 100 we could get $2000^2 / 100^2 = 400$ users. In either case we should be able to fully load the MCDD POC spectrum without significant quantization effects.

6.5 Critical Interfaces

All interfaces between commercial test equipment will be through the IEEE-488 bus (GP-IB). The Mac IIci will act as controller of this interface. Cabling between the controller and all other components will be through standard IEEE-488 cables, and connectors. An interface diagram is shown in Figure 6.5-1.

The POC will also have a limited GP-IB interface that will allow the controller to reconfigure the POC system. The POC will act in a listener only mode, such that the only action initiated across the GP-IB interface to the POC will be to write to the POCs control register.

The POC will also interface directly with the MD6420A Data Transmission Analyzer. The POC will output a demodulated digital data stream along with a corresponding data clock. Both signals will be TTL levels at either the wideband channel rate of 2.048 Mhz or the narrowband channel rate of 64 Khz.



MCDD POC Interface Diagram

Figure 6.5.1

6.6 Design Tradeoffs Summary and Conclusions

The commercial test equipment considered for the STE is summarized below with pertinent information outlined briefly. The item selected will be noted with an * :

Arbitrary Waveform Generator

*HP8770A:

Features -

a) GP-IB controlled

b) Digitally specified waveform generation

c) Up to 50 Mhz frequencies (non-aliased)

Disadvantages - NONE

Price - $25,000.00

No other alternatives

Selected Model : HP8770A

Programmable Attenuator (eliminated as of 5/5/91)

*HP11713A Switch Controller, HP8494G, and HP8496G:

Advantages -

a) GP-IB controlled

b) 0 - 120 dB in 1 and 10 dB steps

Disadvantages -

a) Separate switch controller and attenuators

Price - $3,495.00

No other alternatives are GP-IB controlled.

Selected Model : HP11713A Switch Controller, HP8494G, and HP8496G

Noise Generator

*MDF8151:

Advantages -

a) GP-IB controlled

b) +13 dB noise power

c) 0 -120 dB attenuation in 1 dB steps

d) power combiner included with 0-120dB attenuator for signal input

Disadvantages - NONE

Price - $5,350.00

Marconi 291B:

Advantages -

a) GP-IB controlled

b) +10 dB noise power

c) 0 -120 dB attenuation in .01 dB steps

Disadvantages -

a) power combiner not included

Price - $6,485.00

Selected Model : MDF8151

Bit Error Rate Test Set-

*Anritsu MD6420A with MD0620A GP-IB module:

Advantages -

a) GP-IB controlled

b) Auto-synchronization

c) PRN sequences of length 2**n-1

(n = 6,7,9,11,15,19,20,23)

Disadvantages -

a) Need additional module for GP-IB interface

Price - $7,895.00

HP3784a:

Advantages -

a) GP-IB controlled

b) Auto-synchronization

c) PRN sequences of length 2**n-1 (n = 6,9,11,15,17,20,23)

Disadvantages -

a) Does not support the STE requirement of a PRN sequence of 2**7-1

Price - $10,200.00

Tau-Tron BERTS-25 :

Advantages -

a) GP-IB controlled

b) Auto-synchronization

c) PRN sequences of length 2**n-1 (n = 7,23)

Disadvantages -

a) Does not spec lower than 100 Kbits/sec

Price - $15,850.00

Selected Model : Anritsu MD6420A with MD0620A GP-IB module

AWG D/A Frequency Source-

*HP8656B:

Advantages -

a) GP-IB controlled

b) 0.1 Khz - 990 Mhz Sine wave output

c) Phase reference in/out

d) Spurious: Harmonics < -30 dBc, Non-Harmonics < -60 dBc

e) Phase Noise: < -114 dBc/Hz @ 500 Mhz

Disadvantages - NONE

Price - $6,250.00

HP8657A:

Advantages -

a) GP-IB controlled

b) 100 Khz - 1040 Mhz Sine wave output

c) Phase reference in/out

d) Spurious: Harmonics < -30 dBc, Non-Harmonics < -60 dBc

e) Phase Noise: < -124 dBc/Hz @ 500 Mhz

Disadvantages - NONE

Price - $8,300.00

Wavetek 2405:

Advantages -

a) GP-IB controlled

b) .01Hz - 500 Mhz Sine wave output

c) Phase reference in/out

d) Spurious: Harmonics < -30 dBc, Non-Harmonics < -50 dBc

e) Phase Noise: < -113 dBc/Hz @ 500 Mhz

Disadvantages - NONE

Price - $4,995.00

Selected Model : HP8656B

POC Digital Clock Source-

*Wavetek 178:

Advantages -

a) GP-IB controlled

b) 0 - 50 Mhz Square wave output (TTL level)

c) Phase reference in/out

Disadvantages - NONE

Price - $6,285.00

HP3225B:

Advantages -

a) GP-IB controlled

b) 1 Khz - 10 Mhz Square wave output

c) Phase reference in/out

Disadvantages -

a) 23.04 Mhz square wave not available

Price - $4,590.00

HP8111A:

Advantages -

a) GP-IB controlled

b) 0 - 20 Mhz Square wave output

Disadvantages -

a) No phase reference in/out

b) 23.04 Mhz square wave not available

Price - $2,500.00

Selected Model : Wavetek 178

Controller

*Macintosh IIci 4/80, with NI-488, LABVIEW, and Think C:

Advantages -

a) GP-IB controller

b) Color Monitor

c) User friendly "front panel" interface

d) Proven design

e) General purpose computer can be used with many commercially available software packages

f) Comfortable programming environment

Disadvantages -

a) Need additional board for GP-IB interface

Price - $7,438.00

HP98581, with HP-BASIC, and WGL:

Advantages -

a) GP-IB controller

b) Color Monitor

c) Easy programming with HP-BASIC

d) Designed specifically for easy GP-IB control

e) Waveform Generation Language allows user to create waveforms similar with stack oriented function calls

Disadvantages -

a) User interface written in HP-BASIC

b) No operating system; no commercial software packages other than HP-specific exist

c) WGL very cryptic

Price - $13,500.00

AST386, with IEEE-488 card and Turbo C :

Advantages -

a) GP-IB controller

b) Color Monitor

c) General purpose computer can be used with many commercially available software packages

Disadvantages -

a) User interface written C

b) LABVIEW ("front panel") interface program not available for IBM-type systems

c) Need additional board for GP-IB interface

Price - $9,600.00

Selected Model : Macintosh IIci 4/80, with NI-488, LABVIEW, and Think C

Equipment Rack

*Electronic Enclosures 2K-219X40LR36F:

Advantages -

a) Double Bay
b) 36" Deep
c) Blower/Filter
d) Storage Drawers
e) Local Factory

Disadvantages - NONE

Price - $2,640.00

Equpto Challenger:

Advantages -

a) Double Bay
b) 36" Deep
c) Blower/Filter
d) Storage Drawers

Disadvantages - NONE

Price - $3,000.00

Selected Model : Electronic Enclosures 2K-219X40LR36F

6.7 Parts and Power Summary

6.7.1 Parts Summary

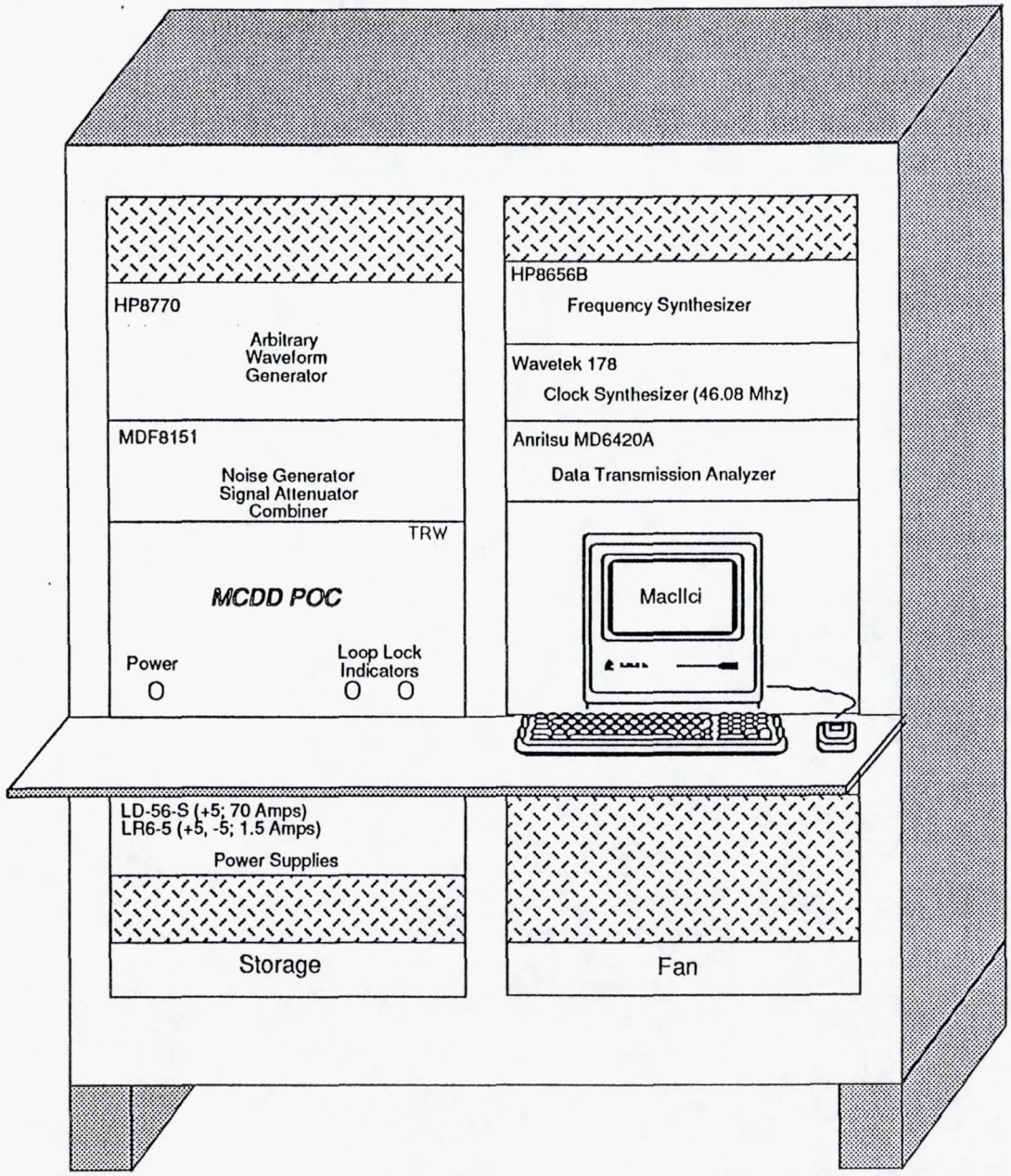
A parts summary for the STE is given below:

Part #	Vendor	Description	Qty
MCDD POC	TRW	POC model	1
HP8770	HP	Arbitrary Waveform Generator	1
MDF8151	MDF Products	Noise Generator	1
MD6420A	Anritsu	Data Transmission Analyzer	1
MD0620A	Anritsu	GP-IB Module for MD6420A	1
MD0626A	Anritsu	TTL Module for MD6420A	1
HP8656	HP	Synthesizer	1
178	Wavetek	Synthesizer/Function Generator	1
DP17.3-10.8-8	Lark	Band Pass Filter	1
TBD	TBD	Coupler	1
Mac IIci	Apple	STE Controller CPU with 4/80	1
		Color Monitor	1
		Extended Keyboard	1
NI-488	National Instr.	IEEE-488 Interface Card	1
LABVIEW	National Instr.	IEEE-488 Interface software	1
Think C	Symantec	C Compiler/Debugger/Editor	1
HP10833D	HP	IEEE-488 0.5 meter cable	5
HP10833B	HP	IEEE-488 2.0 meter cable	1
2K-series	Wiley	6 ft Double Bay Rack	1
BT101EVM	Brooktree	8 bit D/A Evaluation Board	1

6.7.2 Power Dissipation

Power dissipation for the STE is summarized as follows:

Part #	Description	Qty	Power
MCDD POC	POC model	1	200 VA
HP8770	Arbitrary Waveform Generator	1	440 VA
MDF8151	Noise Generator	1	160 VA
MD6420A	Data Transmission Analyzer	1	180 VA
HP8656	Synthesizer	1	125 VA
Wavetek 178	Synthesizer/Function Generator	1	180 VA
HP11713A	Switch/Attenuator Controller	1	50 VA
Mac IIci	STE Controller CPU with 4/80	1	220 VA



STE

Figure 6.7-1

6.8 Test Approach

Since the STE is comprised mainly of commercial test equipment, the checkout phase will primarily involve verifying correct software operation. Once the software is completed then the functionality of the STE will be verified. The various components of the STE will be checked out as follows:

Component	Test(s)
POC	(a) Verify control configuration is modified via GP-IB.
HP8770a	(a) Load test waveform sequence, via GP-IB, verify correct frequency relationship exists between D/A Synthesizer and generated waveform using Spectrum Analyzer. (b) Load sample waveform sequence, verify via Spectrum Analyzer that general frequency characteristic exists.
MDF8151	(a) Vary power level, via GP-IB, verify output noise power via Spectrum Analyzer. (b) Combine output of HP8770a (in cases (a) & (b) above), verify composite waveform via Spectrum Analyzer.
MD6420A	(a) Configure BERT and read BER figure via GP-IB.
HP8656B	(a) Vary phase and frequency via GP-IB. Verify via Spectrum Analyzer.
Wavetek 178	(a) Vary frequency via GP-IB, verify correct clock frequency via oscilloscope & analyzer
All Synthesizers	(a) Verify phase lock relationship via oscilloscope.
Band Pass Filter	(a) Inject noise from MDF8151, verify filter characteristic via Spectrum Analyzer
Coupler	(a) Combine two CW tones and verify composite via Spectrum Analyzer

Calibration: To get meaningful results from BER measurements, the input waveform and communication channel must be fully characterized within the accuracy desired of the test results. This procedure can be done several ways. A method used previously was to take A/D samples, uploaded to a computer via a GP-IB controllable Logic Analyzer, to get accurate measurements of the input Eb/No. This method had accuracy

to 1/100 of a dB. This procedure can also be performed with a Spectrum Analyzer, but is only accurate to about 1/10 of a dB.

To get accurate Eb/No values it is also necessary to characterize the equivalent noise bandwidth of the Band Pass Filter. This can be accomplished using a HP3585B Spectrum Analyzer which has the capability to output a tone that sweeps through a band of interest (this is input to the filter), while measuring the power output from the filter. This procedure has been performed previously with good success.

6.9 Issues and Concerns

One concern is the verification of input signals to the MCDD POC. It might be difficult to verify correct signal characteristics of waveforms output from the AWG without a channelizer and demodulator. It will be simple to verify correct frequency relationships, but phase information is more difficult to observe.

7.0 TEST PLAN AND PROCEDURES

7.1 Test Plan

The STE will be responsible for the detailed evaluation of the POC model performance and compliance with the POC requirements. The STE will allow test signal modifications to be made easily, without hardware modifications.

Functional Testing: The POC will demonstrate proper operation of all POC sub-systems by continuous reception of up-link messages from each of the possible active channels under ideal conditions. The possible active channels are: 3 Wideband channels or 2 Wideband channels and 4 Narrowband channels. It will also be possible to view, with an oscilloscope, the I - Q constellation and eye-diagram (of either I or Q).

Performance Testing:

- BER vs. Eb/No will be measured with and without adjacent channel interference (ACI) and up to 8 dB dynamic range.
- BER vs. Eb/No will be measured with carrier frequency offset and bit rate offset,
- BER vs. Eb/No with ACI and without pulse shaping
- Verify ability of Demod to independently track NB channels

7.2 TEST LISTING

7.2.1 Functional Tests

1a. Verify I - Q constellation and eye-diagram.

1b. Verify proper operation of all POC sub-systems under ideal conditions.

7.2.2 Performance Tests

2. BER vs. Eb/No without ACI.
3. BER vs. Eb/No with ACI, and with and without 8 dB variation between

channels. ACI will consist of populating the channels adjacent to the channel under test with time-offset PRN sequences.

3b. BER vs. Eb/No with no pulse shaping.

4. BER vs. Eb/No with carrier frequency offset.

5a. BER vs. Eb/No with symbol rate offset single AWG.

5b. BER vs. Eb/No with symbol rate offset, two AWG.

6. BER vs. Eb/No with frequency and symbol rate offset and ACI.

7. ASCII test.

7.3 Test Procedures

The test procedures will be referenced as in the test listing above.

7.3.1 Functional Tests

1a. Verify I - Q constellation and eye diagram.

1b. Verify proper operation of all POC sub-systems at high SNR, no carrier frequency, symbol rate, or symbol time offsets.

Procedure:

a) Load AWG with wideband channel of interest, modulated with a 2^7-1 PRN code, and run. Leave adjacent channels empty.

b) Set noise level and adjust signal attenuation to give desired Eb/No.

c) Verify POC and STE synchronization via Loop-Lock indicator on POC front panel.

d) Measure BER; Verify within specification.

e) Configure channel of interest to narrowband mode.

f) Repeat steps a - e four times with the AWG loaded with a different narrowband channel each time.

g) Repeat steps a - e with the AWG loaded with an adjacent WB channel output connected to the BER test set.

h) Repeat steps a - e with the AWG loaded with the other adjacent WB channel output connected to the BER test set.

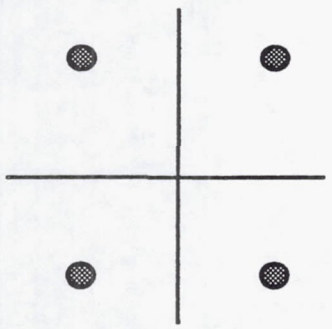
Predicted Results: BER of 5e-7 for input Eb/No = 10.8 dB WB, 10.9 dB NB,for all channels.

Procedure:

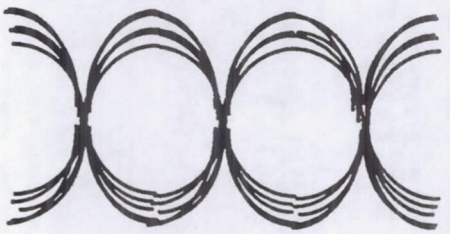
a) Load AWG with wideband channel of interest, modulated with a 2^7-1 PRN code, and run.
b) Connect D/A outputs (one for I and one for Q) to oscilloscope.
c) Place scope in X-Y mode to view I - Q constellation.
d) Place scope in normal triggering mode (either channel) to view eye-diagram.
e) Increase noise power level to observe effects.

Predicted Results:

I - Q Constellation



Eye Diagram



PERFORMANCE TESTS

2. BER vs Eb/No WITHOUT ACI

- MEASURE BER AT Eb/No = 8, 9, 10, 11 AND 12 dB FOR WB AND NB

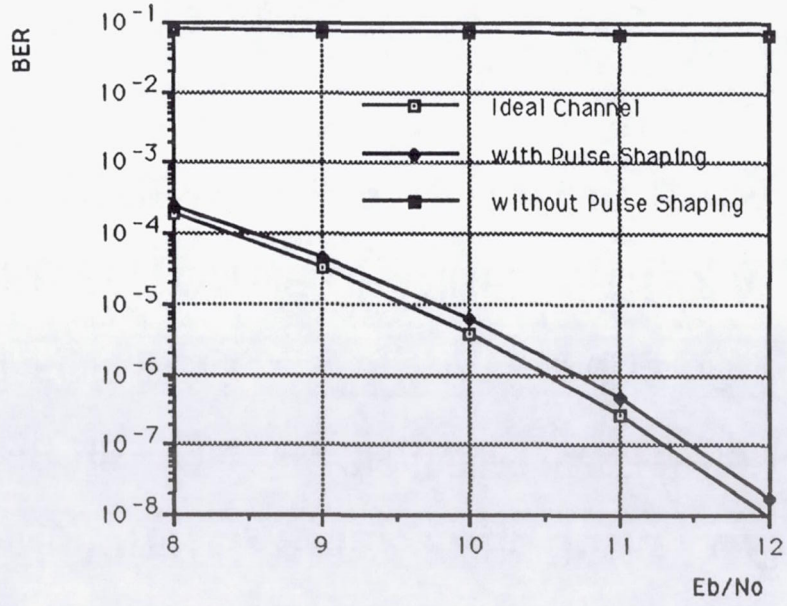
3a. BER vs Eb/No WITH ACI

- MEASURE BER AT Eb/No = 8, 9, 10, 11 AND 12 dB FOR WB AND NB
  - WITH EQUAL POWER
  - WITH ADJACENT CHANNELS 8 dB ABOVE CHANNEL OF INTEREST

3b. BER vs. Eb/No WITH ACI NO PULSE SHAPING

- SAME AS 2a

BER PLOT FOR TEST 3b



PERFORMANCE TESTS (CONT'D)

4. BER vs Eb/No WITH CARRIER FREQUENCY OFFSET, WITH ACI (8db)

- MEASURE BER ON WB CHANNEL WITH ±50 AND 100 KHz, OFFSET
- REPEAT FOR Eb/No = 8, 9, 10, 11 and 12 dB
- MEASURE BER ON NB CHANNEL WITH ±2 AND 3 KHz OFFSET
- REPEAT FOR Eb/No = 8, 9, 10, 11 AND 12 dB

PERFORMANCE TESTS (CONT'D)

5a. BER vs Eb/No WITH SYMBOL RATE OFFSET WITH ACI (8db), SINGLE AWG

- MEASURE BER ON WB CHANNEL WITH ±20, 40 AND 50 Kbps SYMBOL RATE OFFSET
- REPEAT FOR Eb/No = 8, 9, 10, 11 AND 12 dB
- MEASURE BER ON NB CHANNEL WITH ±1.0, 1.25 and 1.5 Kbps SYMBOL RATE OFFSET
- REPEAT FOR Eb/No =8, 9, 10, 11 AND 12 dB

5b. BER vs Eb/No WITH SYMBOL RATE OFFSET WITH ACI (8 dB), TWO AWG

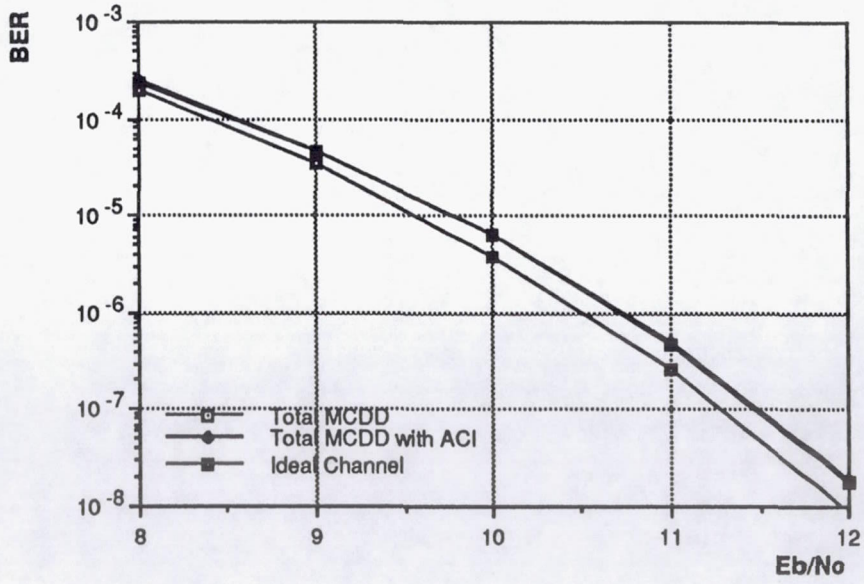
- LOAD AWG #1 WITH WB (NB) AS IN 5a BUT WITH NO ACI
- LOAD AWG #2 AS WITH TWO WB (NB)ADJACENT CHANNELS
- REPEAT TEST AS IN 5a

PERFORMANCE TESTS (CONT'D)

6. **BER vs Eb/No WITH FREQUENCY AND SYMBOL RATE OFFSET AND ACI (NEW TEST, NOT IMPLEMENTED YET)**
   - MEASURE BER: ON WB CHANNEL WITH +100KHz AND +50 Kpbs OFFSET
     ON WB CHANNEL WITH +100KHz AND -50Kpbs OFFSET
     ON WB CHANNEL WITH -100KHz AND +50Kpbs OFFSET
     ON WB CHANNEL WITH -100KHz AND -50Kpbs OFFSET
     ON NB CHANNEL WITH +3KHz AND +1.5 Kpbs OFFSET
     ON NB CHANNEL WITH +3KHz AND -1.5 Kpbs OFFSET
7. **ASCII TEST**
   - LOAD AWG WITH ASCII MESSAGE ON CHANNEL OF INTEREST
   - TRANSMIT AND VERIFY RECEPTION AT TERMINAL

TRW

BER PLOTS FOR TOTAL MCDD



APPENDIX A: MCDD A/D SIZING JUSTIFICATION

The MCDD A/D size (number of bits) has been selected to accommodate the input dynamic range - the performance figure of merit being BER. The following is a clarification of the assumptions and analysis used to derive the 8 bit baseline sizing.

As signal plus thermal noise loading is varied over an A/D input range, several phenomena occur. As the input power decreases such that few quantization steps are used, the percentage of quantization error increases. Although this effect is actually a signal distortion, the error can be modeled accurately as an additional noise. By comparing the quantization and thermal noises, the degradation caused by the quantization noise can be calculated. At high power loadings into the A/D, the A/D chip begins to play a dramatic role in the performance. As input signals begin to saturate the A/D, harmonics and intermodulation products are formed that alias inband due to sampling. If many tones constitute the input signal at the high end, many products will be formed and again a "clipping noise" model will apply.

For MCDD, the following assumptions concerning the A/D input dynamic range will be made to start.

1. Difference between max and min signal users is 8 dB

2. Thermal noise in detection bandwidth (38 KHz) at BER operating point of interest is 11.6 dB below smallest signal.

3. Maximum number of simultaneous users at A/D input is 728 (26 wideband channels x 28 narrowband channels/ wideband channel).

The criteria for evaluating A/D sizing and loading is BER performance. Under maximum loading conditions, 728 simultaneous users will be present at SNRs (in detection bandwidth) of 11.6 +8 = 19.6 dB. The thermal noise contribution to the total power will therefore be less than 0.1 dB and will be ignored. The distribution of the composite signal can be assumed to be Gaussian since it is the sum of numerous modulated tones. Figure 1 shows the ratio of the output thermal noise power to the

A/D induced noise power. A/D loading for various size A/Ds when Gaussian noise is the A/D input.

For the purposes of this analysis, Loading Factor is defined as:

$$LF = 10 \log (P_n/V_p^2), \quad \text{where}$$
$$P_n = \text{A/D input noise power}$$
$$V_p^2 = \text{A/D clip voltage squared}$$

As the loading factor decreases, the percentage of A/D induced noise increases due to quantization noise. As loading increases, "clipping noise" rapidly begins to dominate. For an 8 bit A/D, the optimal loading is at LF = -12 dB (see figure). This is commonly referred to as 4σ loading, since $\frac{1}{10^{-12/20}} \approx 4$

Let's look at MCDD performance if maximum loading is placed at a -12 dB loading factor. To do this we want to compare the A/D induced noise to the thermal noise. We must also be careful to compare the noise power in the same bandwidth. I like to determine each noise power, then subtract out (dB) the bandwidth over which it occurs to get an A/D induced noise density and a thermal noise density. They can then be compared to determine Eb/No degradation. The common reference power for all levels will be the sinewave power that just clips in the A/D - call it A/D clip power. Such a signal has power $V_p^2/2$ and if applied to the A/D has loading power $10 \log \left(\frac{V_p^2}{2}/V_p^2\right) = -3$ dB

Under max loading (728 simultaneous users):

Quantization Noise Density

-9.0 dB	Total signal power (-12 dB LF + 3 dB A/D clip power)
-41.0 dB	A/D quantization noise w.r.t. signal power (from figure)
-76.6 dB	Bandwidth of quantization noise, fs/2 $\left(10 \log \left(\frac{92.06 \times 10^6}{2}\right)\right)$
-126.6 dB/Hz	Quantization noise density

Worst case thermal noise density:

-9.0 dB	Total signal power - maximum users
-28.6 dB	728 signals (10 log (728))
-8.0 dB	Max to min user difference
-11.6 dB	Thermal noise to signal difference at BER operating point
-45.8 dB	Detection bandwidth (10 log (38×10^3))
-103.0 db/Hz	Thermal noise density

The degradation to Eb/No from quantization noise is given by the equation:

$$\text{Deg} = 10 \log (1 = 10^{(\text{quart-thermal})/10})$$

or

Deg = 0.02 dB for 23.6 difference above

If loading is set as described above for an 8 bit A/D, the minimum loading scenario (single user) can be evaluated as follows. The minimum scenario is a single minimum power user. The SNR in the detection bandwidth for the single user is 11.6 dB, but the SNR in the A/D input bandwidth will be 11.6 - 28.6 = -17.0 dB. The A/D input will therefore again be Gaussian distributed. First we must find the loading factor this corresponds to: (use Figure 1 again). The signal has a LF of

-12.0 dB	Loading factor for 728 max users
-28.6 dB	Convert to 1 max user
-8.0 dB	Convert to 1 min user
-48.6 dB	Loading factor for 1 min user

-48.6 dB	
+17.0 dB	Amt. Noise is above 1 min user
-31.6 dB	LF for input signal plus noise

Extrapolating Figure 1, this LF will give an NPR of 21.4 dB. The quantization density calculation in terms of the A/D chip power is:

Under min. Loading Quantization Noise Density

-31.6 dB	LF of input signal plus noise
+3.0 dB	Convert LF to power w.r.t. A/D clip power
-21.4 dB	A/D quantization noise w.r.t. signal plus noise power
-76.6 dB	Bandwidth of quantization noise
-126.6 dB/Hz	Quantization noise density, same as before

The thermal noise density is the same as previously calculated. Therefore, under minimum loading conditions the Eb/No degradation is 0.02 dB as before. Maximum and minimum loading performance is the same at this A/D operating point.

Note that if the gain to the A/D is increased, the max loading performance will degrade as "clipping noise" is introduced, yet minimum loading performance will improve as the thermal noise moves above the quantization noise. The opposite response occurs for decreasing gain to the A/D. Additional signal dynamic range or gain variations prior to the A/D will degrade performance. Use the degradation equation to evaluate other dynamic ranges. For each additional A/D bit 6 dB more dynamic range can be accommodated.

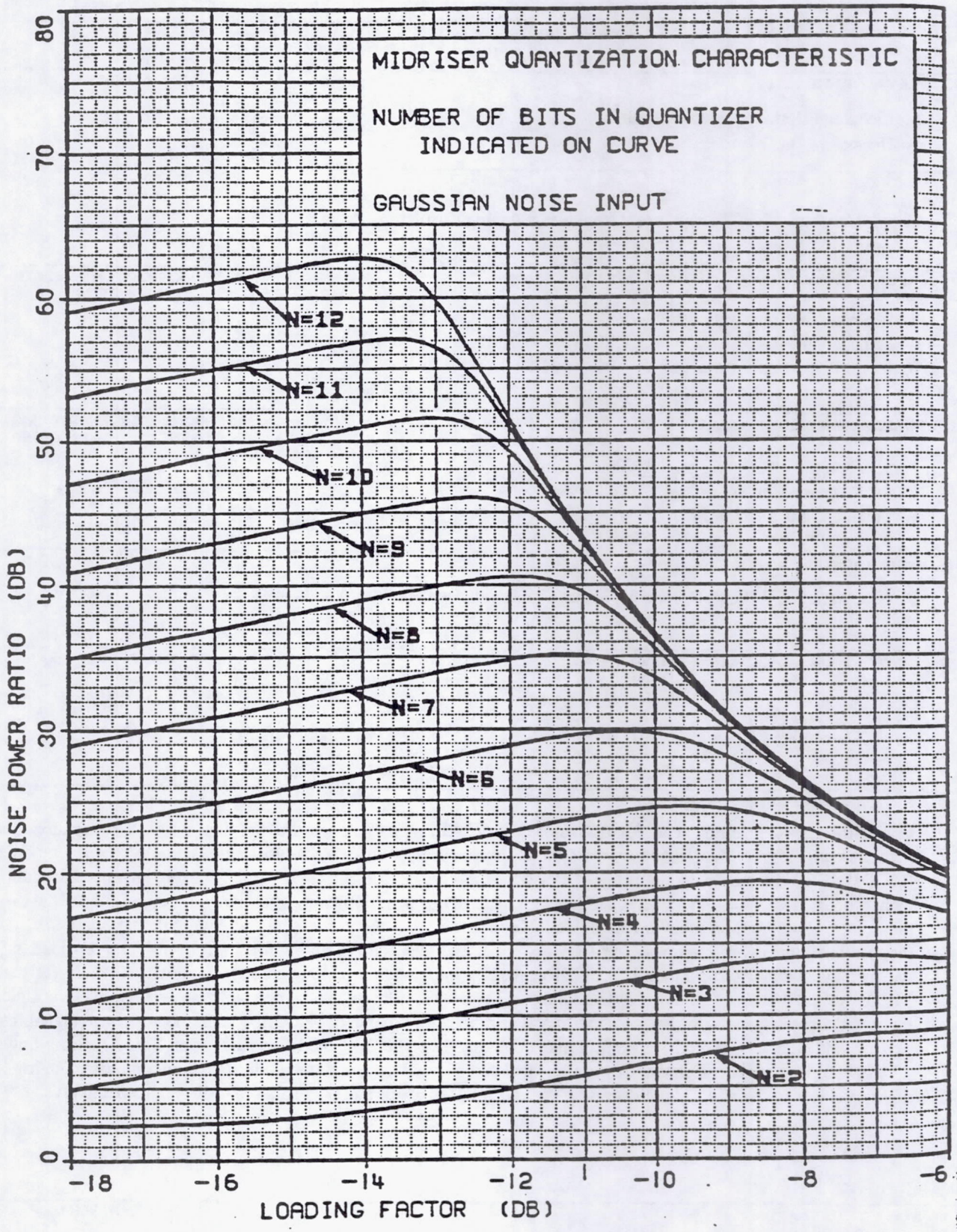


Figure A1 Theoretical A/D Noise Power Ratio Performance

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13. ABSTRACT ***(Maximum 200 words)***

One of the critical satellite technologies in a meshed VSAT (very small aperture terminal) satellite communication networks utilizing FDMA (frequency division multiple access) uplinks is a multichannel demultiplexer/demodulator (MCDD). TRW Electronic Systems Group developed a proof-of-concept (POC) MCDD using advanced digital technologies. This POC model demonstrates the capability of demultiplexing and demodulating multiple low to medium data rate FDMA uplinks with potential for expansion to demultiplexing and demodulating hundreds to thousands of narrowband uplinks. The TRW approach uses baseband sampling followed by successive wideband and narrowband channelizers with each channelizer feeding into a multirate, time-shared demodulator. A full-scale MCDD would consist of an 8 bit A/D sampling at 92.16 MHz, four wideband channelizers capable of demultiplexing eight wideband channels, thirty-two narrowband channelizers capable of demultiplexing one wideband signal into 32 narrowband channels, and thirty-two multirate demodulators. The POC model consists of an 8 bit A/D sampling at 23.04 MHz, one wideband channelizer, 16 narrowband channelizers, and three multirate demodulators. The implementation loss of the wideband and narrowband channels is 0.3dB and 0.75dB at 10^{-7} E_b/N_0 respectively.

14. SUBJECT TERMS

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