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A Planar Approximation for the Least Reliable Bit Log-Likelihood Ratio of 8-PSK Modulation

William H. Thesling
Cleveland State University
Cleveland, Ohio

and

Mark J. Vanderaar
NYMA, Inc.
Brook Park, Ohio

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William H. Thesling¹
Department of Electrical Engineering
Cleveland State University
Cleveland, Ohio 44115

Mark J. Vanderaar²
NYMA, Inc.
2001 Aerospace Parkway
Brookpark, Ohio 44142

Abstract - The optimum decoding of component codes in Block Coded Modulation (BCM) schemes requires the use of the Log-Likelihood Ratio (LLR) as the signal metric. An approximation to the LLR for the Least Reliable Bit (LRB) in an 8-PSK modulation based on planar equations with fixed point arithmetic is developed that is both accurate and easily realizable for practical BCM schemes. Through an error power analysis and an example simulation it is shown that the approximation results in 0.06 dB in degradation over the exact expression at an E_s/N_0 of 10 dB. It is also shown that the approximation can be realized in combinatorial logic using roughly 7300 transistors. This compares favorably to a look up table approach in typical systems.

Index Terms - Log-likelihood ratio, 8-PSK, block coded modulation, multilevel codes, multistage decoding, soft-decision metric

I. INTRODUCTION

Combined modulation and coding is an efficient method of conveying information through power and bandwidth limited channels. Imai-Hirakawa coding schemes [1], also called block coded modulation (BCM) can achieve Trellis-Coded Modulation (TCM) performance in a block structure. They can be an alternative to TCM in systems where a block format, code flexibility, and decoding speed are important. Though a BCM scheme is generally not Maximum Likelihood (ML), its structure can offer more coding for less complexity than TCM in some systems.

The BCM structure applies individual codes for each bit in a modulated symbol. These component codes are denoted C_0, C_1, \dots, C_{n-1} where n is the number of bits in the symbol. Each component code can be a block or convolutional code, and they can be decoded with or without channel information. The error correcting capability of the i^{th} component code is chosen in accordance with the channel bit error probability associated with the i^{th} ($i = 0, 1, \dots, n-1$) bit in the modulated symbol as well as taking into account information provided by the

decoder from the $(i-1)^{th}$ level. Usually the overall goal is to "balance" the system by obtaining approximately the same decoded error probability for each level of decoded bits.

II. 8-PSK LOG-LIKELIHOOD RATIO

In applications such as satellite and mobile communications, the digital modulation format 8-PSK is one emerging as a practical choice in bandwidth and power limited situations. One example of BCM applied to 8-PSK uses three component codes, one for each bit in an 8-PSK symbol. The associated encoder and decoder structures are illustrated in Figures 1 and 2. In order to obtain a benefit from multistage decoding the least significant bit in the constellation must alternate between binary 0 and 1 as the symbols are defined from 0 to $7\pi/8$ radians [2]. A mapping that fits this criteria is shown in Figure 3. Each symbol is defined to have a power normalized to 1.

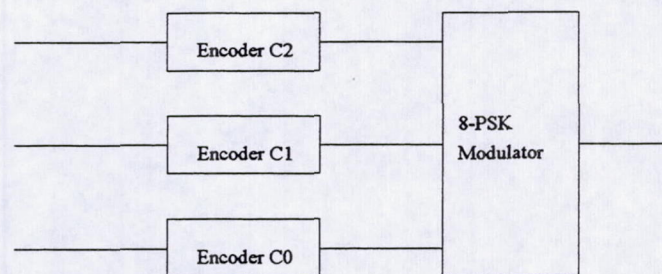


Figure 1 : General 8-PSK Multilevel Encoder / Modulator

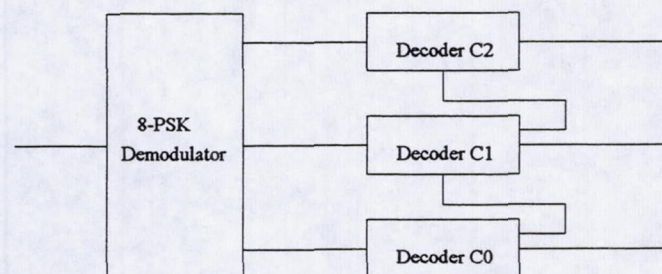


Figure 2 : General 8-PSK Multilevel / Multistage Decoder / Demodulator

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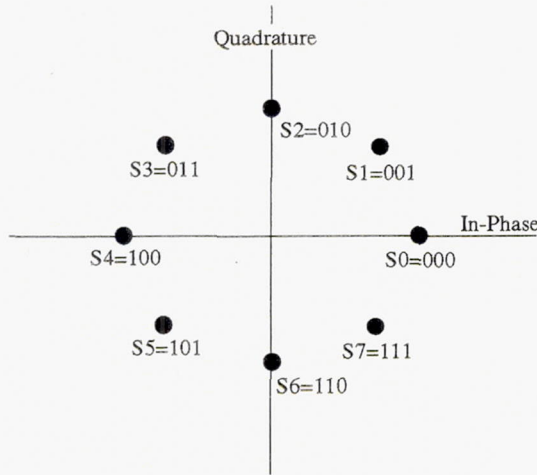


Figure 3 : 8-PSK Constellation

Multistage decoding requires that the bottom code, C_0 , is decoded first. The signal metric for Maximum Likelihood decoding (MLD) for this code with the given constellation assignment is the Log-Likelihood Ratio (LLR) [3, 4]. In 8-PSK, the LLR of the rightmost bit or the Least Reliable Bit (LRB) being a binary 0 can be expressed as

$$LLR(I, Q) = \ln \left[\frac{\sum_{i=0, \text{even}}^7 -\left(\frac{E_s}{N_0}\right) d_i^2}{\sum_{i=0, \text{odd}}^7 -\left(\frac{E_s}{N_0}\right) d_i^2} \right]$$

Where, E_s is the energy per symbol, N_0 is the single sided noise power spectral density, and d_i is the distance from the (I,Q) point to the i^{th} symbol in the constellation.

This expression contains the likelihood of each of four symbols that contain a binary 0 in the LRB in the numerator and the likelihood of each of the four symbols that contain a binary 1 in the denominator. The LLR as a function of the in-phase and quadrature component as a function of the E_s/N_0 equal to 2, 6, and 10 dB is plotted in Figures 4-6, respectively. Note that in each case the LLR has been normalized so that the maximum absolute value is equal to 1 in each of these plots.

An explicit evaluation of the LLR in real-time is very undesirable in most practical systems due to the number of complicated mathematical operations required. For this reason a look-up table (LUT) approach is used in which the values of the LLR at a particular E_s/N_0 are calculated off-line and stored in dedicated memory. This LUT approach is

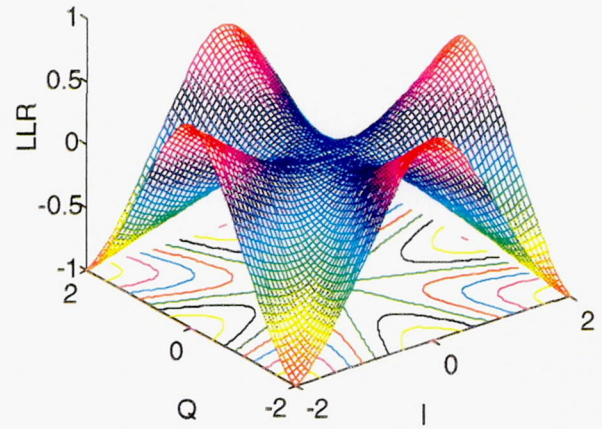


Figure 4, LLR at $E_s/N_0 = 2.0$ dB.

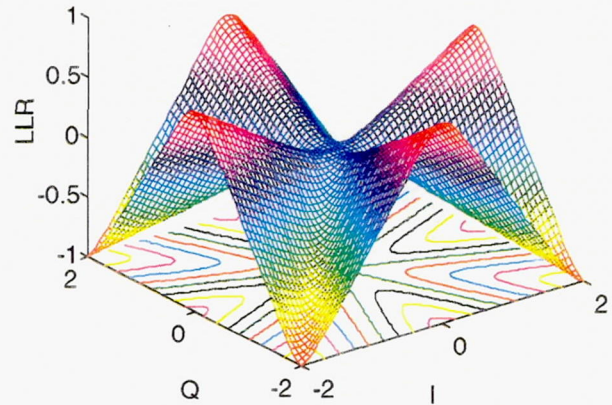


Figure 5, LLR at $E_s/N_0 = 6.0$ dB.

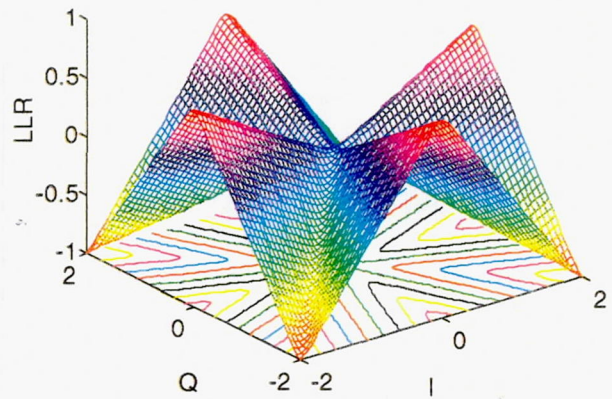


Figure 6, LLR at $E_s/N_0 = 10.0$ dB.

commonly used for branch metrics in TCM decoders.

Visual inspection of the figure illustrating the LLR at an E_s/N_o of 10 dB suggests that it can be approximated by a series of 8 planes. The value of 10 dB is of particular relevance because it is near the required E_s/N_o to obtain a bit-error-rate of 10^{-6} commonly required in practical coded satellite systems. Note that the LLR for the given 8-PSK constellation is symmetric about the first quadrant. This results in the observation that the LLR is invariant with respect to the absolute value function for both the in-phase (I) and quadrature (Q) channels. Therefore, by replacing I and Q with their respective absolute values, the problem is now one of evaluating one of two planar equations as a function of I and Q . The two remaining planes are symmetric about the line $I = Q$. Therefore, if $I > Q$ only one planar equation at (I, Q) needs to be evaluated. If $I < Q$ the planar equation is evaluated at (Q, I) . The equation of the LLR planar approximation (LLRPA) can be expressed as,

$$LLRPA(I, Q) = \max \left\{ \alpha \times \text{abs}(I) + \beta \times \text{abs}(Q) \right. \\ \left. \alpha \times \text{abs}(Q) + \beta \times \text{abs}(I) \right\}$$

Where,

$$\frac{\alpha}{\beta} = -\tan 22.5^\circ$$

It is important to remember that these values, whether the exact LLR or the LLR planar approximation, are the soft decision metrics to be sent to the decoder. The performance of the decoder does not depend on the *absolute* size of the metrics. Thus, any positive scaling factor that is convenient can be chosen since multiplying all outputs by some constant has no effect on the performance of the decoder. This translates into a freedom of choice for one of the two values for α and β . The other value is determined by the ratio between α and β . If one considers fixed point arithmetic (integers) $\alpha = 29$, and $\beta = -70$ preserves the ratio quite well. Therefore, the equation of the plane is given by,

$$LLRPA(I, Q) = \max \left\{ \begin{array}{l} 29 \times \text{abs}(I) - 70 \times \text{abs}(Q) \\ 29 \times \text{abs}(Q) - 70 \times \text{abs}(I) \end{array} \right\}$$

The evaluation of the LLRPA as a function of I and Q is plotted in Figure 7. Unlike the exact values for the LLR, the planar approximation is not dependent on the E_s/N_o . Visually, the plot looks like an increasing good fit to the LLR as the E_s/N_o increases.

III. ERROR POWER ANALYSIS

An error power analysis can be used to find the "effective" SNR degradation due to the use of the LLRPA as compared

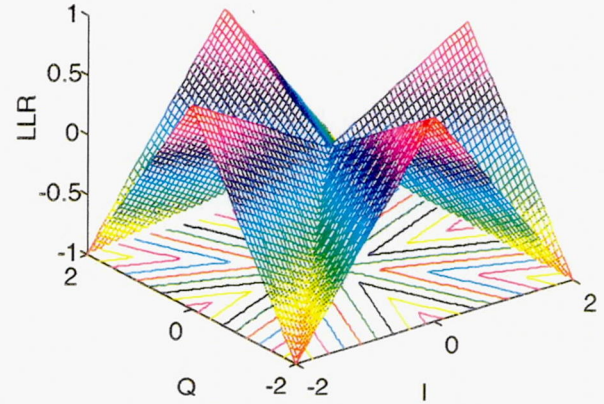


Figure 7. Log Likelihood Ratio Planar Approximation.

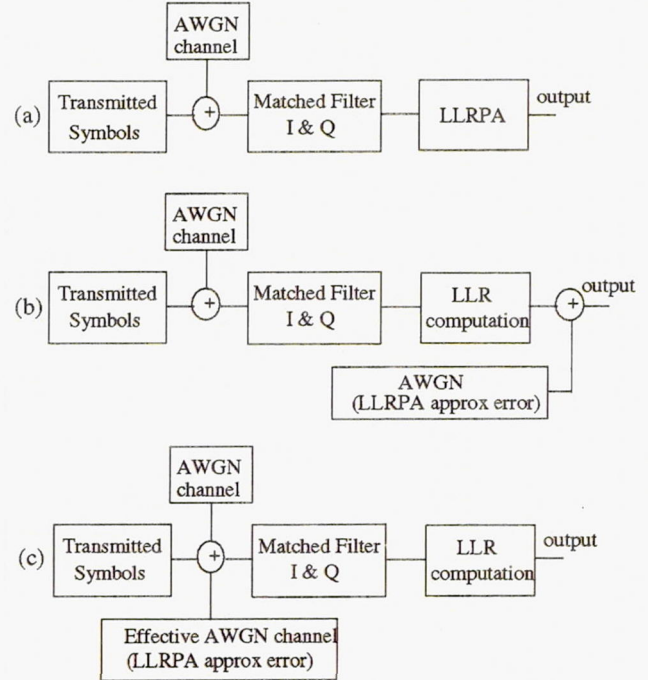


Figure 8. Channel model with the LLRPA and the effective model relative to performing the true LLR computation.

to the exact LLR. The approach finds the power associated with the LLRPA and considers it as an additional noise term. This noise is considered as an effective increase in the channel noise as depicted in Figure 8 (a, b, c). This analysis is an estimate since both the effect of the non-linearity associated with LLR device and the fact that the noise term associated with Figure 8b (the LLRPA noise) is correlated to the channel noise are ignored.

The LLRPA noise in Figure 8b is the error noise of the approximation. Although this noise is i.i.d. and therefore white, it is not gaussian. However, since a decoder effectively adds and subtracts many outputs, the intermediate values tend toward a gaussian distribution giving a valid approximate error power analysis.

The relative size of the LLRPA noise term associated with Figure 8c is estimated by the relative size of the noise term associated with Figure 8b. In other words, the expected power in the noise term in Figure 8b is used to compare to the expected power in the output from the exact LLR. The error power is given by the expected value of the squared difference signal. The difference signal is given by:

$$DS(I, Q) = LLR(I, Q) - \lambda[LLRPA(I, Q)]$$

$$DS(I, Q) = \ln \left[\frac{\sum_{i=0, \text{even}}^7 \left(\frac{E_s}{N_0} \right)^2 d_i^2}{\sum_{i=0, \text{odd}}^7 \left(\frac{E_s}{N_0} \right)^2 d_i^2} \right] - \lambda \max \left\{ \begin{array}{l} 29abs(I) - 70abs(Q) \\ 29abs(Q) - 70abs(I) \end{array} \right\}$$

The coefficient λ is a scaling factor to find the best fit between the LLR and the LLRPA. The best fit is defined when the expected value of the squared value is minimized. As mentioned in section II, a scaling factor on the LLRPA does not effect the performance of the decoder. The coefficient λ is therefore omitted in any real system, though it is important in an analysis of error power.

Once the difference signal $DS(I, Q)$ is determined, the expected value of the squared error is found as;

$$E[DS^2] = \sum_{i=0}^7 P(S_i) \iint p_i(I, Q) DS^2(I, Q) dIdQ$$

Where $P(S_i)$ is the probability that the i^{th} signal was sent, and $p_i(I, Q)$ is the probability of receiving the point (I, Q) given the i^{th} signal constellation point was transmitted. If the assumption is made that the eight signals are equally likely, this simplifies to;

$$E[DS^2] = \iint p(I, Q) DS^2(I, Q) dIdQ$$

Here $p(I, Q)$ is the probability of receiving the point (I, Q) given a particular symbol was transmitted. The expected squared difference signal can then be related to the expected squared signal or signal power (after the LLR operation). This is essentially the expected squared output (no approximation) which is given by;

$$E[LLR^2] = \iint p(I, Q) LLR^2(I, Q) dIdQ$$

The ratio

$$\frac{E[DS^2]}{E[LLR^2]}$$

is an estimate of the additional noise to signal ratio due to the log likelihood ratio planar approximation. An estimate of the overall signal to noise ratio is obtained by

$$SNR_{\text{estimate}} = \frac{1}{\frac{1}{SNR_{\text{channel}}} + \frac{E[DS^2]}{E[LLR^2]}}$$

In dB, this corresponds to a reduction in SNR given by,

$$SNR_{\text{db, reduction}} = SNR_{\text{channel, db}} - SNR_{\text{estimate, db}}$$

IV. AN ILLUSTRATIVE EXAMPLE

As an example, consider an E_s/N_0 of 6.0 dB as an operating point. Figure 5 illustrates the LLR for this SNR. The difference signal (DS) is the difference between the normalized LLR and the planar approximation (with the appropriate λ). This is shown in Figure 9. Figure 10 is the squared error signal. Figure 11 is the probability density function of the received signal for a given symbol transmitted at E_s/N_0 of 6.0 dB.

The ratio of the expected squared difference signal and the expected squared true LLR is an estimate of the additional effective noise to signal ratio.

For the example, the estimated reduction in the signal to noise ratio due to the log likelihood ratio planar approximation is calculated numerically to be 0.216 dB. This is an estimate of the degradation associated with the LLRPA.

As previously mentioned, this is an upper estimate of the degradation due to the fact that the LLRPA noise is highly correlated with the channel noise.

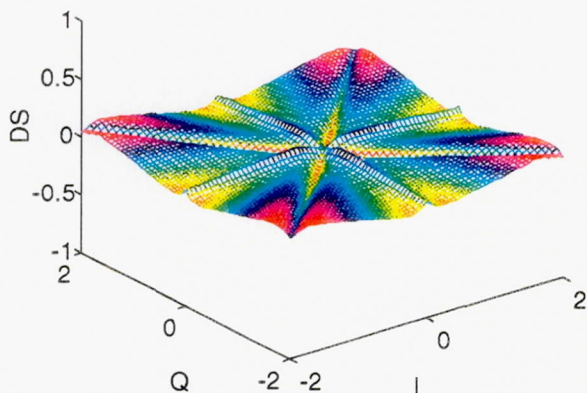


Figure 9. The Difference signal as a function of I & Q.

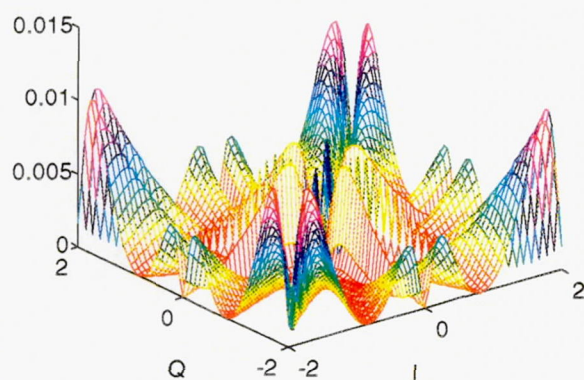


Figure 10. The squared difference signal.

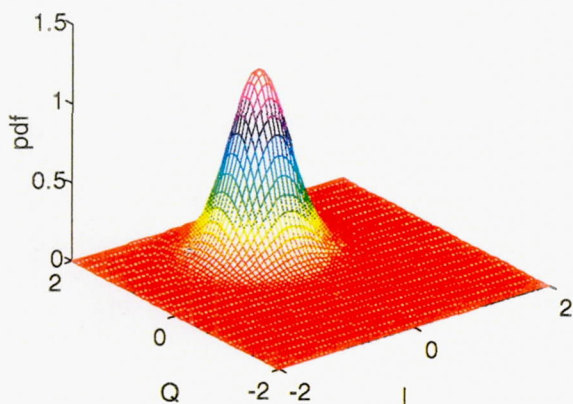
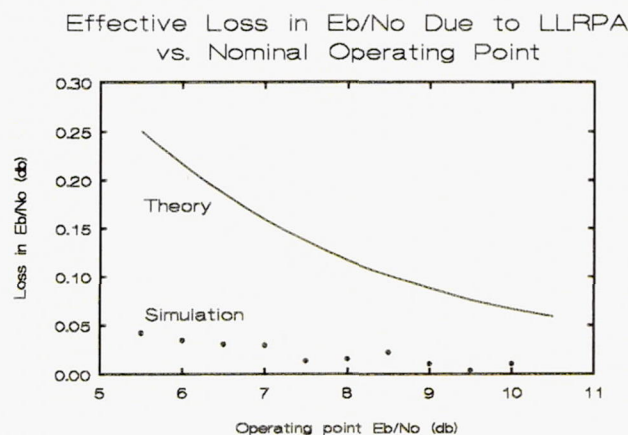


Figure 11. pdf of the received signal at $E_s/N_o = 6.0$ dB

The accuracy of the approximate degradation can be assessed through simulation. A realistic simulation example uses the rate $1/4$, 16 state convolutional code given in [3] as C_0 , and 8 bits of quantization on both I and Q . One simulation uses a LLR look up table, while the other simulation uses the LLRPA equation. Both simulations use the same PN sequences for both the information and the noise. The exact LLR look up table performs better for all operating points (values of channel SNR), but the difference (as measured in SNR reduction for a given BER or SNR operating point) is quite small. The following graph illustrates the difference between the SNR reductions computed theoretically, and those found by simulation.



V. IMPLEMENTATION ANALYSIS

Though it is intuitive that a hardware realization of the LLRPA would be simpler than the exact LLR, in practice the exact LLR is computed via a look-up table (LUT). As such, an implementation analysis is really a comparison between the hardware realization of the LLRPA and a sufficient size memory based LUT to find the exact LLR. This type of comparison is somewhat system dependent, and the comparison presented here that is based strictly on an approximate transistor count must be taken within the system context.

For example, in a demodulator/decoder that is realized mostly with VLSI technology, coming off the device to an external LUT and then back on the device has disadvantages in both the speed of external routing and the increase of VLSI complexity due to increased I/O requirements. In this case, the number of transistors required for both techniques in the context of the particular VLSI device is a good comparison. Further, systems implemented with programmable logic such as Field Programmable Gate Arrays (FPGAs) tend to be constrained in the amount of memory space available, making the LLRPA implementation attractive. Alternately, systems

that are not fully realized in VLSI circuitry may benefit from the potential simplicity of a single memory device to perform the LLR LUT. The benefits gained from the design maturity of memory technology may outweigh a specific implementation of an algorithm such as the LLRPA.

A block diagram of the required processing for the LLRPA is shown in Figure 13. The block diagram indicates that 8 bit data from an analog to digital converter or digital filter is first converted to its absolute value. The resulting 7 bit magnitude values of I and Q are compared to find the greatest value. If the magnitude of I is greater than or equal to the magnitude of Q , the I data follows the top leg of processing and the Q the bottom leg. If the magnitude of Q is greater than the magnitude of I this is reversed. The appropriate values are then multiplied by either 29 or 70 and are then subtracted. The result is then divided by 256 to maintain only the 6 most significant bits.

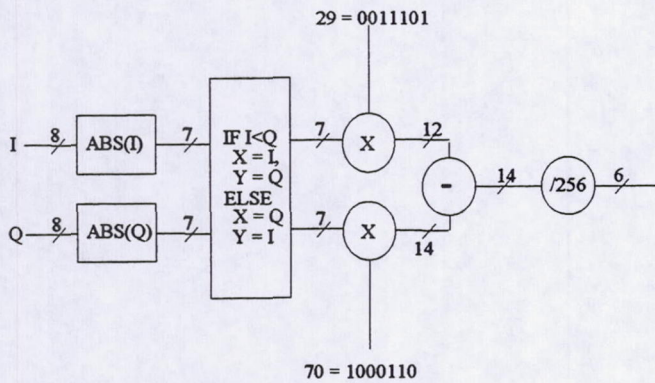


Figure 13 :Implementation Block Diagram of the LLRPA

The complexity of the LLRPA implementation can be approximated through a rough estimation of the complexity in terms of gates for each of these functions. These gate counts are then converted to an overall estimate of transistor count. The accuracy of the approximation is subject to the goals of a particular system in terms of speed, power consumption, or real estate. Further, the number representation presented by the upstream hardware and required by the downstream hardware can also be relevant.

First, in its worst case, the absolute value function requires a magnitude compare, a select, and then an 8 bit addition or subtraction, requiring a rough total of 200 gates. Second, the magnitude comparison and select require about 80 gates. Next, the fixed multiplies can be realized by shifts and adds resulting in about 250 gates. The final subtractor requires approximately 200 gates and the divider chooses the 6 MSBs. Assuming an average of 10 transistors per gate, the total approximate transistor count is 7300.

For a rough comparison, the LUT table would have a $2^8 \times 2^8 = 65,536$ memory addresses. If each address contains 6 bits to maintain good quantization accuracy this corresponds to a $65,536 \times 6$ memory. A Static Random Access Memory (SRAM) that used 5 transistors per cell would require 1.97×10^6 transistors. This ignores the transistors required for column decoders, row decoders, and read/write circuitry.

These estimates indicate that the LLRPA requires approximately 270 times fewer transistors than the LUT. Also, the LLRPA computation can be implemented in parallel to obtain an operating speed increase. In this case, the number of transistors will increase by the factor of the speed increase plus the gates required to multiplex and demultiplex the I/O.

VI. LLR AND THE C1 CODE

Once the bottom code C0 is decoded and re-encoded, the re-encoded data is used to determine which of two 4-PSK symbol sets is used for the remaining 2 bits. That is set $\{S0, S2, S4, S6\}$ or set $\{S1, S3, S5, S7\}$ with respect to figure 3. Given one of these two sets, the least reliable bit (which is really the middle bit now) must also alternate between 0 and 1 as the symbols are encountered moving around the circumference of the circle. The data impressed onto this symbol is from the C1 code. For decoding purposes, the optimum signal metric is the log likelihood ratio for this constellation. If we consider the set $\{S0, S2, S4, S6\}$ then the LLR of the right most bit (middle bit) being a binary 0 verses being a 1 can be expressed as,

$$LLR_{4PSK}(I, Q) = \ln \left[\frac{\sum_{i=0,4} e^{-\left(\frac{E_s}{N_0}\right) d_i^2}}{\sum_{i=2,6} e^{-\left(\frac{E_s}{N_0}\right) d_i^2}} \right]$$

which can be approximated by,

$$LLRPA_{4PSK} = abs(I) - abs(Q)$$

We state without proof that error associated with this approximation is less than that associated with C0. It should be mentioned that if the set in question is the set $\{S1, S3, S5, S7\}$, then a "rotation" operation will need to be performed.

VII. CONCLUSIONS

It has been shown that the planar approximation to the log-likelihood ratio in the least reliable bit of an 8PSK

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