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Testing and Performance Analysis of a 650 Mbps QPPM Modem for Free-Space Laser Communications

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TESTING AND PERFORMANCE ANALYSIS OF A 650 MBPS QPPM MODEM FOR FREE-SPACE LASER COMMUNICATIONS

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Introduction

Free-space optical communication systems digitally modulate lasers for wireless transmission of data over large distances. They offer size, weight, and power advantages over existing radio frequency systems for high data rate applications. Because of atmospheric degradation effects free-space optical systems are best suited for inter-satellite links and space exploration applications. For their use in such applications certain technologies such as described in this paper must first be proven viable.

NASA's Lewis Research Center, under the High-speed Laser Integrated Terminal Electronics (Hi-LITE) project, has developed a prototype modem to demonstrate some of the technologies needed for free-space optical links. The Hi-LITE modem employs quaternary pulse position modulation (QPPM) and direct detection at 325 Megabits per second (Mbps) on two parallel channels. A single 650 Mbps per second data stream is multiplexed and demultiplexed between the two channels by the modem. The two channels use slightly different optical carriers, offset in wavelength by at least 10 nm, so they can be distinguished by the receiver.

Previous papers have reported on the design, fabrication, and basic performance of Hi-LITE.[1,2,3] This paper describes the testing and performance in greater detail, including effects of data type, video data, operational mode, simulated platform jitter, pointing errors, Doppler frequency shifting, and channel timing skew. Analysis of how specific components and subsystems contribute to performance degradations is also presented. To facilitate the discussion of test results, a brief review of the QPPM modem and special test equipment is given first.

Quaternary Pulse Position Modulation (QPPM)

In a direct detection system the laser transmitter is intensity modulated. Hi-LITE does this with digital data stream control of the bias current to a semiconductor laser diode. Digital "ones" and "zeros" effectively turn the laser on and off, converting the electrical digital data signals to optical pulses. At the receiver the opposite is achieved as an avalanche photodiode (APD) converts the optical pulses back to electrical pulses. In order to reduce the average laser duty cycle and improve data detection performance, QPPM is used to encode two digital data bits into one symbol or laser pulse. As Figure 1 illustrates, there are four possible symbols in QPPM, each having a pulse in one of four time slots of the symbol period. With this encoding, the laser duty cycle is reduced from 50% to 25%. Also, data detection is improved by 3 dB over simple threshold detection of an on/off keyed data stream using maximum likelihood detection in the receiver. In this detection scheme, the energy of each of the four slots for a given symbol is compared to each of the other slots to determine in which slot the pulse most likely occurred.

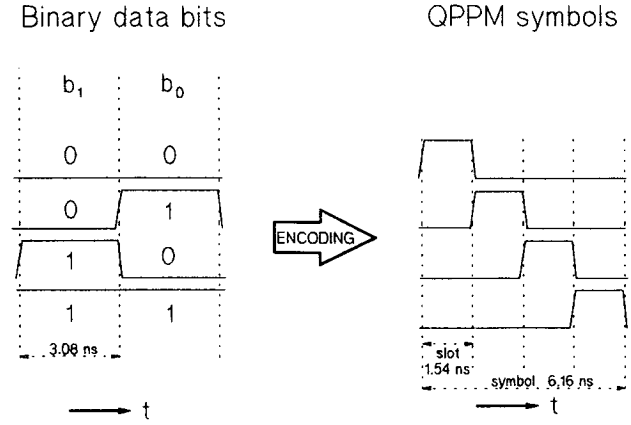

Figure 1: QPPM encoding and timing.

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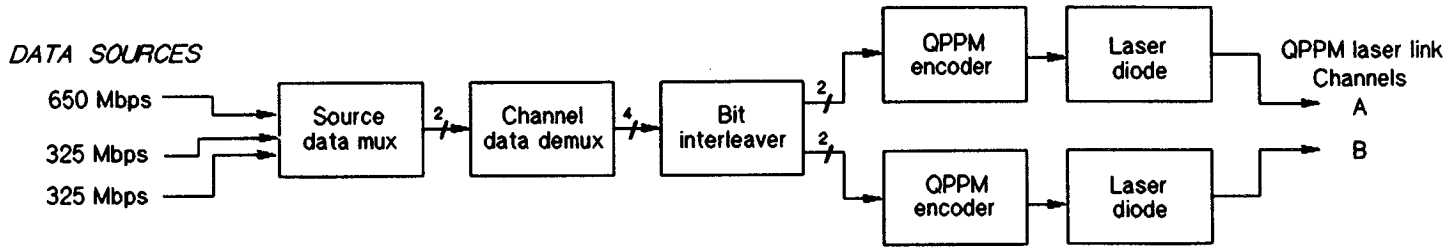

Figure 2: Block diagram of Hi-LITE dual-channel QPPM transmitter.

QPPM Modem: Transmitter and Receiver

The prototype QPPM modem is comprised of separate transmit and receive chassis. The transmit chassis converts one 650 Mbps or two 325 Mbps binary data sources into two 325 Mbps QPPM data output streams. The two QPPM outputs are then fed directly to separate laser diodes, as the functional block diagram of Figure 2 illustrates.

The receiver itself is housed in two chassis: the Analog Receive Chassis, containing the analog signal conditioning electronics; and the Digital Receive Chassis, containing primarily digital clock and data recovery circuits. A functional block diagram of the receiver is shown in Figure 3. The APD converts the received laser photons to an electrical signal, which is pre-amplified before going to the Analog Receive Chassis. Amplification, automatic gain control (AGC), and filtering are done by the Analog Receive Chassis to condition the signal for optimum clock and data recovery by the Digital Receive Chassis.

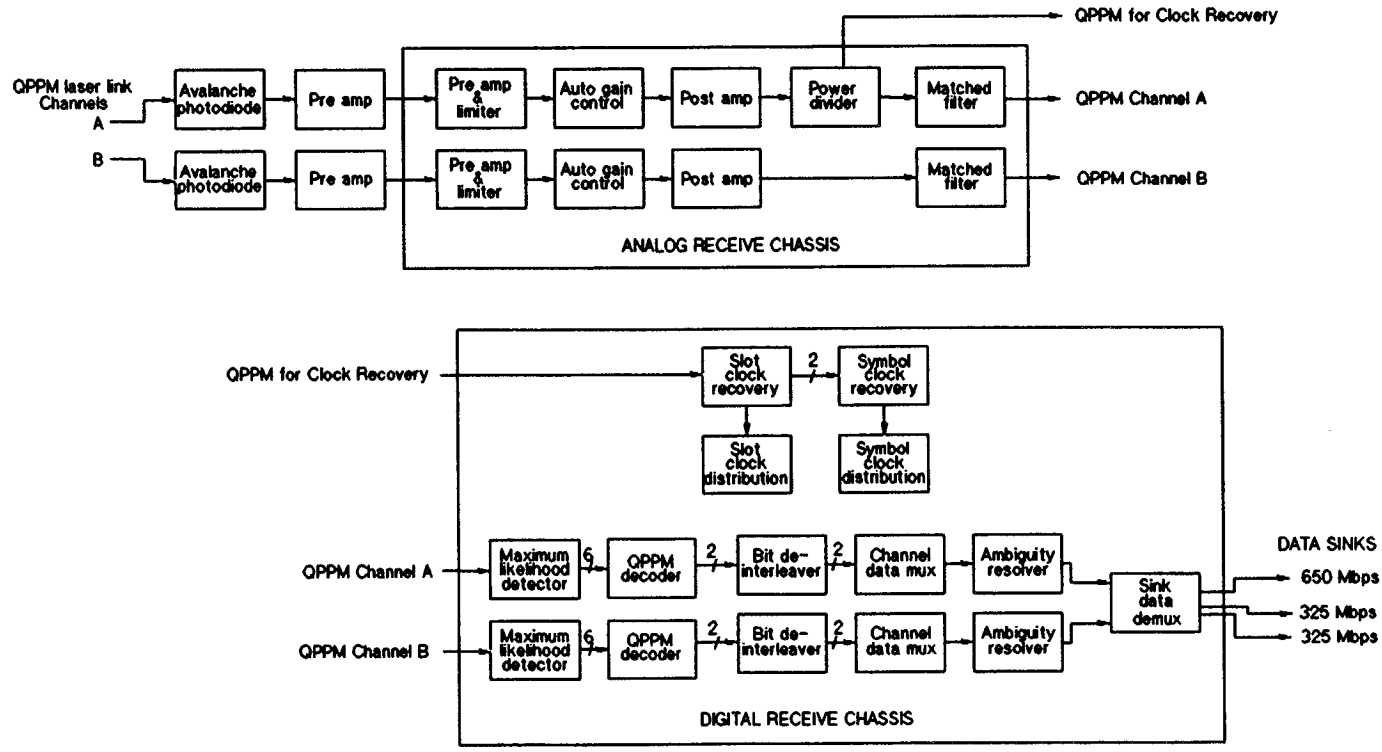

Figure 3: Block diagram of Hi-LITE dual-channel QPPM receiver.

All of the receiver functions are duplicated for the two QPPM 325 Mbps channels (A and B) with the exception of slot and symbol clock recovery. A signal is split off from channel A in the Analog Receive Chassis and then sent to the Digital Receive Chassis where it is used to recover slot and symbol clock for both channels A and B. A commercial module extracts the 650 MHz slot clock from the QPPM data stream with an injection-locked oscillator circuit, and then uses a threshold comparator to provide a first order approximation of the QPPM waveform for the symbol clock recovery circuit. Invalid symbol detection is done on the QPPM data stream by the symbol clock recovery circuit to determine by elimination which one of the four possible symbol boundaries is correct. The three incorrect symbol timings create many invalid symbols, (i.e. two pulses or no pulses within one symbol period).

The maximum likelihood detection circuits depend upon the recovered symbol clock for correct sampling of the QPPM waveforms. The QPPM decoder circuits then convert the symbols back to the original binary data, and finally the two 325 Mbps binary data streams are combined into one 650 Mbps stream. The 650 Mbps and the two 325 Mbps channels along with accompanying clocks are brought out to the chassis front panel for connection to appropriate data sinks.

Bit interleaving for the two 325 Mbps channels is an optional mode. In the transmitter, the two 325 Mbps binary streams are interleaved before the QPPM encoding, so that the QPPM symbols for each output channel are determined by one bit from each input stream. De-interleaving is performed reciprocally in the Digital Receive Chassis after the QPPM decoding. This enables the BER performance of one channel carrying real-time data, such as video, to be inferred from the BER measurement of the other channel carrying PRBS data.

Special Test Equipment

The modem is integrated with special test equipment (STE) to simulate some of the link degradations expected in a flight system. Simulation is done optically and electrically with the Optical STE and the Analog STE, respectively. The STE as well as the modem are controlled and monitored by a 386sx personal computer. Figure 4 functionally illustrates the operation of the two STEs and the computer within the Hi-LITE system.

A variable neutral density filter in the Optical STE (OSTE) attenuates the laser beam between the laser transmitter and APD receiver. This variable filter along with some fixed

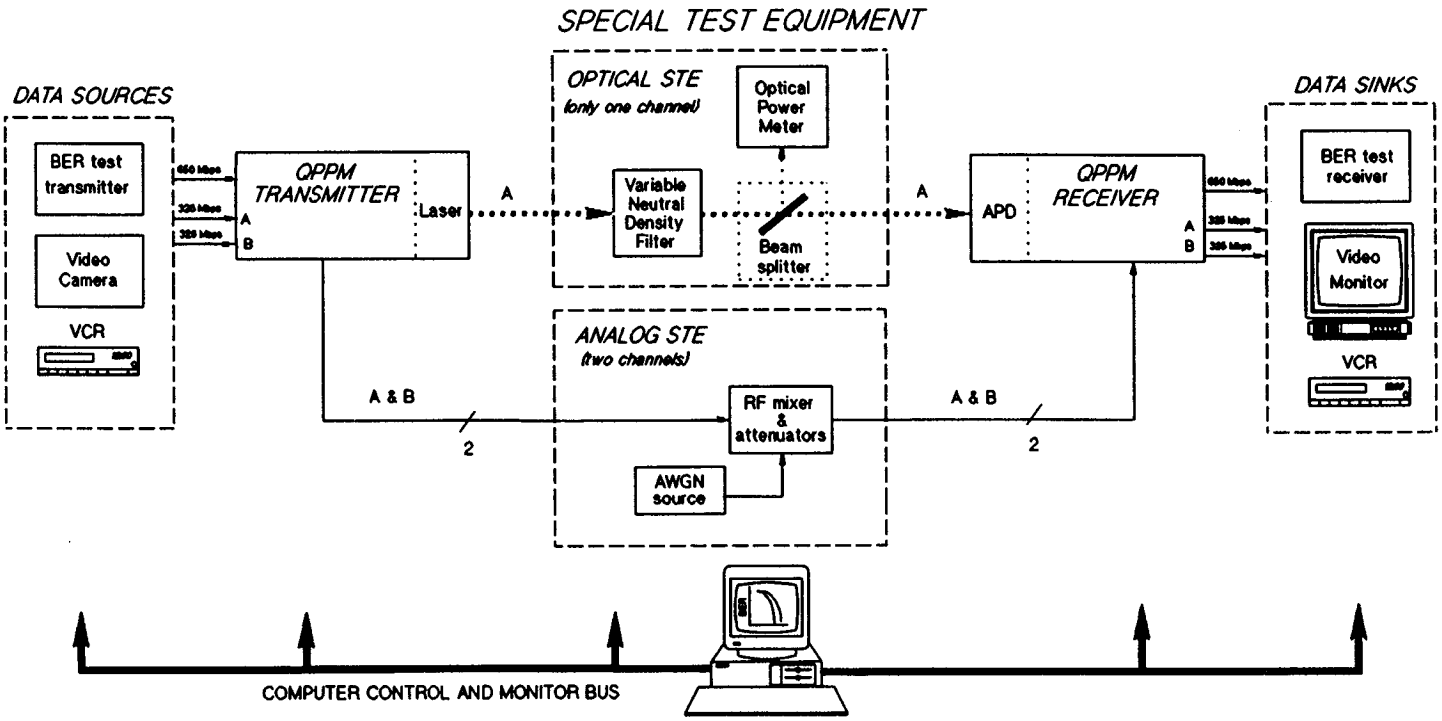

Figure 4: System test configuration block diagram.

filters simulate signal degradation due to background noise and beam divergence that occurs over several thousand kilometers of free-space, in a distance of less than a meter. A beam splitter provides for receiver optical power measurements. Note, as Figure 4 indicates, there is only one laser channel. The availability and high cost of such state-of-the-art lasers and APDs prevented the full dual channel optical link from being implemented.

However, a two channel radio frequency (rf) link was implemented with the Analog STE (ASTE).** Bypassing the optical carrier, the ASTE electrically attenuates, adds white Gaussian noise, and low-pass filters the QPPM signals at baseband. With attenuators for both signal and added noise, the ASTE has a wide and varied dynamic range. Most testing was done with the ASTE rather than the OSTE because of the ASTE's flexibility in adding noise or attenuating the signal, as well as its dual channel capability. For the following test results sections it is also important to note that a standard (CCITT Rec. O.151) $2^{23}1$ length pseudo random bit sequence (PRBS) was used for all tests, except where noted otherwise.

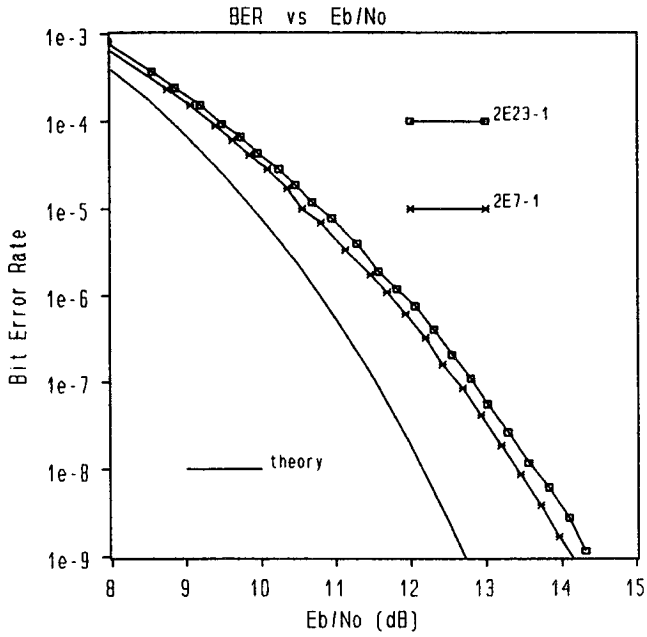

Figure 5: Pattern length sensitivity, 2^{23}-1 and 2^{7}-1 length PRBS.

Testing and Results

Effects of data type - slot clock and symbol timing recovery

A test of measuring bit error rate (BER) performance with different PRBS lengths showed that the receiver is sensitive to the type of data being sent through the link. As Figure 5 indicates, there is up to 0.3 dB E_b/N_o performance improvement for the shorter 2^{7}-1 length pattern compared to the 2^{23}-1 length pattern. (Figure 5 also shows a theoretical optimum BER curve for comparison, indicating the receiver's performance is about 1.5 dB away from optimum at a BER of 10^{-9}. This was reported previously.[3]) The receiver slot clock recovery circuits were found to be the major cause of this effect. This was demonstrated by testing with the slot clock fed from the transmitter directly to the receiver clock distribution board, so that the slot clock recovery circuits were bypassed. No sensitivity to different data pattern lengths could be seen in this configuration.

More specifically, the pattern sensitivity is related to timing jitter in the recovered slot clock. The clock is more difficult to extract from longer QPPM data patterns because the

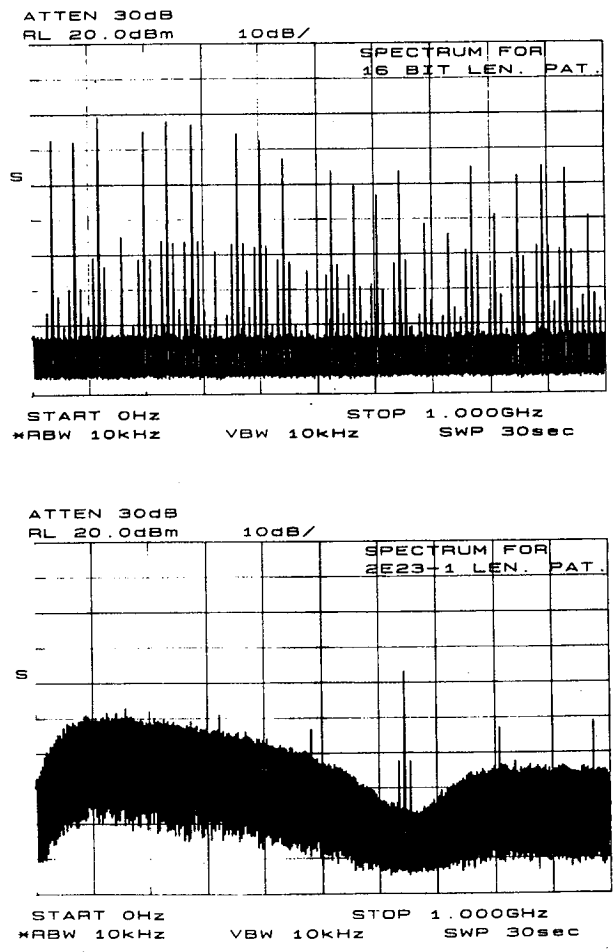

Figure 6: QPPM pattern noise spectra, 16 bit (top) and 2^{23}-1 bit (bottom) lengths.

**The Hi-LITE system also includes a Digital STE, the design of which was reported on in an earlier paper[1], but it has not been integrated with the system yet and will not be reported upon in this paper. The Digital STE was designed to simulate some of the effects of an optical link and especially the random nature of photon arrival and detection. Timing jitter on a symbol by symbol basis can be created with the Digital STE.

longer patterns have more pattern noise, as can be seen in the spectra of Figure 6. The result is more timing jitter on the recovered slot clock, as shown in oscilloscope photographs of Figure 7. Among other effects, this jitter leads to less than optimum sampling for the maximum likelihood detector, thus degrading BER performance.

Sensitivity to data type was also seen in the symbol timing recovery circuit performance. The symbol timing circuit "slips" when timing is shifted to one of the three incorrect symbol boundaries due to errors in the threshold detected data stream. For shorter length patterns, such as 2^7-1, and high E_b/N_o (>20 dB) the receiver is able to maintain symbol lock without slipping. But for longer patterns, such as 2^{23}-1 and video data, the circuit loses lock and incorrectly shifts timing regularly.

The symbol timing performance dependence on data type is probably linked to the slot clock recovery dependence and some non-optimum timing. Due to the relative complexity of the symbol timing recovery circuits, timing optimization by cable length trimming was not done during testing and integration of the boards. Cable and semi-rigid coax line lengths were determined in CAD simulation. Thus, with some non-ideal implementation, there may be some signals with marginal setup and hold times in the circuits that are adversely effected by slot clock jitter, known to increase with longer data patterns.

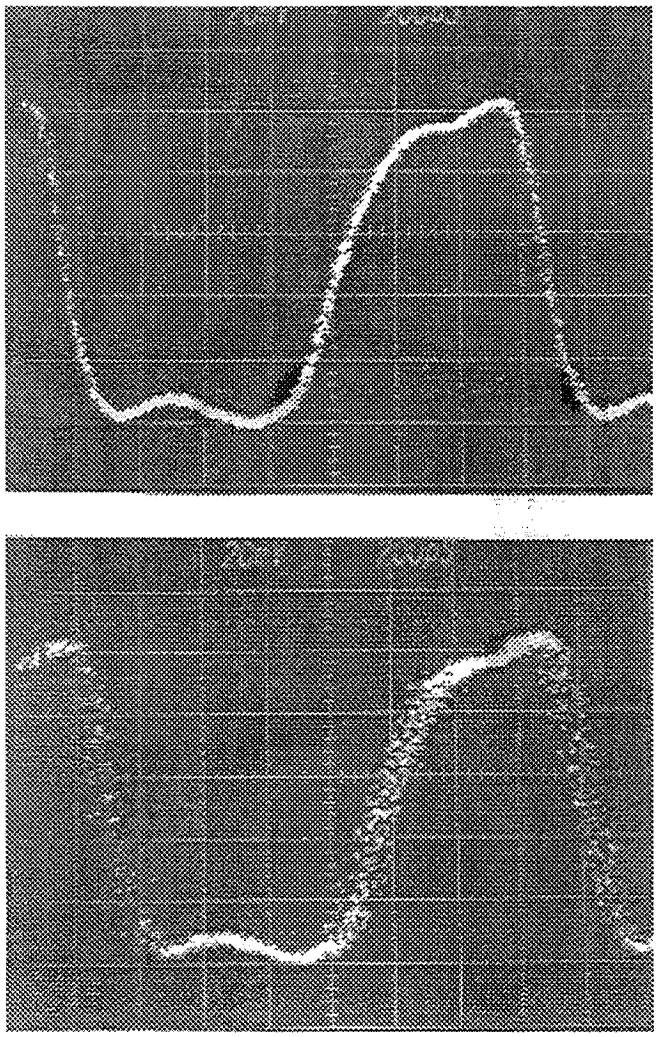

Figure 7: Recovered slot clock jitter, for 16 bit (top) and 2^{23}-1 bit (bottom) length patterns.

As expected, loss of symbol lock occurs more frequently as E_b/N_o is decreased, regardless of the data pattern. This is due to a combination of the increasing slot clock jitter and errors in the threshold detected QPPM data stream used by the symbol timing circuitry. For test purposes, the symbol timing recovery circuit is disabled once correct timing is acquired at high E_b/N_o (>20 dB). This allows operation at lower E_b/N_o without incorrect symbol timing shifts. However, as E_b/N_o is decreased below about 10 dB the increasing slot clock jitter leads to slot clock cycle slips. A single slot clock cycle slip makes the current symbol timing incorrect, so the circuit has to be enabled again to reacquire the correct timing. When running an automated test sequence the computer monitors BER to detect slot clock cycle slips. If the BER is very large (usually around 50%), the computer enables the symbol timing recovery circuit momentarily and then rechecks the BER.

Video data transmission

Figure 8 shows two video camera images transmitted through the ASTE link with different added noise conditions. In the foreground is a prototype modem circuit board, with the computer screen as a backdrop. The BER is displayed in the lower right corner of the screen, and the E_b/N_o is just to the left of the upper left corner of the circuit board. The top image of Figure 8 was transmitted with added noise corresponding to 15.15 dB E_b/N_o, while the bottom image was at 8.64 dB E_b/N_o. The "snow" effect evident in the bottom image is expected for a digital video data stream with random bit errors. With almost 1% of the bits in error (8.6×10^{-3}) the image is still intact. This is not surprising considering there are over 10 megabits of data transmitted for every video frame.[1] At higher BER received video images do start to "break-up" as the synchronization information becomes too corrupted for the VCR servo to maintain lock. A flight system, however, would be expected to operate at less than 1×10^{-6} BER, nearly an order of magnitude better than that in the top image of Figure 8, hence without visible degradation.

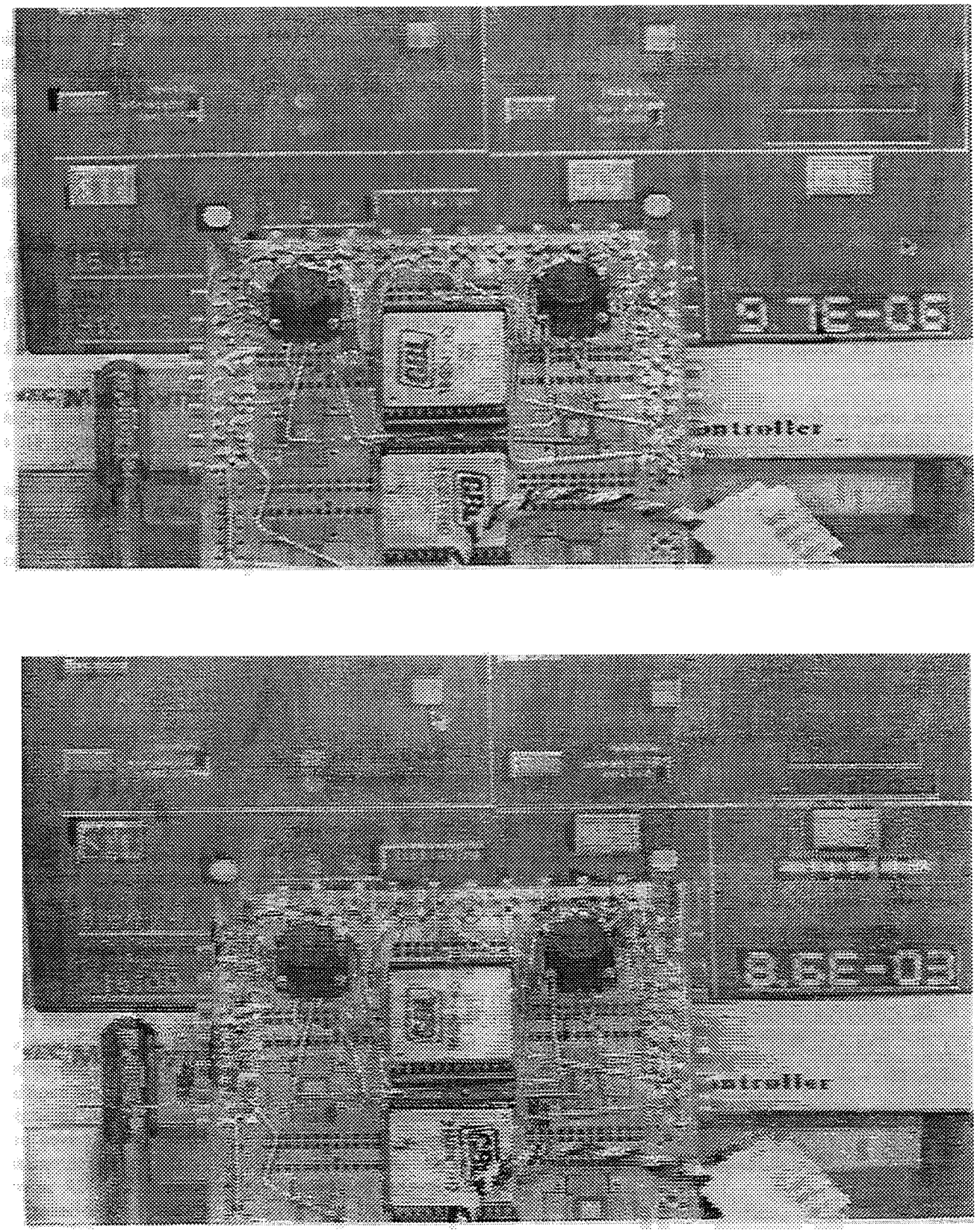

Figure 8: Transmitted video images at 15.15 E_b/N_o (top) and 8.64 dB E_b/N_o (bottom).

Operational modes - channel differences

Three main modes of operation are available with the Hi-LITE system: dual 325 Mbps transmission, single 650 Mbps transmission, and interleaved dual 325 Mbps transmission. Most of the testing was done in the simplest dual 325 mode, no interleaving, allowing characterization and comparison of the two 325 Mbps channels. Channel B of the receiver, however, cannot operate completely independently of channel A because the receiver requires channel A for clock and timing recovery. The receiver data recovery channels contained in the Digital Receive Chassis can operate independently because this chassis has separate inputs for clock recovery, channel A data recovery, and channel B data recovery. Comparison of the two Digital Receive Chassis data recovery channels was done using channel A of the Analog Receive Chassis and by simply switching cables at the chassis front panels. BER tests revealed almost identical performance for the two channels.

Comparison of the two channels in the Analog Receive Chassis is more difficult because the clock recovery signal is split from the channel A signal, (see Figure 3). Therefore, the overall channel B receiver performance is dependent upon the channel A Analog Receive Chassis performance, but the overall channel A receiver performance is not dependent on channel B. Oscilloscope photographs of Figure 9 compare channel A and B outputs of the Analog Receive Chassis when fed with the same input. The figure shows channel B broadens the QPPM pulses about 15% more than channel A. This broadening increases intersymbol interference leading to poorer BER performance. For this reason Channel A was used for BER testing with the single channel OSTE. The receiver's dual channel capabilities, however, are needed for interleaving and 650 Mbps modes of operation.

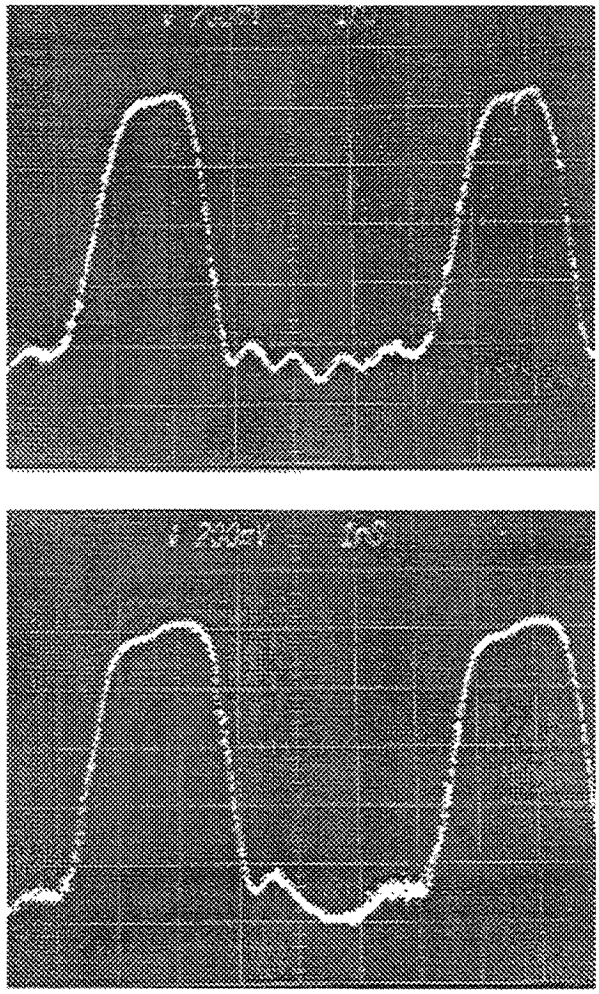

Figure 9: Analog Receiver Chassis outputs, channel A (top) and channel B (bottom).

Interleaving of two 325 Mbps channels is done on a bit by bit basis, so that each QPPM symbol is comprised of one bit from each channel. In this mode, when video data and PRBS data are sent interleaved, a BER measurement can be assessed on the video data transmission because the PRBS data and video data undergo the same link degradations. A symbol detection error has the same probability of affecting either channel. The two video images of Figure 8 discussed in the previous section were transmitted in the interleaving mode. As the computer screen shows, measured BERs were 9.7×10^{-6} for the top image and 8.6×10^{-3} for the bottom image.

These BER measurements, however, are not entirely accurate for the video data due to slight differences in the E_b/N_o levels of the two ASTE channels, whereas E_b/N_o measurements are only made on channel A. Some compensation to correct for ASTE component differences between channels was accomplished in the computer control software and by changing fixed attenuators. Figure 10 reveals the total channel A and B differences, including those in the ASTE. Channel A performs 3 to 5 dB better than channel B, and channel B has a region around 12 dB E_b/N_o where there is a very sudden change in performance. This discontinuity is due either to a non-linearity in the channel B ASTE noise attenuator, or a control software compensation limit.

But differences in the ASTE channels are not the only effects seen in the curves of Figure 10. If the link (in this case the ASTE) were the only source of channel differences, then interleave mode BER measurements should be identical for both channels at the receiver output. Interleaving two 2^{23}-1 length PRBS patterns revealed this is not the case. Two representative data points are shown in the table on the next page. Most of the BER performance difference between the two channels does disappear in the interleaving mode, but there is still about a factor of 2 difference.

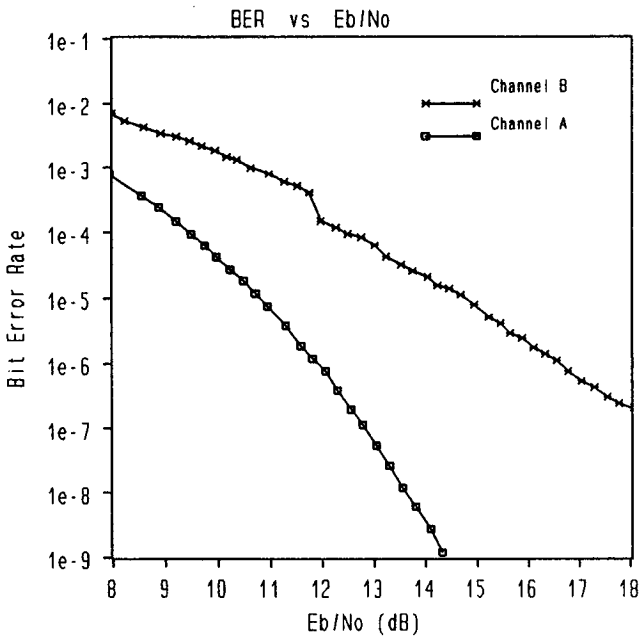

Figure 10: Total channel A and B performance differences.

Notice the calculated averages in the table for both the non-interleave and interleave mode measurements. Ideally the non-interleave BER average is the performance that both channels should see in the interleave mode. Instead, channel A's interleave mode BER was slightly above the average and channel B's slightly below the average. The interleave BER averages do match the non-interleave averages, indicating the digital portions of the transmitter and receiver are interleaving one bit from channel A and one bit from channel B properly, without adding errors. So, the slight performance difference seen between the two channels in the interleaving mode is because the Analog Receive channels are not perfectly equalized. The performance difference is also a quantified measure of the quality difference seen in the signal oscilloscope traces of Figure 9.

As mentioned previously, transmission of a single 650 Mbps data stream is accomplished by splitting it on a bit by bit basis between the two 325 Mbps channels, to be recombined at the receiver. Video data is not available at 650 Mbps so only PRBS data was used to test this mode. As expected, BER performance results in Figure 11 are an average of the channel A and B performances of Figure 10. The channel B characteristics dominate the 650 Mbps performance, such as the discontinuity at 12 dB, because errors occur at least 10 times more often on channel B than on channel A.

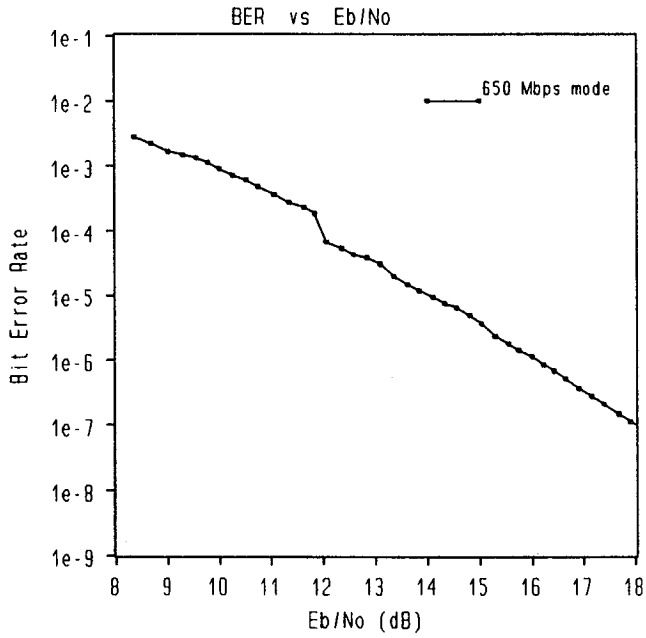

Figure 11: 650 Mbps mode performance.

Data point	Channel	BER Measurement	
		Non-Interleave	Interleave
1	A	3.7×10^{-7}	4.0×10^{-6}
1	B	1.3×10^{-5}	9.4×10^{-6}
AVERAGE for 1	A & B	6.7×10^{-6}	6.7×10^{-6}
2	A	4.4×10^{-5}	2.0×10^{-4}
2	B	5.5×10^{-4}	4.0×10^{-4}
AVERAGE for 2	A & B	3.0×10^{-4}	3.0×10^{-4}

Pointing error simulations - AGC performance

In a free-space optical system there can be signal amplitude fluctuations due to pointing errors and platform jitter. An automatic gain control (AGC) circuit in the receiver compensates for these fluctuations, providing the clock and data recovery circuits with a nearly constant amplitude signal. Hi-LITE's AGC was designed to handle 35 dB of dynamic range at up to 1000 Hz rate. The ASTE simulates the pointing errors with computer controlled variable attenuators. Amplitudes ranges and frequencies can be chosen by the experimenter.

Most of the BER testing with the ASTE varied the E_b/N_o by changing the amount of noise added to the signal. In this manner the overall received power changed only a couple dB as the E_b/N_o varied several dB. These tests do very little to exercise the AGC circuits, but instead measure the performance of other parts of the receiver.

In order to exercise the AGC circuits fully, signal attenuators in the ASTE are varied while the noise attenuators are held fixed. BER performance results of a test for one ASTE noise attenuator setting are in Figure 12. Also shown in Figure 12 are results from a test with added noise variation, (the same test as in Figure 5). Respective total (signal and added noise) rf power variations for these two tests are shown in Figure 13. Note the small rf power change for the "noise variation" test relative to the change for the "signal variation" test, showing that the "signal variation" tests exercise the AGC more. The E_b/N_o and rf power curves also indicate that, even with the AGC circuit, the receiver is sensitive to input power. Therefore the receiver does have an optimum input power operating level, which was found experimentally by varying the added noise for a range of fixed signal attenuator settings. The "noise variation" test results shown in Figures 12 and 13 center around the optimum input rf power level of about -18.2 dBm. The ASTE signal attenuator was fixed at 9 dB for this test.

Although the AGC circuits keep the received QPPM signal amplitude constant for a varying input, they cannot maintain a constant E_b/N_o because the gain control does not distinguish between signal and noise. For example, if the signal gets weaker because of a pointing error the AGC will increase its amplification. But this also amplifies the relatively constant background noise, so the E_b/N_o decreases slightly. Nonetheless, without the AGC the receiver's performance would suffer, and synchronization loss would become a significant problem.

One limitation of the AGC circuits with regard to background noise can be seen in the "signal variation" curves of Figures 12 and 13. In this test the added noise power was relatively high so that the signal power needed to be high as well, raising the total rf power to the receiver much above the optimum -18.2 dBm. With this relatively high input power, the receiver's limiter upstream of the AGC is activated. Thus, some signal quality is lost for the data detection circuits downstream, as the BER versus E_b/N_o curves of Figure 12 indicate. "Signal variation" tests at lower added noise levels, corresponding to lower rf power

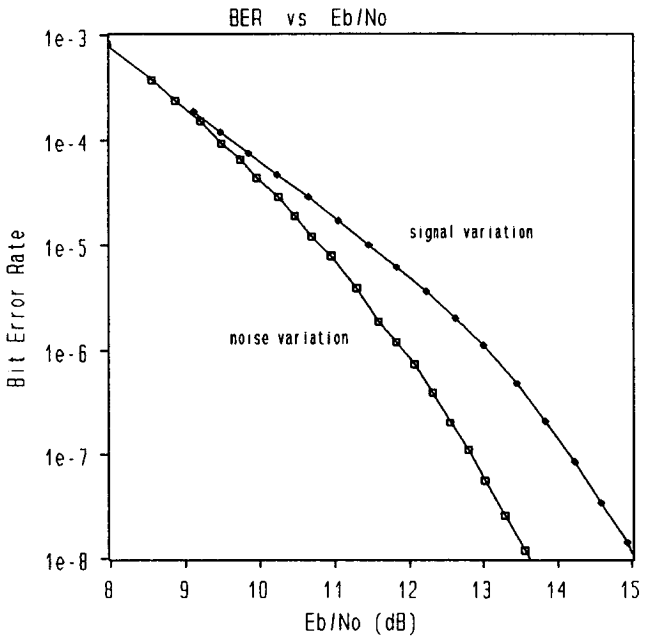

Figure 12: Exercising the AGC (ASTE signal variation), optimal AGC performance (ASTE noise variation)

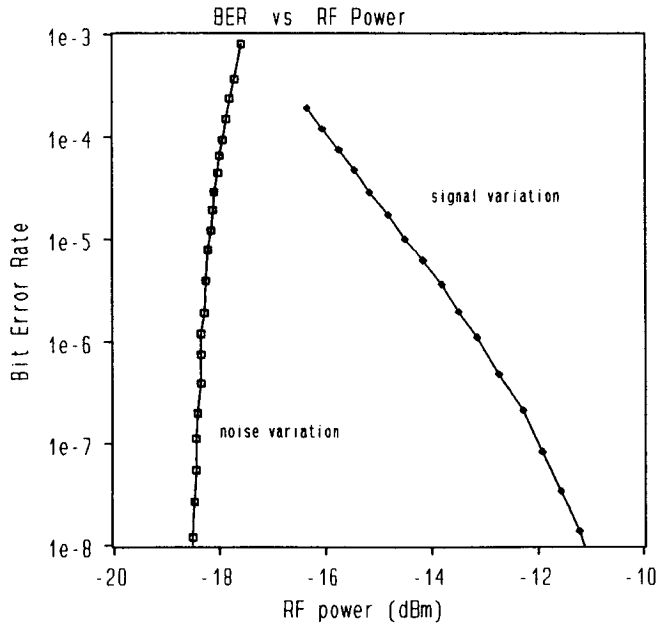

Figure 13: Total received rf power variations for tests of Figure 12.

levels (<-18 dBm), brought BER versus E_b/N_o performance down to the optimal, similar to the "noise variation" tests. In "signal variation" tests with extremely low relative added noise levels the performance departs from optimal again as the total rf power into the receiver is reduced. The total rf power reduction is a result of the signal variation range being reduced commensurate with the added noise range to produce the needed E_b/N_o.

Dynamic sinusoidal variation of the ASTE signal attenuators creates amplitude jitter, simulating pointing errors in a space-borne system. Noise is then added to change the average E_b/N_o. Tests were done with amplitude variations ranging from 2 to 14 dB at 1, 10, 100, and 1000 Hz rates. The frequency of the variation had no measurable effect. However, the BER performance degraded with increasing amplitude range, as displayed in Figure 14. This degradation is to be expected since the BER vs E_b/N_o function is nonlinear. Attenuating the signal more (lower E_b/N_o) during one half of the sinusoidal variation adds more errors than attenuating the signal less (higher E_b/N_o) reduces errors during the other half of the sinusoidal variation. All tests were done with the signal attenuator centered at 9 dB, the optimum setting. So, for example, an amplitude variation range setting of 10 dB sinusoidally varies the signal attenuator between 4 and 14 dB.

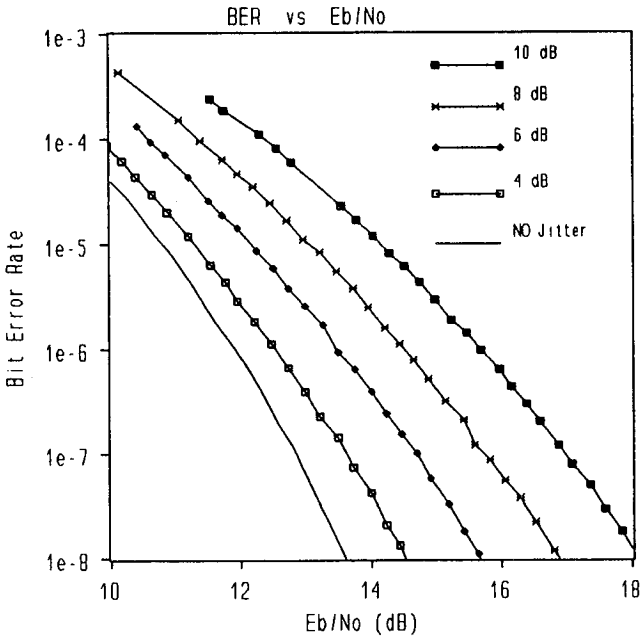

Figure 14: Performance with varying degrees of amplitude jitter at 1000 Hz, simulating pointing errors.

Doppler shift simulations

As in microwave systems, a free-space optical communications system must accommodate Doppler shift effects. For testing, a simple way to simulate Doppler shift on the QPPM data stream is to speed up or slow down the transmit rate. In the Hi-LITE system the transmitter uses a VCXO (voltage controlled crystal oscillator) as its clock source. The 386sx computer can vary the VCXO frequency +/-15 kHz from its center frequency of 650 MHz at a rate up to 1000 Hz/sec, providing a realistic frequency shift simulation capability for a LEO-GEO link, and a frequency shift change rate two orders of magnitude greater than a LEO-GEO link would undergo. Testing revealed no measurable BER performance degradation due to any amount of Doppler shift simulated. Note that this testing only shifts the frequency of the QPPM data rate, not the optical carrier. However, the laser wavelength shift for a LEO-GEO link is in the +/-0.02 nm range, well within the tolerance of the optical components of the system.

Timing skew

Skew in time between the two 325 Mbps modem channels is critical since clock and symbol timing recovery is done from only one channel. Receiver timing alignment between channels was optimized in 50 ps increments using passive delay modules and 1 cm (50ps) SMA connector barrels to change interconnect cable lengths. 50 ps represents about 3% of a slot clock period, and skewing the channels by that amount measurably degrades performance. Quantitative measurements on degradation were not done, other than observing the BER while trimming cable lengths.

Laser performance effects

The Spectra Diodes Labs 150 mW GaAlAs laser has a 500 MHz electrical bandwidth specification, while ideally at least 650 MHz is required.[3] Figure 15 shows scope photographs of the received QPPM waveform, where the long fall time of the pulses can be seen extending into the next 1.5 ns slot. The APD and pre-amplifier are not the cause since their electrical bandwidths are greater, 1.7 GHz and 700 MHz respectively. The long fall time is an obvious source of performance degradation because it increases intersymbol interference. Figure 16 shows the BER versus received photons per bit (in dB) system performance degradation from theoretical optimum, due mainly to the laser bandwidth effects. This curve was presented in reference (3) with an error. It has been corrected here, resulting in a 0.6 dB performance improvement.

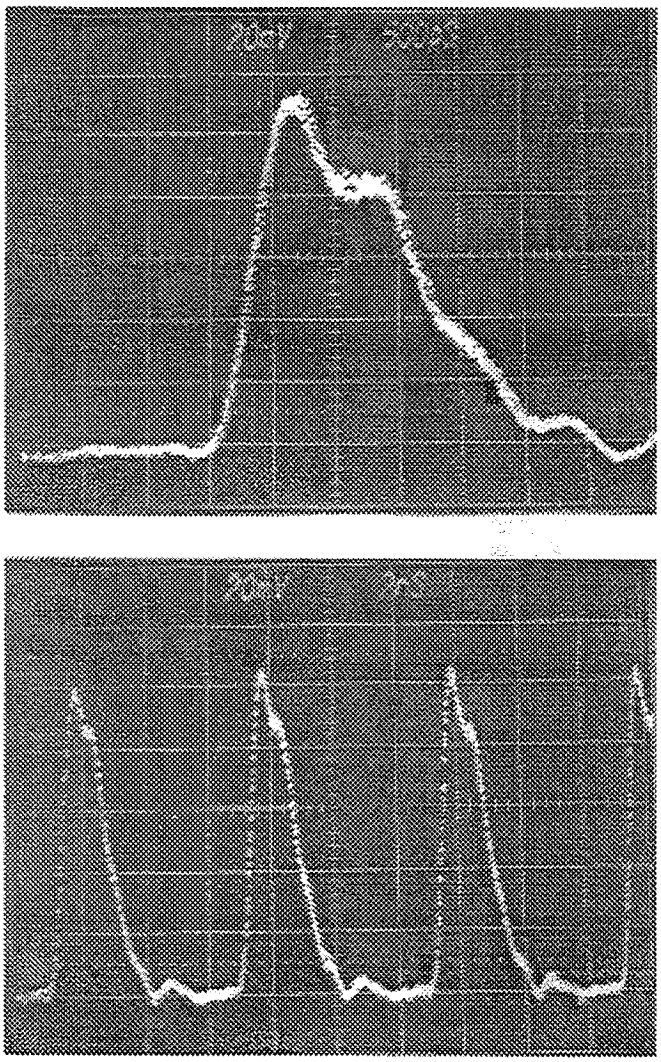

Figure 15: Received QPPM pulses showing laser long fall time, increasing intersymbol interference. Top is a single QPPM pulse, bottom is several QPPM symbols.

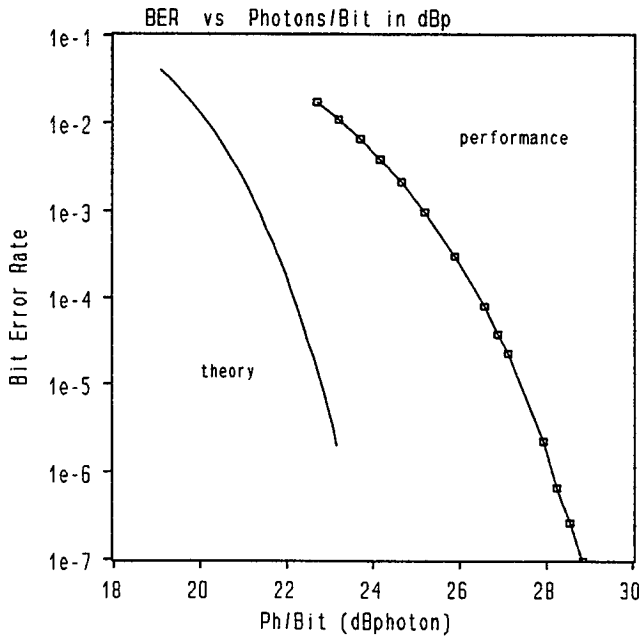

Figure 16: BER performance with OSTE as compared to theoretical optimum. (dBp = relative to one photon)

Statistics of errors

Some statistics are available from the BER test set. A BER measurement is divided into intervals, and the number of errors in each interval is recorded. From this data the number of error free intervals(EFI) is computed as a percentage of the total number of intervals in a measurement. This information indicates to some degree how errors occur, which can help determine the source of errors. The percentage of EFI for tests where errors occur in bursts will be higher than for tests where errors are more evenly distributed. The validity of the EFI measurements depends upon the length in time of the interval relative to the data rate. The more data received in a given interval, the lower the value of EFI, everything else held constant. An interval of 0.01 seconds is the smallest of which the BER test set is capable, so in one interval 3.25 Megabits are received. Needless to say, this is not a good resolution for analysis of Hi-LITE errors.

In performing EFI measurements, the BER receiver can operate in one of two modes: synchronous or asynchronous. Measurement intervals in the synchronous mode of operation are aligned with the errors, while in the asynchronous mode they are not.

A few EFI measurements were taken using the OSTE and ASTE to investigate possible differences in the way errors are created in each of the links. Measurements were done in synchronous and asynchronous modes with interval lengths of 0.01 seconds. Results for the OSTE link are in Figure 17. There was no measurable difference between the two links, but this is not too surprising given the coarse interval resolution. The figure does show a slight difference for the two measurement modes, however. For the same BER or total number of errors there are more EFIs in the synchronous mode measurements than in the asynchronous. This seems to indicate the errors occur in bursts, at least relative to interval period. The bursts might be related to errors occurring at the same points in the PRBS pattern. (A PRBS pattern 2^{23}-1 bits in length takes 0.026 seconds to be

sent through Hi-LITE, which is about two and a half measurement intervals.) This is not unexpected since there is a sensitivity to data pattern length, discussed previously.

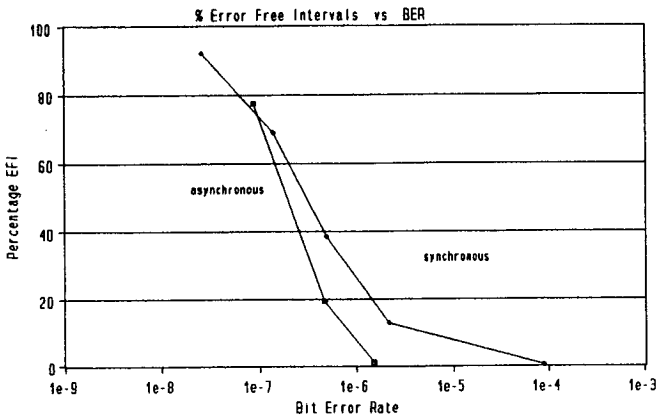

Figure 17: Error free interval BER statistics for OSTE tests, comparison of asynchronous and synchronous measurement modes.

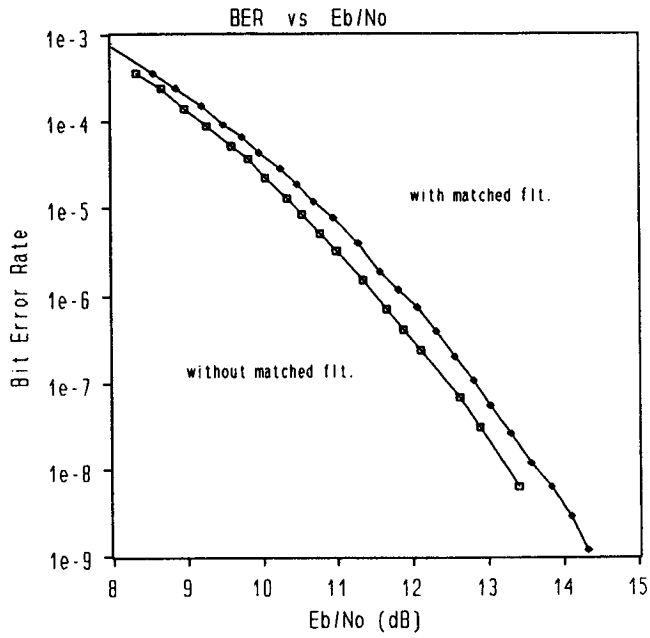

Figure 18: Performance with and without receiver matched filter.

Filtering modifications - matched filter

The receiver was designed with a low-pass Bessel filter to perform the matched filtering[3]. Testing revealed performance was improved slightly without the filter, as shown in Figure 18. A possible explanation of this unexpected result is that the overall receiver is closer to a matched filter without the low-pass Bessel filter than with this filter. Upstream components are, in fact, already doing some low-pass filtering. In parallel is the possibility that, because the filter is part of the AGC feedback loop, the AGC operating point is shifted when the low-pass Bessel filter is removed. The ASTE attenuators have only a 1 dB resolution, so this operating point shift may optimize the AGC within an ASTE resolution increment.

Slot clock recovery enhancements

Slot clock recovery, as discussed earlier in the "Effects of Data Type" section, has a major effect on receiver performance. The commercial clock and data recovery module, used only for clock recovery in Hi-LITE, was made by Broadband Communications Products (BCP). Unfortunately, it was designed for fiber guided applications where the signal-to-noise ratios are generally larger (>20 dB) than those at which the rest of the Hi-LITE receiver can operate. To improve performance at lower signal-to-noise ratios, a few hardware enhancements were made.

First, a pulse doubler circuit was designed and built to condition the received QPPM signal more appropriately for the BCP module. Since the BCP module was designed for Non-Return-to-Zero 50% duty cycle data and not QPPM, a pulse doubler circuit helps by converting each QPPM pulse into two pulses. Figure 19 shows the schematic and timing diagrams for the pulse doubler circuit. Although a spectrum analyzer indicated the circuit creates about 3 dB more spectral energy at 650 MHz, there was little improvement in performance with this enhancement alone.

More improvement in slot clock recovery performance was achieved by cascading two BCP modules together, with the

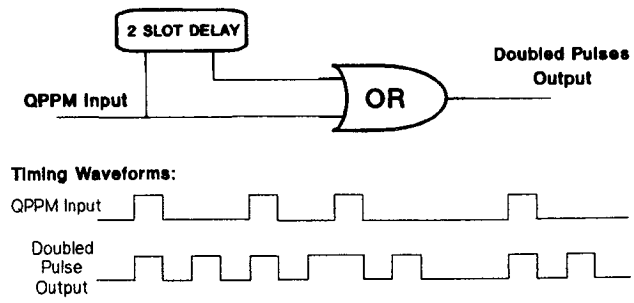

Figure 19: Pulse doubler circuit for slot clock recovery enhancement.

threshold recovered data of the first going to the input of the second. In this configuration the second BCP receives a better S/N ratio signal than the first BCP, so the second BCP's recovered clock is more stable. The cascading was then taken to a third level with a Hewlett-Packard clock and data recovery integrated circuit, the HDMP-2501. Its stand-alone performance is about the same as the BCP module.

Finally, the best performing configuration was found to be cascading the two BCP modules with the pulse doubler circuit and the HDMP-2501, as diagramed in Figure 20. BER performance curves for this and the simpler dual BCP

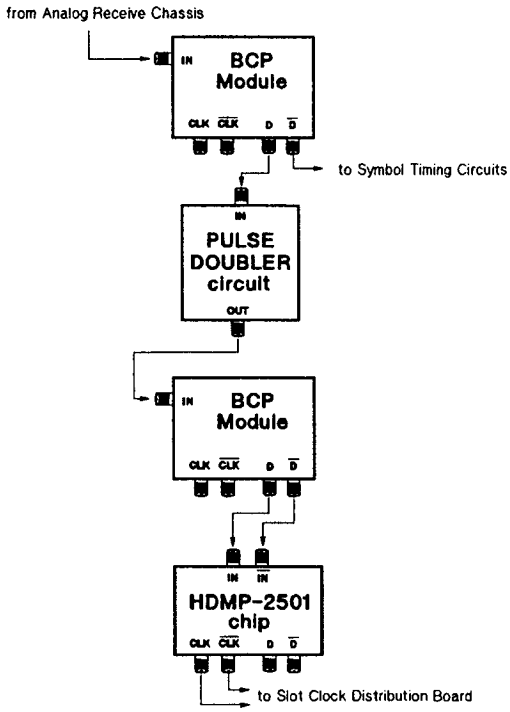

Figure 20: Slot clock recovery enhancement configuration.

configuration are shown in Figure 21. For comparison the figure also shows the performance with the transmit clock fed directly (hardwired) to the receiver. Notice the final and best performing configuration is only 0.2 dB away from the hardwired performance, where there is no clock recovery degradation. All testing reported in this paper, unless otherwise noted, used the slot clock recovery configuration of Figure 20, so that only 0.2 dB of performance degradation was in slot clock recovery.

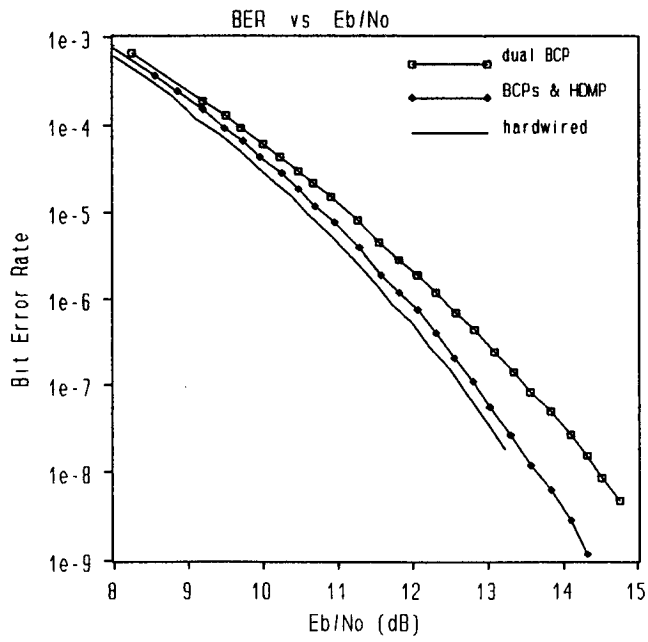

Figure 21: Performance of different slot clock recovery configurations.

Conclusions

An ASIC has been designed (but not yet implemented) that should eliminate some of the prototype's shortfalls.[1] The receiver's sensitivity to channel timing skew would be eliminated with the ASIC's dual clock recovery design, independent for each channel. Also, the symbol timing circuit performance would be improved with the much tighter timing tolerances within the chip as compared to those on several interconnected circuit boards. The slot clock recovery circuit would remain external to the ASIC with its performance still critical to the receiver's performance. A slot clock recovery circuit with a narrower operational bandwidth, and thus a more stable clock, is needed to replace the impractical multi-module configuration used for the prototype. This is not an unreasonable design for an integrated circuit.

Another potential improvement not currently designed into the ASIC is to use maximum likelihood detection for the symbol timing recovery. Using threshold detection for symbol timing makes its performance inferior to the data detection performance, theoretically by 3 dB for QPPM. Maximum likelihood detection for both the data recovery and symbol timing recovery might allow operation at lower

E_b/N_o and without the need for disabling the symbol timing recovery circuits, as is now necessary.

Although there were a few implementation losses, the three operational modes of the modem were tested successfully. Data throughput at 650 Mbps, real-time high quality video data transmission, and BER measurement capability of video or non-PRBS data was demonstrated. In addition, the Hi-LITE prototype modem has proven to operate as designed under various simulated free-space link conditions. The AGC portion of the receiver allows continued operation during pointing errors or platform jitter, and the clock and data recovery circuits can easily track the Doppler frequency shift. Hi-LITE has demonstrated the needed technologies for a high-speed laser communication modem.

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1
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13. ABSTRACT ***(Maximum 200 words)***

The testing and performance of a prototype modem developed at NASA Lewis Research Center for high-speed free-space direct detection optical communications is described. The testing was performed under laboratory conditions using computer control with specially developed test equipment that simulates free-space link conditions. The modem employs quaternary pulse position modulation (QPPM) at 325 Megabits per second (Mbps) on two optical channels, which are multiplexed to transmit a single 650 Mbps data stream. The measured results indicate that the receiver's automatic gain control (AGC), phased-locked-loop slot clock recovery, digital symbol clock recovery, matched filtering, and maximum likelihood data recovery circuits were found to have only 1.5 dB combined implementation loss during bit-error-rate (BER) performance measurements. Pseudo random bit sequences and real-time high quality video sources were used to supply 650 Mbps and 325 Mbps data streams to the modem. Additional testing revealed that Doppler frequency shifting can be easily tracked by the receiver, that simulated pointing errors are readily compensated for by the AGC circuits, and that channel timing skew affects the BER performance in an expected manner. Overall, the needed technologies for a high-speed laser communications modem were demonstrated.

14. SUBJECT TERMS

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