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Report on
**Technical Guidance for the Development of a
Solid State Image Sensor for
Human Low Vision Image Warping**

T-2901T

submitted to
**NASA Lyndon B. Johnson Space Center
Houston, TX 77058**

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Jan Van der Spiegel

October 1994

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GUIDANCE FOR THE DEVELOPMENT OF A
SOLID STATE IMAGE SENSOR FOR HUMAN
LOW VISION IMAGE WARPING Final
Report (Van der Spiegel) 43 p

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1. Summary and Overview

This report surveys different technologies and approaches to realize sensors for image warping. The goal is to study the feasibility, technical aspects and limitations of making an electronic camera with special geometries which implements certain transformations for image warping. This work was inspired by the research done by Dr. Juday at NASA Johnson Space Center on image warping.

The study has looked into different solid-state technologies to fabricate image sensors. It is found that among the available technologies, CMOS is preferred over CCD technology. CMOS provides more flexibility to design different functions into the sensor, is more widely available and is a lower cost solution. By using an architecture with row and column decoders one has the added flexibility of addressing the pixels at random, or read out only part of the image.

Several kind of image pixels have been investigated, ranging from simple CCD cells, and photodiodes to active pixels. An interesting possibility is to use a parasitic bipolar transistor together with a MOS transistor in weak inversion to obtain a large dynamic range. This is made possible through the logarithmic compression offered by the MOS transistor in weak inversion. This allows the sensor to be used under a wide range of illuminating conditions, as encountered in real life situations. The disadvantage of such a pixel is a reduced contrast, fill factor, sensitivity and increased noise and size.

The minimum dimension of a pixel depends on the technology used (minimum feature size) and the complexity of the pixel. In general, the more functionality one builds into the pixel the larger the size will be. A typical pixel which consists of a photodetector with an addressing switch has a size of about $18\mu\text{m} \times 18\mu\text{m}$ in a $2\mu\text{m}$ technology. The fill factor is about 25%. These dimensions can be considerably reduced by going to a more advanced technology. A $1.2\mu\text{m}$ and even $0.8\mu\text{m}$ CMOS technology is widely available at moderate cost. The minimum pixel size in a $0.8\mu\text{m}$ technology will be about $9\mu\text{m} \times 9\mu\text{m}$ and will double if one includes the logarithmic compression circuit.

Several manufacturers were contacted: ORBIT, MOSISTM and IMEC. IMEC is the only one which has a complete CCD technology. These manufacturers were chosen because they allow prototyping of small volumes at a relatively low cost. ORBIT delivers 36 samples of a 9.6×9.6 square mm $1.2\mu\text{m}$ CMOS chip for \$20K. All manufacturers draw the geometries on a grid of $0.1\mu\text{m}$ and allow to draw lines of 0, 90, and 45° orientation. Lines of other orientations will be approximated to the nearest grid point.

2. Introduction

People suffering from field defects in the foveal part of the retina could benefit from low-vision aids which remap the image on the functional part of the retina. Dr. Juday and his group at NASA Johnson Space Center have done innovative work on the mathematical modeling of conformal mappings which could be used as guidelines to warp the image around the scotoma¹. In addition, Juday's group developed an image remapper that can implement any of these transformations and can serve as a test vehicle to be used with patients suffering from scotomas². Tests on such patients are in progress at the University of Houston under the guidance of Dr. D. Loshin. These preliminary tests seem to indicate that an improvement in reading speed has been observed when warped images are presented to patients as compared to unmapped ones¹.

The question arises whether special cameras can be designed and fabricated which realize the required transformation in real time. This would result in a small and light weight low-vision aid for visually impaired people. The purpose of the study whose results are reported here is to look into the feasibility and provide technical feedback of making such a dedicated sensor with current integrated circuit technologies. Also, the goal is to provide information about possible geometries, such as minimum and maximum pixel size, shapes of the pixels, fill factor and other limitations of current technology. However, the goal of this study was not to design such a camera, as this will to a large extent depend on the findings of the clinical studies. These studies which are still in progress will indicate what transformations and geometries are optimal.

In order to address the above items, the following topics have been studied and reported on:

1. Overview imaging technologies
2. Commercially available technologies, layout rules and prices
3. Pixel geometries and sizes
4. State-of-the-art in image sensors
5. Specific issues related to sensors for image warping.

3. Imaging Technologies - an Overview

Solid-State image sensors can be fabricated in a variety of technologies of which the following are most popular: Charge-Coupled Devices (CCD), Complementary Metal Oxide Semiconductor (CMOS) technology, and a combination of CCD and CMOS. All of these approaches are based on the well known planar silicon integrated circuit technology. The difference between them is the presence of particular layers and implants that allow the fabrication of specialized structures, such as CCDs, which require two or three polysilicon layers in addition to a buried channel implant. A CMOS process generally does not support the fabrication of CCD structures or vice versa. However, there are some processes available that support both CCD and CMOS devices. These will be discussed later on.

In the following a brief discussion of the basics of CCD and CMOS technologies will be given. Emphasis will be put on the advantages and disadvantages of each approach, as well as its limitations. This will help in understanding which technology to choose.

a. CCD technology

Charge-Coupled Devices are basically tightly coupled metal-oxide-semiconductor (MOS) capacitors³. Fig. 1 shows such a structure that consists of a p-type semiconductor substrate. When a positive (in case of a p-type substrate; negative for n-type) voltage (typically 5-10V) is applied to the gate of such a capacitor, the semiconductor substrate near the surface will be depleted of its majority carriers. Minority carriers (electrons in case of p-type substrate) can now be stored underneath the gate oxide at the surface of the semiconductor where the potential is maximum. These electrons can be supplied electrically or generated optically. In the latter case, one assumes that the top electrode is transparent. The amount of stored charges will be proportional with the light intensity. However, one has to realize that this structure is in non-equilibrium. In order to restore equilibrium, minority carriers will also be thermally generated and collected at the semiconductor surface along with the optically generated "information" charge. Fortunately, this generation process is relatively slow (several milliseconds). If one pulses the gate voltage regularly (dynamic operation), one can minimize the amount of thermally generated charges which constitute the dark current.

If one applies a sequence of pulses on neighboring gates, the charges can be transported from one gate to another. The gates can be driven by three- or four-phase clocks.

Thus, a CCD is basically a dynamic analog shift register. If one uses the CCD as an imager, the top electrode must be transparent (a thin poly-silicon layer e.g.) so that the incident photons can penetrate the silicon substrate. The minority carriers of the photo-generated charges will flow towards the surface and collected under the gates. Afterwards, the charges are read out quickly in a serial-parallel fashion by clocking the gates appropriately. There are several architectures possible of which the frame transfer and the interline transfer layouts are most popular (see section 5a).

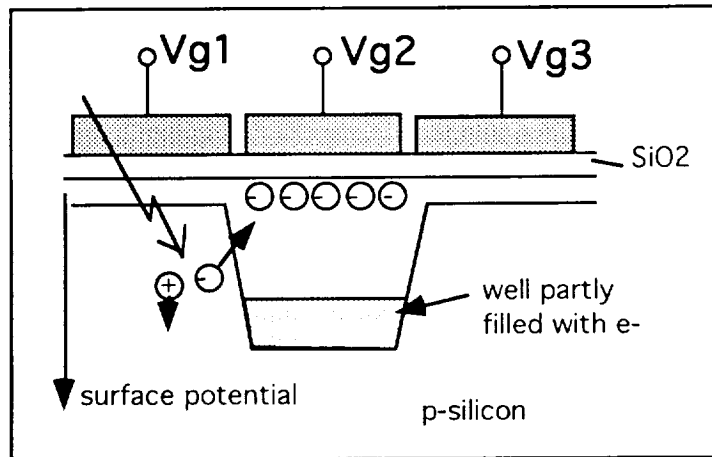


Figure 1: Schematic cross section of a 3 phase CCD cell.

In order to improve the transfer efficiency, most CCDs employ buried channels. This is accomplished by using an ion implantation in the channel which causes the maximum potential in the substrate to move away from the surface. As a result, the minority carriers will not be in contact with the surface, which is advantageous for a better transfer efficiency. Also, CCD processes have additional layers (ion implanted) to prevent blooming (overflow of charges to the neighboring cells) and improve the image quality. This results in quite sophisticated processes.

Advantages of CCD technology can be summarized as follows:

- small pixel size is possible (example: $6\mu\text{m} \times 6\mu\text{m}$)
- good fill factors
- good quantum efficiency
- large formats, large arrays (example for HDTV; up to 4K x 4K illustrated)
- good signal to noise ratio (example: 80 dB)

- one common output amplifier which eliminate fixed pattern noise.
- combination of sensor with charge domain signal processing elements for realizing on-chip vision tasks
- image transformation can be implemented by the geometry of the pixels

Disadvantages are:

- complex and expensive technology
- not widely available processes
- requires almost perfect transfer efficiency
- radiation softness
- no random addressing of pixels: serial or serial/parallel read out.
- less flexibility to realize functions in the charge domain
- complex driving circuits that can consume a considerable amount of power: CV^2f
- some processes require voltage levels for clocks larger than 5V mandating clock amplifiers; the shape of the clocks are critical for good transfer efficiency.

b. CMOS technology

Complementary Metal Oxide Semiconductor (CMOS) technology is by far the most used technology to fabricate microelectronic circuits⁴. It consists of both NMOS and PMOS transistors by making use of a well implantation. Fig. 2 shows an example of a n-well CMOS process. The transistors are similar to the MOS structures found in CCDs except that it has a diode on both sides of the MOS capacitor. The voltage applied to the gate controls the amount of minority charges underneath the oxide at the semiconductor interface (channel) and thus modulates the resistance of the channel. In its simplest form, a MOS transistor can be regarded as a voltage controlled resistor or current source, depending on the mode of operation. For digital applications, one is only interested in two states, i.e. when the resistance is very large, corresponding to an open circuit (transistor is off) or when the resistance is small (transistor is on). The presence of both NMOS and PMOS transistors allows us to make logic gates that consume no DC power (except for a small amount due to the leakage current). This is one of the most important advantages of CMOS for use in digital applications. However, CMOS is equally attractive for the fabrication of analog circuits. The presence of both N and P type transistors gives a lot of flexibility and allows you to make high gain amplifier stages.

Although CMOS has been developed for digital and analog integrated circuits, it is possible to make photosensitive devices. The diodes of the source and drain, or of the well to substrate, can be used as photodetectors. In addition, the source-well-substrate structure allows us to make a (parasitic) vertical bipolar transistor, as is shown in Fig. 3. The bipolar transistor has an inherent current amplification, typically 100, that makes it more suitable

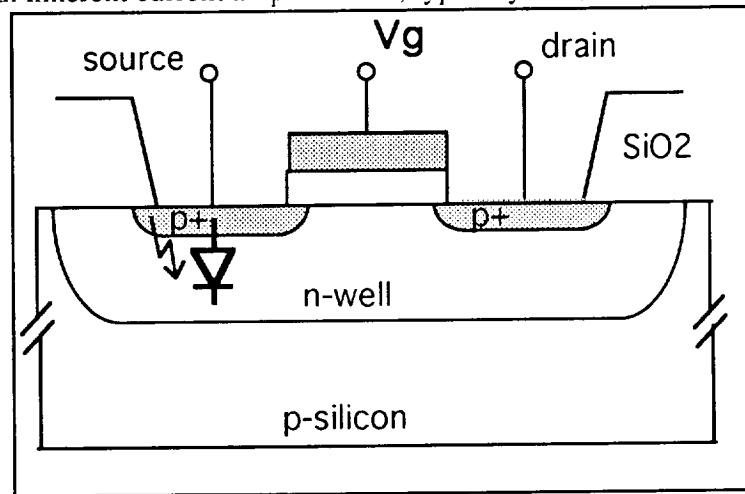


Figure 2: A schematic cross section of a PMOS transistor in a p-well CMOS process

for low light level applications. One can convert the photo generated current into a voltage by feeding the current into a diode-connected transistor, as is shown in Fig. 3. The advantage of using a transistor over a resistor is that one can accomplish a nonlinear compression. For instance, if the diode-connected transistor operates in the weak inversion, the voltage will be a logarithmic function of the current and thus the incident light intensity. As a result of the logarithmic compression, one can measure the light intensity over typically 6 orders of magnitude, as may be encountered in real-world scenes. One should however keep in mind that the price to pay for this large range, is the reduced image contrast. The problem of reduced incremental sensitivity at any light level can be overcome by incorporating adaptation, similar to a local automatic gain control mechanism⁵. The above example illustrates the flexibility and some of the advantages of CMOS, i.e. one can work in both the current and voltage domain and make use of the transistor to modify or condition the signals. Examples of functions are: compression, amplification, filtering, inversion, multiplication, addition and subtraction.

The photo elements in a CMOS process can be used in two modes: photo conductive or integrative mode. The example of Fig. 3 corresponds to the photoconductive mode,

where one has a continuous current whose intensity varies with the light intensity. In the integrative mode one integrates the photo current on a capacitor (usually the intrinsic capacitor of the photo diode) for a certain time. This results in a charge packet on the capacitor or a voltage over the capacitor, as illustrated in Fig. 4. After a fixed time (called integrated time), the voltage or charge is sampled for further processing or read-out purposes. The latter method is basically what is done in a CCD image sensor. The characteristics of each mode of operation are summarized below:

Continuous mode:

- asynchronous operation
- nonlinear compression possible
- continuous time operation (no sampling required): less noise due to lack of clocks
- suitable for continuous time signal processing
- fewer control signals
- higher fixed pattern noise due to pixel to pixel variations

Integrative mode:

- synchronous operation, clock required
- signal integrated on a capacitor during integration time
- more sensitive (by integrating long times)

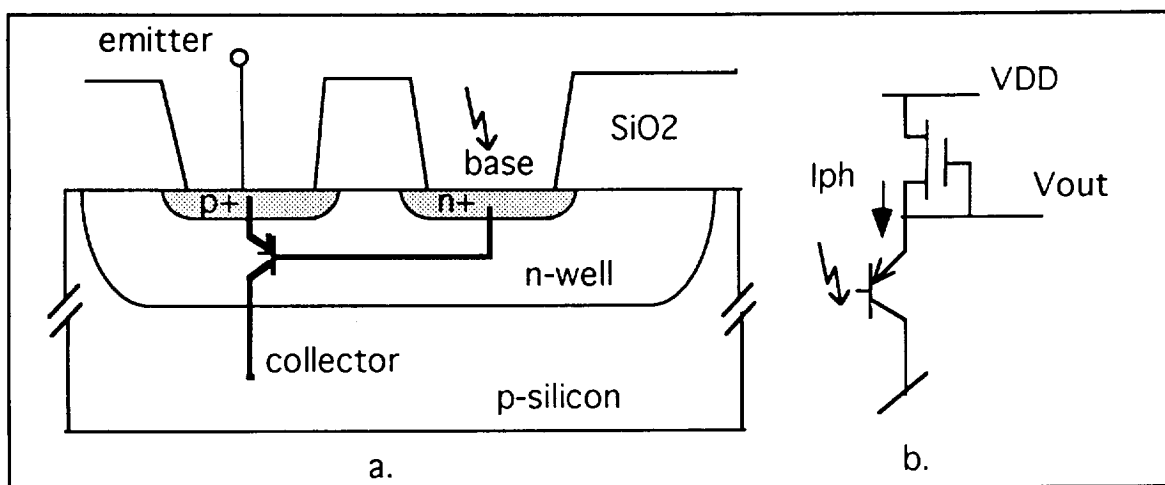


Figure 3: a. Parasitic PNP bipolar transistor in a pwell CMOS process and b. Phototransistor with MOS load.

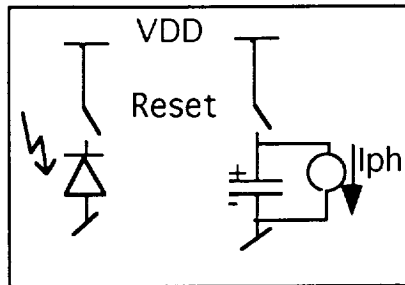


Figure 4: Photodiode used in the integrative mode

A CMOS based imager can be randomly addressed by using X-Y address decoders and switches to address the individual pixels. This can be an advantage over CCD imagers which allow only serial output formats. An example of such an architecture will be shown in section 5b. On the other hand the random switching can introduce noise, and cause non-uniformities. The fill factor is usually smaller than in CCDs because one needs transistors to address the photo detectors. In particular, if one incorporates additional transistors at the pixel site, such as to obtain amplification, contrast detection, etc. (often called active pixels) the fill factor may be as low as 10%. In addition, the pixel size increases considerably and thus reducing the resolution of the image sensor. A summary of the main characteristics of CMOS based imagers is given below.

Advantages of CMOS-based imagers:

- relatively simple, aggressively scaled and widely available technology
- less expensive than CCD technology
- random addressing of pixels possible; pan or zoom on a selected number of pixels
- active pixels possible (incorporating processing functions: compression, amplification)
- smart sensors: combination of sensor with signal processing functions on the focal plane
- simple driving circuits; can be easily incorporated on-chip; clocks and control signals are at the 5V levels
- allows camera system on a chip.

Disadvantages of CMOS-based imagers:

- larger noise levels than CCDs in particular fixed pattern noise
- large capacitance of the read-out line
- non-uniformity
- cross talk between pixels
- smaller fill factor
- larger area per pixel, particularly for active pixels

c. CCD/CMOS technology

Previous discussions indicated that CCD technology is the leading choice for the fabrication of high quality, high resolution image sensors. On the other hand, CMOS is the technology of choice for implementing vision chips that incorporate image processing functions such as amplification of pixel signals, edge detection, filtering, orientation detection, motion detection, in addition to the photodetectors,.

The continued demand placed on the CCD imager to realize higher performance with reduced pixel size, increased sensitivity and chip size reduction requires more complicated technologies. As a result, CCD and CMOS technologies are gradually converging. By incorporating a couple of additional layers it is possible to fabricate both CCD and CMOS devices on the same chip. This allows for combining the best of both technologies. One can now integrate the photo sensitive part (CCD) with the logic and clock drivers (CMOS) on the same chip. One can also combine charge domain and current/voltage domain processing circuits in order to make smart image sensors with better performance or more functions than what is possible in a CCD or CMOS process only.

Major manufacturers have or are developing CCD/CMOS technologies. As mentioned above, these technologies are not usually available for outside customers. However, a few companies are making CCD/CMOS processes available. One such company, Orbit Semiconductor, Inc. of Sunnyvale, CA, is offering through their "Foresight" service, a 2 μm n-well CMOS process with two polysilicon layers. Both layers can be used to make transistors (in contrast to most two layer processes which allow the second poly-layer to be used only as an electrode for capacitors and not as the gate of a transistor). This process also provides an option for a buried channel implant (at an additional cost). This process is basically a CMOS process that is modified to make CCDs. This implies that it does not provide all the features an optimized CCD process has, such as special implants to improve

charge storage, transfer, to reduce blooming, etc. However, it allows one to make CCDs combined with CMOS circuits to make smart sensors. As of this writing Orbit has not offered this process in a 1.2 μm version. In addition, MOSIS[®] (MOS Implementation Service) is also offering the above Orbit process.

Another CCD/CMOS process is made available through IMEC (Interuniversity Micro-Electronics Center in Leuven, Belgium). IMEC recently introduced their 1.25 μm CCD/CMOS process. In contrast to the Orbit's Foresight process, this is a CCD process that incorporates CMOS devices. As a result it is geared more towards the fabrication of CCD imagers with on chip drivers and processing circuits.

d. Other technologies

Imagers with photoconductive overlayer

With the increased demand for higher resolution (HDTV) and performance, the pixel size is continuously shrinking. This poses problems of sensitivity, noise and reduced optical aperture ratio. One way to alleviate these problems is to use a photoconversion overlayer. This layer consists of a photosensitive material on top of a CCD or MOS structure. A typical example of such a layer is amorphous hydrogenated silicon (a-SiH(i)). The main advantage of this structure is that one can increase the photosensitive area to almost 100% which results in high sensitivity and a reduction of aliasing or dead space in the sampling plane. One can also use materials that are sensitive outside the visible region, such as in the infrared to make night vision sensors.

As this approach has clear advantages, the disadvantages are the increased complexity of the technology, high cost and limited availability of commercial processes.

4. Commercially Available CCD and CMOS Processes

Here we will concentrate on the processes that are easily available for outside users: i.e. Orbit's 'Foresight' process, MOSIS and IMEC's CCD/CMOS process. The goal is not to give an exhaustive list of the design rules since this would quickly become too detailed, but also because some of these are proprietary and can be obtained after signing an agreement with the respective companies. We will point out what the critical dimensions are that determine the minimum pixel size as well as the overall sensor geometry. This will help us understand the limitations of the technology. It should be pointed out that there are many

more CCD processes in use in the major CCD manufacturers' laboratories that are often more aggressive than those described here. However, these are generally not available or would be very expensive.

a. Orbit's 2 μm double poly n-well CMOS process with buried layer option

Available processes and prices

Orbit's Foresight Program is a low cost silicon wafer fabrication program that provides fast turn-around runs⁶. The low cost is achieved by putting multiple designs onto a single mask as is done on a mullet-project wafer. The cost of one run (typically \$50-80K) is now divided by the number of different projects on the wafer. The turn-around time is typically 4 to 5 weeks, including packaging, which is considerably faster than with MOSIS. The standard processes supported by Orbit are:

- 1.2 μm double poly double metal CMOS n-well and p-well
- 1.2 μm double poly double metal CMOS with npn transistors in the n-well
- 2 μm double poly double metal CMOS n-well and p-well
- 2 μm double poly double metal with npn transistors in the n-well and buried channel for charge coupled devices.

The prices are very economical as is shown below (effective July 1, 1994)

<u>Name</u>	<u>Die Size(mm)</u>	<u>Project Size</u>	<u>No. of Parts</u>	<u>Price</u>
Tiny	2.4x2.4	fixed 40 pads	12	\$3.5K
Small	4.8x4.8	4.6x4.5	12	\$10K
Medium	7.2x7.2	7.0x6.9	24	\$15K
Large	9.6x9.6	9.4x9.3	36	\$20K

Note: 2 μm buried channel implant option for BCCD: add 25%.

Geometrical design rules

Orbit has its own design rules to take optimal advantage of its processes. However, Foresight's standard processes support also the public domain MOSIS and DOD CMOSN design rules. The DOD CMOSN (scalable 2/1.2 μm) standard cell library with RAM and ROM generators is available from Orbit at a minimal cost.

The following table gives the critical design rules of the 2 μm double poly double metal n-well CMOS process. This process is capable of supporting buried channel CCD and npn bipolar transistors in the n-well. The process requires 13 drawn layers. According to Orbit's support engineering, geometries can be drawn on a 0.1 μm grid. Lines under 45 degrees are possible. This implies that curved geometries will be approximated to the closest 0.1 μm grid point.

TABLE I : Key design rules of the 2 μm ORBIT CMOS process

LAYER	RULE	MICRONS
N-well	width	3.0
	spacing	8.5
Active	width	3.0
	spacing	2.5
	to well	6.5
	N-well overlap N+	0.0
Poly 1	width	2.0
	spacing	2.5
BCCD	width	3.0
	spacing	3.0
Poly 2	width (gate)	2.5
	spacing	3.0
	to poly 2	2.5
Contacts	size	2.0 x 2.0
	spacing	2.0
	overlap active/poly	1.5
Metal 1	width	2.5
	spacing	2.5
	overlap contact	1.0
Via	size	2.0 x 2.0
	spacing	2.5
	overlap metal 1	1.5

Metal 2	width	3.0
	spacing	3.0
	overlap of via	1.5
Pads	size	100x100
	spacing	75

Address and phone number

Orbit Semiconductor, Inc.
 1215 Bordeaux Drive
 Sunnyvale, CA 94089
 (408) 744-1800 phone
 (408) 747-1263 fax

b. MOSIS process

Available processes and prices

MOSIS, which stands for MOS Implementation Service, was established in 1980 by DARPA with the assistance of NSF to provide government contractors and agencies, as well as university classes, access to state-of-the-art IC fabrication facilities at a low cost⁷. For several years, MOSIS services have also become available to commercial users at a slightly higher cost. The MOSIS Service is similar to Orbit's Foresight program, a prototyping service that offers fast turn-around standard cell and full custom VLSI circuit development at a very low cost. MOSIS has developed a methodology that allows the merging of many different projects from various organizations onto a single wafer. Therefore, instead of paying for the cost of mask making, fabrication and packaging for a complete run, MOSIS users only pay for the fraction of the silicon that they use, which can cost as little as \$400. MOSIS has very easy access. All communication can be done over the internet. MOSIS accepts designs submitted in CIF (Caltech Intermediate Format) format over the internet. Packaged chips are mailed to the customers about 10 weeks later.

MOSIS does not have its own fabrication facilities but acts as a silicon broker. It has agreements with several commercial manufacturers to fabricate their multi-project wafers. The turn-around time is somewhat longer than Orbit's, typically 8-10 weeks. As one is not always sure which foundry will fabricate the wafers, it is harder to optimize the design.

The MOSIS layout rules and device parameters are usually a superset that satisfies the rules of the different foundries. As a result, one is not always making optimal use of a particular manufacturer's process. However, MOSIS has recently provided an option for their customers to specify which vendor their design should go. This can result in a considerably longer turn-around time. Among the vendors MOSIS works with are Orbit, HP, and VTI. The HP process is found to be in general a very good process with low defect density.

Wafer fabrication runs are scheduled on a regular basis for 2.0, 1.6, 1.2 and 0.8 micron double metal CMOS/Bulk technologies. A CMOS/Bulk double poly capacitor option for analog design is also available. MOSIS also provides the option to form buried n-channels which allows one to make buried channel CCDs in the double poly 2 μ m n-well CMOS process (low noise analog). An overview of the available processes is given below.

TABLE II: Overview of Current MOSIS Processes

PROCESS NAME	TECHNOLOGY	FABRICATOR
2.0U VLSI	CMOS N-WELL	VLSITECHNOLOGY (CMN20)
2.0U ORBIT	CMOS P-WELL, 2 POLY	ORBIT (CP2)
2.0U ORBIT ANALOG	CMOS N-WELL, 2 POLY (Low Noise Analog; also CCD)	ORBIT (CN2)
1.6 AMI	CMOS N-WELL, 2 POLY (Low Noise Analog)	AMI (ABN)
1.2U HP	CMOS N-WELL (includes linear capacitor option)	HEWLETT-PACKARD (CMOS34)
1.2U ORBIT	CMOS N-WELL, 2 POLY	ORBIT (CN12)
0.8U IBM	CMOS N-WELL	IBM (CMSX 2185)
0.8U HP	CMOS N-WELL	HEWLETT-PACKARD (CMOS26B)
VITESSE HGaAs3	GALLIUM ARSENIDE	VITESSE (HGaAs3)

The prices vary with technology and chip size. Discount prices are available to those universities, government agencies and organizations ordering work that will be charged to a

government contract. The price for the 2 μm CMOS includes packaging. The price for the 1.2 μm CMOS process is calculated per square mm and is equal to \$380 (discount price: 25 parts). The minimum area is 1.94 x 1.94 sq. mm. The cost of packaging is not included in the 1.2 μm technology.

TABLE III: 2.0 MICRON CMOS TECHNOLOGY
(Priced per project, including packaging)

Maximum Project Size	No. Parts	Standard Price	Discount Price	ARPA/NSF Price
2.22 x 2.25 mm (Tiny Chip)	4	\$520	\$480	\$440
4.6 x 6.8 mm	12	\$2,600	\$2,410	\$2,210
6.9 x 6.8 mm	24	\$6,150	\$5,640	\$5,120
7.9 x 9.2 mm	32	\$11,900	\$10,860	\$9,810

Geometrical Design Rules

The design rules are very similar to ORBIT's Foresight design rules.

Address and phone numbers

Contact person: Sam Reynolds
MOSIS Service
USC Information Sciences Inst.
4676 Admiralty Way
Marina del Rey, CA 90292-6695
(310) 822-1511

c. IMEC's 1.25 μm CMOS/CCD Process

IMEC (Interuniversity MicroElectronics Center) is a research center that was set up in 1984 to promote research in the area of microelectronics. It works under contract for private or government agencies and makes their processes available for outside use.

Available processes and prices

IMEC and its predecessor, ESAT have been designing and fabricating CCDs for over 15 years. IMEC has a 1.25 μm CMOS/CCD process on line that allows the fabrication of

both CCD and CMOS circuits on the same chip. The process uses two polysilicon layers. The CCD structures use both poly layers and are realized in a 4 phase structure; the transfer gate is realized by an extension of the poly layer. CMOS transistors are made only of the first poly layer.

The prices vary with die size. The following table gives the prices for unpackaged devices. The prices are in belgian franks. An approximate dollar value is given based on BF35/\$. The prices are for a full custom run, i.e. without sharing it with other customers. If the chip size is smaller than the recticle of 9.6x9.6 mm² and one finds another customer, the price will be reduced.

TABLE IV: Prices of the 1.25 Double poly CCD process of IMEC (exclusive packaging)

DIE SIZE (mm ²)	# of CHIPS	COST IN BF	COST in US\$
1.1 x 1.1	150	650,000	18,600
4.8 x 4.8	150	800,000	22,900
9.6 x 9.6	150	1430,000	40,000

Price for packaging in ceramic package: BF1500 (\$43) per package

Geometrical Design Rules

This process has 17 layers. The key design rules are summarized in Table V below. Similar as for the ORBIT's rule, the masks are written in a cartesian grid of 0.1 μm. If one intends to use angles different from 90 degree, the design rules have to be increased by 0.1 μm. Real circular lines are not possible.

TABLE V: Key Design Rules of the 1.25 μm IMEC CMOS/CCD Process

LAYER	RULE	MICRONS
N-well	width	6.0
	spacing	6.0
Active	width as trans. width	1.2 or 1.5
	spacing	2.4
	to well	3.6-6.0
	N-well overlap N+	1.0

BCCD	width	1.2
	spacing	1.2
	overlap over active	0.9
TG	width	1.2
	spacing	1.2
	overlap active	0.9
Poly 1	width	1.2
	spacing	1.8
Poly 2	width (gate)	1.3
	spacing	2.0
	overlap with poly 1	0.6
Contacts	size	1.5 x 1.5
	spacing	1.5
	overlap active/poly	1.0
Metal 1	width	1.8
	spacing	1.8
	overlap contact	1.0
Via	size	1.8 x 1.8
	spacing	1.8
	overlap metal 1	1.0
Metal 2	width	2.0
	spacing	2.0
	overlap of via	1.0
Pads	size	100x100
	spacing	50

Address and phone number

Mr. Lou Hermans
IMEC vzw
Kapeldreef 75
3001 Leuven, Belgium
32-16-281211 phone
32-16-289400 fax
email: hermans@imec.be

5. Description of different unit cell structures and sizes.

The choice of a unit cell structure is important because it will determine the minimum pixel size, the overall sensor size, the fill factor, flexibility to implement transformations, and simplicity/complexity of driving and control electronics. A brief overview of possible realizations of cells, including photodetector with shift register or addressing transistors, will be given for a CCD and CMOS or combined CCD/CMOS process. Advantages and disadvantages will be given where appropriate. The goal is to provide some guidance with the future choice of a particular structure. The final choice will depend on several factors of which some may not be known at this point. We will discuss three main classes of pixels: CCD based pixels or charge domain pixels; CMOS pixels with a current output or with voltage output. The CCD pixels are synchronous or clocked while the CMOS pixels can be either asynchronous (continuous mode) or synchronous.

a. CCD based pixel (Charge domain)

CCD photo detectors are based on the integration of charge during a defined amount of time (integration time). The higher the intensity of the incident light, the more charge will be collected. Charges are stored in the potential well underneath the MOS gate or in a reverse biased diode. The charge collection and the transfer occurs all in the charge domain. Read out is usually done in a parallel-serial fashion until the charges reach the output diode where a charge to voltage conversion occurs as a result of the capacitance of the output diode. Instead of measuring the output voltage, one can also measure the output current. The latter method is not often used in practice. A schematic block diagram of a CCD imager with interline transfer architecture is shown in Fig. 5. The photodetectors are represented by diodes, but they can be photo gates as well, as will be discussed next. The vertical CCD shift registers are shielded from incident light.

A first type of pixel consists of a polysilicon capacitor isolated from the neighboring pixel by a stopper diffusion and from the shift register by a transfer gate. The transfer gate does not necessarily have to be fabricated from a separate polysilicon layer if one uses proper implantation profiles in the CCD channel. A diode has a better quantum efficiency but suffers more from kTC noise. Fig. 6 shows a cross section and a top view of the cell. A pixel is about $16.5 \mu\text{m} \times 16.5 \mu\text{m}$ in size. These may have to be increased by about 20% to accommodate interconnections, depending on the overall architecture used. Dimensions are indicated for a $2 \mu\text{m}$ technology. In general, these can be scaled for other technologies,

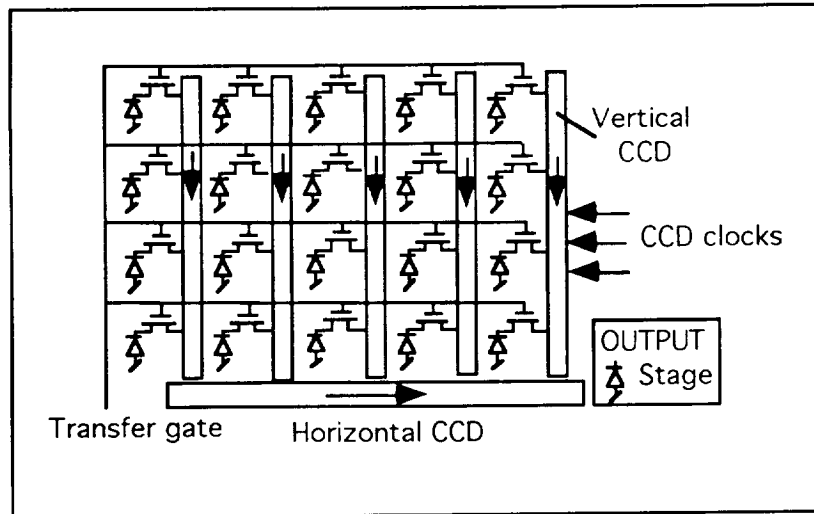


Fig. 5: Schematic architecture of a CCD imager with interline transfer architecture and diodes as photodetectors

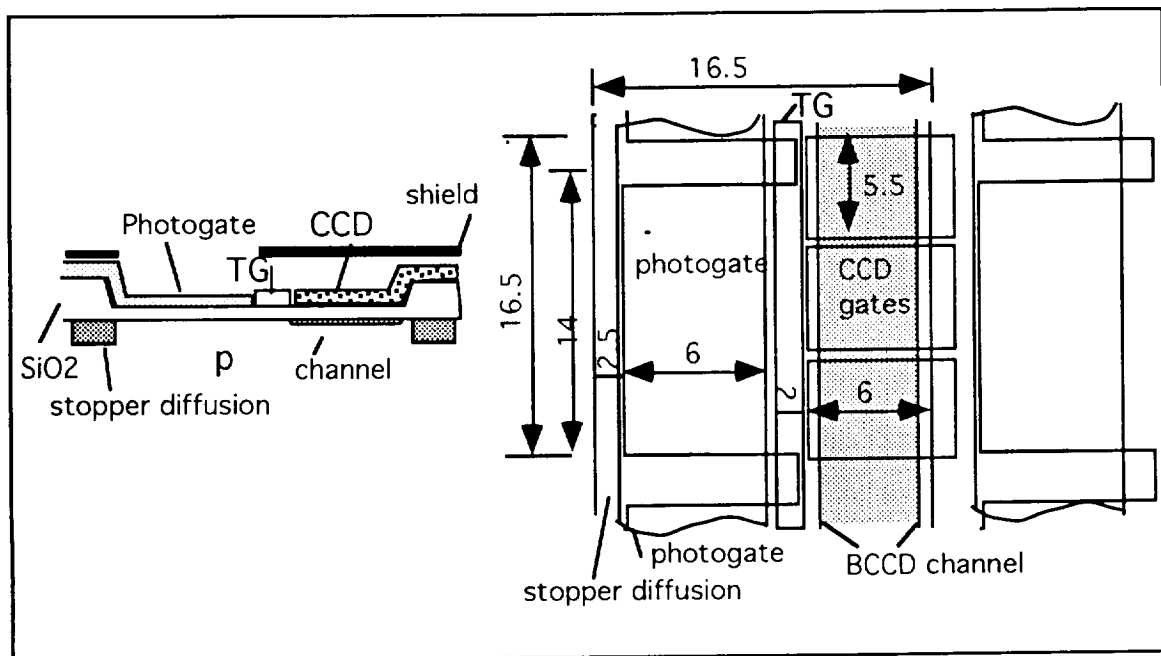


Fig. 6: Schematic cross section and top view of a CCD pixel consisting of a MOS photo gate and CCD shift register. Dimensions are in μm for a $2\mu\text{m}$ technology.

for example, the dimensions for a $1.5\mu\text{m}$ technology are obtained by multiplying the dimensions by 0.75. It should be emphasized that the sizes shown here give only a rough

indication of cell size and that the exact size will be a function of the available technology, the overall architecture and the clocking scheme adapted (3 or 4 phases). The CCD shift register is used to read out the charges. It should be noted that the gates of the CCD shift register are $5.5\ \mu\text{m}$ wide in order to accommodate the MOSIS or ORBIT design rules that require a minimum overlap of poly 2 over poly 1 of $1.5\ \mu\text{m}$ and a minimum spacing between poly 2 layers of $2.5\ \mu\text{m}$. This gives rise to a large CCD cell. This is an example of how a non-optimized technology (such as ORBIT or MOSIS) increases the dimensions of the structure. This structure has a relatively small area and allows an interline transfer architecture. Readout of a current frame is done during integration of the next frame. The disadvantage is the light absorption in the top polysilicon layer. This is particularly severe in the blue part of the spectrum. This problem can be reduced by using very thin poly-silicon layers. However, this is not available in the standard processes to which we have access. This problem can also be eliminated by using a photodiode as the sensitive element, as shown in Fig. 7.

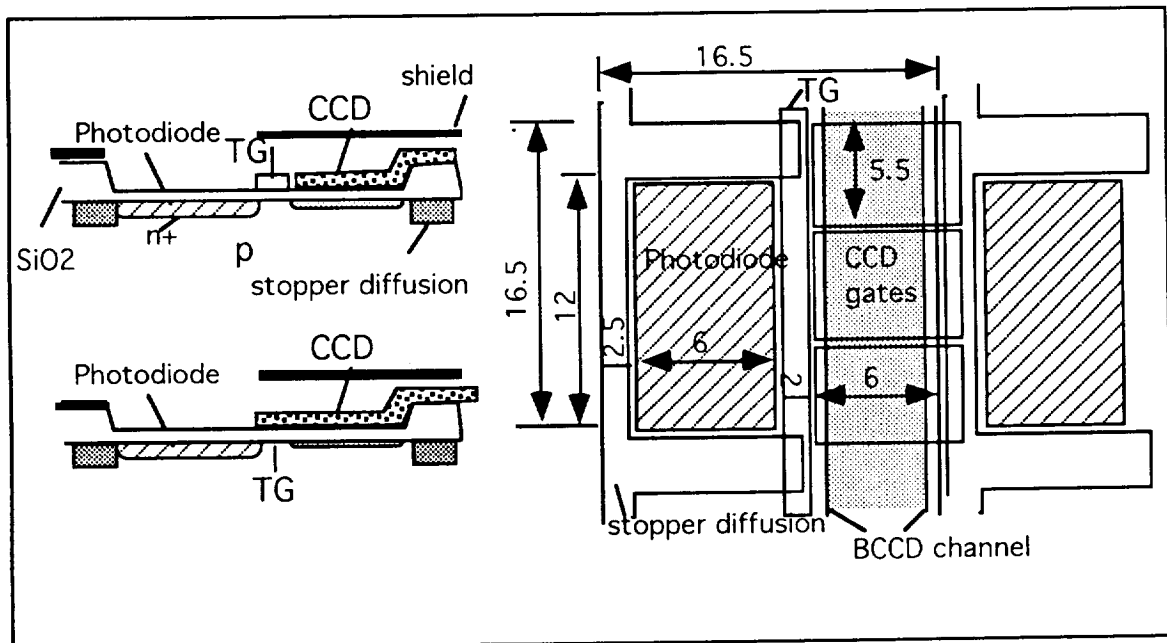


Fig. 7: Schematic cross section and top view of a CCD pixel consisting of a photodiode and CCD shift register. Dimensions are in μm for a $2\ \mu\text{m}$ technology.

During the integration cycle, the photo generated electron hole pairs discharge the reversed biased diode. After the integration cycle, the charge is transferred into the shift register

through the transfer gate (TG). During this period the diode is emptied of its charges and thus reversed biased. The potential disadvantage of the photodiode is that the diode will not be completely emptied resulting in higher noise. This can be overcome by using tailored doping profiles in order to fully deplete the diode. The advantage of the diode is the better sensitivity in the blue region. In addition, with the diode one can make an electronic shutter by pulsing the diode and draining the charge towards the substrate where it will be collected in overflow drains. If one uses a more sophisticated process that has tailored implantation levels, one can implement the TG and the gates of the CCD shift register as one gate and thus potentially reduce the dimensions. The dimensions are in general similar to the pixel discussed above. The fill factor is in the range of 25-30%.

b. CMOS based pixels

We will first give pixels that are based on the integration of charges during a fixed time, called the integration time. This requires clocked operation. Charges can be read out as a voltage or as a current pulse. The overall organization of such a structure is given in Fig. 8. Pixels are now addressed using a series of switches (MOS transistors) that are driven by vertical and horizontal registers. In its simplest implementation, these are shift registers which address each pixel serially. However, by using row and column decoders, one can randomly address each pixel, in a similar fashion as is done in a RAM. This opens interesting possibilities. One can envision putting a dummy pixel that can be addressed every time one needs to rip a line in order to span an unseen part of the output video line that represents the scotoma on the display. One could store the addresses in a neighboring RAM or EPROM that could be customized for each patient. Of course, a similar approach could be used for CCD where one would modify the clocking sequence in order to allow dummy charge packets to be inserted at the place where one needs to rip a line.

Fig. 9 gives a schematic circuit diagram, a cross section and top view of a simple diode pixel which is part of a scanned diode array as shown in the above figure. It consists of a photodiode surrounded by stopper diffusion on three sides and a polysilicon layer on the fourth side which acts as the gate of the pass transistor (row select switch - MRS). We have implemented the photodiode as a n+ to substrate junction for simplicity. However, a well-substrate diode would be better for sensitivity, at the cost of increased size. A minimum well size is 3 μm with a minimum spacing between wells of 8.5 μm . Note that we have not made the diode minimum size in order to increase the aperture ratio and the sensitivity. The advantage is a simple and relatively small structure (18.5 μm x 17 μm). As

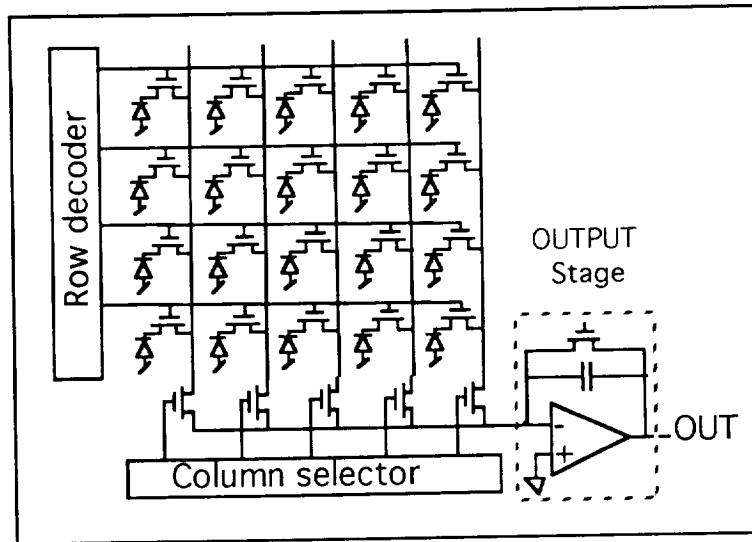


Fig. 8: Schematic architecture of an X-Y addressed MOS imager with diodes as photodetectors

mentioned before, it is compatible with random addressing of each pixels. The drawback of this structure is that the capacitance on which the charge of the diode is dumped during readout is the line capacitance of the column which can be large. This reduces the sensitivity and increases noise. Clock feed through from the addressing clocks can cause considerable fixed pattern noise on the output line. The readout process is destructive, as is the case with CCD sensors. One can overcome some of these problems by buffering the pixels from the column capacitance by inserting an amplifier. This can be a source follower as shown in Fig. 10. The diode is reset with the reset transistor MR before the integration cycle starts. The pixel contains a sample switch (MS) that opens just after the capacitor C has been reset with transistor MCR and at the end of the integration time. This puts the information charge on capacitor C (parasitic). After this is done, the photodiode is reset and a new frame can start. In the mean time, addressing of the individual pixel commences by clocking the gate of the row select transistor (MRS). The information charge on capacitor C remains during readout due to the buffering action of the source follower transistor MF. As a result, charge is not destroyed during reading and the pixel capacitance is much smaller than in the previous case without the buffer. Note that the load of the source follower is not included in the pixel as it can be common to all the pixels in a column. In addition, the presence of the reset transistor can act as an effective overflow drain to prevent blooming when a high intensity light beam falls on the sensor. Disadvantages are a larger pixel area and a smaller

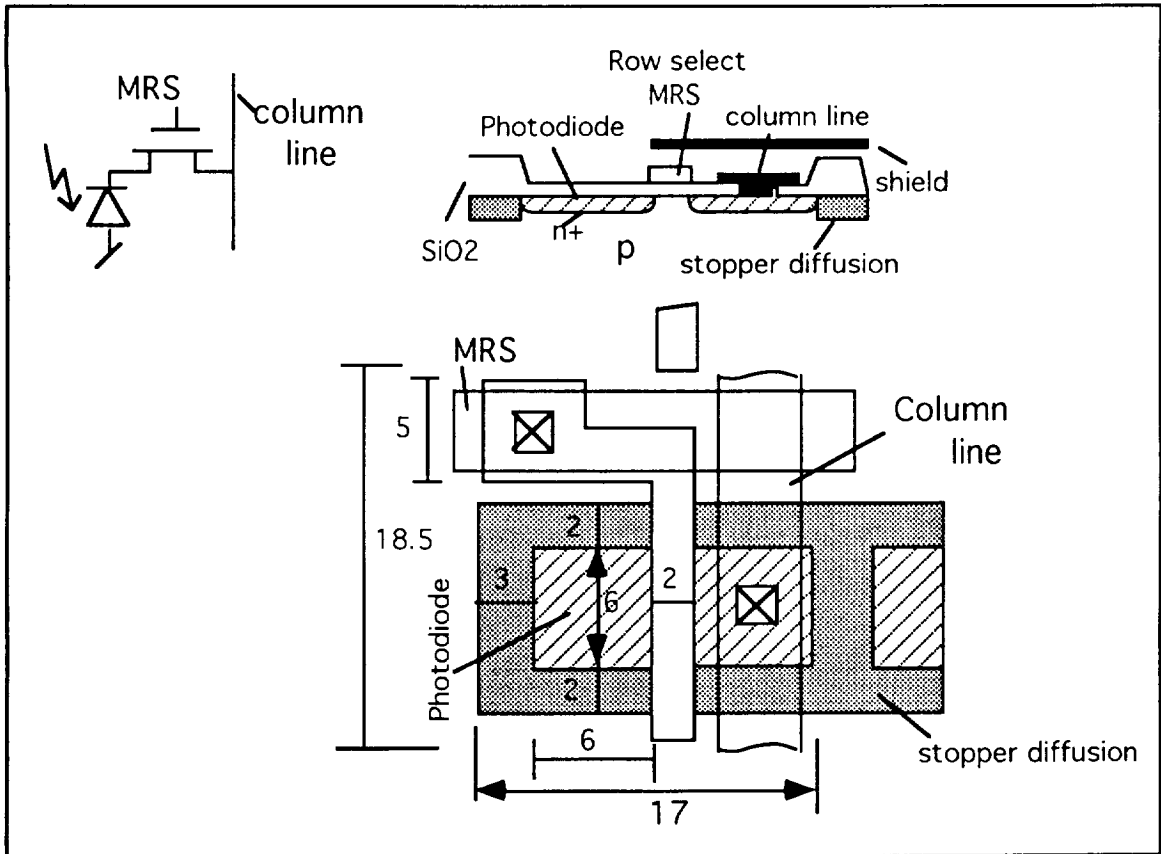


Fig. 9: Circuit schematic, cross section and simplified top view of a pixel in a MOS scanned array. The dimensions are in μm for a $2\mu\text{m}$ technology.

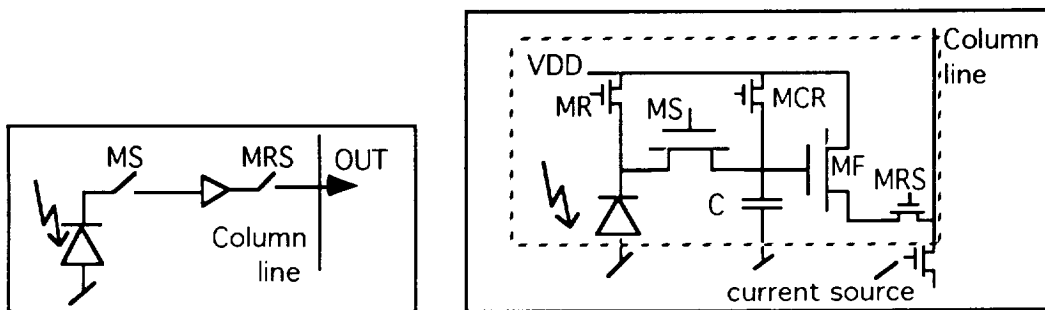


Fig. 10: Schematic circuit diagram of a pixel cell with multiple read capability. The structure contains a buffer (source follower MF) to isolate the information charge from the large line capacitance; transistor MS samples the diode charge onto C and MRS is the row select transistor. MR and MCR are reset transistors.

fill factor due to the presence of 4 transistors. Also, the source follower gain may be relatively small (~ 0.7) if one cannot short the bulk to the source (which requires that the transistor MF sit in its own well, further increasing the size). This structure would occupy about 50×50 sq. microns with a 6-10 % fill factor in a $2 \mu\text{m}$ CMOS technology.

A somewhat different structure is shown in Fig. 11. The pixel consists of a diode that is now buffered with a MOS transistor MA that acts as an amplifier. The row select switch is transistor MRS connecting the output current of the pixel amplifier to the column line where it can be measured. Resetting is done by transistor MR. The advantage of this structure is the smaller size, better fill factor and built-in amplification. The charge amplification is equal to $A_v \cdot C_o / C_d$, in which A_v is the voltage gain of the amplifier MA, C_o the line capacitance, and C_d the diode capacitance. A charge amplification of 80-100 is achievable. Potential problems are threshold variations among the transistor MA which can affect the gain and thus the uniformity. Also, the voltage levels may be critical to ensure proper operation of the amplifier. A similar structure had been used before with good performance⁸. The structure would occupy an area of about $23 \mu\text{m} \times 23 \mu\text{m}$ with an aperture ratio of 20% in a $2 \mu\text{m}$ CMOS technology.

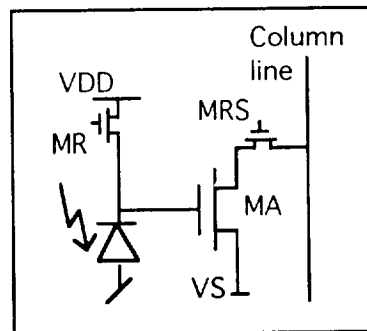


Fig. 11: Schematic circuit diagram of a CMOS pixel operating in the integration mode consisting of a photodiode and amplifier MA. The transistor MRS is the row select switch and MR the reset transistor.

The previous CMOS pixels integrated the photo generated charge onto a diode capacitance for a certain time. After integration time, the pixel is clocked in order to isolate the charge from the one generated during the next frame and to read the charge out. This scheme requires a clock. The next couple of possible pixels are not clocked but operate in the continuous mode by measuring the photo generated current in a reverse biased diode or bipolar transistor. Fig. 12 shows such a scheme. It consists of a diode connected to a

diode-connected MOS transistor ML acting as the load transistor. The current in the diode is proportional to the incident light and is converted into a voltage by the load. If the current is small enough, the load transistor will operate in the sub-threshold regime where the relationship between current and voltage is exponential. Due to the logarithmic compression, this scheme can be used under about 5-6 orders of magnitude of light intensity. The voltage is buffered using a source follower transistor (MF). The pixel is addressed with the row select transistor MRS which puts the voltage on the common column output line. No reset transistor or reset line is required. A pixel occupies about $22 \times 22 \mu\text{m}$ in a $2 \mu\text{m}$ CMOS process. This structure also works with a bipolar transistor that will give considerable amplification due to the current amplification in a bipolar transistor. The structure will be slightly larger than the one with a simple diode as photo detector.

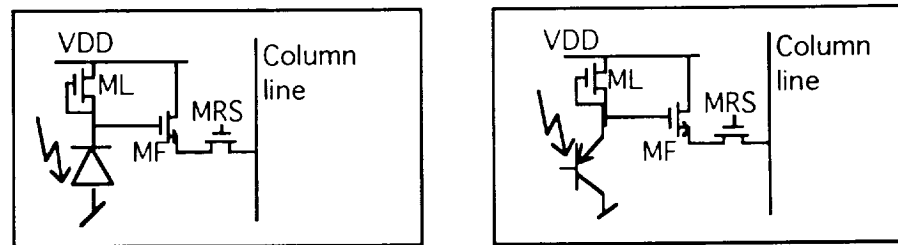


Fig. 12: Schematic circuit of a CMOS pixel with photo detector (diode or transistor) operating in a continuous mode. The transistor ML is the load which converts the photo current into a voltage. A source follower MF buffers the output voltage and transistor MRS act as the row select switch.

A slightly modified structure is given in Fig. 13. It consists of a photo transistor (or photo diode) with two load transistors and amplifier MA. The current source MCS can be made common to all pixels in a column. The transistor MRS is the row select transistor. The structure has logarithmic compression and is buffered by the amplifier from the column line. Instead of using an amplifier (common source) MA, one can also use a source follower by replacing the PMOS (MA) with an NMOS transistor which is basically the structure in the previous figure.

Another structure makes use of feedback in order to increase the dynamic range. It consists of a phototransistor and three MOS transistors, as shown in Fig. 14. The feedback keeps the currents smaller and thus extends the range of the logarithmic compression. However, it reduces the sensitivity at low light levels as the structure without feedback.

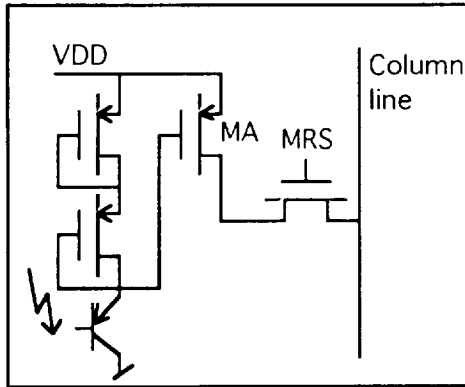


Fig. 13: Pixel with logarithmic compression and amplification (MA). The row select switch is implemented by transistor MRS.

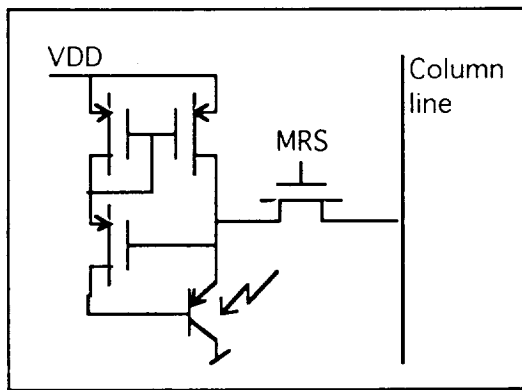


Fig. 14: CMOS pixel with feedback to obtain a large range of logarithmic compression. Transistor MRS is the row select switch⁹

There are several variations on the above scheme. One such scheme is given in Fig. 15. This structure consists of a load transistor ML and common source amplifier transistor MS. The feedback keeps the voltage over the diode constant. The pixel is basically a logarithmic trans-impedance amplifier except that the output is now a voltage. Also, this pixel allows continuous operation but requires four transistors. As the output node is a high impedance point, it may be more susceptible to noise pick up. As a result, the structure is less suitable for X-Y addressing.

Choosing a pixel structure depends on a variety of factors such as size, sensitivity, overall architecture. CMOS pixels provide the advantage of random addressing and amplification, if necessary, at the cost of increased pixel size. The choice among the above structures should be made after carefully considering the layout of each pixel and the inter-

connection and clock lines as well as doing some preliminary simulation on HSPICE to get a better idea about the performance.

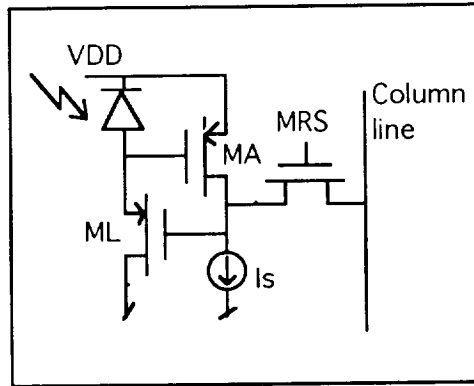


Fig 15: CMOS pixel consisting of photodiode, amplifier MA and row select transistor. The transistor ML acts as the load¹⁰.

6. Examples of State-of-the-Art Image Sensors

The goal of this section is to give a couple examples of the most recent image sensor developments. These sensors are not yet on the market. The purpose is not to give an exhaustive overview but some typical examples that will illustrate what will become possible in the near future. Most of the sensors are aimed at realizing HDTV quality cameras. As a result, they are making use of cartesian coordinates for the sensor geometry. It should be mentioned that the companies who are fabricating these imagers are generally not making their process available to outside customers. As a result, the dimensions of the cells and overall sizes given in these examples are not available to us.

6.1 Imagers for commercial HDTV applications.

- a. A 2/3" 2 Mega Pixel CCD for HDTV¹¹

This camera consists of 1920 horizontal and 1036 vertical pixels. Its a multiple frame-interline-transfer structure. The multiple frame transfer that makes use of multiple transfer of the diode charge using time sharing in the blanking interval. This scheme increases the dynamic range by almost a factor of two because the vertical CCD area can be increased.

The pixel size is only 5.2 x 5.0 sq. microns including the photodiodes, channel stop and vertical CCD cell for the data transfer. The width of the vertical CCD shift register is only 1 μm . These small dimensions usually degrade the performance (transfer efficiency). However, special implants were made to ensure high performance. Also, an optimized pixel was used which had a larger diode area and thus enhanced the sensitivity of the sensor which was 44 nA/lx. A schematic diagram of the overall sensor and pixel is shown in Fig. 16. A summary of the imager characteristics and performance is given in Table VI.

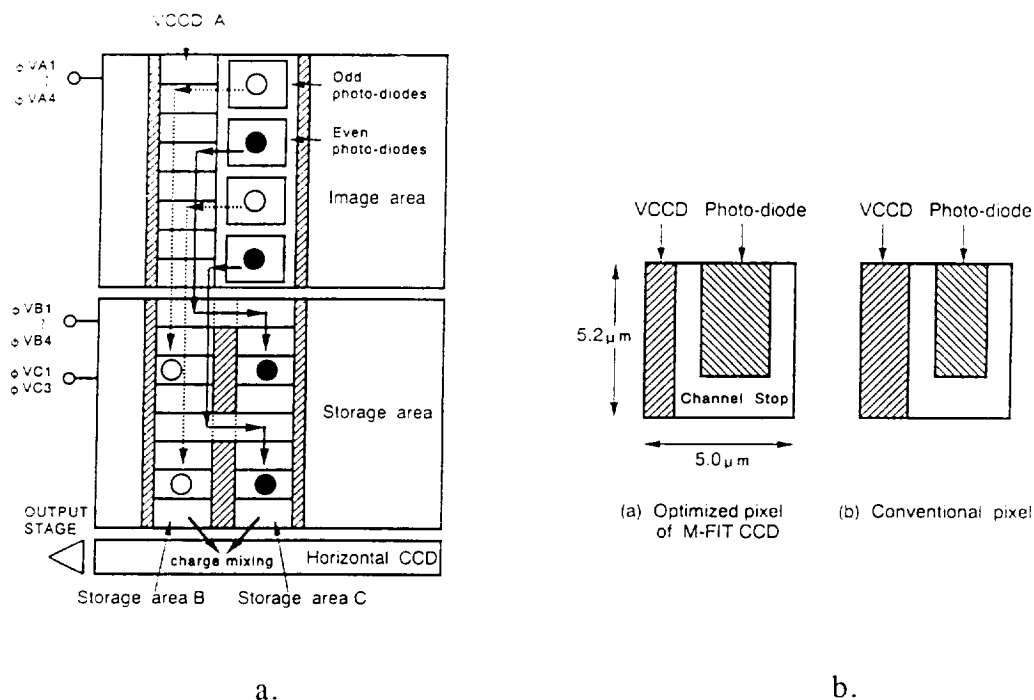


Fig. 16: a: Schematic diagram of the CCD FIT imager and b: pixel schematic¹¹

b. A 2/3" 2 Mega Pixel CCD Image Sensor¹²

This sensor has 1920 x 1080 pixels with each pixel occupying only 5.0 x 5.0 sq. microns. The overall architecture is an interline transfer scheme. Small dimensions combined with good performance have been obtained by using multiple wells and optimized implantation steps. This improves the charge handling capability and transfer efficiency in the vertical CCD transfer registers. Fig. 17 shows the overall architecture as well as the cross section of a unit pixel. The sensitivity is 27 nA/lx and dynamic range is 71 dB. The power consumption is only 0.49 W.

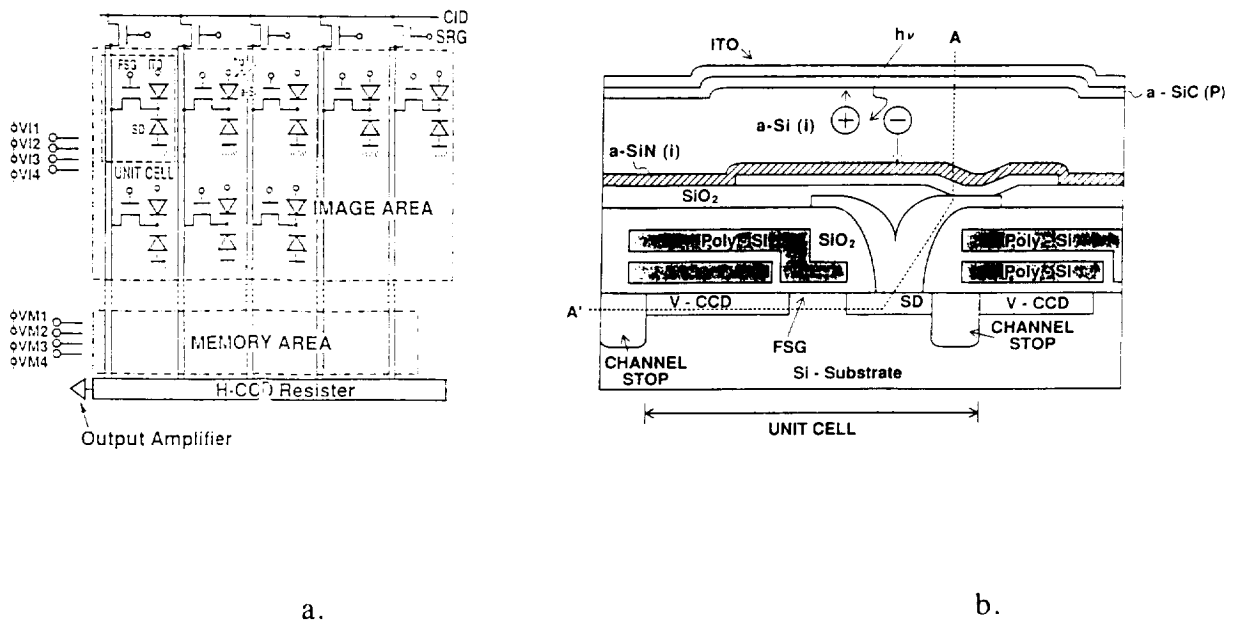


Fig. 17. a: CCD Image sensor diagram and b: cross section of a unit pixel¹².

c. A 2/3" 2 Megapixel STACK CCD Imager¹³

This image sensor makes use of stacked CCD cells in order to further increase the resolution without degrading the performance such as noise and smear level. The sensor makes use of an amorphous silicon photo conversion overlayer on top of the CCD scanning areas. This has the additional advantage of 100% aperture ratio regardless of the pixel size. The sensor is a frame interline transfer type CCD which consists of 1920 x 1036 pixels with a unit cell area of 5.0 x 5.2 sq. microns. The overall architecture and a unit cell cross section is shown in Fig. 18. The sensitivity of 100 nA/lx is quite high due to the large aperture ratio and the smear level low (-140dB). The dynamic range is 90 dB. The small cell size was realized by moving the charge injection diode (CID) and the resetting gate (SRG) outside each unit cell and placing it at the edge of the vertical CCDs. Tungsten silicide shunt wiring is used for high speed charge transfer by reducing the resistance of the vertical CCD polysilicon gates. It acts at the same time as a light shield. A summary of the sensor is given in Table VI.

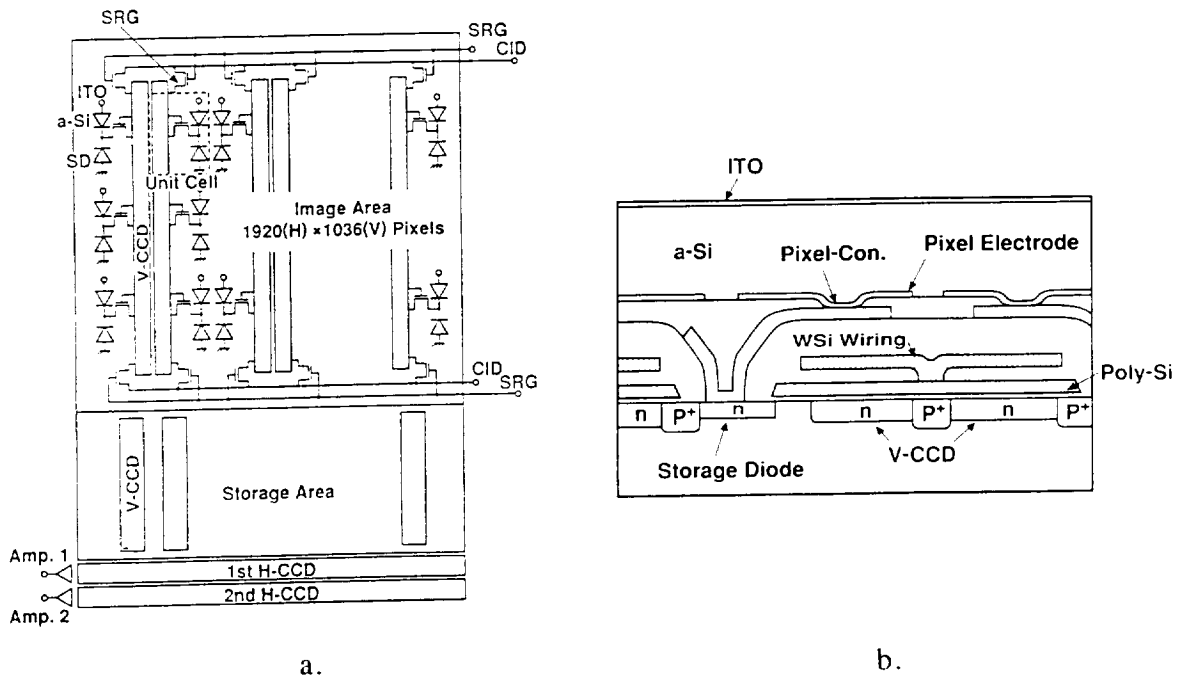


Fig. 18. a: Schematic block diagram of the STACK-CCD and b: pixel cross section¹³.

d. A 1/4 " Format 250K pixel MOS Imager with amplified pixel¹⁴

This imager is fabricated in a 0.8 μm double poly, double metal CMOS process. The authors claim that in order to further shrink the chip area and to obtain better sensitivity, CMOS technology would be preferred over CCD technology. The latter one requires complicated impurity profiles which is not suitable for LSE processing required for doing smart image processing on-chip. This sensor makes use of an amplified pixel in order to obtain high sensitivity, large dynamic range capability of rapid video readout and non-destructive readout. This was obtained by making use of the amplification capability of MOS transistors offered in a CMOS process. The pixel size is only 7.2 x 5.6 sq. micron, including the photodiode and 2.5 MOSFETs (a unit consists of 2 photodiodes and 5 MOSFETs).

A schematic block diagram and a unit (containing 2 pixels) is shown in Fig. 19. High sensitivity is also obtained by vertical two line mixing. This allows to keep the sense capacitance low and thus to increase the sensitivity. The sensitivity is very high, 1.6 $\mu\text{A}/\text{lX}$ without use of a microlens. The image area is 3.67 x 2.76 sq. mm for a total of 510 x 493

pixels. Data rates up to 74 MHz have been obtained. A summary of the imager is given in Table VI.

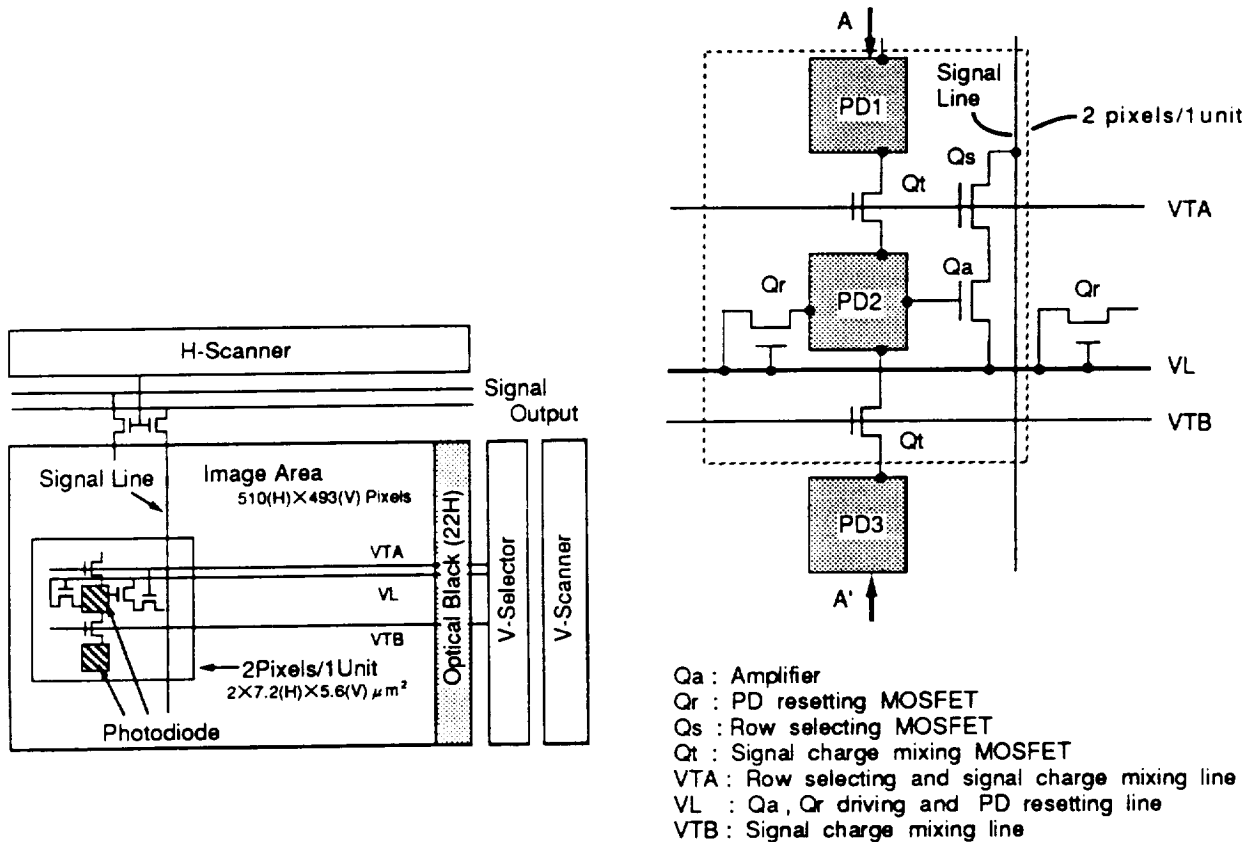


Fig. 19. a. Block diagram of CMOS image sensor and b. circuit configuration of 2 pixels¹⁴

6.2 Imagers with built-in computations not intended for HDTV.

The following sensors are being developed in various research laboratories and often incorporate computational elements to enhance the functionality of the imager. These sensors have usually a lower resolution because the increased real estate to accommodate the processing elements. The first example gives a CMOS sensor with active pixels which can

be randomly addressed. The second imager is an example of using the geometry to obtain functionality. It is a circular CCD that implements a logarithmic polar transformation. This is an interesting example because it is the only sensor fabricated with a non cartesian geometry.

a. A 128 x 128 CMOS Active Pixel Image Sensor¹⁵

Similar to the previous sensor, this one is also fabricated in a CMOS process. The process used was MOSIS 2 μ m p-well with double polysilicon layer. The authors have chosen CMOS technology over CCD for its capability to incorporate processing circuits at the pixel level as well as to fabricate architecture with random access of the pixels. Basically, each pixel consists of a small surface-channel CCD including photo gate, transfer gate, floating output diode with reset transistor and X address transistor (see Fig. 20). One pixel occupies 40 x 40 sq. μ m. The fill factor is only 28%, illustrating the price one must pay for incorporating processing circuitry at the pixel level. By making use of a more advanced technology the pixel size will shrink considerably. The structure makes use of a sample and hold circuitry that allows it to do correlated double sampling in order to reduce the kTC noise at the pixel and the 1/f noise. The frame rate of the 128 x 128 pixel sensor was 30 Hz. The sensor suffered from global fixed pattern noise (3.3% of the saturation signal). A summary of the sensor characteristics is given in Table VI.

b. Foveated Retina-like CCD image sensor¹⁶

A photosensor which models the sampling structure of the human retina has been implemented in a CCD technology. It consists of a relatively high resolution central area surrounded by a peripheral area whose resolution decreases with eccentricity. The photodetectors in the periphery are arranged in a log-polar grid. This is an example of an intelligent sensor whose computing elements are built into the geometry of the sensors. The unique organization of this sensors provide the following three advantagee over conventionalt imageres fabricated on a carthesian grid: (1) rotation invariance around the origian; (2) scale invariance; and (3) data reduction due to the exponential growth of the cell size along the radial axis. Each of these properties reduces the computational complexity of image processing. The sensor has applications for robotics, time-to-impact, and docking.

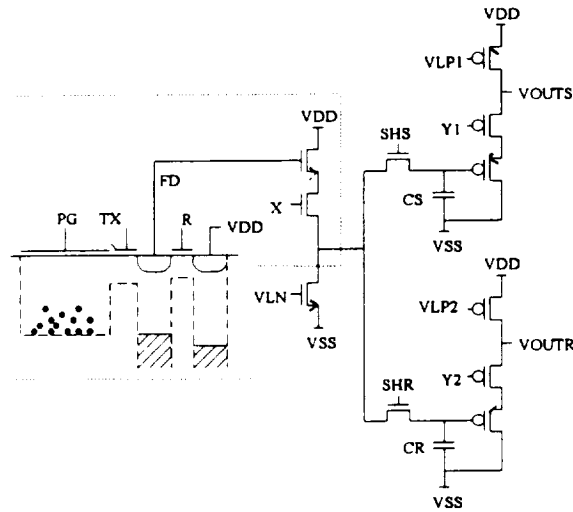
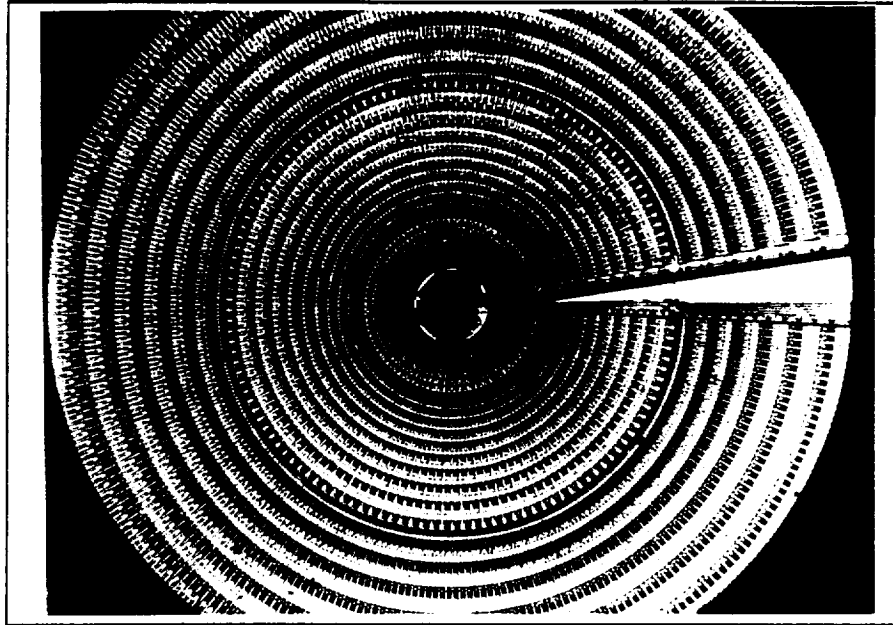
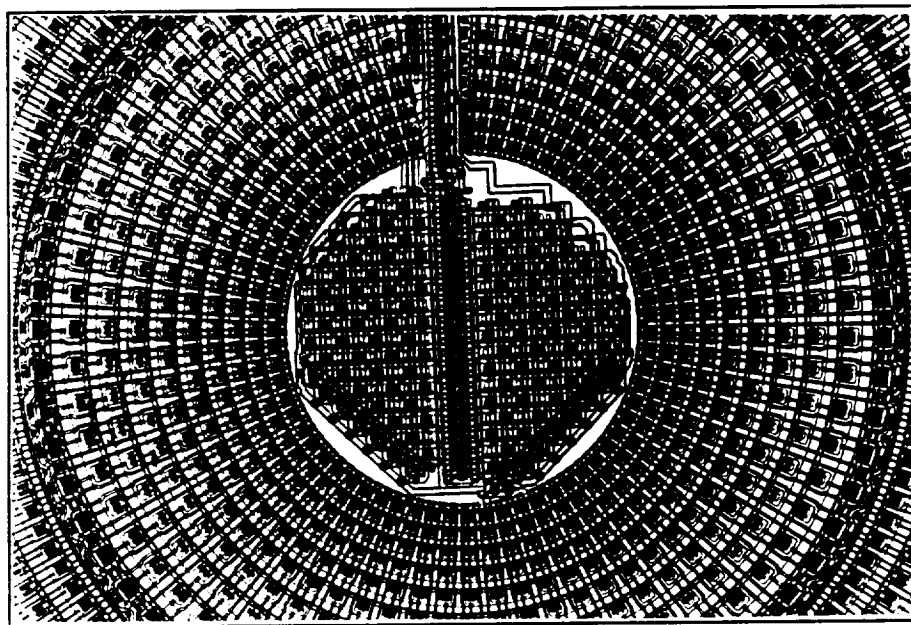


Fig. 20: Schematic of an active pixel sensor unit cell in a CMOS technology¹⁵.

The sensor consists of five functional parts: the fovea, the circular periphery, the serial or radial CCD register, the coupler between the circular and radial CCD, and the output structure. The periphery consists of 30 concentric circles which contains 64 cells each for a total of 1920 pixels. Each cell consists of a photodiode, a transfer gate and a CCD three phase shift register cell. The photosensitive area is defined by a light shielded. This structure is similar to the one shown in Fig. 6. The CCD was fabricated in a very conservative $5\ \mu\text{m}$ 3 phase polysilicon gate technology at IMEC. This resulted in a minimum cell size of $30\ \mu\text{m} \times 30\ \mu\text{m}$. The cell size increases exponentially with eccentricity which gives a maximum cell size of $412\ \mu\text{m}$. In order to maintain a good transfer efficiency, the sensor is divided into three radial parts. The middle part consists of 10 circles whose number of cells is doubled in order to reduce the cell size. The cells in the ten outer circles are further divided by two. This requires a clocking frequency which is twice and quadruple of the one of the inner circles for the middle and outer parts, respectively.



a



b

Fig. 21: Microphotograph of the Retina-like sensor: (a) overall sensor and (b) fovea and first 10 inner circles¹⁶.

TABLE VI: Overview of state-of-the-art CCD and CMOS imagers

	I	II	III	IV	V
Technology	CCD	CCD	CCD, 0.6 μ m	CMOS, 0.8 μ m	CMOS, 2 μ m
Format	2/3"	2/3"	2/3"	1/4"	
No. of Pixels	1920 x 1036	1920 x 1080	1920 x 1036	510 x 493	128 x 128
Pixel Dimen. (μ m)	5.2 x 5.0	5.0 x 5.0	5.0 x 5.2	7.2 x 5.6	40 x 40
Image Area	9.6 x 5.4	9.6 x 5.4	9.6 x 5.4	3.67 x 2.76	6.9 x 6.9
Sensitivity (nA/lx)	44	27	100	1800	4 μ V/e ⁻
Dyn. Range (dB)		71	90	75	71
Saturation (nA)	580	400	960	7200	150 Ke ⁻
Noise e ⁻		11.3e-		.55 dB	42e ⁻
Smear (dB)	- 100	- 80	- 140		
Aperture Ratio					26%
Remarks	On-Chip μ lens	On-Chip μ lens, low power 0.49 W		Stacked photo- conversion layers	
References	1	2	3	4	5

7. Issues related to implementing a sensor for image warping

a. Minimum pixel sizes.

Details on the size and geometry of individual pixels are discussed in the section above, dealing with design rules and pixel types. The purpose of this section is to draw some general conclusions about possible sizes. The numbers are given for a 2 μ m technology. These can be scaled for processes with different feature sizes.

The smallest sizes are obtained for the simplest pixels, i.e. those pixels which consists of the photodetecting element and addressing circuits (or shiftregister for read-out). Sizes of 18 by 18 μ m² are feasible of which the photosensitive area may vary between 6x6 μ m² to 6x12 μ m² for a CMOS or CCD cell, respectively. This will give fill factors of 11% and 22%. Figure 22 gives a schematic view of the pixels and photosensitive area. The

numbers are based for pixels on a cartesian grid. One can draw non-manhattan geometris (which will be required for realizing the warping), the sizes will increase slightly as imposed by the design rules. One can expect an increase of about 8-10%.

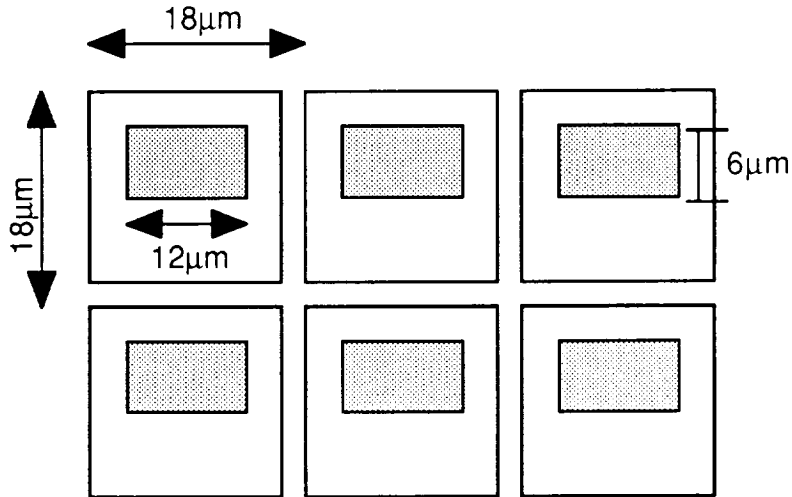


Figure 22: Schematic floorplan of pixels and photosensitive area.

If needed, one can make the photosensitive area smaller. As the rest of the circuit can not be reduced much, this will result in a smaller fill factor and sensitivity. The smallest obtainable geometry for the photodetectors is in principle the minimum feature size, i.e. $2 \times 2 \mu\text{m}$ for a photodiode. The effective area will be somewhat larger due to lateral diffusion of the charges generated in the area surrounding the photodetectors. However, it is not recommended to work with these small area because the low sensitivity (small fill factor), increased aliasing and also the larger pixel to pixel variations. For all practical purposes, one should not use sizes smaller than about 6×6 to $8 \times 8 \mu\text{m}^2$ for the photoelements itself.

One is not limited to the cartesian geometry for implementing the photosensitive areas. In principles one can make any shape, taking into account the effect of the finite grid size with which the masks and thus the geometries are defined. The result is that any orientation different from 0 , 45 and 90° will be approximated with $0.1 \mu\text{m}$ (not scalable with the technology) line segments. To implement a sensor that does image warping, there are different options. One can use pixels fabricated on a cartesian grid but offset from each other along the line of the transformation, as illustrated in Fig. 23 a. In addition to displace the pixels one can also shape the pixels appropriately. The latter method may implement the warping more accurate but will require a slighter larger area. In comparison to the floor

plan of Fig. 22, the one of Fig. 23 will require a larger overall area to accommodate inter-connection lines which will not run along straight channels. Also there will be more "dead" area between elements to accommodate the layout rules resulting in a less efficient layout structure (e.g. it will be more difficult to combine areas among pixels). The exact penalty one has to pay can be determined only after making a detailed layout. However, to a first approximation gives an increase of about 10-20 % over the manhattan geometry.

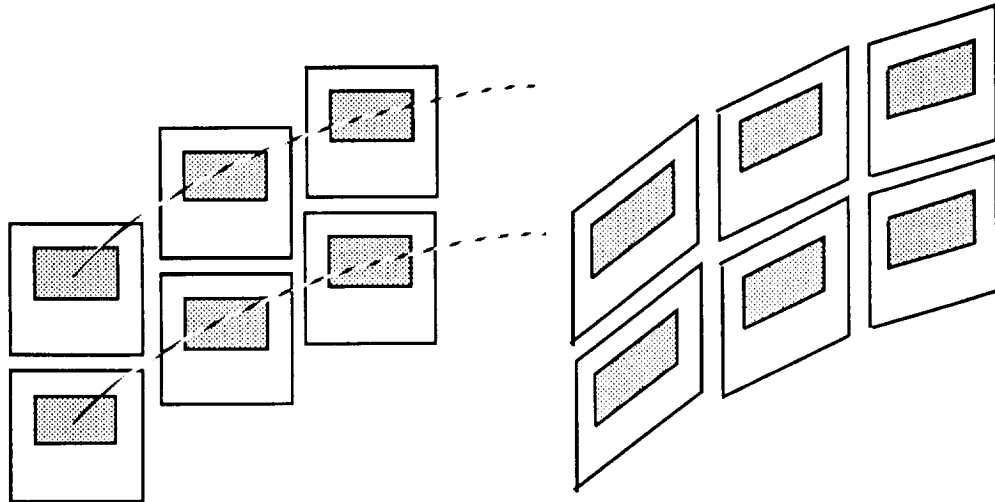


Fig. 23: Floor plan of a warped image with pixels on a Cartesian (a) or a non-Cartesian grid (b).

b. Maximum pixel size

Creating pixels with larger sizes is always possible from a technology point of view. Design rules usually specify only minimum dimensions and rarely maximum ones. However, the limitation on the maximum size is usually imposed by the performance. In case of a CCD cell for instance, making the cell size larger will reduce the transfer efficiency considerably. For CMOS detectors larger area will give larger capacitances which could slow down the read-out speed. In general one should limit the maximum cell size to about $150 \times 150 \mu\text{m}^2$. If larger sizes are required one can split the cells into smaller ones and combine their output later on.

c. Making curved lines and the effect of finite grid size

Realizing a warped sensor requires a non-Cartesian geometry. One of the first questions that comes to mind, is how accurate can one implement non-Cartesian structures.

According to the two manufactures who were contacted (Orbit and IMEC) the smallest grid size for mask fabrication is $0.1 \mu\text{m}$; lines under a 45° angle can be fabricated as well. This implies that lines with any other orientation than 0° , 45° and 90° will be approximated by smaller line segments snapped to the closed grid point. Figure 24 shows this schematically in case that the line is approximated by a staircase or by line segments of 0° , 45° and 90° , respectively. The maximum distance, measured orthogonal, from a grid point to the line is $0.07\mu\text{m}$ for a $0.1 \mu\text{m}$ grid. However, the average error will be considerably smaller.

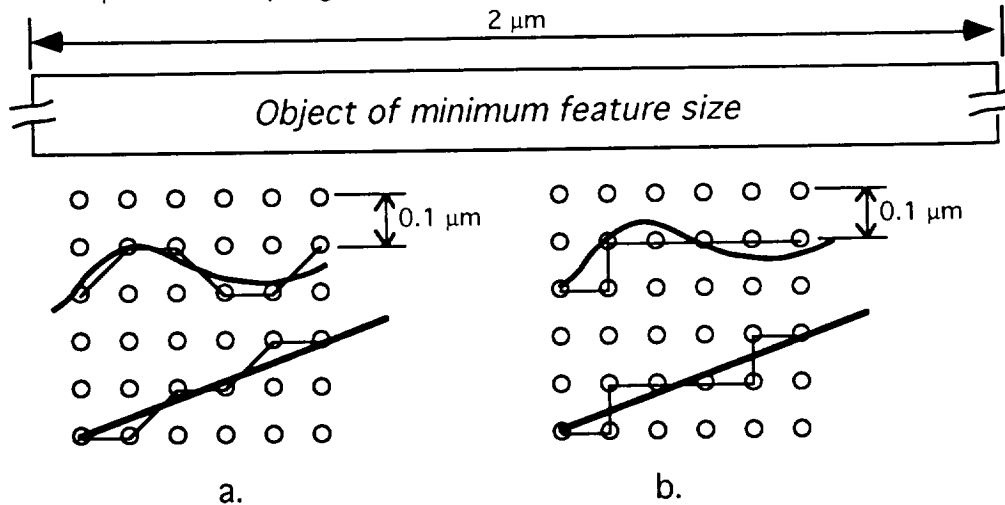


Fig. 24: Illustration of how a non-carthesian geometry will be approximated in case that (a) lines of 45° are possible or (b) only 0° and 90° lines are possible.

This approximation must be looked at in relation with the size of the geometrical figure one wants to fabricate. The design rules limit the minimum feature size. In case of a $2\mu\text{m}$ technology this means that one cannot make anything that is smaller than $2 \mu\text{m}$ (similarly for a $1.25 \mu\text{m}$ technology). It is compared to this dimension that one needs to look at the error introduced by the finite grid size. To get an idea of the relative scale, the length of the rectangle in Fig. 24 corresponds to the minimum size that one is allowed to draw in a $2 \mu\text{m}$ technology. The maximum error that is introduced in relation to the minimum feature size is around 3.5% (5.6% for a $1.25 \mu\text{m}$ technology). From the discussion of pixel sizes, we know that a typical pixel has a minimum size of about $16 \mu\text{m}$ (for a $2\mu\text{m}$ technology). Compared to these dimensions, the error is about 0.4%. In addition, one should keep in mind that the image is already convoluted by the finite window size of each pixel which have a size of about $6 \times 6 \mu\text{m}^2$ and pitch of $16 \mu\text{m}$. Also one has to take into account the tolerance on the actual size of the geometry as a result of errors in the production (lithography, etching and registration errors) which is typically several percent of the mini-

mum feature size. As a result, we can expect that the effect of the finite grid approximation on the imager performance will not be significant or worse than other factors, such as fabrication tolerances or the finite pixel size.

8. Summary and Recommendations

This report gives an overview of different imaging technologies and explains what is feasible in terms of minimum pixel size, geometries and functions. CMOS is the recommended technology over CCDs for its flexibility to implement function on the array ranging from active pixels, random addressing, logarithmic compression, to adaptation . Also the lower cost and wider availability is an advantage of CMOS sensors. This and the above advantages result in a smaller and less expensive overall system.

The smallest pixel size in a 0.8 μm technology is about $9\mu\text{m}\times 9\mu\text{m}$ with a fill factor of about 20-30%. The fabrication of a 1.2 μm CMOS prototype chip of $9.6\text{mm}\times 9.6\text{mm}$ is about \$20K or up for a limited number of samples (typically 36). The actual geometry will be drawn on a grid of 0.1 μm which will introduce small deviations from the desired geometry, if the line orientation is different from 0, 90 or 45°.

9. Addresses

Orbit Semiconductor, Inc.
1215 Bordeaux Drive
Sunnyvale, CA 94089
(408) 744-1800 phone
(408) 747-1263 fax

Contact person: Sam Reynolds
MOSIS Service
USC Information Sciences Inst.
4676 Admiralty Way
Marina del Rey, CA 90292-6695
(310) 822-1511

Mr. Lou Hermans
IMEC vzw
Kapeldreef 75
3001 Leuven, Belgium
32-16-281211 phone
32-16-289400 fax

email: hermans@imec.be

Jan Van der Spiegel
University of Pennsylvania
Dept. of Electrical Engineering
200 S. 33rd Street
Philadelphia, PA 19104-6390
215-898-7116
fax: 215-573-2068
jan@ee.upenn.edu

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