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Pulse Code Modulation Encoder Handbook for Aydin Vector MMP-900 Series System

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for
AYDIN VECTOR MMP-900 SERIES SYSTEM

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INTRODUCTION

The information required to efficiently and reliably use the Aydin Vector Division MMP-900 PCM series is presented in this document. The MMP-900 series is an upgrade of the MMP-600 series. The system's capacities and restrictions are outlined and obligatory interfacing facts are provided.

Due to the system's small size , low power depletion and programmable flexibility, a broad range of telemetry data transmission requirements can be fulfilled by this encoder system. Components and system level testings are performed by the manufacturer. The systems are submitted to temperature extremes of -35 degrees Centigrade and +85 degrees Centigrade.

Once the data requirements for a particular mission are defined, the essential components are provided from the NASA/Wallops Flight Facility stock of PCM components. The modules are then assembled, followed by the functional and vibration testing.

GENERAL DESCRIPTION

The MMP-900 PCM encoder system has flown on more than or close to 100 sounding rockets without any in-flight anomaly. Functional testing has encountered stack failures and an account of some of these failures will be provided in this document. A general block diagram of the system is shown in Figure 1 and an exploded view of a typical stack is shown in Figure 2. The following modules will be described:

Group I - System control modules

PX-984	-	Power Supply module
TM-915D	-	Timer module
FL-919A	-	Quad Filter module
FM-918	-	Formatter module
PR-914	-	Programmer module
AD-906	-	Sample & Hold and Analog to Digital Converter module

Group II - Multiplexer modules

MP-901	-	High Level Analog Multiplexer module
PD-929	-	Parallel Digital Data Multiplexer module
SD-924	-	Serial Digital Data Multiplexer module
CM-922PB	-	Counter/Accumulator module
TA-923	-	Time Event Monitor with Alternating Registers module
TB-925	-	Time Event Monitor with Timing Buffers module

These modules should be handled with care when assembling a particular stack. The connectors can be damaged if the modules are not properly interconnected.

The Power Supply module, PX-984, must be located at the bottom of the stack. The Power Supply and the entire stack must be heat sinked during operation. The Sample & Hold and Analog to Digital module, AD-906, should be located above the Power Supply module. The Formatter module, FM-918, should be positioned above the Sample & Hold and Analog to Digital module. The Quad Filter module, FL-919A, must be located directly above the Formatter module. This permits adjustment of the potentiometer in the Quad Filter module through a slot in the Formatter module. The Timer module, TM-915D, should be positioned above the Quad Filter module. The End Plate, EP-912, must terminate the physical stack. The Programmer module, PR-914, must be located directly beneath the End Plate. All multiplexer modules, MP-901, PD-929, SD-924, CM-922PB, TA-923, and TB-925, may be situated between the FL-919A and the TM-915D. These modules may be placed in any type of stacking order.

The MMP-900 encoder system may be mounted in three configurations, external connectors facing up, right, or left. #4-40 socket head screws are used to mount the system onto the payload.

In each group of modules, hardwire programming is required. This is accomplished by grounding appropriate pins on the external connectors of these modules. The programming pin inputs are pulled up to a specific voltage dc through a specific resistance.

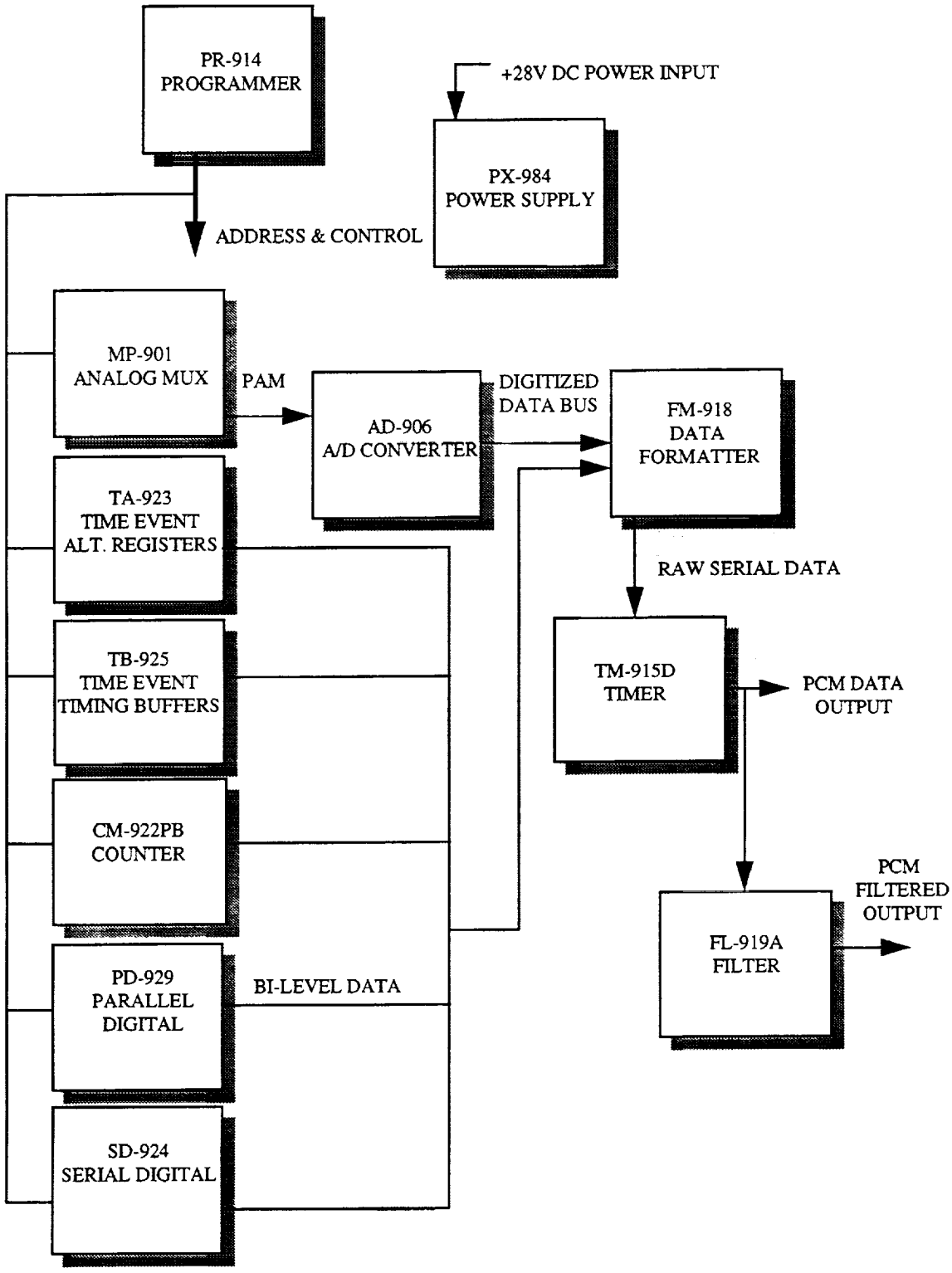


Figure 1. - General block diagram of MMP-900 system.

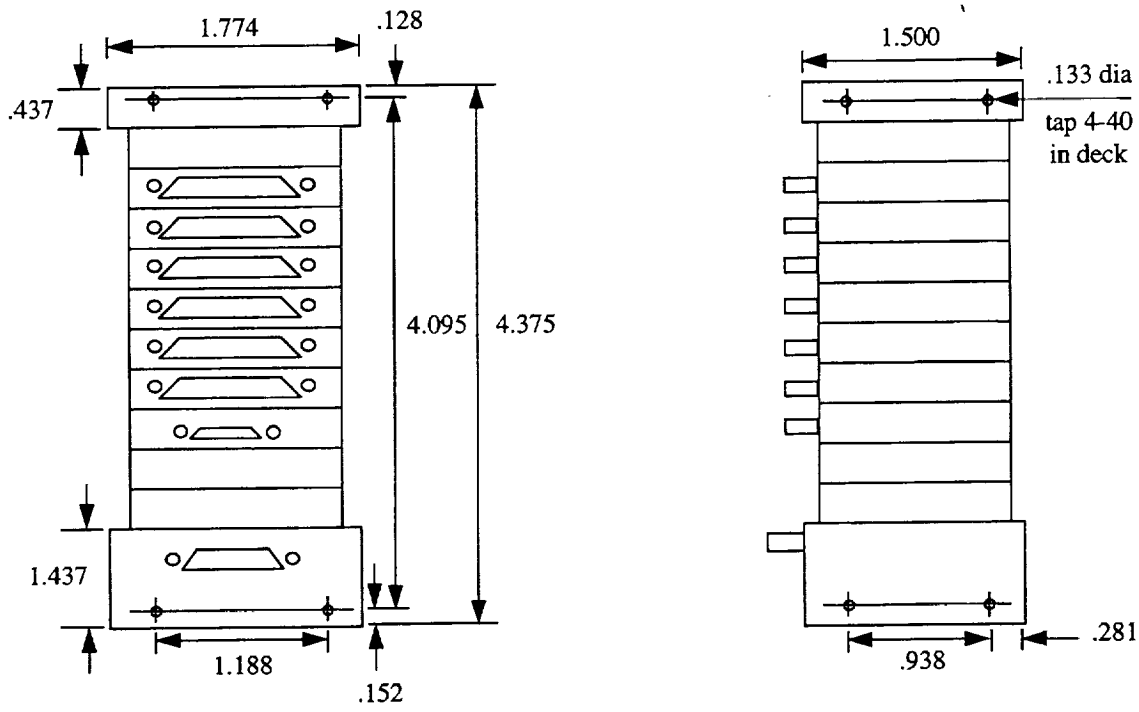


Figure 2. - Exploded view of MMP-900 PCM encoder system.[1]

[1] Of course, the length of the PCM stack may vary. 4.095" and 4.375" are typical length measurements.

One of each module listed below is required in every system.

PX-984 Power Supply. - This module embodies a synchronous, isolated dc to dc power supply which also includes the basic crystal oscillator for the system. An external clock input exists at the Power Supply module. Bit rates up to 1 megabits per second are feasible.

PR-914 Programmer. - This module contains the processor control circuit. The PR-914 performs as a microprocessor, executing the software program entered in the EPROM. This module also controls the timing and operation of the entire system.

FM-918 Formatter. - This module accepts all of the digital data from the AD-906 and all the digital data modules. This module merges them with frame synchronization words and performs parallel to serial conversion.

TM-915D Timer. - This module receives serial data from the Formatter module then converts this data into the desired output codes Biϕ-L, Biϕ-M, Biϕ-S, NRZ-L, NRZ-M, NRZ-S. The Timer module also provides buffered test point outputs. Programmable parameters at the Timer module are number of bits per word (8, 9 or 10 bits), parity select (odd or none), and the output codes mentioned above.

EP-912 End Plate. - This module holds the removable EPROM and terminates the stack.

Utilization of each module listed below is discretionary. Variable quantities of each module can be used dependent upon the data input requirements.

FL-919A Quad Filter. - This module contains four linear phase lowpass filters, and an adjustable gain amplifier. The output voltage gain is variable using the potentiometer on this module.

AD-906 Sample & Hold and Analog to Digital Converter. - This module is, of course, obligatory only when analog data inputs are existent. This module digitizes each analog word into a 10-bit binary code by method of successive approximations. The AD-906 does not have an external connector and no programming is necessary.

MP-901 32-Channel High Level Multiplexer. - This module accepts 32 individual analog inputs. The system allows for up to seven MP-901.

SD-924 Serial Digital Data Multiplexer. - This module accepts eight individual serial channel inputs. The system allows up to four Serial Digital Data Multiplexer modules.

CM-922PB Dual Counter/Accumulator. - This module counts pulses and includes two counters/accumulators. The system allows up to nineteen modules.

TA-923 Time Event Monitor with Alternating Registers. - This module accepts two event pulse inputs and is used to determine the relative occurrence of events. The alternating registers reduce the rate at which this module must be read out. Only one TA-923 module is allowed per system.

TB-925 Time Event Monitor with Timing Buffers. - This module accepts two event pulse inputs and is used to determine the relative occurrence of events. The timing buffers provide counter outputs of word number per frame and minor frame number. Only two TB-925 modules are allowed per system.

MULTIPLEXING CONTROL

The multiplexing sequence is determined by means of an 8-bit parallel address, A7-A0, generated by the Programmer module and bused internally to all multiplexer modules. The most significant bit (MSB) is designated by A7 and the least significant bit (LSB) is designated by A0. The higher order address lines select a multiplexer module while the lower address lines select a single channel within a specific module. Each data module is allocated a particular address in a system.

EPROM CONTROL & DATA FORMAT

The written system program residing in the 512 x 8 EPROM is responsible for several format characteristics. *It takes two 8-bit bytes for a full instruction.*

- The system program sets the sampling rate of all analog and digital data inputs. Subcommutation and supercommutation yield , of course, changeable sampling rates within the data sampling format.

- The bit pattern and the number of frame synchronization words in the format are under EPROM dominion.

- The position of each measurement (input channel), synchronization words and the subframe identification within the data format are under EPROM control.

- Major and minor frame lengths are under EPROM control. A major frame length of 247 words is possible (without subcommutation in the format). The following equation rules when subcommutation is used:

$$L = 256 - 2F - \Sigma Q_n (n + 2) \qquad (1)$$

where

L	=	Maximum minor frame length
F	=	Number of frame synchronization words in one minor frame (including the subframe identification counter word)
Q_n	=	Number of subframes that are n words in depth
n	=	Subframe depth (number of words in subcommutation)

SYSTEM SPECIFICATIONS

I. Analog Accuracy

Using the maximum internal bit rate of 800 kilobits per second, four MP-901, and introducing a source impedance of 2 kΩ will cause no more than 0.075% ±1/2 LSB error. The percentage refers to full scale input of +5 volts.

II. Analog to Digital Conversion

The conversion process is achieved by the method of successive approximations.

III. Bit Rate Stability

The crystal clock in the power supply provides an error no greater than 0.02%. The bit rate accuracy and stability for systems utilizing an external clock meet the standards set by IRIG Document 106-80 sections 4.3.1 and 4.3.2.

IV. Crosstalk

Based upon an 8-bit word, there is not more than ±1 count of crosstalk with a *noiseless* (steady) signal generator at any time with a fully assembled stack.

V. Frame Synchronization

The number, bit pattern, and location within the format of the frame synchronization words are under EPROM control. A subframe identification counter is used when using subcommutation. All synchronization words are programmable by the user as preferred.

VI. Linearity

The analog to digital converters deviation from a best straight line is ±1/2 of the LSB maximum.

VII. PCM Output Formats

PCM output codes include Biϕ-(Level, Mark, or Space) and NRZ-(Level, Mark, or Space). These output codes are available at the Timer module.

VIII. Premodulation Filter

The premodulation filters are linear phase low pass filters. The final roll off slope of the filters, past the -3 dB corner frequency, is -36 dB/Octave minimum. The voltage level of the filtered PCM output is adjustable at the Quad Filter module and covers the range 0.1 volt peak-to-peak through 10 volts peak-to-peak centered about 0 volt. The output impedance is 10 Ω maximum.

IX. Resolution

The number of bits per word is determined by the resolution entered at the Timer module. Naturally, eight, nine or ten bits are selected. Word length programming is also available at the external connector of the Serial Digital Multiplexer module and the Dual Counter/Accumulator module.

X. Unfiltered PCM Output Level

The unfiltered PCM output level is CMOS and low power TTL compatible. Logic "0" falls in the range 0 to 0.1 volt dc. Logic "1" falls in the range +5 ±0.5 volts dc. The output impedance is 1 kΩ. The outputs are short circuit protected to ground.

XI. Word Structure

Word length is fixed such that all words within a single system contain an equal number of bits. The transmitted bit sequence is MSB first then LSB last. For systems using less than 10 bits per word, the LSB is truncated from the 10-bit analog to digital conversion.

ELECTRICAL SPECIFICATIONS

I. Current Drain

The current drain is 500 milliAmperes *maximum*.

II. Data Channel Inputs

All analog channel inputs are 0 to 5 volts. The condition of all analog channels with inputs ranging from -35 to +35 volts dc will not cause any permanent damage to the system. It is recommended that no more than 20 inputs per module be subjected to the voltage extremes simultaneously.

Parallel digital channels will accept -35 to +2 volts dc to provide an output of logic "0" and +3 to +35 volts dc to provide an output of logic "1". All parallel digital inputs will tolerate any voltage within the above specified range without causing permanent damage to the module.

Serial digital channels will accept -1.5 to +0.9 volts dc to provide an output of logic "0" and +3.15 to +6.5 volts dc to provide an output of logic "1". All serial digital inputs will tolerate any voltage within the above specified range without causing permanent damage to the module.

Counter inputs will accept full 0 to +5 volts dc pulses of duration 500 nsecs minimum. Voltages applied to counter inputs within the range -0.5 to +5.5 volts dc will not cause any permanent damage to the module.

Time event pulse inputs, used to measure relative time between pulses, are 0 to +5 volts nominal and of duration 1 microsecond minimum to insure triggering of the module. Voltages applied to the inputs within the range -0.3 to +36 volts will not cause any permanent damage to the modules.

III. Fault Protection

With all outputs shorted to ground, no permanent damage will result to the system.

IV. Power Input

The power input is +28 $\pm$4 volts dc. Power is applied to the external connector of the Power Supply module.

V. Reverse Polarity Protection

A continuous supply of -32 volts dc applied to the power input will not cause permanent damage to the system.

VI. System Grounding

The signal, power, and chassis grounds in the system are all mutually isolated.

MECHANICAL SPECIFICATIONS

I. Connectors

A connector with 3 feet of insulated wire installed onto each pin is provided. Each connector includes slotted screw and screwlock assemblies. Each connector mates properly with the intended module.

II. Finish

The finish is nickel plate.

III. Mounting

The system has the capability to be mounted in either of two planes, connectors facing upward and laterally. The mounting screws are #4-40 socket head screws and are supplied with each system.

IV. Size

The overall size of a 32-channel High Level Analog Multiplexer module is 1.52" x 1.77" x 2.38" not including the mating connectors.

V. Stacking

The stacking screws are #2-56 pan head screws supplied uncut and then custom cut to satisfy the stack length of the specific systems.

VI. Weight

The Power Supply module weighs no more than 95 grams (3.4 oz.). All other modules weigh no more than 25 grams (0.88 oz.).

ENVIRONMENTAL SPECIFICATIONS

I. Acceleration

The satisfactory acceleration is 100 G steady state for one minute in each of the three major axes.

II. Altitude

All modules will operate within specification up to an altitude of 2,000 kilometers.

III. Electromagnetic Interference

The electromagnetic interference (EMI) tolerance conforms with MIL-STD-461A and 462.

IV. Humidity

The admissible range for all modules is 0 to 95% relative humidity.

VI. Operating Temperature

The operating temperature is between -35°C and +85°C. All modules will operate within specification at all bit rates of (6.25, 12.5, 25, 50, 100, 200, 400, 800) kilobits per second and for 8, 9 or 10 bits/word over this temperature range.

VI. Random Vibration

Tolerable vibration is 29.3 G rms from 20 to 2,000 Hz in each of the three major axes.

VII. Shock

The tolerable shock is 100 G rms for 11 milliseconds in each of the three major axes.

VIII. Storage Temperature

The storage temperature is between -54°C and +100°C. No permanent damage will occur to any module after being stored within this temperature range.

The modules making up the system contain static sensitive electronics. Proper electrostatic discharge precautions should be exercised when handling any module.

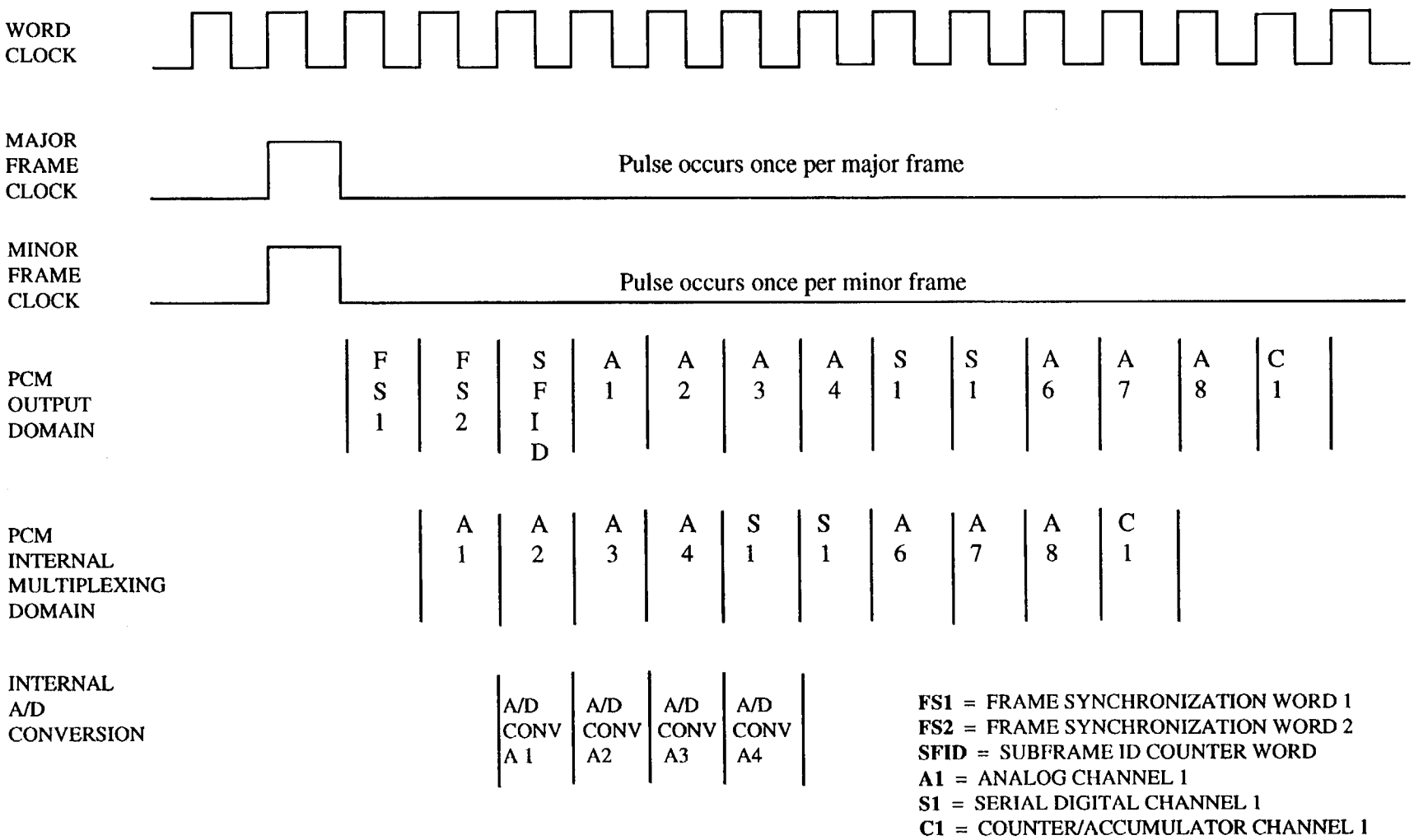


Figure 3. - System timing diagram.

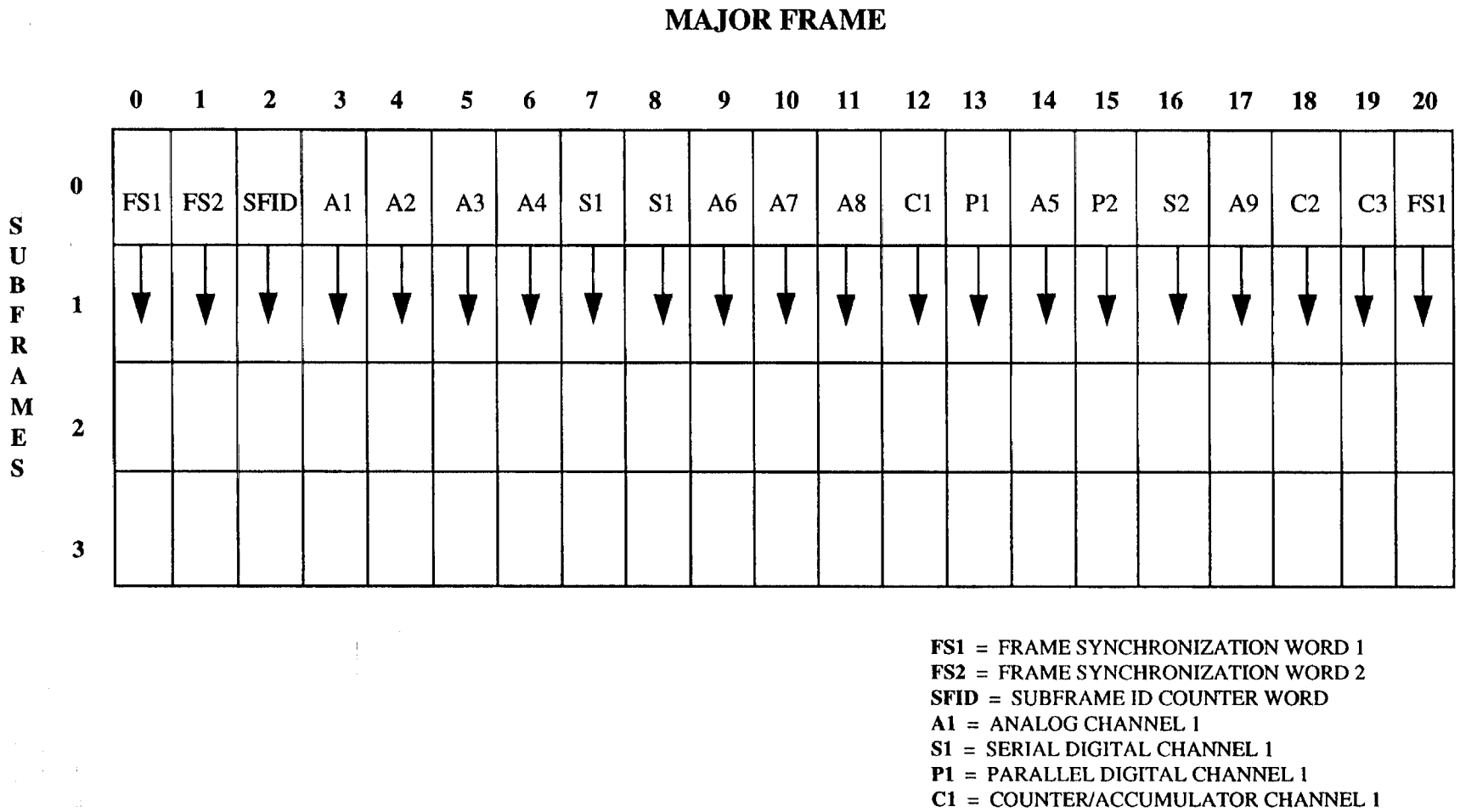


Figure 4. - Sample data format.

DETAILED DESCRIPTION OF THE PCM ENCODER SYSTEM GROUP I MODULES

PX-984 POWER SUPPLY MODULE P/N 17984010-501

The Power Supply module (Appendix C, page C-3) holds a synchronous, isolated dc to dc power supply which provides power to the system on an as needed basis. This module accepts +28 volts ±4 volts dc as nominal power input. A crystal oscillator is also included in this module which contributes the essential 2X clock for the system.

Three programming pins found at the external connector allow for the option of one of the eight bit rates. Programming is attained by grounding appropriate pins. An open programming pin is considered to be a logic "1". The programming pins are pulled up to +10 volts through 50 kilohm resistors. The Power Supply module also allows for the utilization of an external clock. This capability will permit system bit rate to reach 1 megabits per second. In the occurrence of a failure of the external clock, the system will revert to the programmed system bit rate. It is recommended to program a system bit rate close to the desired bit rate when using an external clock. Please refer to the table below for the bit rate programming and the external clock frequencies.

TABLE 1. - BIT RATE PROGRAMMING

Program C	Program B	Program A	8.0 MHz Xtal Kbit/sec	6.4 MHz Xtal Kbit/sec	External Clock (Resulting bit rate expressed as fraction of external clock)
0	0	0	1000	800	1/2
0	0	1	500	400	1/4
0	1	0	250	200	1/8
0	1	1	125	100	1/16
1	0	0	62.5	50	1/32
1	0	1	31.2	25	1/64
1	1	0	15.6	12.5	1/128
1	1	1	7.81	6.25	1/256

TABLE 2. - PX-984 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	NC
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	Signal Ground
9	Chassis Ground
10	External Clock Input
11	+28 volts Input
12	+28 volts Return
13	Program C
14	Program B
15	Program A

PX-984 SPECIFICATIONS

Power Input. - Nominal input of +28 volts ±4 volts dc is accepted by the Power Supply module.

Reverse Polarity Protection. - A continuous supply of -32 volts dc will not cause permanent damage to the system.

System Grounding. - The signal, power, and chassis grounds are mutually isolated. For most applications, it is recommended to bring each of these system ground points to a single reference, external to the PX-984.

Current Drain. - The current drain depends on the exact system configuration. The ideal range is 250 to 500 milliAmperes.

External Clock. - The external clock input is 0 to +10 ±0.5 volts dc. Frequency shall be between 1.2 to 3.2 MHz. The duty cycle of the external clock must be 50% ±10%. If the external clock inputs are too narrow, the transitions may not be detected.

PX-984 Programming. - 0 = grounded pin, 1 = open pin.

It is important to heat sink the power supply and the entire stack when using the system.

EP-912 END PLATE

The End Plate (Appendix C, page C-5) terminates the stack on the end opposite the Power Supply module and contains the EPROM. Four screws safeguard the EPROM access lid. One EPROM is supplied with each system. The EPROM is removable for programming and reprogramming by unscrewing the 4 Phillips head screw on the access lid. No external connectors exist for this module.

TM-915D TIMER MODULE
P/N 17915100-501

The Timer module (Appendix C, page C-4) receives serial data from the Formatter module then converts this data into the desired output codes. The two fixed output codes serviceable are NRZ-L and Biϕ-L. Several system functions must be selected at the Timer module. Programming is attained by grounding appropriate pins on the external connector. An open programming pin is considered to be a logic "1". The Programming inputs are pulled up to +10 volts through 15 kilohm resistors. The programmable guidelines are number of bits per word, parity select and output code. The number of bits per word are 8, 9 or 10. All words within a system will be the same length. The parity option is either odd or none. The output codes chosen by programming are Biϕ-M, Biϕ-S, NRZ-M, and NRZ-S. Refer to the tables below for external connector pin-out and for programming information.

TABLE 3. - TM-915D EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	NRZ-L Secondary
2	Biϕ-L Secondary
3	Biϕ/NRZ Program
4	NRZ-L Primary
5	Major Frame Sync
6	Biϕ-L Primary
7	1/2X Bit Clock
8	1/4X Bit Clock
9	1/8X Bit Clock
10	1/16X Bit Clock
11	Parity Enable

TABLE 3. - TM-915D EXTERNAL CONNECTOR PIN-OUT (Continued)

PIN	DESCRIPTION
12	Bits/word B3
13	Bits/word B2
14	Bits/word B4
15	Bits/word B1
16	NC
17	NC
18	NC
19	Digital Ground
20	Coded PCM Output
21	Coded PCM Output (Inverted)
22	Mark/Space Program
23	Bit Sync (Inverted)
24	Minor Frame Sync
25	Word Sync
26	Bit Sync
27	2X Bit Clock
28	NC
29	NC
30	NC
31	NC
32	NC
33	NC
34	NC
35	NC
36	NC
37	NC

TABLE 4. - TM-915D WORD LENGTH PROGRAMMING CODES

B4	B3	B2	B1	BITS/WORD
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10

TABLE 5. - TM-915D PARITY SELECT PROGRAMMING CODES

PIN 11	PARITY
0	None
1	Odd

TABLE 6. - TM-915D OUTPUT PROGRAMMING CODES

PIN 3	PIN 22	OUTPUT CODE
0	0	Biϕ-M
0	1	Biϕ-S
1	0	NRZ-M
1	1	NRZ-S

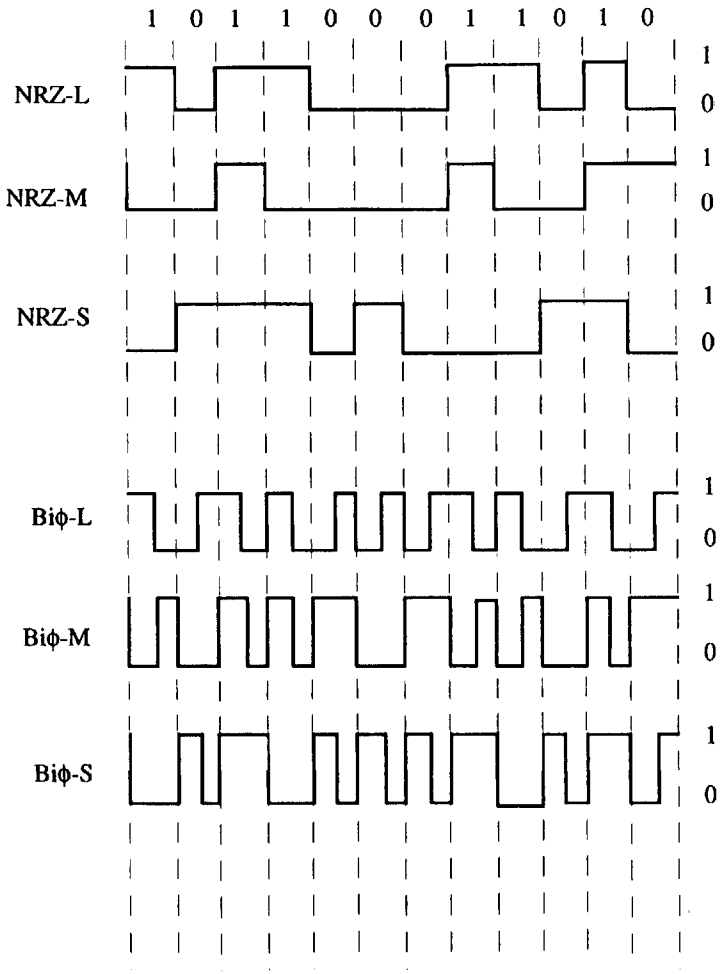
TABLE 7. - TM-915D INPUTS

PIN	DESCRIPTION	INPUT DEVICE
3	Biϕ/NRZ Program	RCA 4030
11	Parity Enable	RCA 4081
12	Bits/word B3	RCA 4029
13	Bits/word B2	RCA 4029
14	Bits/word B4	RCA 4029
15	Bits/word B1	RCA 4029
22	Mark/Space Program	RCA 4030

TABLE 8. - TM-915D OUTPUTS

PIN	DESCRIPTION	OUTPUT DEVICE
1	NRZ-L Secondary	RCA 4049
2	Biϕ-L Secondary	RCA 4049
4	NRZ-L Primary	RCA 4050
5	Major Frame Sync	RCA 4050
6	Biϕ-L Primary	RCA 4050
20	Coded PCM Output	RCA 4049
21	Coded PCM Output (Inverted)	RCA 4049
23	Bit Sync (Inverted)	RCA 4049
24	Minor Frame Sync	RCA 4050
25	Word Sync	RCA 4050
26	Bit Sync	RCA 4050

All outputs are CMOS or low power TTL compatible and operate within 0 to +5 volts dc.



NON-RETURN-TO-ZERO-LEVEL
"One" is represented by one level
"Zero" is represented by the other level

NON-RETURN-TO-ZERO-MARK
"One" is represented by a change in level
"Zero" is represented by no change in level

NON-RETURN-TO-ZERO-SPACE
"One" is represented by no change in level
"Zero" is represented by a change in level

BI-PHASE-LEVEL (SPLIT PHASE)
Level change occurs at center of every bit
"One" is represented by a "one " level with transition to the "zero" level
"Zero" is represented by a "zero" level with transition to the "one" level

BI-PHASE-MARK
Level change occurs at the beginning of every bit period
"One" is represented by a midbit level change
"Zero" is represented by no midbit level change

BI-PHASE-SPACE
Level change occurs at the beginning of every bit period
"One" is represented by no midbit level change
"Zero" is represented by a midbit level change

PCM TELEMETRY TRANSMISSION
Set Pre-Modulation filter cutoff at:
.7 times bit rate for NRZ codes
1.4 times bit rate for Biϕ codes

Figure 5. - PCM waveforms.

FL-919A QUAD FILTER MODULE
P/N 17919020-533

The Quad Filter module (Appendix C, page C-6) contains four linear phase lowpass filters, and an adjustable gain amplifier. The unfiltered serial PCM, from the Timer module, is connected to all four active filter inputs. The output of the applicable filter is connected to the input of the adjustable gain amplifier. The output voltage gain is variable using the potentiometer contained in the Quad Filter module. Access to the potentiometer is accomplished through an aperture in the Formatter module. The FL-919A must be located directly above the FM-918 to permit adjustments.

TABLE 9. - FL-919A EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	Adjustable Amplifier Input
2	Adjustable Amplifier Output
3	Signal Ground
4	Filter #3 Output
5	Filter #1 Output
6	Filter Input
7	NC
8	Filter #4 Output
9	Filter #2 Output

TABLE 10. - FILTER SELECTION (-3 dB cutoff frequencies in KHz)

PART NUMBER	FILTER #1	FILTER #2	FILTER #3	FILTER #4
17919020-533	1120	560	280	140
17919020-534	1400	700	350	175

FL-919A SPECIFICATIONS

Input Voltage. - The input voltage is 0 to +5 volts referenced to digital ground in the Power Supply module.

Output Voltage. - The output voltage is bipolar, adjustable ±0.1 to ±5 volts centered about 0 volt.

Filter Cutoff Frequencies. - A filter for Biϕ–L code is selected by the formula:

$$1.4 \times \text{bit rate} = \text{Upper -3 dB } f_{co}.$$

A filter for NRZ-L , the other common code output by the system, is selected by the formula:

$$0.7 \times \text{bit rate} = \text{Upper -3 dB } f_{co}.$$

Filter Characteristics. - 6-pole Bessel response.

Output Device. - All op-amps are CF-2515.

Output Impedance. - The output impedance is less than 10 ohms.

Roll-Off Slope. - The roll-off slope past the -3dB point is -36 dB/Octave.

FM-918 FORMATTER MODULE
P/N 17918010-559

The Formatter module (Appendix C, page C-7) merges digitized data from the AD-906 and Digital Data modules with frame synchronization words and performs parallel to serial conversion as necessary. The output of the Formatter module is transmitted to the Timer module. The Formatter module sets the threshold voltage level for the PD-929 inputs. The Formatter module must be located directly under the Quad Filter module consequently allowing access to the output gain potentiometer. No external connectors exist at the FM-918, and no hardwire programming is required.

PR-914 PROCESSOR MODULE
P/N 17914010-515

The Processor module (Appendix C, page C-5) contains the control circuit for the system. The PR-914 executes the software entered into the EPROM and controls the timing and operation of the entire system. There is no external connector on this module. The Processor module is connected to an End Plate module by a ribbon cable. The End Plate module terminates the physical stack on the opposite end of the Power Supply module, and contains the Intersil IM6654AMJG UV EPROM. Four screws secure the EPROM access lid. The EPROM is not soldered into the End Plate module, and can be removed for programming and reprogramming. There is no external connector on the Programmer module.

PROCESSOR CONTROL & PROGRAMMING

The Processor module executes the program entered into the 512 x 8 EPROM to accomplish the following functional capabilities. Multiple subframes with subcommutation rates up to 1/32 of the minor frame rate are possible. The maximum minor frame length is about 256 words and the maximum subframe depth is 32 subframes. The combination of these maximums in one data format is not permissible. Actual format sizes are a trade-off between long minor frames and deep subcommutations. The rate of supercommutation is limited by the processor; however, supercommutation is limited by the size of the EPROM. Lastly, frame and subframe synchronization words may be located in any position of the format in any bit pattern. It is required to have a subframe identification counter word precede any subcommutated word.

Two memory locations MSH (Most Significant Half) and LSH (Least Significant Half) of the 512 x 8 EPROM are required for each minor frame word, independent of the number of minor frames per major frame. In general, data which is transmitted during BYTE 1 is retrieved from the MSH of the EPROM memory, i.e., address locations 100-1FF. Data which is transmitted during BYTE 2 is retrieved from the LSH of the EPROM memory, i.e. address locations 000-0FF. The format size is limited by the size of the EPROM. The maximum number of input channels is near 240, depending on the format configuration. Ten bits of bi-level parallel inputs are considered one data channel for a 10-bit system.

A machine cycle of the processor is carried out within one PCM word period. The machine cycle is divided into seven clock periods, T0-T6. The special instruction codes, recognized by the processor and used to program the system, can be used as input data channel addresses provided these channels are subcommutated. This is possible because --after the T2 clock period -- the instruction decoder is ineffective.

Figure 6 illustrates the block diagram of the Processor module. There is no external connector on this module.

PR-914 Processor Control Sequence

The following discussion covers the seven machine cycles, T0-T6, required by the processor to execute the program that is stored in the EPROM. The machine code is given for each machine cycle for each type of code that the processor may encounter followed by a comment explaining the machine code. (N) represents the contents of the EPROM.

T0: PC <--- N; Program Counter updates to N

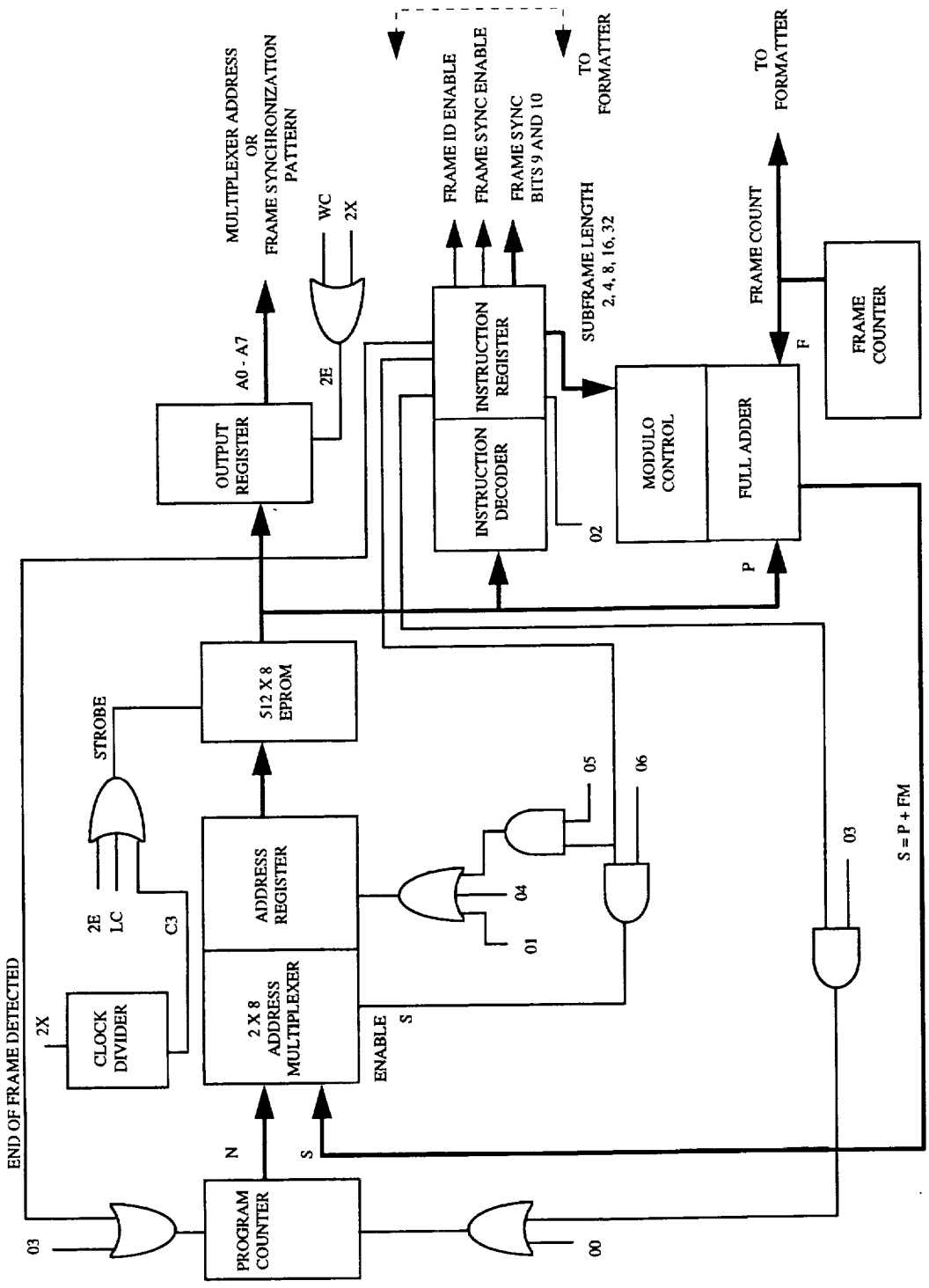


Figure 6. - Processor block diagram.

T1: AR <--- N; Address Register is loaded with N

T2: IR <--- (N); Instruction Register is loaded with the contents of N

Now the instruction decoder examines the contents of N.

Contents of N is not an instruction. - Nothing important happens until T6.

T6: OR <--- (LSH) Data; Output Register is loaded with data channel address
(MSH) Data; Output Register is also loaded with data channel address
Strobe circuitry determines which half of the memory is to be transmitted.

Contents of N is an instruction. -

T3: PC <--- N+1; Program Counter is updated to N+1

T4: AR <--- N+1; Address Register is loaded with N+1

Subcommutated data instruction detected:

T5: AR <--- (N+1) + (FC); Address Register is loaded with the sum of the contents of N+1 and the frame counter

T6: OR <--- AR; Output Register is loaded with the subcommutated channel address

(N+1) is the initial memory address for that subframe. This instruction contains indirect address information.

Frame ID word instruction detected:

PCM Output <--- Status of the frame counter

A command is issued to the Formatter module to transfer the status of the frame counter to the PCM output.

(N+1), the contents of register N+1, contains the subframe counter reset information. This information is used to reset the frame counter as appropriate. (N+1) is composed of the following:

The three MSB's are ones and the five LSB's are a binary representation of the number of minor frames per major frame.

Frame synchronization word detected:

This instruction is used by three to five percent of major frame words but can be used as often as desired and carry any information desired. (N+1) is the eight MSB's of the frame synchronization word. For 10-bit systems, the two LSB's are included as the two LSB's of the frame synchronization word instruction.

T6: OR <--- (N+1);	Output Register is loaded with the contents of (N+1). (Eight MSB's of frame synchronization word.) Then a command is sent to the Formatter module to transfer the complete frame synchronization word to the PCM output

End of Frame (EOF) detected:

This instruction is the exception to the rule stated in the paragraph headed "Contents of N is an instruction".

T3: PC <--- 0; Program Counter resets to zero

The contents of memory location 0 in the EPROM are the eight MSB's of the frame synchronization word. For nine and ten bit systems, the two LSB's of the End of Frame instruction are the LSB's of the frame synchronization word. This instruction marks the end of the major frame and outputs the first synchronization word.

Refer to Table 11 for the EPROM instruction codes.

Programming Equipment

The IM6654AMJG EPROM can be programmed using any commercially available EPROM programmers.

Instruction Codes

The codes below must be used only for instruction. Any Analog Multiplexer module enabled by 111XXXXX must not use these fourteen codes if the multiplexer is a prime frame multiplexer. If the multiplexer is a subcommutated multiplexer, it is permissible to use these codes.

Table 11. - EPROM INSTRUCTION CODES

INSTRUCTION	A7	A6	A5	A4	A3	A2	A1	A0	HEX	COMMENTS
	1	1	1	1	1	1	1	1	FF	Bits A1, A0 are stored for
End of Frame	1	1	1	1	1	1	1	0	FE	insertion into bit 9 and 10
	1	1	1	1	1	1	0	1	FD	position of first frame
	1	1	1	1	1	1	0	0	FC	sync word for 9 and 10 bit systems.
	1	1	1	1	1	0	1	1	FB	Bits A1, A0 are stored for
Frame Sync Word	1	1	1	1	1	0	1	0	FA	insertion into bit 9 and 10
	1	1	1	1	1	0	0	1	F9	position of first frame
	1	1	1	1	1	0	0	0	F8	sync word for 9 and 10 bit systems.
Frame ID Word	1	1	1	1	0	1	1	1	F7	
									F6	RESERVED Do Not Use
									F5	RESERVED Do Not Use
	1	1	1	1	0	1	0	0	F4	32 Deep Subframe
	1	1	1	1	0	0	1	1	F3	16 Deep Subframe
Subcommutated Data Word	1	1	1	1	0	0	1	0	F2	8 Deep Subframe
	1	1	1	1	0	0	0	1	F1	4 Deep Subframe
	1	1	1	1	0	0	0	0	F0	2 Deep Subframe

Table 12. - HEX CODES ADDRESS LOCATIONS

TYPE	FORMAT (HEX)	EPROM ADDRESS LOCATION	REMARKS
Instruction Code	F0 thru FF	000 thru 0FF	Used to assert Frame Sync, SFID, Subcommutation or EOF.
Jump to Address	XX	000 thru 0FF	Used in conjunction with subcommutation code.
Data Code (BYTE 1 MSH)	XX	100 thru 1FF	The data code used shall be the same code as the data code selected in BYTE 2 (LSH).
Data Code (BYTE 2 LSH)	XX	000 thru 0FF	Used to program Frame Sync Words, SFID Depth; used to enable specific data inputs.

Programming the System

Obtain the PCM format drawing. An example format drawing is given in Table 13.

Choose the multiplexer types and quantities of each to satisfy mission requirements.

Assign multiplexer enable addresses from the available codes. Refer to the specific module section and Table 11 to insure selecting allowable codes.

Assign the input channels to be used on each multiplexer.

Convert the binary codes of the input channels to hexadecimal codes.

Convert the frame synchronization word patterns to hexadecimal and the subframe ID instruction word if subcommutation is to be used.

Convert instructions necessary for the format configuration to hexadecimal.

The entire format must be programmed through the End of Frame instruction before assigning the indirect addresses. Generate the indirect addresses for the subcommutated data if subcommutation is used. The indirect addresses follow the subcommutated data word instructions in consecutive EPROM memory locations. The indirect addresses may then be assigned to the blank EPROM memory locations.

A sample payload configuration is included in Appendix A. Refer to that section for further information. Also refer to the programming codes section in Appendix B for each module involved.

Programming Exceptions and Examples

For subframe depths other than binary multiples, the instruction for 32 deep subframe is programmed. The fourteen codes listed in Table 11 must be used for instruction only. Any Analog Multiplexer module enabled by 111XXXXX code must be a subcommutated multiplexer. The instruction register, which recognizes EPROM instruction codes, is ineffective after machine cycle T2. Therefore, this group of codes can be used as a subcommutated multiplexer address or a system instruction.

End of Frame and Frame Synchronization Programming Example

Documentation below steps through a typical EPROM program starting with the End of Frame instruction and proceeding through the subframe ID instruction. Examples are given for EPROM address locations, address contents and PCM output. The End of Frame instruction is started at a chosen location in the EPROM assumed to be at the end of the program. Refer to Table 13 for sampling format used in the following programming example.

End of Frame

As the last data word of each frame is encountered in the MMP-900, it is necessary to proceed to the first data word of the next data frame. This program jump is achieved through the use of the End of Frame (EOF) instruction. See Table 11 for EOF instruction code. The EOF instruction performs several tasks:

- Accomplishes program jump from last data word of one frame to the first data word of the next frame.
- Enables MMP-900 to transmit the first frame synchronization word, FS1.
- Determines the two LSB's of FS1 depending on which one of four EOF instructions is used.
- Asserts frame synchronization test points outputs.

Frame Synchronization Words

FS1 and FS2 represent the first and second frame synchronization words respectively. In the example, the synchronization codes were taken from Barker Code Patterns. To determine the frame synchronization hexadecimal codes to be used in the EPROM, the following disassembly procedure is to be used.

Table 13. - SAMPLE FORMAT

FS1	FS2	SFID	A1	A2	B1
					B2
					B1
					B2
					B1
					B2
					B1
					B2

Bit Rate = 800 kbps, Word Rate = 80 kwps
FS1 - 1110110111 - Frame Synchronization Word
FS2 - 1000100000 - Frame Synchronization Word
SFID - 8 Deep - Subframe Identification Counter Word
A1, A2 - Analog Data channels at Main Frame Rate 13,333.33 sps
B1, B2 - Subcommutated Digital Data Channels at 6,666.66 sps

Determination of Frame Synchronization Hexadecimal Codes

	FS1			FS2		
Binary Barker	1110	1101	11	1000	1000	00
Hex Data Code	E	D		8	8	
2 LSB of FS Instruction Code			11			00

The data code for FS1 is "ED Hex" and is always placed at address 000. This is followed by the instruction code for FS2. "F8 Hex" is the appropriate instruction code because the last two bits of FS2 are "00 Hex". The data code for FS2 is "88 Hex" and is placed at address 002, immediately following the instruction code.

Note that the instruction code for FS1 has not yet appeared. It will be entered by the End of Frame (EOF) instruction later in the program. Locations 100-102 can be left blank as the MSH of the EPROM is not accessed during MMP-900 operation.

HEX ADDRESS	PROM CODE	FUNCTION	HEX ADDRESS	PROM CODE	FUNCTION
000	ED	FS1	100	FF	
001	F8	Frame Sync Instruction	101	FF	
002	88	FS2	102	FF	

In cases requiring more than two frame synchronization words, the appropriate Barker Code Pattern is selected and disassembled as before, and the hexadecimal data codes are positioned in the EPROM as before.

Frame synchronization instructions must always preceed the hexadecimal data codes. Note that the blank condition in the EPROM is "FF Hex".

SFID Word

The subframe identification word (SFID) will usually follow the last frame synchronization word in the data format. For a typical data format, the SFID word immediately follows FS2. Thus, the SFID instruction code ("F7 Hex")

and its associated subframe depth code (refer to Table 14 for subframe depth codes) are placed immediately following the data code for FS2.

HEX ADDRESS	PROM CODE	FUNCTION	HEX ADDRESS	PROM CODE	FUNCTION
000	ED	FS1	100	FF	
001	F8	Frame Sync Instruction	101	FF	
002	88	FS2	102	FF	
003	F7	SFID Instruction	103	FF	
004	07	SFID 8 Deep	104	FF	

The SFID word need not be placed immediately after the last frame synchronization word. Indeed, it can be placed anywhere within the data format, with the following restriction in mind:

- If the SFID word does not immediately follow the last frame synchronization word, then no subcommutated data words can be placed between the last frame synchronization word and the SFID word. Doing so will cause sampling errors in the first minor data frame.

Subcommutated Data Words --- 2-Deep

Word 6 of the typical data format is a subcommutated data word. The procedure for programming subcommutated words is as follows:

1. Assert the appropriate subcommutation instruction word according to the required depth.

2. Then, enter the "Jump to Address". This allows the MMP-900 to enter a subroutine mode where it will fetch hexadecimal data codes from some reserved space in memory. It will execute this fetch in accordance with the status of an internal counter called a "Subframe Counter" (SFC).

   For example, during the first minor data frame, the SFC is reset to "00000 Bin". This is then added to the "Jump to Address" which moves the entire program sequence into a new area of memory. After execution, the program automatically returns to its normal operating area within memory.

   However, during the second minor data frame, the SFC has been incremented to "00001 Bin". When the MMP-900 then encounters the subcommutated instruction, the "Jump to Address" is added with the

new SFC contents, resulting in a program jump to a different reserved memory area than before. This arrangement allows for a very efficient utilization of available memory space.

3. The final step in programming is to fill up the before mentioned "Jump to Address" area with the appropriate hexadecimal data codes.

   An example will help to render this procedure intelligible.

Word 6 of the typical data format calls for a 2-deep subcommutated word. The appropriate instruction for this is "F0 Hex" as found in Table 11. Next, the user selects some area within the LSH of the EPROM (Address 000 thru 0FF) which will not normally be used by the main body of the EPROM program. For this example, we need to set aside two "Jump to Address" locations (because the subcommutation is 2-deep). We will thus arbitrarily assign address 020 as being the "Jump to Address". We will then place the hexadecimal data code and for B1 (CM-922PB) at address locations 020 and 120 respectively. Likewise, we place the hexadecimal data code for B2 (CM-922PB) at address locations 021 and 121 respectively.

Note that, as before, the MSH address locations associated with the instruction code and "Jump to Address" are left blank.

HEX ADDRESS	PROM CODE	FUNCTION	HEX ADDRESS	PROM CODE	FUNCTION
000	ED	FS1	100	FF	
001	F8	Frame Sync Instruction	101	FF	
002	88	FS2	102	FF	
003	F7	SFID Instruction	103	FF	
004	07	SFID 8 Deep	104	FF	
005	20	A1	105	20	
006	21	A2	106	21	
007	F0	Instruction: 2-Deep	107	FF	
008	20	Jump to 020	108	FF	
020	10	B1	120	10	B1
021	11	B2	121	11	B2

Table 14. - SUBFRAME DEPTH CODES

REQUIRED SUBFRAME DEPTH	SUBFRAME DEPTH CODE FORMAT HEX	SUBFRAME DEPTH CODE FORMAT BINARY MSB TO LSB
2	01	00000001
3	02	00000010
4	03	00000011
5	04	00000100
6	05	00000101
7	06	00000110
8	07	00000111
9	08	00001000
10	09	00001001
11	0A	00001010
12	0B	00001011
13	0C	00001100
14	0D	00001101
15	0E	00001110
16	0F	00001111
17	10	00010000
18	11	00010001
19	12	00010010
20	13	00010011
21	14	00010100
22	15	00010101
23	16	00010110
24	17	00010111
25	18	00011000
26	19	00011001
27	1A	00011010
28	1B	00011011
29	1C	00011100
30	1D	00011101
31	1E	00011110
32	1F	00011111

Subcommutated Data Words --- General

To accomodate subcommutated data words in general, the following procedure is used:

1. Select appropriate subcommutation instruction according to required subcommutation depth.

2. Select a suitable area in memory away from the main body of the program (i.e., after the EOF instruction). If the subcommutation is "N" deep, then there must be at least "N" EPROM locations reserved for use with the subcommutation instruction. The first address location of this reserved area called the "Jump to Address" is placed immediately after the subcommutation instruction.

End of Frame Instruction

The first frame synchronization word of the system has as its instruction code the End of Frame (EOF) instruction which resets the counter and sets up the PR-914 for the first frame synchronization word of the frame. The instruction code for EOF will be written into the last minor frame address of the EPROM. See Table 11 for proper EOF instruction code. In the example sampling format, the first frame synchronization code is "ED Hex". The instruction code "FF Hex" is to be used since the last two bits of FS1 are 11 for a 10-bit frame synchronization code.

HEX ADDRESS	PROM CODE	FUNCTION	HEX ADDRESS	PROM CODE	FUNCTION
000	ED	FS1	100	FF	
001	F8	Frame Sync Instruction	101	FF	
002	88	FS2	102	FF	
003	F7	SFID Instruction	103	FF	
004	07	SFID 8 Deep	104	FF	
005	20	A1	105	20	
006	21	A2	106	21	
007	F0	Instruction: 2-Deep	107	FF	
008	20	Jump to 020	108	FF	
009	FF	EOF Instruction	109		

EPROM Removal/Insertion

The MMP-900 EPROM is an Intersil IM6654AMJG UV erasable PROM. It is physically located inside the End Plate module beneath the micro PCM labeled access plate. The access plate is secured with four # 1-72 x 1/8 LG FLTHD screws which can be removed with an Xecelite P-12-S phillips head screwdriver or equivalent. Note that these four screws DO NOT use any Locktite compound.

After removing the access plate, the EPROM can be removed from its socket by using an OK Model EX-1 dip/IC extractor or equivalent. Be sure the power to the unit is turned off and the operating personnel, tools, and other equipment are properly grounded and static protected before attempting EPROM removal.

The window of the EPROM is covered with a dot of teflon tape which is opaque to UV light. This prevents degradation of EPROM contents due to exposure to ambient light. This dot must be removed before attempting EPROM deletion, and must be reinstalled after completing EPROM erasure.

AD-906 SAMPLE & HOLD AND ANALOG TO DIGITAL CONVERTER P/N 17906030-520

The Sample & Hold and Analog to Digital Converter module (Appendix C, page C-8) provides a high input impedance to the PAM bus. The hold amplifier provides a low output impedance to the analog to digital conversion circuit. The Analog to Digital Converter module digitizes each analog word into a 10-bit binary code by method of successive approximations. The output is normalized for 0 to +5 volts. The AD-906 does not have an external connector and no programming is required.

AD-906 SPECIFICATIONS

Accuracy. - The accuracy of the analog to digital conversion process is ±1/2 of the LSB.

Conversion Method. - The conversion process is by method of successive approximations.

Bits per Word. - The number of bits per word is ten.

Coding. - The coding of the AD-906 module is offset binary as follows, for a 10-bit system:

Input	Binary Output	Decimal Equivalent
≥ + 5 volts over scale	1111111111	1023
+ 5 volts full scale	1111110100	1012
+ 2.5 volts mid scale	1000000000	512
0 volts zero scale	0000001100	12
≤ - 0.055 volts under scale	0000000000	0

Conversion Time. - The conversion is 4.5 ± 0.5 microseconds.

Bit Weight Sensitivity. - 5 millivolts per count for a 10-bit system.

DETAILED DESCRIPTION OF THE PCM ENCODER SYSTEM GROUP II MODULES

MP-901 32-CHANNEL HIGH LEVEL MULTIPLEXER P/N 17901050-509

The Analog Multiplexer module (Appendix C, page C-9) accepts 32 individual analog inputs. The system allows for up to seven analog modules. This provides 224 analog input channels per system as a maximum. Programming pins 18, 19 and 36 found on this module's external connector are utilized to give each module a unique address.

Programming is accomplished by grounding appropriate pins. Programming pins are pulled up to +5 volts through 10 kilohm resistors.

TABLE 15. - MP-901 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	Channel 1 Input
2	Channel 3 Input
3	Channel 5 Input
4	Channel 7 Input
5	Channel 9 Input
6	Channel 11 Input
7	Channel 13 Input
8	Channel 15 Input
9	Channel 17 Input
10	Channel 19 Input
11	Channel 21 Input
12	Channel 23 Input
13	Channel 25 Input
14	Channel 27 Input
15	Channel 29 Input
16	Channel 31 Input
17	Analog Ground
18	Program A6
19	Program A7
20	Channel 2 Input
21	Channel 4 Input
22	Channel 6 Input
23	Channel 8 Input
24	Channel 10 Input
25	Channel 12 Input

TABLE 15. - MP-901 EXTERNAL CONNECTOR PIN-OUT (Continued)

PIN	DESCRIPTION
26	Channel 14 Input
27	Channel 16 Input
28	Channel 18 Input
29	Channel 20 Input
30	Channel 22 Input
31	Channel 24 Input
32	Channel 26 Input
33	Channel 28 Input
34	Channel 30 Input
35	Channel 32 Input
36	Program A5
37	NC

TABLE 16. - MP-901 EPROM PROGRAMMING CODE

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
M	M	M	C	C	C	C	C

M = MODULE CODE {(1 thru 7) - 1}
C = CHANNEL CODE {(1 thru 32) - 1}

i.e. 01000110 = Module 3, Channel 7

MP-901 SPECIFICATIONS

Input Voltage. - The input voltage is 0 to +5 volts dc referenced to analog ground on the MP-901 module connector.

Input Impedance. - The input impedance is 10 Megohms shunted by 300 picofarads capacitor during maximum sampling and non-sampling periods with power on.

Input Capacitance. - The input capacitance is 10 picofarads plus 30 picofarads per analog module within the system.

Backcurrent. - The maximum backcurrent is 300 nA during sampling and non-sampling intervals.

Crosstalk. - Crosstalk depends upon system configuration and bit rate. A typical system will have less than 0.1% of full scale maximum crosstalk error.

Overvoltage Protection. - The data inputs are over-voltage protected for voltages of ±35 volts. (It is recommended no more than 20 inputs per multiplexer be overvoltaged simultaneously.)

TABLE 17. - MP-901 EPROM PROGRAMMING CODES (Broadened)

CHANNEL	PIN	A7	A6	A5	A4	A3	A2	A1	A0
1	1	M	M	M	0	0	0	0	0
2	20	M	M	M	0	0	0	0	1
3	2	M	M	M	0	0	0	1	0
4	21	M	M	M	0	0	0	1	1
5	3	M	M	M	0	0	1	0	0
6	22	M	M	M	0	0	1	0	1
7	4	M	M	M	0	0	1	1	0
8	23	M	M	M	0	0	1	1	1
9	5	M	M	M	0	1	0	0	0
10	24	M	M	M	0	1	0	0	1
11	6	M	M	M	0	1	0	1	0
12	25	M	M	M	0	1	0	1	1
13	7	M	M	M	0	1	1	0	0
14	26	M	M	M	0	1	1	0	1
15	8	M	M	M	0	1	1	1	0
16	27	M	M	M	0	1	1	1	1
17	9	M	M	M	1	0	0	0	0
18	28	M	M	M	1	0	0	0	1
19	10	M	M	M	1	0	0	1	0
20	29	M	M	M	1	0	0	1	1
21	11	M	M	M	1	0	1	0	0
22	30	M	M	M	1	0	1	0	1
23	12	M	M	M	1	0	1	1	0
24	31	M	M	M	1	0	1	1	1
25	13	M	M	M	1	1	0	0	0
26	32	M	M	M	1	1	0	0	1
27	14	M	M	M	1	1	0	1	0
28	33	M	M	M	1	1	0	1	1
29	15	M	M	M	1	1	1	0	0
30	34	M	M	M	1	1	1	0	1
31	16	M	M	M	1	1	1	1	0
32	35	M	M	M	1	1	1	1	1

PD-929 PARALLEL DIGITAL DATA MULTIPLEXER
P/N 17929010-504

The Parallel Digital Data Multiplexer module (Appendix C, page C-10) accepts up to 30 individual data bits, for a total of three 10-bit words. The system will accept up to sixteen PD-929 modules for a total of forty eight 10-bit words. The module's addresses are assigned by programming pins on the external connector. The programming is achieved by grounding appropriate pins or by utilizing a logic interface to determine the state of the programming pins. A positive logic system is used. An ungrounded programming pin will be interpreted as a logic "1". Programming pins are pulled up to +10 volts through 30 kilohms. A data enable signal output is available for two of the three parallel word inputs. Refer to Figure 7 for PD-929 interface timing information.

Table 18. - PD-929 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	Word 3 Bit 1
2	Word 1 Bit 1
3	Word 2 Bit 2
4	Word 3 Bit 3
5	Word 1 Bit 3
6	Word 2 Bit 4
7	Word 3 Bit 5
8	Word 1 Bit 5
9	Word 2 Bit 6
10	Word 3 Bit 7
11	Word 1 Bit 7
12	Word 2 Bit 8
13	Word 3 Bit 9
14	Word 1 Bit 9
15	Word 2 Bit 10
16	Program A3
17	Program A2
18	Enable Word 1
19	Digital Ground
20	Word 2 Bit 1
21	Word 3 Bit 2
22	Word 1 Bit 2
23	Word 2 Bit 3
24	Word 3 Bit 4
25	Word 1 Bit 4

Table 18. - PD-929 EXTERNAL CONNECTOR PIN-OUT (Continued)

PIN	DESCRIPTION
26	Word 2 Bit 5
27	Word 3 Bit 6
28	Word 1 Bit 6
29	Word 2 Bit 7
30	Word 3 Bit 8
31	Word 1 Bit 8
32	Word 2 Bit 9
33	Word 3 Bit 10
34	Word 1 Bit 10
35	Enable Word 2
36	Program A5
37	Program A4

Parallel input bit 1 is the first bit transmitted.

TABLE 19. - PD-929 EPROM PROGRAMMING CODE

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
0	0	M	M	M	M	C	C

M = MODULE CODE {(1 thru 16) - 1}
C = CHANNEL CODE {(1 thru 3) - 1}

i.e. 00000100 = Module 2, Channel 1

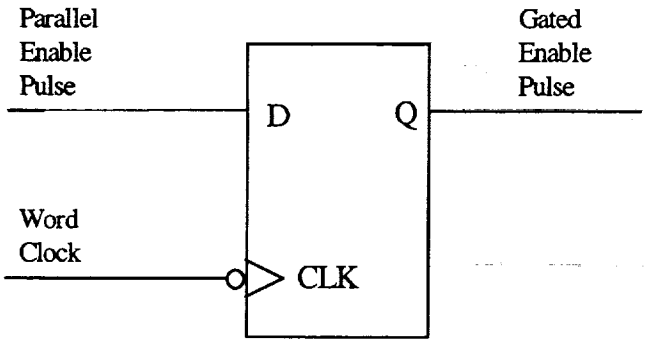
PD-929 SPECIFICATIONS

Input Voltage. - The input voltage is -35 volts to 2 volts dc referenced to digital ground (recognized as a logic "0") and +3 volts to +35 volts dc referenced to digital ground (recognized as a logic "1"). Voltages outside this range will cause permanent damage to the module. Open circuit is detected as a logic "0".

Input Impedance. - The input impedance is 100 kilohms minimum.

TABLE 20. - PD-929 EPROM PROGRAMMING CODES (Broadened)

CHANNEL	PIN	A7	A6	A5	A4	A3	A2	A1	A0
1	2, 5, 8, 11, 14, 22, 25, 28, 31, 34	0	0	M	M	M	M	0	0
2	3, 6, 9, 12, 15, 20, 23, 26, 29, 32	0	0	M	M	M	M	0	1
3	1, 4, 7, 10, 13, 21, 24, 27, 30, 33	0	0	M	M	M	M	1	0



The interface circuit that is recommended when the parallel enable pulses are used is illustrated in the figure above. This circuit will suppress any spurious voltage spikes.

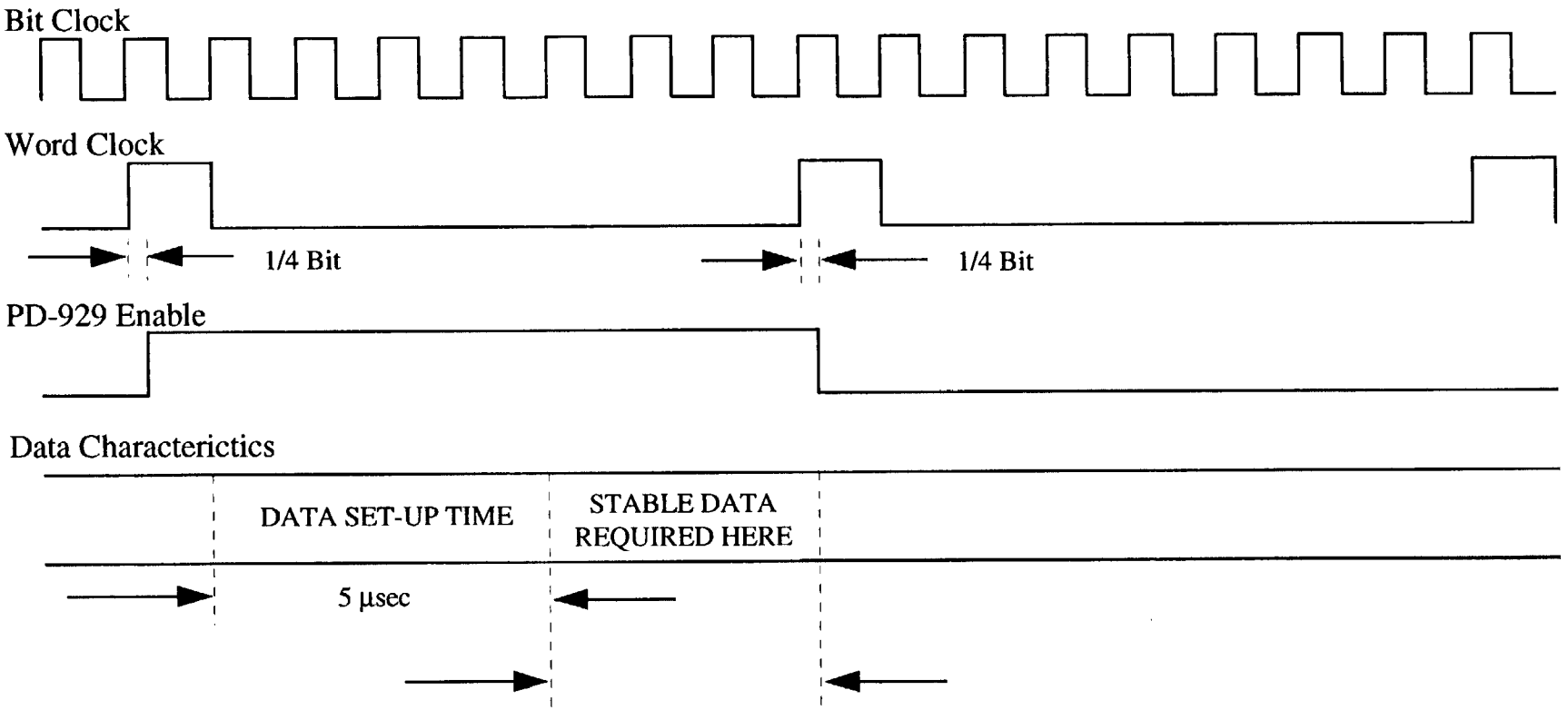


Figure 7. - PD-929 timing diagram.

SD-924 SERIAL DIGITAL DATA MULTIPLEXER
P/N 17924010-505

The Serial Digital Data Multiplexer module (Appendix C, page C-11) accepts 8 individual serial channel inputs. The system will accept up to four SD-924 modules, for a total of 32 individual serial data channels. Each serial data input channel has three interfacing signals available. These signals are: inverted load pulse, enable pulse, and gated bit clock. Contiguous serial data words are possible. **A serial data word must not be sampled immediately following a frame synchronization word or subframe counter word**. Refer to Figure 8 for SD-924 timing information. The module's addresses are assigned by grounding appropriate pins. An open programming pin is interpreted as a logic "1". The module's word length programming pins are pulled up to +5 volts through 20 kilohm resistors. For programming codes, see Table 22.

TABLE 21. - SD-924 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	Serial Channel 5
2	Serial Channel 7
3	Gated Clock 8
4	Gated Clock 6
5	Gated Clock 4
6	Gated Clock 2
7	Serial Channel 4
8	Serial Channel 2
9	PROG WL1
10	Digital Ground
11	PROG WL2
12	Inverted Load 4
13	Inverted Load 2
14	Enable 8
15	Enable 6
16	Enable 4
17	Enable 3
18	Inverted Load 6
19	Inverted Load 8
20	Serial Channel 6
21	Serial Channel 8
22	Gated Clock 7
23	Gated Clock 5
24	Gated Clock 3

TABLE 21. - SD-924 EXTERNAL CONNECTOR PIN-OUT (Continued)

PIN	DESCRIPTION
25	Gated Clock 1
26	Serial Channel 3
27	Serial Channel 1
28	Program A4
29	Program A5
30	Inverted Load 3
31	Inverted Load 1
32	Inverted Load 7
33	Enable 7
34	Enable 5
35	Enable 2
36	Enable 1
37	Inverted Load 5

TABLE 22. - SD-924 EPROM PROGRAMMING CODE

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
0	0	M	M	X	C	C	C

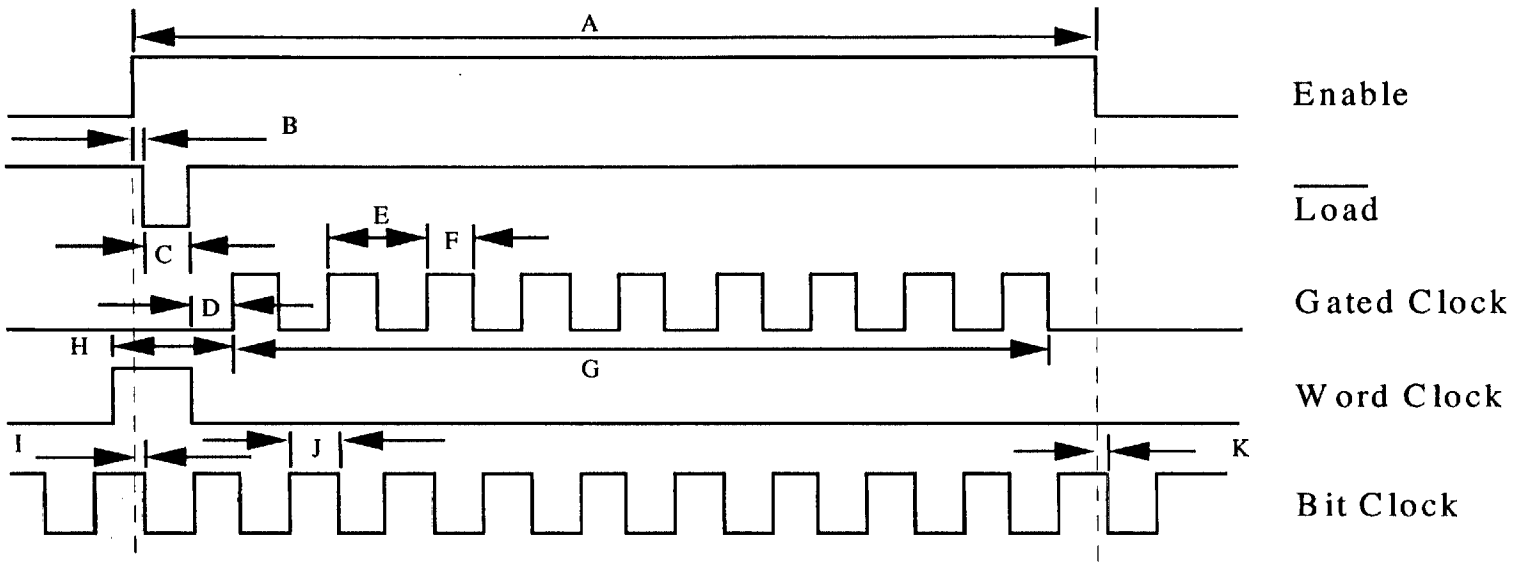
M = MODULE CODE {(1 thru 4)- 1}
C = CHANNEL CODE {(1 thru 8)- 1}
X = DON'T CARE CONDITION

i.e. 00100110 = Module 3, Channel 7

TABLE 23. - SD-924 WORD LENGTH PROGRAMMING CODES

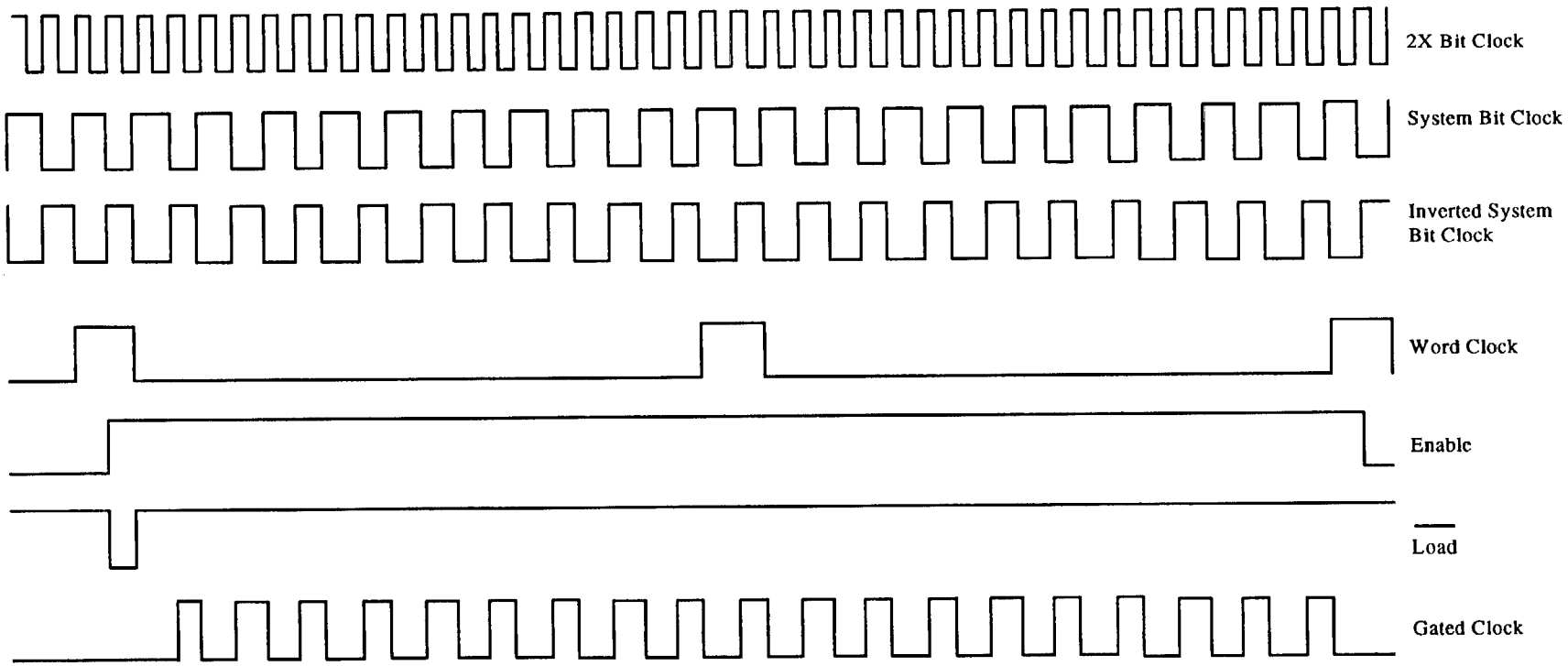
PROG WL1 PIN 9	PROG WL2 PIN 11	BITS/WORD
0	1	8
1	0	9
0	0	10

The word length program must be the same as the word length programmed on the TM-915D. This program doesn't necessarily have to match the number of bits in the actual data word, which may be less than the word length of the PCM system.



SYMBOL	TYPICAL TIME
A	10 * BIT PERIOD * NO. OF SERIAL WORDS
B	50 TO 100 NSEC
C	1/2 BIT PERIOD
D	1/2 BIT PERIOD
E	1 BIT PERIOD
F	1/2 BIT PERIOD
G	8 1/2 BIT PERIOD
H	1 1/2 BIT PERIOD
I	100 NSECS
J	1/2 BIT PERIOD
K	100 NSECS

Figure 8. - SD-924 timing diagram.



Notes:

1. Multiple contiguous words are possible with restrictions of EPROM size and not placing serial words contiguously with synchronization words.

2. Only one inverted load and one extended enable pulse are generated during a contiguous serial data channel.

Figure 9. - SD-924 contiguous data timing diagram.

Input Voltage. - -1.5 volts to +0.9 volts dc referenced to digital ground is recognized as a logic "0" and +3.15 volts to +6.5 volts dc referenced to digital ground is recognized as a logic "1".

Bit Alignment. - The first bit shifted into the PCM encoder will be the first bit transmitted.

TABLE 24. - SD-924 EPROM PROGRAMMING CODES (Broadened)

CHANNEL	PIN	A7	A6	A5	A4	A3	A2	A1	A0
1	27	0	0	M	M	X	0	0	0
2	8	0	0	M	M	X	0	0	1
3	26	0	0	M	M	X	0	1	0
4	7	0	0	M	M	X	0	1	1
5	1	0	0	M	M	X	1	0	0
6	20	0	0	M	M	X	1	0	1
7	2	0	0	M	M	X	1	1	0
8	21	0	0	M	M	X	1	1	1

M = MODULE CODE {(1 thru 4)- 1}
C = CHANNEL CODE {(1 thru 8)- 1}
X = DON'T CARE CONDITION

i.e. 00110110 = Module 4, Channel 7

TABLE 25. - SD-924 INPUTS

PIN	DESCRIPTION	INPUT DEVICE
1	Serial Channel 5	54HC251
2	Serial Channel 7	54HC251
7	Serial Channel 4	54HC251
8	Serial Channel 2	54HC251
20	Serial Channel 6	54HC251
21	Serial Channel 8	54HC251
26	Serial Channel 3	54HC251
27	Serial Channel 1	54HC251

TABLE 26. - SD-924 OUTPUTS

PIN	DESCRIPTION	INPUT DEVICE
3	Gated Clock 8	54HC259
4	Gated Clock 6	54HC259
5	Gated Clock 4	54HC259
6	Gated Clock 2	54HC259
22	Gated Clock 7	54HC259
23	Gated Clock 5	54HC259
24	Gated Clock 3	54HC259
25	Gated Clock 1	54HC259
12	Inverted Load 4	54HC138
13	Inverted Load 2	54HC138
18	Inverted Load 6	54HC138
19	Inverted Load 8	54HC138
30	Inverted Load 3	54HC138
31	Inverted Load 1	54HC138
32	Inverted Load 7	54HC138
37	Inverted Load 5	54HC138
14	Enable 8	54HC259
15	Enable 6	54HC259
16	Enable 4	54HC259
17	Enable 3	54HC259
33	Enable 7	54HC259
34	Enable 5	54HC259
35	Enable 2	54HC259
36	Enable 1	54HC259

CM-922PB DUAL COUNTER/ACCUMULATOR
P/N 17922003-506

The Counter/Accumulator module (Appendix C, page C-12) counts pulses, and accepts 2 individual counter channel inputs. The system will accept up to 19 CM-922PB modules, for a total of 38 individual counter data channels. The actual number of active channels is determined by the program entered in the EPROM. Each Counter module must be assigned a unique address. This is done by grounding pins on the external. Open programming pins will be interpreted as a logic "1". Module address programming pins are pulled up to +10 volts through 20 kilohm resistors. For programming codes, see Table 28.

Each Counter module includes two 10-bit counters/accumulators. Each Counter module may be used in either single or dual counter mode. Single counter mode will provide a 16, 18, or 20-bit counter word. Dual counter mode will provide two counter words of equal word length, 8, 9, or 10 bits per word. When using single counter mode, use input #1 for data input, and program channel #2 in the EPROM to read out before channel #1. Channel #2 contains the MSB. Word length is programmable at the external connector of this module. See Figure 9 for timing information.

TABLE 27. - CM-922PB EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	NC
2	NC
3	Program A1
4	Input #1
5	Input #2
6	PROG WL1
7	Reset Input #1
8	NC
9	Strobe Output #1
10	Strobe Output #2
11	PROG WL2
12	Reset Input #2
13	Program A4
14	Program A5
15	Complement Reset
16	Mode Select
17	Program A2
18	Program A3
19	Digital Ground

TABLE 27. - CM-922PB EXTERNAL CONNECTOR PIN-OUT (Continued)

PIN	DESCRIPTION
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC
26	NC
27	NC
28	NC
29	NC
30	NC
31	NC
32	NC
33	NC
34	NC
35	NC
36	NC
37	NC

TABLE 28. - CM-922PB EPROM PROGRAMMING CODE

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
0	0	M	M	M	M	M	C

M = MODULE CODE {(1 thru 19)- 1}
C = CHANNEL CODE {(1 or 2)- 1}

i.e. 00000110 = Module 4, Channel 1

TABLE 29. - CM-922PB WORD LENGTH PROGRAMMING CODES

PROG WL1 PIN 6	PROG WL2 PIN 11	BITS/WORD
1	1	8
0	1	9
0	0	10

TABLE 30. - CM-922PB MODE SELECT PROGRAMMING CODES

MODE SELECT PIN 16	COUNTER MODE
0	Single
1	Dual

TABLE 31. - CM-922PB RESET MODE PROGRAMMING CODES

RESET INPUT #1 PIN 7	RESET INPUT #2 PIN 12	COMPLIMENT RESET PIN 15	RESET MODE
0	0	0	Overflow
1	1	1	Overflow
Jump to Pin 9	Jump to Pin 10	1	Automatic
Positive External Pulse	Positive External Pulse	0	External
Negative External Pulse	Negative External Pulse	1	External

Automatic Clear -- The counter is automatically reset to zero after each time its contents are read out.

External Clear -- The counter continues to totalize until an external reset is applied.

Overflow -- The counter continues to totalize until it clears itself by overflowing upon reaching the maximum count.

The counter is prevented from changing state during transfer of its contents into the PCM Formatter. This prevents an erroneous count readout.

CM-922PB SPECIFICATIONS

Input Voltage. - 0 to +5 volts dc nominal. CMOS or TTL compatible. Voltages within the range -0.5 to +5.5 volts dc will not cause permanent damage to the module.

Pulse Pair Resolution. - 1 Hz up to 1 Mhz nominal. Also depends on the input voltage amplitude. For a pulse input of less than 0 to +5 volts dc, the minimum pulse duration shall be 1000 nsecs.

External Reset Input Voltage. - The positive external reset pulse shall be 0 volt during the totalize period and +5 volts to reset the counter. The negative external reset pulse shall be +5 volts during the totalize period and 0 volt to reset the counter.

TABLE 32. - CM-922PB EPROM PROGRAMMING CODES (Broadened)

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
0	0	M	M	M	M	M	0
0	0	M	M	M	M	M	1

M = MODULE CODE {(1 thru 19)- 1}
C = CHANNEL CODE {(1 or 2)- 1}

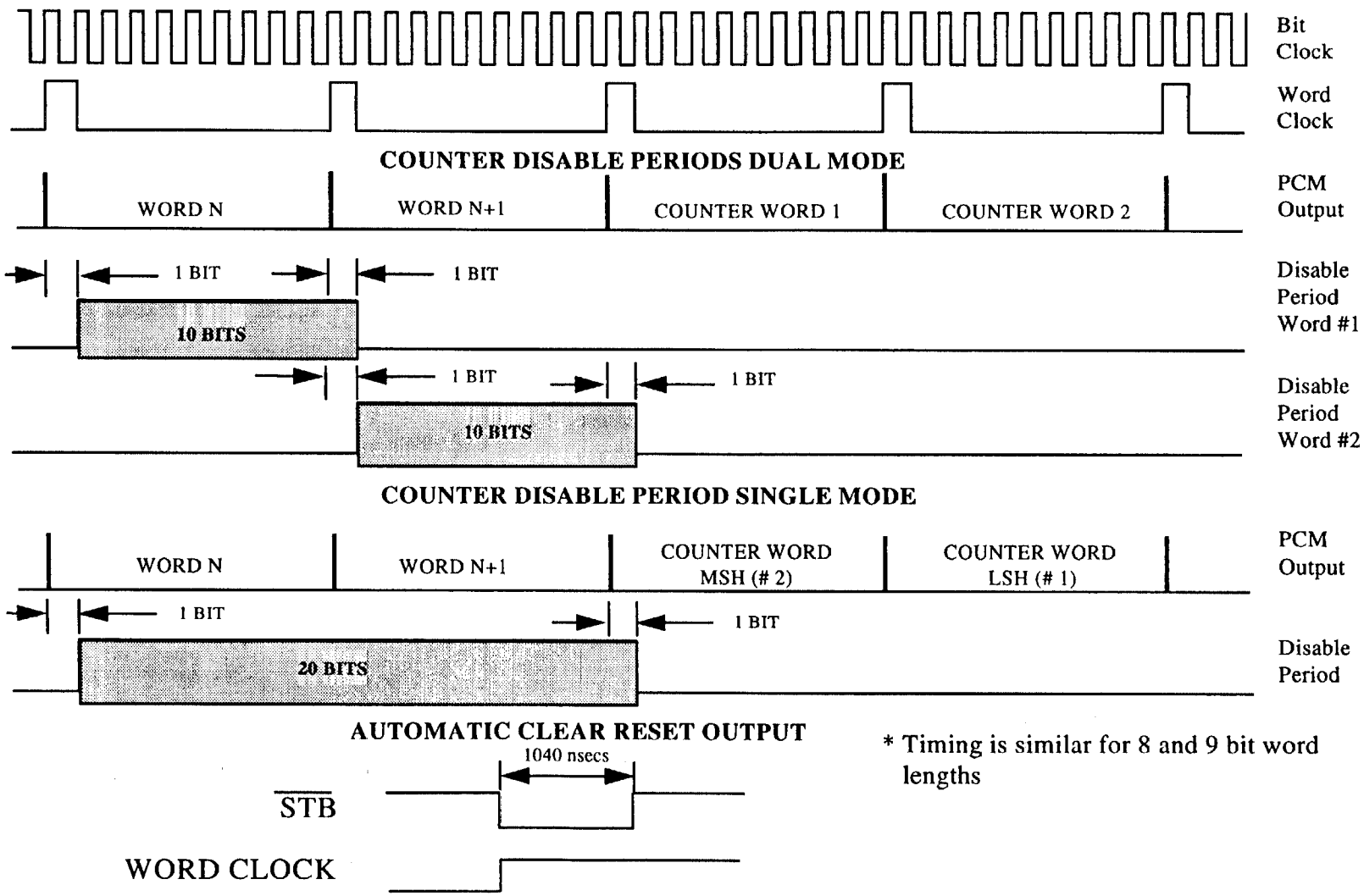
i.e. 00000110 = Module 4, Channel 1

TABLE 33. - CM-922PB INPUTS

PIN	DESCRIPTION	INPUT DEVICE
3	Program A1	4030B
17	Program A2	4063B
18	Program A3	4063B
13	Program A4	4063B
14	Program A5	4063B
4	Input #1	40109B
5	Input #2	40109B
6	PROG WL1	4071B & 4027B
11	PROG WL2	4071B
7	Reset Input #1	CD40109B
12	Reset Input #2	CD40109B
15	Complement Reset	4030B
16	Mode Select	4049B & 4019B

TABLE 34. - CM-922PB OUTPUTS

PIN	DESCRIPTION	OUTPUT DEVICE
9	Strobe Output #1	4049B
10	Strobe Output #2	4049B



* Timing is similar for 8 and 9 bit word lengths

Figure 10. - CM-922PB timing diagram.

TA-923 TIME EVENT MONITOR WITH ALTERNATING REGISTERS P/N 17923010-501

The function of the Time Event module (Appendix C, page C-13) is to allow the user to determine the elapsed time between the occurrence of two events (pulses). This is attained by determining the position in the major frame at which the user's pulses occur. There is a binary counter accumulator in the module which is reset to zero at the beginning of the major frame. The input to this counter is the word clock. The binary count is incremented by one at the beginning of each word. The parallel output of the counter is latched into a storage register by the leading edge of each input pulse. The contents of the latched register can be read out as often as required in the format. The readout is nondestructive. However, since a new word number is stored in the latched register by each input pulse, data will be lost if the register is not read out between input pulses.

Obviously, the resolution to which the elapsed time between two input pulses can be determined is two word periods. Also, the following ambiguity exists. The only way to determine if a new pulse has occurred is to monitor the word number which is read out each time for a change. When it changes, a new pulse input has occurred. Should a new pulse input occur in the same word period as the previous pulse, the latter will not be detected since the new word count stored in the latch will be the same as the old value.

Careful consideration must be exercised in the selection of system parameters such as bit rate, word size, number of words in the major frame, readout rate, and input pulse length to obtain useful data from a Time Event module.

The bit rate and word size control the maximum elapsed time resolution obtainable. Increasing the number of words in the major frame diminishes the probability that the ambiguity will occur. If the readout rate is inadequate, the output data will not be correct.

For certain types of data, as depicted in Figure 11, the required readout rate may be reduced significantly by storing the word numbers in which alternate pulses occur in alternate registers. The registers are then read out independently -- this is the reason why the TA-923 has two different types of time event monitors with two separate inputs. The input associated with the alternating registers is interface connector pin no. 1, and the word numbers at the time of occurrence of alternate pulses on that input are stored in alternate registers numbers 2 and 3. For asynchronous pulse inputs, the register in which the first pulse is stored is inconclusive. This complicates, but does not inhibit, data reduction.

The input associated with interface connector pin no. 6 is the normal type of time event monitor described beforehand. It has only one register no. 1 in which the word number at the time of the event input pulse is latched.

Figure 11. - TA-923 alternating register application.

The design of the alternating registers is suited to the data input in Figure 11. When pulse pairs occur on the data input and then are followed by a comparatively long delay before another pulse pair occurs, the alternating registers can be used advantageously. The time event information is stored in two storage registers alternately. For pulse groups of more than two pulses per group, the alternating registers will no longer be of advantage. The output data must be predictable as indicated in Figure 11 to utilize the advantage of the alternating registers.

For the non-alternating input, the time event channel must be programmed to be sampled at a rate greater than the highest pulse pair resolution of the actual data. The alternating registers can be used as in the previous example to read out that particular channel at a lower rate. In this way, more of the output format is reserved for other data channels.

The binary counter accumulator, which counts the word number in the major frame, is 12 bits long. Therefore, it can accommodate a major frame length of 4095 words. **When the number of words in the major frame exceeds the maximum binary value of the system word, the word number data stored in the 12-bit storage register must be read out in two contiguous system words.** The word number is read out LSB first. When a two-word readout is necessary, the most significant bits are located in the second word with some duplication. For a detailed description of the readout configuration and technique, see tables 41 and 42 in the TB-925 section.

The contents of the storage registers are multiplexed and entered into the PCM output format under EPROM program control. Only one TA-923 is admissible per system. Important information concerning the input and output time domains are given in Figure 12.

In Figure 12, an important point to note in the system timing is the offset that exists between the internal system domain and the PCM output domain. The two domains are skewed by two word periods. Further, the word per

major frame counter is reset to zero at the leading edge of the major frame pulse.

The event pulse shown will load no. 6 into the storage register within the Time Event Monitor modules. The time event channel may be read out anywhere in the output format. The sampling rate of the time event channel should be greater than the highest frequency component in the actual data.

Since event pulses are synchronous with the PCM timing, the word count is latched into each register by the first bit clock pulse that occurs immediately after the appropriate event pulse. Specific EPROM codes are dedicated to select each register within the module. The contents of each register is entered into the PCM output format at the coincidence of the assigned address and the internally generated "Load Command" pulse. The leading edge of the event pulse is used for information storage and the trailing edge has no effect.

Four synchronization signals utilized in this module are buffered and made available to the user as a convenience. Their use is not required to properly interface with the TA-923.

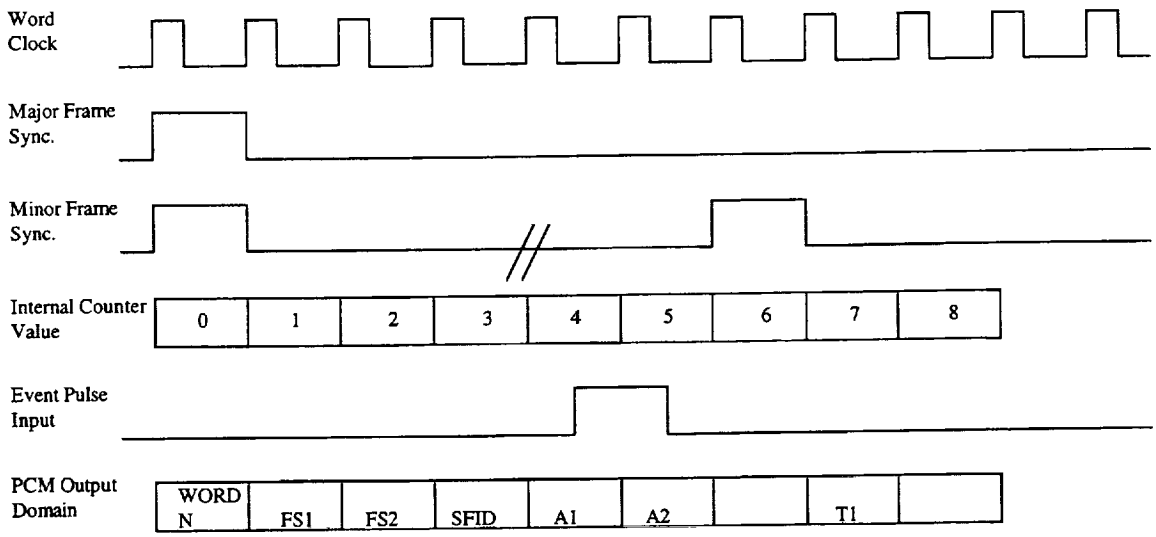


Figure 12. - Time event timing diagram.

TA-923 SPECIFICATIONS

Input Voltage. - The event pulse inputs are CMOS or low power TTL compatible and are 0 to +5 volts nominal. Voltages outside the range -0.3 to +36 volts dc will cause permanent damage to the module.

Pulse Duration. - The pulse input must be of duration one microsecond minimum.

These specifications are boundary conditions and reliable interface design will fall well within these limits.

Table 35. - TA-923 INPUTS

PIN	DESCRIPTION	INPUT DEVICE
6, 1	Event 0, 1 Inputs	LM 339
8	A3 Programming	RCA 4063

Table 36. - TA-923 OUTPUTS

PIN	DESCRIPTION	OUTPUT DEVICE
3	Major Frame Sync	RCA 4050
2	Minor Frame Sync	RCA 4050
5	Word Clock	RCA 4050
4	Bit Clock	RCA 4050
7	2X Bit Clock	RCA 4050

TB-925 TIME EVENT MONITOR WITH TIMING BUFFERS P/N 17925010-502

The TB-925 is a second type of time event monitor used for determination of the relative time of occurrence of events. This module performs in exactly the same manner as the non-alternating input of the TA-923 time event monitor. The TB-925 has two separate event pulse inputs. Two TB-925 modules are permitted per system for a capability of four time event channels from TB-925 modules. Selecting between TB-925 modules is done by an address assignment made at the external connector of the module. The address programming pin is pulled up to +10 volts through a 30 kilohm resistor.

Programming is accomplished by grounding the appropriate pin at the external connector. An open programming pin will be interpreted as a logic "1". For module programming codes, see Tables 37 through 40.

Another feature provided by the TB-925 is a set of internal binary counters which provide the "X" and "Y" positions in the format at any time. The outputs of these two counters are buffered and available on the external interface connect to permit external devices to be synchronized with the PCM major frame format. The output from one of the counters provide the word number in the frame and is reset to zero by the minor frame pulse. The output from the other counter is the minor frame number and is reset by the major frame pulse. The word/frame counter has eight stages and counts from 0 to 255. The minor frame counter has five stages and counts from 0 to 31.

As with the non-alternating input of TA-923, the TB-925 has a single twelve-stage binary counter used to count major frame words from 0 to 4095. Associated with each of the inputs is a single 12-bit register into which the word number from the 12-bit word counter is latched. Again the number of active channels within this module, the readout rate, and position within the PCM format are under EPROM format control.

Table 37. - TA-923 PROGRAMMING CODES

REGISTER	WORD	A7	A6	A5	A4	A3	A2	A1	A0	HEX CODE	MODULE
	1	1	1	0	1	1	0	0	0	D8	
1	2	1	1	0	1	1	0	0	1	D9	
	1	1	1	0	1	1	0	1	0	DA	1
2	2	1	1	0	1	1	0	1	1	DB	
	1	1	1	0	1	1	1	0	0	DC	
3	2	1	1	0	1	1	1	0	1	DD	

Table 38. - TB-925 PROGRAMMING CODES

REGISTER	WORD	A7	A6	A5	A4	A3	A2	A1	A0	HEX CODE	MODULE
	1	1	1	0	0	1	0	0	0	C8	
1	2	1	1	0	0	1	0	0	1	C9	
	1	1	1	0	0	1	0	1	0	CA	
2	2	1	1	0	0	1	0	1	1	CB	1
	1	1	1	0	0	0	0	0	0	C0	
1	2	1	1	0	0	0	0	0	1	C1	
	1	1	1	0	0	0	0	1	0	C2	
2	2	1	1	0	0	0	0	1	1	C3	2

The above codes are to be used in the EPROM program. A7 represents the MSB and A0 the LSB. When using TA-923 and/or TB-925 modules in a system, program A7 = 1, A6 = 1, and A5 = 0. A4 programming determines whether the TA-923 or the TB-925 module is addressed. A3 applies only to the TB-925 module and is used for module number selection. Since only one address line is designated for module selection, only two TB-925 modules can be used per system. A1 and A2 programming determines which data register, No. 1, No. 2 (or No. 3 in the TA-923) is selected for readout. A0 programming determines which word is read out. See Table 39 for more information concerning word selection. When using a Time Event module in a system, the program for the MP-901 Analog Multiplexer A7 = 1, A6 = 1 and A5 = 0 cannot be used.

Table 39. - TA-923 & TB-925 PROGRAMMING CONDITIONS

BITS PER WORD	CONDITION	USE FROM TABLE
	MFL <= 2^{10}	Word 1
10	MFL > 2^{10}	Words 1 & 2
	MFL <= 2^{9}	Word 1
9	MFL > 2^{9}	Words 1 & 2
	MFL <= 2^{8}	Word 1
8	MFL > 2^{8}	Words 1 & 2

The conditions listed in the above table are used to determine the EPROM program necessary to recover correct data from the Time Event modules. MFL equals the major frame length measured by the number of words. Words 1 and 2 are taken from Tables 37 and 38 and different programming

codes are required to read out each word. Recall that the storage registers consist of twelve stages. It follows that the maximum count of these registers cannot be read in one 8, 9, or 10-bit word. This is why programming of word 2 is sometimes necessary. The condition for only word 1 to be read out of each register is, if MFL is less than or equal to 2^n, where n equals the number of bits per word. If MFL is greater than 2^n, then word 1 and 2 must be read out of each register. The program for readout of word 1 and 2 must occur in consecutive EPROM locations. For information concerning the word organization, see the table below.

Table 40. - TA-923 & TB-925 WORD ORGANIZING

					A0 = "0" Word 1										A0 = "1" Word 2					
1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**		**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9											
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9		2^8	2^9	2^{10}	2^{11}	1	0	1	0	1	0

The word organization described above depicts the PCM output. Bit 1 is the first bit transmitted and bit 10 is the last. In this organization, the LSB of the counter value is the first bit transmitted. When programming both words 1 and 2 for readout, word 2 will have alternating ones and zeros in bits 5 through 10.

Since event pulses are asynchronous with the PCM timing, the word count is latched into each register by the first bit clock pulse that occurs immediately after the appropriate event pulse. Specific EPROM codes are dedicated to select each register within this module. The contents of each register is entered into the PCM output format at the coincidence of the assigned address and the "load command" pulse internally generated within the system. The leading edge of the event pulse is used for information storage and the trailing edge has no effect. The resolution of the reduced data will then be equivalent to two word periods of the system. The sampling rate chosen for time event channels must be greater than the greatest frequency component of the actual data being measured.

TB-925 SPECIFICATIONS

Input Voltage. - The event pulse inputs are CMOS or low power TTL compatible and are 0 to +5 volts nominal. Voltages outside the range -0.3 to +36 volts dc will cause permanent damage to the module.

Pulse Duration. - The pulse input must be of duration one microsecond minimum.

These specifications are boundary conditions and reliable interface design will fall well within these limits.

Table 41. - TB-925 INPUTS

PIN	DESCRIPTION	INPUT DEVICE
20, 1	Event 0, 1 Inputs	LM 339
37	A3 Programming	RCA 4063

Table 42. - TB-925 OUTPUTS

PIN	DESCRIPTION	OUTPUT DEVICE
3	Major Frame Sync	RCA 4050
2	Minor Frame Sync	RCA 4050
5	Word Clock	RCA 4050
4	Bit Clock	RCA 4050
13	2X Bit Clock	RCA 4050
6, 16, 17, 18, 36	Minor Frame Number	RCA 4050
7, 8, 9, 10, 11, 12, 14, 15	Word per frame	RCA 4050

SYSTEM CONFIGURATION & TESTING

This section presents information concerning the testing performed on the encoder systems and the documentation necessary to configure.

TESTING

All hardware is subjected to the following three levels of testing prior to its use on an actual mission:

1. Component, system and thermal testings by Aydin Vector
2. System level acceptance testings by Wallops Flight Facility
3. Mission specific system functional and environmental testings.

Aydin Vector performs a practical test on a module basis in a microprocessor controlled test set. All appropriate inputs and outputs are put to use and responses are limit checked. Then, the modules are joined in an ideal system configuration and all parameters are functionally checked again to attest module compatibility. At this point, the system is checked for proper operation over the temperature range from -35 degrees Centigrade to +85 degrees Centigrade.

Wallops Flight Facility performs system functional acceptance tests on the modules to two typical configurations. Once a mission's requirements are defined, the required modules are selected from the library of components and assembled. The EPROM is programmed for the mission's format and all mission inputs are simulated while all required outputs are functionally checked and calibrated. At that time, the PCM system is integrated into the payload accompanied by the compatibility tests and calibrations. The whole payload is then environmentally tested and the PCM system's performance is observed. If there are no inadequacies, the PCM system's flight quality is soon afterward established.

DOCUMENTATION

Necessary documentation for assembling an encoder system consists of the EPROM program, the PCM output format, a listing of each data channel word-frame-interval information, all outputs of the system, information specifying operational modes and hardwire addresses, the precise stacking configuration and information necessary to program the PCM decommutation system.

ACCOUNT OF FAILURES

There have been four major stacks that encountered specific failures. There were the Pfaff, Zipf, Kintner and Arnoldy PCM encoder stacks. An exact description of these blemishes will justify the reasons why different modules were returned to Aydin Vector Division for modification and repair. Of course, there have been many other minor failures which affected certain data modules.

Pfaff PCM encoder stack

Failure

There was no filtered conditioned Biϕ-L output from the FL-919A Quad Filter module.

Cause and Solution

The failure was originally considered to be due to the FL-919A. A step-by-step process was executed to ascertain the reason for the loss of the filtered conditioned Biϕ-L output. The supply voltage rails were measured at U101 (operational amplifier) in the FL-919A. The -15 volts supply measured -15.32 volts but the +15 volts supply measured +3.68 volts (minimum level required is +15.2 volts). The investigation was then shifted to the PX-984 Power Supply module which was removed from the system stack. The input voltage to U12 (LM317, +15 volts Regulator) was checked and was nominal at +17.5 volts. Upon visual inspection of the Voltage Regulator, it was found that the output wire bond was melted open into a ball. This failure was due to excessive current. No reason for this condition was apparent and no debris in a module or connector was found that could have caused a short circuit. The failure is under investigation by the manufacturer of the LM317.

Zipf PCM encoder stack

Failure

Three bits of the frame synchronization code dropped out when the PCM encoder was operating below -10°C.

Cause and Solution

The system stack was activated at room ambient to verify the frame synchronization code patterns. The encoder was then placed in the temperature chamber and cooled to -15°C. After five minutes of temperature stabilization, the system was powered up. The loss of decommutator frame synchronization lock was evident. An oscilloscope was used to verify the frame synchronization code patterns. It was detectable that bits 8 and 9 of

the FS2 were a logic "1" instead of the anticipated "0". After fifteen to twenty seconds, bits 8 and 9 changed to a logic "1" and frame synchronization lock on the decommutator had returned. The address lines A5 (bit 8) and A6 (bit 9) were monitored through the PR-914 Programmer module. The address lines were at the accurate logic levels. It was then determined that the parallel data bus bits 2 and 3 from the SD-924 Serial Digital module were behind the failure. This occurred since the address bus from the PR-914 shares the parallel data bus with the SD-924. One of the SD-924 modules was identified as the source of nonperformance. There was no visual evidence of damage in the module. The SD-924 module was then placed back into the stack which was cooled to -20°C. The input lines to U2 (SD-5000) were checked and found to be correct. The enable line to U2 was tested and found to be at +7.5 volts as opposed to the nominal ground (at ambient, it read +2 volts). The enable line is generated at U5 (SD-5000) using one gate of the switch. Analyses of the enable circuitry revealed that the on resistance of the device appeared excessively high, notably in cold temperature. The enable is used to gate the remaining switches within itself along with the other SD-5000s (U2 & U3). This yielded the gate voltage to be +7.5 volts at cold temperature which is high enough to switch on the SD-5000s. U2, being more reactive, turned on and data was granted on the parallel data bus at an improper time. This influenced the contention between the address data bus used by the PR-914 and the parallel data bus by the SD-924. Consequently, U2 data bits 2 and 3 were portrayed by the FM-918 as a logic "1" during the time the address data bits A5 and A6 should have been a logic "0" for the frame synchronization code time interval. This led the frame synchronization code patterns to be incorrect until U5 warmed up and its on resistance discontinued. This is looked upon as random part failure. Test procedures have been incorporated to detect this anomaly during system testing at Aydin Vector.

Kintner PCM encoder stack

Failure

The serial channels were interactive with each other and the unit was operational up to 400 kilobits per second.

Cause and Solution

The failure was isolated to the SD-924 Serial Digital module. There was also an unforeseen failure in the PR-914 Programmer module. The MM74C374 register chip was a random part failure. The load on the A0 address line was the failure. For 30 nanoseconds, the address line jitters on the falling edge. Design changes were implemented in the SD-924 and the TM-915D to help the unit operate at 800 kilobits per second. Two capacitors, C4 and C5, 33 picofarads and 27 picofarads respectively, were removed in the SD-924. The

TM-915D was moved to phase 3. In doing so, a 1/4 of a bit period was gained. These alterations were not implemented to be a permanent replacement. The Arnoldy PCM encoder stack later revealed the reason for the real nonperformance.

Arnoldy PCM encoder stack

Failure

There was a SD-924 serial data enable pulse failure at 200 kilobits per second.

Cause and Solution

The failure was isolated to the CM-922PB Counter module. The routing of the A0 address line should have been from the peripheral connector pin 19 to the input of the OR gate via a magnet wire. Instead, the magnet wire was connected to the pad of the substrate and the pin of the peripheral connector. All Counter modules were returned to Aydin Vector for rework.

Appendix A

DOCUMENTATION FOR A SAMPLE SYSTEM

ELECTRICAL CONFIGURATION FOR WALLOPS STANDARD MMP-900
PULSE CODE MODULATION ENCODER SYSTEM

Instrumentation Engineer: David Raphael

Date: 4/95

PCM Matrix

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	SFID	A1	S1	S1	S1	S1	S1	S1	S1	A59	C12	A70	A61	A64	C2	A42	A43	A44	A45	A40	A50	S3	A71	A62	A82	A59	C12	A70	A61	A91	C10	A121
2		A2	A6	C1	S2	S2	A19	A26	A33						C3					A41	A51	S4									C11	
3		A3	A7	A10	A13	A16	A20	A27	A34						C4					A48	A52	A46									A63	
4		A4	A6	C1	S2	S2	A21	A28	A35						C5					A49	A53	P5									P2	
5		A5	A8	A11	A14	A17	A22	A29	A36						C6					A60	A54	S3									C10	
6		P1	A6	C1	S2	S2	A23	A30	A37						C7					A47	A55	S4									C11	
7		A58	A9	A12	A15	A18	A24	A31	A38						C8					A48	A56	A46									P3	
8		A120	A6	C1	S2	S2	A25	A32	A39						C9					A49	A57	P6									P4	
9																																
10																																
11																																
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32	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼

Data Rate: 800 Kbps
Bits/Word: 10

Parity: None
Alignment: MSB First

FS1 = 1110110111
FS2 = 1000100000

PCM Matrix

	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
1	A72	A73	A75	A80	A83	A85	A87	A89	A92	A59	C12	A70	A61	A64	A93	A42	A43	A44	A45	A101	A109	A122	A71	A62	A82	A59	C12	A70	A61	A91	FS1	FS2
2		A74	A76	A81	A84	A86	A88	A90							A94					A102	A110											
3			A75												A95					A103	A111										
4			A77												A96					A104	A112										
5			A75												A97					A105	A113										
6			A78												A98					A106	A114										
7			A75												A99					A107	A115										
8			A79												A100					A108	A116										
9																					A109										
10																					A110										
11																					A111										
12																					A112										
13																					A113										
14																					A117										
15																					A118										
16																					A119										
17																															
18																															
19																															
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31																															
32	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼

Data Rate: 800 Kbps
Bits/Word: 10

Parity: None
Alignment: MSB First

FS1 = 1110110111
FS2 = 1000100000

PROM PROGRAM

800 Kbits/sec

10 Bits/Word

FS1 = 1110110111 FS2 = 1000100000

Loc.	Prog.	Data	Loc.	Prog.	Data	Loc.	Prog.	Data
00	ED	FS1	20	F2	IC 8 Deep	40	BB	A92
01	F8	FS2IC	21	A8	Go To	41	9A	A59
02	88	FS2	22	F2	IC 8 Deep	42	0D	C12
03	F7	FSIC	23	B0	Go To	43	A5	A70
04	1F	32 Deep	24	F2	IC 8 Deep	44	9C	A61
05	F2	IC 8 Deep	25	B8	Go To	45	9F	A64
06	60	Go To	26	A6	A71	46	F2	IC 8 Deep
07	F2	IC 8 Deep	27	9D	A62	47	E0	Go To
08	68	Go To	28	B1	A82	48	89	A42
09	F2	IC 8 Deep	29	9A	A59	49	8A	A43
0A	70	Go To	2A	0D	C12	4A	8B	A44
0B	F2	IC 8 Deep	2B	A5	A70	4B	8C	A45
0C	78	Go To	2C	9C	A61	4C	F2	IC 8 Deep
0D	F2	IC 8 Deep	2D	BA	A91	4D	E8	Go To
0E	80	Go To	2E	F2	IC 8 Deep	4E	F3	IC 16 Deep
0F	F2	IC 8 Deep	2F	C0	Go To	4F	F0	Go To
10	88	Go To	30	58	A121	50	59	A122
11	F2	IC 8 Deep	31	A7	A72	51	A6	A71
12	90	Go To	32	F0	IC 2 Deep	52	9D	A62
13	F2	IC 8 Deep	33	C8	Go To	53	B1	A82
14	98	Go To	34	F2	IC 8 Deep	54	9A	A59
15	9A	A59	35	CA	Go To	55	0D	C12
16	0D	C12	36	F0	IC 2 Deep	56	A5	A70
17	A5	A70	37	D2	Go To	57	9C	A61
18	9C	A61	38	F0	IC 2 Deep	58	BA	A91
19	9F	A64	39	D4	Go To	59	FF	EOF
1A	F2	IC 8 Deep	3A	F0	IC 2 Deep	5A	00	
1B	A0	Go To	3B	D6	Go To	5B	00	
1C	89	A42	3C	F0	IC 2 Deep	5C	00	
1D	8A	A43	3D	D8	Go To	5D	00	
1E	8B	A44	3E	F0	IC 2 Deep	5E	00	
1F	8C	A45	3F	DA	Go To	5F	00	

PROM PROGRAM (Continued)

800 Kbits/sec
10 Bits/Word
FS1 = 1110110111 FS2 = 1000100000

Loc.	Prog.	Data	Loc.	Prog.	Data	Loc.	Prog.	Data
60	60	A1	80	10	S1	A0	03	C2
61	61	A2	81	11	S2	A1	04	C3
62	62	A3	82	6F	A16	A2	05	C4
63	63	A4	83	11	S2	A3	06	C5
64	64	A5	84	70	A17	A4	07	C6
65	30	P1	85	11	S2	A5	08	C7
66	99	A58	86	71	A18	A6	09	C8
67	57	A120	87	11	S2	A7	0A	C9
68	10	S1	88	10	S1	A8	87	A40
69	65	A6	89	72	A19	A9	88	A41
6A	66	A7	8A	73	A20	AA	8F	A48
6B	65	A6	8B	74	A21	AB	90	A49
6C	67	A8	8C	75	A22	AC	9B	A60
6D	65	A6	8D	76	A23	AD	8E	A47
6E	68	A9	8E	77	A24	AE	8F	A48
6F	65	A6	8F	78	A25	AF	90	A49
70	10	S1	90	10	S1	B0	91	A50
71	02	C1	91	79	A26	B1	92	A51
72	69	A10	92	7A	A27	B2	93	A52
73	02	C1	93	7B	A28	B3	94	A53
74	6A	A11	94	7C	A29	B4	95	A54
75	02	C1	95	7D	A30	B5	96	A55
76	6B	A12	96	7E	A31	B6	97	A56
77	02	C1	97	7F	A32	B7	98	A57
78	10	S1	98	10	S1	B8	12	S3
79	11	S2	99	80	A33	B9	13	S4
7A	6C	A13	9A	81	A34	BA	8D	A46
7B	11	S2	9B	82	A35	BB	35	P5
7C	6D	A14	9C	83	A36	BC	12	S3
7D	11	S2	9D	84	A37	BD	13	S4
7E	6E	A15	9E	85	A38	BE	8D	A46
7F	11	S2	9F	86	A39	BF	36	P6

PROM PROGRAM (Continued)

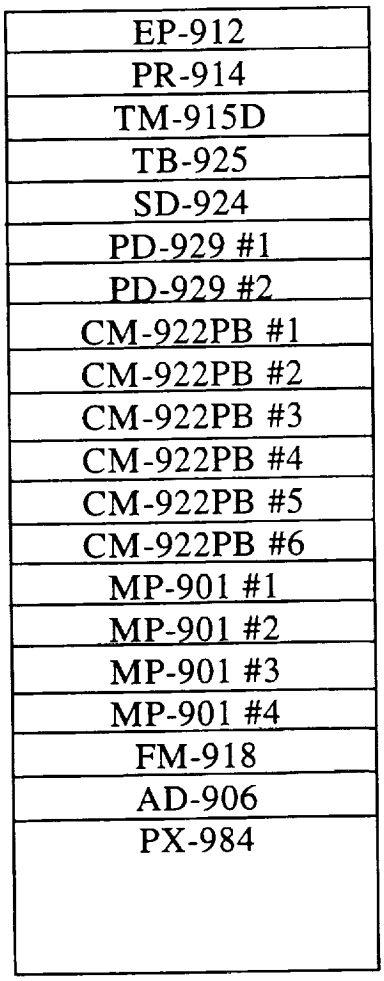
800 Kbits/sec
10 Bits/Word
FS1 = 1110110111 FS2 = 1000100000

Loc.	Prog.	Data	Loc.	Prog.	Data
C0	0B	C10	E0	BC	A93
C1	0C	C11	E1	BD	A94
C2	9E	A63	E2	BE	A95
C3	31	P2	E3	BF	A96
C4	0B	C10	E4	40	A97
C5	0C	C11	E5	41	A98
C6	32	P3	E6	42	A99
C7	34	P4	E7	43	A100
C8	A8	A73	E8	44	A101
C9	A9	A74	E9	45	A102
CA	AA	A75	EA	46	A103
CB	AB	A76	EB	47	A104
CC	AA	A75	EC	48	A105
CD	AC	A77	ED	49	A106
CE	AA	A75	EE	4A	A107
CF	AD	A78	EF	4B	A108
D0	AA	A75	F0	4C	A109
D1	AE	A79	F1	4D	A110
D2	AF	A80	F2	4E	A111
D3	B0	A81	F3	4F	A112
D4	B2	A83	F4	50	A113
D5	B3	A84	F5	51	A114
D6	B4	A85	F6	52	A115
D7	B5	A86	F7	53	A116
D8	B6	A87	F8	4C	A109
D9	B7	A88	F9	4D	A110
DA	B8	A89	FA	4E	A111
DB	B9	A90	FB	4F	A112
DC	00	Spacer	FC	50	A113
DD	00	Spacer	FD	54	A117
DE	00	Spacer	FE	55	A118
DF	00	Spacer	FF	56	A119

PCM SYSTEM MODULE ADDRESS PROGRAMMING

Module	A7	A6	A5	A4	A3	A2	A1	A0	HEX
TB-925	1	1	0	0	0	0	X	X	C0-C3
CM-922 #1	0	0	0	0	0	0	1	X	02-03
CM-922 #2	0	0	0	0	0	1	0	X	04-05
CM-922 #3	0	0	0	0	0	1	1	X	06-07
CM-922 #4	0	0	0	0	1	0	0	X	08-09
CM-922 #5	0	0	0	0	1	0	1	X	0A-0B
CM-922 #6	0	0	0	0	1	1	0	X	0C-0D
SD-924	0	0	0	1	0	X	X	X	10-17
PD-929 #1	0	0	1	1	0	0	X	X	30-32
PD-929 #2	0	0	1	1	0	1	X	X	34-36
MP-901 #1	0	1	1	X	X	X	X	X	60-7F
MP-901 #2	1	0	0	X	X	X	X	X	80-9F
MP-901 #3	1	0	1	X	X	X	X	X	A0-BF
MP-901 #4	0	1	0	X	X	X	X	X	40-5F
FS1	1	1	1	0	1	1	0	1	
FS2	1	0	0	0	1	0	0	0	
SFID	0	0	0	2^4	2^3	2^2	2^1	2^0	

X = Used to determine specific input for each module.



Stack Configuration

MP-901 ANALOG MULTIPLEXER: 1

Module Address:
A5 1 A6 1 A7 0

Associated Inputs: A1 thru A32

MP-901 ANALOG MULTIPLEXER: 2

Module Address:
A5 0 A6 0 A7 1

Associated Inputs: A33 thru A64

MP-901 ANALOG MULTIPLEXER: 3

Module Address:
A5 1 A6 0 A7 1

Associated Inputs: A65 thru A96

MP-901 ANALOG MULTIPLEXER: 4

Module Address:
A5 0 A6 1 A7 0

Associated Inputs: A97 thru A128

PD-929 PARALLEL DIGITAL DATA MULTIPLEXER: 1

Module Address:
A2 0 A3 0 A4 1 A5 1

Bits being used in respective words.

Word Number	Bit Number									
	1	2	3	4	5	6	7	8	9	10
1	x	x	x	x	x					
2	x	x	x	x	x	x	x	x	x	x
3	x	x	x	x	x	x	x			

Word Enable: Word 1 ____ Word 2 ____

PD-929 PARALLEL DIGITAL DATA MULTIPLEXER: 2

Module Address:
A2 1 A3 0 A4 1 A5 1

Bits being used in respective words.

Word Number	Bit Number									
	1	2	3	4	5	6	7	8	9	10
1	x	x	x	x	x	x	x	x		
2	x	x	x	x	x					
3	x	x	x	x	x	x	x	x	x	x

Word Enable: Word 1 ____ Word 2 ____

SD-924 SERIAL DIGITAL DATA MULTIPLEXER: 1

Module Address:
A4 1 A5 0

Input 1	x	Gated Clock 1	x
Input 2	x	Gated Clock 2	x
Input 3	x	Gated Clock 3	x
Input 4	x	Gated Clock 4	x
Input 5		Gated Clock 5	
Input 6		Gated Clock 6	
Input 7		Gated Clock 7	
Input 8		Gated Clock 8	

Inverted Load 1	x	Enable 1	x
Inverted Load 2	x	Enable 2	x
Inverted Load 3	x	Enable 3	x
Inverted Load 4	x	Enable 4	x
Inverted Load 5		Enable 5	
Inverted Load 6		Enable 6	
Inverted Load 7		Enable 7	
Inverted Load 8		Enable 8	

Is the SD-924 being read out in two or more consecutive words?
YES x NO

If YES, how many bits are to be shifted in a series? 80 Bits

Word Length A 0 B 0

Word Length Codes

Bits/Word	A	B
8	0	1
9	1	0
10	0	0

CM-922P DUAL COUNTER/ACCUMULATOR: 1

Word Length A 0 B 0

Word Length Codes

Bits/Word	A	B
8	1	1
9	0	1
10	0	0

Module Address:
A1 1 A2 0 A3 0 A4 0 A5 0

Dual x Single _____

Reset Mode No. 1 3
Reset Mode No. 2 3

1. External Reset Pulse
2. Reset on Read
3. Overflow
4. Overflow Complement

Counter No. 1 Input C1
Counter No. 2 Input C2

CM-922P DUAL COUNTER/ACCUMULATOR: 2

Word Length A 0 B 0

Word Length Codes

Bits/Word	A	B
8	1	1
9	0	1
10	0	0

Module Address:
A1 0 A2 1 A3 0 A4 0 A5 0

Dual x Single _____

Reset Mode No. 1 3
Reset Mode No. 2 3

1. External Reset Pulse
2. Reset on Read
3. Overflow
4. Overflow Complement

Counter No. 1 Input C3
Counter No. 2 Input C4

CM-922P DUAL COUNTER/ACCUMULATOR: 3

Word Length A 0 B 0

Word Length Codes	Bits/Word	A	B
	8	1	1
	9	0	1
	10	0	0

Module Address:
A1 1 A2 1 A3 0 A4 0 A5 0

Dual x Single _____

Reset Mode No. 1 3
Reset Mode No. 2 3

1. External Reset Pulse
2. Reset on Read
3. Overflow
4. Overflow Complement

Counter No. 1 Input C5
Counter No. 2 Input C6

CM-922P DUAL COUNTER/ACCUMULATOR: 4

Word Length A 0 B 0

Word Length Codes	Bits/Word	A	B
	8	1	1
	9	0	1
	10	0	0

Module Address:
A1 0 A2 0 A3 1 A4 0 A5 0

Dual x Single _____

Reset Mode No. 1 3
Reset Mode No. 2 3

1. External Reset Pulse
2. Reset on Read
3. Overflow
4. Overflow Complement

Counter No. 1 Input C7
Counter No. 2 Input C8

CM-922P DUAL COUNTER/ACCUMULATOR: 5

Word Length A 0 B 0

Word Length Codes	Bits/Word	A	B
	8	1	1
	9	0	1
	10	0	0

Module Address:
A1 1 A2 0 A3 1 A4 0 A5 0

Dual x Single _____

Reset Mode No. 1 3
Reset Mode No. 2 3

1. External Reset Pulse
2. Reset on Read
3. Overflow
4. Overflow Complement

Counter No. 1 Input C9
Counter No. 2 Input C10

CM-922P DUAL COUNTER/ACCUMULATOR: 6

Word Length A 0 B 0

Word Length Codes	Bits/Word	A	B
	8	1	1
	9	0	1
	10	0	0

Module Address:
A1 0 A2 1 A3 1 A4 0 A5 0

Dual x Single _____

Reset Mode No. 1 3
Reset Mode No. 2 1

1. External Reset Pulse
2. Reset on Read
3. Overflow
4. Overflow Complement

Counter No. 1 Input C11
Counter No. 2 Input C12

TB-925 TIME EVENT MONITOR AND TIMING BUFFERS: 1

Output Description	Pin No.	Check if required
Bit Clock	4	x
2X Bit Clock	13	
Digital GND	19	
Major Frame Sync	3	x
Minor Frame Sync	2	
Word Clock	5	
WD ACC 0	11	
WD ACC 1	7	
WD ACC 2	12	
WD ACC 3	10	
WD ACC 4	8	
WD ACC 5	9	
WD ACC 6	14	
WD ACC 7	15	
FR ACC 0	16	x
FR ACC 1	17	
FR ACC 2	36	x
FR ACC 3	18	
FR ACC 4	6	x

WD ACC = Word Number Accumulator
FR ACC = Frame Number Accumulator

GROUP I MODULE OUTPUTS REQUIRED FOR THIS MISSION (INSTRUMENTATION ENGINEER CHECK ONLY THOSE REQUIRED)

TIMER TM-915D

Output Type	TM-915D Pin No.	Required	Waveform Description
NRZ-L Secondary	1	_____	5 V TTL output with rise time = 100 nsecs
Biϕ-L Secondary	2	_____	5 V TTL output with rise time = 100 nsecs
NRZ-L Primary	4	x	5 V TTL output with rise time = 100 nsecs
Major Frame	5	x	High for one word period one prior to first Frame Sync Word in format in last subframe of format
Biϕ-L Primary	6	x	5 V TTL output
Output Type	**TM-915D Pin No.**	**Required**	**Waveform Description**
1/2X Bit Sync	7	_____	5 V TTL output
1/4X Bit Sync	8	_____	5 V TTL output
1/8X Bit Sync	9	_____	5 V TTL output
1/16X Bit Sync	10	_____	5 V TTL output
Biϕ/NRZ	20	_____	5 V TTL output
$\overline{\text{Biϕ/NRZ}}$	21	_____	5 V TTL output
$\overline{\text{Bit Clock}}$	23	_____	5 V TTL output ± 15% symmetry. Inverse polarity from pin 26
Minor Frame Sync	24	x	High for one word period one prior to first Frame Sync Word in format for each subframe
Word Clock	25	x	Goes high for 1 bit period at leading edge of each word
Bit Clock	26	x	Symmetrical ± 15% 5 V TTL output
2X Bit Sync	27	_____	5 V TTL output

All TM-915D outputs are CMOS operated on 5 volts. However, the simulator buffers them with TTL logic operated on 5 volts.

INPUT SIMULATOR PROGRAMMING INFORMATION

POWER SUPPLY PX-984

Bit Rate 800 Kbit/sec
Internal x External _____

Timer TM-915D

Select Biϕ (0) _____ or NRZ (1) _____
Select Mark (0) _____ or Space (1) _____

Connect the bit synthesizer to the output which will be used for flight. If premod filter is to be used, select the proper input.

Parity Odd (1) _____ or None (0) x

Total Bits/Word B4 1 B3 0 B2 0 B1 1

Bits/Word Codes

Bits/Word	B4	B3	B2	B1
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1

BIT SYNCHRONIZER

Bit Rate ___800___ Kbit/sec
Output Code _____
Inverted ___x___ Normal _____
Bandwidth _____

FRAME SYNCHRONIZER

FRAME SYNC PATTERN
1 1 1 0 1 1 0 1 1 1 1 0 0 0 1 0 0 0 0 0 - - - - - - - - - - -
FBT LBT

Pattern Length ___20___ Bits

Strategy _____ _____ Bit Window

Accept any errors per frame? YES _____ NO __x__

Verify __1__ pattern(s) to proceed from verify to lock

Accept any errors in lock mode? YES _____ NO __x__

Number of Bits/Frame ___640___ including FS

MSBF __x__ LSBF _____

Word Length __10__ Bits

Number of Data Words/Frame __62__ excluding FS pattern

SUBFRAME SYNCHRONIZER

Are there any subframes? YES __x__ NO _____

Is subframe identification counter used? YES __x__ NO _____

Does subframe ID counter count up or down? UP __x__ DOWN _____

Subframe Length ___32___ Words

Number of bit errors accepted in pattern? __1__

Bit number of MSB of subframe ID counter __4__

Identification Counter Length __5__ Bits

MSBF Identification Count Bit Alignment? YES __x__ NO _____

Initial Identification Count __0__

WORD SELECTOR

Number of Bits/Word ___10___

MSBF __x___ or LSBF _____

Is parity included? YES _____ NO __x__

Appendix B

PROGRAMMING CODES AND EXTERNAL CONNECTOR PIN-OUT REFERENCES

RECOMMENDED FRAME SYNCHRONIZATION PATTERNS

# of bits										
7	101	100	0							
8	101	110	00							
9	101	110	000							
10	110	111	000	0						
11	101	101	110	00						
12	110	101	100	000						
13	111	010	110	000	0					
14	111	001	101	000	00					
15	111	011	001	010	000					
16	111	010	111	001	000	0				
17	111	100	110	101	000	00				
18	111	100	110	101	000	000				
19	111	110	011	001	010	000	0			
20	111	011	011	110	001	000	00			
21	111	011	101	001	011	000	000			
22	111	100	110	110	101	000	000	0		
23	111	101	011	100	110	100	000	00		
24	111	110	101	111	001	100	100	000		
25	111	110	010	110	111	000	100	000	0	
26	111	110	100	110	101	100	010	000	00	
27	111	110	101	101	001	100	110	000	000	
28	111	101	011	110	010	110	011	000	000	0
29	111	101	011	110	011	001	101	000	000	00
30	111	110	101	111	001	100	110	100	000	000

EPROM INSTRUCTION CODES

INSTRUCTION	A7	A6	A5	A4	A3	A2	A1	A0	HEX	COMMENTS
	1	1	1	1	1	1	1	1	FF	Bits A1, A0 are stored for
End of Frame	1	1	1	1	1	1	1	0	FE	insertion into bit 9 and 10
	1	1	1	1	1	1	0	1	FD	position of first frame
	1	1	1	1	1	1	0	0	FC	sync word for 9 and 10 bit systems.
	1	1	1	1	1	0	1	1	FB	Bits A1, A0 are stored for
Frame Sync Word	1	1	1	1	1	0	1	0	FA	insertion into bit 9 and 10
	1	1	1	1	1	0	0	1	F9	position of first frame
	1	1	1	1	1	0	0	0	F8	sync word for 9 and 10 bit systems.
Frame ID Word	1	1	1	1	0	1	1	1	F7	
									F6	RESERVED Do Not Use
									F5	RESERVED Do Not Use
	1	1	1	1	0	1	0	0	F4	32 Deep Subframe
	1	1	1	1	0	0	1	1	F3	16 Deep Subframe
Subcommutated Data Word	1	1	1	1	0	0	1	0	F2	8 Deep Subframe
	1	1	1	1	0	0	0	1	F1	4 Deep Subframe
	1	1	1	1	0	0	0	0	F0	2 Deep Subframe

PX -984 BIT RATE PROGRAMMING

Program C	Program B	Program A	8.0 MHz Xtal Kbit/sec	6.4 MHz Xtal Kbit/sec	External Clock (Resulting bit rate expressed as fraction of external clock)
0	0	0	1000	800	1/2
0	0	1	500	400	1/4
0	1	0	250	200	1/8
0	1	1	125	100	1/16
1	0	0	62.5	50	1/32
1	0	1	31.2	25	1/64
1	1	0	15.6	12.5	1/128
1	1	1	7.81	6.25	1/256

TM-915D WORD LENGTH PROGRAMMING CODES

B4	B3	B2	B1	BITS/WORD
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10

TM-915D PARITY SELECT PROGRAMMING CODES

PIN 11	PARITY
0	None
1	Odd

TM-915D OUTPUT PROGRAMMING CODES

PIN 3	PIN 22	OUTPUT CODE
0	0	Biϕ-M
0	1	Biϕ-S
1	0	NRZ-M
1	1	NRZ-S

MP-901 EPROM PROGRAMMING CODE

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
M	M	M	C	C	C	C	C

MP-901 EPROM PROGRAMMING CODES (Broadened)

CHANNEL	PIN	A7	A6	A5	A4	A3	A2	A1	A0
1	1	M	M	M	0	0	0	0	0
2	20	M	M	M	0	0	0	0	1
3	2	M	M	M	0	0	0	1	0
4	21	M	M	M	0	0	0	1	1
5	3	M	M	M	0	0	1	0	0
6	22	M	M	M	0	0	1	0	1
7	4	M	M	M	0	0	1	1	0
8	23	M	M	M	0	0	1	1	1
9	5	M	M	M	0	1	0	0	0
10	24	M	M	M	0	1	0	0	1
11	6	M	M	M	0	1	0	1	0
12	25	M	M	M	0	1	0	1	1
13	7	M	M	M	0	1	1	0	0
14	26	M	M	M	0	1	1	0	1
15	8	M	M	M	0	1	1	1	0
16	27	M	M	M	0	1	1	1	1
17	9	M	M	M	1	0	0	0	0
18	28	M	M	M	1	0	0	0	1
19	10	M	M	M	1	0	0	1	0
20	29	M	M	M	1	0	0	1	1
21	11	M	M	M	1	0	1	0	0
22	30	M	M	M	1	0	1	0	1
23	12	M	M	M	1	0	1	1	0
24	31	M	M	M	1	0	1	1	1
25	13	M	M	M	1	1	0	0	0
26	32	M	M	M	1	1	0	0	1
27	14	M	M	M	1	1	0	1	0
28	33	M	M	M	1	1	0	1	1
29	15	M	M	M	1	1	1	0	0
30	34	M	M	M	1	1	1	0	1
31	16	M	M	M	1	1	1	1	0
32	35	M	M	M	1	1	1	1	1

PD-929 EPROM PROGRAMMING CODE

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
0	0	M	M	M	M	C	C

PD-929 EPROM PROGRAMMING CODES (Broadened)

CHANNEL	PIN	A7	A6	A5	A4	A3	A2	A1	A0
1	2, 5, 8, 11, 14, 22, 25, 28, 31, 34	0	0	M	M	M	M	0	0
2	3, 6, 9, 12, 15, 20, 23, 26, 29, 32	0	0	M	M	M	M	0	1
3	1, 4, 7, 10, 13, 21, 24, 27, 30, 33	0	0	M	M	M	M	1	0

SD-924 EPROM PROGRAMMING CODE

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
0	0	M	M	X	C	C	C

SD-924 EPROM PROGRAMMING CODES (Broadened)

CHANNEL	PIN	A7	A6	A5	A4	A3	A2	A1	A0
1	27	0	0	M	M	X	0	0	0
2	8	0	0	M	M	X	0	0	1
3	26	0	0	M	M	X	0	1	0
4	7	0	0	M	M	X	0	1	1
5	1	0	0	M	M	X	1	0	0
6	20	0	0	M	M	X	1	0	1
7	2	0	0	M	M	X	1	1	0
8	21	0	0	M	M	X	1	1	1

SD-924 WORD LENGTH PROGRAMMING CODES

PROG WL1 PIN 9	PROG WL2 PIN 11	BITS/WORD
0	1	8
1	0	9
0	0	10

CM-922PB EPROM PROGRAMMING CODE

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
0	0	M	M	M	M	M	C

CM-922PB EPROM PROGRAMMING CODES (Broadened)

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)
0	0	M	M	M	M	M	0
0	0	M	M	M	M	M	1

CM-922PB WORD LENGTH PROGRAMMING CODES

PROG WL1 PIN 6	PROG WL2 PIN 11	BITS/WORD
1	1	8
0	1	9
0	0	10

CM-922PB MODE SELECT PROGRAMMING CODES

MODE SELECT PIN 16	COUNTER MODE
0	Single
1	Dual

CM-922PB RESET MODE PROGRAMMING CODES

RESET INPUT #1 PIN 7	RESET INPUT #2 PIN 12	COMPLIMENT RESET PIN 15	RESET MODE
0	0	0	Overflow
1	1	1	Overflow
Jump to Pin 9	Jump to Pin 10	1	Automatic
Positive External Pulse	Positive External Pulse	0	External
Negative External Pulse	Negative External Pulse	1	External

TA-923 PROGRAMMING CODES

REGISTER	WORD	A7	A6	A5	A4	A3	A2	A1	A0	HEX CODE	MODULE
	1	1	1	0	1	1	0	0	0	D8	
1	2	1	1	0	1	1	0	0	1	D9	
	1	1	1	0	1	1	0	1	0	DA	1
2	2	1	1	0	1	1	0	1	1	DB	
	1	1	1	0	1	1	1	0	0	DC	
3	2	1	1	0	1	1	1	0	1	DD	

TB-925 PROGRAMMING CODES

REGISTER	WORD	A7	A6	A5	A4	A3	A2	A1	A0	HEX CODE	MODULE
	1	1	1	0	0	1	0	0	0	C8	
1	2	1	1	0	0	1	0	0	1	C9	
	1	1	1	0	0	1	0	1	0	CA	
2	2	1	1	0	0	1	0	1	1	CB	1
	1	1	1	0	0	0	0	0	0	C0	
1	2	1	1	0	0	0	0	0	1	C1	
	1	1	1	0	0	0	0	1	0	C2	
2	2	1	1	0	0	0	0	1	1	C3	2

PX-984 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	NC
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	Signal Ground
9	Chassis Ground
10	External Clock Input
11	+28 volts Input
12	+28 volts Return
13	Program C
14	Program B
15	Program A

TM-915D EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION	PIN	DESCRIPTION
1	NRZ-L Secondary	20	Coded PCM Output
2	Biϕ-L Secondary	21	Coded PCM Output (Inverted)
3	Biϕ/NRZ Program	22	Mark/Space Program
4	NRZ-L Primary	23	Bit Sync (Inverted)
5	Major Frame Sync	24	Minor Frame Sync
6	Biϕ-L Primary	25	Word Sync
7	1/2X Bit Clock	26	Bit Sync
8	1/4X Bit Clock	27	2X Bit Clock
9	1/8X Bit Clock	28	NC
10	1/16X Bit Clock	29	NC
11	Parity Enable	30	NC
12	Bits/word B3	31	NC
13	Bits/word B2	32	NC
14	Bits/word B4	33	NC
15	Bits/word B1	34	NC
16	NC	35	NC
17	NC	36	NC
18	NC	37	NC
19	Digital Ground		

FL-919A EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	Adjustable Amplifier Input
2	Adjustable Amplifier Output
3	Signal Ground
4	Filter #3 Output
5	Filter #1 Output
6	Filter Input
7	NC
8	Filter #4 Output
9	Filter #2 Output

MP-901 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Channel 1 Input	20	Channel 2 Input
2	Channel 3 Input	21	Channel 4 Input
3	Channel 5 Input	22	Channel 6 Input
4	Channel 7 Input	23	Channel 8 Input
5	Channel 9 Input	24	Channel 10 Input
6	Channel 11 Input	25	Channel 12 Input
7	Channel 13 Input	26	Channel 14 Input
8	Channel 15 Input	27	Channel 16 Input
9	Channel 17 Input	28	Channel 18 Input
10	Channel 19 Input	29	Channel 20 Input
11	Channel 21 Input	30	Channel 22 Input
12	Channel 23 Input	31	Channel 24 Input
13	Channel 25 Input	32	Channel 26 Input
14	Channel 27 Input	33	Channel 28 Input
15	Channel 29 Input	34	Channel 30 Input
16	Channel 31 Input	35	Channel 32 Input
17	Analog Ground	36	Program A5
18	Program A6	37	NC
19	Program A7		

PD-929 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Word 3 Bit 1	20	Word 2 Bit 1
2	Word 1 Bit 1	21	Word 3 Bit 2
3	Word 2 Bit 2	22	Word 1 Bit 2
4	Word 3 Bit 3	23	Word 2 Bit 3
5	Word 1 Bit 3	24	Word 3 Bit 4
6	Word 2 Bit 4	25	Word 1 Bit 4
7	Word 3 Bit 5	26	Word 2 Bit 5
8	Word 1 Bit 5	27	Word 3 Bit 6
9	Word 2 Bit 6	28	Word 1 Bit 6
10	Word 3 Bit 7	29	Word 2 Bit 7
11	Word 1 Bit 7	30	Word 3 Bit 8
12	Word 2 Bit 8	31	Word 1 Bit 8
13	Word 3 Bit 9	32	Word 2 Bit 9
14	Word 1 Bit 9	33	Word 3 Bit 10
15	Word 2 Bit 10	34	Word 1 Bit 10
16	Program A3	35	Enable Word 2
17	Program A2	36	Program A5
18	Enable Word 1	37	Program A4
19	Digital Ground		

SD-924 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Serial Channel 5	20	Serial Channel 6
2	Serial Channel 7	21	Serial Channel 8
3	Gated Clock 8	22	Gated Clock 7
4	Gated Clock 6	23	Gated Clock 5
5	Gated Clock 4	24	Gated Clock 3
6	Gated Clock 2	25	Gated Clock 1
7	Serial Channel 4	26	Serial Channel 3
8	Serial Channel 2	27	Serial Channel 1
9	PROG WL1	28	Program A4
10	Digital Ground	29	Program A5
11	PROG WL2	30	Inverted Load 3
12	Inverted Load 4	31	Inverted Load 1
13	Inverted Load 2	32	Inverted Load 7
14	Enable 8	33	Enable 7
15	Enable 6	34	Enable 5
16	Enable 4	35	Enable 2
17	Enable 3	36	Enable 1
18	Inverted Load 6	37	Inverted Load 5
19	Inverted Load 8		

CM-922PB EXTERNAL CONNECTOR PIN-OUT

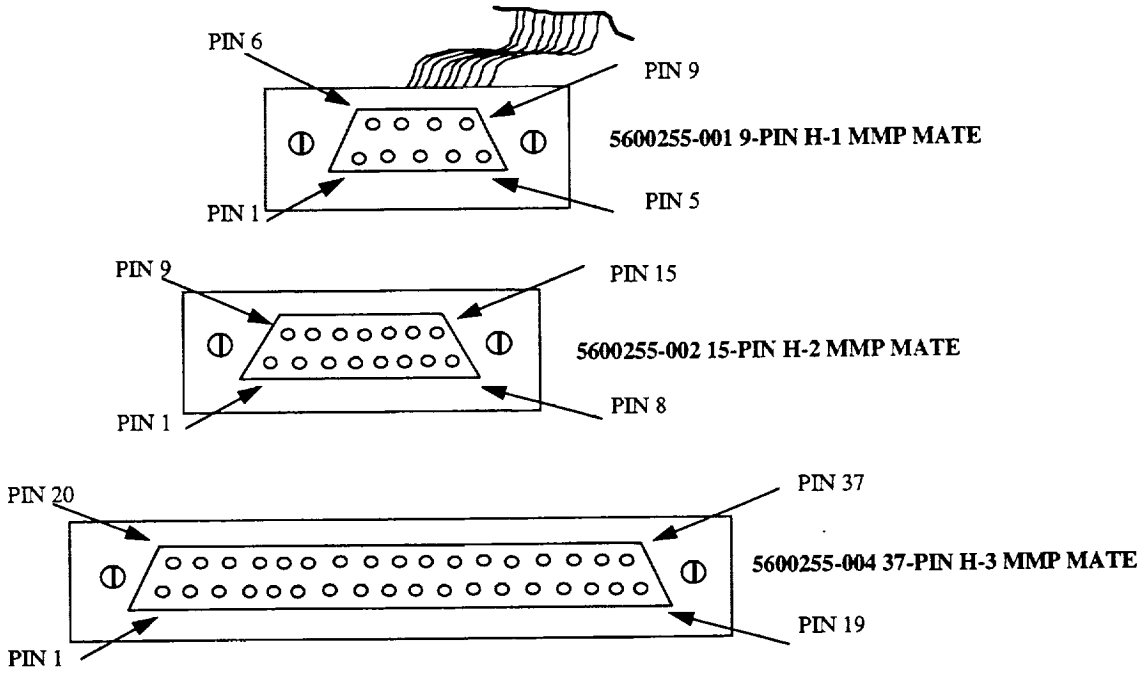
PIN	DESCRIPTION	PIN	DESCRIPTION
1	NC	20	NC
2	NC	21	NC
3	Program A1	22	NC
4	Input #1	23	NC
5	Input #2	24	NC
6	PROG WL1	25	NC
7	Reset Input #1	26	NC
8	NC	27	NC
9	Strobe Output #1	28	NC
10	Strobe Output #2	29	NC
11	PROG WL2	30	NC
12	Reset Input #2	31	NC
13	Program A4	32	NC
14	Program A5	33	NC
15	Complement Reset	34	NC
16	Mode Select	35	NC
17	Program A2	36	NC
18	Program A3	37	NC
19	Digital Ground		

TA-923 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION
1	Event 1 Input
2	Minor Frame Sync Output
3	Major Frame Sync Output
4	Bit Clock Output
5	Word Clock Output
6	Event 0 Input
7	2X Bit Clock Output
8	A3 Programming Pin
9	Ground

TB-925 EXTERNAL CONNECTOR PIN-OUT

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Event 1 Input	20	Event 0 Input
2	Minor Frame Sync Output	21	NC
3	Major Frame Sync Output	22	NC
4	Bit Clock Output	23	NC
5	Word Clock Output	24	NC
6	Minor Frame Counter Output (Bit 2^4)	25	NC
7	Word per Frame Counter Output (Bit 2^1)	26	NC
8	Word per Frame Counter Output (Bit 2^4)	27	NC
9	Word per Frame Counter Output (Bit 2^5)	28	NC
10	Word per Frame Counter Output (Bit 2^3)	29	NC
11	Word per Frame Counter Output (Bit 2^0)	30	NC
12	Word per Frame Counter Output (Bit 2^2)	31	NC
13	2X Bit Clock	32	NC
14	Word per Frame Counter Output (Bit 2^6)	33	NC
15	Word per Frame Counter Output (Bit 2^7)	34	NC
16	Minor Frame Counter Output (Bit 2^0)	35	NC
17	Minor Frame Counter Output (Bit 2^1)	36	Minor Frame Counter Output (Bit 2^2)
18	Minor Frame Counter Output (Bit 2^3)	37	A3 Programming Pin
19	Ground		



External connectors mating sockets view looking into the mating surface of the socket connectors.

GLOSSARY OF TERMS

BIT: A bit is the smallest unit of information in this system. It consists of an on or off condition, effectively, yes or no.

WORD: A word contains 8, 9, or 10 bits of data. The value of the word expresses the value of a single channel of data. The system uses the binary number system so the maximum value of an 8-bit word is 255 and so on.

FRAME: A frame begins with the frame synchronization pattern and continues up to, but not including, the next frame synchronization pattern.

MAJOR FRAME: A major frame is made up of multiple minor frames in a subcommutated format. One complete sampling history is contained in one major frame.

MINOR FRAME: Minor frames appear when subcommutation is used. A minor frame begins with the frame synchronization pattern and continues up to, but not including, the next frame synchronization pattern. In effect, a minor frame is equal to a frame in length and is only present when subcommutation is used. Minor frames are often referred to as subframes.

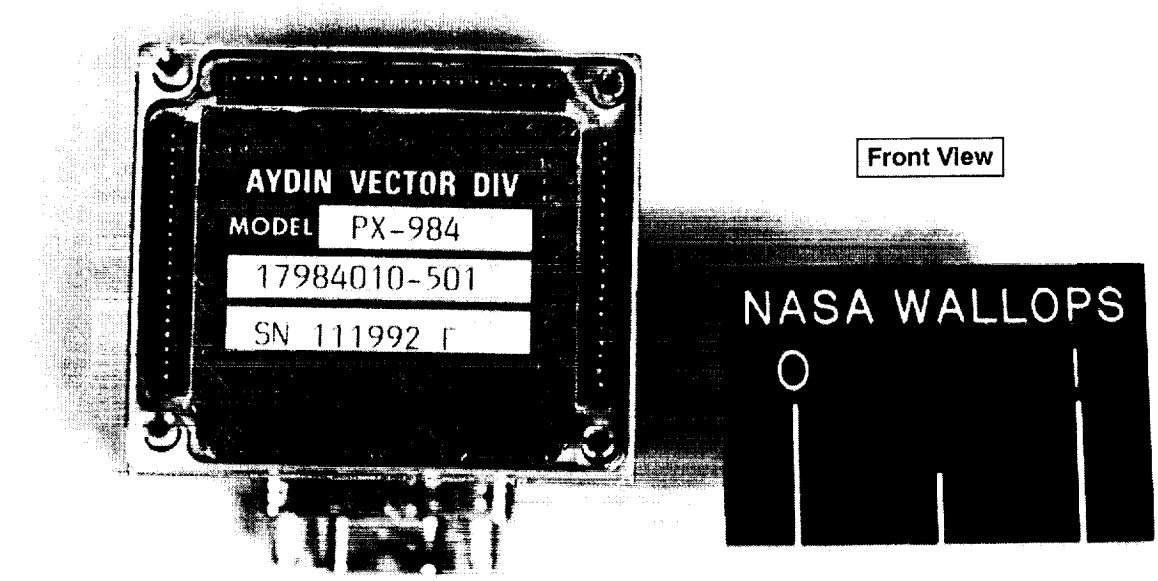
MAINFRAME RATE: One sample per minor frame in a subcommutated format is a mainframe sampling rate and one sample in a major frame if subcommutation is not used is also a mainframe sampling rate.

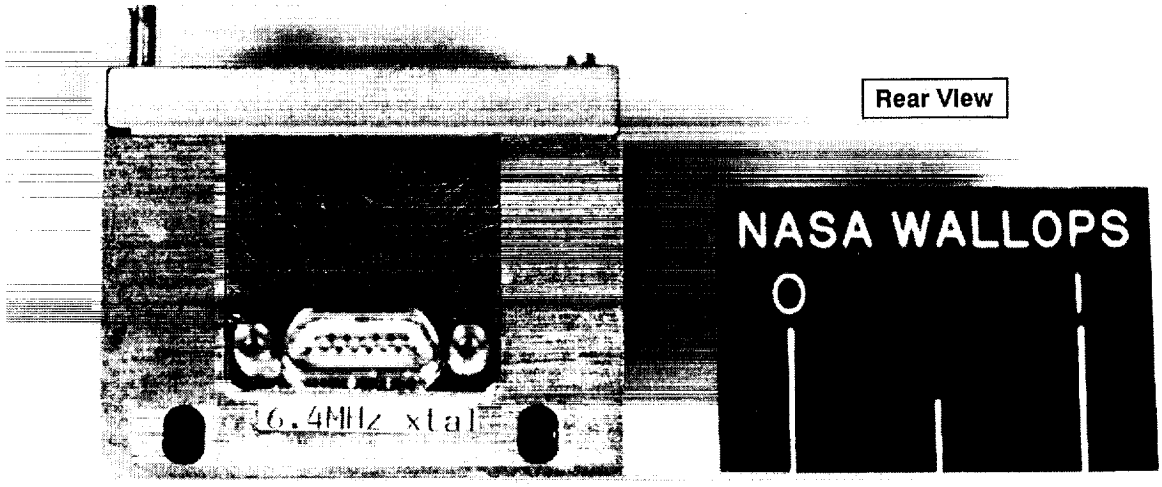
SUBCOMMUTATED DATA: This is data sampled at a rate less than the mainframe sampling rate. A subcommutated data channel is not sampled in every minor frame.

SUPERCOMMUTATED DATA: This is data that is sampled at a rate greater than the mainframe rate. Supercommutated data is sampled more than one time per minor frame in a subcommutated format and is sampled more than one time per frame if subcommutation is not used.

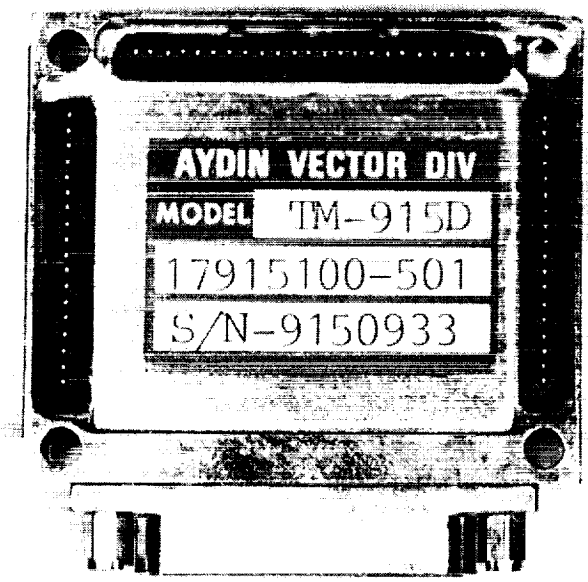
Appendix C

MMP-900 PCM ENCODER MODULES

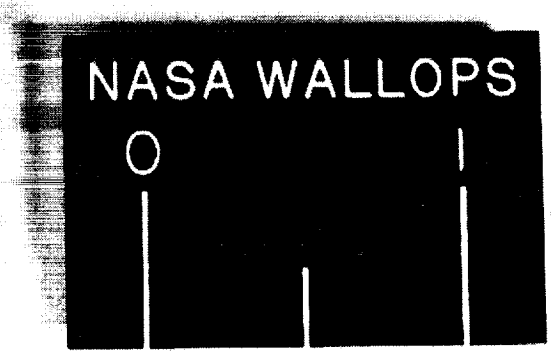


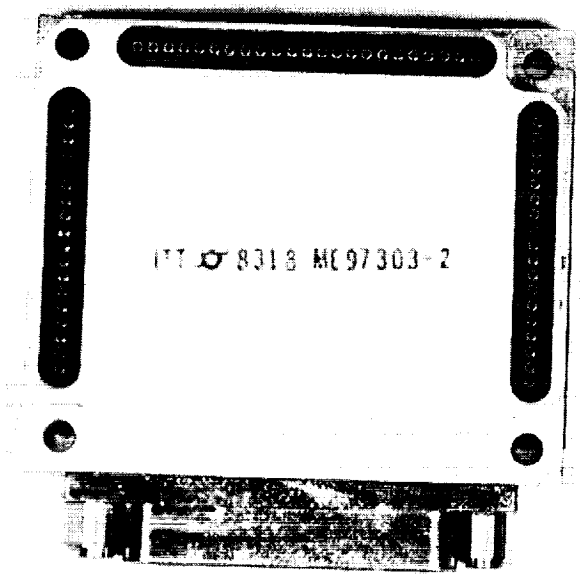


PX-984 POWER SUPPLY MODULE

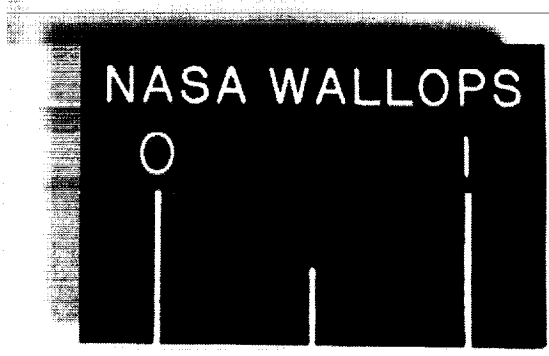


Front View

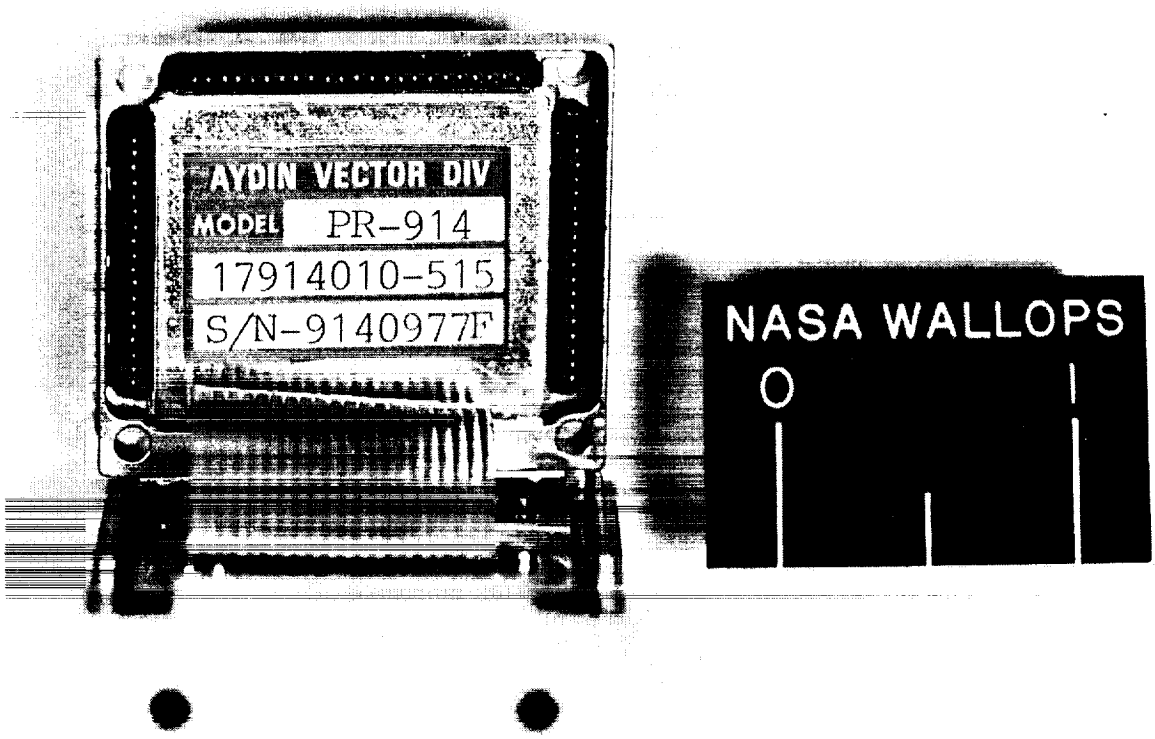




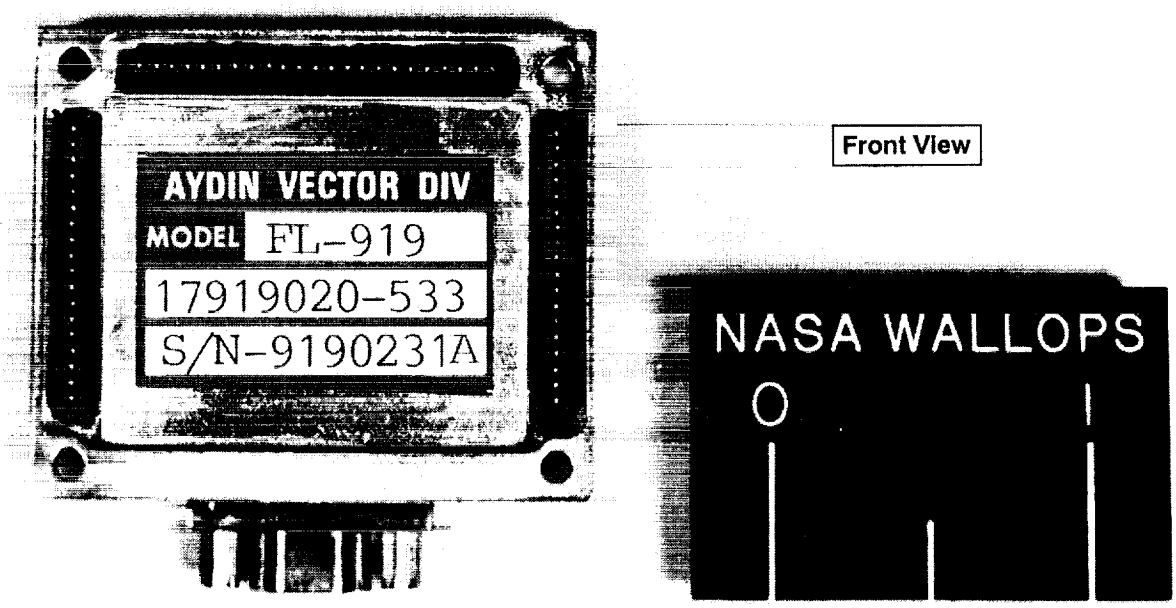
Rear View

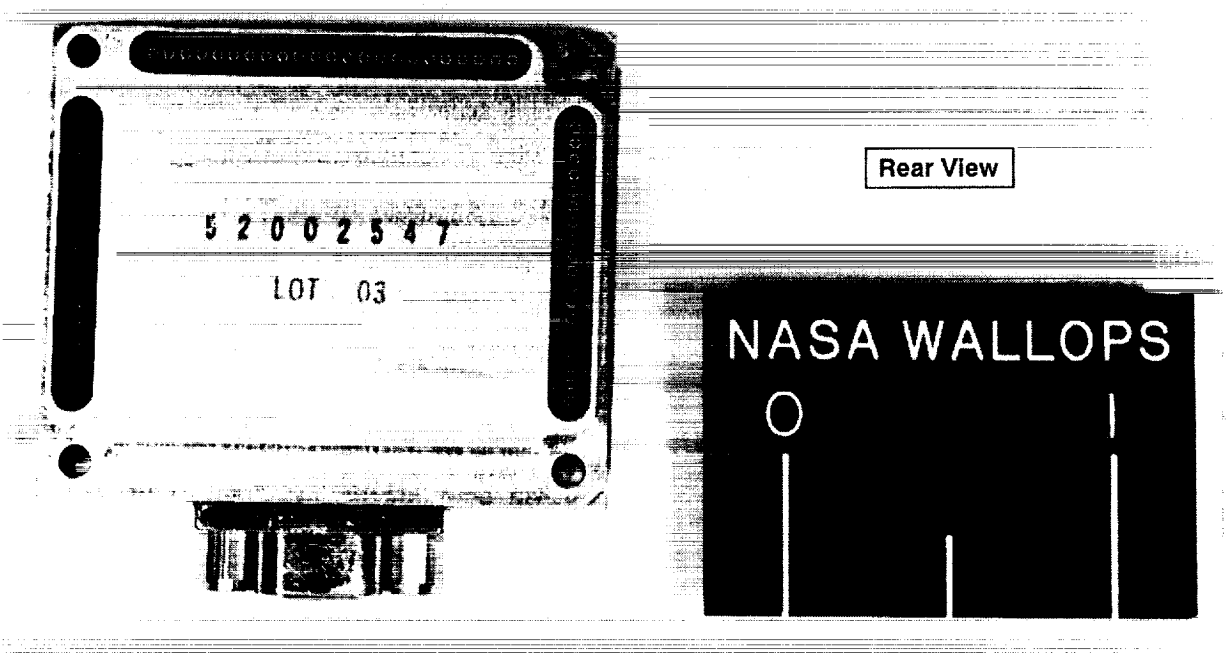


TM-915D TIMER MODULE

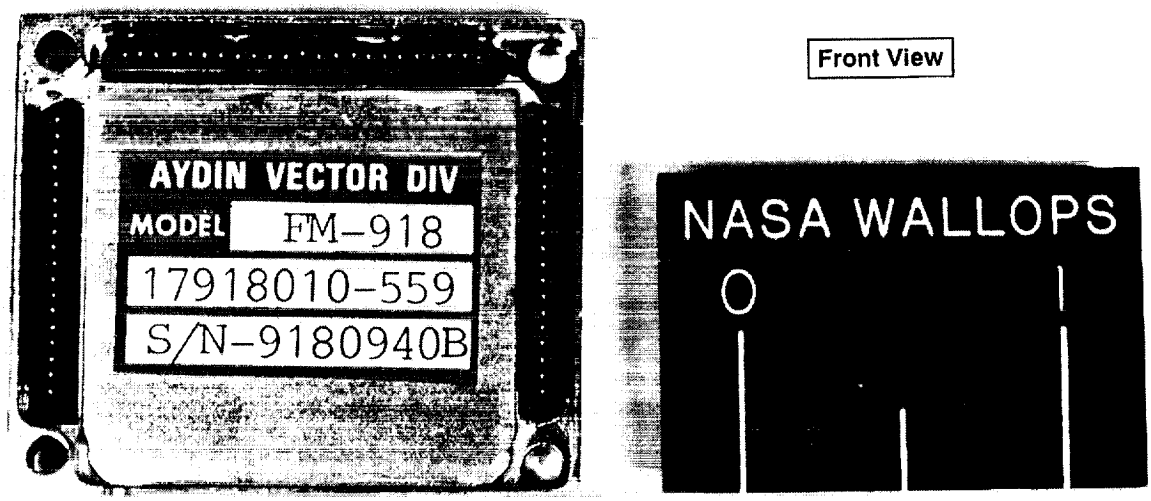


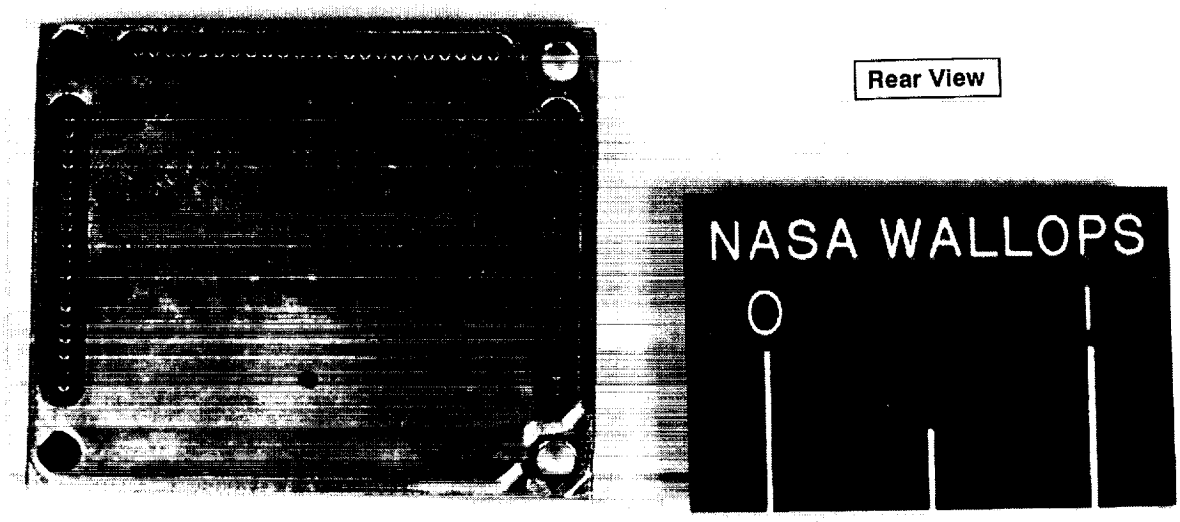
PR-914 PROCESSOR & EP-912 END PLATE MODULES



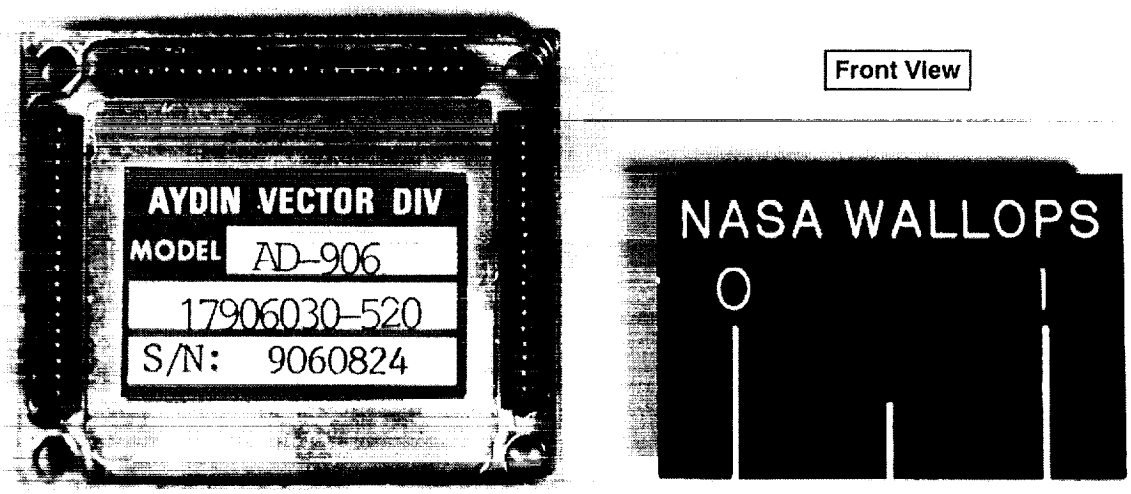


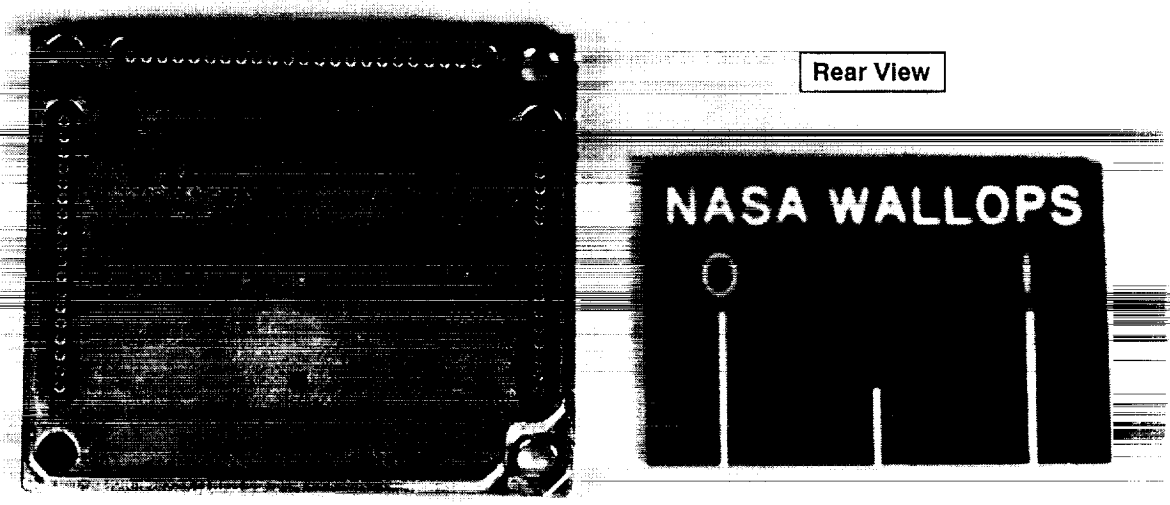
FL-919A QUAD FILTER MODULE





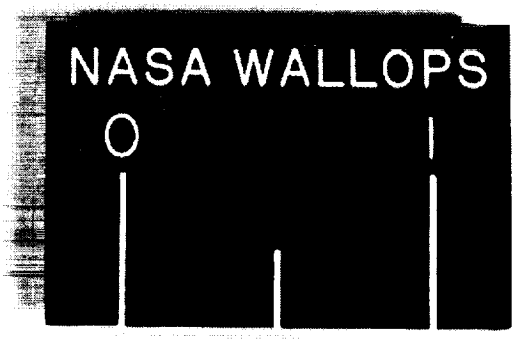
FM-918 FORMATTER MODULE

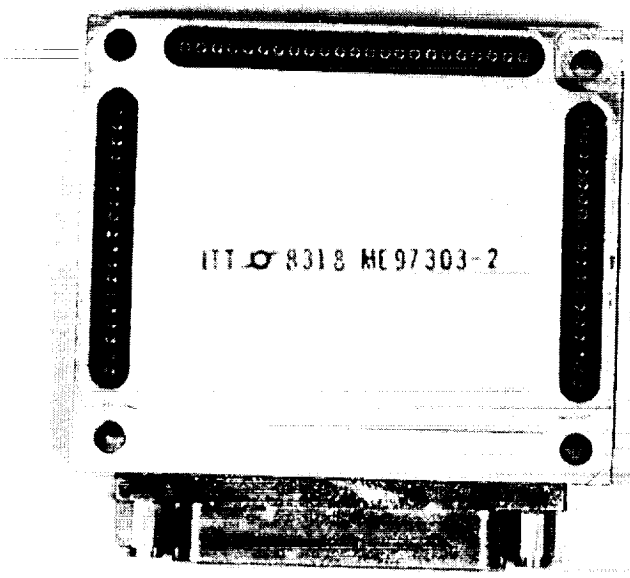




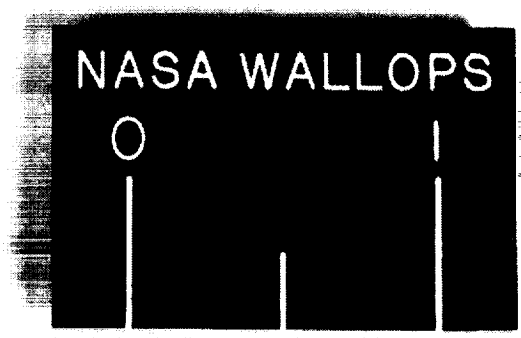
AD-906 SAMPLE & HOLD AND ANALOG TO DIGITAL CONVERTER MODULE

Front View

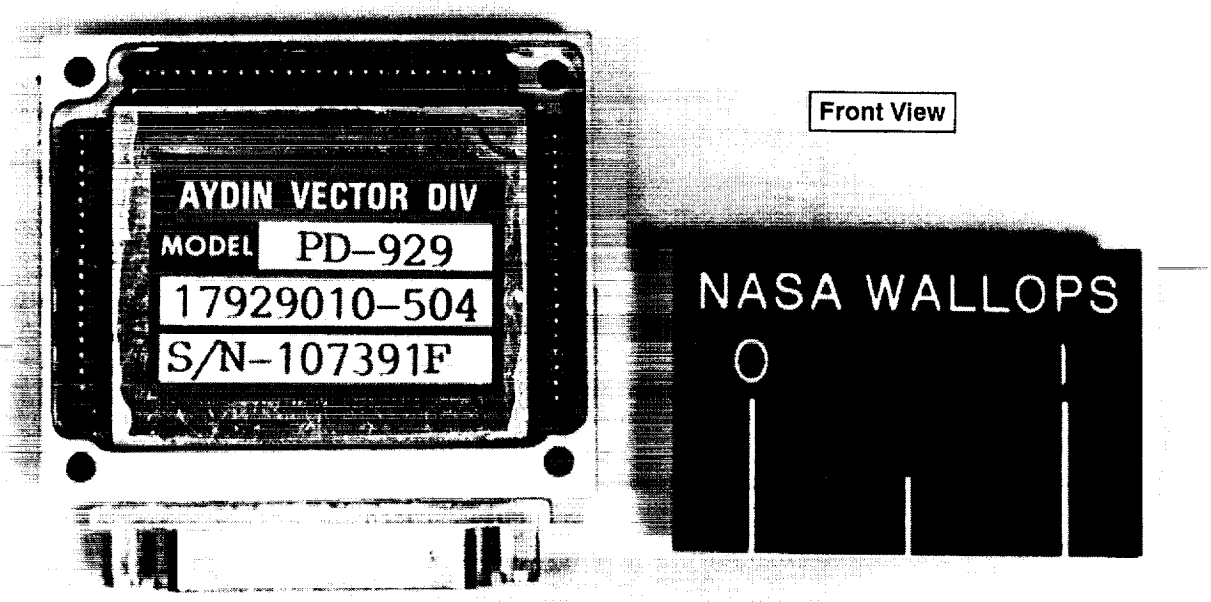


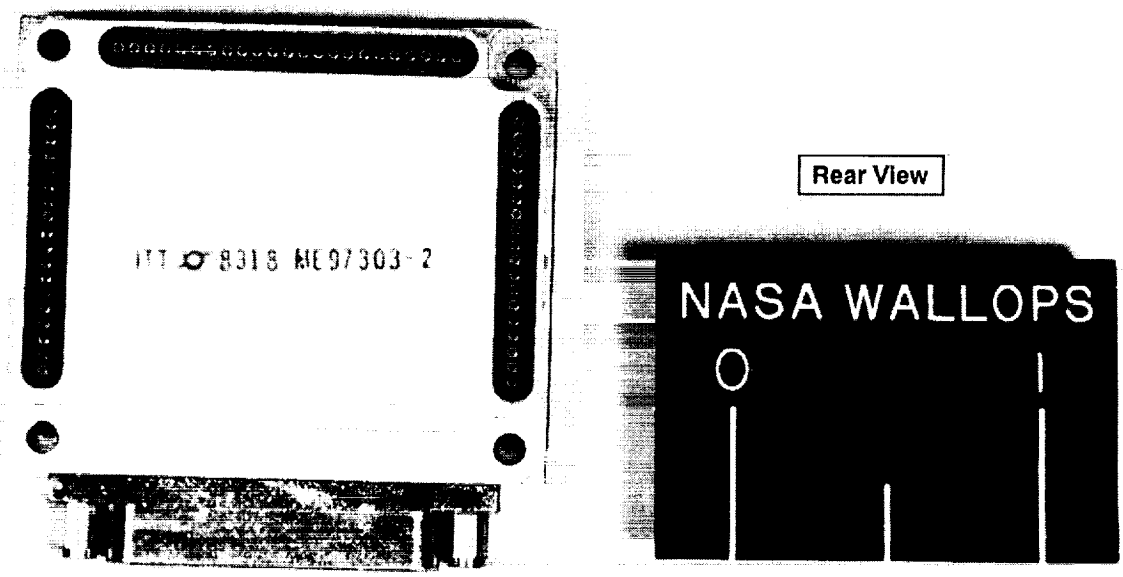


Rear View

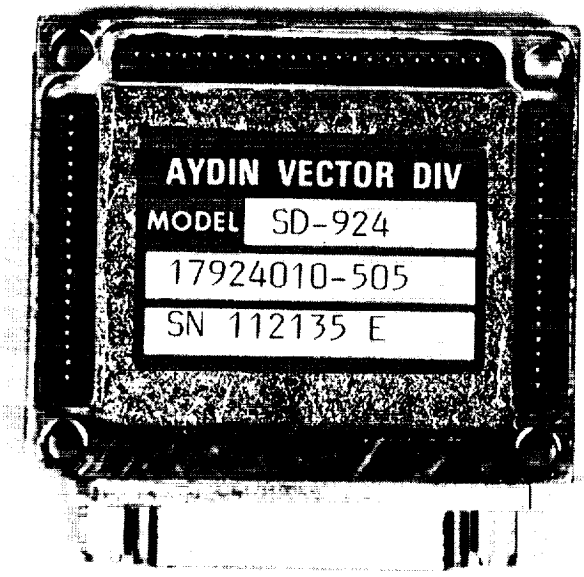


MP-901 32-CHANNEL HIGH LEVEL MULTIPLEXER MODULE





PD-929 PARALLEL DIGITAL DATA MULTIPLEXER MODULE



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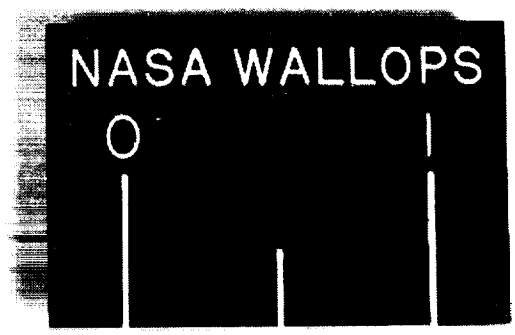

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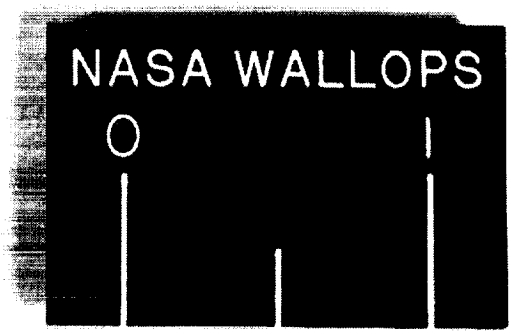
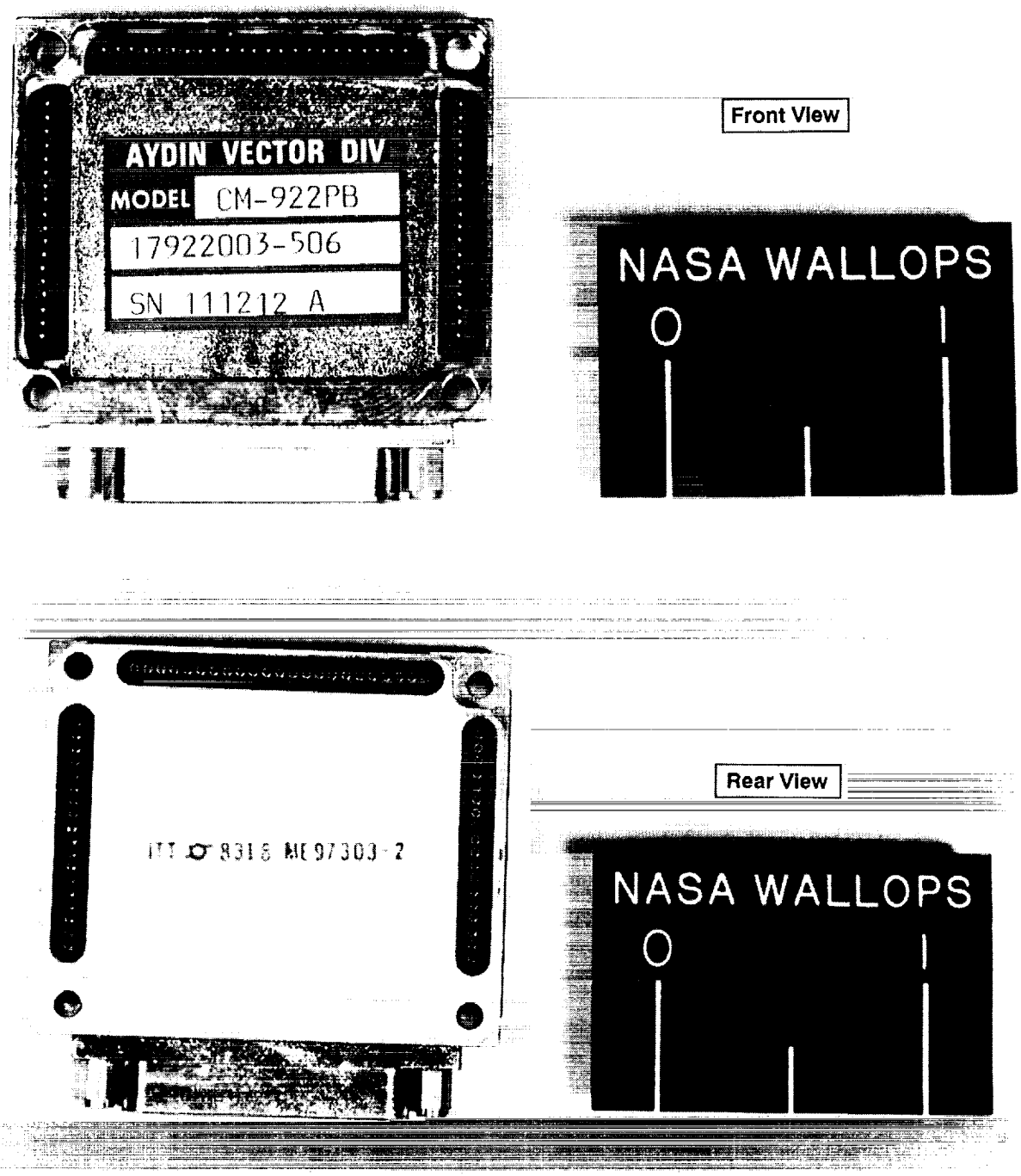
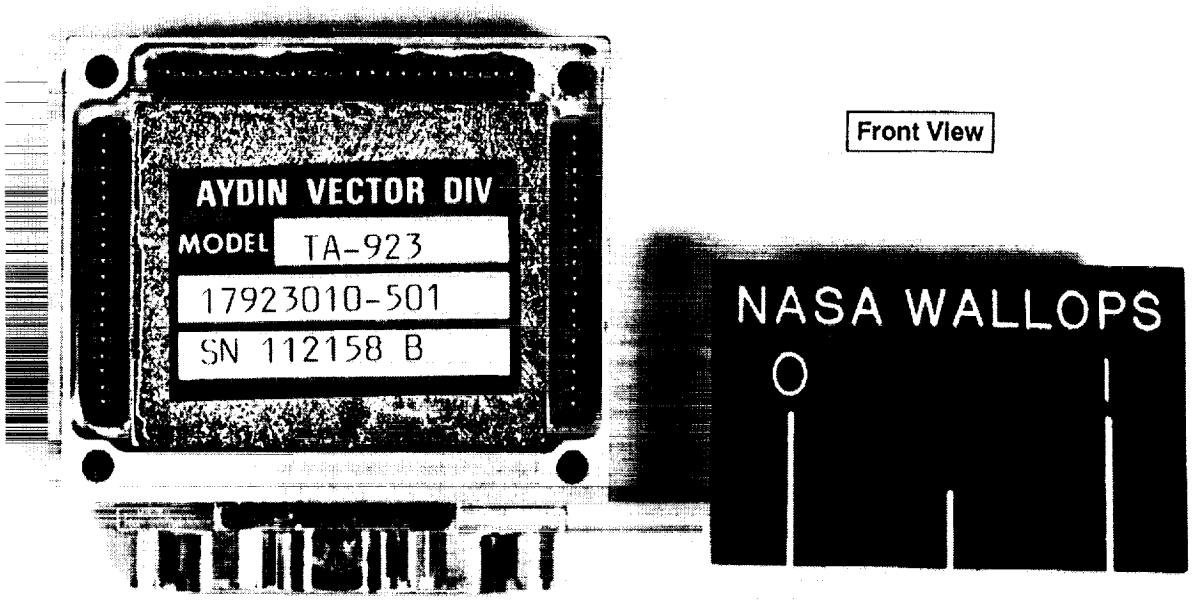
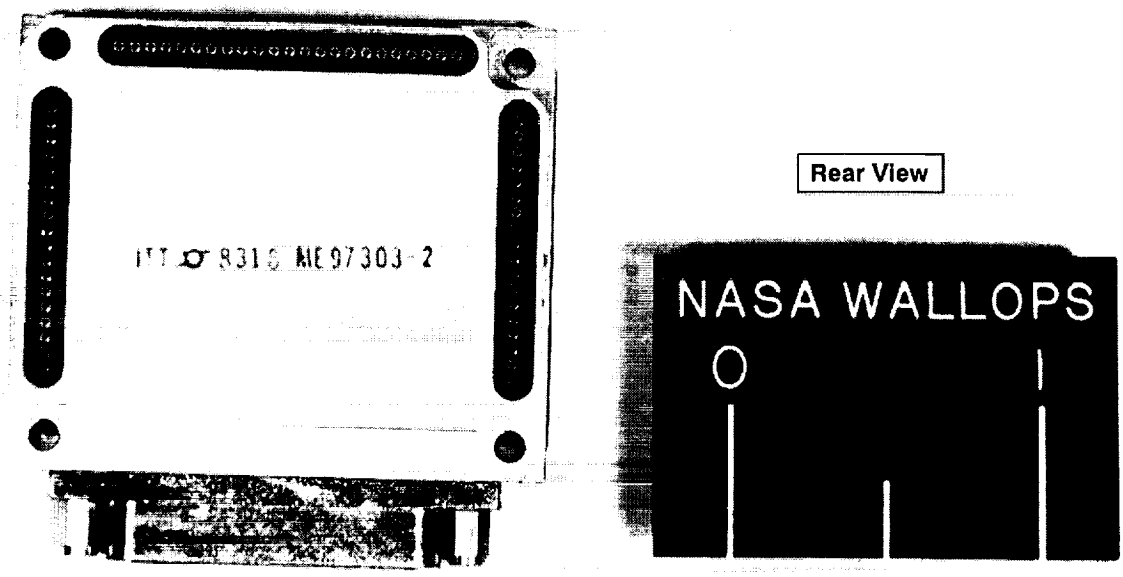


SD-924 SERIAL DIGITAL DATA MULTIPLEXER MODULE



CM-922PB DUAL COUNTER/ACCUMULATOR MODULE





TA-923 TIME EVENT MONITOR WITH ALTERNATING REGISTERS MODULE

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13. ABSTRACT *(Maximum 200 words)*

This handbook explicates the hardware and software properties of a time division multiplex system. This system is used to sample analog and digital data. The data is then merged with frame synchronization information to produce a serial pulse coded modulation (PCM) bit stream.

Information in this handbook is required by users to design congruous interface and attest effective utilization of this encoder system.

Aydin Vector provides all of the components for these systems to Goddard Space Flight Center/Wallops Flight Facility.

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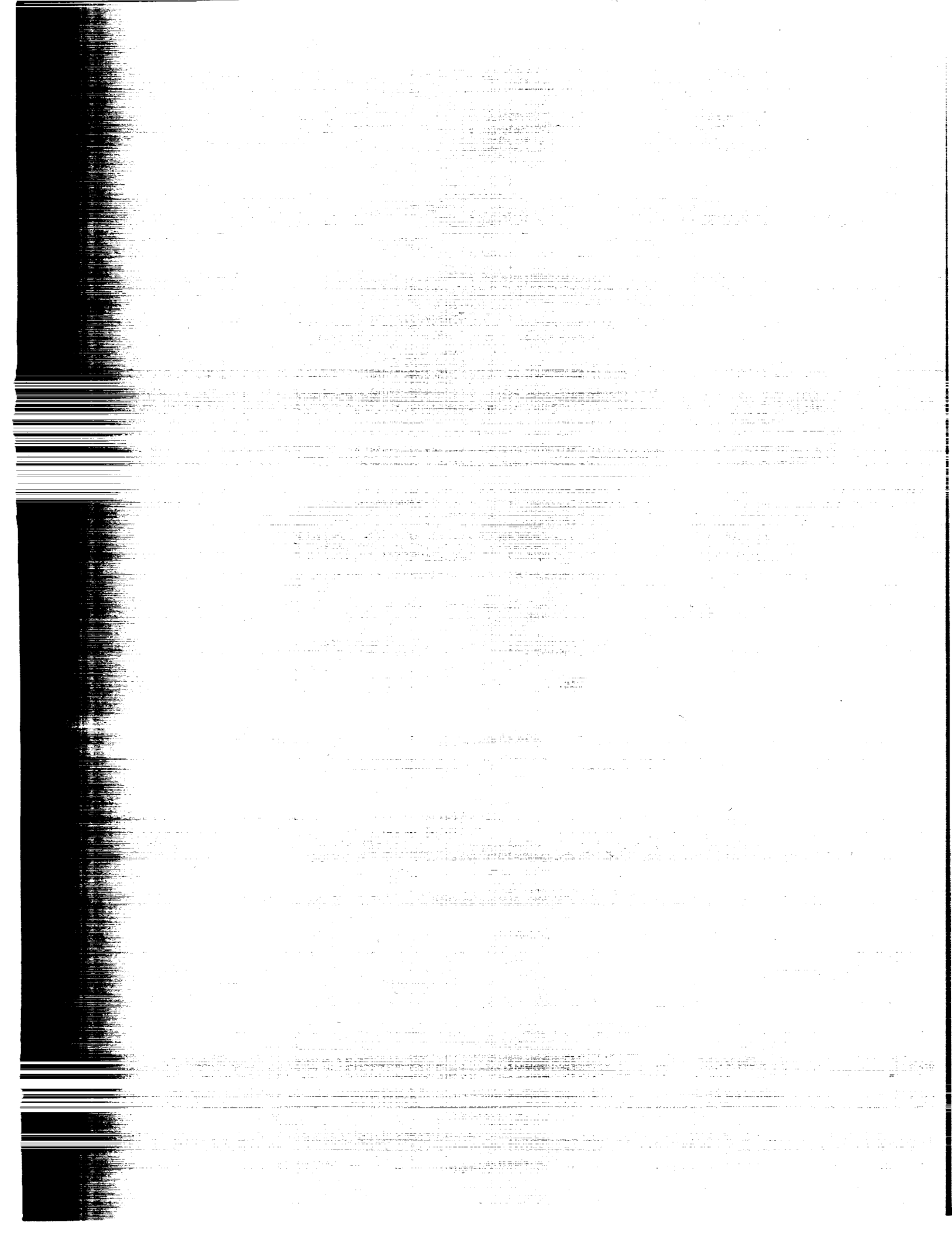

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