FABRICATION OF LARGE-AREA CCD DETECTORS ON HIGH-PURITY, FLOAT-ZONE SILICON*

J.A. Gregory, B.E. Burke, M.J. Cooper,
R.W. Mountain, and B.B. Kosicki

Lincoln Laboratory
Massachusetts Institute of Technology
Lexington, Massachusetts 02173-9108

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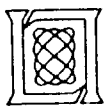


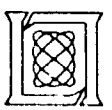
256967-1

OUTLINE

- INTRODUCTION
  - 1024 × 1024 CCD IMAGER
  - AXAF MISSION
- PRESENCE OF DISLOCATIONS IN IMAGERS
  - DARK CURRENT IMAGE
  - STRUCTURAL EVIDENCE
  - CHARACTERIZATION OF DISLOCATION TRAPS
- CONTROLLING DISLOCATIONS
  - CAUSES OF SLIP
  - DISLOCATION-FREE PROCESS DEVELOPMENT
- RESULTS
  - DARK CURRENT IMAGE
  - CTE
  - ENERGY RESOLUTION
- CONCLUSIONS

AXAF REQUIREMENTS OF CCD IMAGER

- LOW-NOISE ($<2e^-$), HIGH SENSITIVITY (20 $\mu V/e^-$) OUTPUT CIRCUIT
- 2 μm TROUGHS FOR HARDENING TO DISPLACEMENT DAMAGE
- HIGH QUANTUM EFFICIENCY FOR PHOTONS BETWEEN 0.25 keV AND 10 keV
- FABRICATED ON 6 – 10 kΩ-cm Si FOR DEEP DEPLETION



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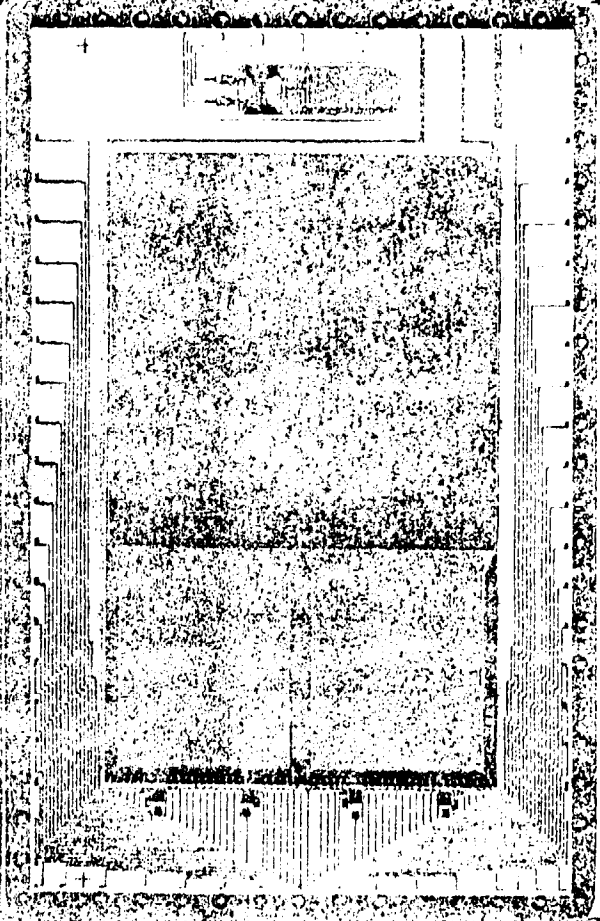
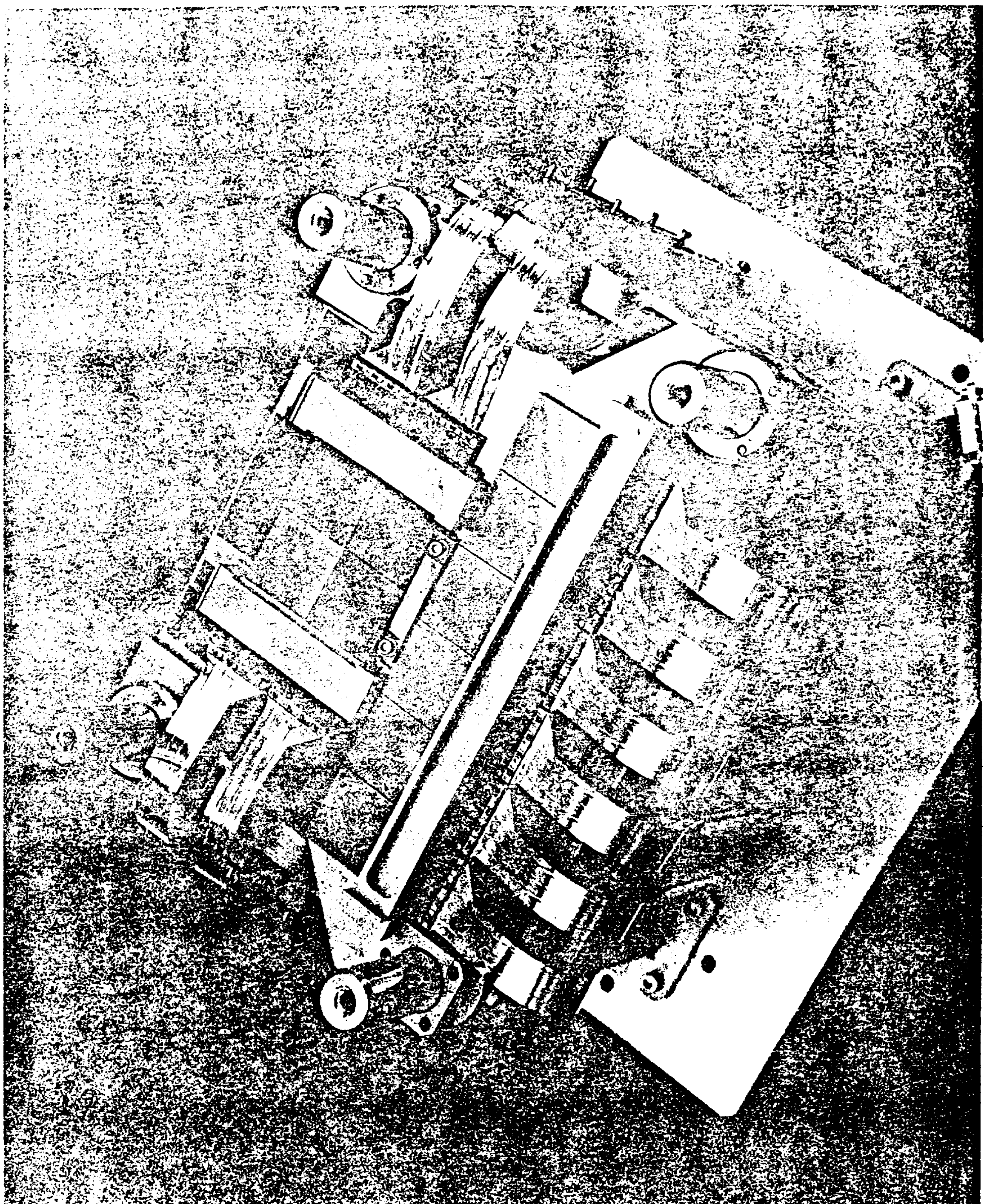
These figures describe the basic structure and the design features of a 1024X1024 CCD imager to be used as a soft x-ray sensor on the Advanced X-ray Astronomical Facility (AXAF). This sensor must have low noise and low charge transfer inefficiency for good energy resolution, deep depletion for efficient detection of x-rays > 5 keV, and must be radiation hardened to withstand radiation damage from energetic particles in space. This device is abuttable on three sides of the imaging array, and this feature will be used in making the two multi-chip arrays for AXAF.

1024 × 1024 FRAME-TRANSFER IMAGER

- 24 × 24 μm PIXELS
- TRIPLE-POLY Si, n-BURIED CHANNEL
- THREE SIDE ABUTTABLE
- TWO OR FOUR PORT OPERATION
- FRONT- OR BACK-ILLUMINATED





This figure depicts the CCD focal-plane assembly for ACIS (AXAF CCD Imaging Spectrometer) A 2×2-chip array is to be used for spectroscopic imaging while the 1×6 array will detect x-rays from a dispersive spectrometer. Both arrays must be slightly curved to best match the x-ray optics. The packaging of these arrays requires precise positioning which must be maintained through launch.

We are developing at Lincoln Laboratory the packaging techniques for this focal plane. One of the key features of our approach is that individual devices may be replaced should they become damaged or found to be defective. The gaps between the pixels on adjacent chips will be less than 500 μm, and the placement accuracy will be on the order of 25 μm.

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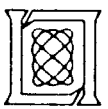
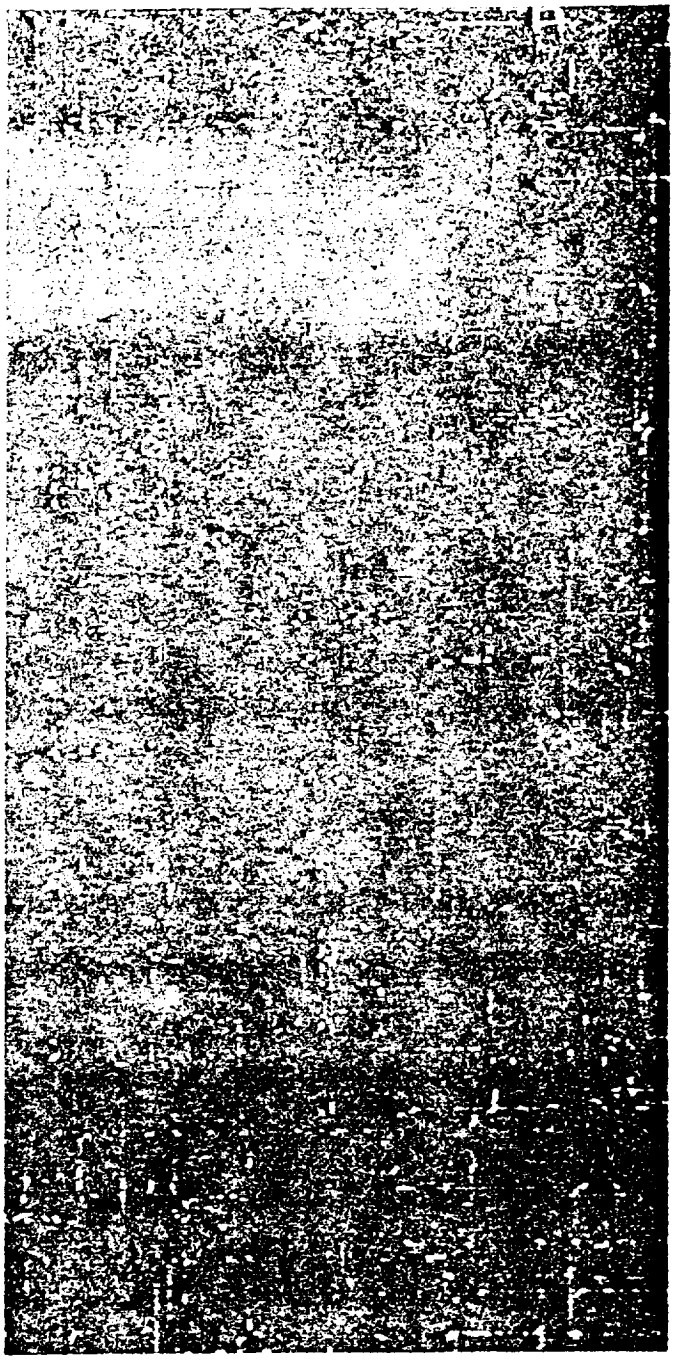
  - CHARACTERIZATION OF DISLOCATION TRAPS
- CONTROLLING DISLOCATIONS
- RESULTS
- CONCLUSIONS

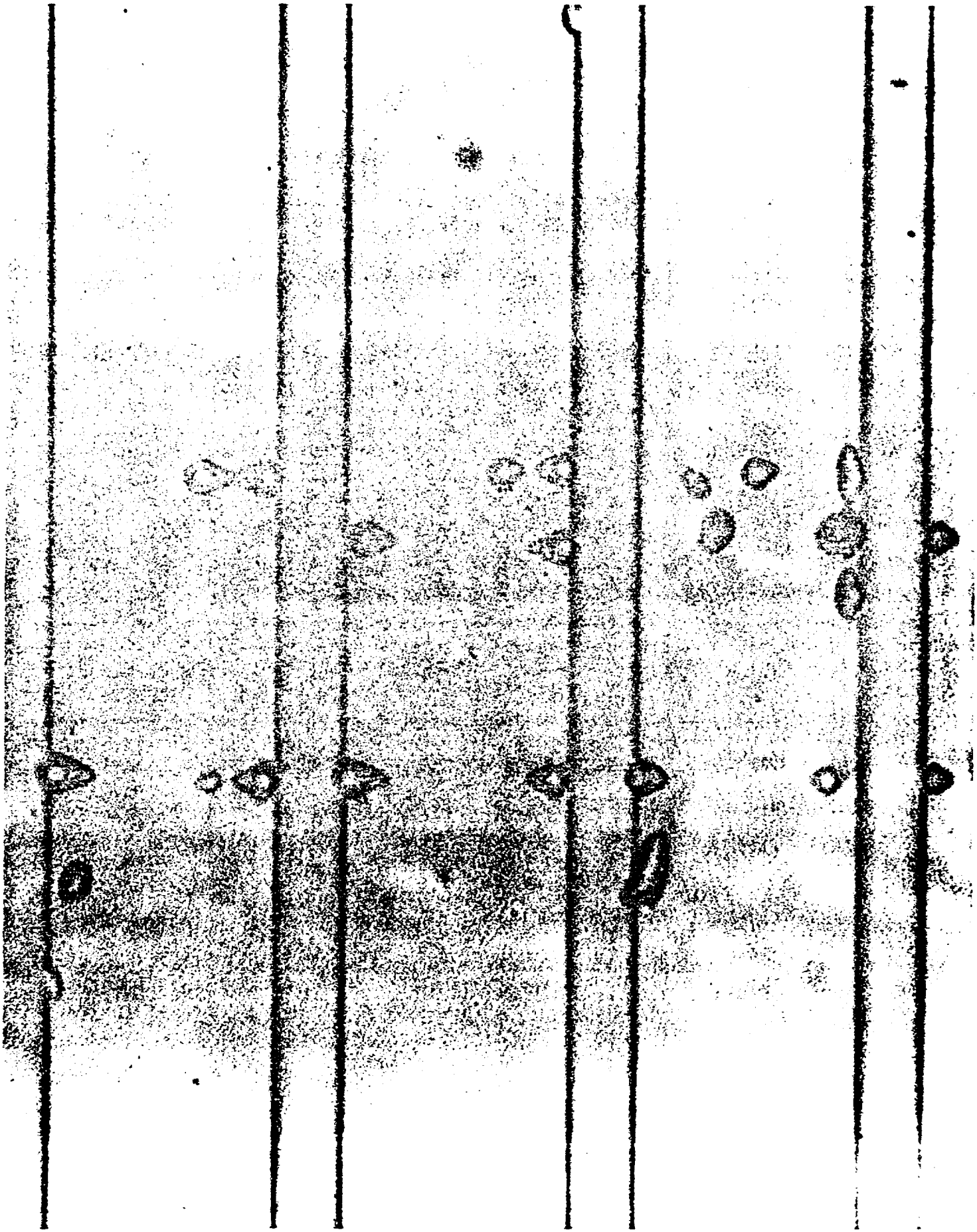


256967-3



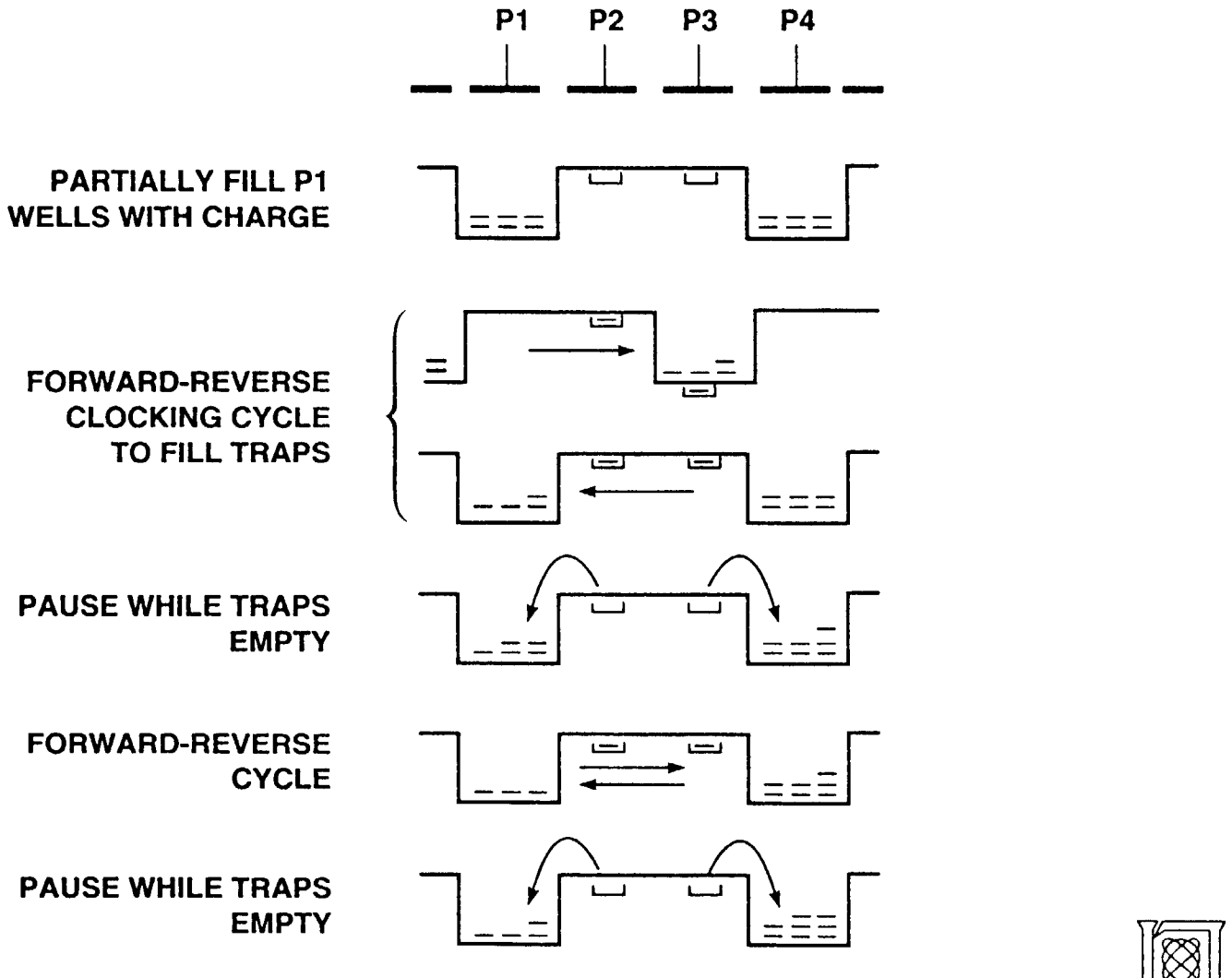
This dark current image of a device shows the enhanced generation current due to dislocations. This image illustrates the propagation of slip dislocations across the wafer <110> directions.

The dislocations also cause the charge transfer inefficiency to rise from 1×10^{-6} to well over 1×10^{-5}.



This is a photo of a portion of a device after the polysilicon gates, SiO_2, and Si_3N_4 layers have been removed down to the silicon substrate. The horizontal lines correspond to the LOCOS channel stops. The device was then etched lightly to reveal dislocations, seen here as oval or comma-shaped pits. The pits tend to line up along and orthogonal to the channel stops. Many of the dislocations occur at the edge of the LOCOS where the stresses are highest.

MEASURING PROPERTIES OF TRAP LEVELS IN CCD

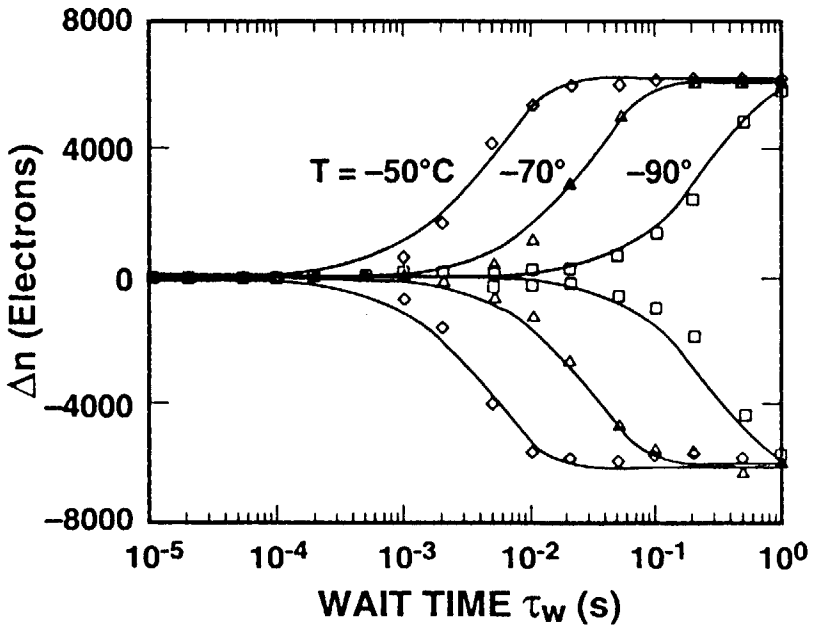


257036-4

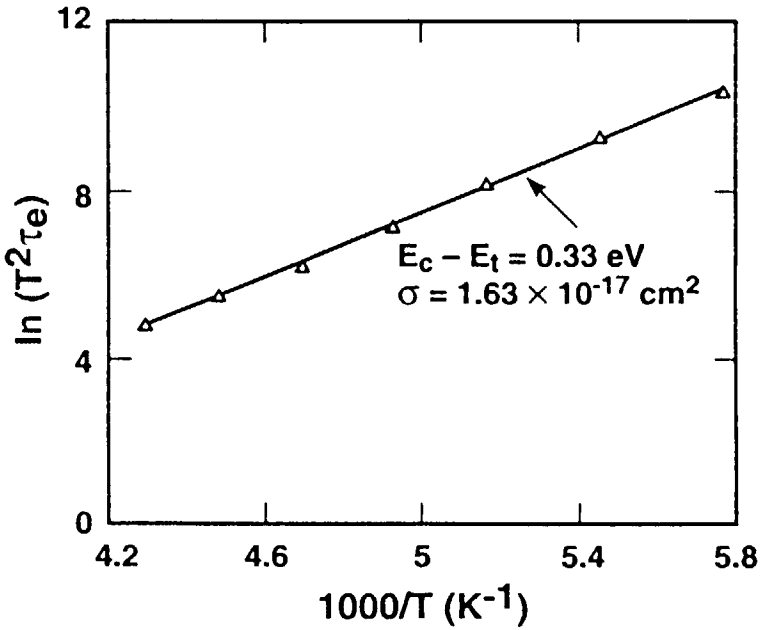
This viewgraph indicates the technique used to locate the position of traps in the CCD by multi-reversal clocking. The presence of traps transfers charge between charge wells. This transfer can be monitored and analyzed to derive the fundamental properties of the traps.

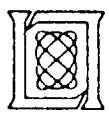
MEASUREMENT OF DISLOCATION TRAP PARAMETERS

CHARGE SURPLUS/DEFICIT FROM MULTIREVERSAL CLOCKING PAST TRAP



TEMPERATURE DEPENDENCE OF DISLOCATION TRAP EMISSION TIME





257036-5

The figure on the left of the viewgraph indicates the number of electrons that are transferred between potential wells during multi-reversal clocking at various temperatures. The figure on the right plots charge surplus data as a function of temperature to obtain the activation energy and capture cross section of the trap.

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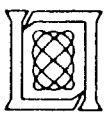
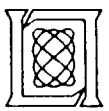
  - CAUSES OF SLIP
  - DISLOCATION-FREE PROCESS DEVELOPMENT
- RESULTS
- CONCLUSIONS



INTRODUCTION OF GLISSILE DISLOCATIONS DURING FABRICATION OF AXAF CCD IMAGERS

- SUSCEPTIBILITY OF FLOAT ZONE Si TO PLASTIC DEFORMATION
  - DEEP-DEPLETION REQUIREMENTS DICTATE USE OF HIGH RESISTIVITY, FLOAT-ZONE Si
  - FLOAT-ZONE Si LACKS INTERSTITIAL O ATOMS THAT PIN DISLOCATIONS IN CZOCHRALSKI Si
- SOURCES OF STRESS DURING FABRICATION
  - THERMAL GRADIENTS WHERE WAFER CONTACTS FURNACE BOAT
  - THERMAL GRADIENTS INDUCED BY WAFER INSERTION / WITHDRAWAL AND FURNACE RAMPING
  - FORCES IMPOSED BY INTRINSIC STRESSES IN OVERLYING MATERIALS



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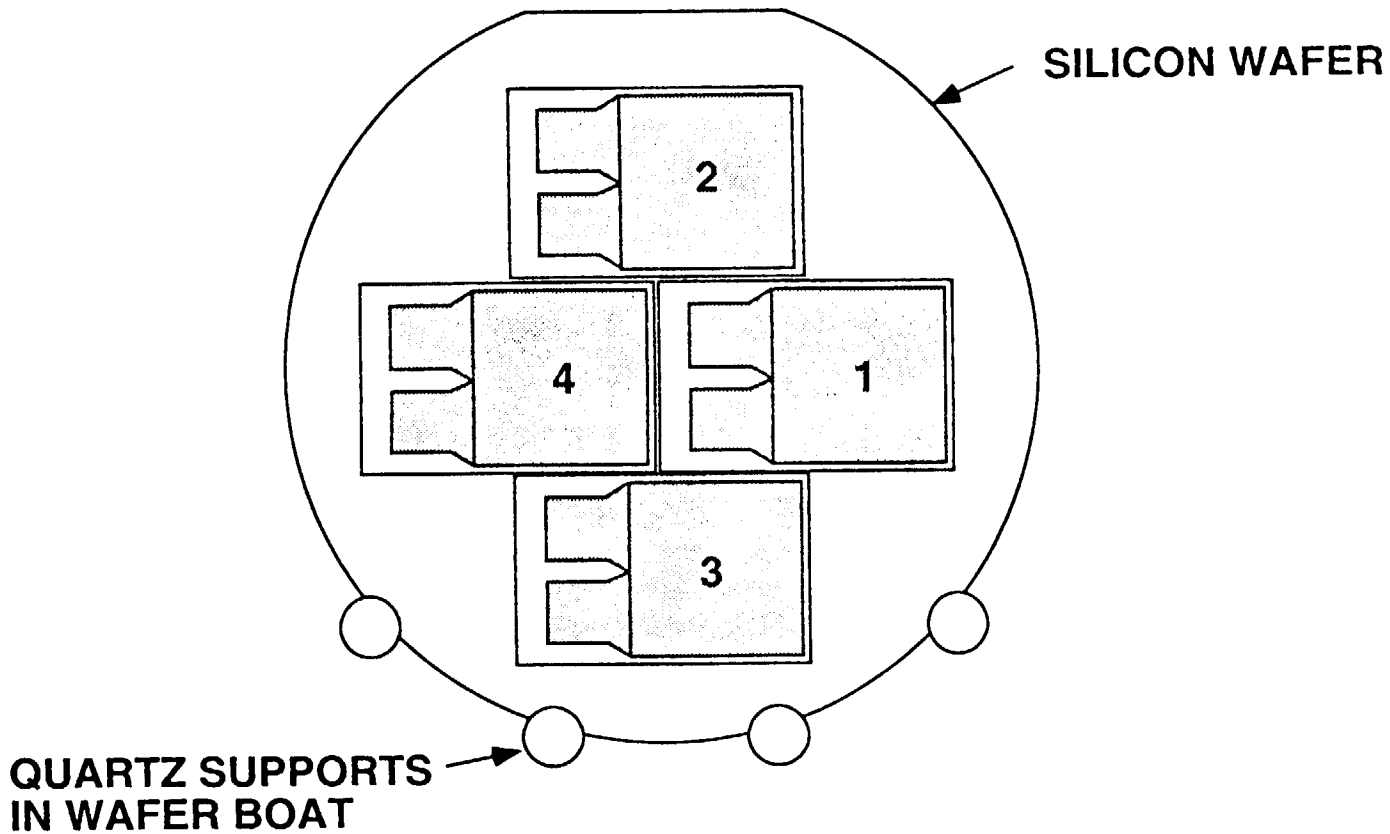
This viewgraph indicates why float-zone Si is susceptible to plastic deformation and lists some of the specific sources of stress induced during integrated circuit processing.

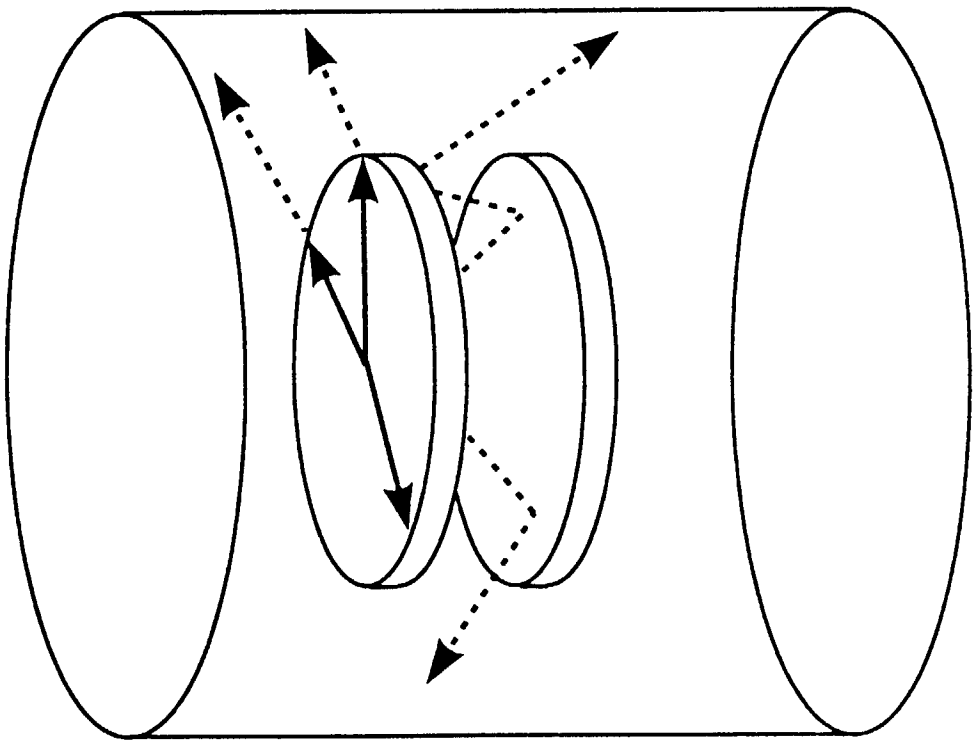
LOADING OF DEVICE WAFERS IN PROCESS FURNACE

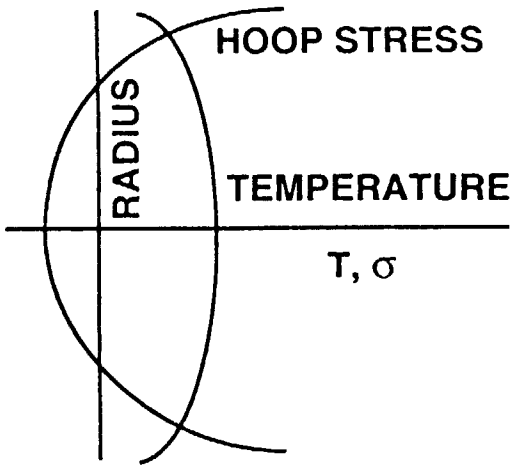


257036-1

This drawing depicts the quartz wafer boat used for high-temperature processing of the device whose dark current image is shown above. The wafers are supported by grooves in four quartz rods that form the wafer boat. During furnace insertion and removal the silicon wafers heat and cool faster than the more massive wafer boat and result in temperature gradients across the wafer. These gradients produce stresses that initiate defects near the points where the wafers are supported by the boat. The density of dislocations is highest at these points; the density decreases as dislocations propagate across the wafer.

HEAT FLOW AND TEMPERATURE PROFILE OF WAFER DURING COOLING





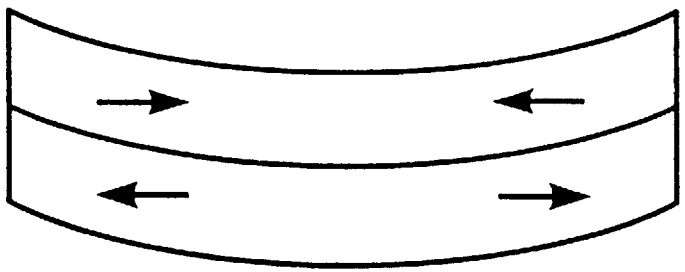
CONDUCTION

RADIATION

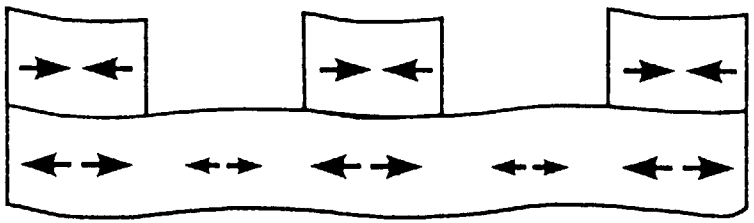
257036-2

This figure indicates how heat flow from a wafer to the furnace walls is limited by radiation from the edge of the wafer. This dependence leads to a radial gradient in temperature and, in turn, to a hoop stress in the wafer.

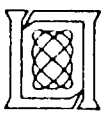
STRESS INDUCED BY OVERLYING FILMS



- FORCES INDUCED BY COUPLE OF MATERIALS IN COMPRESSION AND TENSION



- FORCES AND REACTION
- FORCES INDUCED BY PATTERNED COUPLE OF MATERIALS IN COMPRESSION AND TENSION

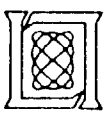


257036-3

This viewgraph shows how stress can arise from material couples that are in tension and compression. On the left, uniform films lead to simple bowing of the couple, while on the right, patterning the films lead to warping of the couple and to high stress levels at the pattern edges. This situation pertains to wafer processing after stressed films have been etched.

DEVELOPMENT OF DISLOCATION-FREE PROCESS FOR CCD SENSORS

- EMPLOY POLYSILICON BOATS
- SLOW WAFER INSERTION / WITHDRAWAL
- SLOW FURNACE RAMPING
- REDUCE FORCES DUE TO INTRINSIC STRESS



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This viewgraph lists measures which can be taken to eliminate the incidence of plastic deformation during wafer processing. These procedures reduce the strength of any forces arising due to temperature differentials or to intrinsic stresses in the materials on the wafer.

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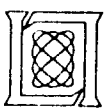
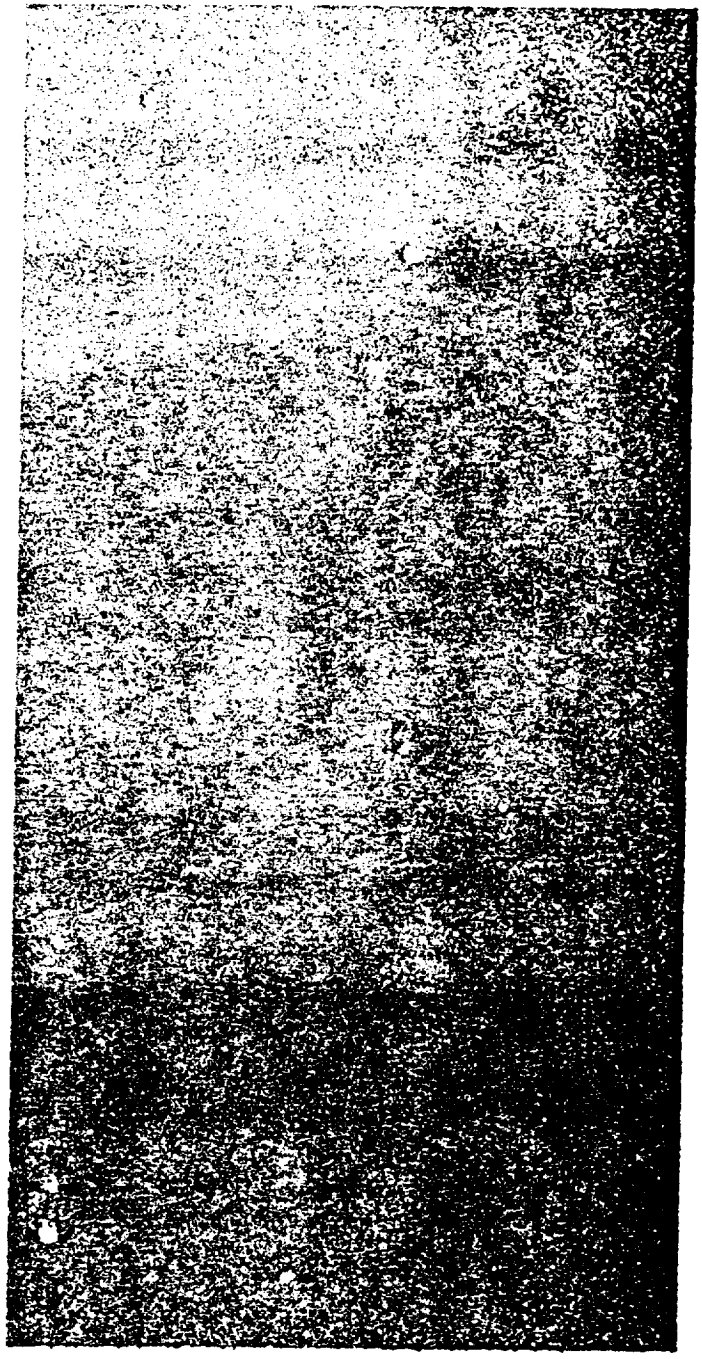
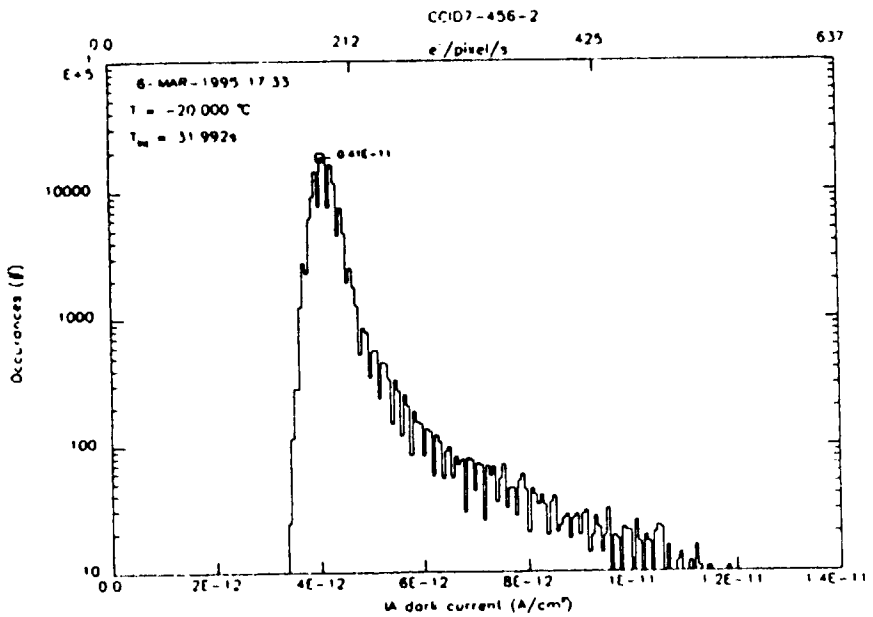


256967-5

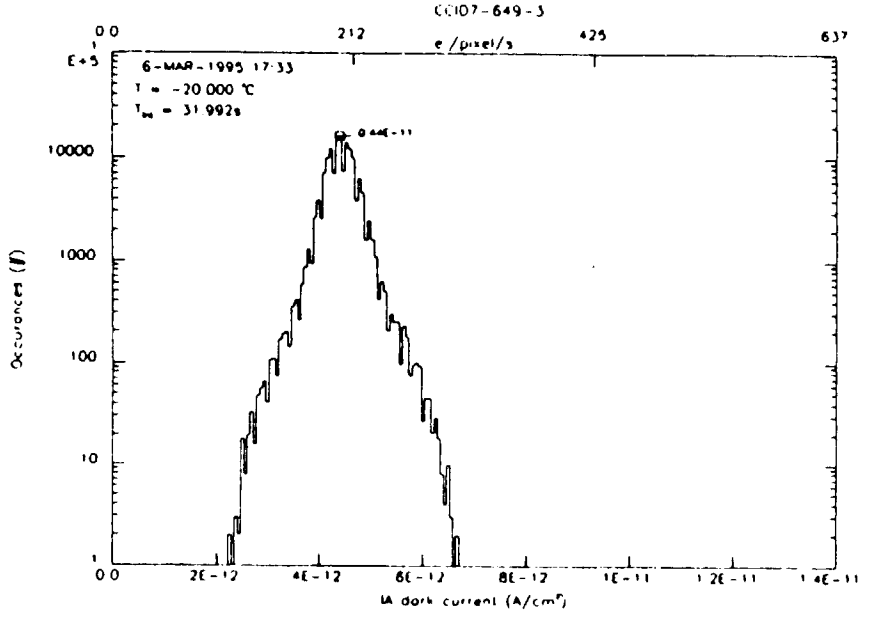


This dark current image of a device shows that no pixels have enhanced electron generation due to dislocations, indicating our processing changes have been successful. The bright spots are due to cosmic rays.

DARK CURRENT DISTRIBUTION
(NON-INVERTED MODE, –20 °C)



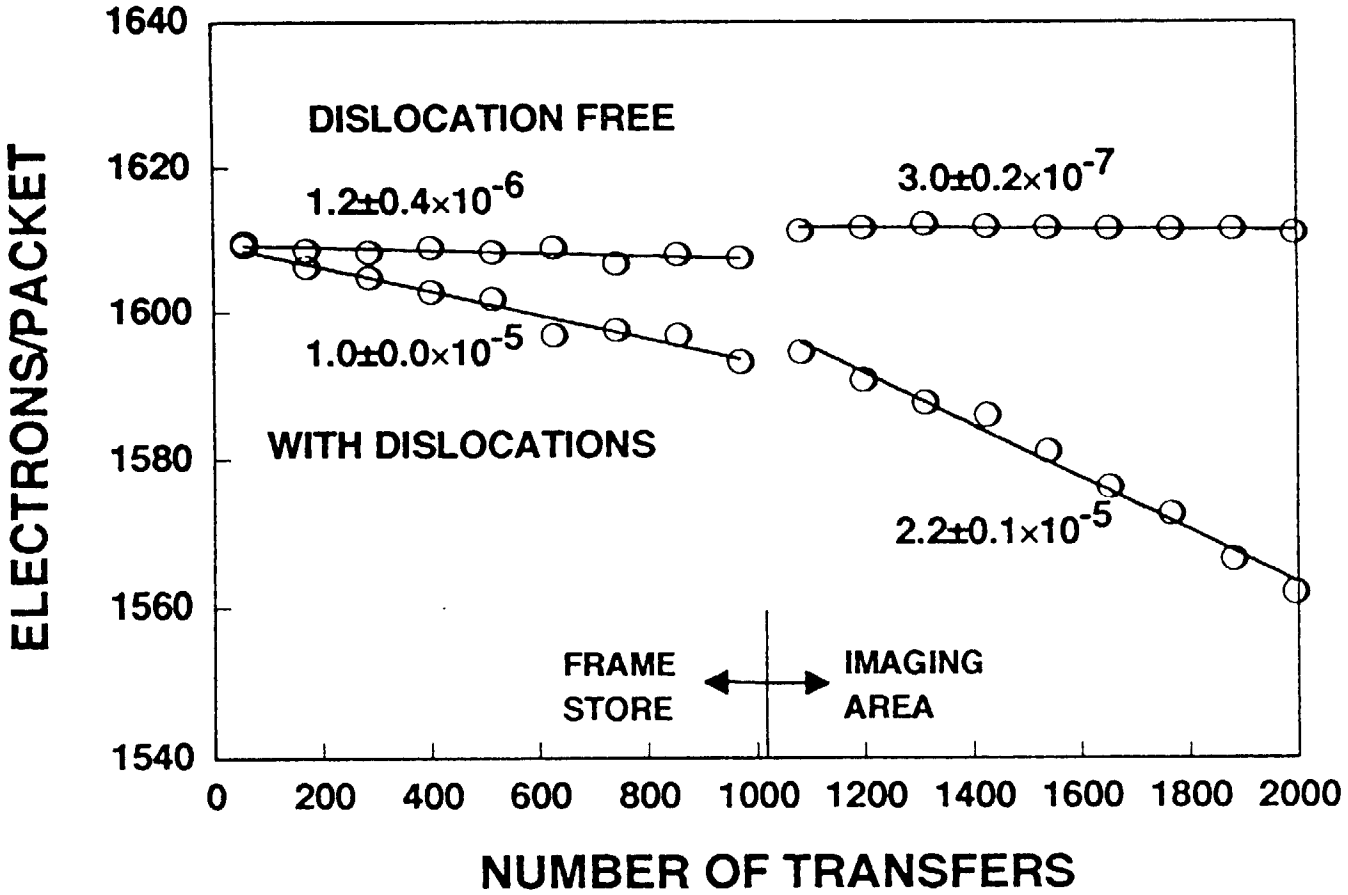
CCD WITH DISLOCATIONS



DISLOCATION FREE CCD

The changes in dark current level are apparent in this figure, where, on the left, the dark current histogram for the imaging array of a device containing dislocations is displayed. A dislocation free device is shown on the right hand side of the figure; this histogram is much narrower than the dislocated device and the distribution is not skewed toward higher dark current levels.

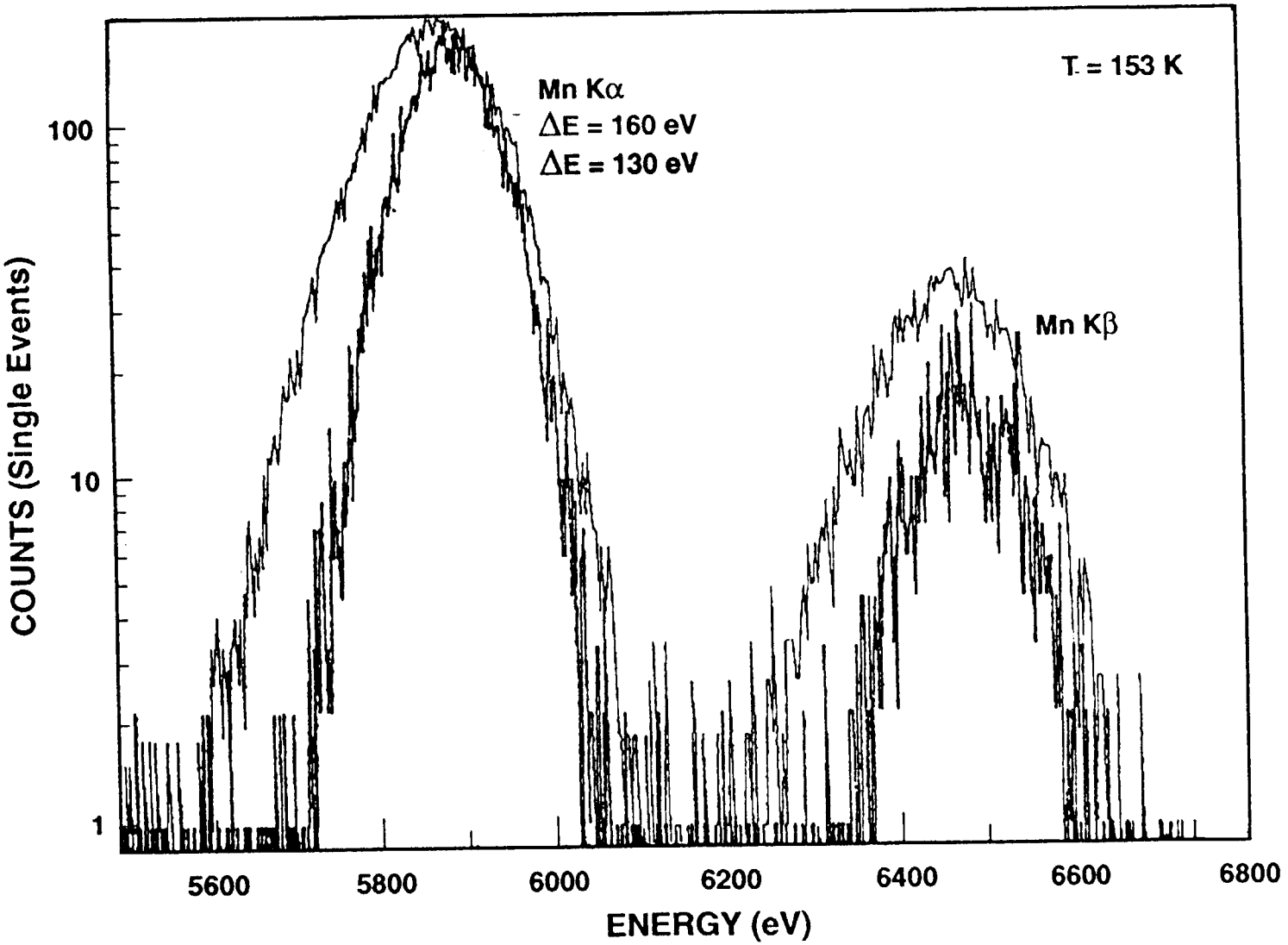
CHARGE-TRANSFER EFFICIENCY (Mn Kα X RAYS)



The CTI of dislocated and dislocation free devices are shown in this viewgraph, where it is apparent that the CTI of the dislocated device is quite poor compared to the device processed more conservatively. The CTI of dislocation free devices are consistently 3×10^{-6} or lower, from wafer to wafer and processing lot to processing lot.

ENERGY RESOLUTION: WITH DISLOCATIONS

DISLOCATION FREE



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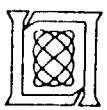
These two figures show a comparison of histograms for devices with and without glissile dislocations. Both devices were illuminated with x rays from Fe^{55}, and the energy resolution for the Mn Kα line is 160 eV with and 130 eV without slip. The difference is due to the improved CTI in the device without slip.

SUMMARY

- DISLOCATIONS LIMITING PERFORMANCE OF HIGH RESISTIVITY IMAGERS CHARACTERIZED
- SOURCES OF STRESS IDENTIFIED AND DISLOCATIONS ELIMINATED
- CTI OF 10^{-6} AND READ NOISE AS LOW AS 1.3 e^- DEMONSTRATED



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