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Modeling and Dynamic Analysis of Paralleled dc/dc Converters With Master-Slave Current Sharing Control

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Modeling and Dynamic Analysis of Paralleled dc/dc Converters with Master-Slave Current Sharing Control

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Abstract: A simple, application-oriented, transfer function model of paralleled converters employing Master-Slave Current-sharing (MSC) control is developed. Dynamically, the Master converter retains its original design characteristics; all the Slave converters are forced to depart significantly from their original design characteristics into current-controlled current sources. Five distinct loop gains to assess system stability and performance are identified and their physical significance is described. A design methodology for the current share compensator is presented. The effect of this current sharing scheme on "system output impedance" is analyzed.

I. Introduction

Paralleled dc/dc converters require an explicit current sharing mechanism to ensure proper operation. The advantages of a parallel converter architecture in providing fault-tolerance, high-current outputs at low voltages and modularity are realized only with the use of current sharing controls. Current sharing mechanisms fall into three categories: a) Programming of output impedances to achieve load current sharing. The droop method [1] belongs to this category and is a low cost method. b) Peak current-mode control schemes; where pulse-by-pulse current sharing is achieved by the use of a fast acting current loop [2]. c) Voltage loop error-signal modification; Master-Slave [3], Current-balance [4] and Central-limit control [5] belong to this category. These schemes achieve current sharing by injecting a signal proportional to the desired converter output current, into the voltage loop. The increased voltage loop error signal forces the duty ratio and consequently the output current of the converter to increase. In this paper the autonomous MSC current sharing scheme [3,6] is modeled and analyzed. In Section 2 the MSC control method is briefly reviewed. The small-signal model of two paralleled buck-derived converters with individual voltage loops and MSC current sharing circuits is developed using the PWM switch model [7] in Section 3. In Section 4 the five loop gains that determine stability and performance of the paralleled converter are examined. A current share compensator design that takes into account the stability of the current sharing loop, and which minimizes interactions between paralleled converters is presented. The dynamic characteristics of the loops is analyzed and physical significance of these loop gains is presented. The output impedance of the parallel-converter system is derived and examined.

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II. Paralleled Converters with MSC

The MSC scheme as applied to two identical modules, with individual voltage loops feeding a common load R_L is shown in Fig. 1.

In the absence of current-share/control circuitry any small imbalance in parameters associated with the voltage loop gain of individual converters will cause large differences in converter output current. The two converters would interact, as each converter would try to regulate the bus voltage causing oscillations in the bus voltage and eventually the duty-ratio of the converter with the lower loop gain would saturate and it would drop out.

MSC circuitry is hierarchically embedded above the voltage loop compensator circuitry. It forces the paralleled converters to share current, almost equally, by adjusting the *effective* voltage reference signals to the voltage loop. By *effective* is meant the sum of the voltage reference signal derived from a precision voltage

source, and the signal from the current share circuitry. Among the paralleled converters, the converter with the lowest voltage loop gain automatically becomes the master in the absence of startup sequencing; then all the other converters automatically become slaves. The *current share bus* is forced through the buffer circuitry to a voltage proportional to the output current of the Master converter. While the effective voltage reference signal of the master converter is unaffected by the current-share circuitry, the effective voltage reference signals of the slave converters are adjusted so as to increase their output currents to a magnitude almost equaling the master's output current.

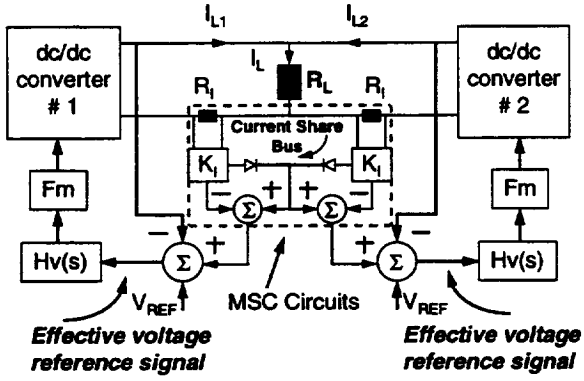

Fig. 1: Paralleled dc/dc converters with individual voltage loops and Master-Slave current sharing circuitry.

Paralleling of converters and addition of current share circuitry introduces new dynamics in the paralleled system. The current share compensator design based on the current-response loop gain is described. The various loop gains that need to be analyzed to assess system stability and performance is presented next.

III. Modeling of Paralleled Converters with MSC control

The derivation of the complete small-signal model of the paralleled converters with MSC control is composed of the following two steps: 1) Derivation of the small-signal transfer functions of the power stage, 2) Derivation of the small-signal models of the voltage loop and the MSC control circuitry.

3.1) Small-signal modeling of the power stage

The power stage models of two buck converter modules in parallel is shown in Fig. 2. The active and passive switches in each converter can be replaced by the PWM switch equivalent circuit large-signal averaged model [7,8]. The large-signal model is a very convenient tool for studying the long-term low-frequency dynamics as in time-domain simulations. The small-signal model is obtained by perturbing and linearizing the variables and is shown in Fig. 3.

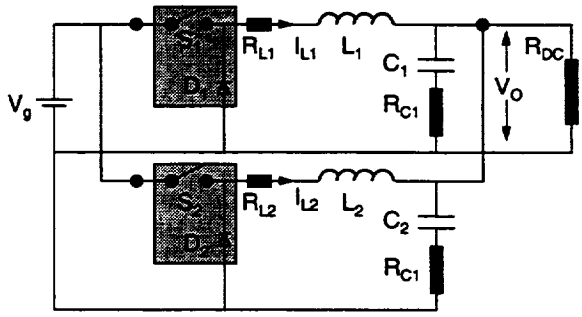

Fig. 2: Paralleled buck converter power stages

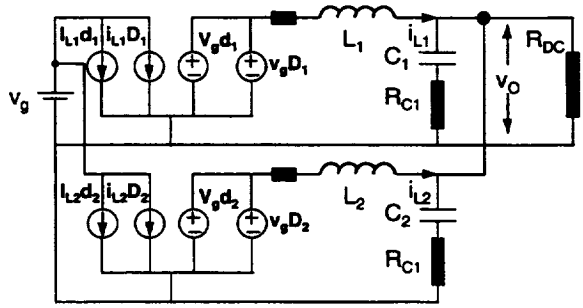

Fig. 3: Paralleled buck converter small-signal equivalent circuit model.

Using this model any of the 6 transfer functions between the output variables (output voltage and inductor current) and the input variables (input voltage, load current, duty ratio) as well as the *cross-coupling transfer function* between change in inductor current in one converter due to change in duty ratio of another converter can be computed. The block-diagram representation of the power stage small-signal model of one converter is shown in Fig. 4. This is very similar to the small-signal model of a single converter [9] except for the additional cross-coupling term F_6 (i_{bx}/d_y, $x \neq y$). By application of superposition and circuit theory to the small-circuit equivalent circuit model of Fig. 3, transfer function F_1~F_6 of Fig. 4 can be computed. The same transfer functions can also be derived using a matrix formulation [10]. The expressions derived using the PWM switch model are the same from matrix expressions providing a method of verification.

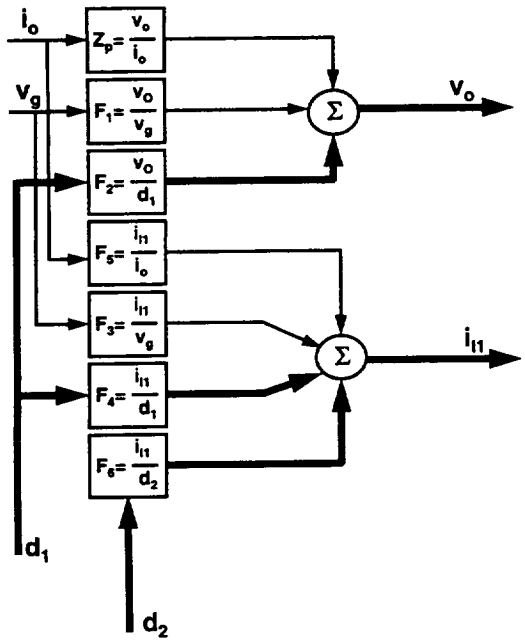

Fig. 4: Complete-small signal model of one converter among the paralleled converters.

The power stage transfer functions for loop gain analysis are:

$$\frac{v_O}{d} = \frac{V_g}{L} \frac{(R_c s + 1/C)}{(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{2}{LC})} \quad (1)$$

$$\frac{i_L}{d} = \frac{V_g}{L} \frac{(s^2 + s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right] + \frac{1}{LC})}{(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{2}{LC})(s + \frac{R_l}{L})} \quad (2)$$

$$\frac{i_{LX}}{d_y} = -\frac{V_g}{L} \frac{(s\left[\frac{R_C}{L}\right] + \frac{1}{LC})}{(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{2}{LC})(s + \frac{R_l}{L})} \quad (3)$$

where L and C are the power stage inductance and capacitance, R_l and R_C are the respective parasitics, R_L is the load resistance, $Re' = R_l + 2.R_c$, $R_e'' = R_l + R_c$.

3.1) Small-signal modeling of the feedback control

The feedback control circuits are the a) the output voltage control circuit and b) the MSC control circuitry.

The output voltage feedback loop is modeled using well-established small-signal methods. The Pulse-Width Modulator is modeled as a constant gain block with gain determined by reciprocal of ramp voltage height; the voltage loop compensation circuitry is modeled by the transfer function determined by the passive components around the op-amp.

The MSC control circuit model is based on the IC implementation in [3]. The current share bus voltage is determined by a voltage that is given by $I_{converter}.R_s.G_c$,, where $I_{converter}$ is the output current of one converter, R_s is the current sense resistor gain, G_c is the gain of the current-amplifier. This is denoted as $A_a(s)$ in the Fig. 5. A signal proportional to the difference between the converter under consideration, and the current share bus signal is summed with the voltage reference signal to produce the *effective* voltage reference signal. The dynamics of the current share loop are determined in part by the current share compensator. This compensator is denoted by the transfer function block $A_b(s)$ in Fig. 5. The design of this compensator is detailed in the next section.

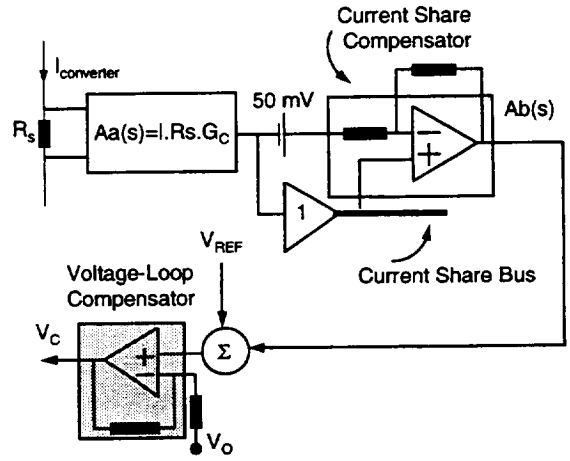

Fig. 5: Model of feedback circuitry for paralleled converters.

IV. Dynamic Analysis of Paralleled Converters with MSC control

To analyze the stability of the parallel system, and for current-share compensator design, the loop gains are the quantities of interest. The feedback circuitry present are the output voltage feedback loop and the current (inductor current) share loop. These two loops control the duty ratio, which in turn controls output voltage and inductor current. Thus in order to derive analytical expressions for loop gains the power stage transfer functions of interest are the

output voltage to duty ratio (v_O/d) transfer function and the inductor current to duty ratio (i_L/d) transfer functions and the cross-coupling transfer function (i_{LX}/d_Y). The block diagram for loop gain analysis and compensator design, extracted from the complete small signal model is shown in Fig. 6. Without loss of generality, module #1 is designated as Master and module #2 is the Slave. The super-scripts refer to the module number.

The dynamics of current sharing in MSC are determined by the *current-share loop gain* defined by:

$$T_{CS}=A_a(s).A_b(s).\ Hv(s)^{(2)}\ Fm^{(2)}.F_4{}^{(2)} \qquad (4)$$

Physically this loop determines the current-share dynamics. The voltage loop compensator is designed prior to the design of the current share compensator. It is usually a 3-pole, 2-zero compensator with a pole at the origin, so as optimize the phase margin, dynamic response and provide zero steady-state error [11].

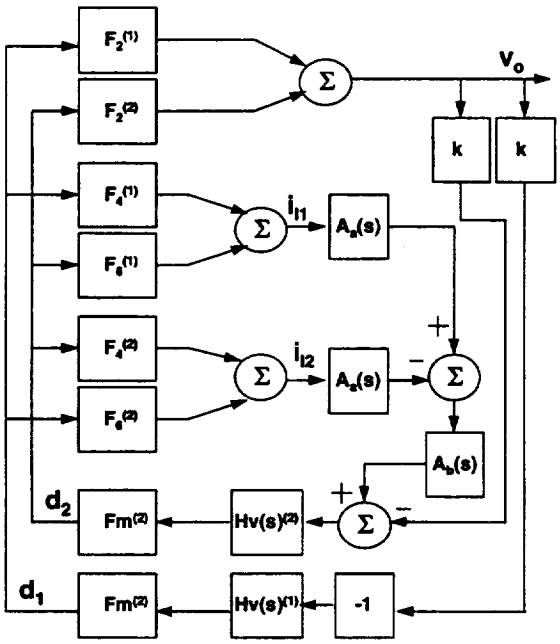

Fig. 6: Small-signal model of paralleled converters for analysis of loop gains and design of current share compensator.

In eqn. (4) the only transfer function with the freedom of being designed, to optimize the current share dynamics is the current-share compensator transfer function $A_b(s)$. The asymptotic Bode magnitude plot of the all terms excluding $A_b(s)$ {eqn. (4)} is shown in Fig. 7. Based on this transfer function the current share compensator is designed. The current share compensator is designed based on the following requirements: limited bandwidth of the path from Master to Slave module, sufficiently high low-frequency gain, sufficient phase-margin (≅ 60°), sufficient attenuation of switching frequency ripple. Based on these requirements a compensator of the form $K_c/(s/w_p + 1)$ is able to satisfy these requirements; w_p is based on a tradeoff between switching frequency ripple current attenuation and dynamic response, and k_c is adjusted for suitable cross-over frequency.

Shown in Fig. 8 are the Bode plots of the current-share compensator and the current-share loop gain for two 1 kW buck converter modules with a switching frequency of 160 kHz. The current share compensator should have a constant low-frequency gain (k_c) and a single-pole (w_p) when used with a voltage loop compensator which has an integrator characteristic. The implementation of this compensator in the existing architecture is rather simple. Since the operational amplifier for use in the current share compensator is of a transconductance type, use of a resistor and capacitor at the output in parallel will suffice. Care should be taken not to use too small a resistor value; the value chosen should not degrade the output voltage swing of the transconductance differential amplifier.

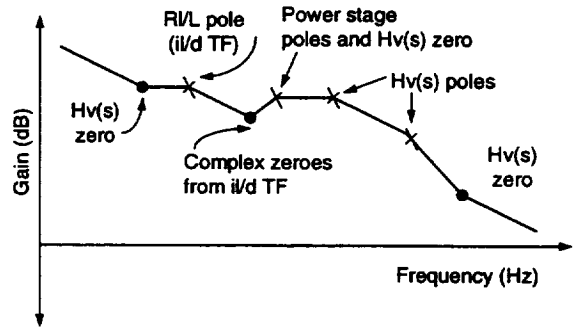

Fig. 7: Asymptotic gain plot of path gain for design of current share compensator

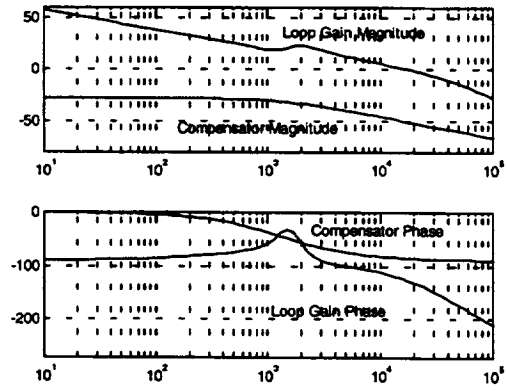

Fig. 8: Bode plots of Current-share loop gain and compensator (x-axis: Frequency (Hz))

Presence of the interaction term i_{lx}/d_y causes a change on the duty-ratio of one converter to affect the inductor current of another converter. While the Master converter current signal is used to regulate the output current of the slave converter, the master current is affected by response of the slave converter.

The change in Master reference signal is mathematically determined by the properties of the cross-coupling loop gain T_{cc}:

$$T_{cc}= A_a(s).A_b(s).\ Hv(s)^{(2)}\ Fm^{(2)}.F_6{}^{(1)}. \qquad (5)$$

Acceptable dynamics of this "cross-coupling current-share loop" is an important step in accepting the current-share compensator design. The loop gain T_{cc} is shown in Fig. 9. The phase-margin is measured by comparing the phase lag of this loop with the -360 deg. (Not -180. This is because of the absence of an explicit external negative sign in the loop). The phase margin is 107 degrees; thus this current share compensator design is valid.

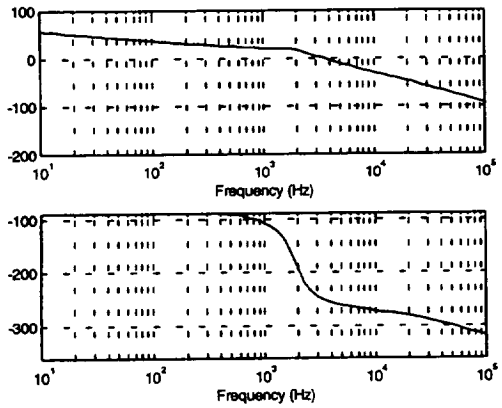

Fig. 9: Bode plots of cross-coupling current-share loop gain

The voltage loop gain of the slave converter is measured by opening the outer voltage loop of the Master converter and measuring the output voltage response to an injection into slave converter's voltage loop. The purpose of opening the loop of the Master converter is to analyze the response dynamics of the slave converter is given by:

$$T_{SL}=T_V/(1+T_{CS}-T_{CC}) \qquad (6)$$

where T_V is the voltage loop gain of an individual module, T_{CS} is the current-share loop gain and T_{CC} is the cross-coupling gain. From the above expression it can be seen that at low frequencies T_V is divided by the nested loops T_{CS} and T_{CC}. The negative sign in denominator of eqn (6) does not provide positive feedback even though a negative sign is present. This is because of the -180 deg. phase delay provided by the i_{lx}/d_y transfer function in T_{CC}.

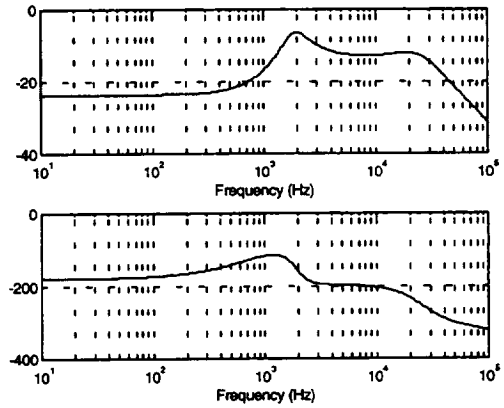

Fig. 10: Bode plots of slave converter voltage loop gain

The dramatic change in the voltage loop gain characteristics is because of the MSC strategy. The purpose and effect of MSC is to ensure that two non-identical voltage sources do not contend with each other for output voltage control. The MSC control strategy thus changes the slave converter(s) from a voltage source to a current-controlled (by Master) current source. The loop gain is shown in Fig. 10. The voltage loop gain is much less than 0 dB throughout the frequency range. Thus the slave converter does not directly respond to load disturbances but only after the Master reacts and issues a current regulation command. This is confirmed by presence of a significant current loop gain of the slave converter. In certain current share compensator designs the voltage loop gain of the slave converter may be above 0 dB at intermediate frequencies. Also, the gain of slave converter may equal the voltage loop gain of the Master converter in this frequency range. This is an undesirable situation as in this case, both the Master and Slave converters would contend and fight among each other to regulate the output voltage.

The voltage loop gain of the Master module is shown in Fig. 11 alongwith the voltage loop gain of an individual module prior to paralleling. The expression of voltage loop gain, based on observation of the block diagram [Fig. 4] is:

$$T_{ML} = T_V + 2.F_2.(T_{CS} - T_{CC}) \qquad (7)$$

where T_{ML} is the Master module voltage loop gain, T_V is the voltage loop gain of an individual module, F_2 is the duty-ratio to output voltage transfer function, T_{CS} is the current-share loop gain, T_{CC} is the cross-coupling current loop gain. An important observation

from Fig. 11 is the increase in crossover frequency and a decrease in phase margin of the Master module.

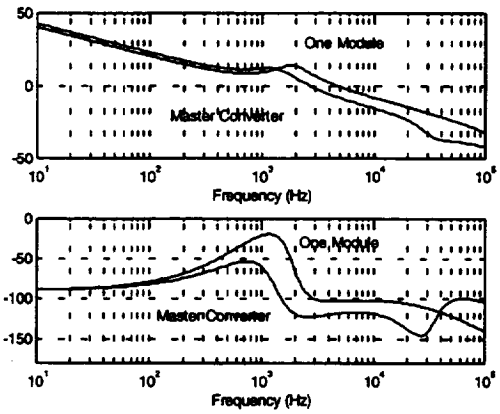

Fig. 11: Bode plots of Master converter voltage loop gain and an individual module

The system loop gain (Master and Slave modules in parallel) is shown in Fig. 12 and is given by:

$$T_{OUTER} = T_{ML} + T_{SL} \qquad (8)$$

The salient points of this loop gain are a) system voltage loop gain crossover frequency is lower than that of an individual module, b) the phase characteristic of the loop gain is greatly modified in the vicinity of gain crossover frequency.

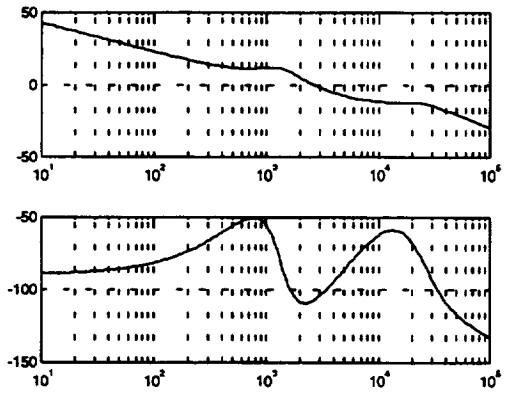

Fig. 12: Bode plots of system (Master and Slave) outer loop gain

The output impedances of a single module with voltage loop, slave module, master module and two paralleled modules with individual voltage loops and MSC control is shown in Fig. 13.

The output impedance of the Master Module is one half the output impedance of the single module (reduction by 6 dB). This is an extremely interesting point. The output impedance of the slave module is quite high. This is the current source behavior of the slave module.

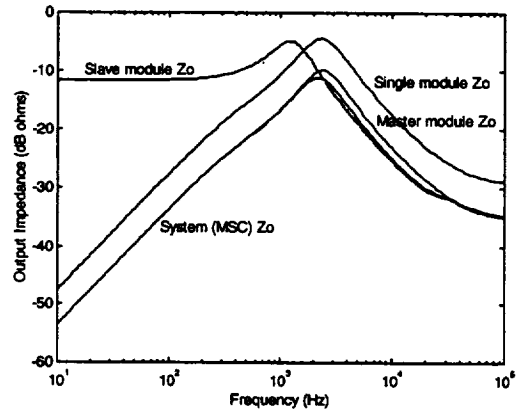

Fig. 13: Output Impedance magnitudes of single module, master module, slave module, master-slave control paralleled modules.

The reduction in system output impedance is due to increased overall outer loop gain. The system output impedance is the parallel combination of the Master and Slave output impedances. From Fig. 13 it can be seen that the system output impedances is closer to the value of the smaller of the two (Master and Slave) output impedances.

V. Conclusions

A simple, application oriented, small-signal model for paralleled dc/dc converters with MSC is developed. A design methodology of the current share compensator based on the current share loop gain has been presented. Proper design of this compensator is necessary to minimize interactions between paralleled converters and to ensure system stability. Five loop gains that need to be analyzed to assess system stability and performance have been identified and analytical expressions developed. The effect of this current sharing method on the output impedance has been analyzed.

Appendix A

Buck Converter Parameters

Power Stage: L=113μH, 0.6 Ω, C: 126μF, 33mΩ, Vg=224V, Vo=140V, Fm=0.228, Load=1000 W, Current Share Compensator: 40e-3/(s/8380+1), Voltage Loop Compensator: (s+8.5e3)(s+4.43e11)/(s(s+5.29e5)(s+2.43e5)), Vref=2.42 V. Two identical modules were paralleled.

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