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PORTABLE COMPUTER TECHNOLOGY (PCT) RESEARCH AND DEVELOPMENT PROGRAM PHASE II

FINAL REPORT

Prepared for
National Aeronautics and Space Administration
Ames Research Center
Moffett Field, California 94035

September 25, 1995

In Compliance with
Prime Contract No. NAS2-13902

Science Applications International Corporation
4224 Campus Point Court
San Diego, California 92121-1513

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APPENDICES

1.0 INTRODUCTION

The Portable Computing Technology (PCT) project was structured to evaluate and test advanced computer processing technology, create testbeds, integrate advanced wireless communications, and demonstrate advanced mobile client server applications.

Phase I, which was completed June 1993, concentrated on research in display and processor technologies, modular packaging techniques, software testing, and customization of power and interface technology to meet NASA performance and safety requirements for the Shuttle. As a result of the research five testbed systems were completed based upon an Intel 486 microprocessor, with a modular design featuring a display module, a detachable keyboard and a removable hard disk drive. These testbeds supported multiple mounting configurations for additional flexibility in a micro-gravity environment.

Phase II, the subject of this project report, focused on:

1) Design and development of two Advanced Portable Workstation II (APW II) units. These units incorporate advanced technology features such as a low power Pentium processor, a high resolution color display, National Television Standards Committee (NTSC) video handling capabilities, a Personal Computer Memory Card International Association (PCMCIA) interface, and Small Computer System Interface (SCSI) and ethernet interfaces.

2) Use these units to integrate and demonstrate advanced wireless network and portable video capabilities.

3) Qualification of the APW II systems for use in specific experiments aboard the Mir Space Station.

A major objective of the PCT Phase II program was to help guide future choices in computing platforms and techniques for meeting National Aeronautics and Space Administration (NASA) mission objectives. The focus being on the development of optimal configurations of computing hardware, software applications, and network technologies for use on NASA missions.

1.1 Final Report Format

The final report has been organized in sections, with each section representing an APW II Module, mechanical specifications and test results. Below is a list of the major sections that are covered in the report:

- Wireless Server Module (WSM)
- Display Module (DM)
- Battery Module (BM)
- Keyboard Module (KM)
- APW II Mechanical Configuration
- Wireless Computing Device
- Demonstrations
- Test Results
- Safety Data Information

Each APW II module section describes the main features of that particular APW II module and its components. Each section has an associated appendix that includes the data sheets of the components used in the APW II design as well as reference information on additional complimentary products. In addition, the appendices also contain test results conducted on the APW II during the design verification phase of the program.

1.2 Preface and Acknowledgments

The PCT Phase II project was supported by Contract Number NAS2-13902 from the NASA Ames Research Center. The SAIC project team consisted of the following individuals: Michael Castillo, Kenyon McGuire, and Alan Sorgi. Product and corporate names may be trademarks or registered trademarks of other companies, and are used only for explanation and to the owners' benefit, without intent to infringe. A list of abbreviations and acronyms is provided in Appendix 12.

2.0 WIRELESS SERVER MODULE

The APW II Wireless Server Module (WSM), Part Number 65460-1, consists of a single assembly which includes the Central Processing Unit (CPU) (printed circuit card and components) and the power supply (printed circuit card and components). The WSM is the main module of the APW II system. It was designed to include the most current computer technology such as the Pentium Processor, a Peripheral Component Interconnect (PCI) Local Bus, Error Detection and Correction (EDAC) Single Inline Memory Modules (SIMM), NTSC video input and a Dual PCMCIA interface. Figure 1 depicts the overall APW II system configuration.

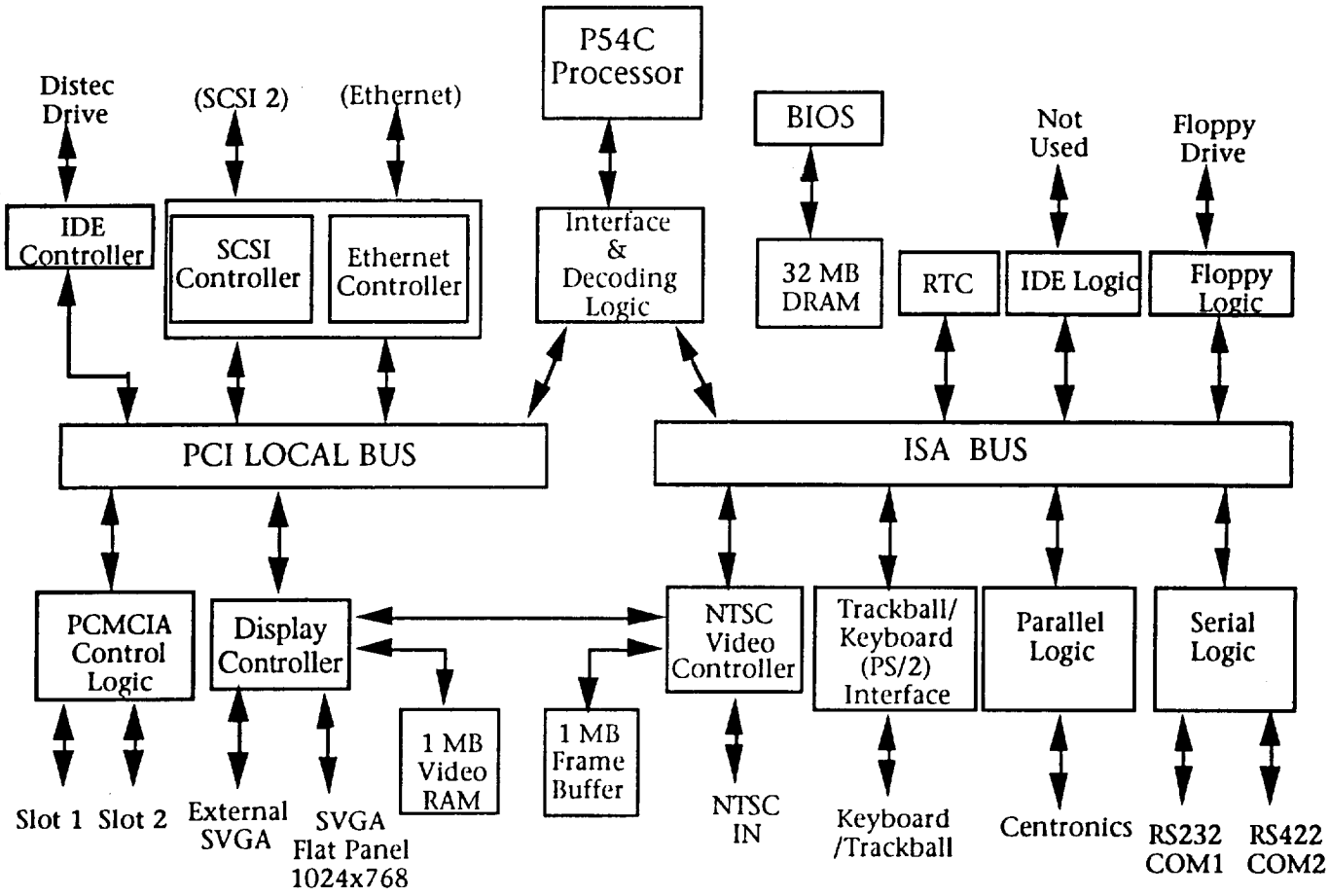


Figure 1 Overall System Block Diagram

2.1 WSM Specification

At the start of the project the initial baseline requirements for the APW II focused on six major elements. These elements were considered important to the success of the project so they were evaluated closely. SAIC assessed both the technical and financial merit of incorporating these elements into the APW II with the focus of the design on the WSM, since it was the module that would have the most complex elements (the CPU and the power supply). The key areas reviewed were:

- a low power 486 processor
- 16 Mega Bytes (MB) Dynamic Random Access Memory (DRAM)
- a PCMCIA Ethernet card (Type II or Type III)
- PCMCIA slot
- One RS-232 interface and one RS-422 interface
- a NTSC Video interface

Once SAIC completed the assessment the results were presented to NASA at the Requirements Review. As a result of the review, both SAIC and NASA Ames decided that the above features could be incorporated into the APW II with little risk and within the projects budget and schedule. Besides the listed features above, several additional features were evaluated for possible incorporation into the APW II. The features included:

- a low power Intel Pentium processor at 90 MHz
- 32 MB DRAM expandable to 64 MB with Error Detection and Correction (EDAC)
- a 260 MB removable hard disk
- a 3.5", 1.44 MB floppy drive of low-volume design
- A SCSI interface supporting SCSI-II operation
- a built-in Ethernet interface
- an Enhanced Parallel Port
- a Super Video Graphics Accelerator (SVGA) analog RGB monitor output

SAIC evaluated the additional features and concluded that these features could be included.

2.2 WSM CORE SYSTEM

Architecturally, the WSM is comprised of a core system and other major components. Figure 2 depicts the Core System Block Diagram.

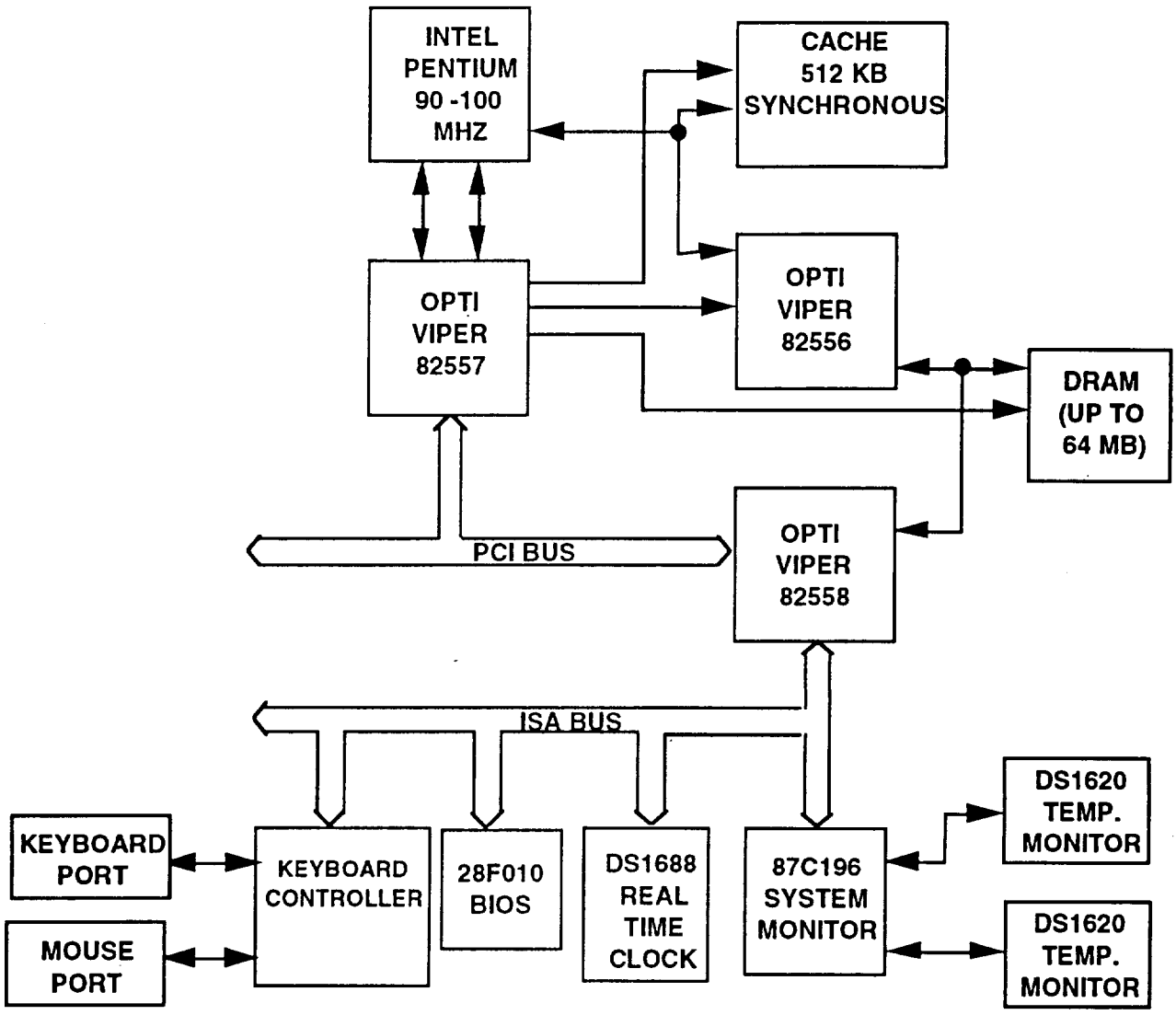


Figure 2 Core System Block Diagram

The core system consists of a low power Intel Pentium processor at 90 MHz, an OPTi Viper Chipset, 32 MB of DRAM expandable to 64 MB with error detection and correction (EDAC), 512 KB of Cache Memory, a PCI Bus, and an International System Architecture (ISA) Bus.

Other major system components include a SCSI-II and Ethernet Interface, a NTSC Video Interface, a Video Graphics Accelerator (VGA) and Flat Panel Interface, /AT Interfaces

(Serial, Parallel, Keyboard/Mouse, Integrated Drive Electronics (IDE), Floppy), a PCMCIA Interface (Dual Slot), a Power Supply, and a temperature monitoring feature.

2.2.1 Pentium Processor

2.2.1.1 486 versus Pentium

During the preliminary design phase, it was decided that a higher performance machine was more important than a lower power implementation of a 486 processor. Therefore, it was decided to go forward with a design using a Pentium. Another consideration for using a Pentium processor was NASA needed a system that could handle Electronic Still images and real-time video input. These functions typically require a high speed bus for processing of the data. SAIC determined that a PCI bus could support these functions, however, to take full advantage of the PCI bus a Pentium processor would be required.

The decision to implement a system using a Pentium was not without risk. The risks centered around the use of certain critical interfaces, availability of components, and system design approach as it relates to the Pentium architecture. The critical interfaces included the PCI Bus, the NTSC video, the ethernet and the SCSI II, all of which were newly released products. These interfaces were relatively new and in most cases SAIC relied on the preliminary information from the manufacturer and pre-production components to start the design process early.

2.2.1.2 Pentium Processor Features

The Intel Pentium processor (90 Mhz) delivers the highest performance possible for a Personal Computer (PC). It is compatible with the huge base of PC software and runs applications up to twice as fast as the Intel DX4 processor. Additionally, a Pentium processor delivers the extra power needed for today's PC applications. The Pentium processor is capable of running the most demanding mobile applications and has the performance to run full screen, full-motion video, real-time animation, compute intensive 3D modeling graphics applications, and mobile multimedia presentations.

Another characteristic which makes the Pentium unique, is its power management capabilities. With concern over power consumption, the Pentium has incorporated an architecture to provide a platform for high performance computing, yet manages to keep power consumption to a minimum. For instance, the Pentium has the ability to quickly disable the numeric processor when no floating point operations are occurring, and can also reduce its power consumption to 20 percent of normal during "HALT" states. Another main feature of the Pentium is the use of a 3.3 volt design, which significantly reduces power consumption over that of its predecessor. One other power saving feature of the Pentium is its ability to stop its internal clock on demand. This can also be used to reduce the Pentium's power consumption by reducing its performance in small increments until the desired level of heat production or power consumption is reached.

2.2.1.3 Pentium Benchmarks

Figures 3 and 4 show comparative benchmark results for the Pentium processor and the PCI bus, both of which were incorporated in the APW II design. The results show tremendous gain over that of a 486 DX4 and an ISA bus respectively. See Appendix 10 for additional benchmark results for the APW II.

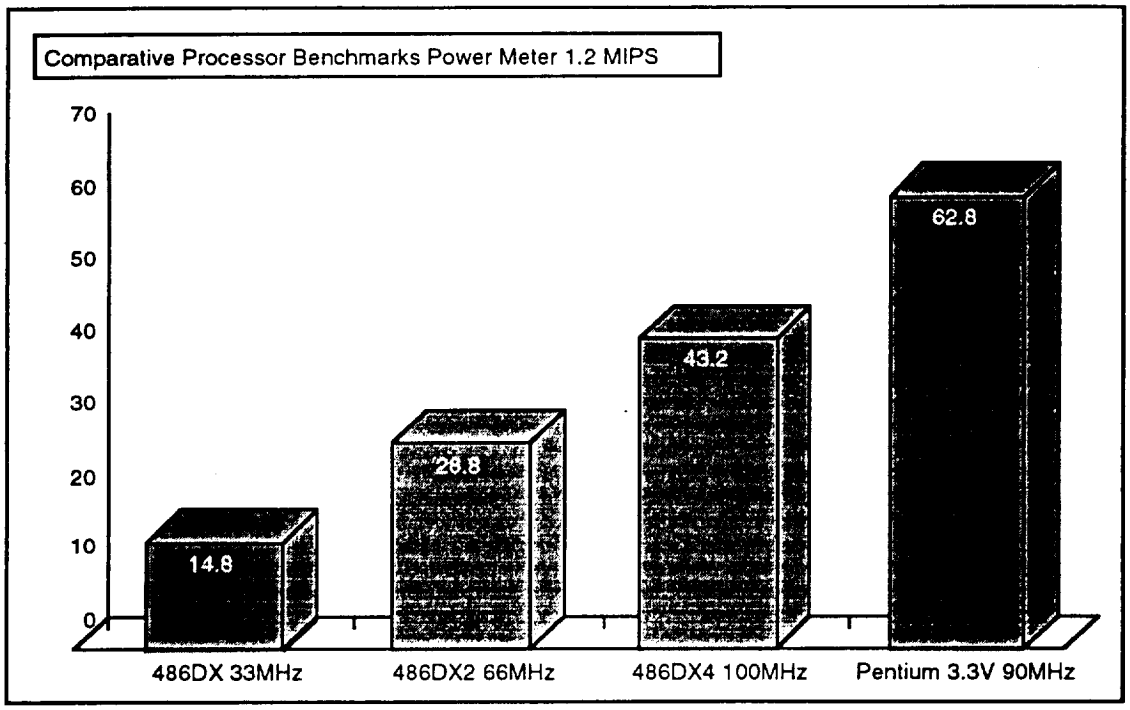


Figure 3 Power Meter Benchmark Results

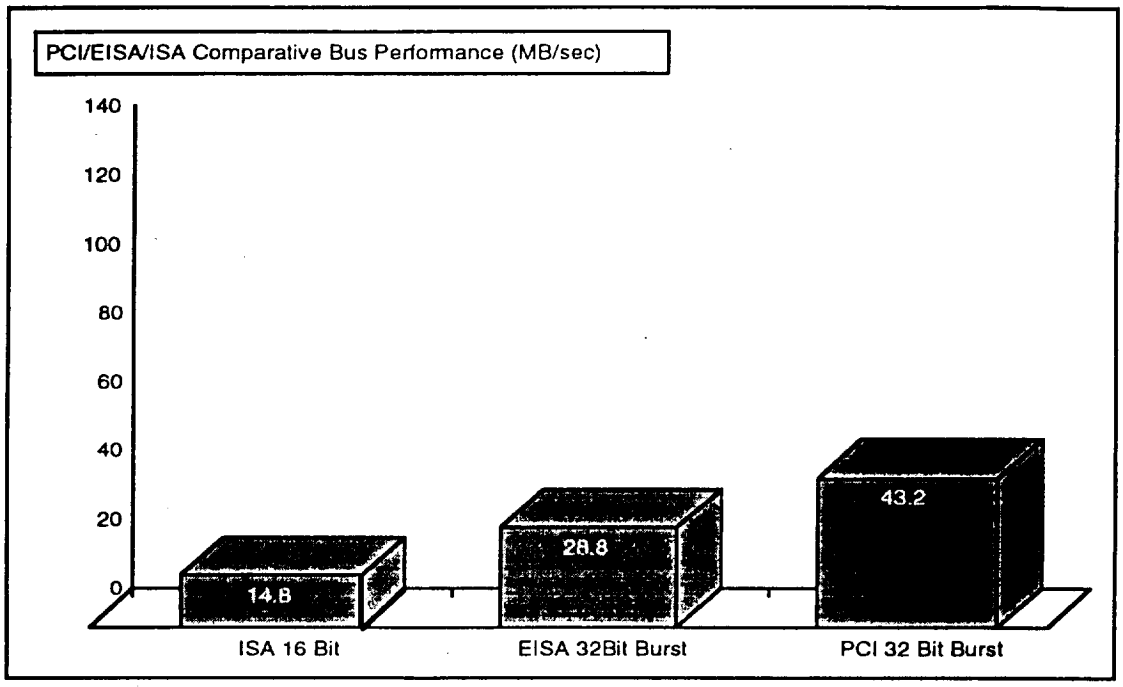


Figure 4 PCI/EISA/ISA Bus Performance Benchmark Results

2.2.2 Chipset Selection

Several processing core logic chipsets were considered for implementation into the APW II design. The choices were based primarily on availability. Other criteria centered around the chipsets ability to work with the Pentium architecture. The initial choices under consideration were VLSI Technology's "Supercore 590", ACER's "Aladdin" M1461/M1449, International Business Machine's (IBM's) latest EDAC chipset and OPTi's "Viper" Desktop Chipset. All the chipset candidates exhibited main features meeting the basic requirements for the APW II system. These included 3.3 volt support for reduced system power, an integrated PCI local bus, an ISA bus, and a memory system optimized for operation without secondary cache.

The following is a summary of each of the chipsets reviewed.

IBM Microelectronics. This chipset features the ability to run with any speed variant of the Pentium, supports low power 3.3 Volt operation, "green" features for implementing a Microsoft Advanced Power Management (APM) driver, and contains a built-in EDAC circuit. The chipset's EDAC feature can be used with standard 36 bit SIMMS. Other features included a very high integration which reduces part count, a built-in cache controller and a PCI interface. The IBM chipset was in alpha test at the time chipsets were being evaluated. Due to unavailability and the high risk of using alpha parts, these chips were not tested.

VLSI Supercore 590. The VLSI chip was evaluated and found that it did not support ECC. Non-availability of the parts for testing and evaluation after initial release of the design eliminated this choice.

ACER "Aladdin". The ACER chipset was reviewed as a candidate for implementation into the APW II, however, several things worked against using the chipset. First, the chip was developed and manufactured overseas in Taiwan. This was a concern considering the complexity of the design, and getting adequate technical support during the design process. Second, there were some existing problems with ACER's existing chipset design which raised a flag of concern on the new design.

The OPTi "Viper" Desktop Chipset was selected for use in the APW II. SAIC has had past experience using OPTi components and has developed a good working relationship with the company. Because of the schedule constraints and the complexity of the design, SAIC felt this relationship would be a benefit during the design process should there be problems later on.

In the end it was OPTi's Viper Desktop chipset that provided the best performance, compatibility, technical support, and most important, availability.

2.2.2.1 OPTi Viper Desktop Chipset Features

The OPTi Viper Desktop Chipset provides an integrated solution for the Pentium processor. It is 100% PC/AT compatible, supports the 3.3 V Pentium, supports up to three PCI masters, one VESA slave and six ISA slots. It also supports both synchronous and asynchronous SRAM and DRAM configurations up to 512 MB. The OPTi Viper is comprised of three chips: a Data Buffer Controller (82C556), a System Controller (82C557), and an Integrated Peripherals Controller (82C558).

The Data Buffer Controller performs the task of buffering the CPU to DRAM memory data path, and also performs parity check. While the System Controller provides the control functions for the host CPU interface, the level 2 cache, the DRAM bus, the VESA Local bus interface and the PCI interface. The Integrated Peripherals Controller contains the AT bus controller, which includes a Real Time Clock (RTC) interface, a 82C206, a Direct Memory Access (DMA) controller and a system power management unit. Appendix 1 contains additional information on the OPTi chipset architecture and the other components used in the APW II design.

2.2.3 Memory

Due to memory corruption failures experienced in space, as it relates to Single Event Upsets, it was decided to design the APW II to use either a core chipset that implements an embedded Error and Correction Coding algorithm within the chipset itself, or as an alternative, ECC SIMMS which would provide the same function but at a much lower cost. It was decided to use the ECC SIMMS primarily because there was no ECC Core

Chipset in production. A new ECC chipset from IBM was reviewed, however the Beta release and delivery would not meet the PCT II project schedule requirements. Using a Beta ECC chipset was determined to be a high risk to the APW II design as well.

The ECC SIMMs selected for implementation were the IBM11D4480B-70, in production by IBM. This product has been in use by IBM internally on their corporate main frame systems and by the military in some of their critical computer system applications. It has been only recently that IBM made this product available to the public. Although the size of the SIMM itself is larger than normal SIMMs, they were incorporated into the APW II design to provide a more reliable and robust memory system.

In addition to installing 32 MB of ECC DRAM, SAIC designed the APW II with 512 KB of secondary cache. Although the decision to add cache would add to the overall power consumption of the unit, cache was essential in order to take maximum advantage of the Pentium's speed. The cache operates synchronously to the Pentium processor in "synchronous burst" mode providing the utmost in system performance. The secondary cache architecture design uses "write-back" cache.

2.2.4 PCI Bus

The PCI local bus is a high performance bus that provides a processor independent data path between the CPU and high speed peripherals. PCI is a robust interconnect and is designed specifically to accommodate multiple high performance peripherals such as graphics, full motion video, SCSI, and Local Area Network's (LAN's). In addition, PCI offers low latency data access and a guaranteed minimum bandwidth by featuring programmed burst size, bus arbitration for single accesses, resource locks and support for look ahead arbitration.

In general, the overall performance of the PCI on a 486 system is about equal to the ISA bus or both read and write operations. In Pentium systems the technical capabilities of PCI will exceed the current ISA bus architecture.

On a high-performance computer running a true multitasking operating system such as OS/2, Windows NT, or Unix, PCI gains the upper hand in performance, because of its ability to work concurrently with the CPU. This allows the CPU and PCI bus to proceed along simultaneously. In addition, the PCI's bus isolation allows faster processor speeds.

For the APW II design the PCI bus was used with high performance peripherals including video, SCSI, Ethernet and PCMCIA. The ISA bus was used for lower performance peripherals such as IDE, keyboard/trackball and floppy.

2.3 SCSI/Ethernet Interface

The APW II design initially required ethernet being implemented through use of a PCMCIA Ethernet Adapter card. Advanced Micro Devices (AMD) recently developed a single SCSI/Ethernet chip which provided both functions in a single a chip, the Am79C794. Figure 5 depicts the SCSI/Ethernet Block diagram. This chip was examined and the decision made to use it to provide an on-board ethernet function, freeing up one of the PCMCIA slots for future expansion.

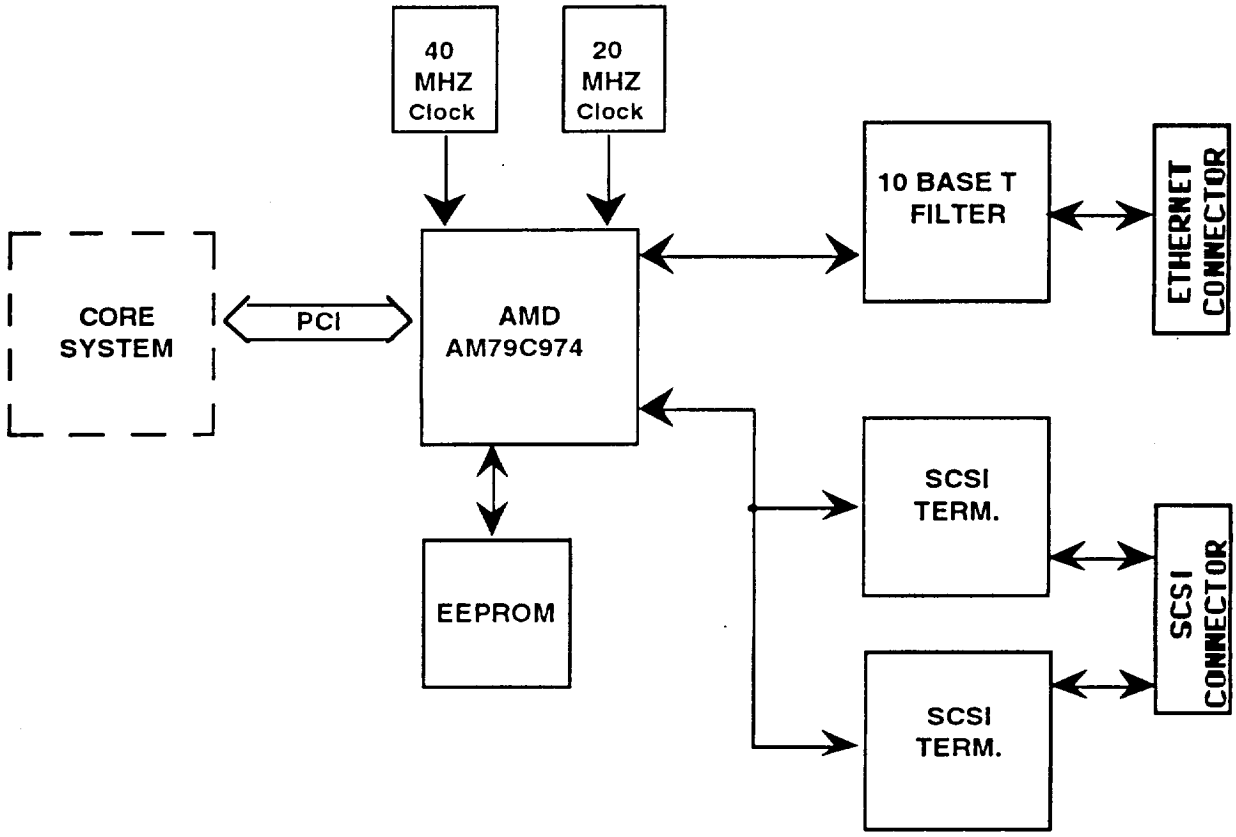


Figure 5 SCSI/Ethernet Block Diagram

The APW II SCSI/Ethernet interfaces are controlled by the AMD Am79C794 combination Ethernet and 8-bit Fast SCSI Controller with a 32-bit PCI interface. This chip is a high performance bus-mastering device that provides high data throughput in the system with low CPU and bus utilization.

The Ethernet interface supports ISO 8802-3 (IEEE/ANSI 802.3) and Ethernet standards. The SCSI interface is compliant to ANSI standards X3.131-1986 (SCSI-1) and X3.131-199X (SCSI-2).

The SCSI disk interface provides high performance fast SCSI-II transfers at up to a 10 Mbytes/sec transfer rate when using synchronous drivers. By using PCI bus mastering in conjunction with a 96 byte transfer First-In-First-Out (FIFO), this transfer rate can be maintained with a minimum of bus latency. In addition, an on-chip state machine automates many common command sequences in order to reduce "low-density" PCI traffic.

2.4 Video Interface

The APW II was designed to provide a high performance video controller with a 32-bit PCI bus interface and the ability to accept NTSC Video input. Figure 6 shows the Video subsystem and the major components that comprise the video interface subsystem. The video section is actually split, with the primary VGA controller on the PCI bus and the NTSC front end on the ISA bus. In order to speed data transfer to the display, the VGA controller is located on the PCI bus.

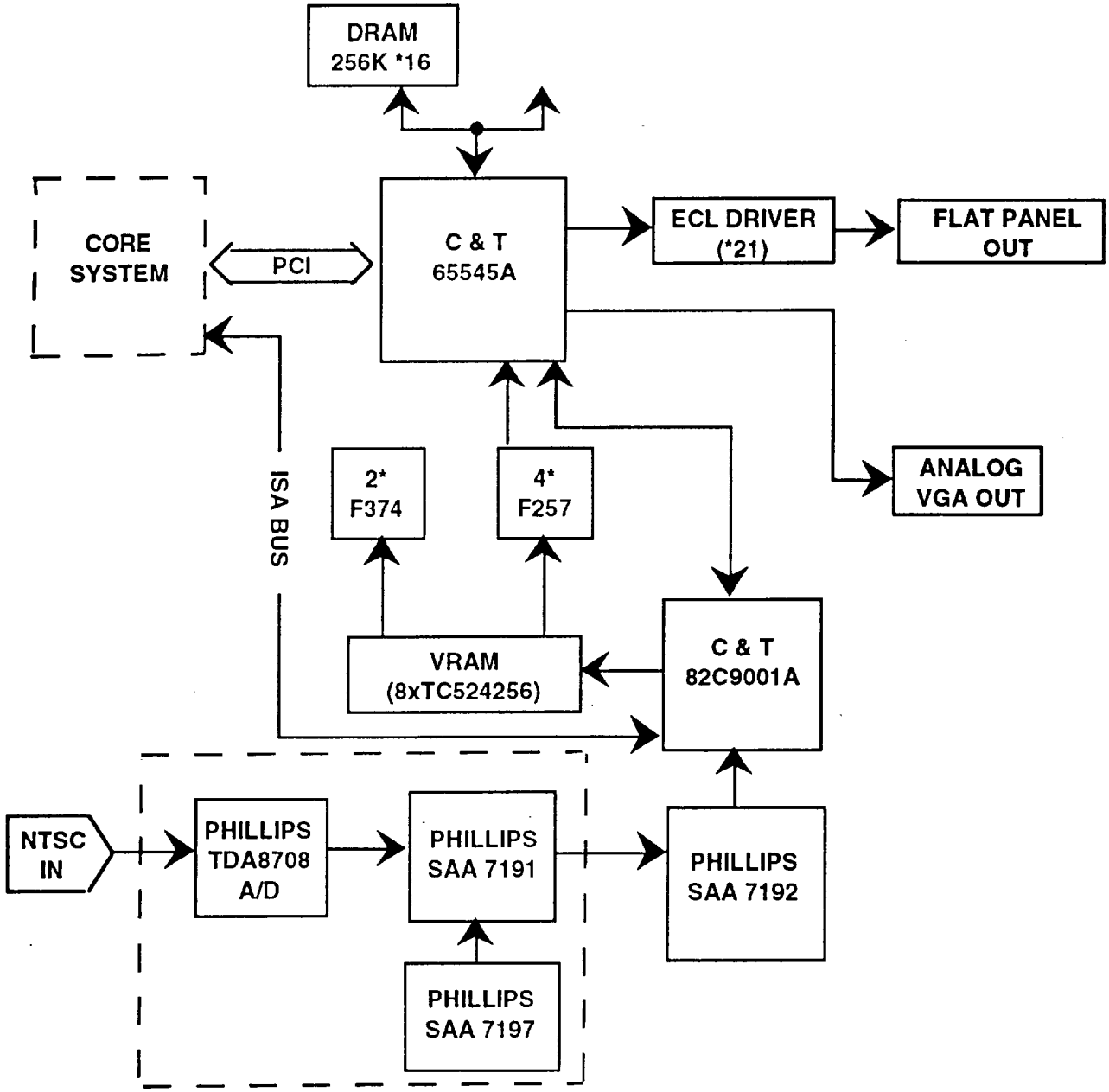


Figure 6 Video Block Diagram

One megabyte of video memory was provided in the form of two 256 K x 16 DRAM's. This allows support of all standard, Super and Extended VGA resolutions up to 1024 x 768 with 256 colors as well as 16 bit color and 24 bit color modes. Hardware based acceleration is provided by a sophisticated 32-bit graphics engine for Bit Block Transfer, color expansion, hardware line drawing, hardware cursor, and other functions used extensively by Graphical User Interfaces (GUI's). An onboard 32 bit graphics engine provides fast GUI interface operations such as BitBLT transfers and hardware line drawing. The APW II also supports a flat panel interface which has been optimized for

the Sharp LQ10DX01 Display. ECL drivers were used to source the flat panel signals allowing the signals to be transmitted over twisted pair cables of lengths up to 10 feet.

The Chips & Technology 82C9001A PC Video windowing chip is the core component of the APW II video subsystem which converts a standard full-motion video image into a format for display on a CRT or flat panel monitor. The PC Video logic controls positioning and scaling of the video image on the output display and allows the video image to be merged with computer graphics. The NTSC feed is processed using a Phillips Desktop video chipset. Windowing and frame capture of the NTSC feed is managed by the Chips 82C9001A "PC Video" chip.

Because of the high risk involved with designing an analog NTSC video input interface, a separate circuit board was designed for the analog portion of the NTSC video design. This board connects directly to the main CPU board. This design approach allows for easy redesign of the analog portion of the NTSC Video if changes are required. The thought being that a redesign of a small board versus a complete redesign of the CPU board is much more cost effective, both in time and money.

2.5 /AT Interfaces

The APW II was designed to provide standard /AT interfaces. Figure 7 shows the major components of the /AT interfaces used in the design.

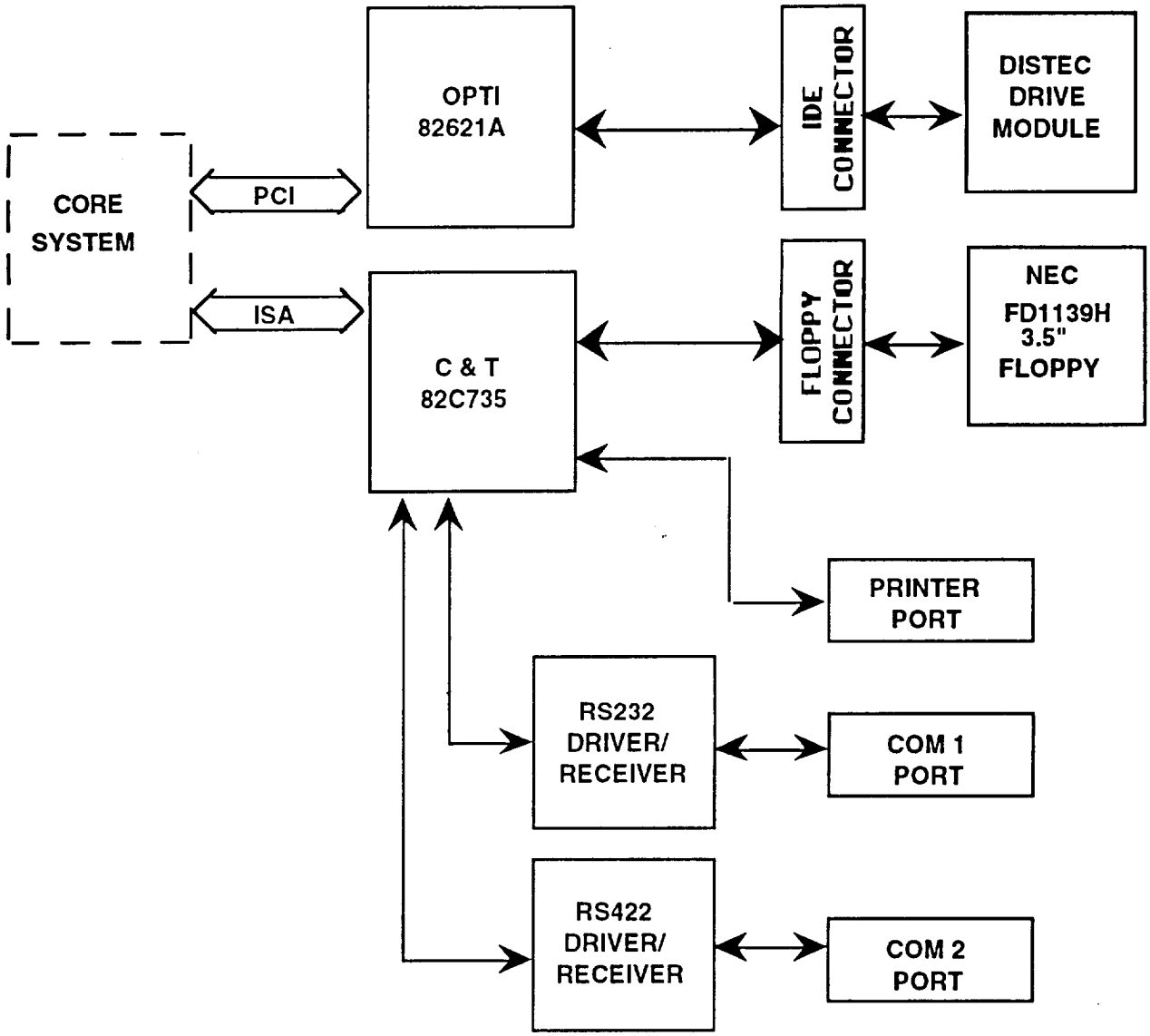


Figure 7 /AT Interface Block Diagram

The serial, parallel, IDE and floppy interfaces are provided by a single-chip I/O adapter (82C735). This adapter allows for software controlled power-down of individual sections for power conservation. In order to provide optimal compatibility with current software, the individual sections for the Input/Output (I/O) adapter are register compatible with commonly available I/O adapters.

Two high-speed IBM compatible serial ports are provided on the APW II. Serial port 1 is implemented using the RS-232 standard interface. While the second serial port is implemented using the RS-422 standard interface. Although RS-422 is recognized as a 'standard' the fact is there is no clearly defined signal pinout which can be followed. With the RS-530 fast becoming a widely accepted recommended standard, the RS-530 protocol was used to define the signals for the RS-422. In fact, many manufactures are now using the RS-530 as the signal definition for the RS-422.

The parallel interface supports both the "Enhanced Parallel Port" or "EPP" versions 1.7 and 1.9 as well as the Microsoft/Hewlett-Packard "Enhanced Capabilities Port" or "ECP" parallel port specification.

The APW II supports a 32 bit PCI local bus IDE hard disk interface. The IDE interface supports both primary and secondary drives and can be enabled or disabled.

The floppy interface supports up to a 1.44 MB floppy. The internal controller uses a digital data separator, and is software and hardware compatible with Intel's 82077AA floppy adapter.

2.6 PCMCIA Interface

The APW II was designed to support a dual socket PCMCIA (Personal Computer Memory Card International Association) interface. The interface makes use of the Cirrus Logic CL-PD6729 PCMCIA Host Adapter on the PCI bus and is compatible with PCMCIA standards 1.0, 2.0, 2.01 and 2.1 as well as JEIDA 4.1.

The PCMCIA interface uses a dual slot 136-pin connector that accepts Type I, II and Type III cards. Mechanically the two slots were stacked to conserve space. A "side-by-side" configuration was considered, but limited external surface space on the WSM prevented this configuration from being implemented.

The two PCMCIA sockets can be of mixed voltage requirements (5 volt and 3.3 volt). In addition, access cycle timing is programmable, multiple power saving modes are also available, including suspend mode which turns off the internal clock, and low power mode which stops PCMCIA transactions and turns off most of the internal circuitry. Figure 8 depicts the PCMCIA Controller block diagram.

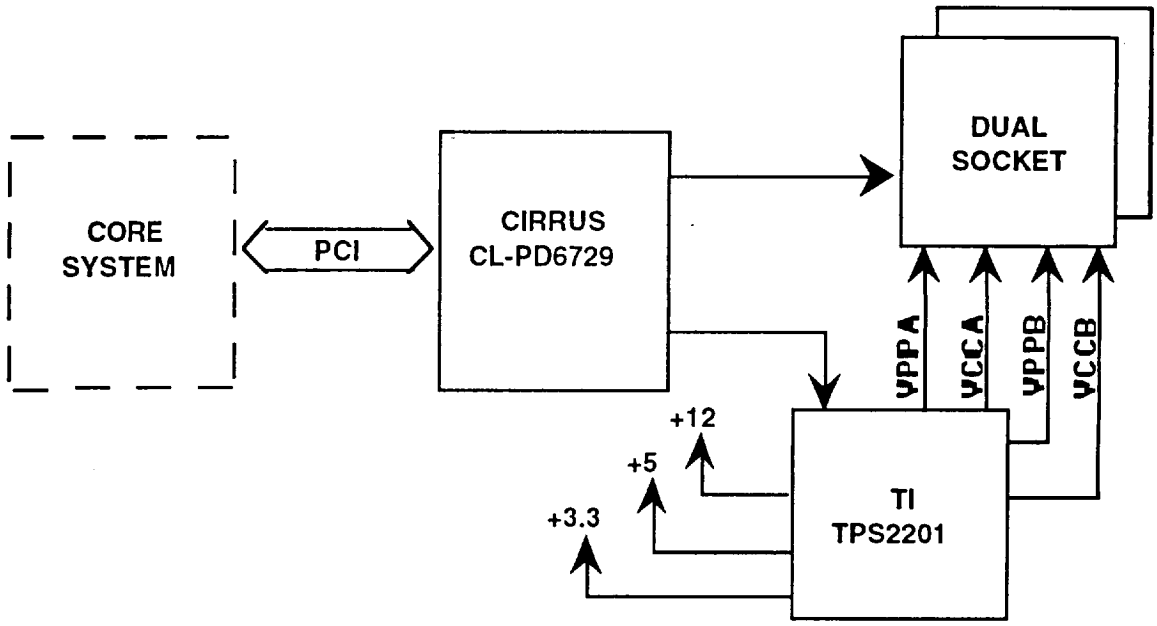


Figure 8 PCMCIA Controller Block Diagram

2.7 Power Supply

A large portion of the APW II system design was spent determining the power supply architecture. The design effort focused on getting the power supply in the space available, meeting the voltage input boundary conditions, and providing a charging circuit for the battery pack.

2.7.1 Power input

The voltage input range requirements were specified to be 24 to 32 volts. Implementation of a voltage range between 12-45 volts was evaluated, however it was determined that this entire input voltage range would be relatively difficult to accommodate with an acceptable efficiency rating. Also, the preliminary power budget analysis indicated that it would be difficult to develop a small power supply due to the large peak currents required in the battery pack. The APW II power supply was extended to accept an input voltage of 18 to 45 volts. Figure 9 shows the power supply system architecture.

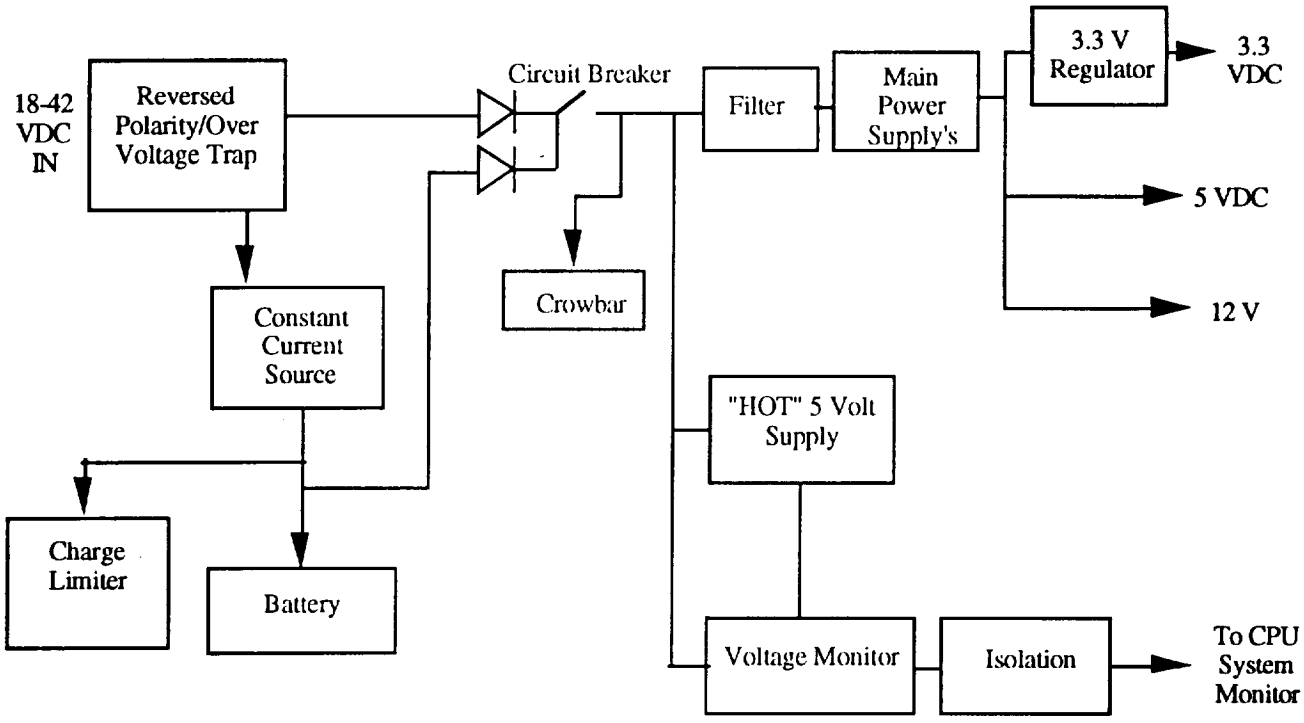


Figure 9 Power Supply Block Diagram

The power input of the power supply is protected against reverse polarity and voltages of over 45 volts by a simple crowbar circuit and self-resetting fuses. In the event that a

continuous power fault is applied, the crowbar will activate and open the fuses. Upon removal of power, the fuses reset.

2.7.1.1 Power Supply Protection Circuits

The power supply is designed with three levels of protection to prevent damage to the CPU and other electrical components from a power glitch or failure; input voltage protection, current surge protection and over voltage protection.

The first level of protection is the input fuses used at the power input of the unit. These resettable fusses will trip if there is an abnormally large current drain on either of the input lines. The fuses are rated to trip at 5.7 Amps.

The second level of protection is provided by the circuit breaker (on/off switch). The breaker (current rating is 5 Amps) will also trip if the current draw is abnormally high on either of the input lines. The fuses and the circuit breaker provide the APW II system with a dual redundant power input circuit protection against large input currents.

In addition to the two circuit protection schemes described above, the APW II power supply design also incorporates reverse polarity and over voltage protection circuits. The reverse polarity protection was designed by using a diode across the two input lines. The over voltage protection is accomplished within the American Telephone and Telegraph (AT&T) modules themselves. If a voltage spike of more than 45 volts is detected the power supply modules shutdown until the voltage is lowered below 45 volts.

2.7.2 Power Supply Evaluations

Following is a summary of several power supply products that were evaluated for possible implementation into the APW II power supply design. The selection criteria was based on finding a power supply that would; fit within the mechanical layout of the WSM, be at least 80% efficient, have an input voltage range capability of 12 to 40 volts and be reliable. Availability was another factor which also weighed heavily in the final decision.

Vicor, which is a major manufacturer of power supplies, was one of the main candidates under consideration based on previous designs completed at SAIC. In fact, Vicor modules were used in the APW I design.

Vicor was thought to have produced a more efficient, smaller power supply than their current VI-j series, but did not. The VI-j series would have been a consideration, but the size of the module was a concern. Vicor indicated that the next generation power supplies will be completed next year.

1) Vicor

The relatively large size of the VI-j Vicor power supplies only allows two modules to fit into the mechanical envelope of the WSM. In order to get the power budget to fit the design constraints, one module would need to be 5 volts, the other 12 volts. In the 18-36 volt range inputs, the VI-j would only supply 50 watts at 5 volts. This is sufficient for the 5 volt supply. The 3.3 volt and 12 volt requirements must then be generated from a single 12 volt VI-j supply. This is technically feasible, but would not be very efficient. The 12 volts could be filtered well enough, however, to increase the noise immunity on the Liquid Crystal Display (LCD) bias supply a 15 volt VI-j would be required. The LCD bias could then be supplied by small linear supply of the 15 volts. With no more than a 3 volt drop, the power loss from the linear would be trivial. The linear regulator would act as both a decoupling and a noise filter. Most backlight supply vendors stock 15 volts as a standard input. A problem with this is that Vicors do not withstand input spikes. Vicor would not guarantee the units operating with an input spike of 45 volts for a duration of 3 seconds, even with the IAM module.

2) Pico

The Pico power supplies require at least a ten percent load on the outputs of the modules. The supplies react to an under load situation by eventually "blowing up" due to over voltage spikes within the power supply. This is an unacceptable side effect, therefore SAIC dropped the Pico power supply from consideration.

3) Interpoint

Interpoint makes a pair of power supplies which met the APW II power requirements. The Interpoint supplies meet most of the requirements such as size, surge suppression, emissions, and Mean Time Between Failure. The model numbers that were evaluated were the HR703-2812 for the 5 volts and "clean" 12 volts, and the HR301-2812 for the "dirty" 12 volts and 3.3 volt supply. These modules can tolerate the 45 volt spike, have no minimum load and have a manageable inrush current. However, they are difficult to mount and fit within the mechanical envelope of the WSM. For example, they have a flat plate with pins coming out and are covered with a metal can. In order to heat sink these, they would need to be secured to a metal plate with the pins passing through. Evaluating the WSM design, implied that in order to use the WSM case as a heat sink, the modules would appear as "blisters" on the outside cover. In addition, the Interpoint power supplies are very expensive compared to the other modules evaluated.

4) Modular Devices

Modular Devices also made small packaged power supplies, but were very expensive. They were similar to the Interpoint device, in that they mounted through the heat sink instead of on it. The Modular Device power supplies were not considered for

incorporation in the APW II design due to the expense of the supplies and the mounting configuration issue.

5) EG&G

The EG&G module met most of the APW II functional requirements. It is more expensive than the Vicor's, but much less than Modular Devices and Interpoint. It is 2" x 4.6" x 0.5", which fits well in the projected mechanical layout of the WSM. They operate from 45 volts with spikes up to 55 volts, while not tripping the input protection. The EG&G power supply is over 80% efficient and heat sinks directly onto the surface which is highly desired. It has a 5 volt output with a capacity of providing 15 amps.

The EG&G power supply has a minimum load, but the factory said that the 12 volts can be totally unloaded without any problems. The unloaded 12 volts will rise approximately 10% in voltage. EG&G recommended using a Zener to limit the voltage rise if this is a problem. This would not be a problem since very little current will flow when the LCD is powered down. In this case only the external backlight/bias control switch MOSFETs will see the over voltage, which they can easily handle. If the 5 volts is unloaded, the 12 volts will "droop". The minimum load on the 5 volt output is rated at 2 A at 5 volts, which is not a problem, however, EG&G said that if the full 12 volt output is not being used this can be relaxed to about 1 Amp.

The only problem with the EG&G unit is the cost and availability. The part number evaluated was the LC810, which is the commercial version of the HPC2. Even as a commercial product, the LC810 meets MIL-STD-704D, MIL-STD-810, NAVMAT ESS and MIL-STD-461 noise emission with an external LC filter. SAIC was very pleased with this product and would have used it in the design. However, the product was currently behind in production and EG&G could not commit to a delivery date. For this reason the EG&G product was removed from consideration.

5) AT&T

The AT&T power supply modules that were evaluated, fit within the size constraints of the WSM mechanical envelope, and met the power and voltage requirements. The power supplies could easily be attached to the printed circuit board and then mounted directly to the WSM chassis. The WSM chassis was used to reduce the heat dissipation that the power supplies produce. In addition to meeting the APW II power supply requirements, these modules were also available and reasonably priced, making the AT&T modules the preferred choice for implementation into the APW II design.

In summary, the AT&T modules meet with NASA approval in that they're aerospace "style" power supplies, they are fairly compact which eases the mechanical design constraints, they can be mounted directly to the WSM chassis and they could be procured in time to meet the project schedule.

2.7.3 Battery Charging and Discharging

Preliminary estimates showed that nearly 45-50 watts would be needed at peak power consumption of the APW II unit. This estimate excluded the PCMCIA sockets and battery charging current. The final power budget showed these initial estimates to be low. This presented problems primarily in heat dissipation and in the current loading on the batteries. In order to reduce the peak battery current, the battery pack voltage must be held as high as is reasonably possible and converted down.

To design an efficient charging/discharging scheme for APW II, several different techniques were considered. Following is a summary of each technique.

A simple resistor circuit design-passive solution. This design approach has the following advantages; its inexpensive, it's NASA approved (was used on APW I), and it's hard to break because it's a simple solution. The disadvantages are; it dissipates a lot of heat if the batteries are low, it doesn't deal with overcharging if the spacecraft power rises above the normal voltage (this can be alleviated with a Zener at the input of the circuit), and it doesn't bring the batteries to full charge unless the charge voltage is at or above 24 volts.

A two-stage constant current source. The two-stage constant current is similar to the simple resistor method and has the same advantages and disadvantages of charging more quickly (.1Charge) when the battery voltage is low, and stepping down to a lower trickle rate (.01C) when the battery is "charged".

Active battery charging method. An active charging circuit will charge a battery pack by using a fast charge rate (a high current rate such as 1 C) for a sustained period of time that is calculated by how much charge is stored in the battery pack. An active charger will stop fast charging and start trickle charging (for example 1/64 C) when the battery pack is fully charged. This is important since if the charger continues fast charging, the batteries will heat up, vent and possibly ignite. This is a significant problem with using batteries for space applications because of the stringent NASA flight safety requirements. Adding a two fault tolerant circuit will provide added protection to this implementation.

In summary, the two stage constant current source, with a two fault tolerant circuit, was chosen as the best solution. The main reason is that, if the circuit fails, the worst that can happen is slow charging will continue or charging will stop. In addition, the two-stage constant current source design is more efficient than the simple resistor method and has a linear charge rate as opposed to a non-linear charge rate (charges with external voltage). A two-stage constant current source also has the advantage of lowering the charge rate down to a lower trickle rate should the battery voltage rise.

2.7.4 Power Supply Measurements

Below are power supply measurements that were taken over the input voltage range of 18 Volts to 40 Volts for the APW II in the two configurations described below using the AT&T modules. Although the power input requirement for the APW II is 28 V ± 4 (24 V to 32 V) the APW II was tested beyond these limits to demonstrate the allowable range of input voltage required to support operation on Mir Space Station.

TEST VOLTAGE (V)	MAX POWER (WATTS)	STEADY STATE MAX (AMP)
18	32.8	1.82
22	32.6	1.48
24	32.6	1.36
26	32.5	1.25
28	32.8	1.17
30	33.0	1.10
32	33.3	1.04
34	34.0	1.00
40	34.8	0.87

APW II Configuration 1:

- 32 MB ECC DRAM
- No Battery, No Display Module
- Hard Drive Operating
- Fan on Pentium Operating (1.1 W)
- Running Speed 6.00

TEST VOLTAGE (V)	MAX POWER (WATTS)	STEADY STATE MAX (AMP)
18	49.0	2.72
22	52.8	2.40
24	52.8	2.20
26	48.6	1.87
28	53.2	1.90
30	54.0	1.80
32	54.1	1.69
34	52.7	1.55
40	53.2	1.33

APW II Configuration 2:

- 32 MB ECC DRAM
- Battery & Display Module Connected
- Hard Drive Operating
- Fan on Pentium Operating (1.1 W)
- Running Speed 6.00 & Windows

The following additional testing was done on the APW II:

- Startup Current Test
- Isolation Strength Test
- Isolation Resistance and Breakdown Test

Refer to Appendix 6 for complete test description and results.

2.8 Temperature Sensors

One of the problems faced during the design of the APW II was high internal operating temperature of the unit. The heat generation is primarily from the Pentium, Static RAM (SRAM) and DRAM SIMMs. Special cooling methods were added to compensate for the use of these components. One of the methods used was a monitoring mechanism that reports internal ambient temperature. Two internal temperature sensors, one under the Pentium and one located on the CPU board to monitor ambient internal temperature. Based on the readings of these sensors the Pentium can be cycled down to reduce the amount of heat dissipation.

3.0 DISPLAY MODULE

The APW II Display Module, Part Number 65430-1, consists of a single assembly which includes the Sharp flat panel, the Display PWA and the cable harnesses. Both assemblies are enclosed within the Display Module. The display was designed to support tethering up to 10 feet away from the WSM.

3.1 APW II Display Specification

The display module includes:

- a Sharp 10.4" 1024 x 768 resolution super VGA flat-panel color display (part number LQ10DX01), with 256 color display capability.
- support for power conservation allowing the display to be disabled.
- an anti-reflection coating and hard polycarbonate screen capable of withstanding a 5 pound load applied over one square inch.
- provisions for bulkhead and wall mounting
- design for use in a micro-gravity environment

3.1.1 Sharp 10.4" LCD Display Characteristics

The Sharp Thin-Film-Transistor (TFT)-based display (part number LQ10DX01) is a 10.4-inch, 256 color LCD that is lighter, thinner, and uses less power than its current TFT line. The display itself uses approximately 6 watts and is 12 mm thick. Sharp's backlight, a hot- cathode fluorescent tube, is packaged with the display and uses approximately 10 watts. Below is a list of the LQ10DX01 display characteristics:

• Diagonal screen size	10.4 inch
• External WxHxD dimensions (mm)	283 x 215 x 12.5
• Effective viewing area (mm)	212.0 x 159.0
• No. of pixels	1024 x 768
• Pixel pitch (mm)	0.207 (horz) x 0.207 (vert)
• Color filter	vertical-RGB stripes
• No. of colors	256
• Contrast Ratio	1:80
• Weight (g)	approx. 850

For complete specifications on the Sharp panel refer to Appendix 2. Additional display information is also provided in the appendix.

4.0 BATTERY MODULE

The APW II Battery Module, Part Number 65410-1, consists of a single module which includes a 16 cell battery pack.

4.1 Battery Module Specification

The battery module includes:

- a capacity to operate the APW II for at least 10 minutes at full-power operation.
- Provisions for slow charging through the WSM DC power connection when the Battery Module is attached to WSM.

4.1.1 Operation Characteristics

The battery pack is comprised of 16 Sanyo sub-C NiCad batteries. These cells are rated at 1.2 Volts, 2.3 AHr. Figure 10 is a system diagram of the battery pack. For battery charging and discharging characteristics refer to section 10.3.

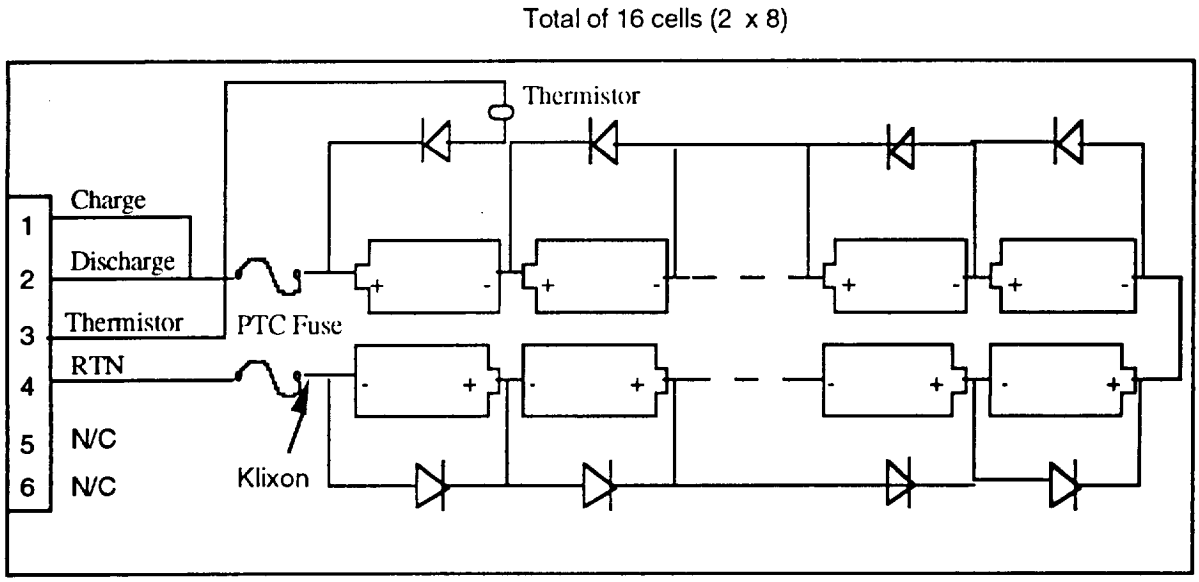


Figure 10 Battery Pack Block Diagram

There are several safety features built into the battery module incorporated to meet the requirements for space flight. Below is a list of these features:

- Two resettable fuses
- Diodes between each cell
- One Klixon (a temperature sensitive ressetable fuse)
- One thermistor (temperature feedback mechanism for external fast charge)
- The battery cells are wrapped in a non-woven polypropylene material
- The battery module chassis is painted with a KOH resistant coating

The ressetable fuses will open the charge/discharge or return lines if there is a large current draw or source current. The main purpose of the fuses is to protect the battery pack and the internal circuitry of the WSM from possible damage.

The diodes between each cell allow current to flow in only one direction, preventing reverse polarity charging.

A klixon fuse is part of the battery pack assembly and protects the battery pack from becoming too hot. The Klixon fuse will trip if the battery pack exceeds 70 °C.

The thermistor was added so that a fast charger could be used to charge the battery pack. For fast charging the thermistor is one of the feedback mechanisms used for switching from fast charging to trickle charge.

The battery module chassis is coated with a black hard anodize for additional protection against KOH electrolyte leaks. For added safety absorbent, non-woven polypropylene material was wrapped around the batteries to absorb any leaking electrolyte. The material used was Part Number MAT204, manufactured by NEW PIG Corporation in Pennsylvania.

4.1.2 Battery Pack Operational Configuration

Table 4-1 shows the various configurations in which the APW II can be configured with the battery module attached, and the resulting conditions.

Table 4-1 Battery Pack Operational Configuration

SWITCH POSITION	EXTERNAL POWER	BATTERY PACK	STATE
OFF	CONNECTED	CONNECTED	BATTERY CHARGING
ON	CONNECTED	CONNECTED	CHARGING & UNIT ON
ON	DISCONNECTED	CONNECTED	UNIT OPERATING OFF BATTERY
OFF	DISCONNECTED	CONNECTED	UNIT OFF/ BATTERY DRAWING NO CURRENT
ON	CONNECTED	DISCONNECTED	UNIT ON/ BATTERY NOT BEING CHARGED

5.0 KEYBOARD MODULE

5.1 Keyboard Module Specification

The APW II Keyboard Module, Part Number 65420-1, consists of a keyboard assembly (printed circuit card and components). The keyboard assembly consists of an alphanumeric American Standard 82 key 'QWERTY' style keyboard with function keys, screen/cursor control keys and four keyboard status indicators. The keyboard supports the IBM-PC AT type 101-key keyboard functions. Figure 11 shows the layout of the keyboard keys.

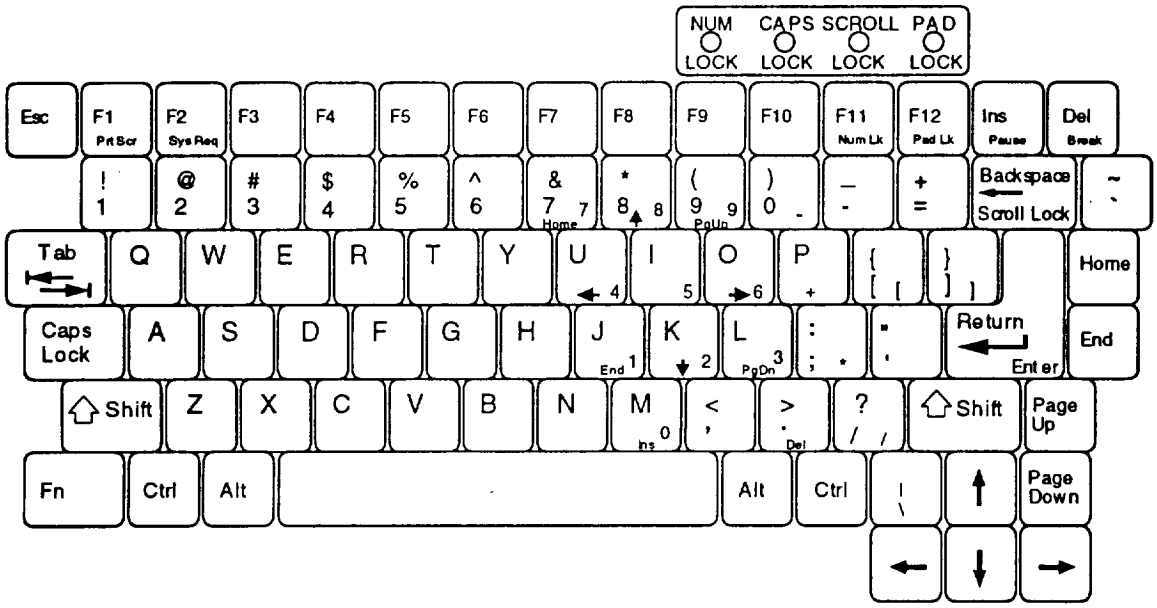


Figure 11 Keyboard Key Layout

5.2 Operation Characteristics

The keyboard electronics support 82 keys with minimum 3-key rollover and the following functions:

- Reset the keyboard micro controller and initialize variables upon power up or software reset.
- Scan the keyboard for key status changes.
- Transmit any available data or status (if enabled by the system).
- Receive, acknowledge, and execute commands from the system.

Appendix 4 contains the complete specification for the keyboard electronics.

6.0 APW II MECHANICAL CONFIGURATION

The APW II is comprised of four main modules, the Wireless Server Module, Display Module, Battery Module, and the Keyboard Module. The modules include the following basic mechanical configurations:

(a) All modules securely attach together in a manner to allow operations in a bulkhead or desktop configuration. See Appendix 1 for the mechanical outline drawings.
(b) The WSM is capable of operating as a stand alone module, without the keyboard module or display module connected.
(c) All modules were designed to comply with the storage requirements of the Space Shuttle and Mir Space Station
(d) All modules were designed with rounded edges and corners

The most challenging aspect of the mechanical design were meeting size and weight constraints, while not exceeding the 45 °C external touch temperature requirement.

The goal was to design the APW II so that all the modules fit within the Shuttle Middeck storage locker. The overall size of the APW II is depicted in Appendix 1 and shows the unit in a storage configuration.

The design goal for one Wireless Server Module (11 lbs), one Display Module (7 lbs), one Keyboard Module (3 lbs) and one Battery Module (4 lbs) was a total weight of 25 lbs. The actual combined total weight of all four modules was 24.5 lbs, meeting the design requirement of 25 pounds or less.

	Actual Weight (lbs)
a) Server Module (Part Number 65460-1)	9.0
b) Display Module (Part Number 65430-1)	8.0
c) Keyboard Module (Part Number 65410-1)	3.5
d) Battery Module (Part Number 65420-1)	4.0
	24.5 lbs

The WSM was the only module that required active cooling primarily due to the use of the Pentium and other high heat dissipating components such as the DRAM SIMMS, the cache and the power supply. The Pentium chip alone produces up to 10 watts of heat. Another major source of heat was from the power supply. Together, these two components contributed more than 50% of the heat dissipation. To minimize the heat dissipation, two fans were used. One fan resided on top of the Pentium chip itself, while

another fan was used to cool the internal ambient air. This fan was located near the Pentium with the air flow going across the Pentium and the SIMMS.

The power supply modules were directly mounted to the WSM chassis. This approach provided sufficient heat sink to disperse the heat generated from the power supplies and still meet the 45 °C external touch temperature requirement. Additional thermal survey test results can be found in Section 10 of this report.

6.1 Wireless Server Module Mechanical Configuration

The WSM provides mounting and interface provisions for both the display module and the keyboard module. The mounting provisions and electrical interface were designed to be unobtrusive when the display module and the keyboard module are detached from the WSM. The connectors on the WSM for the Battery Module power input and the Display Module data input have protective caps when not connected to protect against electrical hazard. Appendix 1 shows the mechanical outline drawing for the WSM.

6.2 Display Module Mechanical Configuration

The APW II Display Module assembly contains an LCD, and a hot cathode fluorescent backlight. These items contain organic liquid crystal material, glass and trace quantities of mercury vapor. The release of any of this material into the spacecraft atmosphere is considered a serious hazard.

To prevent accidental breakage of the display glass assembly, an optical filter, with a 5 pound/square inch load, is used in front of the display glass for protection. To contain leakage of the display organic material the DM incorporates venting using a carbon plug to trap hazardous organic materials. In addition, an environmental gasket seal was used around the perimeter of the DM chassis for added containment.

The DM provides mechanical mounting to the WSM allowing two display angle positions while in the desktop configuration and one position in the bulkhead configuration. Appendix 2 shows the mechanical outline drawing for the DM.

6.3 Battery Module Mechanical Configuration

The BM provides mounting provisions with the WSM that allow both modules to function as one integral unit. The BM also has provisions for mounting to a bulkhead by using a ball and clamp swivel system (part number is 64270-1) developed by SAIC for micro-gravity applications. Appendix 3 shows the mechanical outline drawing for the BM.

6.4 Keyboard Module Mechanical Configuration

The KM provides a mechanical mounting bracket to the DM allowing the keyboard to be mounted in the bulkhead configuration. The KM may also be used in a desktop configuration. Appendix 4 shows the mechanical outline drawing for the KM.

6.5 Printed Wiring Assemblies (PWA)

6.5.1 CPU PWA Layout

See Appendix 1 for the CPU PWA board layout.

6.5.2 Power Supply PWA Layout

See Appendix 1 for the Power Supply PWA board layout.

6.5.3 Display PWA Layout

See Appendix 2 for the Display board layout.

6.6 Special Safety Design Characteristics

6.6.1 Conformal Coating

As part of meeting the safety requirements for electronic equipment aboard the Shuttle, CPU PWA, Power Supply PWA, NTSC Video card, SIMMS, hard drive interface board were conformally coated. The material used for conformal coat was Dow Corning 3140 RTV, applied per the approved NASA procedures for spray application of RTV for electronic assemblies. See Appendix 11 for additional information on the procedures and the RTV material.

6.6.2 CPU Backup Battery Circuit Protection

A Lithium battery is considered a hazardous device by NASA. The battery can explode, releasing toxic materials, unless electrical precautions are designed into the system. A small lithium battery is used in the real-time clock circuit of the APW II. A two-stage protection circuit was added or the battery, consisting of a diode and resistor in series, which limits the current to and from the battery. For complete schematic details refer to Appendix 1. For the lithium battery data specifications refer to Appendix 11.

7.0 WIRELESS COMPUTING DEVICES

The crew members will use both the Personal Digital Assistant (PDA) and subnotebook to view, modify, and store sample flight data files over a wireless network. The ease of use of the devices in a micro-gravity environment and in the cramped conditions on-board the Mir Space Station will be evaluated by the crew member(s) using the device(s). Both keyboard and pen input devices are to be evaluated. In addition, display readability, and ease of swapping battery packs on-orbit are just a few examples of device operational characteristics that will be evaluated.

Several notebook products were reviewed for the PCT project. Appendix 7 lists some of the products evaluated. The wireless computing devices were selected based on the following criteria:

- Each wireless computing device is Commercial-Off-The-Shelf (COTS) equipment
- Provides a 386 processor or better, 4 MB of RAM, Windows for Work Groups compatible, pen or keyboard input, and a display
- Duplex wireless link (>12 feet,) to the WSM (via PCMCIA or other)
- One PCMCIA type II slot
- The capability to act as a limited wireless keyboard (client/server) to the wireless server module
- Operation at full duty cycle for at least 30 minutes

Based on these criteria, a Hewlett-Packard Omnibook 600C and a Dauphin DTR-2 were selected. Following is a summary of the hardware specifications for each device.

7.1 Hewlett-Packard Omnibook 600C Hardware Specifications

Display	Backlit LCD Color VGA (640 x 480 dots) Local Video bus, 1 MB display memory
Keyboard	Enhanced PC functionality with compact layout Embedded numeric keypad
Memory	RAM: 4 MB, expandable to 16 MB maximum
Mass Storage	Card slots: two PCMCIA slots available (two type 1 or type II cards or one type III card) System slot: one ATA-compatible slot
Interfaces	Serial: one 9-pin 115,200-baud RS232 port (with hardware handshaking) Parallel: one 25-pin bi-directional port Infrared: one 115,200-baud bi-directional port VGA output: one 15-pin color-VGA port Floppy drive: one custom floppy drive port Docking port: one custom port for an enhanced port replicator
Card Slots	Card slots: PCMCIA I/O cards Electrical: PCMCIA version 2.0 (5 V) cards Mechanical: PCMCIA type I, II, III cards
AC Adapter	Input: 100 to 240 Vac (50 to 60 Hz) Output: 12 Vdc, 2.5 A Polarity: negative (inner contact is negative) Operating temperature: 0 to 40°C (32 to 104°F)
Battery Pack	Voltage: 9.6 Vdc
Temperature	Operating: 0 to 40°C (32 to 104°F) Storage with data retention: 0 to 55°C (32 to 131°F)
Humidity	Operating and storage: 90% relative humidity at 40°C (104°F) maximum

7.1.1 HP Omnibook 600C Conformal Coating

As part of the preparation for acceptance testing the Subnotebook's went through a conformal coating process. See Appendix 7 for complete details describing the step-by-step process for the dis-assembly and re-assembly of the SNB.

7.2 Dauphin DTR-2 Hardware Specifications

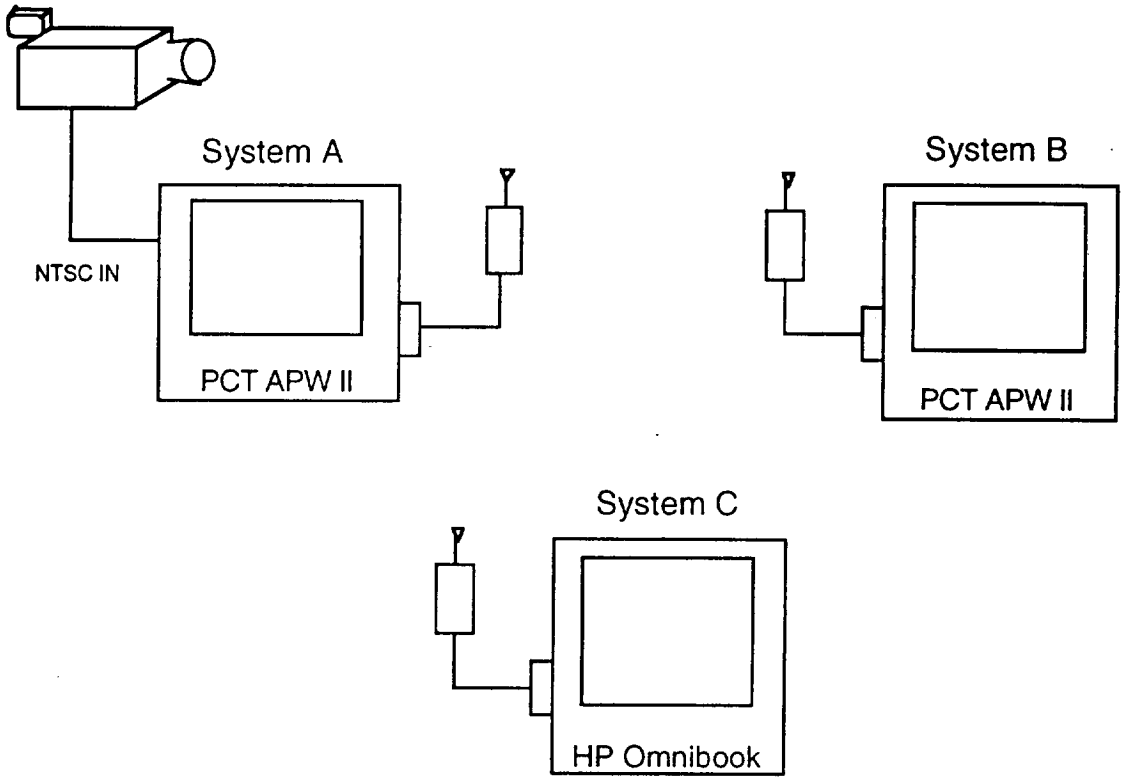
Display	Liquid-crystal display (LCD), 6" diagonal Super VGA (640 x 480 dots), 256 colors
Keyboard	AT/PS2 Style mini-DIN
Memory	RAM: 4 MB, expandable to 16 MB maximum
Mass Storage	Card slots: two PCMCIA slots available (two type 1 or type II cards or one type III card) Fixed drive: 120 MB
Interfaces	Serial: one 9-pin 115,200-baud RS232 port (with hardware handshaking) FDD/Parallel: one 25-pin Centronics: female-type, Multiplexed with proprietary floppy drive interface VGA output: one 15-pin female-type SVGA analog Audio I/O: 2.5 mm stereo phono jack (1 (mono) mic, 1 (mono) speaker) Docking station: configurations supported include: CD ROM, Expanded multimedia sound system, 10 Base-T Ethernet and 14,400 baud FAX/Data modem Card slots: Dual PCMCIA I/O cards
Card Slots	Electrical: PCMCIA version 2.0 (5 V) cards Mechanical: PCMCIA type I, II, III cards
AC Adapter	Input: 90 to 230 Vac
Battery Pack	Voltage: 7.2 V Nickel Metal Hydride
Temperature	Operating: 5 to 38°C (41 to 100°F) Storage: -20 to 60°C (-4 to 140°F)
Humidity	Operating and storage: 80% relative humidity at 38°C (100°F) maximum

8.0 DEMONSTRATIONS

Demonstrations were conducted during the Acceptance Review, with NASA Ames and SAIC, to show both the wireless data transfer and file acquisition capability of the APW II.

8.1 Wireless Data Transmission Demonstration

The setup for this demonstration required two APW II units and a video camera connected to one of the APW II units. The purpose was to show the transfer of real-time video data from system A to System B using the RF Proxim wireless link. In addition to this real-time video images were displayed on System C via the RF wireless link. This capability shows the potential applications for wireless remote maintenance support and other mobile computer applications which require real-time video data.



8.2 File Acquisition Demonstration

Using Intel's Proshare, a video conference software package, and the Proxim Wireless RF card, capability of transferring data files from System A to System B was demonstrated. Files were also transferred from System A to System C.

9.0 APW II SOFTWARE

The APW II software consists primarily of a core Basic Input Output System (BIOS), video and VGA BIOS, Power Management Code, PCMCIA Card and Socket Services and a power on self test (BITF). The system software is comprised of MS-DOS 6.22 and Windows for Work Groups 3.11. In addition, a diagnostic utility is provided to check the basic functional interfaces of the unit.

Software to support all the functions of the CPU PWA was provided by the manufacturer or vendor. The software is in the form of standard BIOS calls, or as device drivers to be executed automatically on power-up from MS-DOS CONFIG.SYS or AUTOEXEC.BAT, or as support utilities. Section 9.1 provides a brief description of the major software elements.

9.1 Software Description

Core BIOS - The Core BIOS is based on an available Off-The-Shelf product (Phoenix BIOS 4.03). The Core BIOS has been customized to meet the various functional requirements and features of the APW II. In addition, support for Advanced Power Management and PCMCIA as a boot device, is provided as part of the software package.

POWER MANAGEMENT - Power Management code is a separate code module for the BIOS core. The Phoenix BIOS 4.03 core is structured to allow modular addition of the power management code, but the module was modified for the specific APW II hardware requirements.

PCMCIA Card and Socket Services - The PCMCIA card and socket services for the CPU PWA is supported by a loadable "Card Manager" device driver. Standard PCMCIA card and socket services (Revision 2.1) are supported. Additional support is provided as an integral part of the core BIOS to support booting from the PCMCIA interface.

Video and VGA BIOS - The CPU PWA Video BIOS includes a configuration program to allow customization of the Video BIOS and support for the Chips and Technologies 65545 video controller. The video BIOS is configured for the Sharp LCD display, P/N LQ10DX01.

PCMCIA - PCMCIA drivers are also available from Phoenix Technologies, Ltd., as well as other BIOS vendors. The Phoenix version is called PC Card Manager PLUS.

Built-In-Test-Facilities (BITF) - The CPU PWA includes Built-In-Test-Facilities (BITF) in the form of a Power-On-Self-Test (POST) from a standard Off-the-shelf BIOS (Phoenix BIOS 4.03).

The BITF checks the following during power up:

- Checks the operation and configuration of the hard disk.
- Checks all peripherals and busses, monitoring system status, error checking, processor checking and DRAM checking.
- Verifies the operation of the communications between the processor and keyboard.
- Verifies the integrity of built-in software (e.g. BIOS).
- Illuminates display/backlight, visual indicators and sounds the external speaker.
- Verifies the operation of the calendar/clock including programmable interrupts.

9.2 Boot Sequence

The Boot Sequence priority is software selectable from a table in the BIOS. The APW II is able to boot from the IDE, floppy or the PCMCIA slot. The order is configurable such that any boot sequence combination is possible.

9.3 Diagnostic Utility

The diagnostic utility developed for the APW II is based on an Off The Shelf (OTS) utility called Checkit, provided by Touchstone Software. Because the Checkit software is only capable of checking the basic system functions (memory, video, floppy, etc.), a custom diagnostic utility was developed to provide a functional check for the NTSC video port, the Ethernet interface, the SCSI II interface, the PCMCIA interface, the mouse port and the battery.

Diagnostics for the NTSC video, Ethernet, SCSI II, and PCMCIA interfaces consist of internal diagnostics of the controllers. The mouse diagnostic verifies communications with the mouse and checks the operation of the buttons. The battery diagnostic verifies the operation of the circuits and reports the battery voltage.

The custom portion of the diagnostic utility is designed to provide a user interface similar to the Checkit environment. The custom utility provides a menu option to execute Checkit.

10.0 TEST RESULTS

The following tests were conducted on the APW II:

- Thermal Survey
- Radiated Emissions (RE02) Characterization
- Battery Pack Discharge
- Environmental Stress Screening
- Software Validation
- Acceptance Testing

10.1 APW II Thermal Survey Test

The purpose of the survey was to verify that the thermal design of the APW II would maintain the chassis touch temperature below the required limit of 45 °C, and maintain component temperatures below their maximum rated level.

10.1.1 Thermal Design

The thermal design of the APW II unit is based on forced air cooling , natural convection, and radiation to the surrounding ambient. There are two small cooling fans within the WSM portion of the unit. One fan is mounted on top of the Pentium chip to maintain its temperature, and another fan draws ambient air through the chassis, exhausting it out the side of the unit. The power supply is the only module mounted in thermal contact to the chassis for heat sinking purposes. Due to the low power within both the keyboard and display, their electronics are designed to dissipate their generated heat via natural convection and radiation.

10.1.2 Thermal Survey Test

The thermal survey was performed at room temperature on a laboratory bench. All testing was performed on June 1, 1995. The unit was operated with the display in both the "desk top" (display up) and bulk head (display down on server) configurations. The unit was also operated within an opened box to see what effect reducing heat transfer via natural convection and radiation had on component temperatures. The unit was operating under windows throughout testing.

Thermal Couples were placed as indicated in Table 11-1, Thermal Survey Test Data.

10.1.3 Thermal Survey Test Results

The results listed are all values achieved under thermal equilibrium conditions.

Test #1 Unit in box, Display down against Server
Test #2 Unit out of box, Display down against Server
Test #3 Unit out of box , but with Display up in "desk top" configuration
Test #4 Same as #3 but with cooling air vents plugged. Test stopped after only 20 minutes due to high Pentium temperature

Table 10-1 Thermal Survey Test Data

TC #	Thermal Couple Location	Test #1	Test #2	Test #3	Test #4
1	Ambient Air	22	22	21	22
2	Pentium Chip	48	47	47	61
3	N/C	–	–	–	–
4	Power Supply	41	41	39	43
5	Exhaust Air	37	36	38	–
6	WSM Chassis Under P/S	40	41	38	43
7	WSM Chassis Bottom Opp P/S	34	33	33	37
8	WSM Chassis Top	34	36	33	37
9	DM Chassis, Center	–	–	27	–

The above results show that having the APW II unit in a box with no top had little effect on the value of the thermal equalized temperatures (difference between test #1 and Test #2). Plugging the cooling air vents had a big effect on the temperatures after just 20 min. This is especially the case with the Pentium chip. This test showed that a large portion of the generated heat is dissipated via forced air cooling. This is substantiated by the rather large increase in air temperature from exhaust to external ambient. Rotating the DM up to a "desk top" configuration (test #3) did reduce temperatures slightly but not significantly.

The maximum chassis temperature is under the power supply, where the power modules are bolted to it. It would require an ambient temperature of 25 °C in order for this portion of the WSM chassis to achieve a temperature of 45 °C in the bulkhead configuration. In the bulkhead configuration though, the bottom of the chassis is not that accessible to

touch. When the DM is raised (as in test #3) the chassis temperature under the power supply drops by 3 °C.

10.1.5 Thermal Survey Conclusion

The results of the thermal survey show that the thermal design of the APW II maintains component temperatures within their rated limits. The Pentium chip, which is the hottest component, is 22 °C below its rated case temperature of 70 °C. Test results also show that the chassis will not reach the touch temperature limit of 45 °C in an accessible area until an ambient of 28 °C is maintained. Test results also reveal that a large portion of the generated heat is dissipated through the fans via forced convection. This shows that when operating in a micro-gravity environment, where the cooling effects of natural convection are minimized, the forced air cooling design of the APW II system will maintain proper component and chassis temperatures. Appendix 5 contains the raw temperature readings for each of the thermocouple locations.

10.2 EMI Test

An EMI test (RE02 only) was conducted on the APW II to establish a baseline EMI characterization of the APW II equipment. Refer to Appendix 5 for complete APW II EMI test data and results.

10.3 Battery Pack Discharging Test

Equipment Used for Testing:

1 APW II WSM
1 APW II BM
1 APW II DM
1 FLUKE 87 Multi-Meter
1 VIEW Sonic 6 VGA Monitor
1 6274B DC Power Supply

The APW II battery pack (see section 4.0 for battery pack diagram) was fast charged for approximately 1 hour and ten minutes with a constant current source set at 2.3 Amps (1 C) at 27 volts, using the DC power supply. At full charge the battery pack was measured, using the FLUKE multi-meter, to be 22.4 volts.

The battery pack was then connected to the APW II system to determine the length of time that it could power the system. The APW II test configuration is shown as follows:

1) No PCMCIA cards installed
2) No floppy disk installed
3) 32 MBytes of EDAC DRAM installed
4) Run video output in simultaneous mode
5) Distec cartridge installed

Power Management of the system was enabled under the custom Power Management Setup option - Power Saver.

Under battery power the unit was turned on and booted into Windows. The unit operated for approximately 50 minutes. The following measurements and observations were made during the test.

Voltage At Battery Pack(VOLTS)	Time Elapsed(Minutes)
19.40 volts	02 minutes
19.27 volts	16 minutes
19.22 volts	18 minutes
19.04 volts	25 minutes
18.89 volts	30 minutes
18.80 volts	32.5 minutes
18.64 volts	36 minutes
18.50 volts	38 minutes
18.38 volts	40 minutes
18.03 volts	44 minutes
17.70 volts	46 minutes
17.25 volts	48 minutes*

* At 49 minutes the voltage dropped off and the system shut down.

Based on the results of these tests a fully charged APW II battery pack will operate the APW II system for approximately 45 minutes with power management disabled. It should be noted that the display was on during entire test to allow monitoring of test.

10.4 Environmental Stress Screening (ESS) Results

The APW II CPU PWA boards were environmentally stressed from 0 °C to 70 °C to screen for infant mortality. Each temperature cycle involved 3 hours hot and 2 hours cold (which results in a cold soak at 0 °C for approximately one hour and a hot soak at 70 °C for approximately two hours). This cycle was continued for a period of 12 hours. Each board was maintained in an operational state and monitored during the ESS process. The results of the testing showed that the boards satisfactorily passed the ESS test with no failed components detected. Refer to Appendix 9 for ESS results.

10.5 Software Validation Test Results

The software validation was run on various software products to benchmark the APW II. The results showed that the APW II is compatible with most of the major operating systems and network application software. Appendix 10 contains the Software Validation test results.

10.6 Acceptance Testing

The acceptance testing procedure (ATP) was developed to test the primary functions of the APW II. These tests typically involve using a COTS software diagnostic tool. However, the APW II design has several interfaces which can not be tested using the standard diagnostic software tool. SAIC developed additional diagnostic software tools to test these additional interfaces. The software was integrated into the existing COTS software package. Section 9.3 contains additional information on the diagnostic utility. Appendix 8 contains a copy of the ATP used to verify functional operation of the APW II.

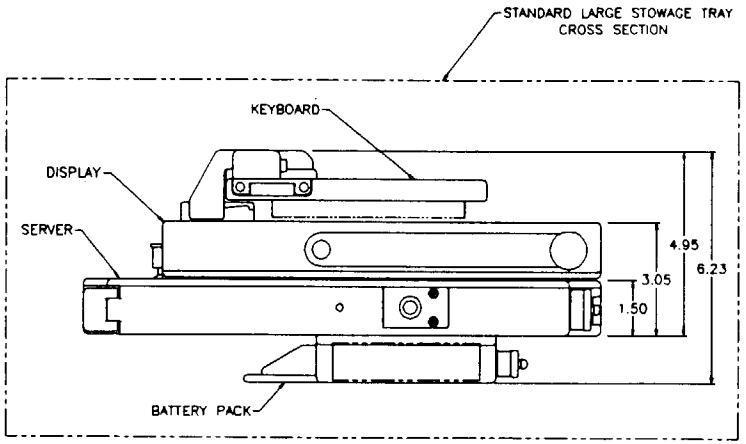
11.0 SAFETY DATA INFORMATION

Equipment that is used for space experiments, must as a minimum conform to certain safety requirements and guidelines. This is to ensure the equipment does not pose a threat to the crew or the vehicle. Typically, the equipment must be non-flammable and must not release toxic or hazardous materials.

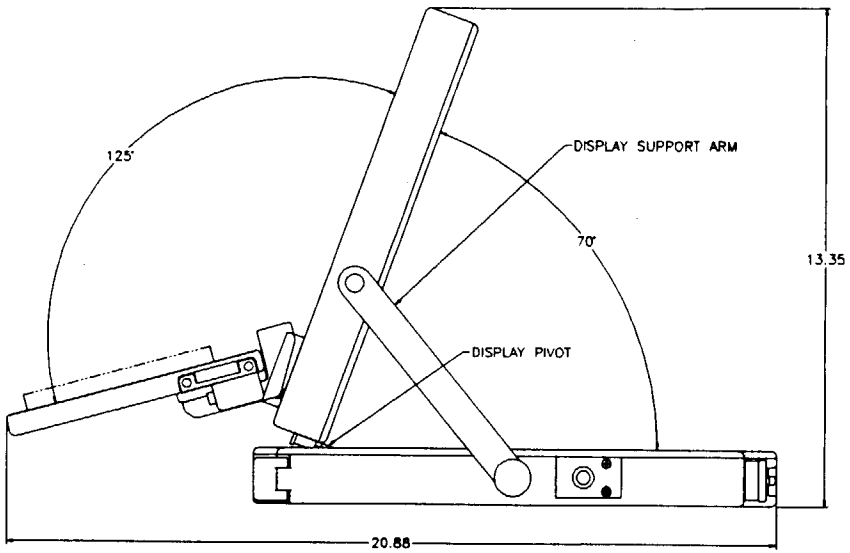
In an effort to conform to the safety guidelines for flight equipment, NASA has conducted flight certification testing and a safety analysis on the APW II unit. In support of this effort, the necessary information on critical components used in the APW II design have been provided. The data sheets for the these components and other critical material is provided in Appendix 11.

APPENDIX 1

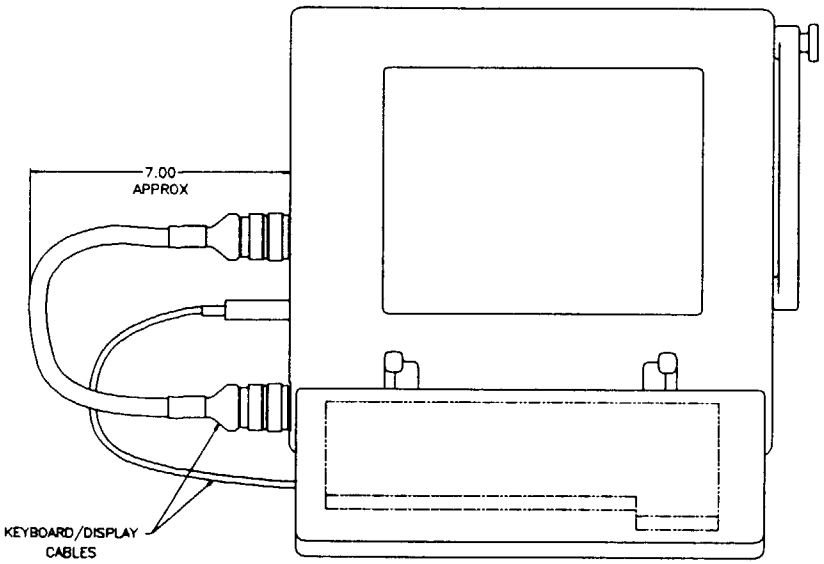
WIRELESS SERVER MODULE DATA SHEETS

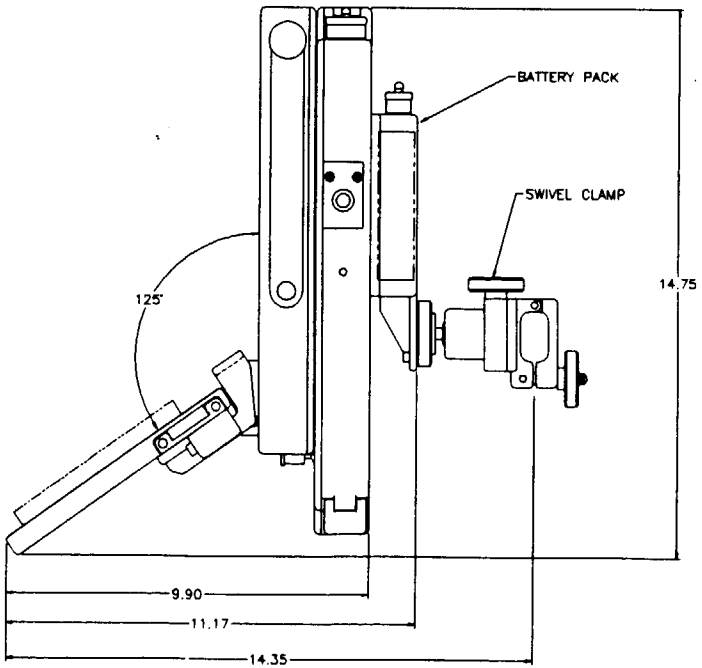


STOWAGE CONFIGURATION



DESKTOP CONFIGURATION





BULKHEAD CONFIGURATION

APW II

OUTLINE DIMENSIONS

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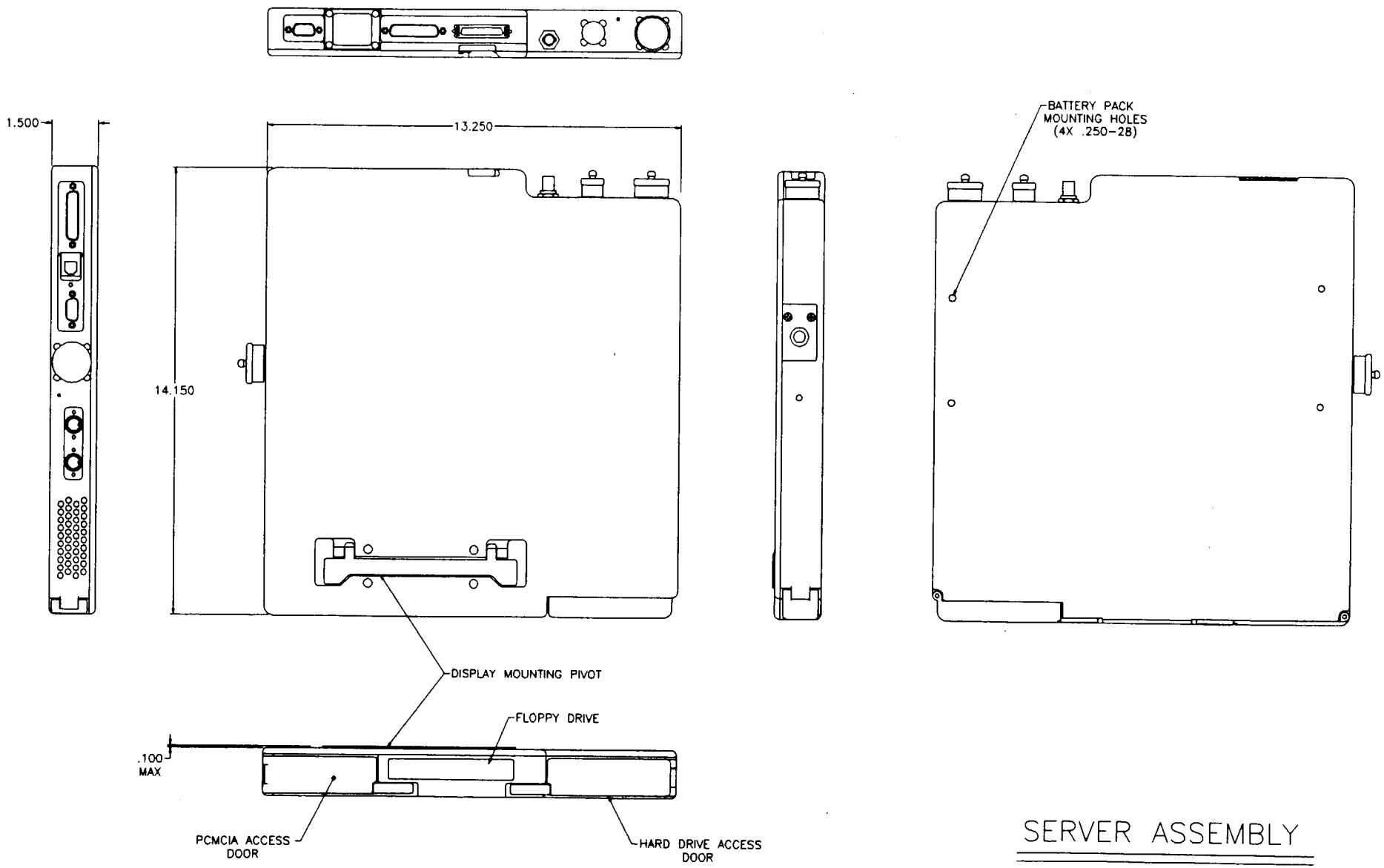

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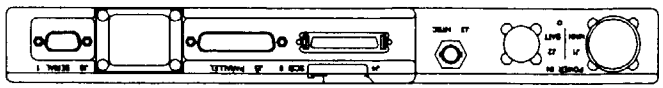
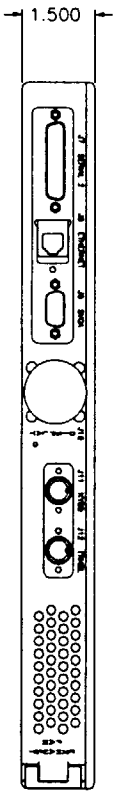
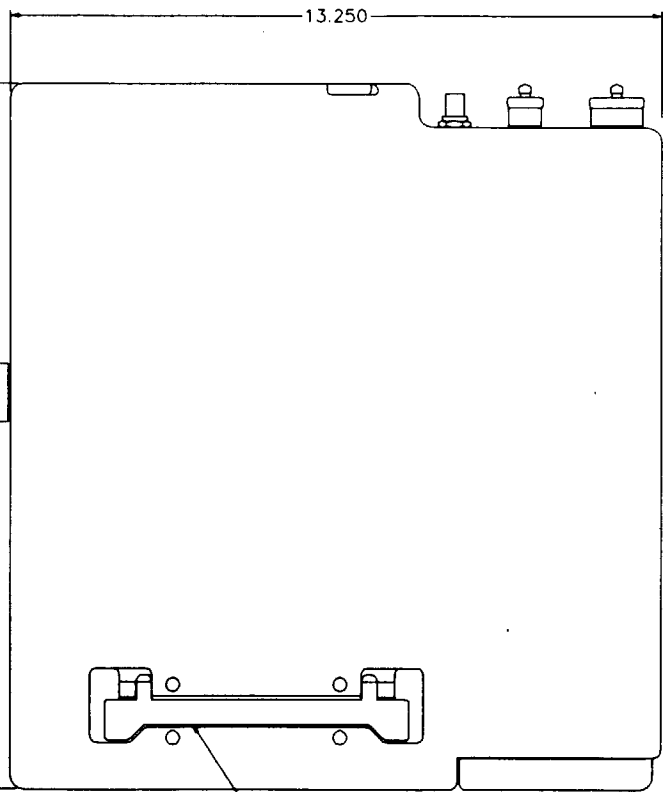
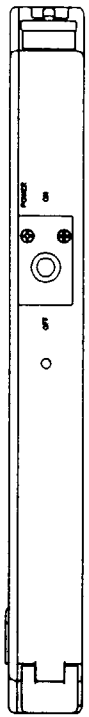
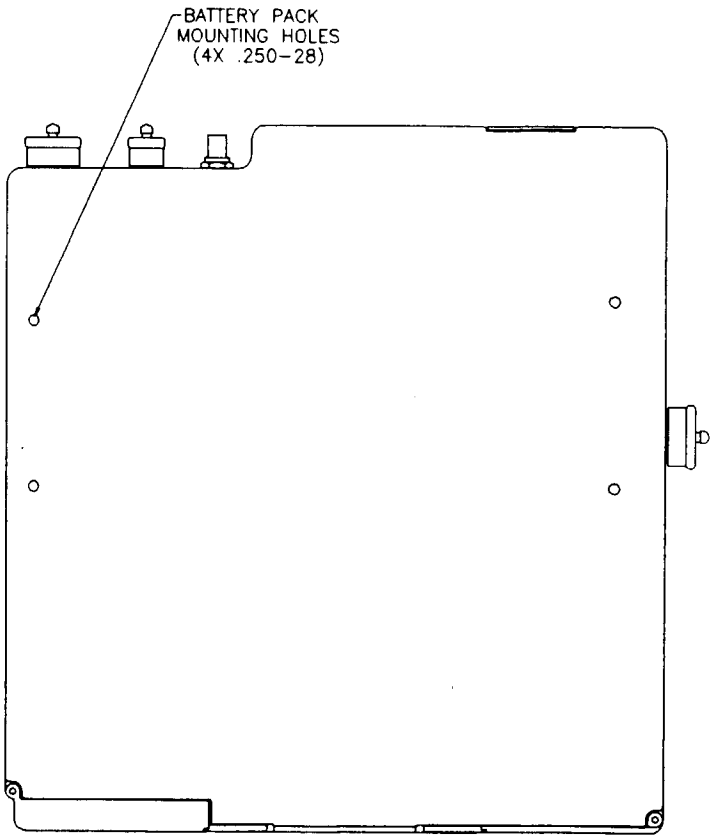
SAI® Technology
A Division of Science Applications
International Corporation

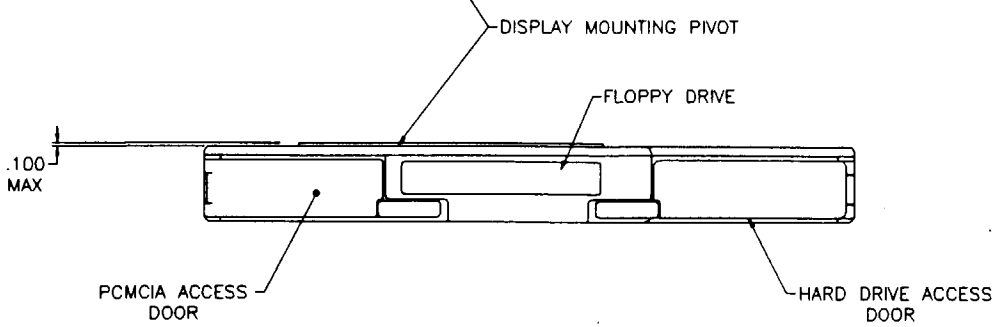












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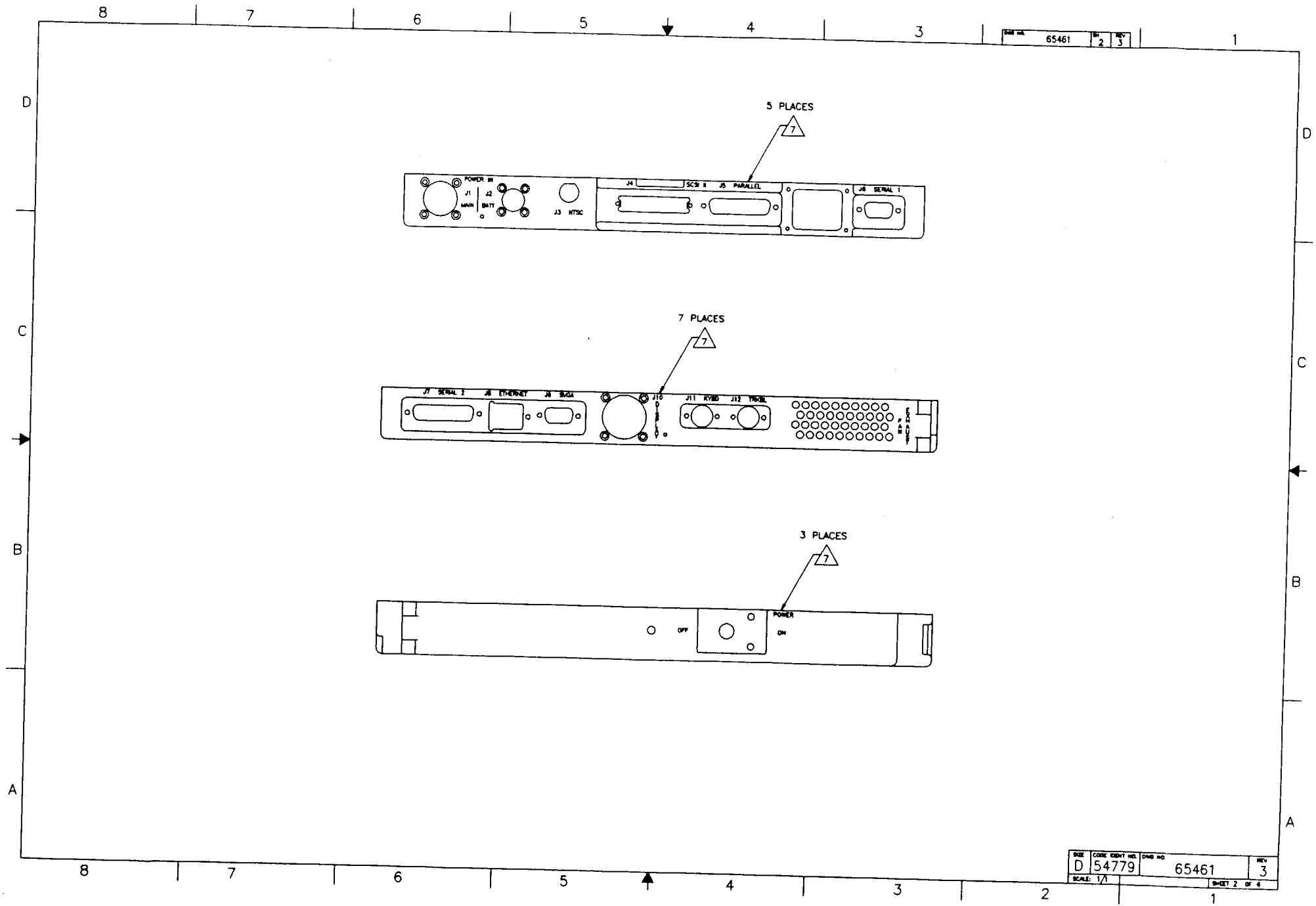
8
7
6
5
4
3
2
1
D
C
B
A
65461
5 PLACES
7
POWER IN
J1
MAIN
J2
BATT
J3 NTSC
J4
SCSI II
J5 PARALLEL
J6 SERIAL 1
7 PLACES
7
J7 SERIAL 2
J8 ETHERNET
J9 SVGA
J10
J11 KYBD
J12 TRKBL
FAN
3 PLACES
7
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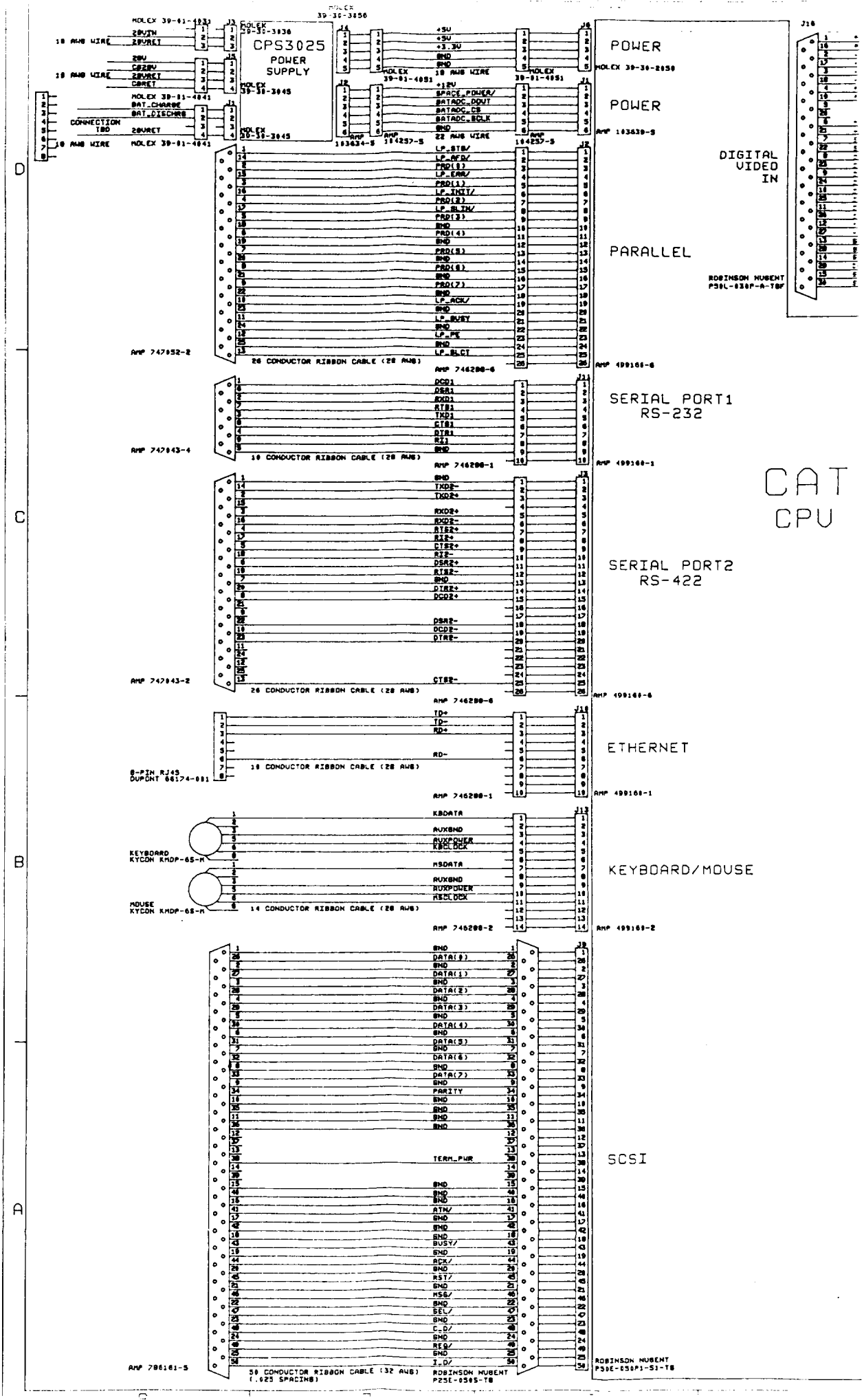
SHEET 2 OF 4

System Interconnect Drawing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POWER SUPPLY
POWER
POWER
DIGITAL VIDEO IN
PARALLEL
SERIAL PORT1 RS-232
SERIAL PORT2 RS-422
ETHERNET
KEYBOARD/MOUSE
SCSI
CAT CPU
20 CONDUCTOR RIBBON CABLE (28 AWG)
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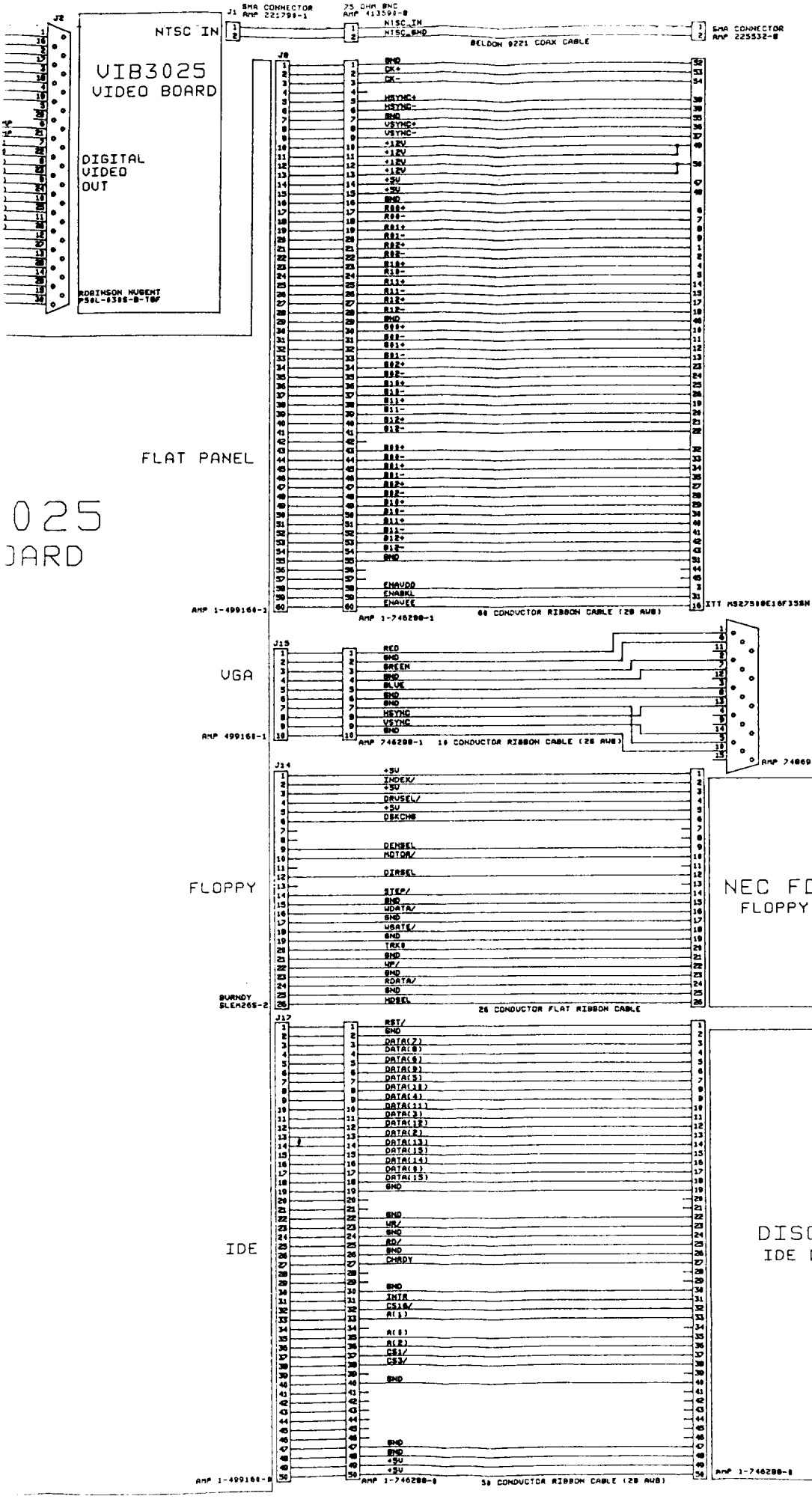
NTSC IN
VIB3025
VIDEO BOARD
DIGITAL
VIDEO
OUT
ROBINSON NUGENT
P50L-8306-B-TGF
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AMP 221798-1
75 OHM BNC
AMP 413598-8
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NTSC_GND
BELDON 9221 COAX CABLE
SMA CONNECTOR
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FLAT PANEL
AMP 1-499168-1
AMP 1-746288-1
68 CONDUCTOR RIBBON CABLE (28 AWG)
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VGA
AMP 499168-1
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BURNDY
SLEM26S-2
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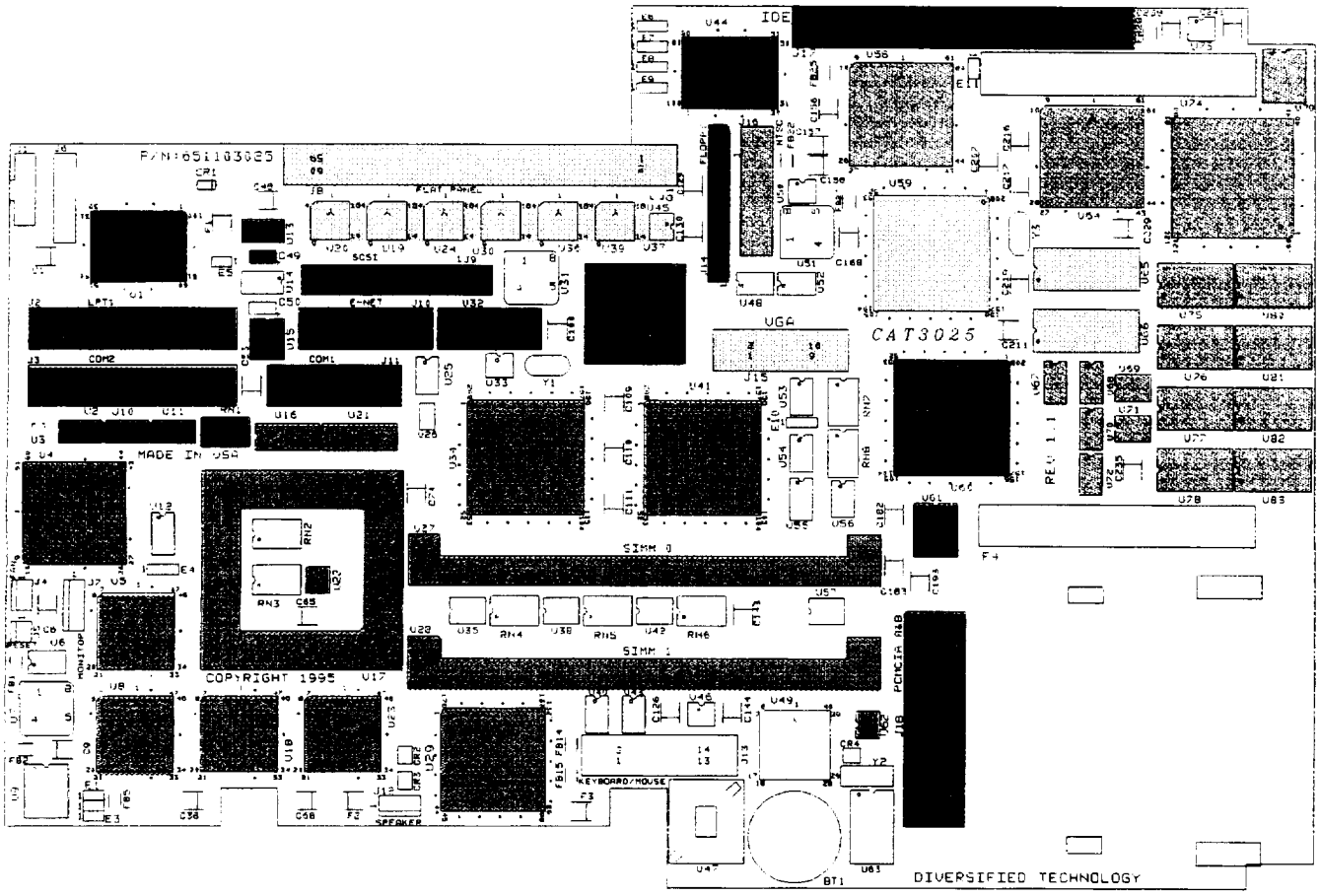
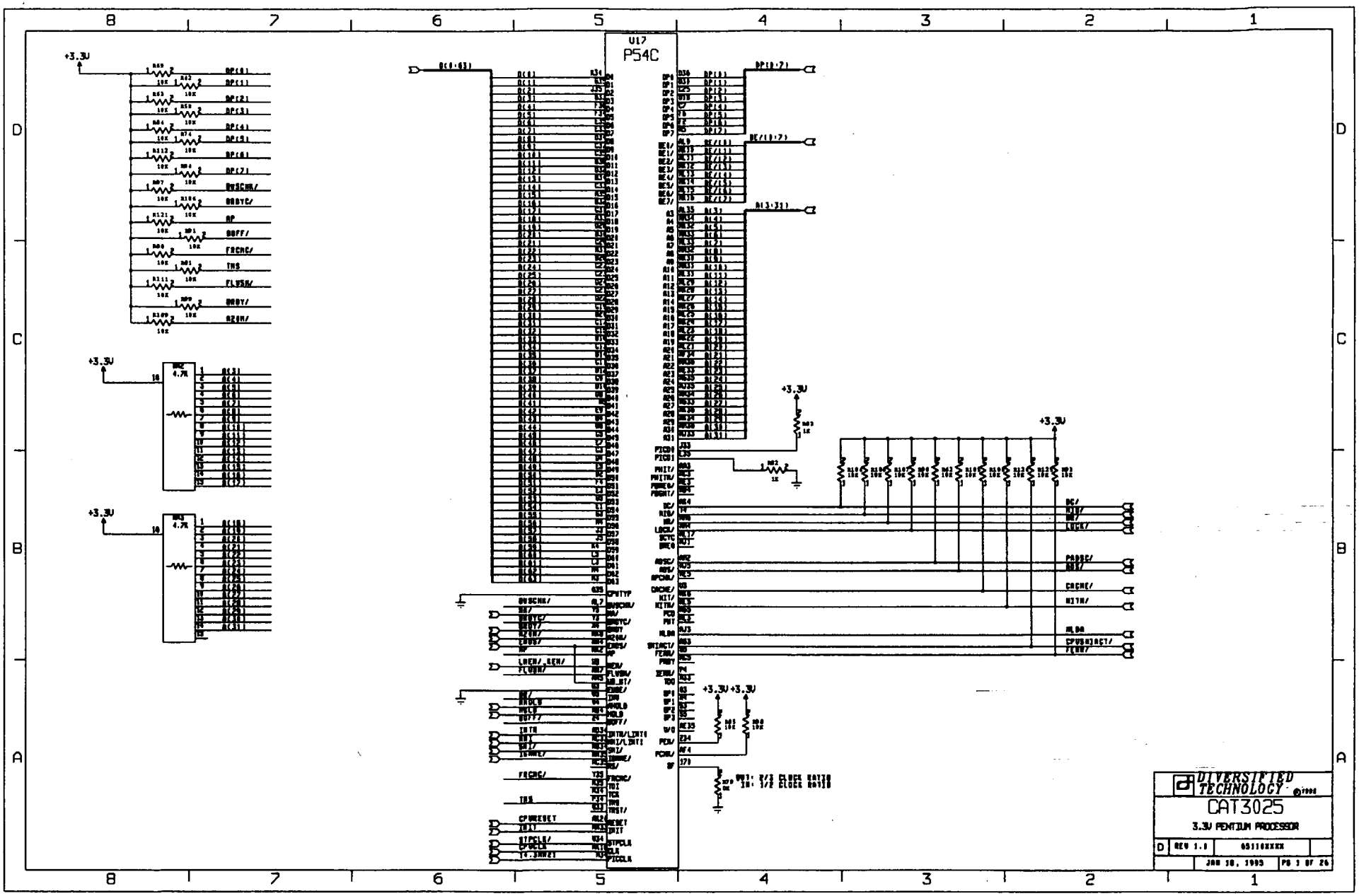
REV 1.0
MARCH 29, 1995

CPU Schematic



CPU PWA BOARD LAYOUT


U17
P54C
+3.3V
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REV 1.0
JAN 18, 1995
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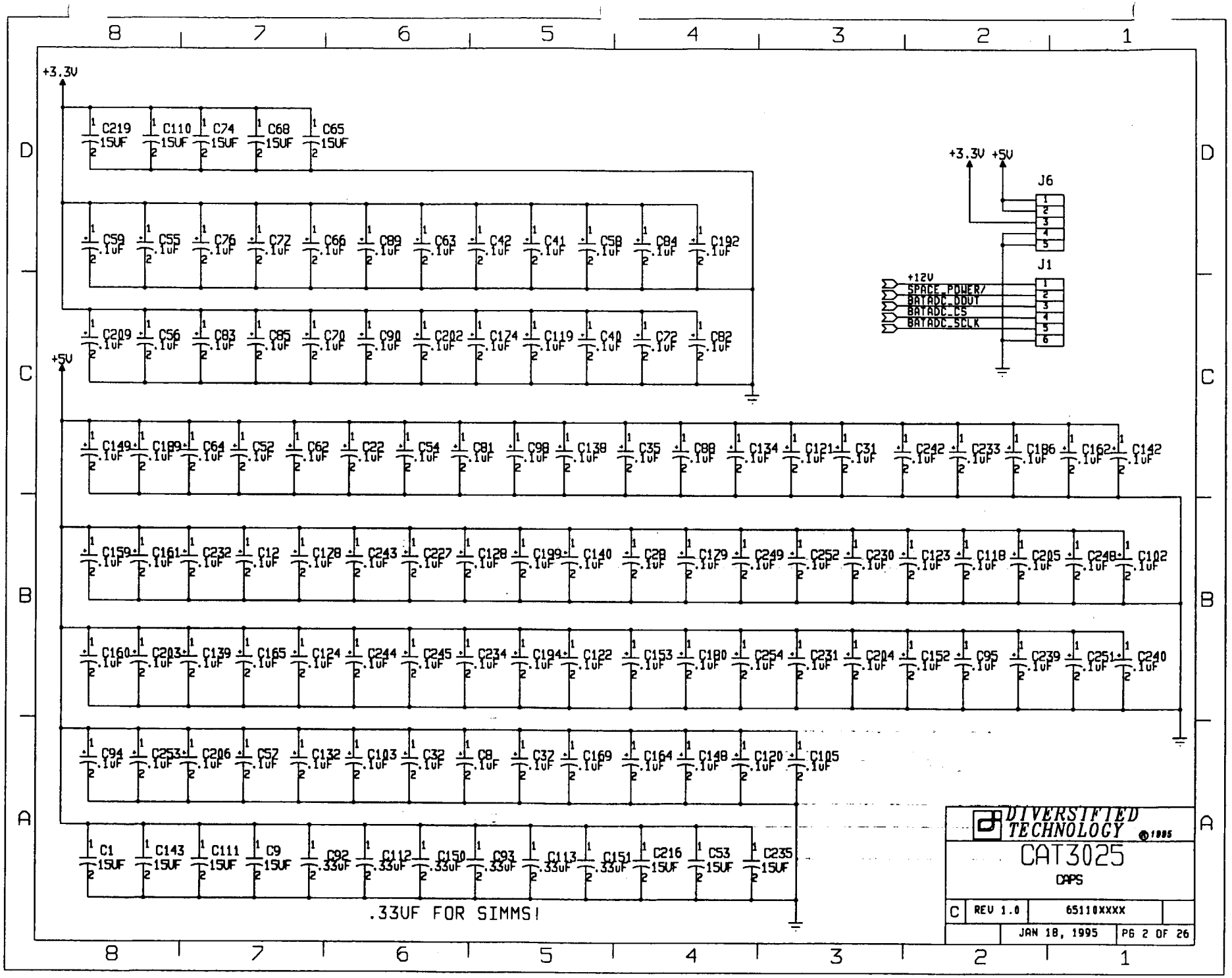
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C77 .1uF
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C189 .1uF
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C81 .1uF
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C243 .1uF
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C252 .1uF
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C239 .1uF
C251 .1uF
C240 .1uF
C94 .1uF
C253 .1uF
C206 .1uF
C57 .1uF
C132 .1uF
C103 .1uF
C32 .1uF
C8 .1uF
C37 .1uF
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C164 .1uF
C148 .1uF
C120 .1uF
C105 .1uF
C1 15UF
C143 15UF
C111 15UF
C9 15UF
C92 .33uF
C112 .33uF
C150 .33uF
C93 .33uF
C113 .33uF
C151 .33uF
C216 15UF
C53 15UF
C235 15UF
.33UF FOR SIMMS!
+3.3V +5V
J6
J1
+12V
SPACE_POWER/
BATADC_DOUT
BATADC_CS
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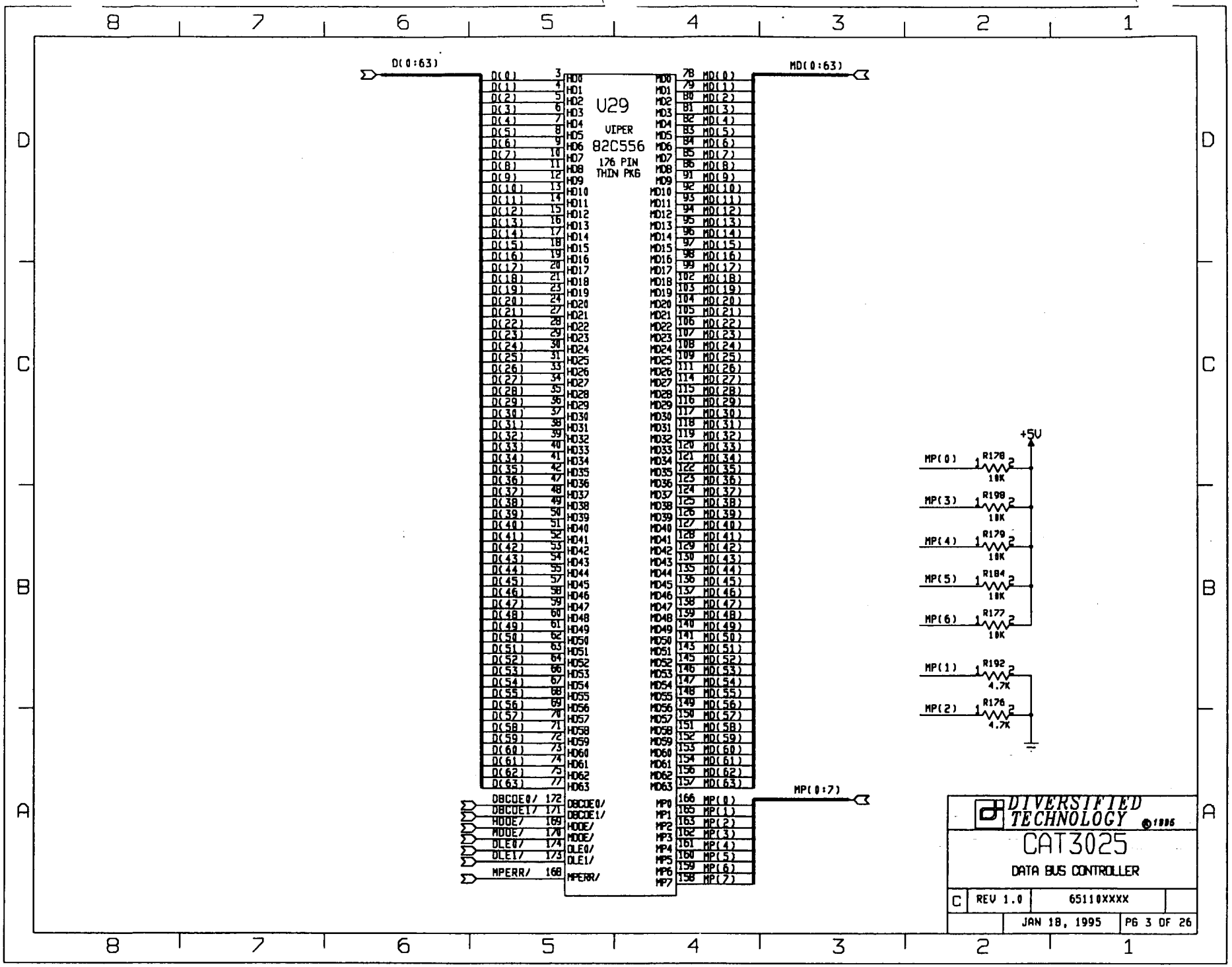
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THIN PKG
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R179
R184
R177
R192
R176
10K
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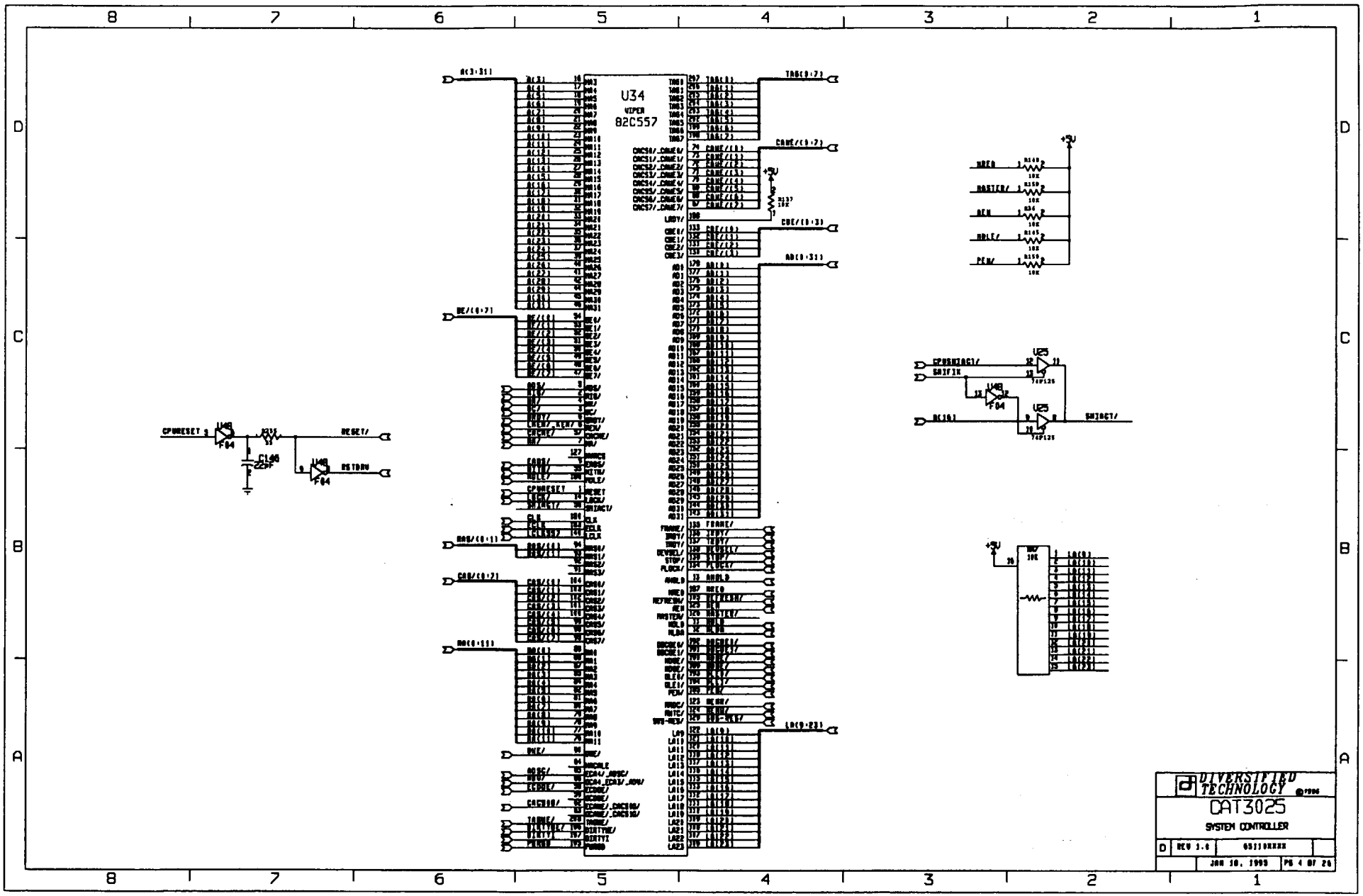
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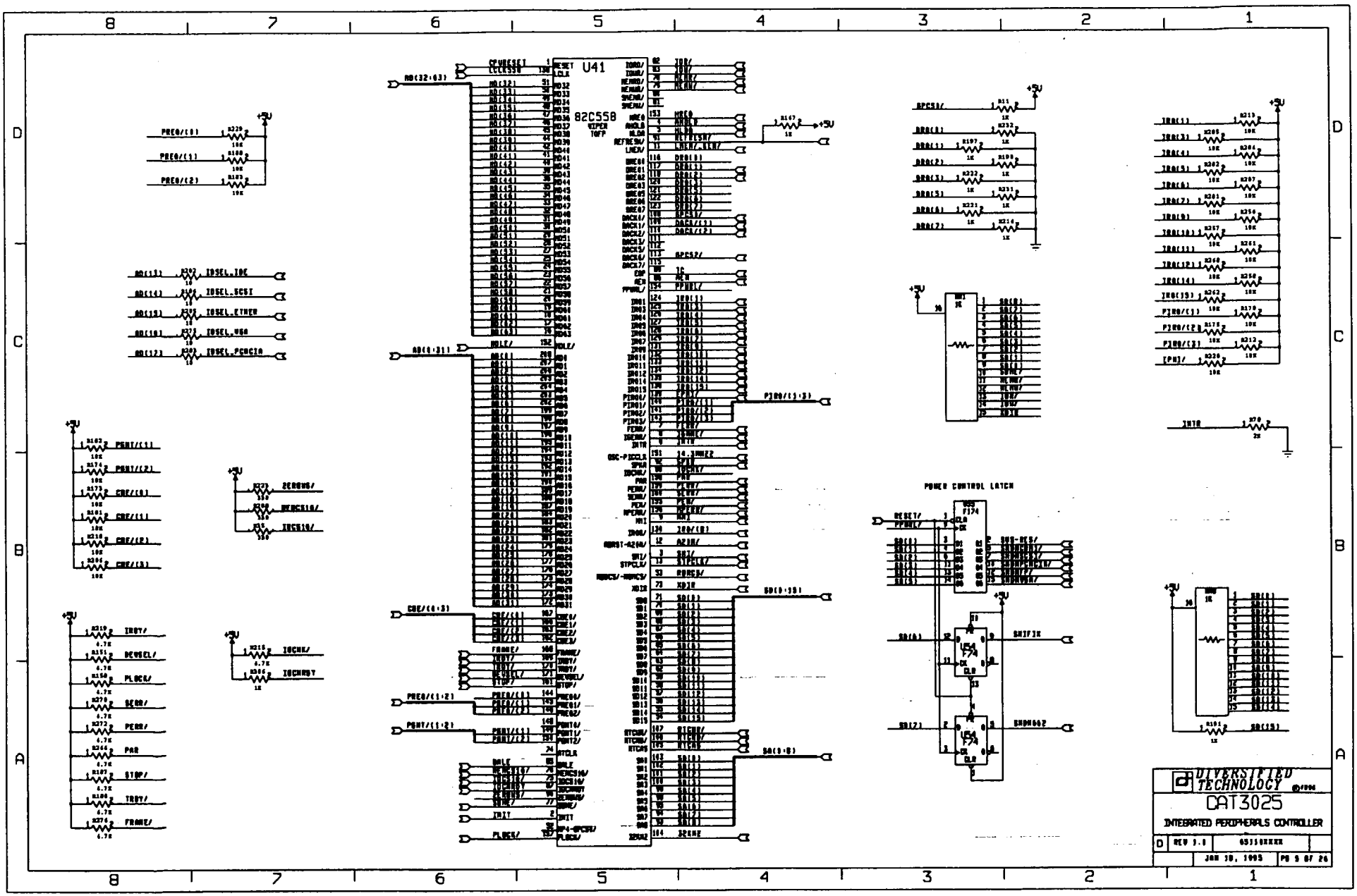
JAN 10, 1995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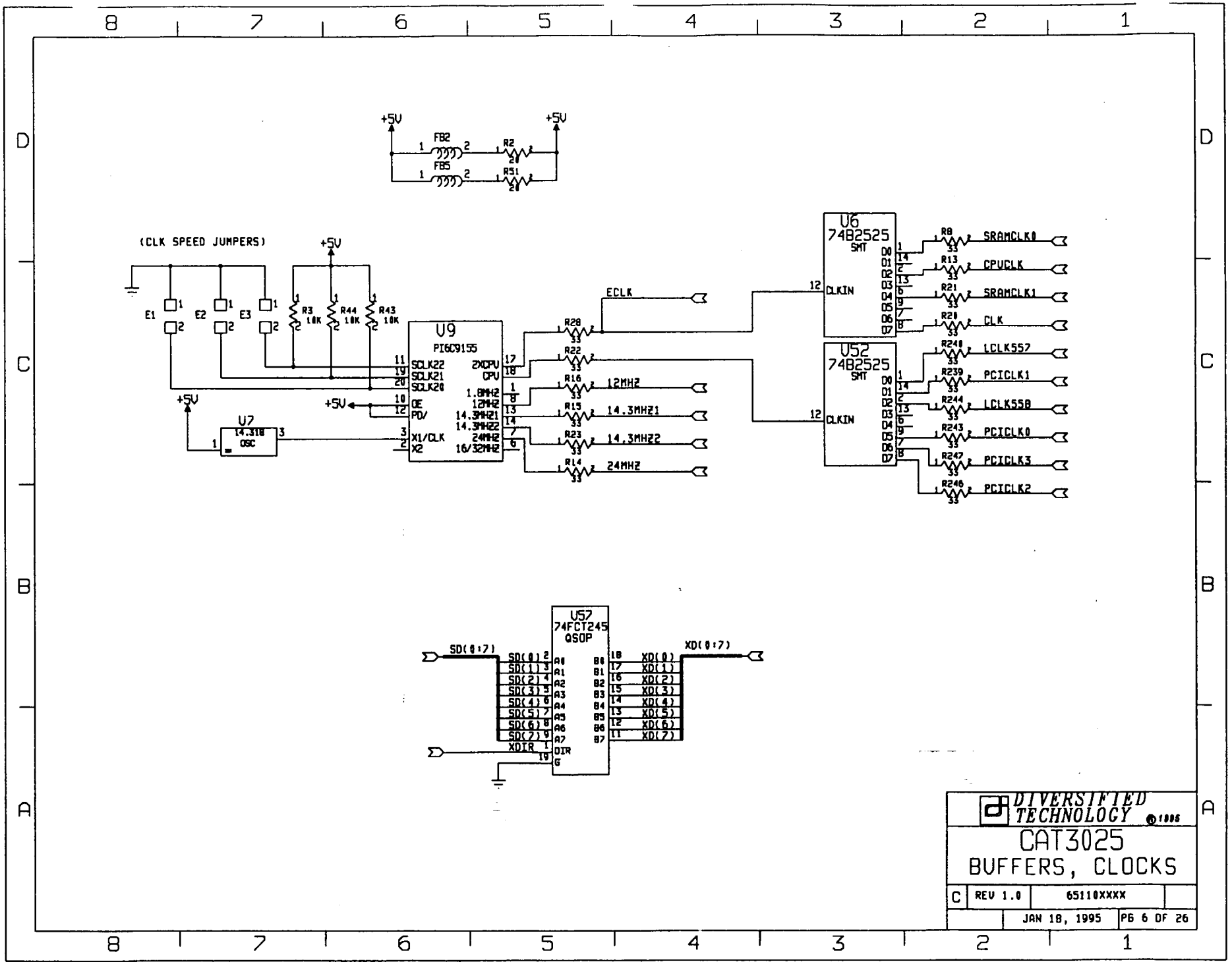
+5V
FB2
R2
FB5
R51
(CLK SPEED JUMPERS)
E1
E2
E3
R3 10K
R44 10K
R43 10K
U9
PI6C9155
SCLK22
SCLK21
SCLK20
OE
PD/
X1/CLK
X2
2XCPU
CPU
1.8MHZ
12MHZ
14.3MHZ1
14.3MHZ2
24MHZ
16/32MHZ
U7
14.318
OSC
ECLK
R28
R22
R16 12MHZ
R15 14.3MHZ1
R23 14.3MHZ2
R14 24MHZ
U6
74B2525
SMT
CLKIN
R8 SRAMCLK0
R13 CPUCLK
R21 SRAMCLK1
R20 CLK
U52
74B2525
SMT
CLKIN
R248 LCLK557
R239 PCICLK1
R244 LCLK558
R243 PCICLK0
R247 PCICLK3
R246 PCICLK2
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QSOP
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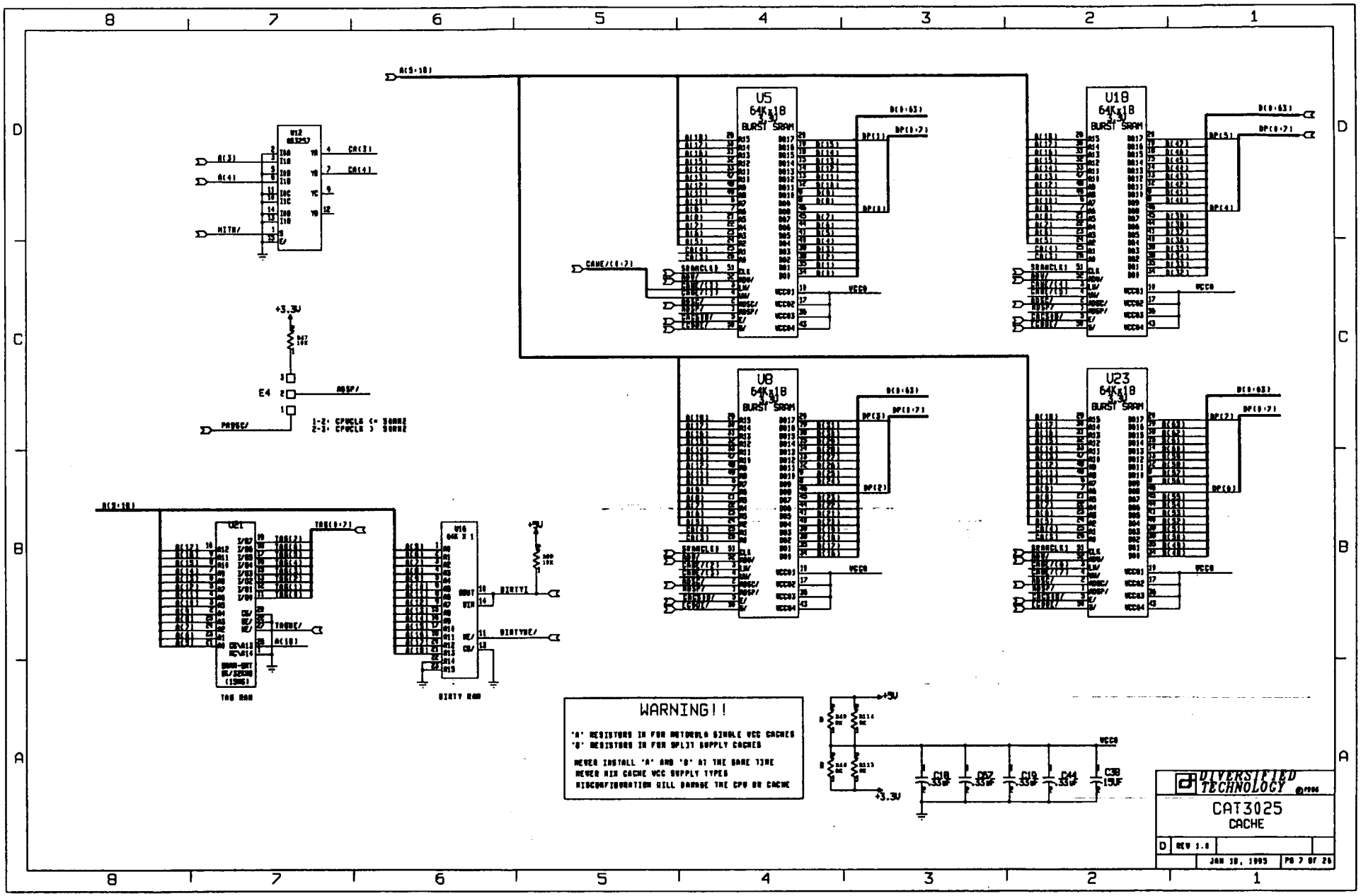
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BURST SRAM
U18
64Kx18
3.3V
BURST SRAM
U8
64Kx18
3.3V
BURST SRAM
U23
64Kx18
3.3V
BURST SRAM
U12
A(3)
A(4)
HITM/
CA(3)
CA(4)
+3.3V
E4
ADSP/
PROC/
1-2: CPUCLK (* 50MHZ
2-3: CPUCLK) 50MHZ
A(5:18)
U21
TAG RAM
TAG(0:7)
TAGOE/
A(18)
U16
DIRTY RAM
DIRTY1
DIRTYOE/
WARNING!!
'A' RESISTORS IN FOR MOTOROLA SINGLE VCC CACHES
'B' RESISTORS IN FOR SPLIT SUPPLY CACHES
NEVER INSTALL 'A' AND 'B' AT THE SAME TIME
NEVER MIX CACHE VCC SUPPLY TYPES
MISCONFIGURATION WILL DAMAGE THE CPU OR CACHE
+5V
+3.3V
VCC0
C18
.33UF
C27
.33UF
C19
.33UF
C41
.33UF
C38
.15UF
DIVERSIFIED TECHNOLOGY
CAT3025
CACHE
D
REV 1.0
JAN 18, 1995
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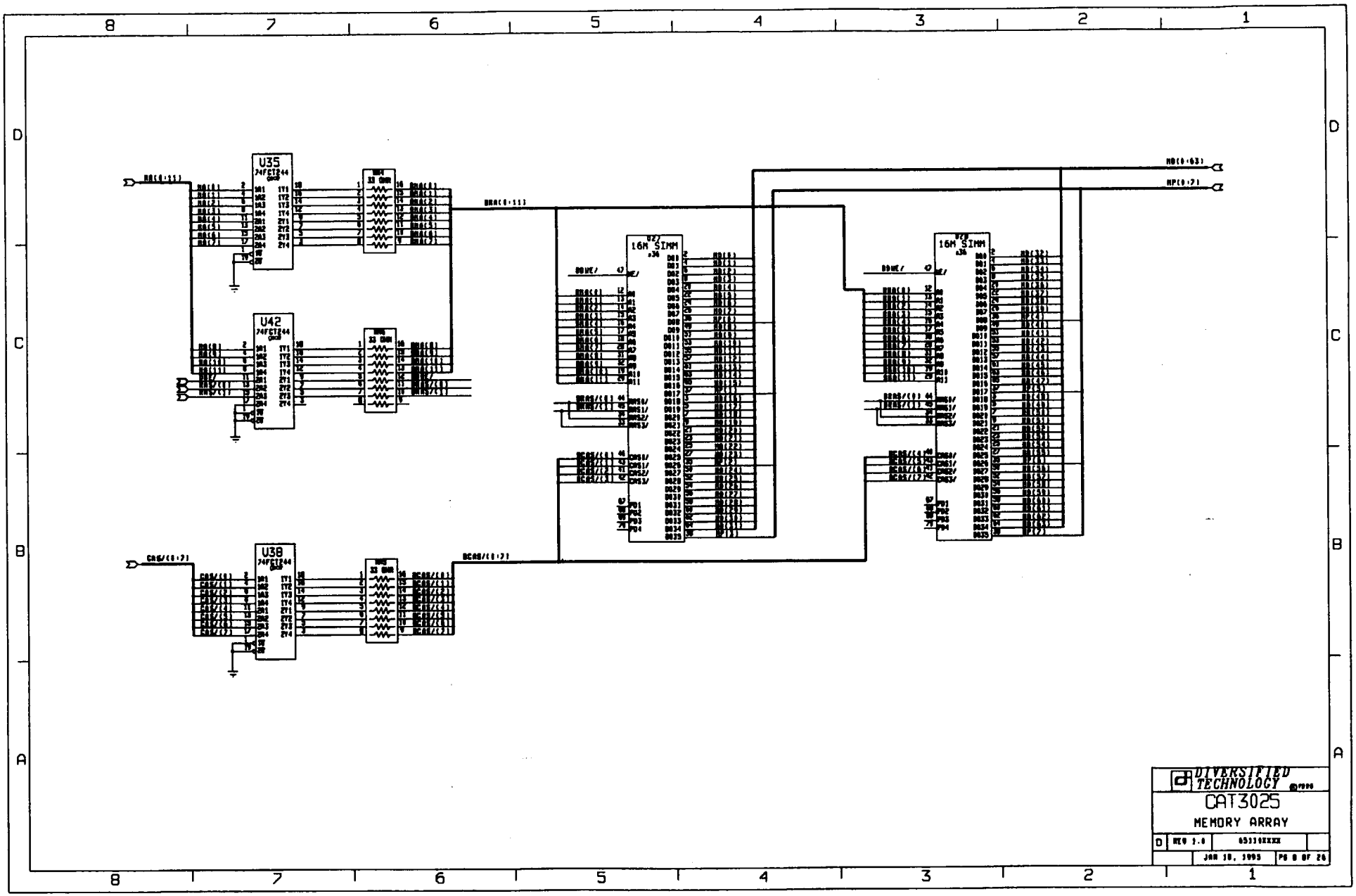
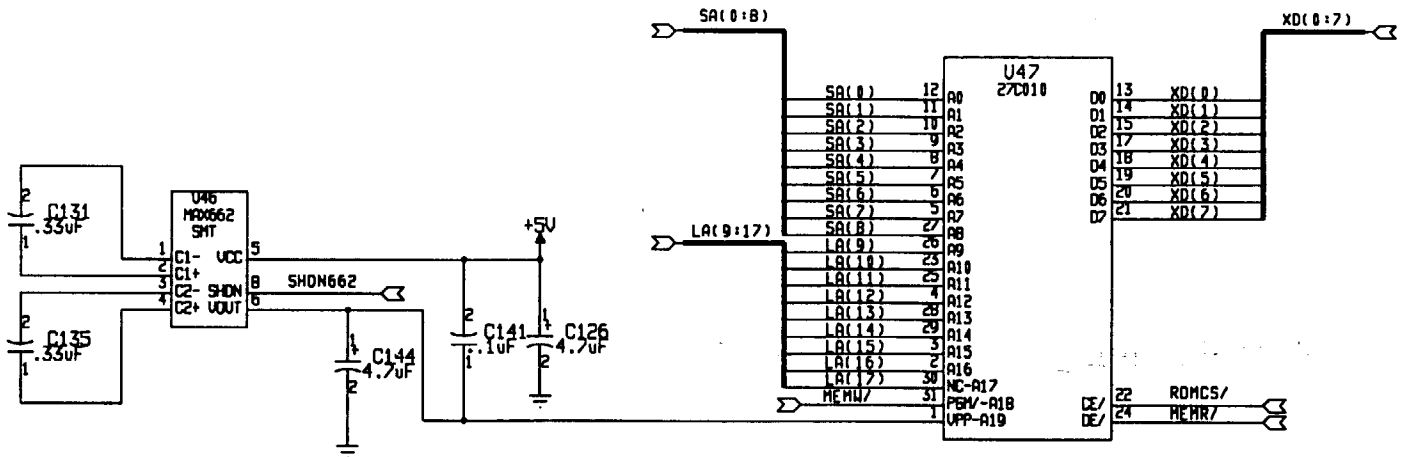

U35
U42
U38
U27
16M SIMM
U28
16M SIMM
DIVERSIFIED TECHNOLOGY
CAT3025
MEMORY ARRAY
REV 1.0
JAN 18, 1995



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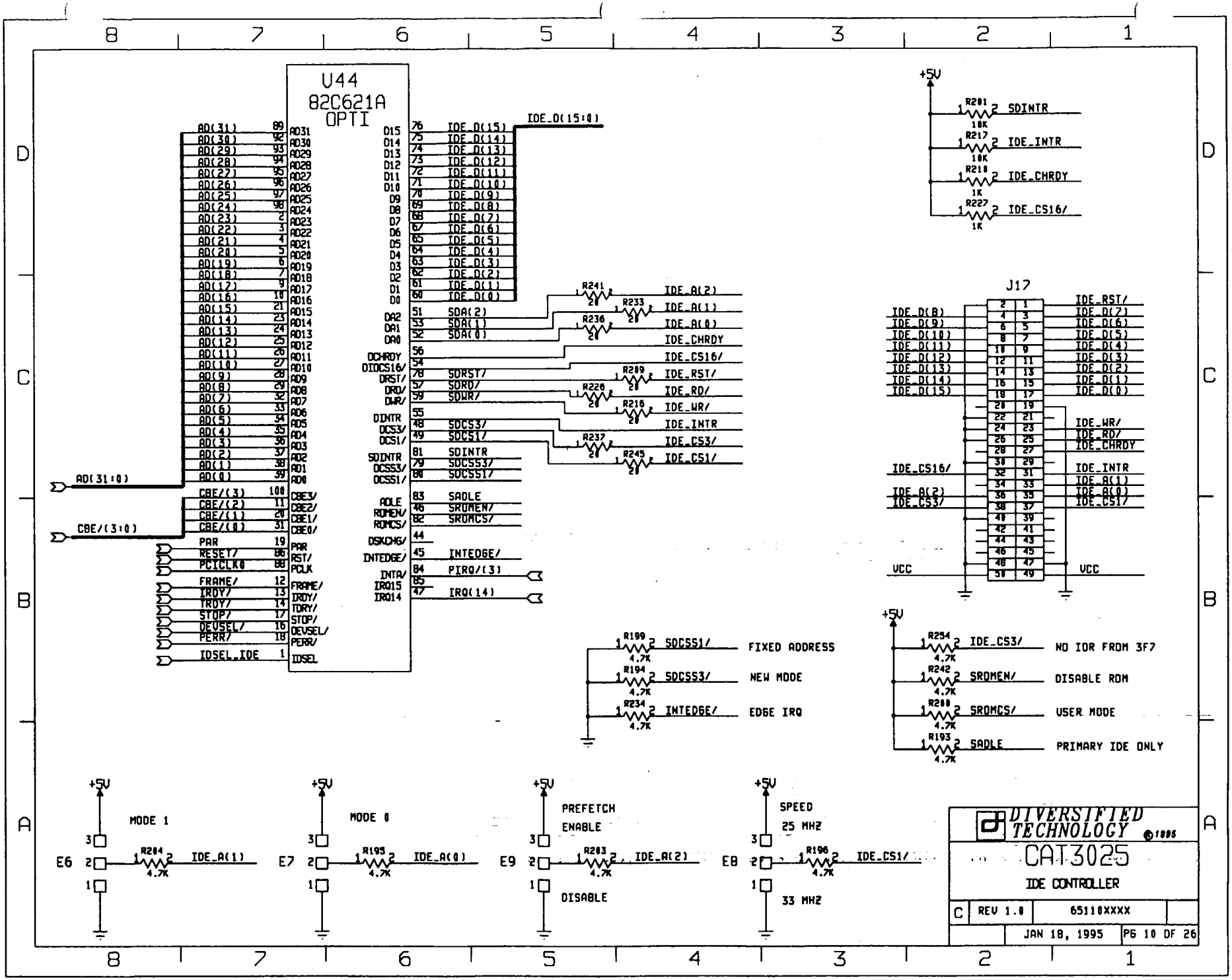
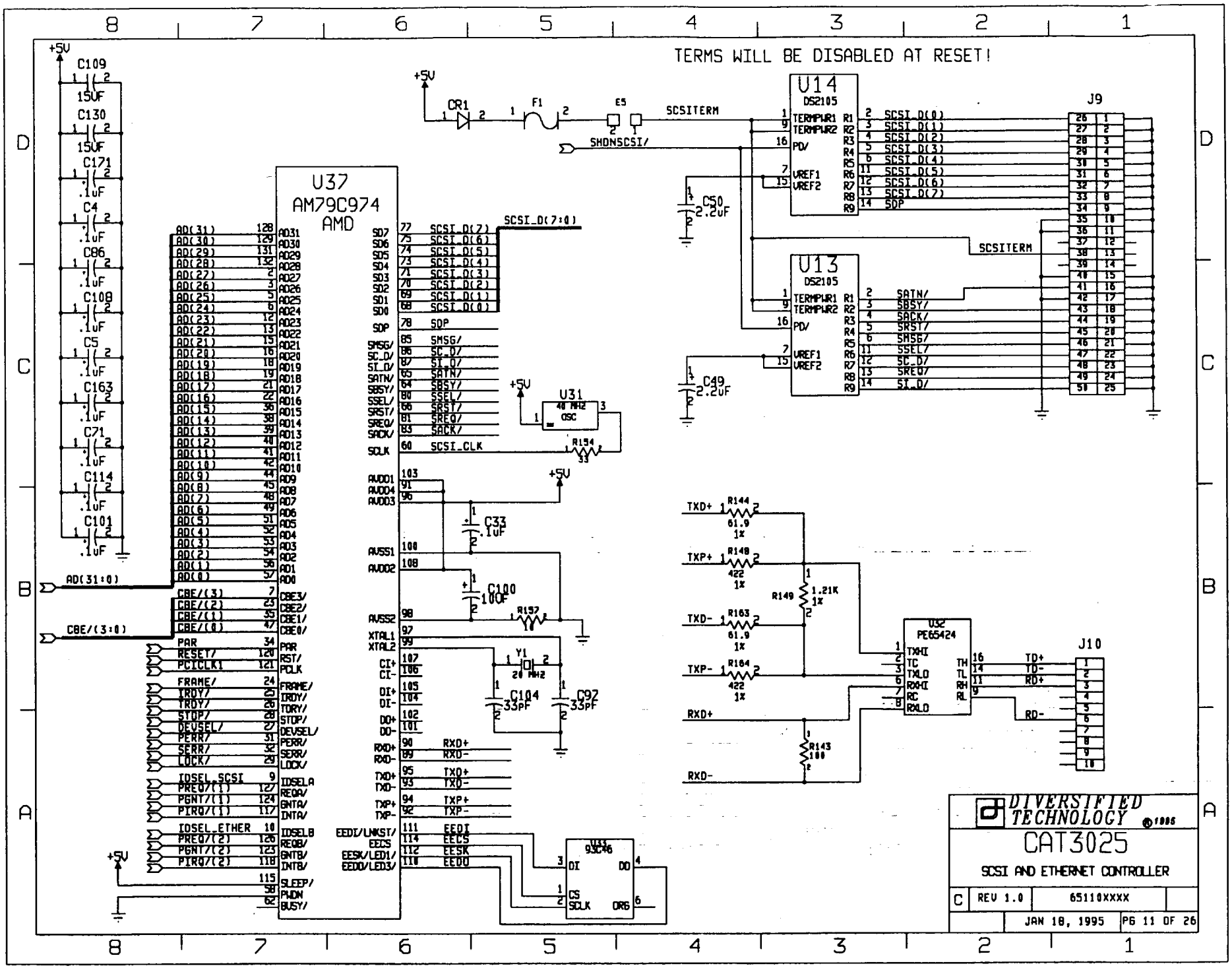
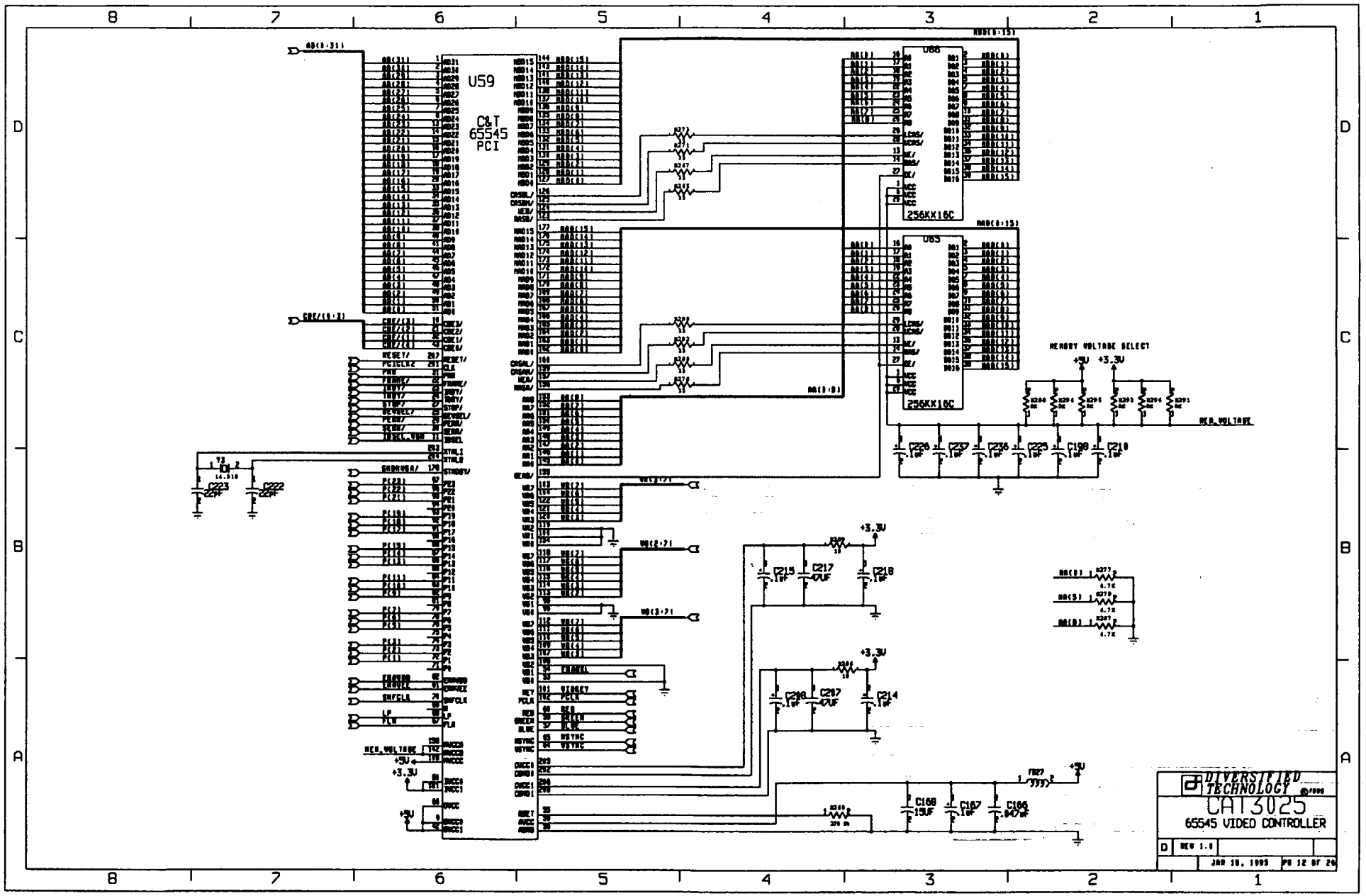
CAT3025

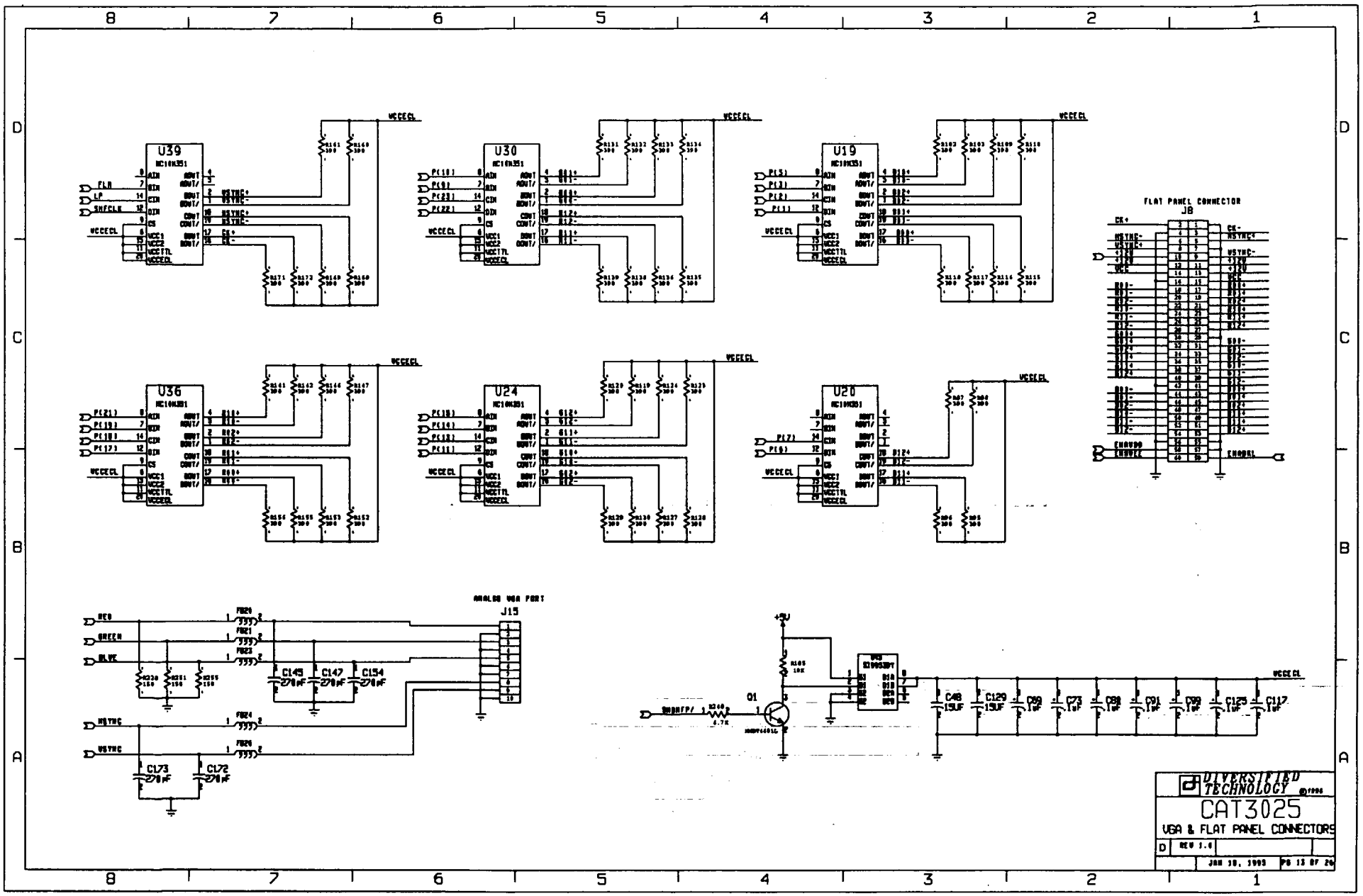
BIOS

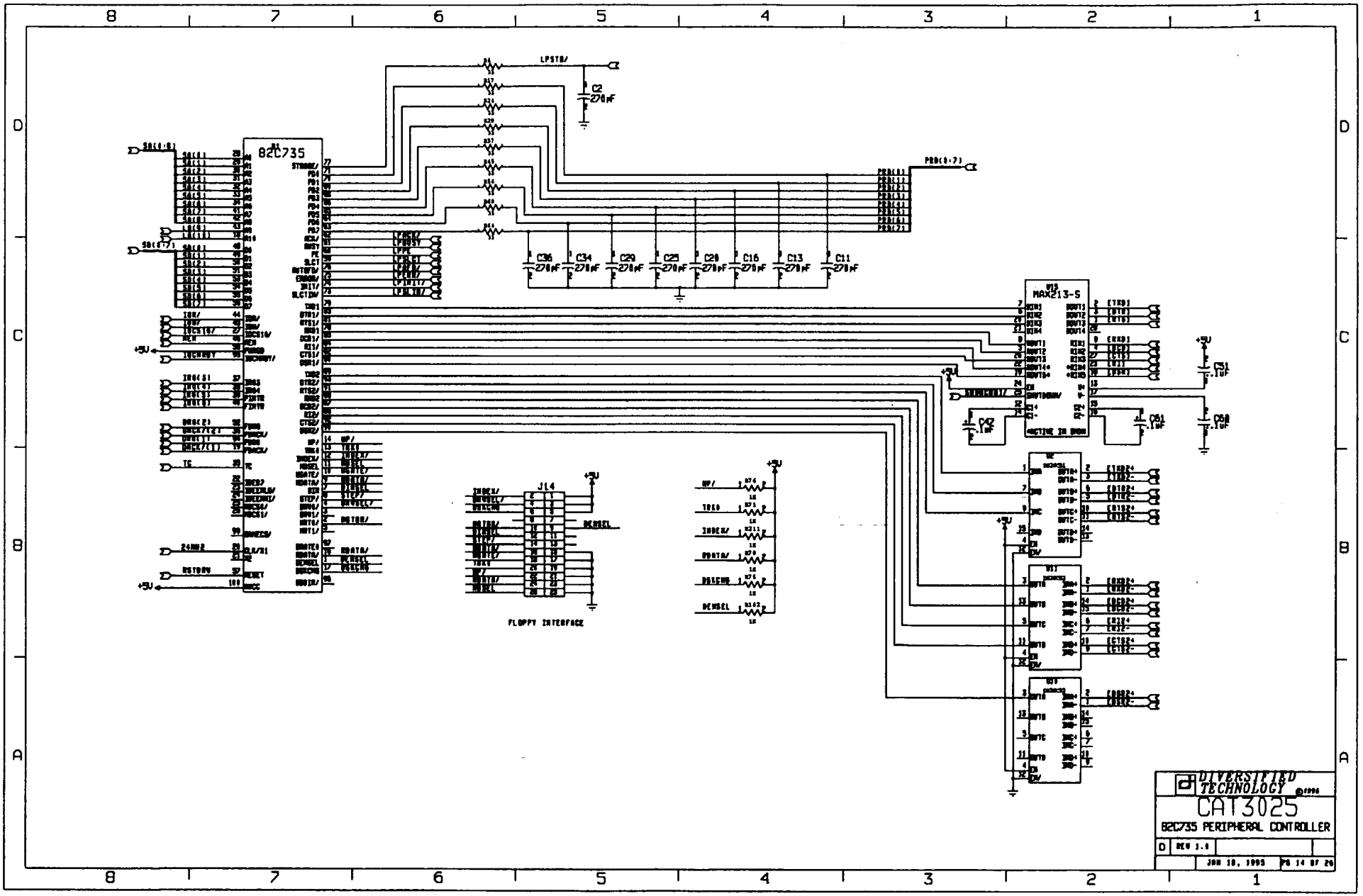
C	REV 1.0		
	JAN 18, 1995	PG 9 OF 26	

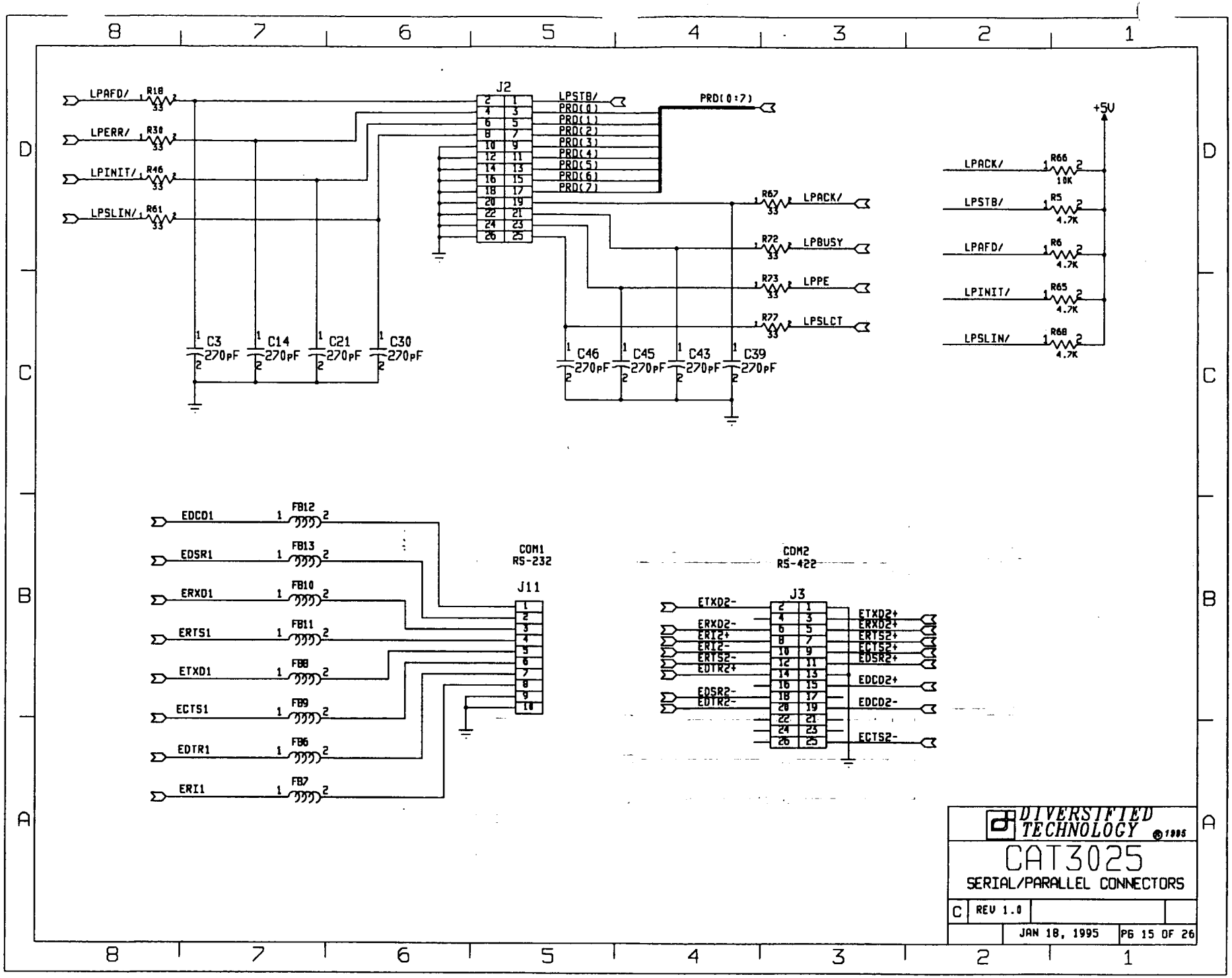

U44
82C621A
OPTI
IDE_D(15:0)
AD(31:0)
CBE/(3:0)
J17
+5V
R201 10K SDINTR
R217 10K IDE_INTR
R218 1K IDE_CHRDY
R227 1K IDE_CS16/
R241 IDE_A(2)
R233 IDE_A(1)
R236 IDE_A(0)
IDE_CHRDY
IDE_CS16/
R209 IDE_RST/
R226 IDE_RD/
R216 IDE_WR/
IDE_INTR
R237 IDE_CS3/
R245 IDE_CS1/
R199 SDCS51/ FIXED ADDRESS
R194 SDCS53/ NEW MODE
R234 INTEDGE/ EDGE IRQ
R254 IDE_CS3/ NO IOR FROM 3F7
R242 SROMEN/ DISABLE ROM
R200 SROMCS/ USER MODE
R193 SADLE PRIMARY IDE ONLY
E6 MODE 1 R204 IDE_A(1)
E7 MODE 0 R195 IDE_A(0)
E9 PREFETCH ENABLE R203 IDE_A(2) DISABLE
E8 SPEED 25 MHZ R196 IDE_CS1/ 33 MHZ
DIVERSIFIED TECHNOLOGY ©1995
CAT3025
IDE CONTROLLER
C REV 1.0 65110XXXX
JAN 18, 1995 PG 10 OF 26


TERMS WILL BE DISABLED AT RESET!
U37
AM79C974
AMD
U14
DS2105
U13
DS2105
U31
40 MHZ
OSC
U32
PE65424
U33
93C46
J9
J10
SCSITERM
SHDNSCSI/
SCSI_D(7:0)
AD(31:0)
CBE/(3:0)
DIVERSIFIED TECHNOLOGY ©1995
CAT3025
SCSI AND ETHERNET CONTROLLER
C
REV 1.0
65110XXXX
JAN 18, 1995
PG 11 OF 26


U59
C&T
65545
PCI
U66
U65
256KX16C
256KX16C
MEMORY VOLTAGE SELECT
+5V
+3.3V
MEM_VOLTAGE
DIVERSIFIED TECHNOLOGY
CAT3025
65545 VIDEO CONTROLLER
D
REV 1.0
JAN 19, 1995


U39
U30
U19
U36
U24
U20
FLAT PANEL CONNECTOR
J8
ANALOG VGA PORT
J15
Q1
VCCECL
DIVERSIFIED TECHNOLOGY
CAT3025
VGA & FLAT PANEL CONNECTORS
REV 1.0
JAN 10, 1995


82C735
MAX213-S
J14
FLOPPY INTERFACE
DIVERSIFIED TECHNOLOGY
CAT3025
82C735 PERIPHERAL CONTROLLER
REV 1.0
JAN 10, 1995



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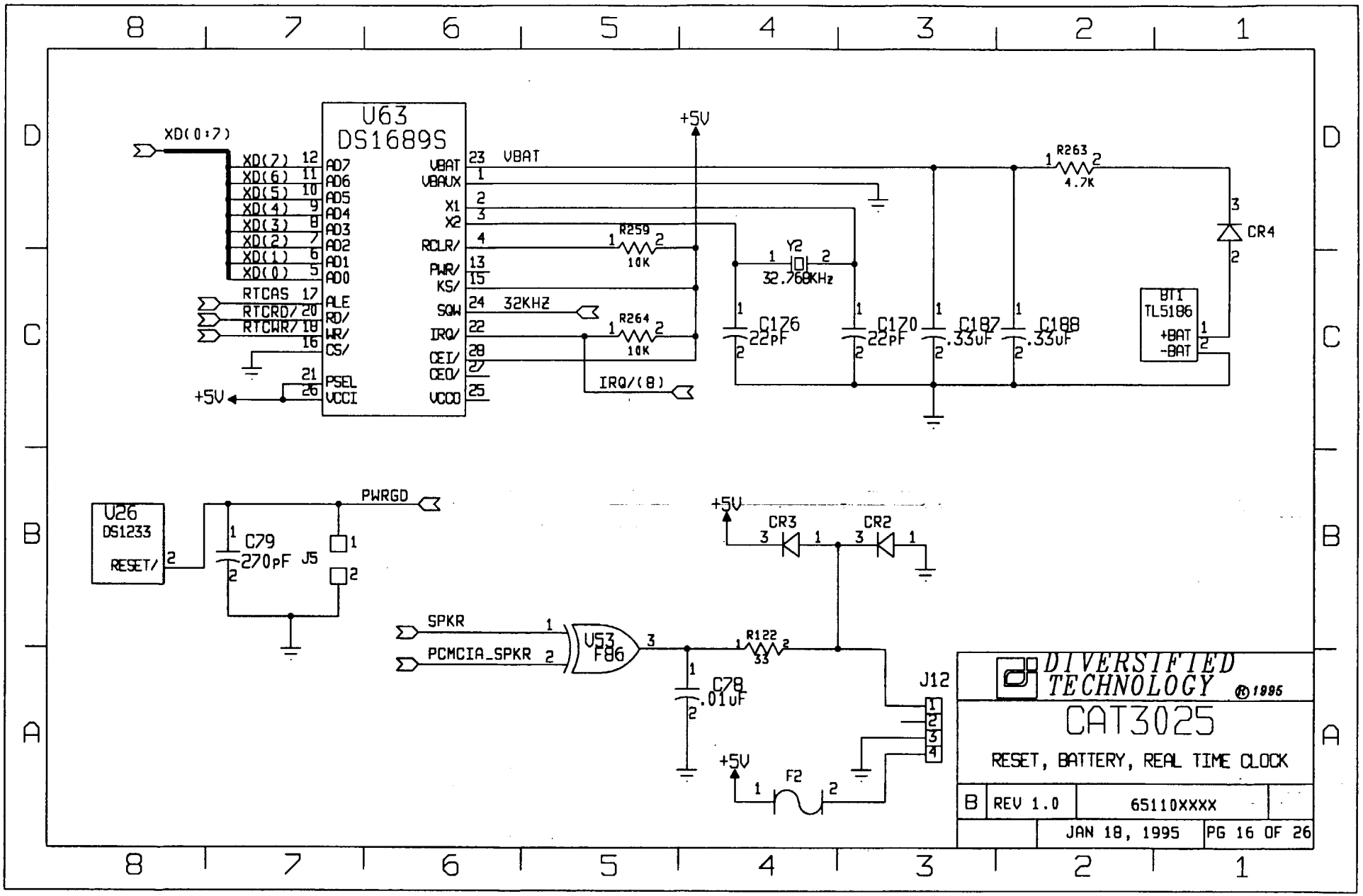
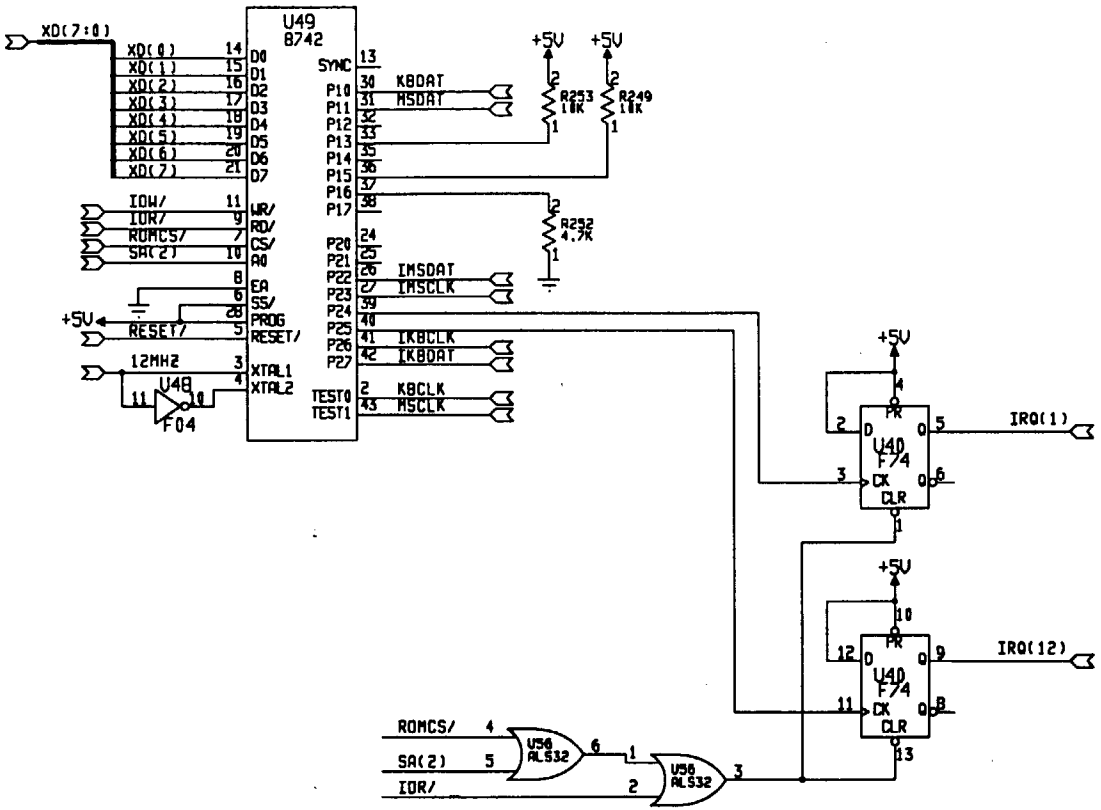
SERIAL/PARALLEL CONNECTORS

C	REV 1.0		
	JAN 18, 1995	PG 15 OF 26	


U63
DS1689S
XD(0:7)
XD(7) 12 AD7
XD(6) 11 AD6
XD(5) 10 AD5
XD(4) 9 AD4
XD(3) 8 AD3
XD(2) 7 AD2
XD(1) 6 AD1
XD(0) 5 AD0
RTCAS 17 ALE
RTCRD/ 20 RD/
RTCWR/ 18 WR/
16 CS/
21 PSEL
26 VCCI
+5V
VBAT 23
VBAUX 1
X1 2
X2 3
RCLR/ 4
PWR/ 13
KS/ 15
SQW 24
IRQ/ 22
CEI/ 28
CEO/ 2
VCCO 25
VBAT
32KHZ
IRQ/(8)
R259 10K
R264 10K
Y2 32.768KHz
C176 22pF
C170 22pF
C187 .33uF
C188 .33uF
R263 4.7K
CR4
BT1 TL5186 +BAT -BAT
U26 DS1233 RESET/
C79 270pF
J5
PWRGD
CR3
CR2
SPKR
PCMCIA_SPKR
U53 F86
R122 33
C78 .01uF
J12
F2
DIVERSIFIED TECHNOLOGY ©1995
CAT3025
RESET, BATTERY, REAL TIME CLOCK
B REV 1.0 65110XXXX
JAN 18, 1995 PG 16 OF 26



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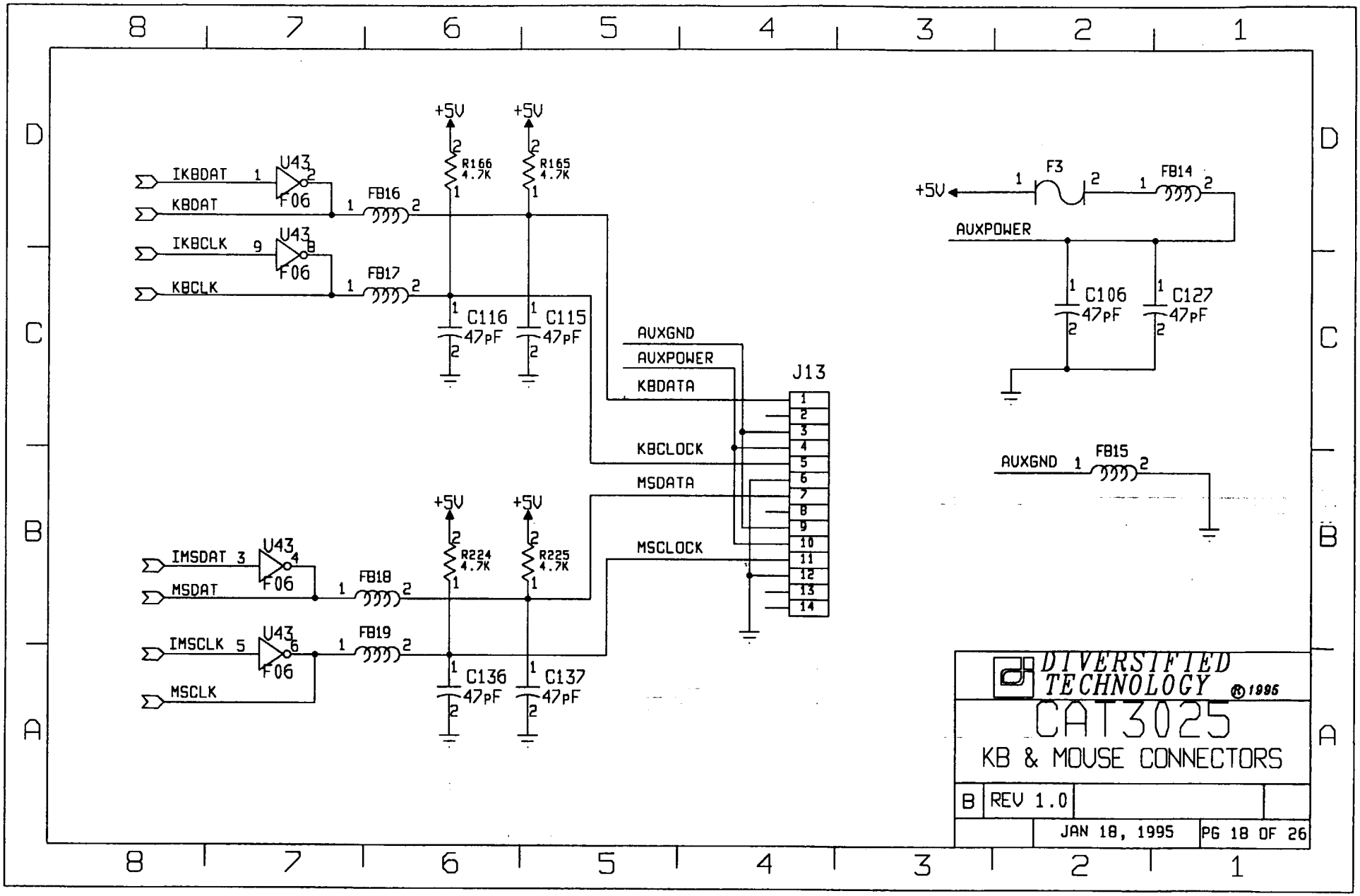
CAT3025
KEYBOARD

C	REV 1.0		
	JAN 18, 1995	PG 17 OF 26	


IKBDAT
KBDAT
IKBCLK
KBCLK
U43
F06
FB16
FB17
+5V
R166 4.7K
R165 4.7K
C116 47pF
C115 47pF
AUXGND
AUXPOWER
KBDATA
KBCLOCK
MSDATA
MSCLOCK
J13
IMSDAT
MSDAT
IMSCLK
MSCLK
FB18
FB19
R224 4.7K
R225 4.7K
C136 47pF
C137 47pF
F3
FB14
C106 47pF
C127 47pF
FB15
DIVERSIFIED TECHNOLOGY ©1995
CAT3025
KB & MOUSE CONNECTORS
B
REV 1.0
JAN 18, 1995
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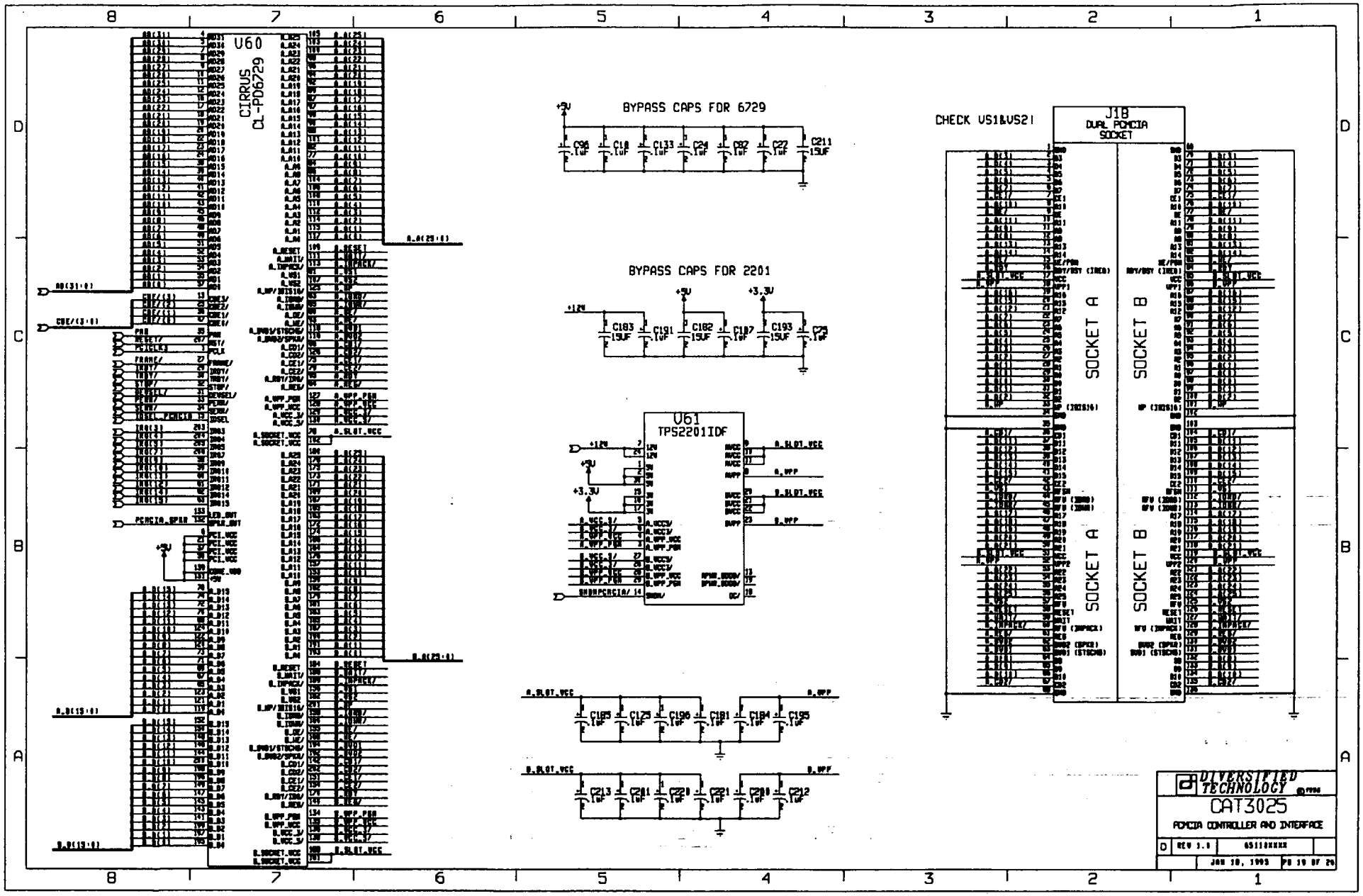
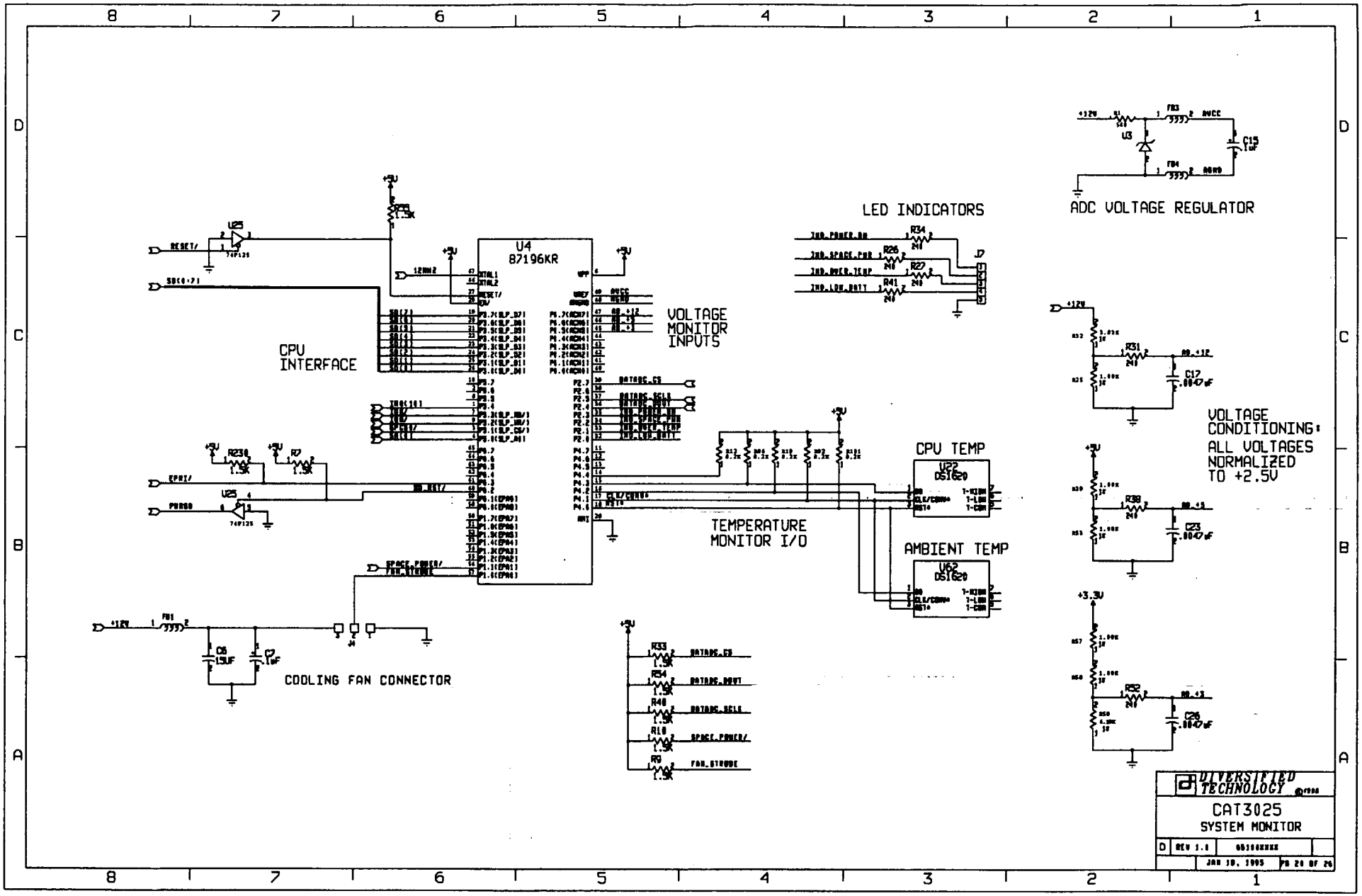
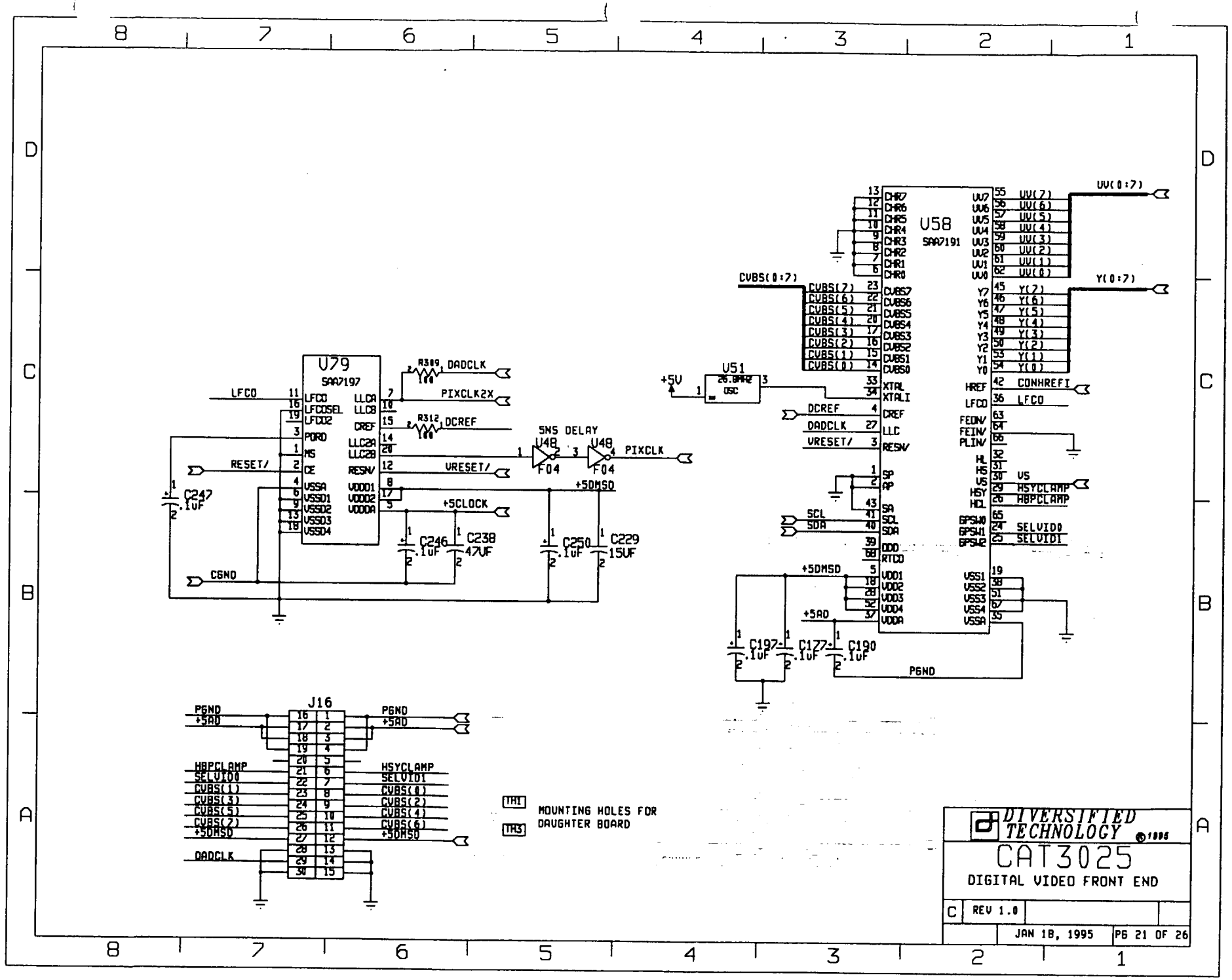

V60
CIRRUS
CL-PD6729
BYPASS CAPS FOR 6729
BYPASS CAPS FOR 2201
V61
TPS2201IDF
CHECK VS1&VS2!
J18
DUAL PCMCIA
SOCKET
SOCKET A
SOCKET B
SOCKET A
SOCKET B
DIVERSIFIED
TECHNOLOGY
CAT3025
PCMCIA CONTROLLER AND INTERFACE
REV 1.0
JAN 10, 1995


U4
87196KR
CPU
INTERFACE
VOLTAGE
MONITOR
INPUTS
LED INDICATORS
ADC VOLTAGE REGULATOR
CPU TEMP
AMBIENT TEMP
TEMPERATURE
MONITOR I/O
COOLING FAN CONNECTOR
VOLTAGE
CONDITIONING:
ALL VOLTAGES
NORMALIZED
TO +2.5V
DIVERSIFIED
TECHNOLOGY
CAT3025
SYSTEM MONITOR
REV 1.0
JAN 10, 1995


U79
SAA7197
LFCO
RESET/
CGND
R309 DADCLK
PIXCLK2X
R312 DCREF
VRESET/
+5CLOCK
5NS DELAY
U48
F04
PIXCLK
+5DMSD
C247 .1uF
C246 .1uF
C238 47UF
C250 .1uF
C229 15UF
U58
SAA7191
CVBS(0:7)
U51
26.8MHz
OSC
+5V
XTAL
XTALI
DCREF
DADCLK
VRESET/
SCL
SDA
+5AD
C197 .1uF
C127 .1uF
C190 .1uF
PGND
UV(0:7)
Y(0:7)
CONHREFI
LFCO
VS
HSYCLAMP
HBPCLAMP
SELVID0
SELVID1
J16
PGND
+5AD
HBPCLAMP
SELVID0
CVBS(1)
CVBS(3)
CVBS(5)
CVBS(7)
+5DMSD
DADCLK
HSYCLAMP
SELVID1
CVBS(0)
CVBS(2)
CVBS(4)
CVBS(6)
+5DMSD
TH1
TH3
MOUNTING HOLES FOR
DAUGHTER BOARD
DIVERSIFIED TECHNOLOGY ©1995
CAT3025
DIGITAL VIDEO FRONT END
C
REV 1.0
JAN 18, 1995
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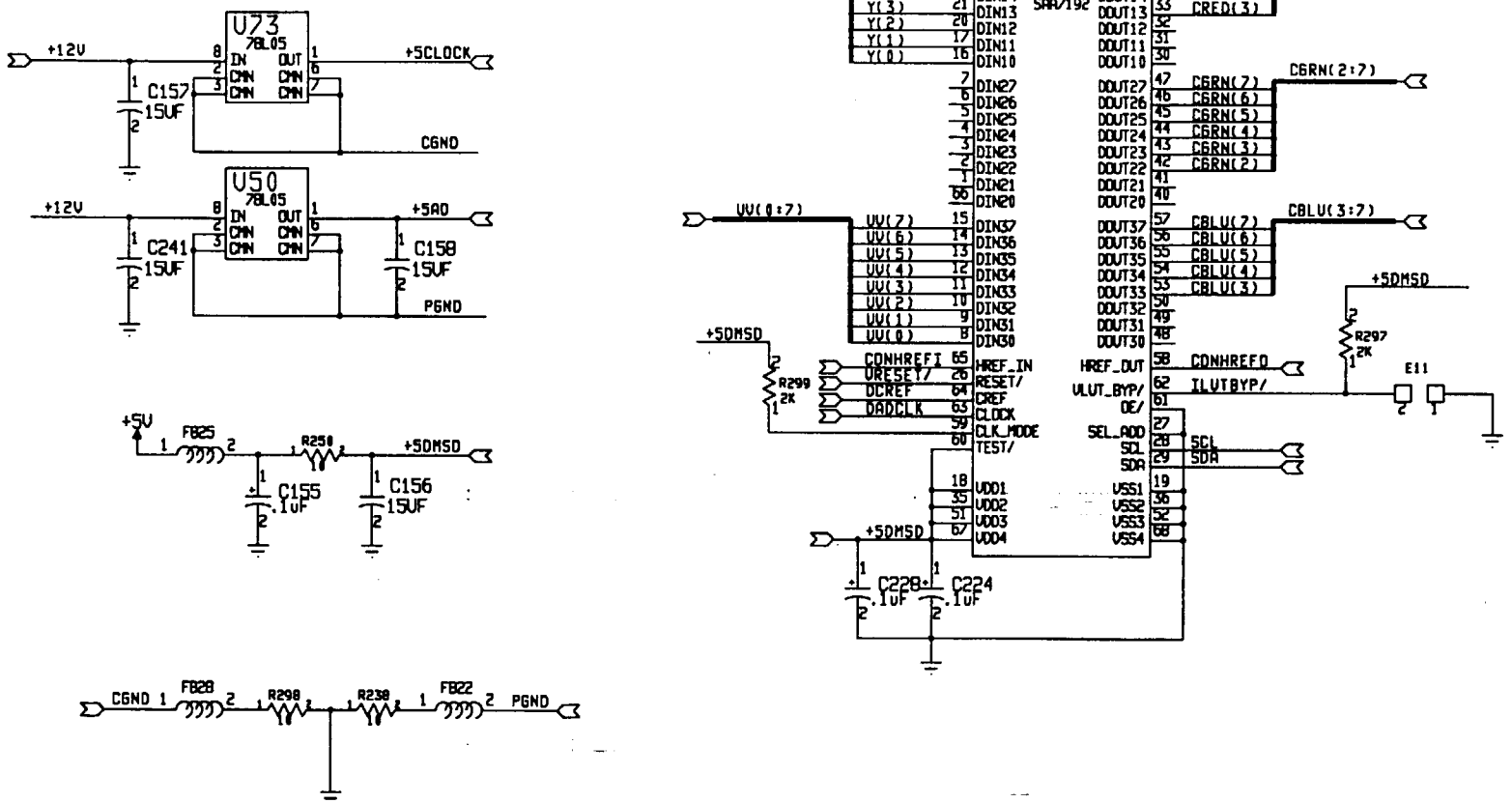

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YUV TO RGB CONVERTER

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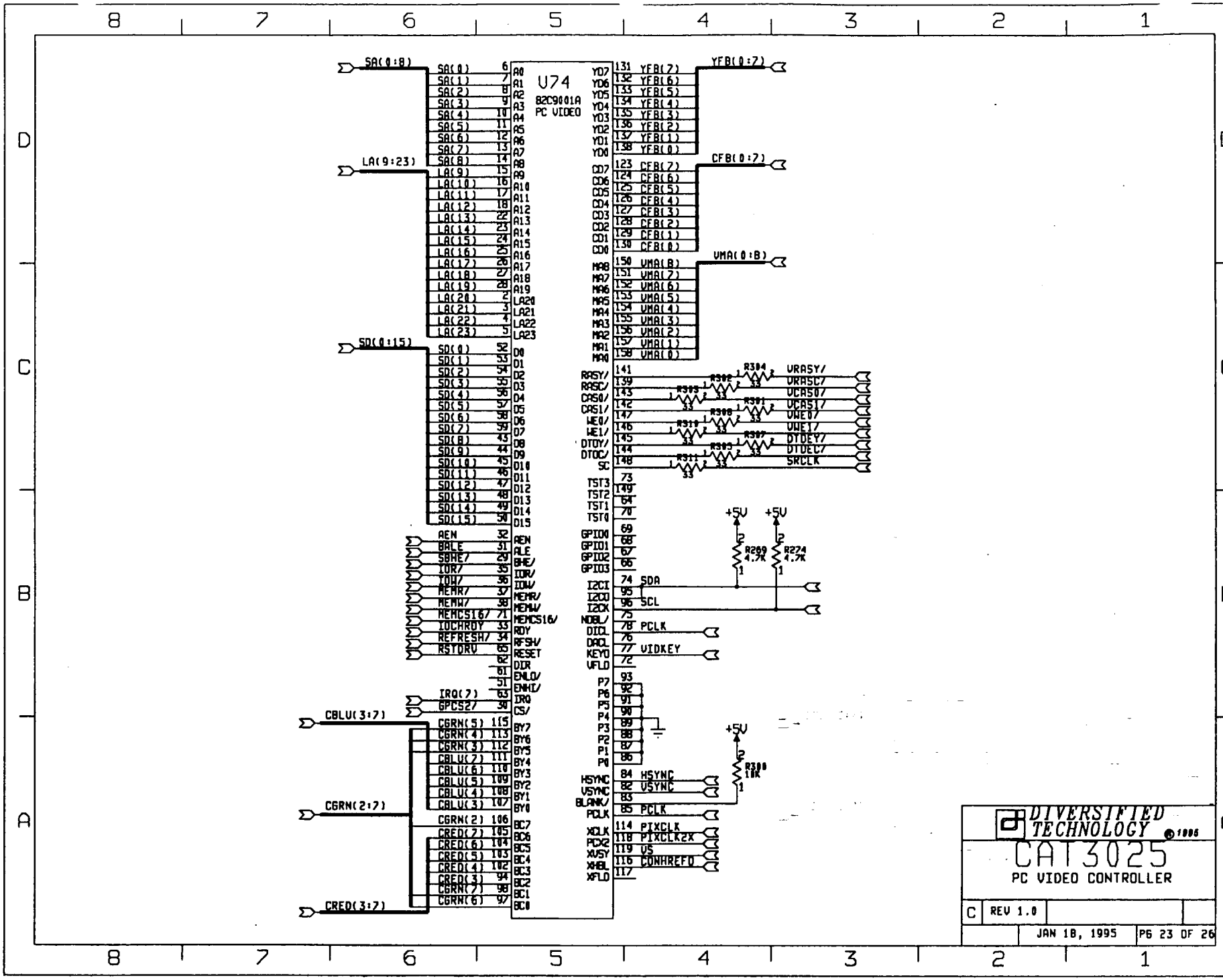
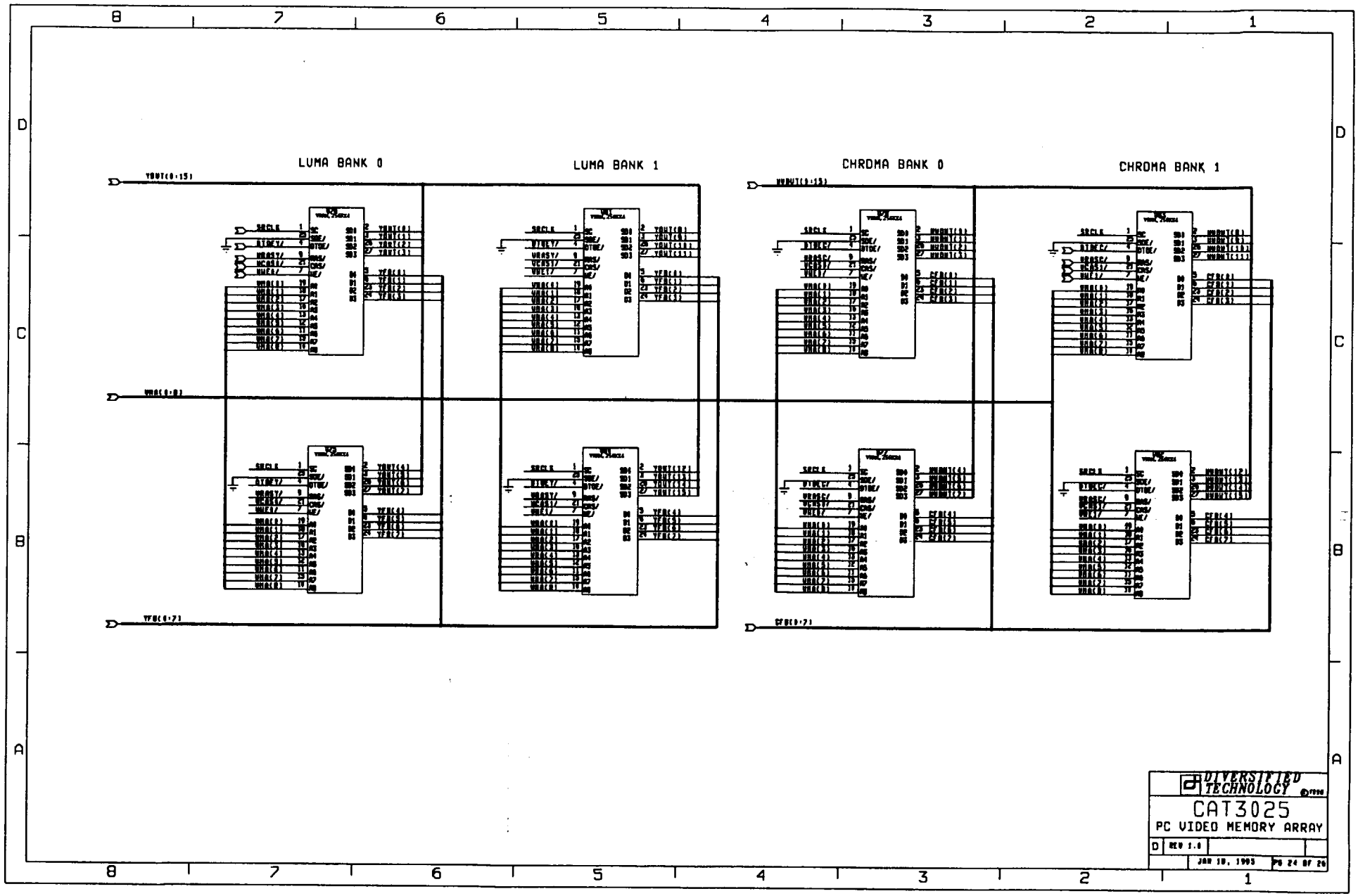
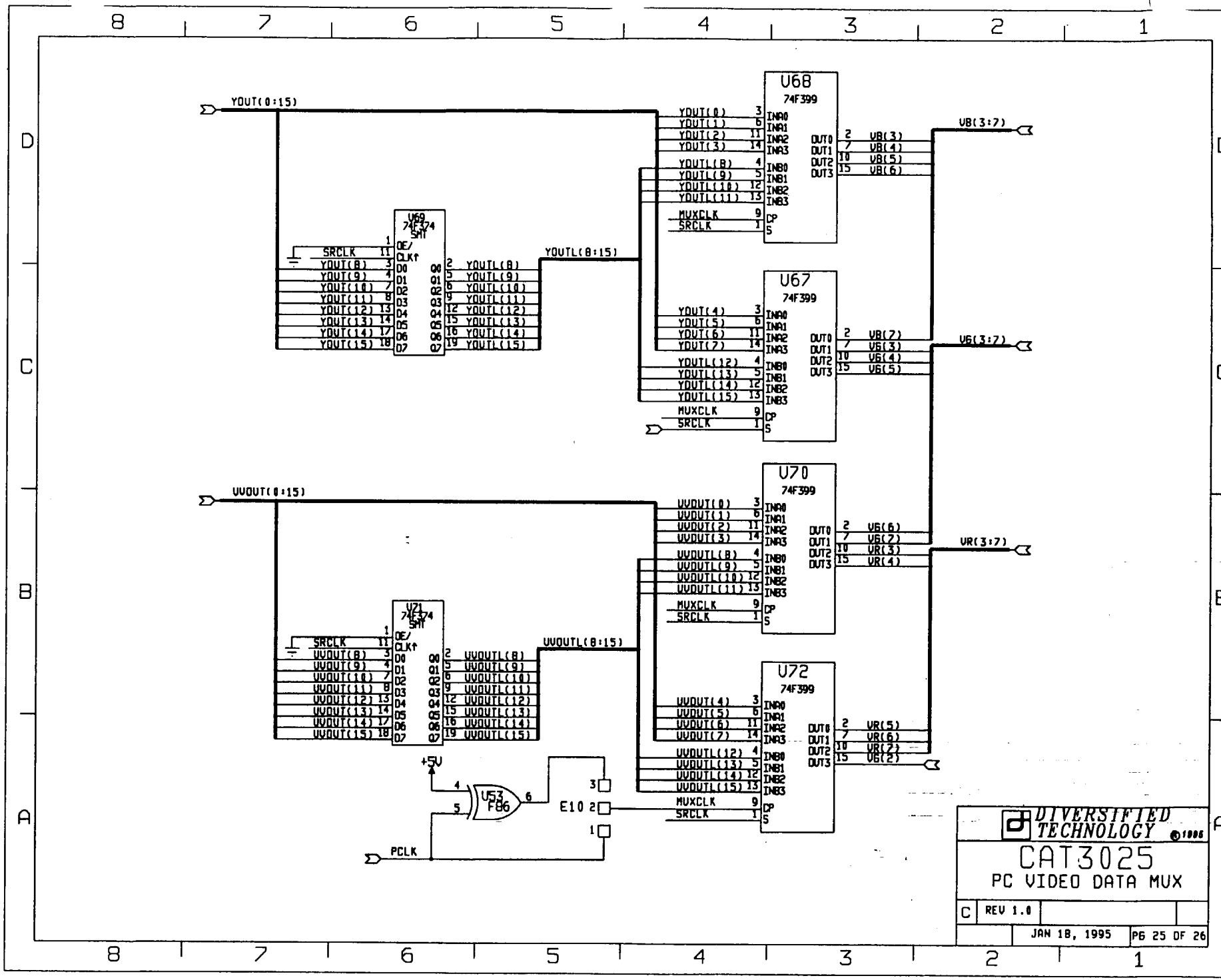

U74
82C9001A
PC VIDEO
SA(0:8)
LA(9:23)
SD(0:15)
CBLU(3:7)
CGRN(2:7)
CRED(3:7)
YFB(0:7)
CFB(0:7)
VMA(0:8)
SDA
SCL
PCLK
VIDKEY
HSYNC
VSYNC
PIXCLK
PIXCLK2X
VS
CONHREFD
+5V
R304
R302
R303
R301
R308
R310
R307
R305
R311
R269 4.7K
R274 4.7K
R300 10K
VRASY/
VRASC7
VCAS07
VCAS17
VWE07
VWE17
DTDEY7
DTDEC7
SRCLK
DIVERSIFIED TECHNOLOGY ©1995
CAT3025
PC VIDEO CONTROLLER
C
REV 1.0
JAN 18, 1995
PG 23 OF 26


LUMA BANK 0
LUMA BANK 1
CHROMA BANK 0
CHROMA BANK 1
DIVERSIFIED TECHNOLOGY
CAT3025
PC VIDEO MEMORY ARRAY
D
REV 1.0
JAN 19, 1993
SHEET 24 OF 26


YOUT(0:15)
YOUTL(8:15)
U68
74F399
U67
74F399
VB(3:7)
VG(3:7)
U69
74F374
SMT
SRCLK
MUXCLK
UVOUT(0:15)
UVOUTL(8:15)
U70
74F399
U72
74F399
VR(3:7)
U71
74F374
SMT
+5V
U53
F86
E10
PCLK
DIVERSIFIED TECHNOLOGY ©1995
CAT3025
PC VIDEO DATA MUX
C
REV 1.0
JAN 18, 1995
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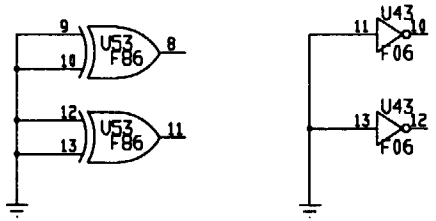

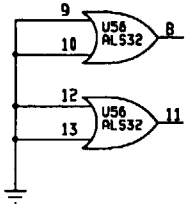

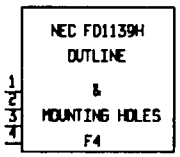

TOOLING HOLE

TH2

MOUNTING HOLES

M3 M6
M7 M1
M4 M2
M5 M8

M9 NO PLATE

FIDUCIALS

FD1 FD3
FD5 FD6
FD4 FD2

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UNUSED GATES & MISC

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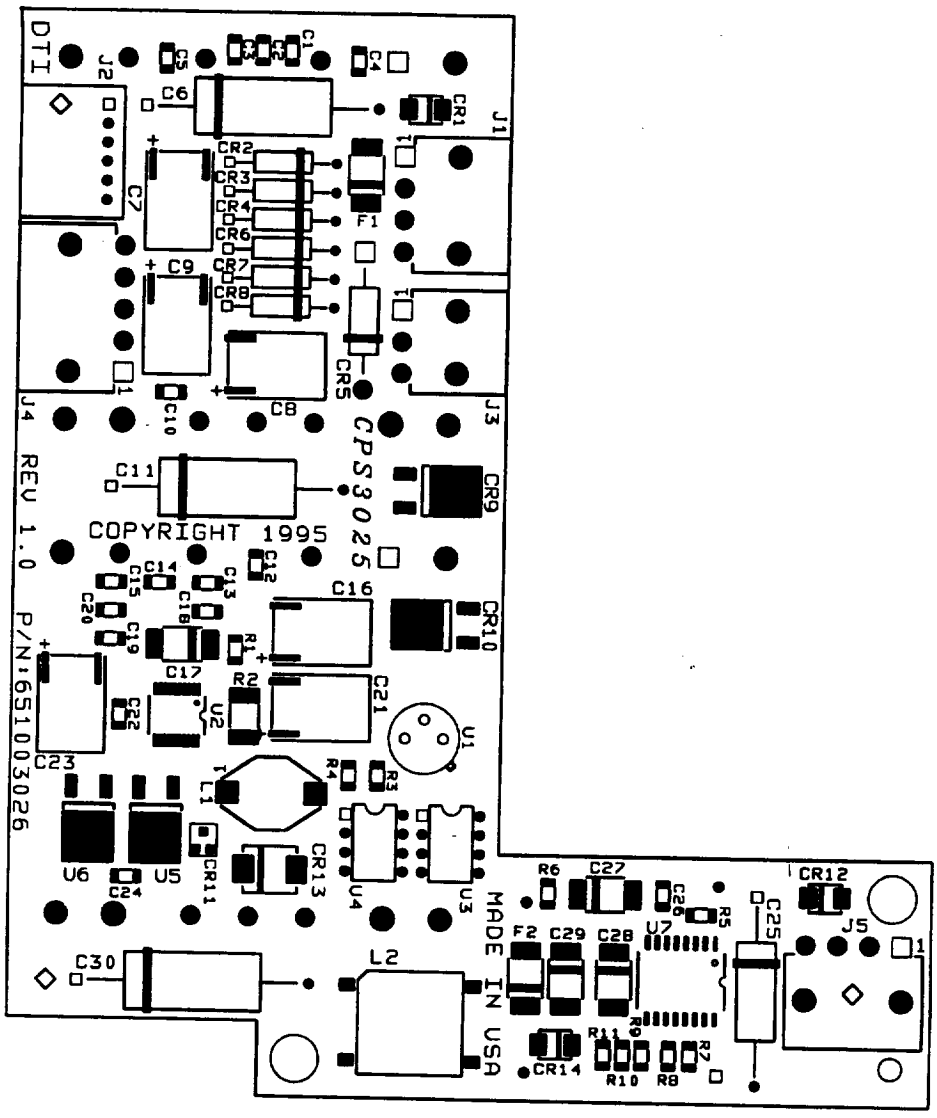
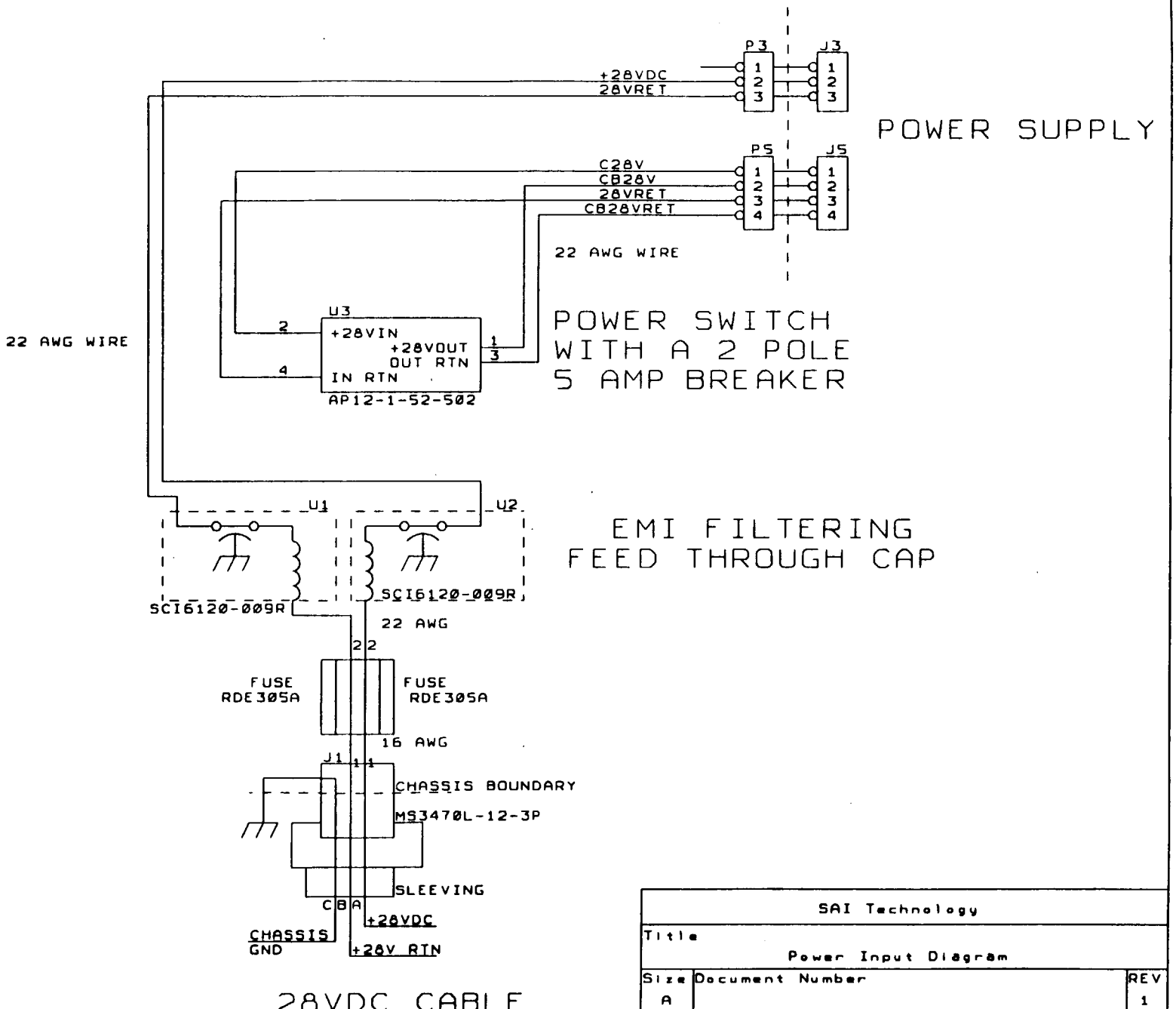
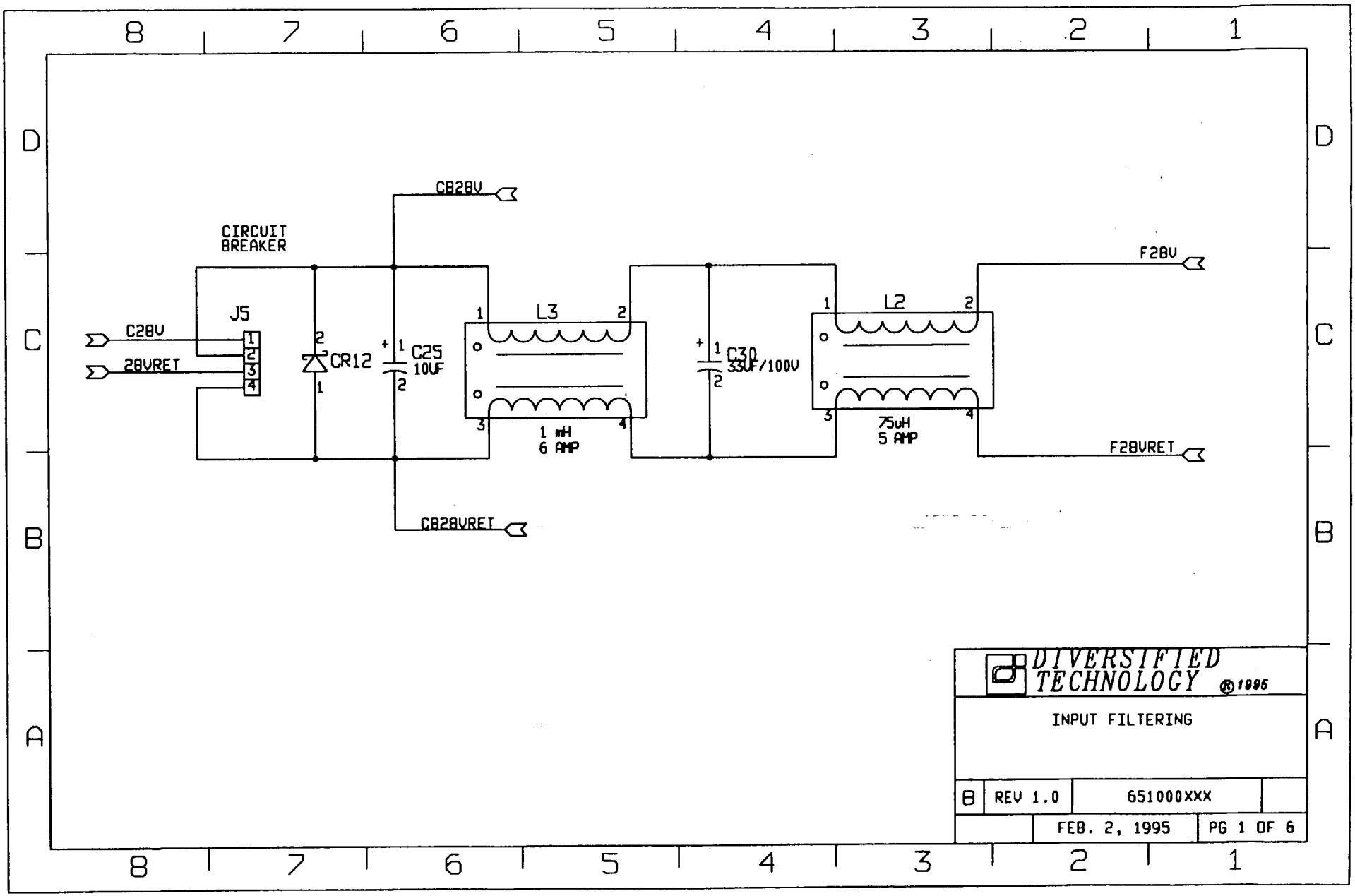
Power Supply Schematic

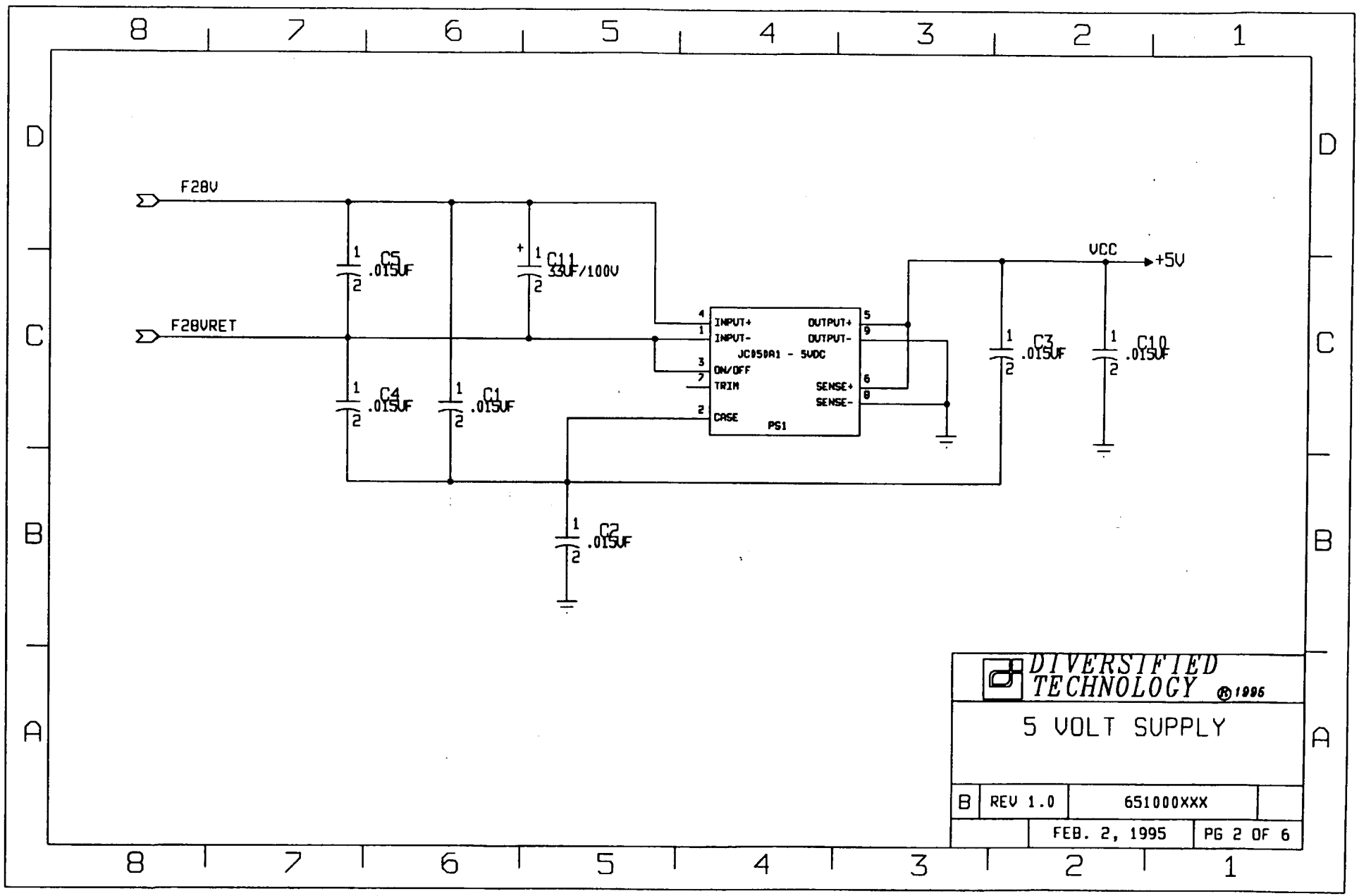


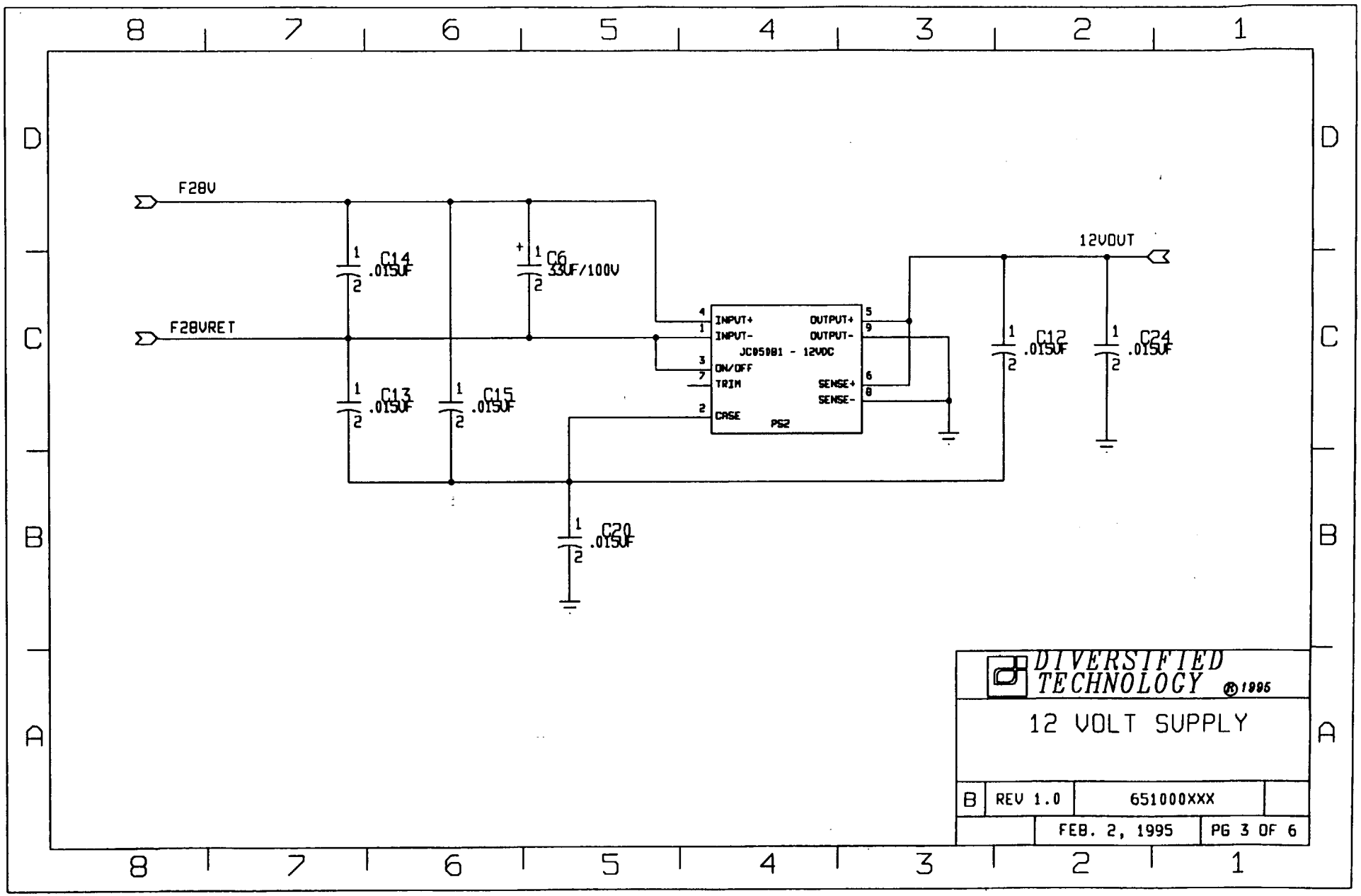
POWER SUPPLY PWA BOARD LAYOUT



SAI Technology		
Title: Power Input Diagram		
Size: A	Document Number:	REV: 1
Date: February 13, 1995	Sheet: 1 of 1	


CB28V
CIRCUIT
BREAKER
J5
C28V
28VRET
CR12
C25
10UF
L3
1 mH
6 AMP
C30
33UF/100V
L2
75uH
5 AMP
F28V
F28VRET
CB28VRET
DIVERSIFIED
TECHNOLOGY
©1995
INPUT FILTERING
B
REV 1.0
651000XXX
FEB. 2, 1995
PG 1 OF 6


F28V
F28VRET
C5
.015UF
C11
33UF/100V
C4
.015UF
C1
.015UF
C2
.015UF
C3
.015UF
C10
.015UF
INPUT+
INPUT-
ON/OFF
TRIM
CASE
OUTPUT+
OUTPUT-
SENSE+
SENSE-
JC050A1 - 5VDC
PS1
VCC
+5V
DIVERSIFIED TECHNOLOGY ®1996
5 VOLT SUPPLY
B
REV 1.0
651000XXX
FEB. 2, 1995
PG 2 OF 6


F28V
F28VRET
C14
.015UF
C6
33UF/100V
C13
.015UF
C15
.015UF
C20
.015UF
INPUT+
INPUT-
ON/OFF
TRIM
CASE
OUTPUT+
OUTPUT-
SENSE+
SENSE-
JC05081 - 12VDC
PS2
12VOUT
C12
.015UF
C24
.015UF
DIVERSIFIED TECHNOLOGY ®1995
12 VOLT SUPPLY
B
REV 1.0
651000XXX
FEB. 2, 1995
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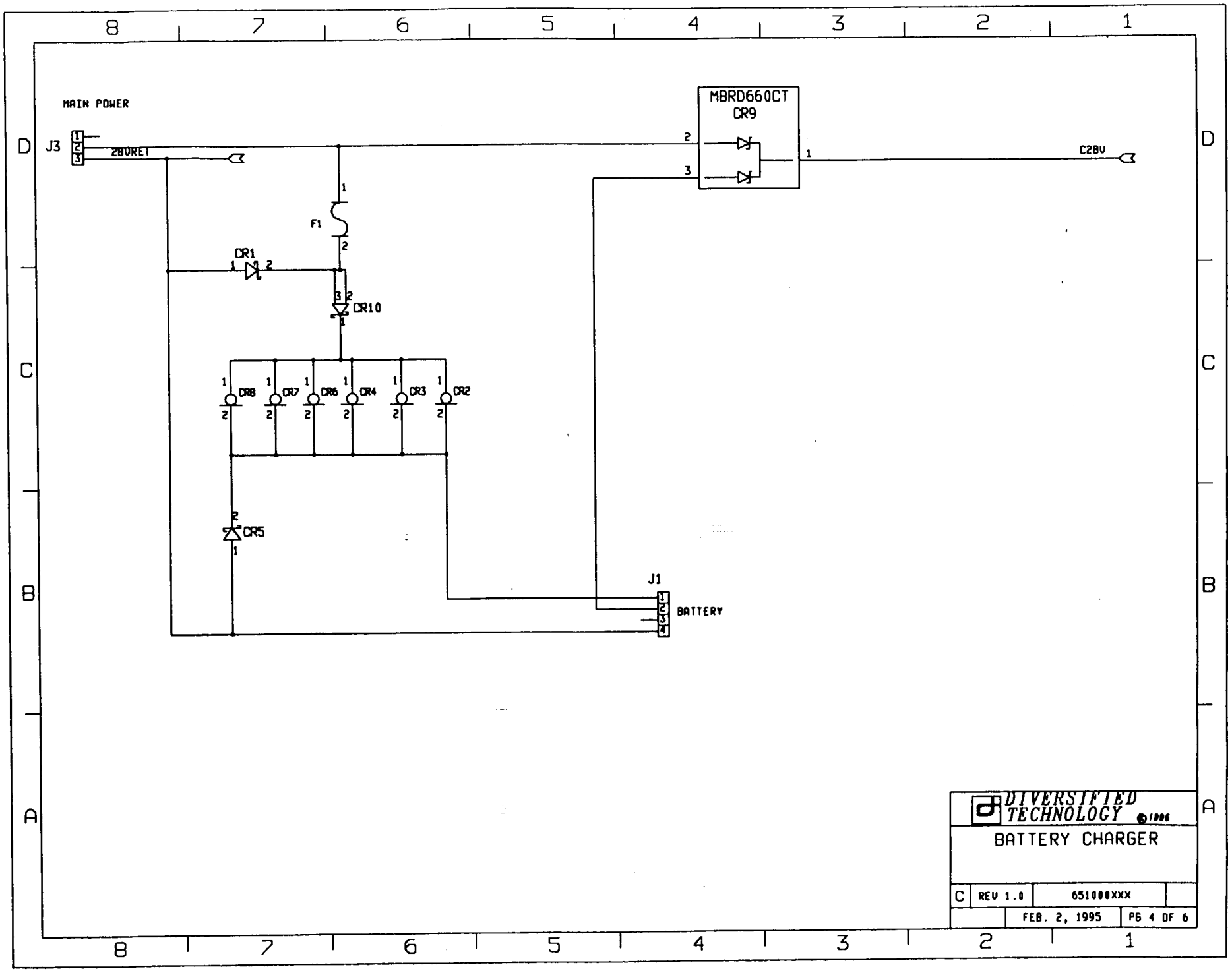
MAIN POWER
J3
28VRET
MBRD660CT
CR9
C28V
F1
CR1
CR10
CR8
CR7
CR6
CR4
CR3
CR2
CR5
J1
BATTERY
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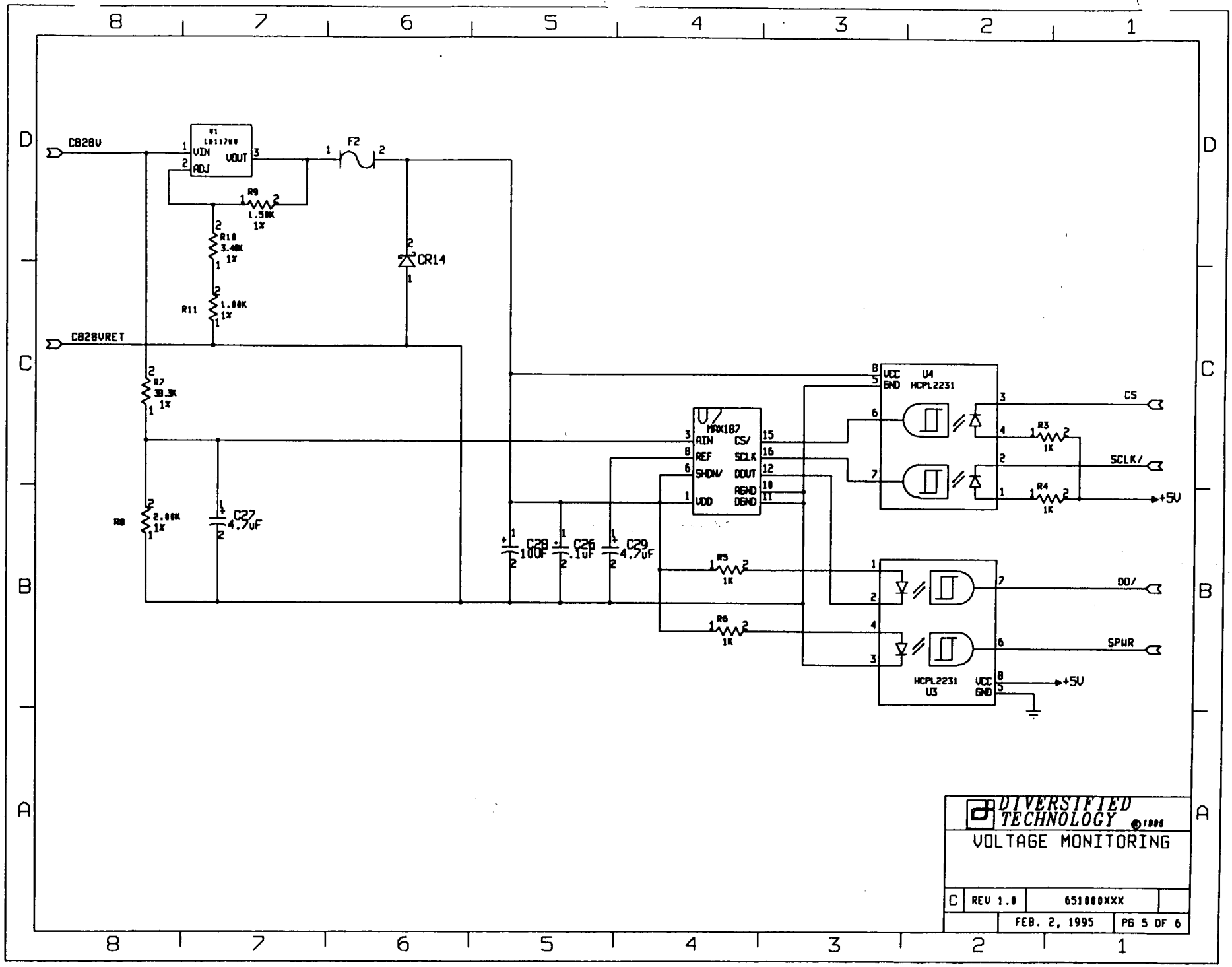
BATTERY CHARGER
C
REV 1.0
651000XXX
FEB. 2, 1995
PG 4 OF 6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CB28VRET
U1
LM117MV
VIN
VOUT
ADJ
F2
R9
1.50K
1%
R10
3.40K
1%
R11
1.00K
1%
CR14
R7
30.1K
1%
R8
2.00K
1%
C27
4.7uF
U7
MAX187
AIN
REF
SHDN/
VDD
CS/
SCLK
DOUT
AGND
DGND
C28
100F
C26
.1uF
C29
4.7uF
U4
VCC
GND
HCPL2231
R3
1K
R4
1K
R5
1K
R6
1K
CS
SCLK/
DO/
SPWR
+5V
U3
HCPL2231
VCC
GND
+5V
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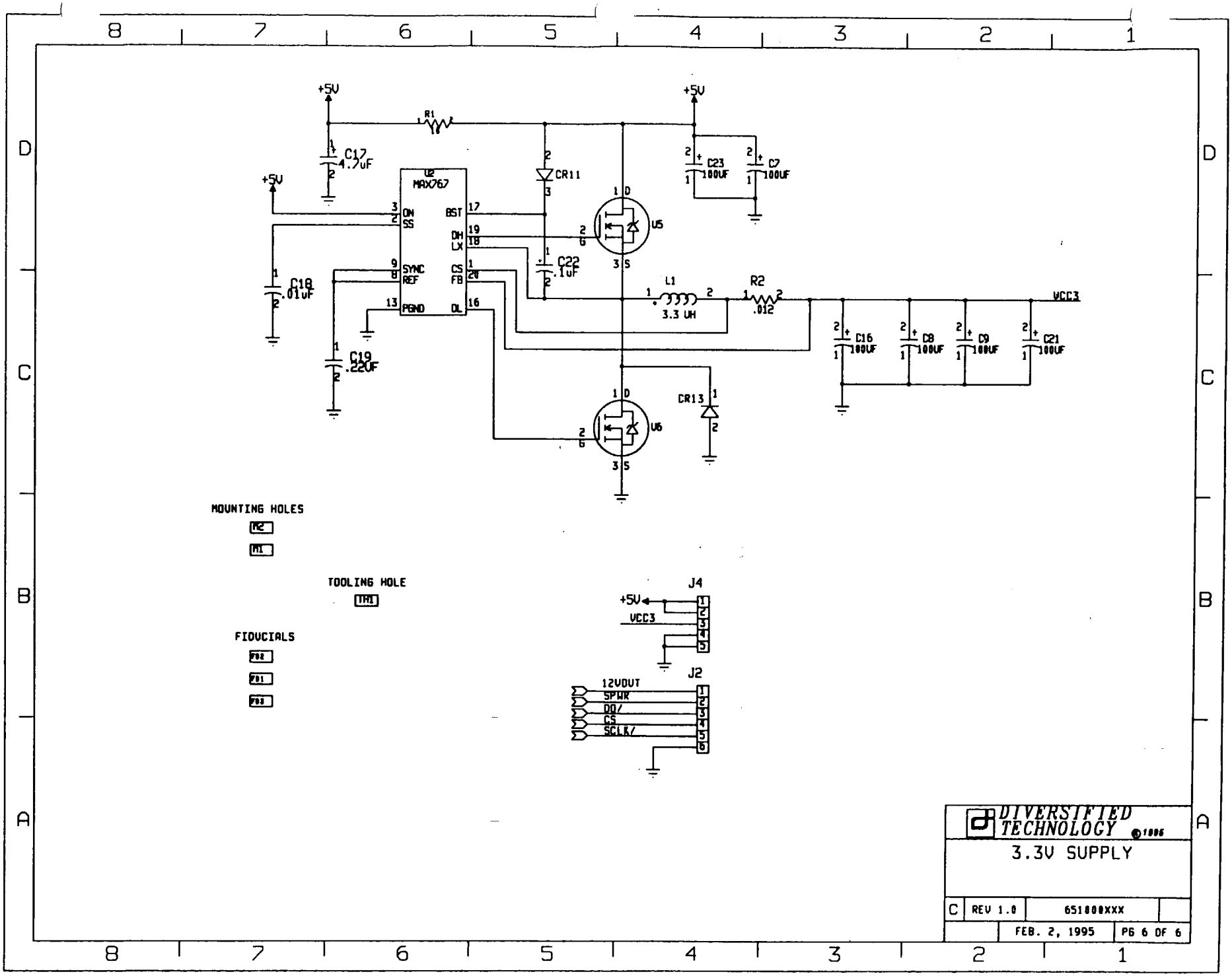
VOLTAGE MONITORING
C
REV 1.0
651000XXX
FEB. 2, 1995
PG 5 OF 6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R1
C17
4.7uF
U2
MAX767
ON
SS
SYNC
REF
PGND
BST
DH
LX
CS
FB
DL
CR11
U5
C22
.1uF
C18
.01uF
C19
.22uF
L1
3.3 UH
R2
.012
VCC3
C16
100UF
C8
100UF
C9
100UF
C21
100UF
C23
100UF
C7
100UF
CR13
U6
MOUNTING HOLES
M2
M1
TOOLING HOLE
TH1
FIDUCIALS
FID2
FID1
FID3
J4
+5V
VCC3
J2
12VOUT
SPWR
DO/
CS
SCLK/
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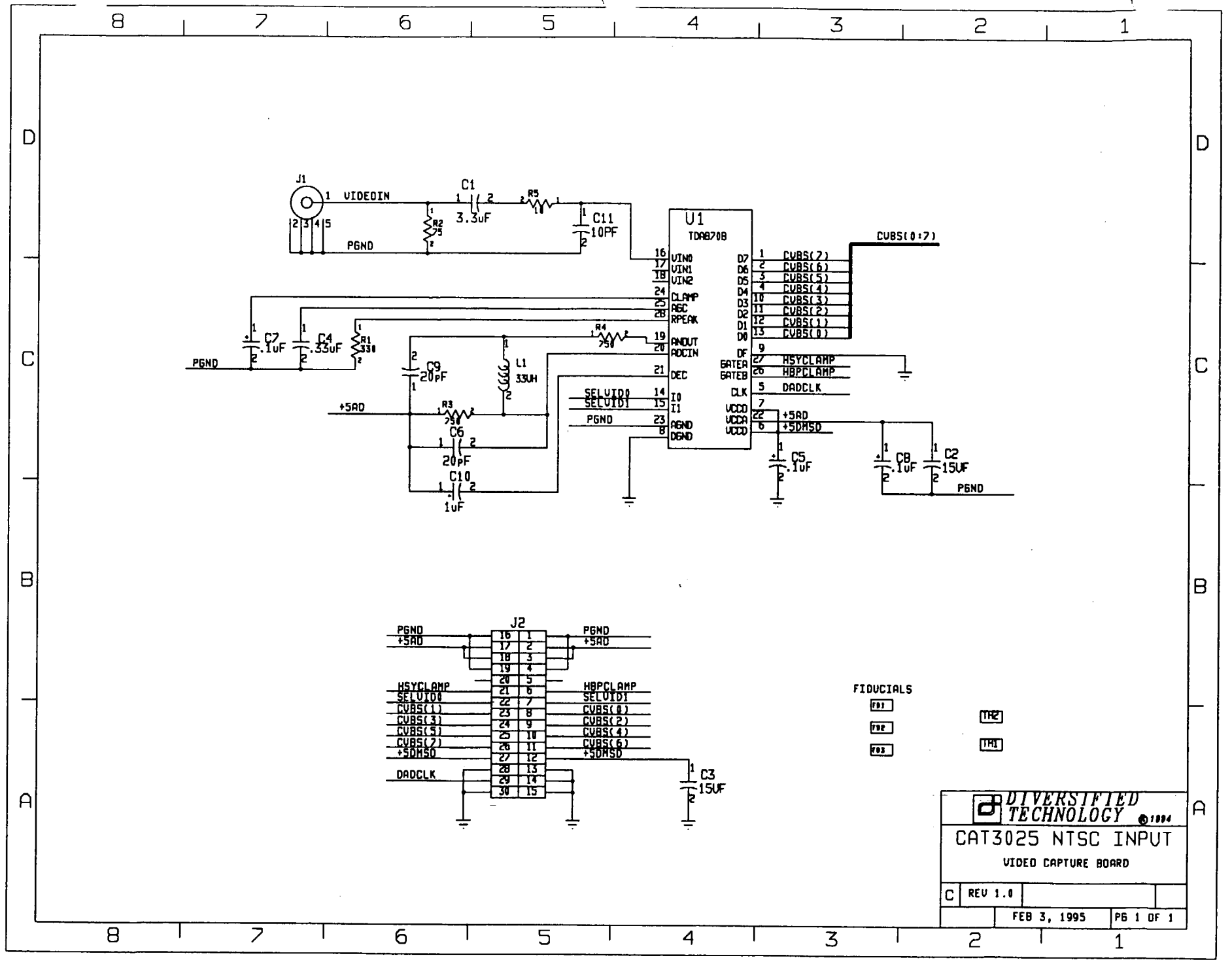
3.3V SUPPLY
C
REV 1.0
651000XXX
FEB. 2, 1995
PG 6 OF 6

NTSC Video Schematic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VIDEOIN
PGND
C1
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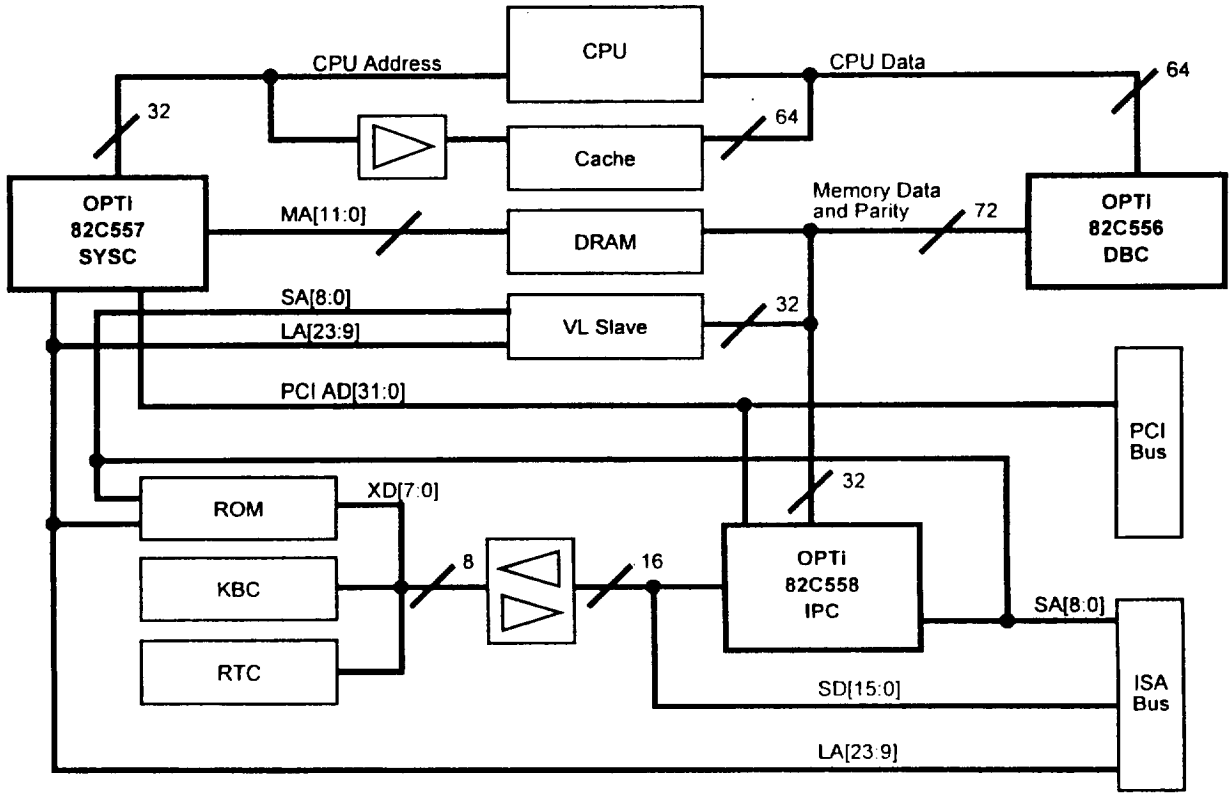
R2
75
R5
C11
10PF
U1
TDA8708
VIN0
VIN1
VIN2
CLAMP
AGC
RPEAK
ANOUT
ADCIN
DEC
I0
I1
AGND
DGND
D7
D6
D5
D4
D3
D2
D1
D0
DF
GATEA
GATEB
CLK
VCCD
VCCA
VCCD
CVBS(0:7)
CVBS(7)
CVBS(6)
CVBS(5)
CVBS(4)
CVBS(3)
CVBS(2)
CVBS(1)
CVBS(0)
HSYCLAMP
HBPCLAMP
DADCLK
+5AD
+5DMSD
C7
.1uF
C4
.33uF
R1
330
C9
20pF
L1
33UH
R4
50
R3
50
C6
20pF
C10
1uF
SELVID0
SELVID1
C5
.1uF
C8
.1uF
C2
15UF
J2
C3
15UF
FIDUCIALS
FID1
FID2
FID3
TM2
TM1
DIVERSIFIED TECHNOLOGY ©1994
CAT3025 NTSC INPUT
VIDEO CAPTURE BOARD
C
REV 1.0
FEB 3, 1995
PG 1 OF 1

OPTi Desktop Chipset Data Sheet

1.0 Features

- 100% PC/AT® compatible
- Fully supports Intel's 3.3V Pentium™ Processor and dual processor configuration at 50, 60, and 66.667MHz
- Supports P55C™, K5™, and M1™ processors
- Supports the Cyrix® M1 Processor linear burst mode
- Three chip solution:
  - 82C556 DBC (160-pin PQFP)
  - 82C557 SYSC (208-pin PQFP or TQFP)
  - 82C558 IPC (208-pin PQFP or TQFP)
- Includes a fully integrated 82C206 with external real-time clock (RTC) interface
- Supports CPU address pipelining
- Interfaces the CPU and standard buses to both Peripheral Component Interconnect (PCI) and VESA local bus operating in synchronous/asynchronous modes, with VESA bus always operating at PCI bus operating frequency
- Supports three PCI masters, one VESA slave, and six ISA slots
- Supports PCI pre-snoop for PCI masters
- PCI byte/word merge support for CPU accesses to PCI bus, and support for PCI pre-fetch
- Burst mode PCI accesses to local memory supported
- Write-back/write-through, direct-mapped cache with size selections: 64KB, 128KB, 256KB, 1MB and 2MB
- Support for synchronous and asynchronous SRAMs, pipelined synchronous SRAMs, and Intel Standard BSRAMs
- Support for the Sony SONIC-2WP™ Cache Module
- Programmable cache write policy:
  - Write-back
  - Write-through
  - Adaptive write-back
- Built-in tag auto-invalidation circuitry
- Fully programmable 3-2-2-2 cache burst read/write cycles. 2-1-1-1 burst read/write support at 50MHz
- Support for two programmable non-cacheable memory regions

Figure 1-1 System Block Diagram



Features (Cont.)

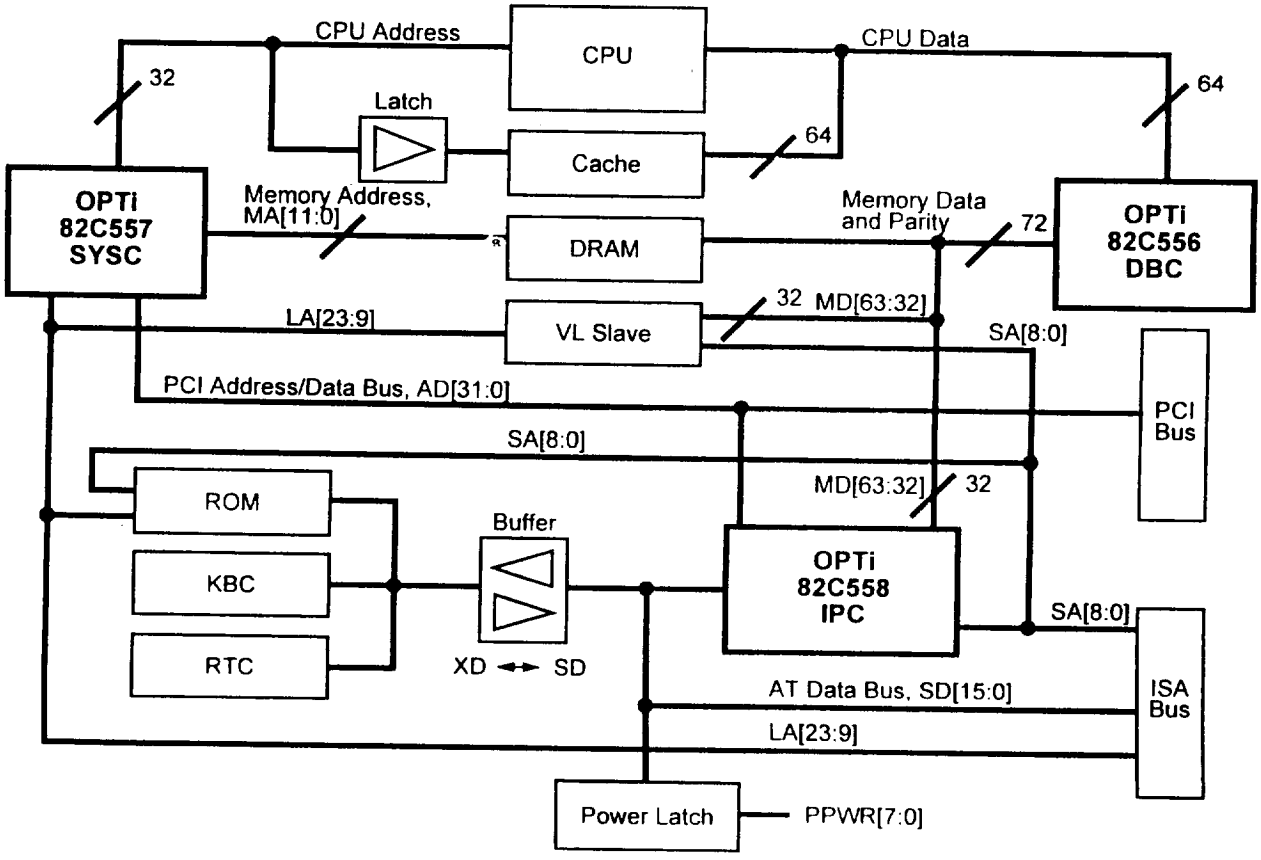
- Options for cacheable, write protected, system and video BIOS
- Supports six banks of 64-bit wide DRAMs with 256KB, 512KB, 1MB, 2MB, 4MB, 8MB and 16MB addressing page mode DRAMs
- Supports DRAM configurations up to 512MB
- Supports 3-3-3-3 pipelined DRAM burst cycles
- Programmable drive currents for the DRAM control signals
- 64-bit DRAM post write buffer
- Hidden refresh with CAS-before-RAS refresh supported
- Self-refresh supported during Suspend mode
- Support for flash ROM
- Shadow RAM option
- Transparent 8042 emulation for fast CPU reset and Gate A20 generation
- Supports Port 92h, fast Gate A20 and fast reset
- "True" GREEN power management support, with support for STPCLK# modulation and the CPU stop clock state

2.0 Overview

The OPTi Viper-DP (82C556/557/558) Desktop Chipset provides a highly integrated solution for fully compatible, high performance PC/AT platforms based on Intel's 3.3V Pentium Processor, Cryix's M1 Processor, and AMD's K5 Processor. The chipset provides 64-bit core logic, integrated PCI and VESA support, and sophisticated power management features. This highly integrated approach supplies the foundation for a cost effective platform without compromising performance. Its feature set furnishes an array of control and status monitoring options that are accessed through a simple and straightforward interface. All major BIOS vendors provide extensive software hooks that allow system designers to integrate their own special features with minimal effort.

The Viper-DP Desktop Chipset is comprised of three chips: 82C556 Data Buffer Controller (DBC), the 82C557 System Controller (SYSC), and the 82C558 Integrated Peripherals Controller (IPC).

Figure 2-1 Viper-DP Desktop Chipset System Block Diagram



2.1 82C556 (DBC) Data Buffer Controller

The 82C556 DBC performs the task of buffering the CPU to the DRAM memory data path. It also performs parity checking.

- CPU to memory data buffer
- CPU to local bus buffer
- Memory to local bus buffer
- 160-pin PQFP

Figure 2-2 shows a block diagram of the 82C556 DBC.

2.2 82C557 (SYSC) System Controller

The 82C557 SYSC provides the control functions for the host CPU interface, the 64-bit Level-2 (L2) cache, the 64-bit DRAM bus, the VL bus interface, and the PCI interface. (The SYSC also controls the data flow between the CPU bus, the DRAM bus, the local buses, and the 8/16-bit ISA bus.) The SYSC interprets and translates cycles from the CPU, PCI bus master, ISA master, and DMA to the host memory, local bus slave, PCI bus slave, or ISA bus devices.

- 3.3V CPU interface
- DRAM controller
- L2 cache controller
- L1 cache controller
- PCI interface
- Arbitration logic
- Data bus buffer control (memory data bus to and from host data bus)
- VL bus interface
- 208-pin PQFP or TQFP

Figure 2-3 shows a block diagram of the 82C557 SYSC.

2.3 82C558 (IPC) Integrated Peripherals Controller

The 82C558 IPC contains the AT bus controller and includes an 82C206, RTC interface, DMA controller, and a sophisticated system power management unit.

- AT bus controller
- Integrated 82C206 IPC
- System power management functions
- PCI local bus interface
- PCI to ISA expansion bridge
- Keyboard emulation of A20M# and CPU warm reset
- Port B and Port 92h Register
- Local bus interface
- Local I/O APIC
- 208-pin PQFP or TQFP

Figure 2-4 shows a block diagram of the 82C558 IPC.

Figure 2-2 82C556 DBC Block Diagram

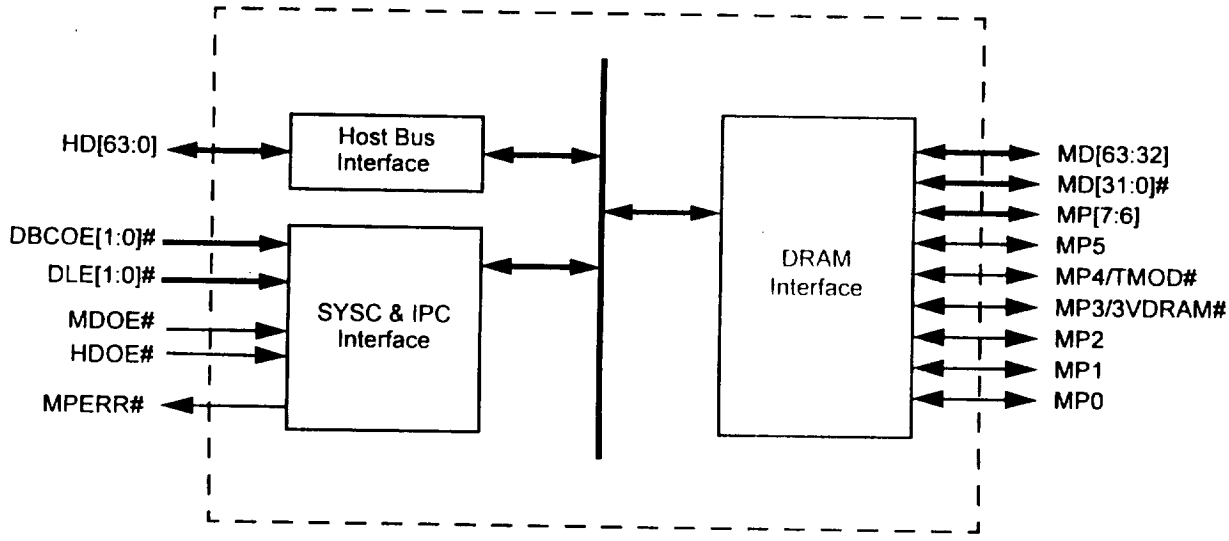


Figure 2-3 82C557 SYSC Block Diagram

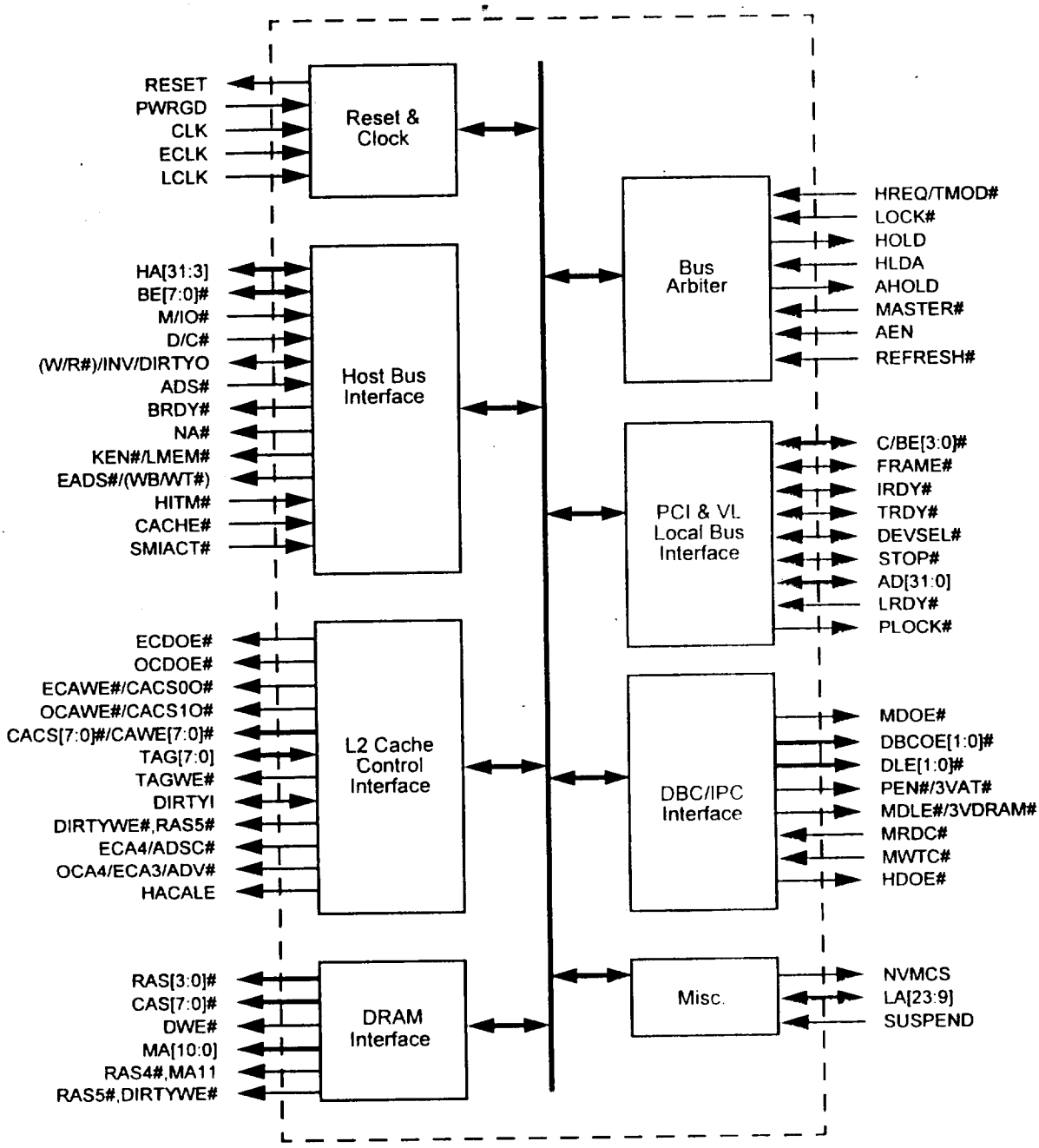
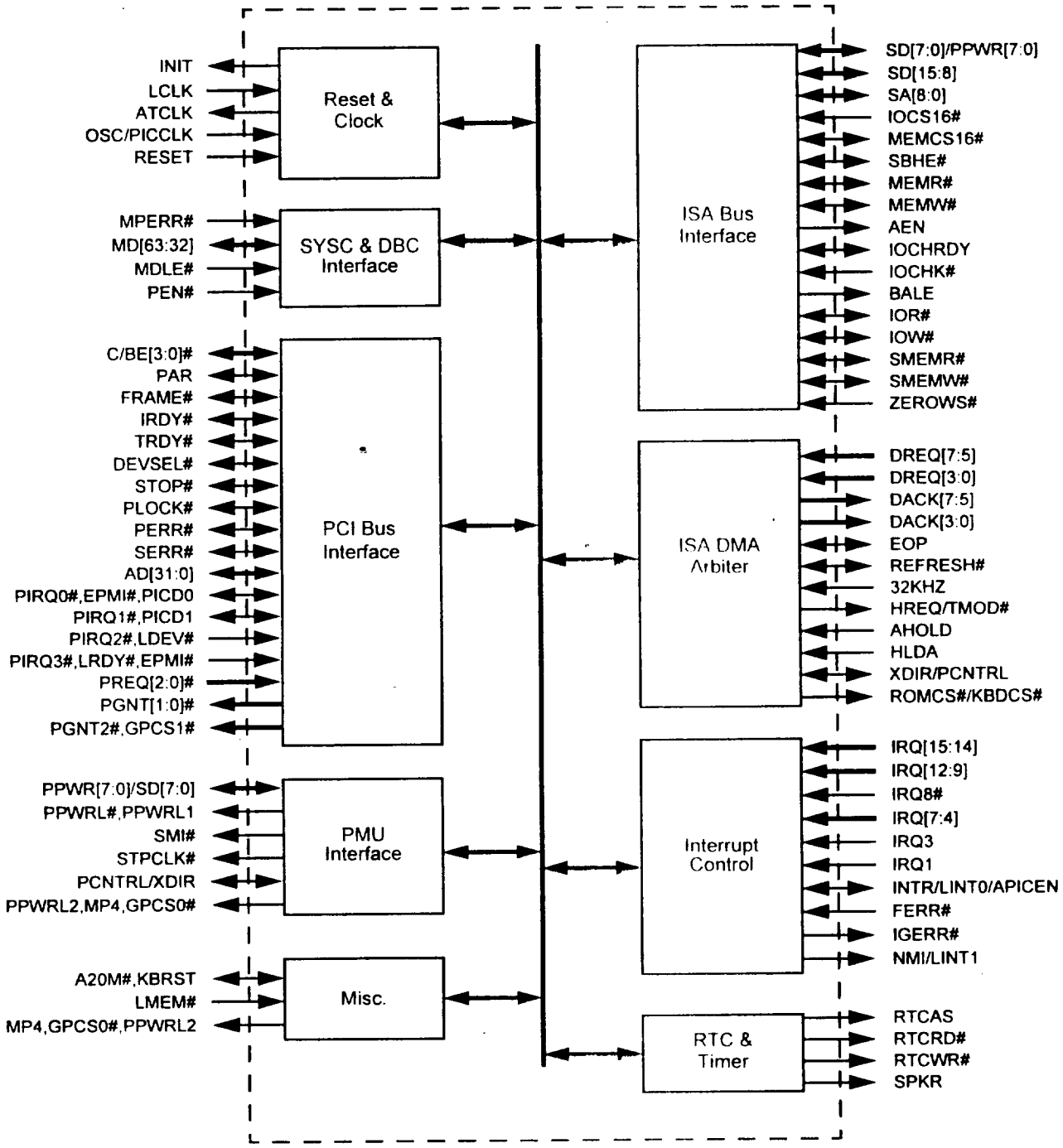


Figure 2-4 82C558 IPC Block Diagram



OPTi, Inc.
2525 Walsh Avenue
Santa Clara, CA 95051
(408) 980-8178
Fax: (408) 980-8860

Applications Note

Product Name: 82C621A Evaluation Board
Product Revision: 700-0012-001 Revision A.4
Date: August 11, 1994

Overview

The OPTi 82C621A Evaluation Board is a high-performance 32-bit PCI bus IDE adapter based on the OPTi 82C621A PCI bus IDE Controller (PIC) that offers exceptional performance, low part count and excellent compatibility features. The OPTi 82C621A PIC interfaces between the PCI bus and the industry-standard IDE bus (also known as the ATA or AT Attachment bus).

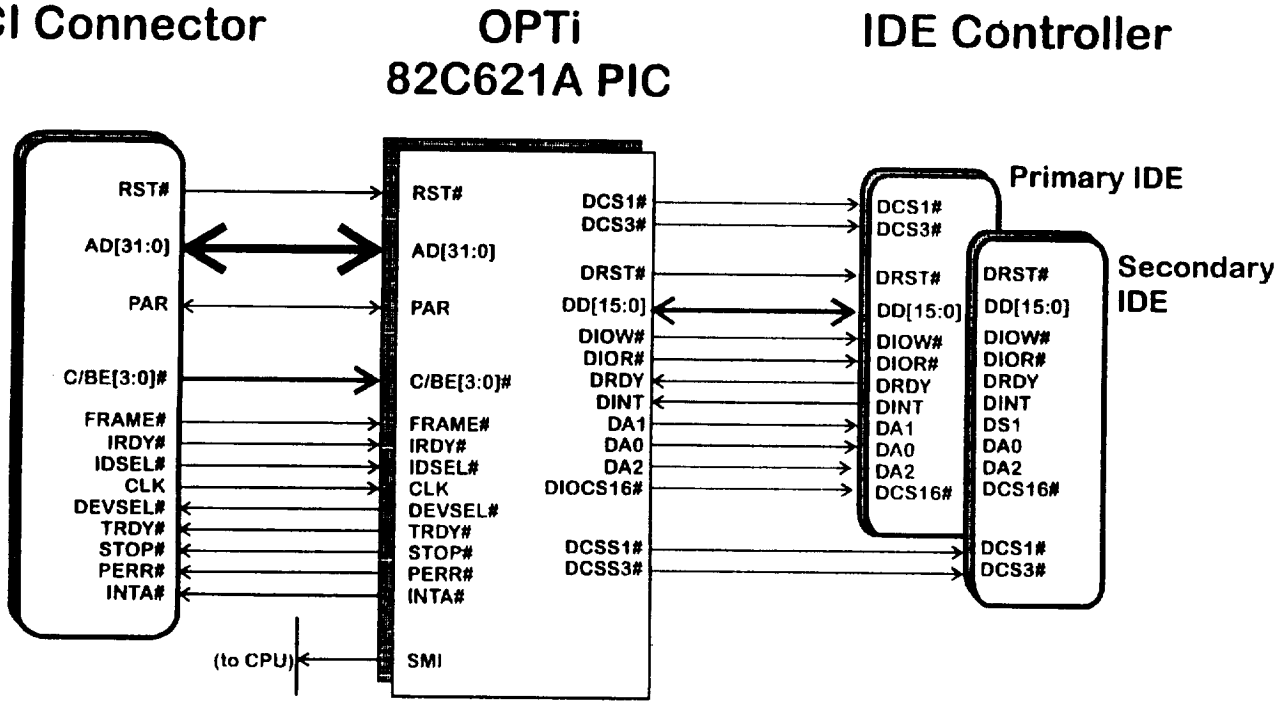
The 82C621A PIC implements single PCI functions to directly support both a Primary and Secondary IDE in a single 100-pin PQFP. This high-integration approach reduces component count, eases board design, reduces cost, and increases reliability. An integrated four-level read-prefetch FIFO and four-level posted-write FIFO supports zero-wait-state operations, substantially improving performance over other IDE implementations.

Write posting and read-prefetch allows CPU memory cycles to run concurrently with IDE cycles and also removes the synchronization penalty for AT bus transfers. IDE cycles can be fine tuned by the ANSI Mode strap options or programmable registers for ANSI-standard devices (mode 0, 1, 2, or 3)or non-standard devices. 32-bit PCI cycles are translated to two 16-bit IDE cycles for faster data access.

Although the board will work as a standard IDE interface, for top performance the OPTi supplied Setup program and device drivers should be used in DOS and Windows 3.1-based systems.

The complete design is available as a Turn-key Manufacturing Package (TMP) from OPTi, which includes complete schematics, Bill of Material (BOM), original CAD artwork (PADS PCB .JOB file), Gerber photoplotter files and design manual.

Figure 1. Evaluation Board Block Diagram



PCI-to-PCMCIA Adapter (CL-PD6729)
Data Sheet

CIRRUS LOGIC®

CL-PD6729

Advance Data Sheet

FEATURES

- Single-chip PCMCIA host adapter
- Direct connection to PCI bus
- Direct connection of two PCMCIA sockets
- Compliant with PCI 2.0
- Compliant with PCMCIA 2.1 and JEIDA 4.1
- 82365SL-compatible register set, ExCA™-compatible
- Automatic Low-power Dynamic mode for lowest power consumption
- Programmable Suspend mode
- Five programmable memory windows per socket
- Two programmable I/O windows per socket
- Programmable card access cycle timing
- 8- or 16-bit PCMCIA card support
- ATA disk interface support
- Automatic flash memory timing support
- 3.3V, 5V, or mixed 3.3/5V operation
- Supports PCMCIA low-voltage card specification
- Multiple CL-PD6729s can be used on the PCI bus without external hardware
- 208-pin PQFP

PCI-to-PCMCIA Host Adapter

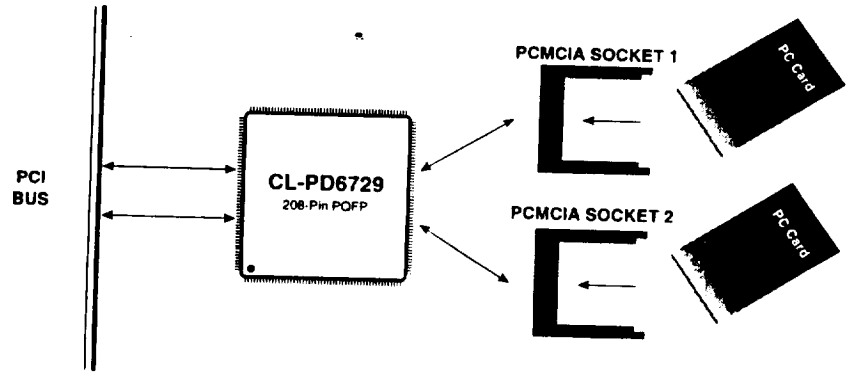
OVERVIEW

The CL-PD6729 is a single-chip PCMCIA host adapter solution capable of controlling two fully independent PCMCIA sockets. The chip is fully PCMCIA-2.1 and JEIDA-4.1 compliant and is optimized for use in notebook and handheld computers where reduced form factor and low power consumption are critical design objectives. With the CL-PD6729, a complete dual-socket PCMCIA solution with power-control logic can occupy less than 2 square inches (excluding connectors).

The CL-PD6729 chip employs energy-efficient, mixed-voltage technology that can reduce system power consumption by over 50 percent. The chip also provides a Suspend mode, which stops the internal clock, and an automatic Low-power Dynamic mode, which stops transactions on the PCMCIA bus, stops internal clock distribution, and turns off much of the internal circuitry.

(cont.)

System Block Diagram



PRELIMINARY

Am79C974

PCnet™-SCSI Combination Ethernet and SCSI Controller for PCI Systems

DISTINCTIVE CHARACTERISTICS

PCI Features

- Direct glueless interface to 33 MHz, 32-bit PCI local bus
- 132 Mbyte/s burst DMA transfer rate
- Compliant to PCI local bus Specification Revision 2.0

Ethernet Features

- Supports ISO 8802-3 (IEEE/ANSI 802.3) and Ethernet Standards
- High-performance Bus Master architecture with integrated DMA Buffer Management Unit for low CPU and bus utilization
- Individual 136-byte transmit and 128-byte receive FIFOs provide frame buffering for increased system latency
- Microwire™ EEPROM interface supports jumperless design
- Integrated Manchester Encoder/Decoder
- Provides integrated Attachment Unit Interface (AUI) and 10BASE-T transceiver with automatic port selection
- Automatic Twisted-Pair receive polarity detection and automatic correction of the receive polarity
- Dynamic transmit FCS generation programmable on a frame-by-frame basis
- Internal/external loopback capabilities
- Supports the following types of network interfaces:
  - AUI to external 10BASE2, 10BASE5, 10BASE-T or 10BASE-F MAU
  - Internal 10BASE-T transceiver with Smart Squelch to Twisted-Pair medium

SCSI Features

- Compliant to ANSI standards X3.131 – 1986 (SCSI-1) and X3.131 – 199X (SCSI-2)
- Fast 8-bit SCSI-2 10 Mbyte/s synchronous or 7 Mbyte/s asynchronous data transfer rate
- SCSI specific Bus Mastering DMA engine (32-bit address/data)
- 96-byte DMA FIFO for low bus latency
- On-chip state machine to control the SCSI sequences in hardware
- Integrated industry standard Fast SCSI-2 core
- Single-Ended 48 mA outputs to drive the SCSI bus directly
- Support for Scatter-Gather DMA data transfers
- Hooks in silicon and software to enable disk drive spin down for power savings

General Features

- Software compatible with AMD's Am79C960 PCnet-ISA, Am79C961 PCnet-ISA+, Am79C965 PCnet-32, Am79C970 PCnet-PCI register and descriptor architecture
- Plug-in and software compatible with AMD's PCscsi family of SCSI controllers for PCI
- NAND Tree test mode for connectivity testing on printed circuit boards
- Single +5 V power supply operation
- Low-power, CMOS design with sleep modes for both Ethernet and SCSI controllers allows reduced power consumption for critical battery powered applications and 'Green PCs'
- Fully static design for low frequency and power operation
- 132-pin PQFP package

GENERAL DESCRIPTION

The PCnet-SCSI combination Ethernet and 8-bit Fast SCSI controller with a 32-bit PCI bus interface is a highly integrated Ethernet-Fast SCSI system solution designed to address high-performance system application requirements. This single-chip is a flexible bus-mastering device that can be used in many applications, including network- and SCSI-ready PCs, printers, fax modems, and bridge/router designs. The bus-master architecture provides high data throughput in the system and low CPU and system bus utilization. The PCnet-SCSI controller is fabricated with AMD's advanced low-power CMOS process to provide low oper-

Publication# 18681 Rev. A Amendment /0
Issue Date: January 1994

ating and standby current for power sensitive applications.

The PCnet-SCSI is part of AMD's PCI product family of plug-in and software compatible SCSI and Ethernet controllers. This product compatibility ensures a low cost system upgrade path and lower motherboard manufacturing costs.

Ethernet Specific

The PCnet-SCSI controller includes a complete Ethernet node integrated into a single VLSI device. It contains a bus interface unit, a DMA buffer management unit, an IEEE 802.3-defined Media Access Control (MAC) function, individual 136-byte transmit and 128-byte receive FIFOs, an IEEE 802.3-defined Attachment Unit Interface (AUI) and Twisted-Pair Transceiver Media Attachment Unit (10BASE-T MAU), and a Microwire EEPROM interface. The PCnet-SCSI controller is also register compatible with the LANCE (Am7990) Ethernet controller, the C-LANCE (Am79C90) Ethernet controller, the ILACC (Am79C900) Ethernet controller, and all Ethernet controllers in the PCnet Family, including the PCnet-ISA controller (Am79C960), the PCnet-ISA+ controller (Am79C961), and the PCnet-32 controller (Am79C965). The buffer management unit supports the LANCE, ILACC, and PCnet descriptor software models. The PCnet-SCSI controller is software compatible with the Novell NE2100 and NE1500 Ethernet adapter card architectures. In addition, a Sleep function has been incorporated to provide low standby current, excellent for notebooks and Green PCs.

The 32-bit multiplexed bus interface unit provides a direct interface to the PCI local bus applications, simplifying the design of an Ethernet node in a PC system. With its built-in support for both little and big endian byte alignment, this controller also addresses proprietary non-PC applications.

The PCnet-SCSI controller supports auto configuration in the PCI configuration space. Additional PCnet-SCSI controller configuration parameters, including the unique IEEE physical address, can be read from an external non-volatile memory (serial EEPROM) immediately following system RESET.

The controller also has the capability to automatically select either the AUI port or the Twisted-Pair transceiver. Only one interface is active at any one time. The individual transmit and receive FIFOs optimize system overhead, providing sufficient latency during frame transmission and reception, and minimizing intervention during normal network error recovery. The integrated Manchester encoder/decoder (MENDEC) eliminates the need for an external Serial Interface Adapter (SIA) in the system. In addition, the device provides programmable on-chip LED drivers for transmit, receive, collision, receive polarity, link integrity or jabber status.

SCSI Specific

The PCnet-SCSI controller also includes a high-performance Fast SCSI controller with a glueless interface to the PCI local bus. The PCnet-SCSI integrates its own 32-bit bus mastering DMA engine with an industry standard Fast SCSI-2 block. The DMA engine and accompanying 96 byte DMA FIFO allow 32-bit burst data transfers across the high bandwidth PCI bus at speeds of up to 132 Mbyte/s. Full support for scatter-gather DMA transfers optimize performance in multi-tasking system applications.

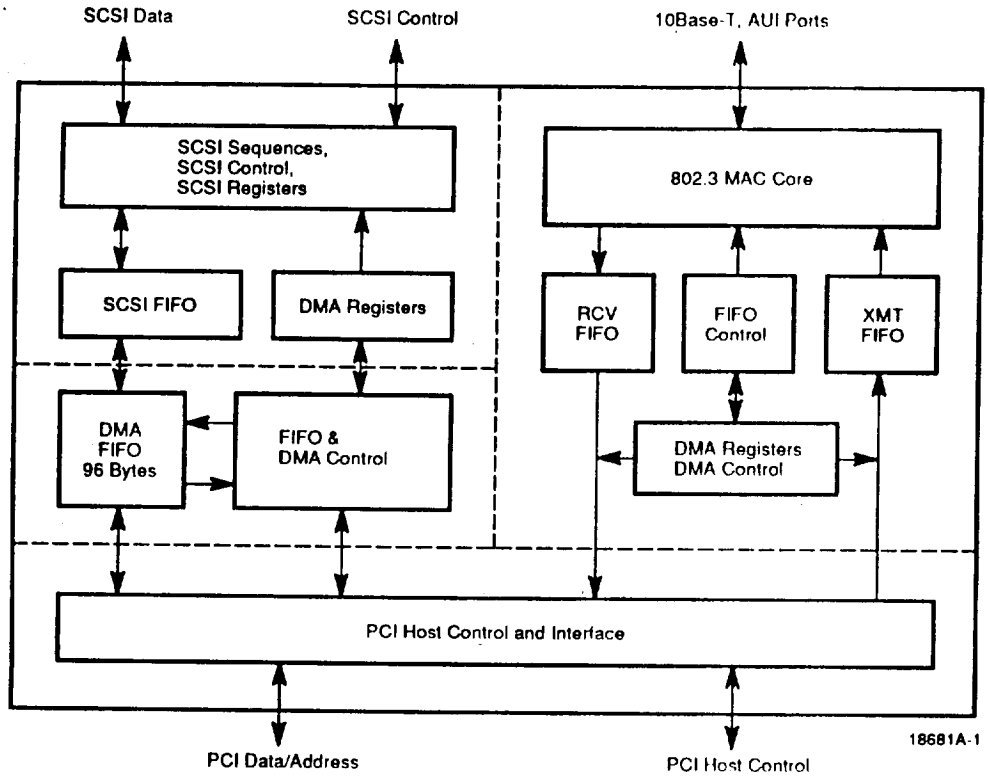
The PCnet-SCSI's on-chip state machine controls SCSI bus sequences in hardware and is coupled with the bus mastering DMA engine to eliminate the need for an on-chip RISC processor. This results in a smaller die size giving the Am79C974 superior price/performance versus competitive offerings.

AMD supports the Am79C974 with a total system solution which includes:

- A full suite of licensable SCSI drivers and utilities fully tested under the following operating system environments:
  - — DOS 5.0 – 6.0
  - — Windows 3.1
  - — Windows NT
  - — OS/2 2.x
  - — Netware 3.x, 4.x
  - — SCO UNIX 3.2.4, ODT 2.0
- An INT13h Compatible SCSI ROM BIOS
- ASPI Compatibility
- Complete hardware reference design kit

For more detailed information on the PCnet-SCSI refer to the technical manual, PID #18738A.

HIGH LEVEL BLOCK DIAGRAM



Philips Video Data Sheet

Digital multistandard colour decoder, square pixel (DMSD-SQP)

SAA7191B

1. FEATURES

- Separate 8-bit luminance (Y or CVBS) and 8-bit chrominance inputs (CVBS or C) from CVBS, Y/C, S-Video (S-VHS or Hi8) sources
- Luminance and chrominance signal processing for standards PAL-B/G, NTSC-M, SECAM
- Horizontal and vertical sync detection for all standards
- Real-time control output RTCO to be used for frequency-locked digital video encoder (SAA7199B). RTCO contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence.
- Controls via the I²C-bus
- User programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross colour cancellation (SECAM)
- 8-bit quantization of input signals
- 768/640 active samples per line equals 50/60 Hz (SQP)
- The YUV bus supports data rates of 780 x f_H equal to 12.2727 MHz for 60 Hz (NTSC-M) and 944 x f_H equal to 14.75 MHz for 50 Hz (PAL-B/G, SECAM) in 4 : 1 : 1 or 4 : 2 : 2 formats (via the I²C-bus)
- One crystal oscillator of 26.8 MHz

2. GENERAL DESCRIPTION

The SAA7191B is a digital multistandard colour decoder suitable for 8-bit CVBS input signals or for 8-bit luminance and 8-bit chrominance input signals (Y/C).

The SAA7191B is down-compatible with SAA7191. The SAA7191B has additional outputs RTCO, GPSW0 and ODD. These new outputs are in high-impedance state when NFEN-bit = 0.

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	-	100	250	mA
V_{IL}	input levels	TTL-compatible			
V_{OL}	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7191B	68	PLCC	plastic	SOT188

5. BLOCK DIAGRAM

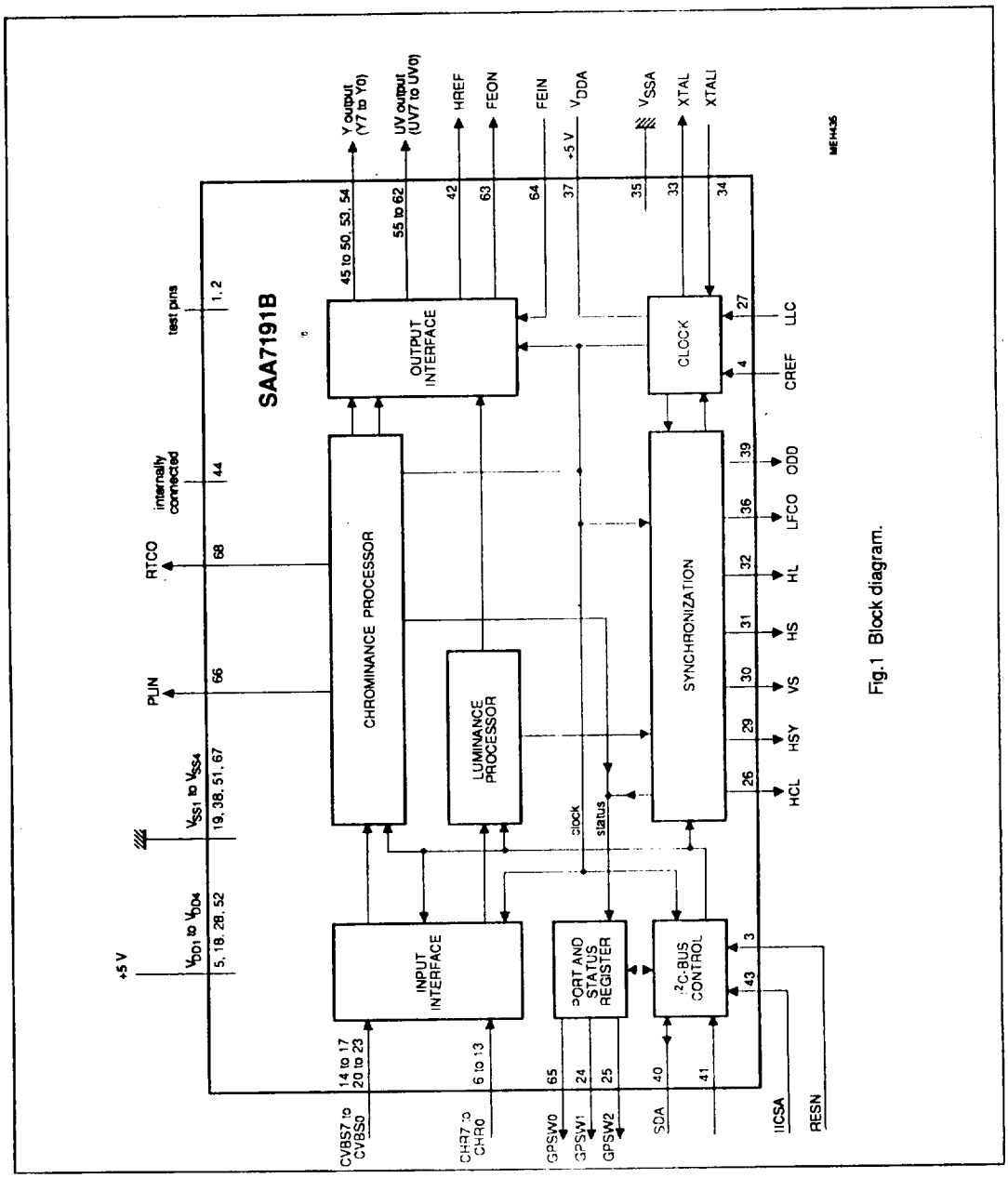


Fig.1 Block diagram.

Digital colour space converter

SAA7192A

FEATURES

- Input formatter with:
  - multiplexer
  - Y-dalay line
  - Cr and Cb interpolating filters
- Conversion matrix (acc. to CCIR 601)
- Video look-up tables (provide gamma correction)
- Pipeline delay line (horizontal reference signal)
- I²C-bus interface

GENERAL DESCRIPTION

The Digital Colour Space Converter (DCSC) is a digital matrix which is used to transform 16/24-bit digital input signals, i.e. Y (luminance), Cr (colour, R-Y) and Cb (colour, B-Y), into an RGB 24-bit format in accordance with the CCIR-601 recommendations.

Accepting inputs from the different formats of the DMSD2 decoder family, the device has a constant propagation delay and a maximum data rate of 16 MHz. A matched pipeline delay line is available to permit the HREF signal to be synchronized with the video data at the output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	Supply voltage	−0.5	7	V
VI	input voltage	−0.5	7	V
VO	output voltage	−0.5	7	V
P_{tot}	total power dissipation	-	1.5	W
T_{stg}	storage temperature range	−65	+150	C
T_{amb}	operating ambient temperature	0	+70	C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7192	68	PLCC	plastic	SOT18-8AA, AGA, CGS

BLOCK DIAGRAM

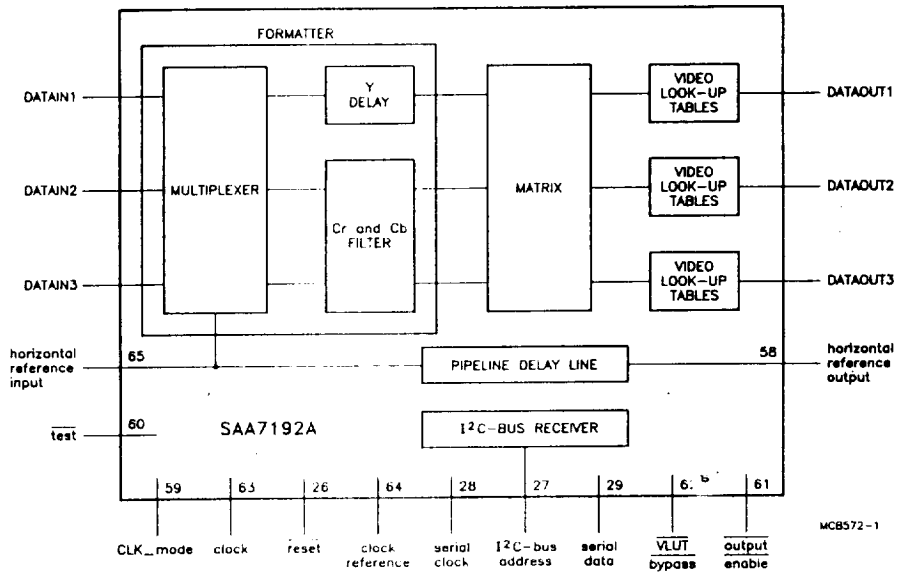


Fig 1 Block diagram.

Clock signal generator circuit for Desktop Video systems (SCGC)

SAA7197

FEATURES

- Suitable for Desktop Video systems
- Two different sync sources selectable
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LLCA, LLCB, LLC2A and LLC2B (2nd and 4th multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	5	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_I	input frequency range	6.0	-	7.2	MHz
V_I	input voltage LOW input voltage HIGH	0 2.4	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family. The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7197	20	DIL	plastic	SOT146
SAA7197T	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for Destop Video systems (SCGC)

SAA7197

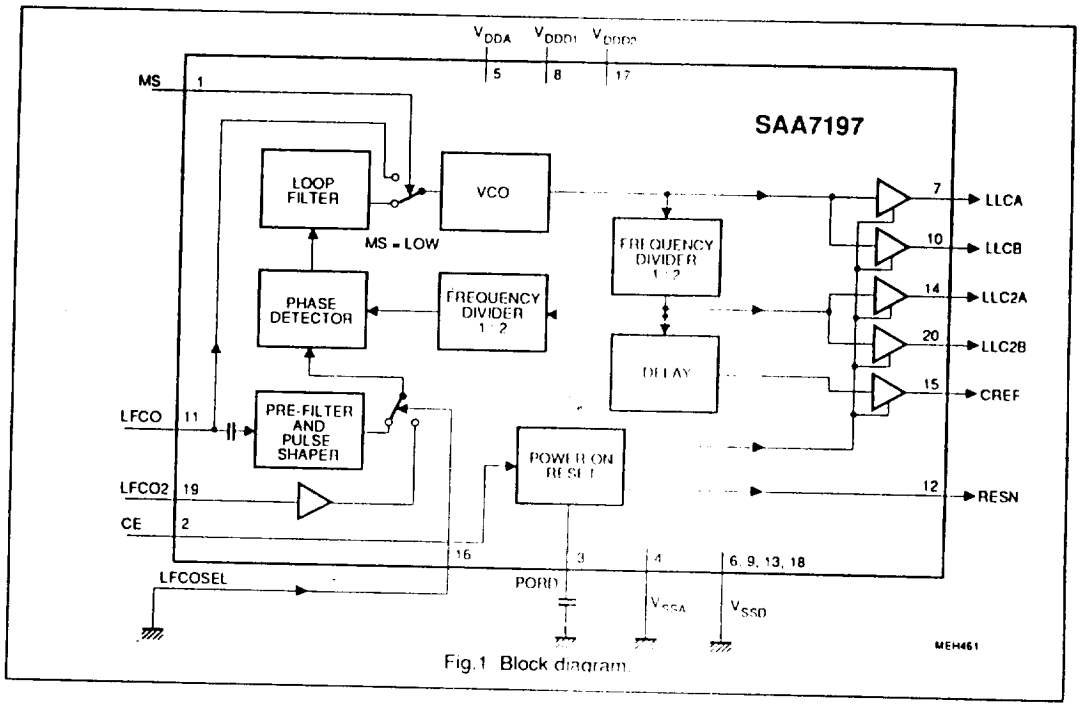


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder, square pixel (DMSD-SQP), digital video colour space converter (DCSC) and optional extentions. The SAA7197 completes a system for Desktop Video applications in conjunction with memory controllers.

The input signal LFCO is a digital-to-analog converted signal provided by the DMDS-SQPs horizontal PLL. It is the multiple of the line frequency:

7.38 MHz = 472 x f_H in 50 Hz systems
6.14 MHz = 360 x f_H in 60 Hz systems

LFCO2 (TTL-compatible signal from an external reference source) can be applied to pin 19 (LFCOSEL = HIGH).

The input signal LFCO or LFCO2 is multiplied by factors 2 or 4 in the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LLCA (pin7), LLCB (pin 10), LLC2A (pin 14) and LLC2B (pin 20) The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal LFCO (pin 11) is selected by LFCOSEL = LOW. LFCOSEL = HIGH selects LFCO2 input signal (pin 19). This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN set HIGH by CE = HIGH (Fig.4). CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

2 f_{LFCO} output to control the clock dividers of the DMSD-SQP chip family.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

Video analog input interface — TDA8708A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required
- The TDA8708A has white peak control in modes 1 and 2 whereas the TDA8708B has control in mode 1 only

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

GENERAL DESCRIPTION

The TDA8708A is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum −3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708A	28	DIP	plastic	SOT117-1
TDA8708AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

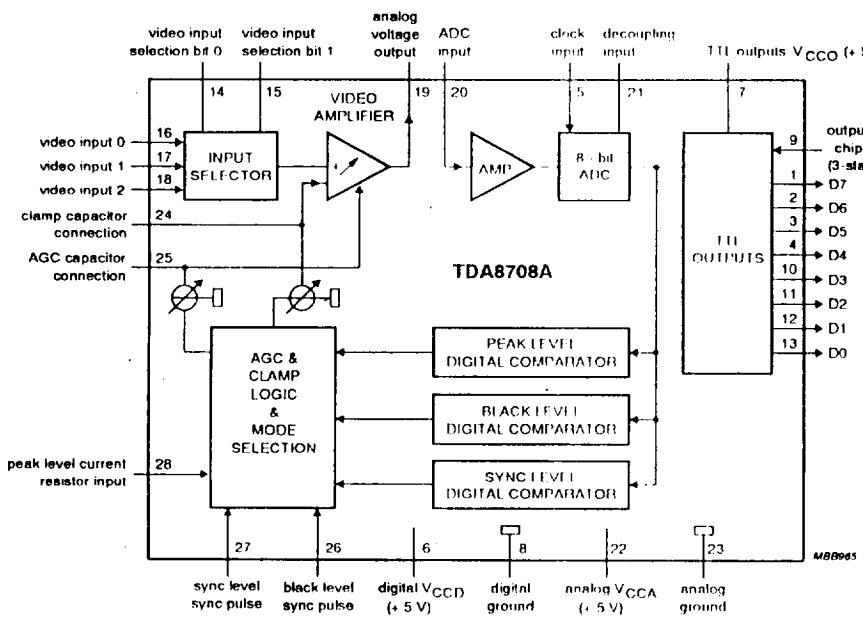


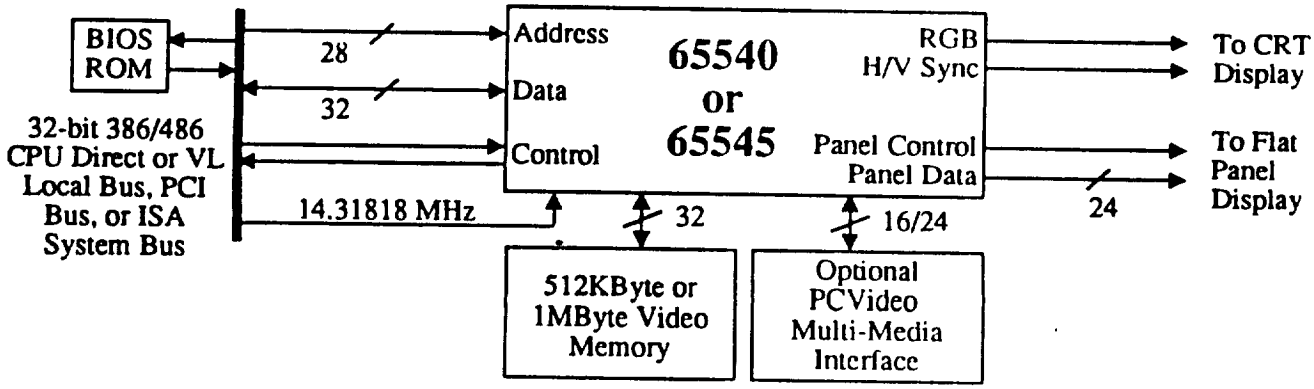
Fig.1 Block diagram.

Chips & Technology 65540/65545 Flat Panel Controller Data Sheet

CHIPS®

65540 / 545
High Performance
Flat Panel / CRT VGA Controller

- Highly integrated design (flat panel / CRT VGA controller, RAMDAC, clock synthesizer)
- Multiple Bus Architecture Integrated Interface
  - Local Bus (32-bit CPU Direct and VL)
  - EISA/ISA (PC/AT) Bus
  - PCI Bus (65545)
- Flexible display memory configurations
  - One 256Kx16 DRAM (512KB)
  - Four 256Kx4 DRAMs (512KB)
  - Two 256Kx16 DRAMs (1MB)
- Advanced frame buffer architecture uses available display memory, maximizing integration and minimizing chip count
- Integrated programmable linear address feature accelerates GUI performance
- Hardware windows acceleration (65545)
  - 32-bit graphics engine
    - System-to-screen and screen-to-screen BitBlt
    - 3 operand ROP's
    - Color expansion
    - Optimized for Windows™ BitBlt format
  - Hardware line drawing
  - 64x64x2 hardware cursor
- Hardware pop-up icon (65545)
  - 64x64 pixels by 4 colors
  - 128x128 pixels by 2 colors
- High performance resulting from zero wait-state writes (write buffer) and minimum wait-state reads (internal asynchronous FIFO design)
- Mixed 3.3V / 5.0V ±10% Operation
- Interface to CHIPS' PC Video to display "live" video on flat panel displays
- Supports panel resolutions up to 1280 x 1024 resolution including 800x600 and 1024x768
- Supports non-interlaced CRT monitors with resolutions up to 1024 x 768 / 256 colors
- True-color and Hi-color display capability with flat panels and CRT monitors up to 640x480 resolution
- Direct interface to Color and Monochrome Dual Drive (DD) and Single Drive (SS) panels (supports 8, 9, 12, 15, 16, 18 and 24-bit data interfaces)
- Advanced power management features minimize power consumption during:
  - Normal operation
  - Standby (Sleep) modes
  - Panel-Off Power-Saving Mode
- Flexible on-board Activity Timer facilitates ordered shut-down of the display system
- Power Sequencing control outputs regulate application of Bias voltage, +5V to the panel and +12 V to the inverter for backlight operation
- SMARTMAP™ intelligent color to gray scale conversion enhances text legibility
- Text enhancement feature improves white text contrast on flat panel displays
- Fully Compatible with IBM™ VGA
- EIAJ-standard 208-pin plastic flat pack



System Diagram

Introduction / Overview

The 65540 / 545 High Performance Flat Panel / CRT Controllers initiate a family of 208-pin, high performance solutions for full-featured notebook / sub-notebook and other portable applications that require the highest graphics performance available. The 65545 is pin-to-pin compatible with the 65540 and adds a sophisticated graphics hardware engine for Bit Block Transfer (BITBLT), line drawing, hardware cursor, and other functions intensively used in Graphical User Interfaces (GUIs) such as Microsoft Windows™. The 65540 and 65545 also use the same video BIOS, offering the system manufacturer a wide range of price / performance points while minimizing overhead for system integration and improving time-to-market. The following table indicates feature differences between the 65540 and 65545:

Features	65540	65545
Support for all flat panels	✓	✓
VESA Local Bus / ISA Bus	✓	✓
32-bit PCI Bus	—	✓
Linear Addressing	✓	✓
Hardware Accelerator	—	✓
Hardware Cursor	—	✓
Pin Compatible	✓	✓
BIOS Compatible	✓	✓

The 65540 / 545 family achieves superior performance through direct connection to system processor buses up to 32-bits in width. When combined with CHIPS' advanced linear acceleration software driver technology, these devices exhibit exceptional performance compared with devices of similar architecture. The 65540 / 545 architecture provides a fast throughput to video memory, maximizing the capability of today's powerful microprocessors to manipulate graphics operations. Based on the architecture of the 65540, the 65545 adds a powerful 32-bit graphics engine to offload graphics processing from the microprocessor for maximum performance.

Minimum chip-count, low-power graphics sub-system implementations are enabled through the high integration level of the 65540 / 545 family. These devices integrate the VGA-compatible graphics controller, true color RAMDAC, and dual PLL clock synthesizers. The entire graphics sub-system can be implemented with a single 256Kx16 DRAM. The 32-bit local bus interface of the 65540 / 545 family eliminates external buffers.

For maximum performance, the 65540 / 545 supports an additional 256Kx16 DRAM, which provides a 32-bit video memory bus and additional display memory to support resolutions up to 1024x768 with 256 colors, 800x600 with 256 colors, and 640x480 with 16M colors. In addition, the 65540 / 545 family can support PC Video multi-media features while interfacing to a 32-bit local bus and one MByte of video memory.

The 65540 / 545 family supports a wide variety of monochrome and color Single-Panel, Single-Drive (SS) and Dual-Panel, Dual Drive (DD) passive STN and active matrix TFT / MIM LCD, EL, and plasma panels. The 65540 / 545 family supports panel resolutions of 800x600, 1024x768, and 1280x1024. For monochrome panels, up to 64 gray scales are supported. Up to 226,981 different colors can be displayed on passive STN LCDs and up to 16M colors on 24-bit active matrix LCDs using the 65540 / 545 controllers.

The 65540 / 545 family offers a variety of programmable features to optimize display quality. For text modes which do not fill all 480 lines of a standard VGA panel, the 65540 / 545 provides tall font stretching in the hardware. Fast vertical centering and programmable vertical stretching in graphics modes offer more options for handling modes with less than 480 lines. Three selectable color-to-grayscale reduction techniques and SMARTMAP™ are available for improving the viewability of color applications on monochrome panels. CHIPS' polynomial FRC algorithm reduces panel flicker on a wider range of panel types with a single setting for a particular panel type.

The 65540 / 545 employs a variety of advanced power management features to reduce power consumption of the display sub-system and extend battery life. The 65540 / 545's internal logic, memory interface, bus interface, and flat panel interfaces can be independently configured to operate at either 3.3 V or 5.0 V. The 65540 / 545 is optimized for minimum power consumption during normal operation and provides two power-saving modes - Panel Off and Standby. During Panel Off mode, the 65540 / 545 turns off the flat panel while

the VGA sub-system remains active. The palette may also be automatically shut off during Panel Off mode to further reduce power consumption. During Standby mode, the 65540 / 545 suspends all CPU, memory and display activities. In this mode, the 65540 / 545 places the DRAM in self-refresh mode and the 65540 / 545 reference input clock can be turned off. The 65540 / 545 also provides a programmable activity timer which monitors VGA activity. After all display activity ceases, the timer will automatically shut down the panel by either disabling the backlight or putting the 65540 / 545 in Panel Off mode.

The 65540 / 545 is fully compatible with the VGA graphics standard at the register, gate, and BIOS levels. The 65540 / 545 provides full backwards compatibility with the EGA and CGA graphics standards without using NMIs. CHIPS and third-party vendors supply fully VGA-compatible BIOS, end-user utilities and drivers for common application programs (e.g., Microsoft Windows™, OS/2, WordPerfect, Lotus, etc.). CHIPS' drivers for Windows include a Big Cursor (to increase the cursor's legibility on monochrome flat panels) and panning / scrolling capability (to increase performance).

MINIMUM CHIP COUNT / BOARD SPACE

The 65540 / 545 provides a minimum chip count / board space, yet highly flexible VGA sub-system. The 65540 / 545 integrates a high-performance VGA flat panel / CRT controller, industry-standard RAMDAC, clock synthesizer, monitor sense circuitry and an activity timer in a 208-pin plastic flat pack package. In its minimum configuration, the 65540 / 545 requires only a single 256Kx16 DRAM, such that a complete VGA sub-system for motherboard applications can be implemented with just two ICs. This configuration consumes less than 2 square inches (1290 sq mm) of board space and is capable of supporting simultaneous flat panel / CRT display requirements while directly interfacing to a 32-bit local bus. As an option, a second memory chip may be implemented to increase performance (via a 32-bit data path to display memory) and support graphics modes which require more than 512 KBytes of display memory. No external buffers or glue logic are required for the 65540 / 545's bus interface, memory interface, or panel interface. The 65540 / 545 employs separate address and data buses with sufficient drive capability such that the bus can be driven directly. The 65540 / 545 also provides up to 24 bits of panel data with sufficient drive capability such that virtually all flat panels can be driven directly.

DISPLAY MEMORY INTERFACE

The 65540 / 545 supports multiple display memory configurations, providing the OEM with the flexibility to use the same VGA controller in several designs with differing cost, power consumption and performance criteria. The 65540 / 545 supports the following display memory configurations:

- One 256Kx16 DRAM (512 KBytes)
- Two 256Kx16 DRAMs (1 MBytes)
- Four 256Kx4 DRAMs (512 KBytes)

Performance is significantly improved when the 65540 / 545 is configured with a 32-bit data path to display memory, which is accomplished by using two 256Kx16 DRAMs. Two 256Kx16 DRAMs support all standard, Super, and Extended VGA resolutions up to 1024x768 256 colors as well as "high" 16bpp color and "true" 24bpp color modes. The table on the following page summarizes the display capabilities of the 65540 / 545.

Display memory control signals are derived from the integrated clock synthesizer's memory clock. The 65540 / 545 serves as a DRAM controller for the system's display memory. It handles DRAM refresh, fetches data from display memory for display refresh, interfaces the CPU to display memory, and supplies all necessary DRAM control signals.

The 65540 / 545 supports 'two-CAS / one-WE' and 'one-CAS / two-WE' 256Kx16 DRAMs. The 65540 / 545 supports the self-refresh features of 256Kx16 DRAMs and certain 256Kx4 DRAMs during Standby mode, enabling the 65540 / 545 to be powered down completely during suspend/resume operation.

Chips & Technology I/O Peripheral Controller Data Sheet

82C735
I/O Peripheral Controllers With Printgine

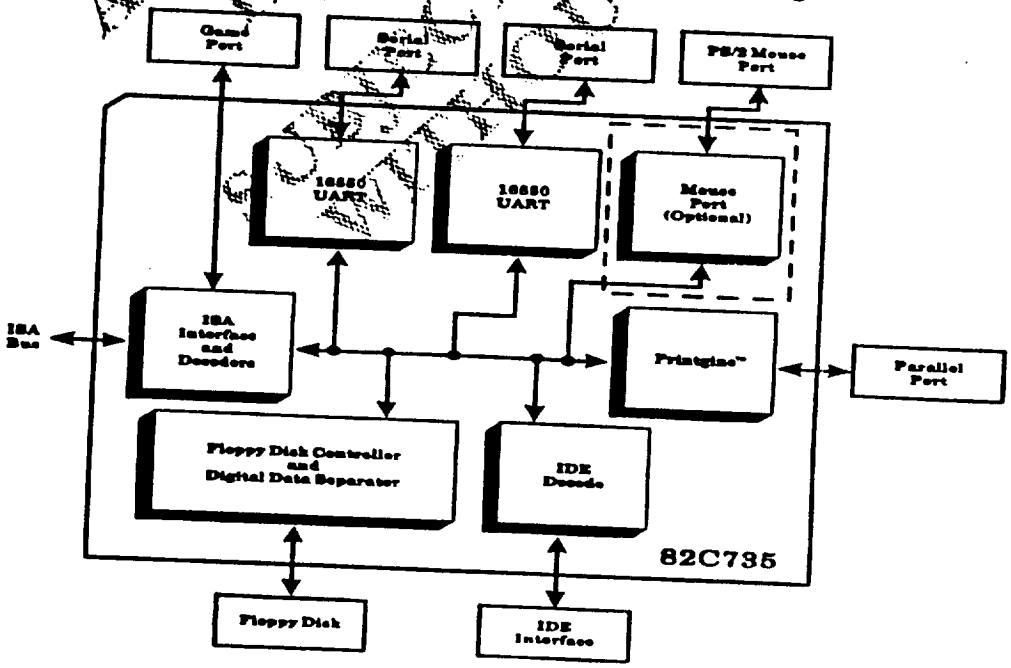
Floppy Disk Controller
- Single-chip floppy solution
- Software compatible with NEC 765B and Intel 82077
- Perpendicular recording support
- 48mA disk drivers and Schmitt-trigger inputs
- Direct support for two drives, and up to four drives with external decoder
- Enhanced digital data separator
- No external filter components required
- Support for 250kB/s, 300kB/s, 500kB/s and 1MB/sec data rates
- Primary and secondary floppy address port selects

Serial Ports
- Two NS16550 compatible UARTs
- 16-byte FIFO
- Modem control circuitry
- Optional PS/2 type mouse port logic operated under BIOS and software driver control

I. nterface
- Provides a complete IDE interface for embedded hard disk drives.
- Primary and secondary IDE address port selects.

Parallel Port—Printgine™
- Multiprotocol parallel port interface, P1284-compatible
- Compatible with IBM PC, XT, AT, and PS/2 architectures
- Standard and bidirectional parallel port
- Microsoft and Hewlett-Packard Extended Capabilities Port (ECP), Enhanced Parallel Port (EPP), and fast Centronics protocols support
- Transfer rates up to 2MB/sec possible with fast protocols
- Protocols implemented in hardware to reduce software overhead
- 24mA parallel port output drivers
- 128-byte FIFO

General
- 100-percent compatible with IBM PC, XT and AT architectures
- 24mA AT/XT bus interface buffers
- Game port and general purpose chip select logic
- On-chip power management features, controllable through hardware and/or software
- Configuration via software
- 100-pin QFP package



System Block Diagram

Introduction

The CHIPS® 82C735 enhanced I/O peripheral controller is a single-chip solution offering complete I/O capabilities for PC/AT and PC/XT motherboard applications. The controller is configured via software.

The 82C735 features a floppy disk controller, a digital data separator, two 16550 compatible UARTs, an enhanced bidirectional parallel port interface called Printgine, IDE interface control logic, and a game port chip select. For more information about these systems, see the "Functional Description."

4MB FLOPPY DISK CONTROLLER

The floppy disk controller is software compatible with 765B and 82077 controller functions. It provides a 4MB perpendicular recording format as well as the standard floppy drive format for 5.25-inch and 3.5-inch media. The controller supports two drives directly and up to four drives with an external decoder.

DIGITAL DATA SEPARATOR

The digital data separator is capable of data transfer rates up to 1MB/sec and requires no external components.

NS16550 UARTS AND IDE

The two licensed NS16550 UARTs are improved versions of the NS16450 UARTs. They are provided with individual 16-byte FIFOs to relieve the CPU of excessive software overhead and are still capable of running existing 16450 software.

The IDE control logic provides a complete IDE interface for embedded hard disk drives.

MOUSE PORT LOGIC

The 82C735 controller features optional PS/2 style mouse port logic with BIOS and driver support. Only one of the UARTs can be used when the mouse is operational.

PRINTGINE PARALLEL PORT INTERFACE

The parallel port interface, Printgine, is a multiprotocol interface capable of supporting both unidirectional and bidirectional transfer modes. It is fully compatible with ISA and PS/2 in the standard modes, and also supports Microsoft ECP, EPP, and fast Centronics in the enhanced modes. The output on the control pins switch to become bidirectional TTL drivers in the fast modes. This makes the port run faster than is possible with the open-drain drivers provided for the standard modes.

Printgine provides an economical mechanism for significantly improving the throughput of an improved parallel port that is upward compatible with the existing parallel port. The interface can operate in five different modes: standard (ISA-style unidirectional), bi-di (PS/2-style bidirectional), Microsoft ECP, EPP, and fast Centronics. The standard and bi-di modes are compatible with existing parallel port protocols.

The ECP, EPP, and fast Centronics protocols are enhanced bidirectional modes that achieve dramatic improvement by implementing the protocols in hardware. The fast Centronics mode is capable of a data transfer rate of 200kB/sec, while the ECP and EPP modes are capable of data transfer rates of 2MB/sec, compared to 15kB/sec in the standard mode.

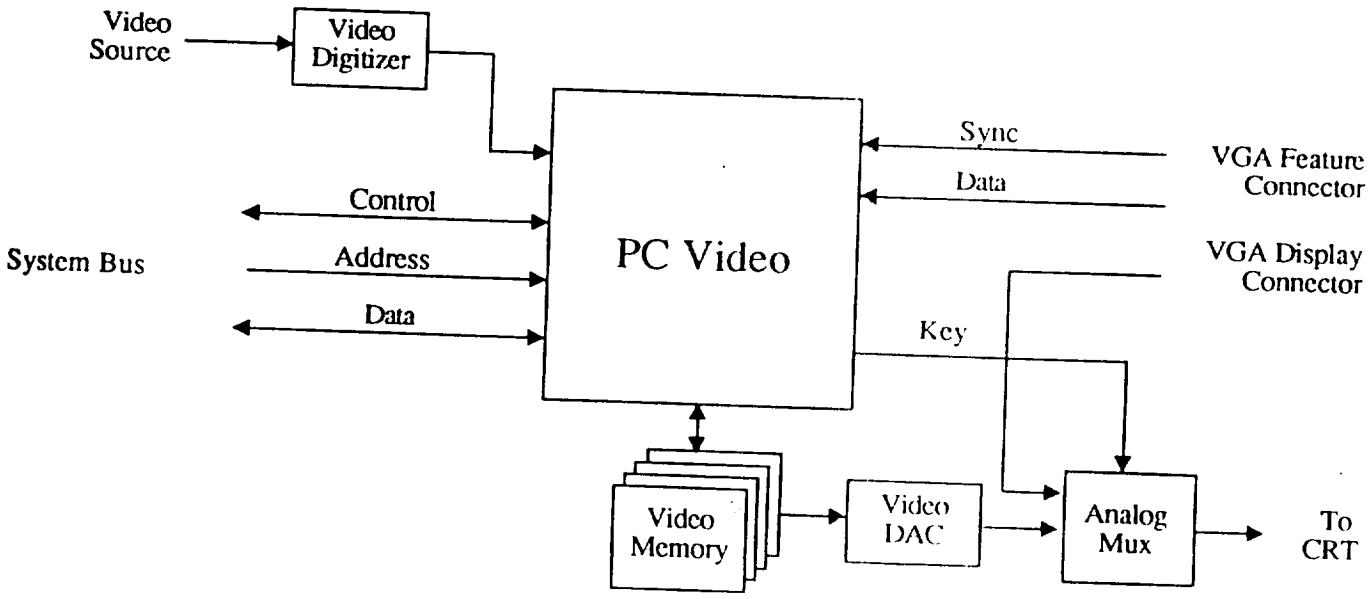
POWER MANAGEMENT

The 82C735 is provided with several power management features that are controllable through hardware or software. In hardware, the device can be completely powered down through a powerdown pin. In this mode, all inputs are disabled, all outputs are inactive, and the contents of all registers are preserved (as long as the power supply is maintained). In software, the device allows each port to be powered down independently.

Chips & Technology Video Controller Data Sheet

82C9001A
PC Video™
Video Windowing Controller

- Scan rate conversion and windowing control for display of a live video image on a computer graphics monitor
- Window positioning controlled by independent X-Y coordinates and by color keying
- Independent X-Y scaling of video image to 1/64 original image size
- Still-frame capture and display of true-color images
- Input resolutions up to 1024H x 512V pixels with full broadcast quality video bandwidth
- Up to 800 x 600 display resolution
- Supports NTSC, PAL, SECAM, S-VHS, and RGB input formats from industry-standard video digitizer chipsets
- Supports standard 4:1:1 and 4:2:2 YUV and 16-bit RGB digital formats
- Supports a memory efficient 2:1:1 YUV format
- Interlaced or non-interlaced input video
- Interlaced or non-interlaced output support
- Output zoom by factors of 2, 4 and 8
- Full-motion color video support on flat-panel displays with the 82C457



PC Video System Block Diagram

Introduction

OVERVIEW

The PC Video video windowing chip is the core component of a video subsystem which converts a standard full-motion video image into a format for display on a computer graphics monitor. PC Video controls positioning and scaling of the video image on the output display and allows the video image to be merged with computer graphics for interactive multimedia applications. Market applications of a subsystem based on PC Video include interactive video training, computer-based education programs, point-of-sale information, business presentations, video conferencing, and desktop publishing. PC Video integrates all the controlling logic for video scan rate conversion, windowing control, and scaling. Operation with VGA graphics is supported via the graphics feature connector.

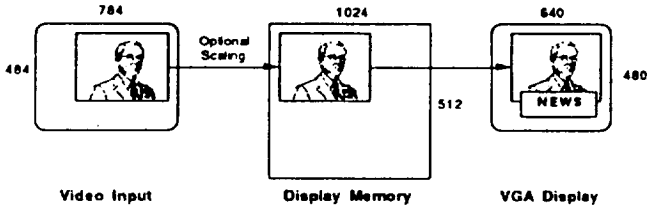
A video windowing sub-system can be implemented with the following components:

- PC Video
- A standard "Digital TV" chip set
- 4 VRAMs

Other optional configurations are supported for higher color and luminance bandwidth.

WINDOW ACQUISITION AND POSITIONING

PC Video provides the control signals for a standard video digitizer chip set. Interlaced and non-interlaced video sources, at full broadcast quality bandwidth, are supported at resolutions up to 1024 x 512 pixels. PC Video may be programmed to capture a full-size video image or a user-defined cropped or reduced area.



Acquisition & Display Process

Video output window positioning is provided by programmable X-Y coordinates and color keying to a specified color. Color Keying is based on the digital color information from the VGA feature connector. Color keying is supported independently or in conjunction with X-Y coordinates.

SCALING

PC Video provides independent X-Y scaling of the input video image in integer increments of 1/64. Images may be compressed down to 1/64 of the original image size, supporting video icons for graphical user interfaces.

MEMORY INTERFACE

PC Video operates with 256K x 4 100 ns VRAMs. Three configurations are supported: 4 VRAMs for 2:1:1 encoding, 6 VRAMs for 4:1:1 encoding, and 8 VRAMs for 4:2:2 and 16-bit RGB encoding.

Memory Requirements

Bits per Pixel	Format	Memory Required	Video Quality
12-bit	2:1:1 YUV	4 VRAM	Compressed luminance bandwidth
12-bit	4:1:1 YUV	6 VRAM	Broadcast video bandwidth
16-bit	4:2:2 YUV	8 VRAM	Improved chroma bandwidth
16-bit	16-bit RGB	8 VRAM	65,536 colors

COLOR FLAT-PANEL SUPPORT

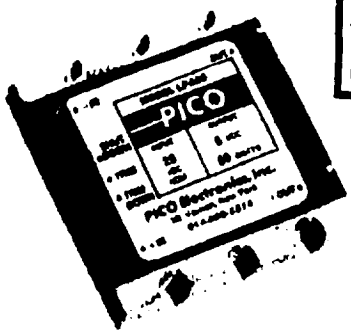
PC Video, with the 82C457 Color flat panel controller and the 82C411 pallette chip, provides full-motion video on a color LCD. The 82C457 dithers the PC Video output data to provide 20,000 colors on a 512-color display.

Power Supply Module Data Sheet

Pico Data Sheet

SERIES LPA

Isolated Regulated 75 Watts DC-DC Converters
Wide Input Range/18-36 VDC
Fully Regulated
Short Circuit Protected
*Parallel Operation



Dual Isolated Outputs
Special Voltage Combinations Available

The new PICO LPA Series of high power DC-DC Converters, allow a wide input voltage of 18–36 VDC, while maintaining a regulated output. They are fully safeguarded for over voltage, over temperature and continuous short circuit protection.

The availability of Dual Isolated Outputs, small size, and the capability of parallel operations as standard features should reduce your design and component costs, while the fixed frequency operation helps parallel connections for higher power requirements.

This high density unit is assembled *in the USA* with PICO quality and component selection, allowing it to meet the most stringent commercial requirements.

SERIES LPA SINGLE • 75 WATTS • INPUT 18–36 VDC

*PICO PART NUMBER	INPUT VOLTAGE RANGE (V DC)	OUTPUT VOLTAGE (V DC)	MAX. OUTPUT POWER (W)	EFF. FULL LOAD TYPICAL ** (%)	MAX LOAD REGULATION (%)**		MAX LINE REGULATION AT FULL LOAD (%)		OUTPUT VOLTAGE RIPPLE (FULL LOAD) 1-10MHz BW (MV P-P)	OUTPUT VOLTAGE TOLERANCE ** (±%)	PRICE
					10-50%	50-100%	18-28	28-36			
LPA3.3S	18-36	3.3	30	73	1.5	1.5	1	1	50	2	129.00
LPA5S	18-36	5	50	78	1.25	1.25	1	1	50	1.5	129.00
LPA5.2S	18-36	5.2	50	78	1.25	1.25	1	1	50	1.5	129.00
LPA9S	18-36	9	55	80	1.25	1.25	1	1	50	1	129.00
LPA12S	18-36	12	60	82	1.25	1.25	1	1	50	0.75	129.00
LPA15S	18-36	15	60	83	1	1	0.75	0.75	50	0.75	129.00
LPA24S	18-36	24	75	84	0.75	0.75	0.5	0.5	50	0.75	129.00
LPA28S	18-36	28	75	85	0.5	0.5	0.5	0.5	50	0.5	129.00
LPA48S	18-36	48	75	85	0.5	0.5	0.5	0.5	50	0.5	129.00
LPA100S	18-36	100	75	85	0.5	0.5	0.5	0.5	50	0.5	129.00

10% Minimum load required at all times
**Reading taken at nominal 28 VDC input
*Using proper thermal management, maximum temp. of +85°C (case)

SERIES LPA DUAL • 75 WATTS • INPUT 18–36 VDC

*PICO PART NUMBER	INPUT VOLTAGE RANGE (V DC)	OUTPUT VOLTAGE (V DC)	MAX. OUTPUT POWER (W)	EFF. FULL LOAD TYPICAL ** (%)	MAX. LOAD REGULATION (%)**		MAX. LINE REGULATION AT FULL LOAD (%)		OUTPUT VOLTAGE RIPPLE (FULL LOAD) 1-10MHz BW (MV P-P)	OUTPUT VOLTAGE TOLERANCE ** (±%)	PRICE
					10-50%	50-100%	18-28	28-36			
LPA5D	18-36	5	50	78	1.25	1.25	1	1	50	1.5	174.00
LPA9D	18-36	9	55	80	1.25	1.25	1	1	50	1	174.00
LPA12D	18-36	12	60	82	1.25	1.25	1	1	50	0.75	174.00
LPA15D	18-36	15	60	83	1	1	0.75	0.75	50	0.75	174.00
LPA24D	18-36	24	75	84	0.75	0.75	0.5	0.5	50	0.5	174.00
LPA28D	18-36	28	75	85	0.5	0.5	0.5	0.5	50	0.5	174.00
LPA48D	18-36	48	75	85	0.5	0.5	0.5	0.5	50	0.5	174.00

10% Minimum load required at all times
**Reading taken at nominal 28 VDC input
*Using proper thermal management maximum temp of +85°C (case)

FEATURES:
- Dual isolated outputs
- Short circuit protection
- Input voltage protection
- Thermal, over temp. shutdown
- Line regulation
- Load regulation
- No external components required
- Hi density, hi efficiency design
- Remote shutdown
- Trim capabilities
- Fixed frequency-100 Khtz

TYPICAL CHARACTERISTICS:

Frequency: 100 Khtz
Base plate: Max. +85°C
Operating Temp.: See thermal chart, Min. 0°C ambient, Max. +85°C base plate temp.
Test conditions: 25° C ambient
Isolation Base Input: 1000 VDC
Isolation Input Output: 1000 VDC
Isolation Output to Base: 1000 VDC
Storage Temp.: −55°C to +105°C

For All Variations Call Factory

17 Standard Models

Meets MIL STD 704 Surge Requirements

*Parallel Operation Add Suffix P to: LPA5SP

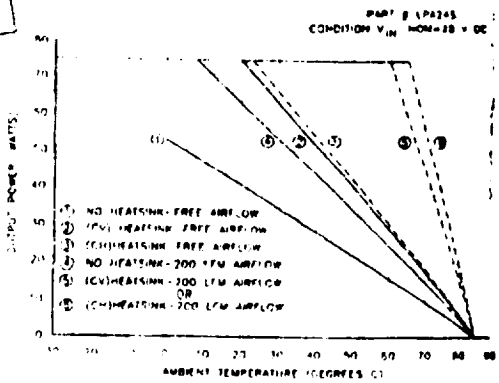
Application Notes Page D-2207
Mechanical Configuration Pages D-2208-12

Fixed Frequency

Hi Density 75 Watts

100 VDC Output Models

Full thermal analysis can be determined using application notes on Page D-2207. By using the efficiency and thermal resistance of your desired unit in the formula you can complete your evaluation.
The curves below were generated for Part #LPA24S using Application Notes on Page D-2207. Please consult factory with any questions.



For immediate engineering assistance or to place an order–
Call Toll Free 800-228-6747

PICO Electronics, Inc.
453 N. MacQuesten Pkwy. Mt. Vernon, N.Y. 10552
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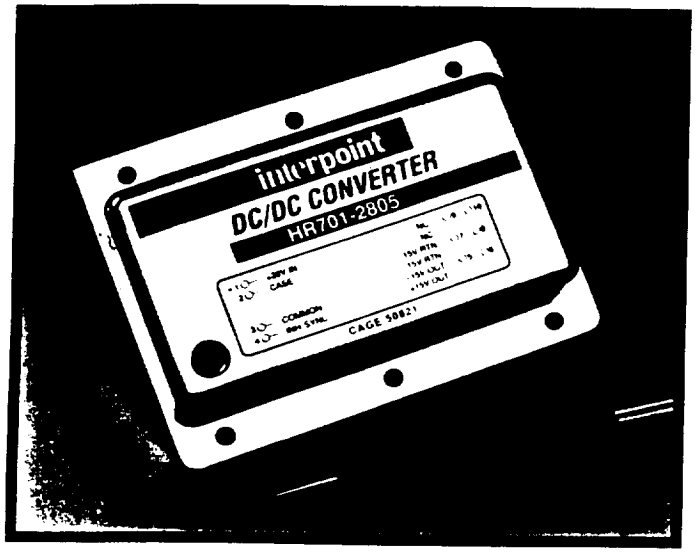
Delivery– stock to one week

Interpoint Data Sheet

interpoint

10301 Willows Road P.O. Box 97005 Redmond, WA 98073-9705 TEL: (206) 882-3100 TEL: (800) 822-8782 FAX: (206) 882-1990

HR700 SERIES DC-DC CONVERTERS



- **Up to 70 watts output power**
- **Hermetically sealed metal case**
- **Up to 83% efficiency**
- **Industrial converters with Military program reliability**
- **Burn in and stabilization bake standard**
- **External synchronization**
- **Short circuit protected**
- **19-40 Vdc input range**
- **20 watts per inch³**
- **–20 to +70°C operation**

HR700 Series dc-dc converters offer up to 70 watts of power from single, dual, or triple outputs in one package. The converters combine the small size and high reliability of hybrid-based components, the high efficiency of switching regulators, and the isolation, regulation, and low noise characteristics of linear regulators.

SMALL SIZE

The HR700 converters are manufactured using techniques that provide very small size and low profile components. Each converter uses less than eight square inches of board area and is .595 inch high or less. The overall power density is 20 watts per cubic inch.

HIGH RELIABILITY

Assembled using thick-film hybrid technology, the HR700 converters are built to perform reliably in the harshest environments. The converters have more uniform thermal coefficients and 50% fewer connections than converters built by surface mount techniques. The HR700 parts use the same manufacturing procedures and quality controls that we apply to converters designed for commercial airliners, the space shuttle, advanced fighter aircraft, and other high reliability applications. The steel cases are hermetically sealed in a dry nitrogen environment and are guaranteed a maximum leak rate of less than 10^3 atm-cc/sec. Stabilization bake and a 24-hour burn in at maximum operating temperature are standard for all parts. All devices are 100% electrically tested.

HIGH PERFORMANCE

The HR700 series parts are high efficiency, low noise, pulse width modulated converters which utilize a quasi-square wave forward converter design with a nominal switching frequency of 245kHz. Isolation between input and output is provided with a transformer in the forward power loop and a wide band, temperature insensitive optical link in the feedback control loop. Short circuit protection is provided by detecting peak primary switching current on a cycle basis and limiting it to approximately 130% of the full load input current. This method results in quick and positive current limiting under short circuit conditions.

HR700 Series dc-dc converters are designed to provide full power operation over the input voltage range of 19-40 Vdc. Operation below an input of 19 volts is possible with derated output power. Outputs are available as 5, 12, and 15 Vdc in single, dual and triple outputs. The converters typically provide greater than 80% efficiency over the entire input range. Line regulation is typically within 0.1% and load regulation within 0.2%.

LOW NOISE

The HR700 series converters offer low noise on both the input and output lines. A two section, four pole LC input filter is included to provide very low reflected line ripple current. Output ripple is maintained at less than 50mV p-p for single and dual output models and 85mV for triple output models.

INHIBIT/SYNC FEATURE

An inhibit/sync pin is standard on all models of the HR700 series converters. The pin serves as both an output inhibit and as a synchronization input. In the inhibit mode an open collector TTL compatible low (<0.8Vdc) will disable internal switching thereby inhibiting the unit's output. Inhibiting in this manner results in an extremely low quiescent current.

10301 Willows Road P.O. Box 97005 Redmond, WA 98073-9705 TEL: (206) 882-3100 TEL: (800) 822-8782 FAX: (206) 882-1990

SPECIFICATIONS (ALL MODELS) T_A = 25°C, V_{IN} = 28 Vdc unless specified otherwise.

INPUT VOLTAGE RANGE: 19 to 40 Vdc (Note 4).
OPERATING TEMPERATURE RANGE: -20°C to +70°C (Case).
STORAGE TEMPERATURE RANGE: -55°C to +125°C (Case).
OUTPUT VOLTAGE TEMPERATURE COEFFICIENT: 150 ppm/°C (Typical).
ISOLATION: 100 Mohm Minimum at 500 Vdc.
INPUT TO OUTPUT CAPACITANCE: 160 pF Typical.
CONVERSION FREQUENCY: 245 kHz Typical.
EXTERNAL SYNCHRONIZATION RANGE: Nominal to 370 kHz.
EXTERNAL SYNC. DUTY CYCLE: 70 to 98% high.
EXTERNAL SYNC. VOLTAGES: Logic High > +4.5 Vdc
Logic Low < +0.8 Vdc
OUTPUT INHIBIT PIN: Open collector TTL compatible
TTL Logic High (Open Circuit) = output enabled (≥4.5 Vdc)
TTL Logic Low = output disabled (≤0.8 Vdc)
OUTPUT INHIBIT PIN OPEN CIRCUIT VOLTAGE: +4.5 to +5.5 Vdc.
OUTPUT INHIBIT PIN LOGIC LOW CURRENT: 1mA Max.
WEIGHT: 140 Grams Typical.

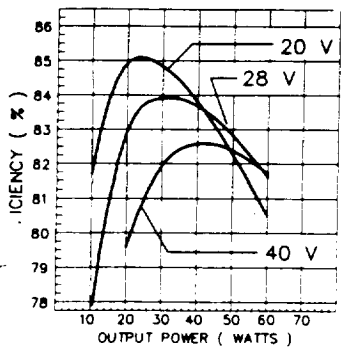
CHARACTERISTICS (SINGLE OUTPUT MODELS) T_A = 25°C, V_{IN} = 28 Vdc free run mode, unless specified otherwise.

PARAMETER	CONDITION	HR701-2805			HR701-2812			HR701-2815			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
OUTPUT VOLTAGE	FULL LOAD	4.9	5.00	5.10	11.75	12.00	12.25	14.75	15.00	15.25	VDC
OUTPUT CURRENT	FULL LOAD	—	—	12.00	—	—	5.83	—	—	4.67	ADC
OUTPUT POWER	TC = -55° TO +85°C	—	—	60	—	—	70	—	—	70	WATTS
OUTPUT RIPPLE	FULL LOAD BW ≤ 2MHz	—	30	100	—	30	100	—	30	100	mVp-p
INPUT CURRENT	NO LOAD INHIBITED	— —	75 30	100 35	— —	70 30	100 35	— —	70 30	100 35	mADC
INPUT REFL. RIPPLE	FULL LOAD	—	10	50	—	10	50	—	10	50	mA
EFFICIENCY		77	80	—	80	83	—	80	83	—	%
LOAD REGULATION	NO LOAD TO FULL	—	10	30	—	10	30	—	10	30	mVDC
LINE REGULATION	19 TO 40 VDC	—	10	30	—	10	30	—	10	30	mVDC
STARTUP TIME	WITH LOW IMP. SOURCE	—	5	10	—	8	10	—	8	10	mS

DERATING INFORMATION

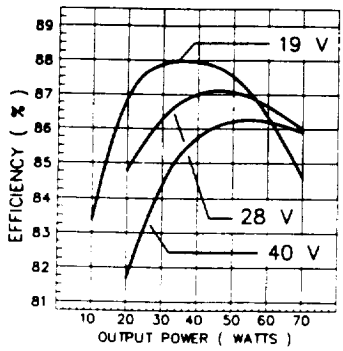
1. Linearly derate output power to zero watts at 125°C.
2. Above 105°C linearly derate steady state and transient input voltage to 33 and 38 volts respectively at 125°C.
3. Indefinite short circuit protection is not guaranteed above + 70°C.
4. Operation below an input voltage of 19 volts, including operation in MIL-STD-704D emergency power conditions is possible with derated output power. See Fig. 4.

TYPICAL PERFORMANCE CURVES



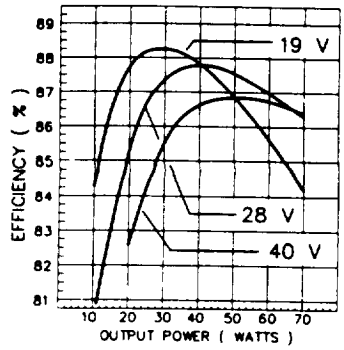
HR701 2805
EFFICIENCY VS LINE & LOAD

Figure 1



HR701-2812
EFFICIENCY VS LINE & LOAD

Figure 2



HR701-2815
EFFICIENCY VS LINE & LOAD

Figure 3

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CHARACTERISTICS (DUAL/TRIPLE OUTPUT MODELS) T_A = 25°C, V_{IN} = 28 Vdc free run mode, unless specified otherwise.

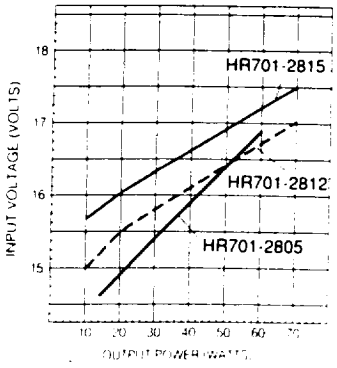
PARAMETER	CONDITION	HR702-2812			HR702-2815			HR703-2812			HR703-2815			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
OUTPUT VOLTAGE	FULL LOAD MAIN	—	—	—	—	—	—	4.90	5.05	5.15	4.9	4.95	5.1	±DCV
	DUAL	11.75	12.00	12.25	14.75	15.00	15.25	11.50	11.80	12.1	15.05	15.30	15.75	±DCV
OUTPUT CURRENT	V_{IN} = 19 to 40 MAIN	—	—	—	—	—	—	—	4.0	10.0	—	4.0	10.0	ADC
	DUAL	—	2.92	5.5	—	2.33	4.4	—	1.67	4.2	—	1.33	3.33	NOTES 1 & 2
OUTPUT POWER	MAIN	—	—	—	—	—	—	—	20	50	—	20	50	WATTS
	± DUAL	—	35	66.5	—	35	66.5	—	20	50	—	20	50	
	TOTAL	—	70	NOTE 1	—	70	NOTE 1	—	60	NOTE 2	—	60	NOTE 2	
OUTPUT RIPPLE	FULL LOAD MAIN	—	—	—	—	—	—	—	50	100	—	50	100	mV p-p
	BW ≤ 2MHz DUAL	—	30	100	—	30	100	—	50	100	—	50	100	
INPUT CURRENT	NO LOAD	—	75	100	—	75	100	—	35	115	—	60	115	mADC
	INHIBITED	—	25	35	—	25	35	—	30	35	—	25	35	
INPUT REFL. RIPPLE	FULL LOAD BW ≤ 10MHz	—	15	50	—	15	50	—	15	50	—	15	50	mA p-p
EFFICIENCY		80	83	—	80	83	—	79	84	—	79	84	—	%
LOAD REGULATION	NO LOAD TO FULL MAIN	—	—	—	—	—	—	—	5	30	—	5	30	mVDC
	DUAL	—	25	50	—	25	50	—	480	750	—	300	600	
LINE REGULATION	19 to 40V MAIN	—	—	—	—	—	—	—	2	25	—	2	25	mVDC
	DUAL	—	10	30	—	10	30	—	100	225	—	100	225	
STARTUP TIME		—	15	25	—	15	25	—	6	10	—	6	10	mS
CROSS [3] REGULATION	DUAL +Po = 3 W to 35 W -Po = 35 W	—	1.5	3.0	—	1.5	3.0	—	—	—	—	—	—	%
	DUAL +Po = 20 W to 50 W -Po = 50 W to 20 W	—	2.0	4.0	—	2.0	3.5	—	—	—	—	—	—	
CROSS [4] REGULATION	MAIN Po = 30 W DUAL +Po = 3 W to 27 W -Po = 27 W to 3 W	—	—	—	—	—	—	—	2.3	6.0	—	2.3	5.0	%
	MAIN Po = 3 W to 30 W DUAL ±Po = 15 W	—	—	—	—	—	—	—	5.4	9.0	—	5.0	7.0	

Note 1: On dual output models the maximum combined output power is 70 watts. A maximum of 95% (66.5W) is available from any single output.
Note 2: On triple output models the maximum combined output power is 60 watts. A maximum of 50 watts is available from a single output.
Note 3: Shows regulation effect on the negative dual output during the defined cross loading conditions.
Note 4: Shows regulation effect on both dual outputs during the defined cross loading conditions.

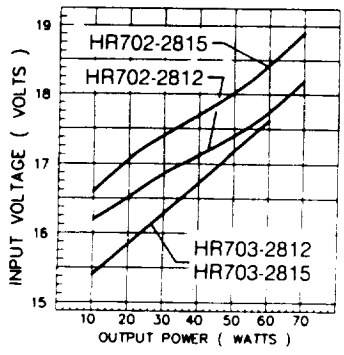
DERATING INFORMATION

1. Derate output power linearly to zero at + 125°C.
2. Above 105°C derate steady state and transient input voltage linearly to 33 and 38 volts respectively at + 125°C.
3. Indefinite short circuit protection is not guaranteed above + 70°C.
4. Operation below an input voltage of 19 Vdc, including operation in MIL-STD-704D emergency power conditions is possible with derated output power. (See Figure 5.)

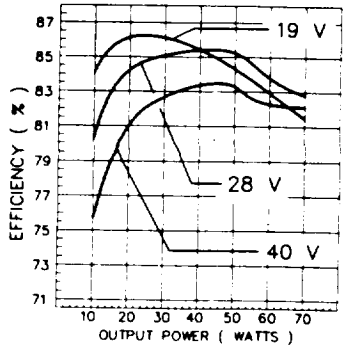
TYPICAL PERFORMANCE CURVES



LOW LINE DROPOUT VS LOAD (50mV DROP)
Figure 4



LOW LINE DROPOUT VS. LOAD (50 mV DROP)
Figure 5



HR702 2812
EFFICIENCY VS LINE & LOAD
Figure 6

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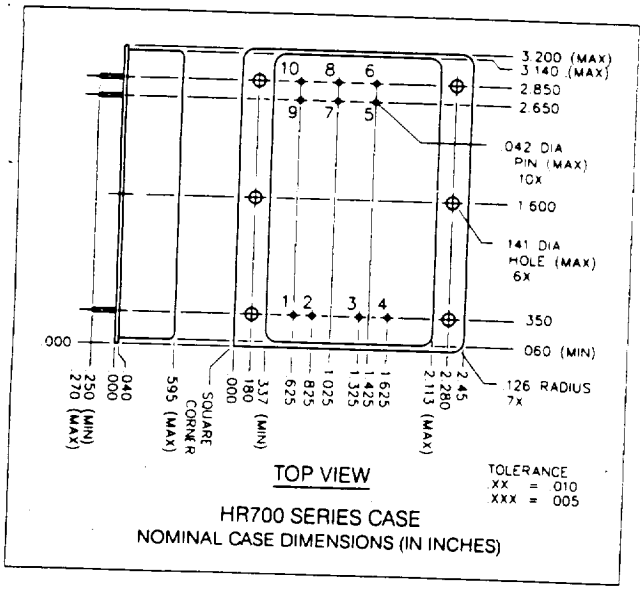
METAL HERMETIC PACKAGE



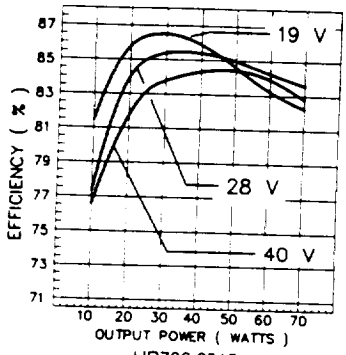
HR700 SERIES CASE
NOMINAL CASE DIMENSIONS (IN INCHES)

DESIGNATION	HR701-2805 HR701-2812 HR701-2815 SINGLE PIN NO.	HR702-2812 HR702-2815 DUAL PIN NO.	HR703-2812 HR703-2815 TRIPLE PIN NO.
POSITIVE INPUT	1	1	1
INPUT COMMON	3	3	3
INHIBIT/SYNC INPUT	4	4	4
CASE GROUND	2	2	2
POSITIVE MAIN OUTPUT (+5, +12 or +15VDC)	9, 10	6	9, 10
POSITIVE AUX OUTPUT (+12 or +15VDC)	N/A	N/A	6
NEGATIVE AUX OUTPUT (−12 or −15VDC)	N/A	5	5
MAIN OUTPUT COMMON	7, 8	7, 8	7, 8
AUX OUTPUT COMMON	N/A	7, 8	7, 8
POSITIVE REMOTE SENSE	6	N/A	N/A
COMMON REMOTE SENSE	5	N/A	N/A

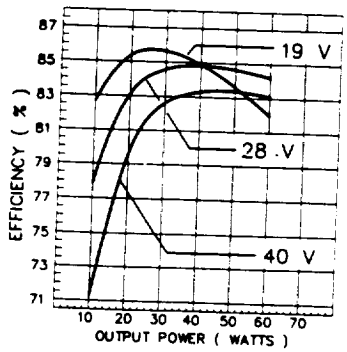
CASE, PINS AND COVER: Cold Rolled Steel with Fused Tin Finish.

CAUTION: Heat from reflow or wave soldering may damage this converter. Solder this part one pin at a time with heat application NOT exceeding 300°C for 10 seconds per pin.

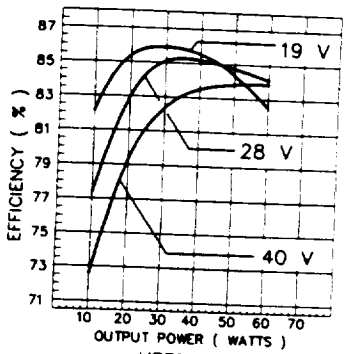
TYPICAL PERFORMANCE CURVES



HR702-2815
EFFICIENCY VS. LINE & LOAD
Figure 7



HR703-2812
EFFICIENCY VS. LINE & LOAD
Figure 8



HR703-2815
EFFICIENCY VS. LINE & LOAD
Figure 9

interpoint

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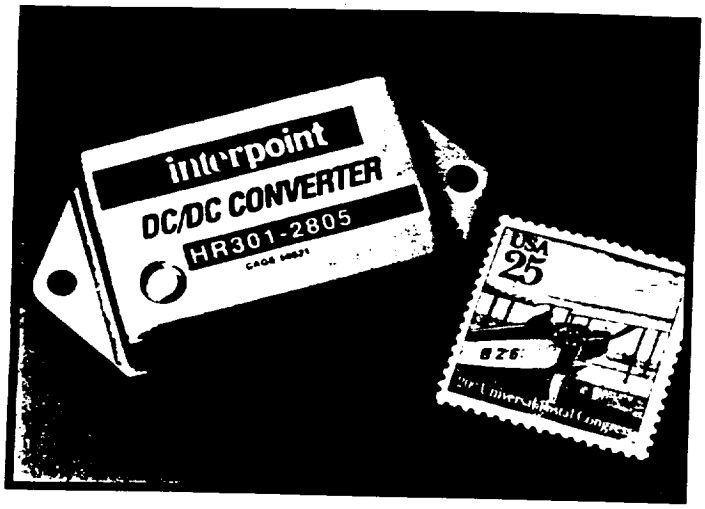
HR300 SERIES DC-DC CONVERTERS



- **Up to 30 watts output power**
- **Less than 3.2 square inches of board area**
- **Hermetically sealed metal case**
- **Short circuit protected**
- **Up to 86% typical efficiency**
- **18 to 36 Vdc input range**
- **Single or dual outputs**
- **Low profile (1/2 inch max.)**

HR300™ dc-dc converters combine the small size and high reliability of hybrid-based components, the high efficiency of switching regulators, and the isolation, regulation, and low noise characteristics of linear regulators.

SMALL SIZE AND HIGH RELIABILITY

HR300 dc-dc converters use thick-film hybrid manufacturing techniques for smaller size, lighter weight and higher reliability than converters produced with other circuit techniques. With a footprint of less than 3.2 square inches and a 0.5 inch maximum height, the HR300 converters reach power densities up to 22 watts per cubic inch.

The HR300 parts use the same manufacturing procedures and quality controls that Interpoint applies to converters built for aerospace and military applications. The converters are hermetically sealed in metal packages that are guaranteed a maximum leak rate of 10^{-3} atm-cc/sec. 24-hour burn-in at maximum operating temperature and 100% electrical testing are standard.

HIGH PERFORMANCE

HR300 converters utilize a constant frequency pulse-width modulated switching regulator design operating in the forward mode with a clock switching frequency of 240 to 300 kHz. Isolation is achieved through the use of a transformer in the forward power circuit and an optocoupler in the feedback control loop. The full load output power of 30 watts is available over the entire 18 to 36 Vdc input range. On dual output models, up to 90% of full power is available from either output up to a combined total of 30 watts.

The HR300's high efficiency is maintained over the entire input voltage range and from approximately 25% of full load to full load (see typical efficiency curves).

Short circuit protection is provided through foldback current limiting. When the output current reaches approximately 125% of the full rated load, the output voltage begins to reduce to protect the converter. The converter can sustain a true short circuit condition indefinitely. The HR300's flanged case facilitates removal of heat and provides for mechanically secure mounting. If full power operation or indefinite short circuit protection is a system requirement, the HR300 converter should be mounted with an efficient heat sink in contact with the mounting flange.

Internal filters in all HR300 converters provide low noise on both the input and outputs. On HR301 models, two-section L-C filters limit output ripple voltage and reflected input ripple current. On HR302 models, single-section L-C filters perform the same function.

For maximum output regulation, the HR301-2805 is provided with external output voltage remote sense pins. Connecting the remote sense pins to the load provides a four-terminal voltage mode which eliminates the adverse effects of line resistance voltage drops. Remote sense pins may be left unconnected, but see cautions in this data sheet. For normal operation, remote sense pins should be connected to the respective output pins.

OUTPUT INHIBIT

An inhibit is provided to allow a logic input to shut down the converter. An open circuit on the inhibit pin (pin 2) allows normal operation. A connection between the inhibit pin and the input common (pin 10) disables the internal oscillator, shutting down the output. The inhibit pin has an open circuit voltage of 11 to 16 Vdc. In the inhibit mode, approximately 1 mA must be sunk. An active low open collector is required to activate the inhibit function.

10301 Willows Road, P.O. Box 97005, Redmond, WA 98073-9705
TEL: (206) 882-3100 TEL: (800) 822-8782 FAX: (206) 882-1990

CHARACTERISTICS: Tcase = 25°C, V_{IN} = 28 Vdc unless otherwise specified.

CLOCK FREQUENCY = 240 to 300 kHz
I/O ISOLATION = 100 megohm minimum at 500 Vdc
OPERATING TEMPERATURE = -40°C to 85°C
TRANSIENT PROTECTION: Up to 50 Vdc for 50 m-sec.

BURN-IN: 24 hrs. at 85°C
HERMETICITY: Leak rate less than 1 x 10^{-3} atm-cc/sec
CASE & PIN MATERIAL: Cold rolled steel with fused tin finish

HR301-2850, HR301-2812, HR301-2815 DC-DC CONVERTERS

PARAMETER	CONDITIONS	HR301-2805			HR301-2812			HR301-2815			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT VOLTAGE	Tcase = -40°C to +85°C	19	—	36	18	—	36	18	—	36	Vdc
INPUT CURRENT	NO LOAD	—	15	—	—	20	—	—	20	—	mA
OUTPUT VOLTAGE		4.95	5.0	5.05	11.88	12.0	12.12	14.85	15.0	15.15	Vdc
OUTPUT CURRENT	V_{IN} = min. to 36 Vdc	—	—	6.0	—	—	2.5	—	—	2.0	A
OUTPUT POWER	Tc = -40°C to +85°C	—	—	30.0	—	—	30.0	—	—	30.0	watts
EFFICIENCY	Po = 30W Rated Load	79	82	—	80	84	—	82	86	—	%
LINE 1/ REGULATION	Po = 30W V_{IN} = min. to 36 Vdc	—	7	25	—	10	40	—	10	40	mV
LOAD 1/ REGULATION	Po = 0 to 30W	—	5	25	—	10	40	—	10	40	mV
OUTPUT RIPPLE VOLTAGE	FULL LOAD BW ≤ 2 MHz	—	30	60	—	30	70	—	30	75	mVp-p
INPUT RIPPLE CURRENT	FULL LOAD BW ≤ 2 MHz	—	5	15	—	10	25	—	10	25	mAp-p
STARTUP 2/ TIME	FULL LOAD	—	15	—	—	30	—	—	40	—	msec
STARTUP OVERSHOOT	FULL LOAD	—	500	—	—	1200	—	—	1500	—	mV
INPUT/OUTPUT CAPACITANCE		—	80	—	—	80	—	—	80	—	pF
INHIBIT PIN OPEN CKT V	Tcase = 25°C	11	—	16	11	—	16	11	—	16	V
INHIBIT PIN CURRENT	UNIT INHIBITED PIN 2 ≤ 1 V	—	1.0	—	—	1.0	—	—	1.0	—	mA
TEMP COEFF OF OUTPUT VOLTAGE	-40°C to +85°C	—	±.01	—	—	±.01	—	—	±.01	—	%/°C
WEIGHT		—	—	60	—	—	60	—	—	60	grams

CAUTION: Permanent damage to the HR301-2805 will result if pin 6 is shorted to ground. Damage may also result if pin 4 or pin 5 is disconnected from the load during operation with the remote sense leads connected to load.

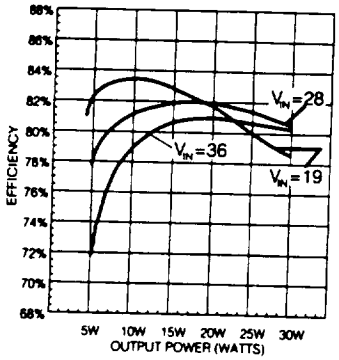
If remote sense pins are not connected to load, output voltage of the HR301-2805 will rise to approximately 6.2 Vdc measured across pins 4 and 5.

NOTES:

1/ With remote sense pins connected to load and no resistance between output pins and load.

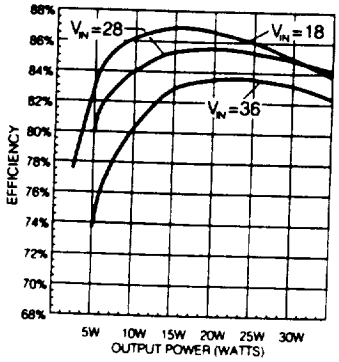
2/ A low output impedance power source is required on the input to realize this startup time. If less than full surge current is available, startup time will be longer.

TYPICAL PERFORMANCE CURVES:



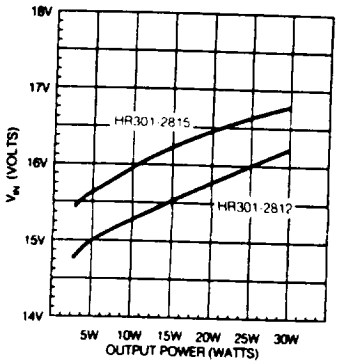
HR301-2805 EFFICIENCY VS LINE AND LOAD

Figure 1



HR301-2812 EFFICIENCY VS LINE AND LOAD

Figure 2



LOWLINE DROPOUT VS LOAD

Figure 3

10301 Willows Road P.O. Box 97005 Redmond, WA 98073-9705 TEL: (206) 882-3100 TEL: (800) 822-8782 FAX: (206) 882-1990

HR302-2812 and HR302-2815 DC-DC CONVERTERS

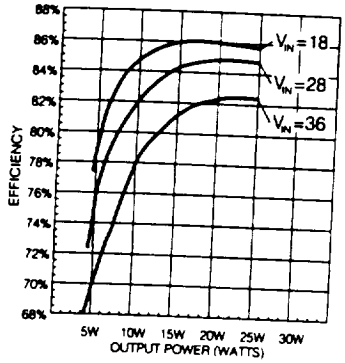
PARAMETER	CONDITIONS	HR302-2805			HR302-2812			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT VOLTAGE	Tcase = -40°C to +85°C	18	—	36	18	—	36	Vdc
INPUT CURRENT	NO LOAD	—	35	50	—	45	60	mA
OUTPUT VOLTAGE	Po = 18 to 36 Vdc	+11.88 -11.88	+12.0 -12.0	+12.12 -12.12	+14.85 14.85	+15.0 -15.0	+15.15 -15.15	Vdc
OUTPUT 1/ CURRENT	V_{IN} = min. to 36 Vdc	—	—	2.5	—	—	2.0	A
OUTPUT POWER	Tcase = -40°C to +85°C	—	—	30.0	—	—	30.0	watts
EFFICIENCY	Po = Max Rated Load	80	84	—	81	85	—	%
LINE REGULATION	Po = 30W V_{IN} = 18 to 36 Vdc	—	10	30	—	10	40	mV
LOAD REGULATION	Po = 0 to 30W	—	20	60	—	20	60	mV
OUTPUT RIPPLE VOLTAGE	FULL LOAD BW ≤ 2 MHz	—	50	90	—	50	90	mVp-p
INPUT RIPPLE CURRENT	FULL LOAD BW ≤ 2 MHz	—	15	60	—	15	60	mAp-p
STARTUP 2/ TIME	FULL LOAD	—	60	—	—	60	—	msec
STARTUP OVERSHOOT	FULL LOAD	—	1500	—	—	1500	—	mV
INPUT/OUTPUT CAPACITANCE		—	—	70	—	—	60	pF
INHIBIT PIN OPEN CKT V	Tcase = 25°C	8	—	12	10	—	14	V
CROSS REGULATION	+Po = 3W (+) Po = 3W to 27W	—	2.5	3.5	—	2.2	3.2	%
	+Po = 3W (-) Po = 3W to 27W	—	2.5	3.5	—	2.2	3.2	%
TEMP COEFF OF OUTPUT VOLTAGE	-40°C to +85°C	—	±.01	—	—	±.01	—	%/°C
WEIGHT		—	—	60	—	—	60	grams

NOTES:

1/ Up to 90% full power is available from either output providing the total output power does not exceed 30 watts.

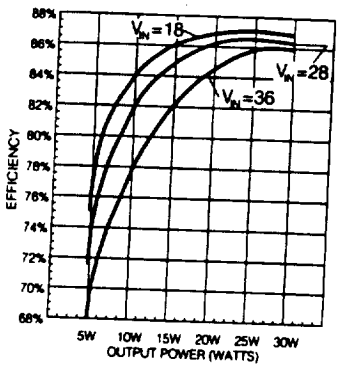
2/ A low output impedance power source is required on the input to realize this startup time. If less than full surge current is available, startup time will be longer.

TYPICAL PERFORMANCE CURVES:



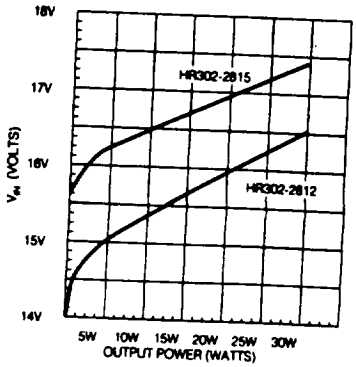
HR302-2812 EFFICIENCY VS LINE AND LOAD

Figure 4



HR302-2815 EFFICIENCY VS LINE AND LOAD

Figure 5

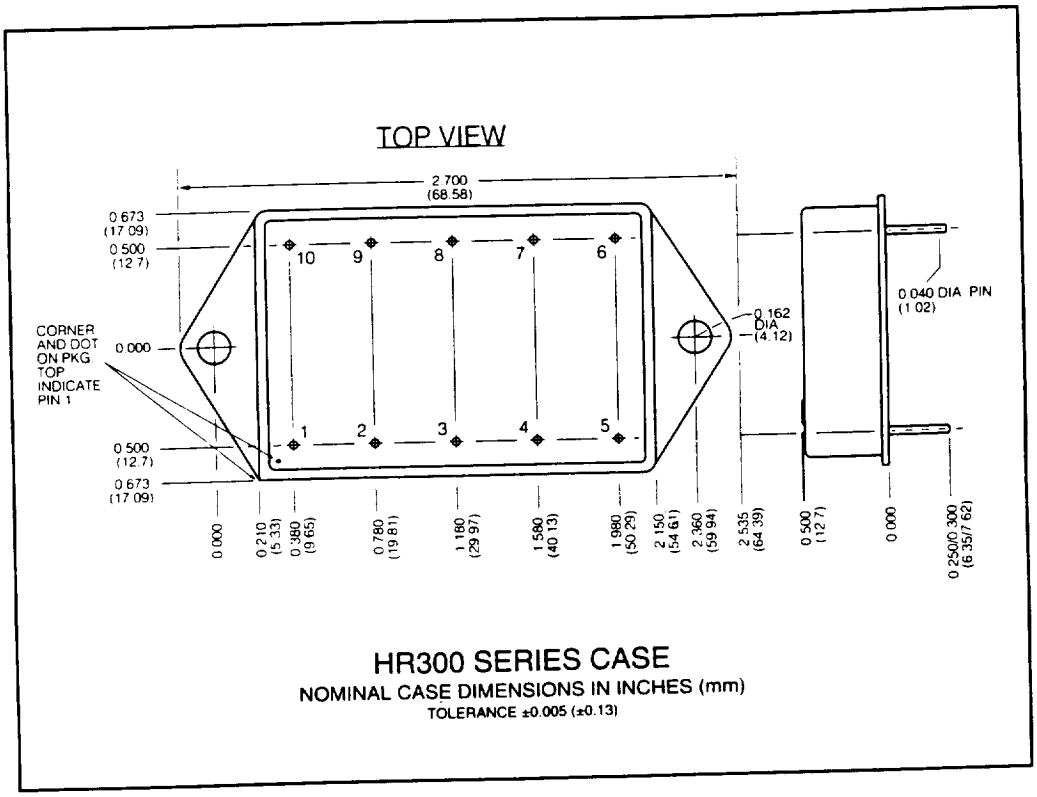


LOWLINE DROPOUT VS. LOAD

Figure 6

10301 Willows Road P.O. Box 97005 Redmond, WA 98073-9705 TEL: (206) 882-3100 TEL: (800) 822-8782 FAX: (206) 882-1990

METAL HERMETIC 10-PIN DIP PACKAGE



HR300 SERIES CASE
NOMINAL CASE DIMENSIONS IN INCHES (mm)
TOLERANCE ±0.005 (±0.13)

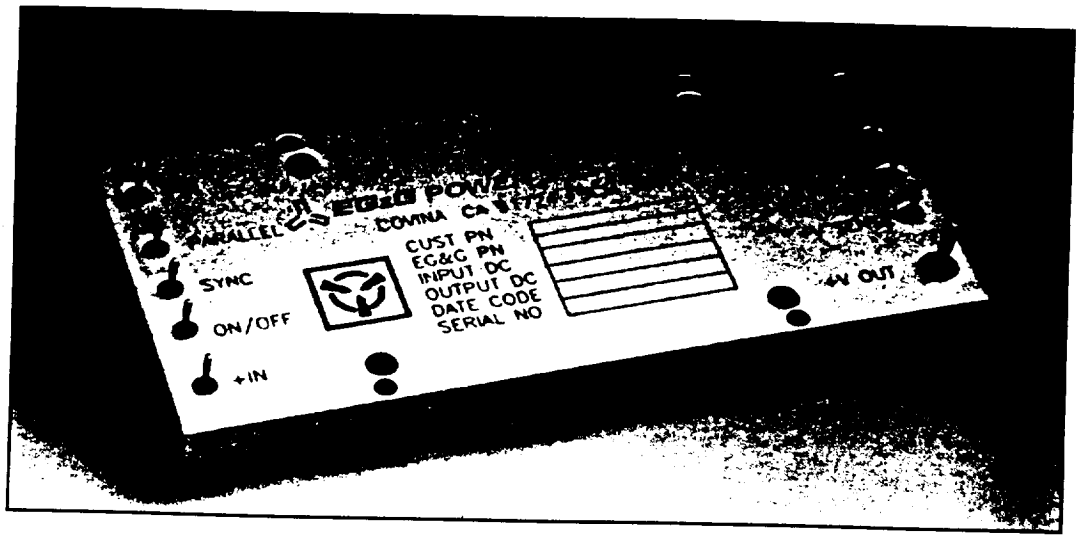
DESIGNATION	HR301-2805, 2812 2815 PIN NO.	HR302-2812 2815 PIN NO.
Positive input	1	1
Inhibit	2	8
Neg. remote sense (301-2805 only)	3	N/A
Output common	4	4
Positive output	5	3
Pos. remote sense (301-2805 only)	6	N/A
Case ground	7	7
Negative output	N/A	5
Input common	10	9, 10
All Other Pins — No Connection		

CAUTION: Heat from reflow or wave soldering may damage this converter. Solder pins individually with heat application NOT exceeding 300°C for 10 seconds per pin.

EG&G Data Sheet

Ruggedized DC-DC Converters

Mil Performance at Non-Mil Prices



LC810 Series

- Up to 200W, Single, Dual, Triple
- MIL STD 704D Wide Input Ranges
- MIL STD 810 Environments
- NAVMAT Derating
- NAVMAT ESS
- Custom Inputs & Outputs Available
- Pin-for-Pin Compatible with EG&G Full MIL Converters
- Fixed Frequency/Parallelable/Synchronous Operation
- Baseplate Temperature Range of -45°C - +85°C
- On/Off Control

EG&G POWER SYSTEMS, INC.

1330 E. Cypress St., Covina, CA 91724-2198
(818) 967-9521 FAX (818) 967-3151

High Density Power Converter (HDPC-2)

Military DC-DC Converter

125W (NOMINAL) AND UP TO 30 W/CU. IN. @ 85° C BASEPLATE

1,2, & 3 Output Models

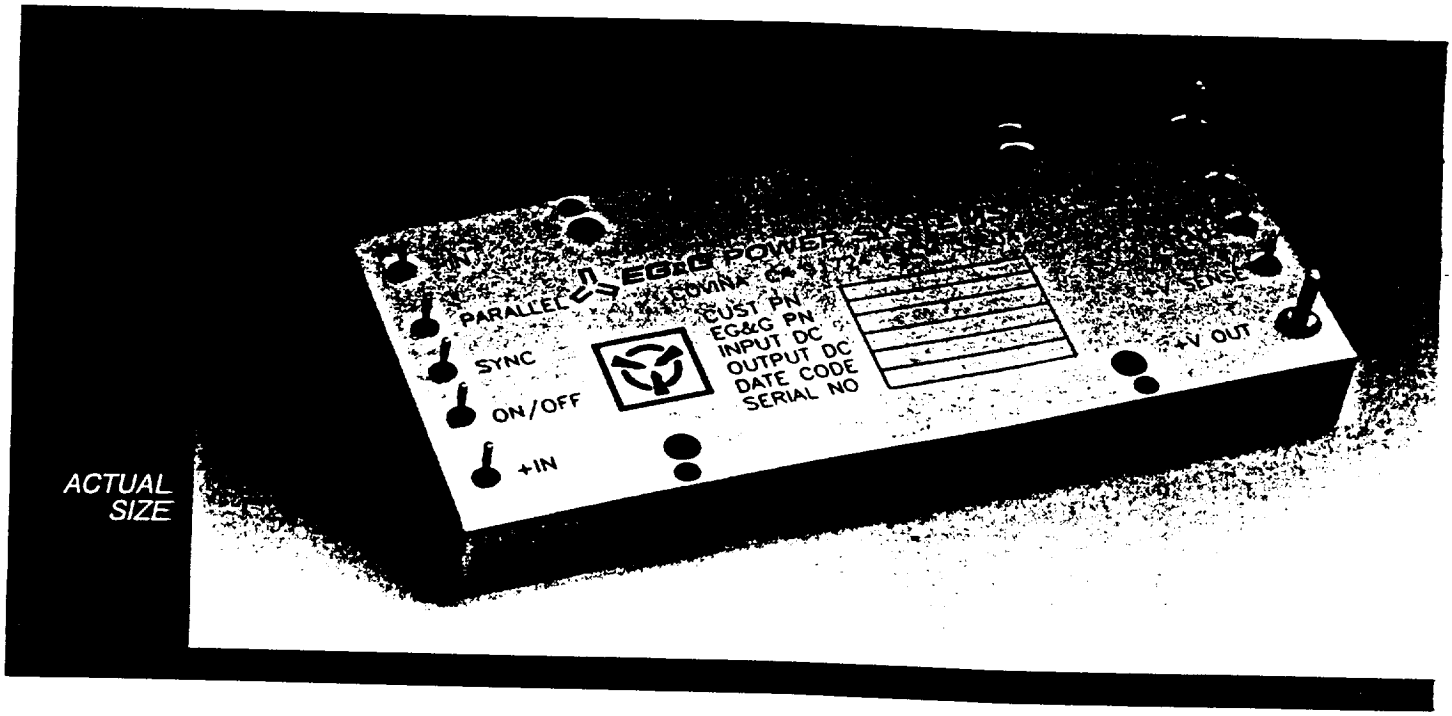
Standard Military DC Inputs: 28 VDC and 270 VDC

Typical DC Outputs: 5 VDC to 40 VDC

EG&G Power Systems' DC-DC Converters, available in 1, 2 and 3 output configurations, offer military electronics designers outstanding flexibility in DC power distribution. The converters are small and lightweight, facilitating decentralized packaging. They can be PC-Board mounted near the load or installed in a centrally located, multiple output power supply. Their high-efficiency operation conserves power and simplifies thermal design, while delivering tightly regulated DC power under dynamic line and load conditions. Additional tailoring can be achieved through N+1 redundancy, paralleling and external synchronization. Consult one of our engineers in the Business Development Department for specification details applicable to your specific requirements. Tel: (818) 967-9521

FEATURES

- High reliability
- High efficiency
- Fixed frequency switching
- MIL-SPEC Design, Workmanship, Environments
- Remote sense (Main output)
- ±5% Voltage adjust
- External sync capability
- Remote ON/OFF
- Parallelable
- Full-Mil components
- Nuclear hardened
- NAVMAT (Derating)
- NAVMAT ESS
- EMI Filter (Additional filtering required for full MIL-STD 461 compliance)
- Weight less than .35 lbs.
- MTBF @ 100W single output configuration
  - 315,000 hour MTBF +65° C baseplate (Naval sheltered)
  - 82,000 hour MTBF +65° C baseplate (Airborne, uninhabited, fighter)
  - 175,000 hour MTBF +65° C baseplate (Ground, mobile)
  - 2,589,000 hour MTBF +25° C baseplase (Ground, benign)
- Custom inputs and outputs available



EG&G POWER SYSTEMS, INC.

AT&T Data Sheet

Advance Data Sheet
March 1994

AT&T Microelectronics

JC050-Series Power Modules: 18 Vdc to 36 Vdc Input; 50 W

The JC050-Series Power Modules use advanced, surface-mount technology and deliver high-quality, efficient, and compact dc-dc conversion.

Features

- Small size: 2.40 in. x 2.28 in. x 0.50 in.
- High power density (37 W/in.^{3})
- High efficiency: 84% typical
- Low output noise
- Constant frequency
- Industry-standard pinout
- Metal baseplate
- 2:1 input voltage range
- Remote sense
- Remote on/off
- Adjustable output voltage: 60% to 110% of $V_{O,\,nom}$
- Case ground pin

Options

- Choice of on/off configuration
- Heat sink available for extended operation

Applications

- Distributed power architectures
- Workstations
- EDP equipment
- Telecommunications

Description

The JC050-Series Power Modules are dc-dc converters that operate over an input voltage range of 18 Vdc to 36 Vdc and provide precisely regulated dc outputs. The outputs are fully isolated from the inputs, allowing versatile polarity configurations and grounding connections. The modules have maximum power ratings of 100 W at a typical full-load efficiency of 84%.

The sealed modules offer a metal baseplate for excellent thermal performance. Threaded-through holes are provided to allow easy mounting or addition of a heat sink for high-temperature applications.

The standard feature set includes remote sensing, output trim, and remote on/off for convenient flexibility in distributed power applications.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Input Voltage Continuous	V_I	—	50	V
I/O Isolation Voltage	—	—	500	Vdc
Operating Case Temperature	T_C	−40	100	°C
Storage Temperature	T_{stg}	−40	110	°C

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions.

Table 1. Input Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	V_I	18	28	36	Vdc
Maximum Input Current (V_I = 0 V to 36 V; $I_O = I_{O,max}$)	$I_{I,max}$	—	—	6.0	A
Inrush Transient	i^2t	—	—	2.0	A^2s
Input Reflected-ripple Current, Peak-to-peak (5 Hz to 20 MHz, 12 µH source impedance; T_C = 25 °C; see Figure 1 and Design Considerations section.)	—	—	—	150	mA p-p
Input Ripple Rejection (120 Hz)	—	—	60	—	dB

Fusing Considerations

CAUTION: This power module is not internally fused. An input line fuse must always be used.

This encapsulated power module can be used in a wide variety of applications, ranging from simple stand-alone operation to an integrated part of a sophisticated power architecture. To preserve maximum flexibility, internal fusing is not included; however, to achieve maximum safety and system protection, always use an input line fuse. To aid in the proper fuse selection for the given application, information on inrush and maximum dc input current is provided. Refer to the fuse manufacturer's data for further information.

Electrical Specifications (continued)

Table 2. Output Specifications

Parameter	Device	Symbol	Min	Typ	Max	Unit
Output Voltage	JC050A	V_O	4.85	—	5.15	Vdc
(Over all operating input voltage,	JC050B	V_O	11.64	—	12.36	Vdc
resistive load, and temperature	JC050C	V_O	14.55	—	15.45	Vdc
conditions until end of life.)	JC050F	V_O	3.20	—	3.40	Vdc
Output Voltage Set Point	JC050A	$V_{O,set}$	4.92	5.0	5.08	Vdc
(V_I = 28 V; I_O = $I_{O,max}$; T_C = 25 °C)	JC050B	$V_{O,set}$	11.82	12.0	12.18	Vdc
	JC050C	$V_{O,set}$	14.77	15.0	15.23	Vdc
	JC050F	$V_{O,set}$	3.25	3.3	3.35	Vdc
Output Regulation:						
Line (V_I = 18 V to 36 V)	all	—	—	0.01	0.1	%
Load (I_O = $I_{O,min}$ to $I_{O,max}$)	all	—	—	0.05	0.2	%
Temperature	JC050A, F	—	—	15	50	mV
(T_C = −40 °C to +100 °C)	JC050B, C	—	—	50	150	mV
Output Ripple and Noise						
(See Figure 2.):						
RMS	JC050A, F	—	—	—	40	mV rms
	JC050B	—	—	—	50	mV rms
	JC050C	—	—	—	60	mV rms
Peak-to-peak (5 Hz to 20 MHz)	JC050A, F	—	—	—	150	mV p-p
	JC050B	—	—	—	200	mV p-p
	JC050C	—	—	—	250	mV p-p
Output Current	JC050A, F	I_O	0.5	—	10	A
(At I_O < $I_{O,min}$, the modules may	JC050B	I_O	0.3	—	4.2	A
exceed output ripple specifications.)	JC050C	I_O	0.3	—	3.3	A
Output Current-limit Inception:	JC050A, F	—	—	12	—	A
V_O = 90% of $V_{O,nom}$	JC050B	—	—	5.5	—	A
	JC050C	—	—	4.0	—	A
Output Short-circuit Current	JC050A, F	—	—	TBD	—	A
(V_O = 250 mV)	JC050B	—	—	TBD	—	A
	JC050C	—	—	TBD	—	A
Efficiency (V_I = 28 V; I_O = $I_{O,max}$;	JC050F	η	77	79	—	%
T_C = 70 °C; see Figure 3.)	JC050A	η	80	82	—	%
	JC050B, C	η	82	84	—	%
Dynamic Response						
($\Delta I_O/\Delta t$ = 1 A/10 µs, V_I = 28 V,						
T_C = 25 °C):						
Load Change from I_O = 50% to 75%						
of $I_{O,max}$:						
Peak Deviation	all	—	—	2	—	$\%V_{O,set}$
Settling Time (V_O < 10% of peak	all	—	—	0.3	—	ms
deviation)						
Load Change from I_O = 50% to 25%						
of $I_{O,max}$:						
Peak Deviation	all	—	—	2	—	$\%V_{O,set}$
Settling Time (V_O < 10% of peak	all	—	—	0.3	—	ms
deviation)						

Electrical Specifications (continued)

Table 3. Isolation Specifications

Parameter	Min	Typ	Max	Unit
Isolation Capacitance	—	2500	—	pF
Isolation Resistance	10	—	—	MΩ

General Specifications

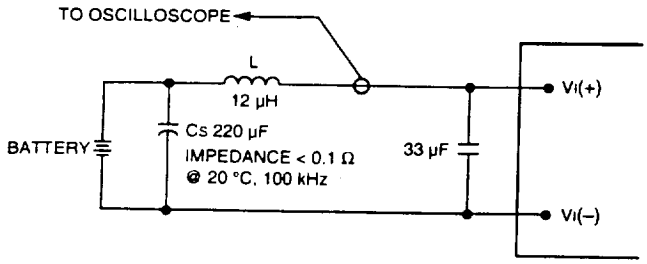
Parameter	Min	Typ	Max	Unit
Calculated MTBF (I_O = 80% of $I_{O,max}$; T_C = 40 °C)		2,600,000		hours
Weight	—	—	35 (100)	oz. (g)

Feature Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. See Feature Descriptions and Design Considerations for further information.

Parameter	Device	Symbol	Min	Typ	Max	Unit
Remote On/Off (V_I = 18 V to 36 V; open collector or equivalent compatible; signal referenced to $V_I(-)$ terminal. See Figure 8 and Feature Descriptions.):						
Module Specifications:						
On/Off Current—Logic Low	all	$I_{on/off}$	—	—	1.0	mA
On/Off Voltage:						
Logic Low	all	$V_{on/off}$	0	—	1.2	V
Logic High ($I_{on/off}$ = 0)	all	$V_{on/off}$	—	—	15	V
Open Collector Switch Specifications:						
Leakage Current During Logic High ($V_{on/off}$ = 10 V)	all	$I_{on/off}$	—	—	50	µA
Output Low Voltage During Logic Low ($I_{on/off}$ = 1 mA)	all	$V_{on/off}$	—	—	1.2	V
Turn-on Time (@ 80% of $I_{O,max}$; T_C = 25 °C; V_O within ±1% of steady state)	all	—	—	20	—	ms
Output Voltage Sense Range	all	—	0.5	—	—	V
Output Voltage Set Point Adjustment Range (See Feature Descriptions.)	all	—	60	—	110	%$V_{O,nom}$
Output Overvoltage Clamp	JC050A	$V_{O,clamp}$	5.6	—	7.0	V
	JC050B	$V_{O,clamp}$	13.5	—	16.0	V
	JC050C	$V_{O,clamp}$	17.0	—	20.0	V
	JC050F	$V_{O,clamp}$	4.0	—	5.0	V

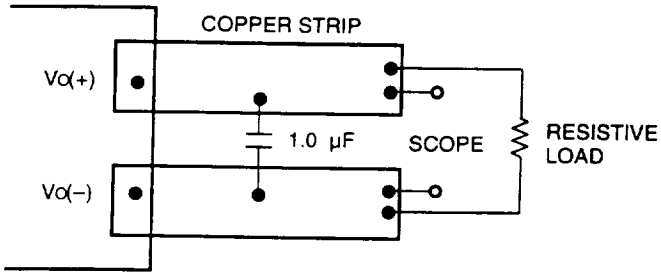
Test Configurations



8-203 (C)

Note: Input reflected-ripple current is measured with a simulated source impedance of 12 µH. Capacitor Cs offsets possible battery impedance. Current is measured at the input of the module.

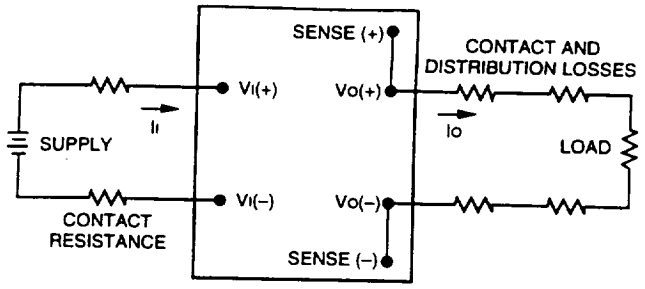
Figure 1. Input Reflected-Ripple Test Setup



8-513 (C)

Note: Use a 1.0 µF ceramic capacitor. Scope measurement should be made using a BNC socket. Position the load between 2 in. and 3 in. from the module.

Figure 2. Peak-to-Peak Output Noise Measurement Test Setup



8-749 (C)

Note: All measurements are taken at the module terminals. When socketing, place Kelvin connections at module terminals to avoid measurement errors due to socket contact resistance.

$$\eta = \left(\frac{[Vo(+) - Vo(-)]\, Io}{[Vi(+) - Vi(-)]\, Ii}\right) \times 100$$

Figure 3. Output Voltage and Efficiency Measurement Test Setup

Design Considerations

Input Source Impedance

The power module should be connected to a low ac-impedance input source. Highly inductive source impedances can affect the stability of the power module. For the test configuration in Figure 1, a 33 µF electrolytic capacitor (ESR < 0.7 Ω at 100 kHz) mounted close to the power module helps ensure stability of the unit. For other highly inductive source impedances, consult the factory for further application guidelines.

Feature Descriptions

Output Overvoltage Clamp

The output overvoltage clamp consists of control circuitry, which is independent of the primary regulation loop, that monitors the voltage on the output terminals. The control loop of the clamp has a higher voltage set point than the primary loop (see Feature Specifications table). In a fault condition, the overvoltage clamp helps ensure that the output voltage does not exceed $V_{O,\,clamp,\,max}$. This provides a redundant voltage-control that reduces the risk of output overvoltage.

Current Limit

To provide protection in a fault (output overload) condition, the unit is equipped with internal current-limiting circuitry and can endure current limiting for an unlimited duration. At the point of current-limit inception, the unit shifts from voltage control to current control. If the output voltage is pulled very low during a severe fault, the current-limit circuit can exhibit either foldback or tailout characteristics (output-current decrease or increase). The unit operates normally once the output current is brought back into its specified range.

Output Voltage Trim

Output voltage trim allows the user to increase or decrease the output voltage set point of a module. This is accomplished by connecting an external resistor between the TRIM pin and either the SENSE(+) or SENSE(–) pins. With an external resistor between the TRIM and SENSE(–) pins ($R_{adj\text{-}down}$), the output voltage set point ($V_{O,\,adj}$) decreases (see Figure 4). The following equation determines the required external resistor value to obtain a percentage output voltage change of $\Delta\%$.

$$R_{adj\text{-}down} = \left(\frac{100}{\Delta\%} - 2\right) \text{k}\Omega$$

The test results for this configuration are displayed in Figure 5. This figure applies to all output voltages.

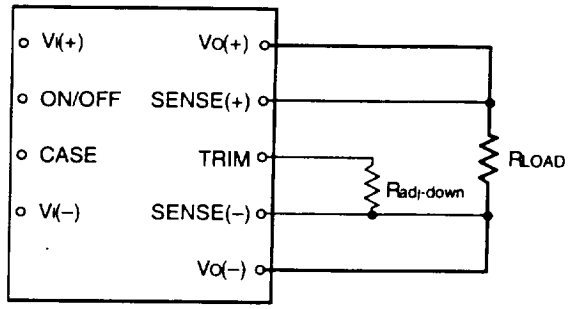
With an external resistor connected between the TRIM and SENSE(+) pins ($R_{adj\text{-}up}$), the output voltage set point ($V_{O,\,adj}$) increases (see Figure 6).

The following equation determines the required external resistor value to obtain a percentage output voltage change of $\Delta\%$.

$$R_{adj\text{-}up} = \left(\frac{V_O\,(100 + \Delta\%)}{1.225\Delta\%} - \frac{(100 + 2\Delta\%)}{\Delta\%}\right) \text{k}\Omega$$

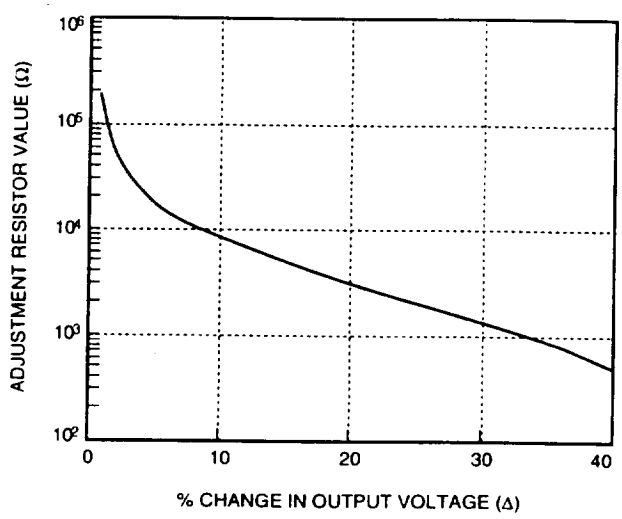
The test results for this configuration are displayed in Figure 7.

The combination of the output voltage adjustment and sense range and the output voltage given in the Feature Specifications table cannot exceed 110% of the nominal output voltage between the Vo(+) and Vo(–) terminals.



8-748 (C)

Figure 4. Circuit Configuration to Decrease Output Voltage

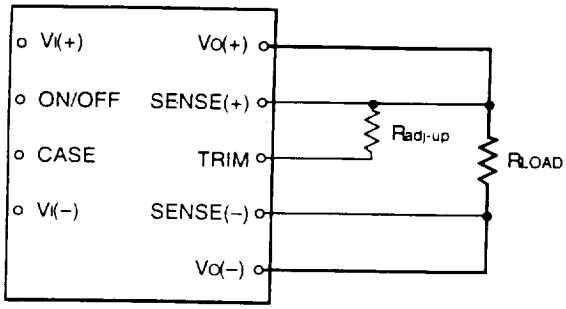


8-879 (C)

Figure 5. Resistor Selection for Decreased Output Voltage

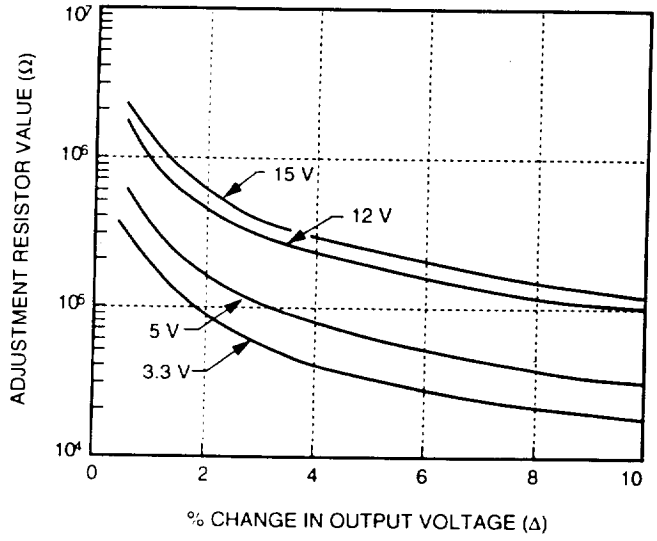
Feature Descriptions (continued)

Output Voltage Trim (continued)



8-715 (C)

Figure 6. Circuit Configuration to Increase Output Voltage



8-880 (C)

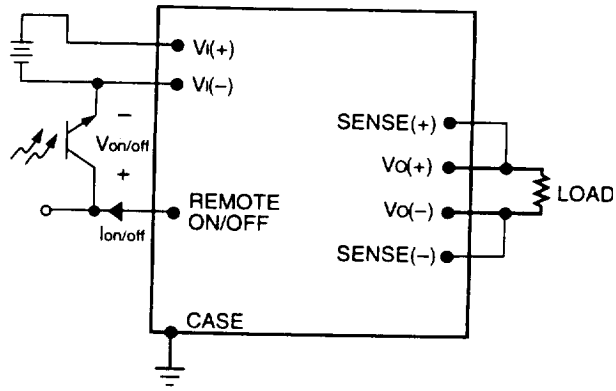
Figure 7. Resistor Selection for Increased Output Voltage

Remote On/Off

Two remote on/off options are available. Positive logic remote on/off turns the module on during a logic high voltage on the remote on/off pin, and off during a logic low. Negative logic remote on/off turns the module off during a logic high and on during a logic low. Negative logic (code suffix of 1) is the factory-preferred configuration.

To turn the power module on and off, the user must supply a switch to control the voltage between the on/off terminal and the $V_{I}(-)$ terminal ($V_{on/off}$). The switch can be an open collector or equivalent (see Figure 8). A logic low is $V_{on/off}$ = 0 V to 1.2 V. The maximum $I_{on/off}$ during a logic low is 1 mA. The switch should maintain a logic low voltage while sinking 1 mA.

During a logic high, the maximum $V_{on/off}$ generated by the power module is 15 V. The maximum allowable leakage current of the switch at $V_{on/off}$ = 15 V is 50 µA.



8-758 (C)

Figure 8. Remote On/Off Implementation

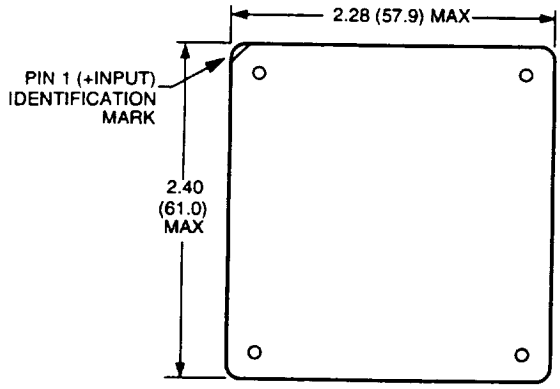
Outline Diagram

Dimensions are in inches and (millimeters).

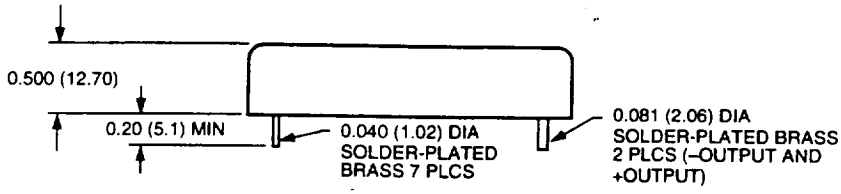
Copper paths must not be routed beneath the power module standoffs.

Tolerances: x.xx in. ± 0.02 in. (0.5 mm), x.xxx in. ± 0.010 in. (0.25 mm)

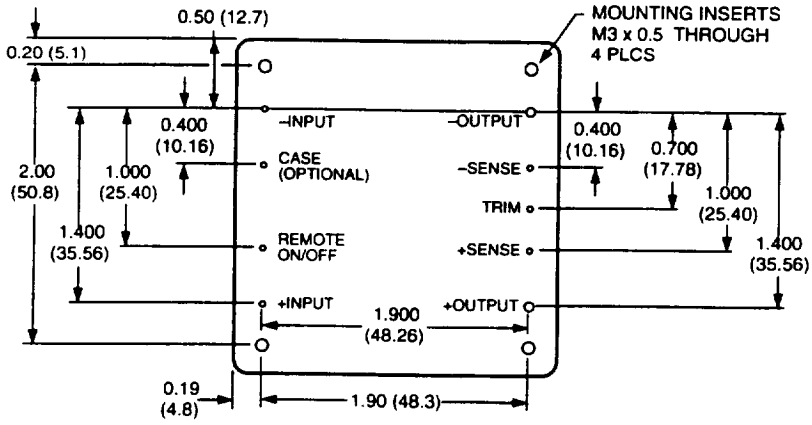
Top View



Side View



Bottom View

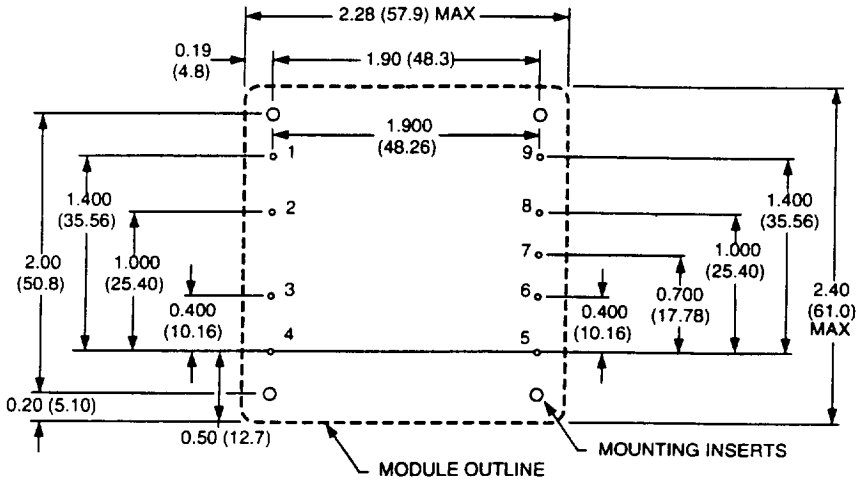


8-881 (C)

Recommended Hole Pattern

Component-side footprint.

Dimensions are in inches and (millimeters).



8-881 (C)

For additional information, contact your AT&T Account Manager or the following:

U.S.A.: AT&T Microelectronics, Dept. AL-500404200, 555 Union Boulevard, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)

ASIA PACIFIC: AT&T Microelectronics Asia/Pacific, 14 Science Park Drive, #03-02A/04 The Maxwell, Singapore 0511
Tel. (65) 778-8833, FAX (65) 777-7495

JAPAN: AT&T Microelectronics, AT&T Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3-5421-1600, FAX (81) 3-5421-1700

For data requests in Europe:

AT&T DATALINE: **Tel. (44) 732 742 999**, FAX (44) 732 741 221

For technical inquiries in Europe:

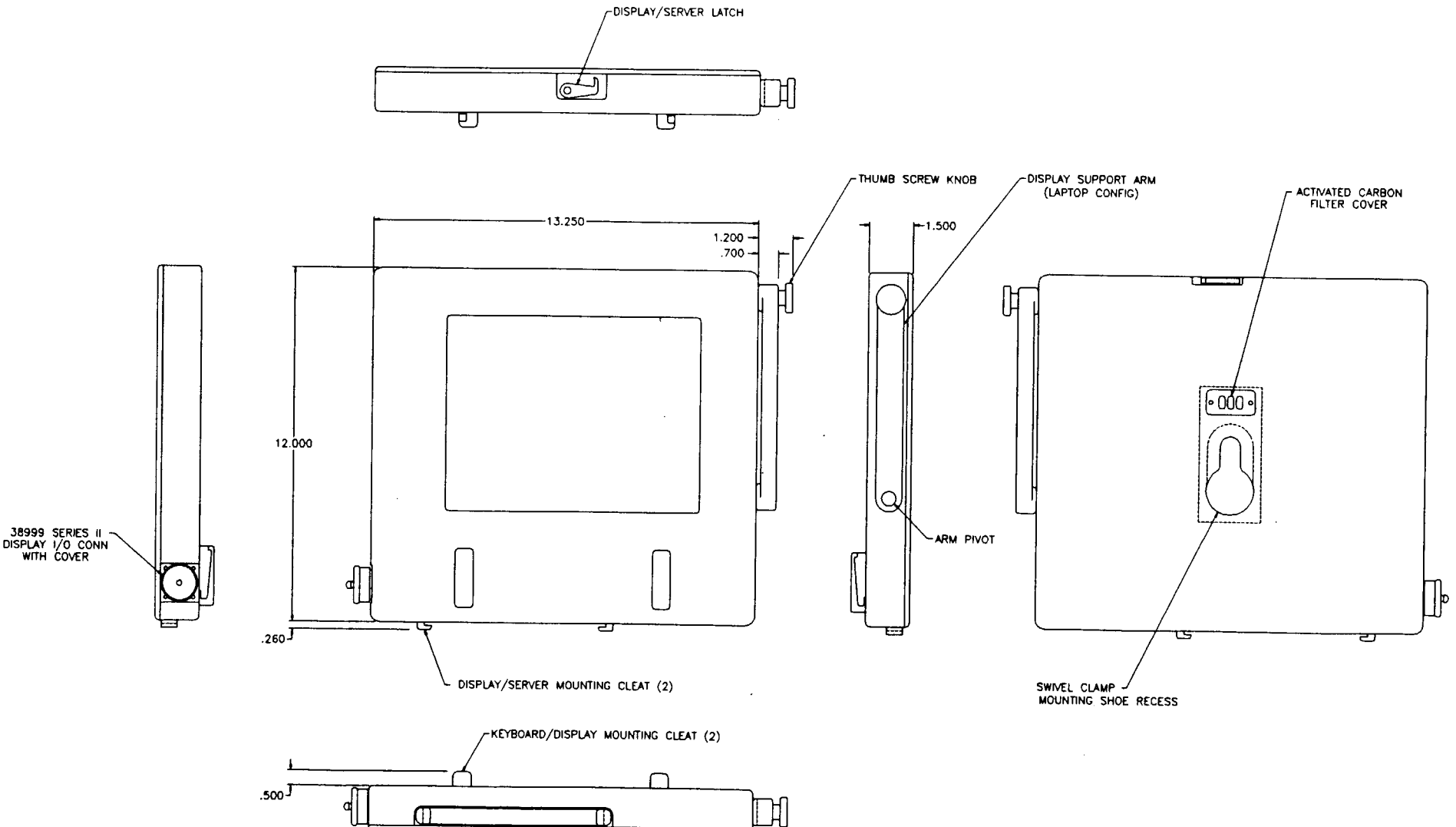
CENTRAL EUROPE: **(49) 89 95086 0** (Munich), NORTHERN EUROPE: **(44) 344 487 111** (Bracknell UK),
FRANCE: **(33) 1 47 67 47 67** (Paris), SOUTHERN EUROPE: **(39) 2 6601 1800** (Milan) or **(34) 1 807 1700** (Madrid)

March 1994
DS94-049EPS

AT&T
Microelectronics

APPENDIX 2

DISPLAY MODULE DATA SHEETS

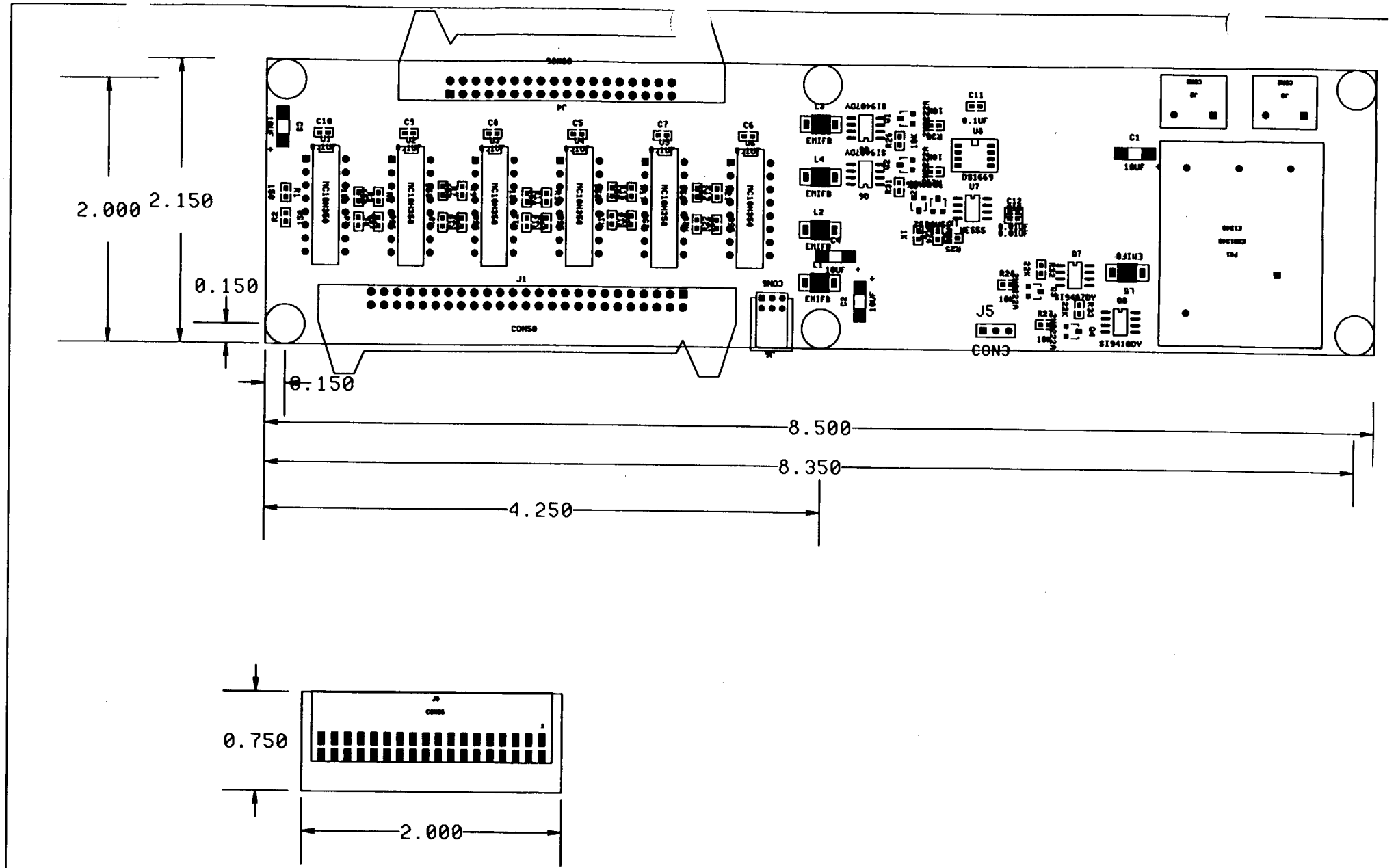


DISPLAY ASSEMBLY

950424

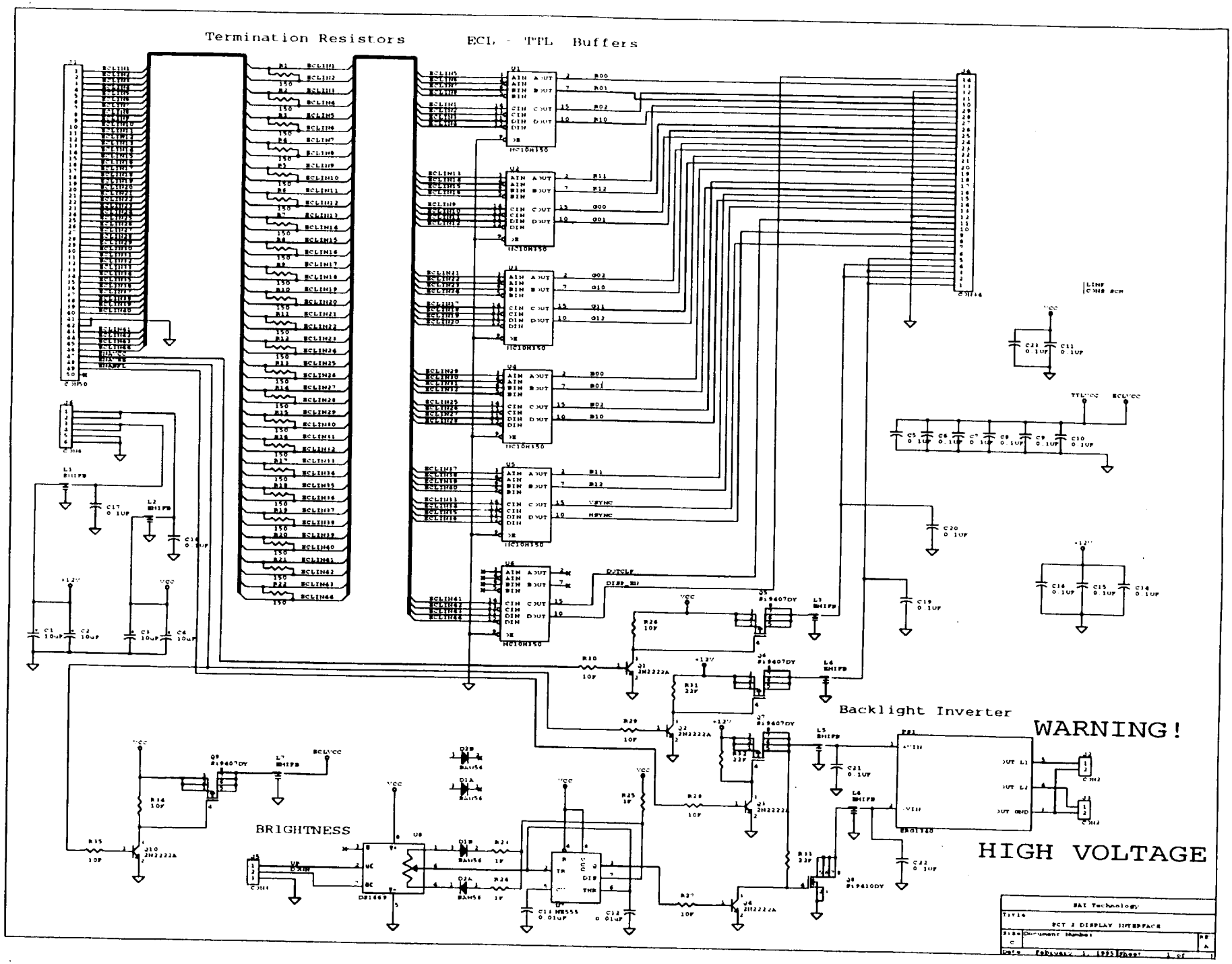
SAIC An Employee-Owned Company

SAI Technology
A Division of Science Applications International Corporation



DISPLAY PWA BOARD LAYOUT

Display Schematic


Termination Resistors
ECL - TTL Buffers
Backlight Inverter
WARNING!
HIGH VOLTAGE
BRIGHTNESS
BAI Technology
PCT 2 DISPLAY INTERFACE
Document Number
February 1, 1995

Display PWA Parts List

BMFSAT FILE
ASSEMBLY 65360-, ASY PWA, PCT II DISPLAY INTERFACE B/M REV...ON DATE - 16FEB95
WITH STANDARD YIELD

REVISION - N/R ECN - NOT REL ECN IMPLEMENTATION DATE - 30NOV94

NOTES:
1. ENDICOTT RESEARCH
2. DIGI -KEY
   701 BROOKS AVE SOUTH
   P.O. BOX 677
   THIEF RIVER FALLS, MN 56701-0677
   (800) 344-4539
3. SEI ELECTRONICS INC
   P.O. BOX 17088
   RALEIGH, NC 27619
   (919)787-2611
4. CAL CHIP
   15 VINCENT CIRCLE
   WARMINSTER, PA 18974
   (215) 672-5500
5. KOA SPEER ELECTRONICS
   BOLICAR DRIVE
   P.O. BOX 547
   BRADFORD, PA 16701

ITEM	PART NUMBER	DESCRIPTION	U/M	REV	QTY	OPT	#	REF DESIGNATOR				
2	ART65361	REF ARTWORK, NEGATIVES AND SOLDER PASTE MASTER	EA		0.000	1						
5	3160003	OPM INK, MARKING, EPOXY BASE, WHITE M43553-II WHT	KT		AR	1						
8	DC-3140-RTV	OPQ CONFORMAL COATING, RTV SILICONE	EA		AR	1						
11	3460000	OPS SOLDER, .025 DIA SN63WRMAP3	LB		AR	1						
14	SN63PRMA	OPS SOLDER PASTE, (25 GRAM SYRINGE)	EA		AR	1						
17	65361-1	PCB PROCESSOR PWB	EA		1.000	1						
18	65362	REF SCHEMATIC DIAGRAM, PROCESSOR	EA		0.000	1						
20	MCH182F104ZK	CAP CAPACITOR CHIP,0.1 UF,25V,+80-20%,CC0603	EA		17.000	1		C10 C17 C22 C8	C11 C18 C23 C9	C14 C19 C5	C15 C20 C6	C16 C21 C7
20	VJ0603U104ZXXAT	CAP CAPACITOR CHIP,0.1 UF,25V,+80-20%,CC0603	EA		7.000	SUB						
20	GMC10Z104M25NT	CAP CAPACITOR,CHIP,0.1UF,25V,+80-20% CC0603	EA		7.000	SUB						
22	TAJ-C-106K016R	CAP CAPACITOR,CHIP,TANT,10UF,16V,10%,TC6032	EA		4.000	1		C1	C2	C3	C4	
22	TCK1D106CT	CAP CAPACITOR,CHIP,TANT,10UF,20V,10%,TC6032	EA		4.000	SUB						
23	MCH182C103KK	CAP CAPACITOR,CHIP,MLC,0.01uF,25V,X7R,+/-10%	EA		2.000	1		C12	C13			
23	GMC10X103K500NT	CAP CAPICITOR,CHIP,MLC,0.01UF,50V,X7R,+/-10%	EA		2.000	SUB						
23	VJ0603Y103KXAAT	CAP CAPACITOR,CHIP,MLC,0.1UF,50V,X7R,+/-10%	EA		2.000	SUB						
30	BAW56	MISC DUAL 1N4148 TYPE, SOT-23, COMMON ANODE	EA		2.000	1		D1	D2			
30	BAW56PH	MISC DUAL 1N4148 TAPE, SOT-23, COMMON ANODE	EA		2.000	SUB						
30	BAW56LT1	DIO DIODE,FAST RECOVERY,DUAL 1N4148 TYPE,SOT-23	EA		2.000	SUB						
35	NFM61R30T472B1	MISC EMI FILTER, SURRFACE MOUNT	EA		7.000	1		L1 L6	L2 L7	L3	L4	L5
35	NFM61R30T472T1M	HDW FILTER,SURFACE MOUNT,4700pF,2A,50VDC NFM61R30T472T1M0057	EA		5.000	SUB						
37	SI9410DY	XTR TRANSISTOR,N-CHANNEL,ENHANCE MODE SO-8,MOSFET	EA		1.000	1		Q8				

REVISION - N/R ECN - NOT REL ECN IMPLEMENTATION DATE - 30NOV94

ITEM	PART NUMBER	DESCRIPTION	U/M	REV	QTY	OPT	#	REF DESIGNATOR				
38	SI9407DY	XTR TRANSISTOR,P-CHANNEL,ENHANCE MODE,SO-8,MOSFET	EA		4.000		1	Q5	Q6	Q7	Q9	
40	SST2222A	XTR TRANSISTOR, 2N2222A SOT23	EA		5.000		1	Q1	Q10	Q2	Q3	Q4
40	KST2222ATR	XTR TRANSISTOR, 2N2222A SOT23	EA		4.000	SUB						
42	DF11-6DP-2DSA	CON CONNECTOR,BATTERY,HEADER,6-PIN,2MM,VERTICAL	EA		1.000		1	J6				
43	QZ-19-A3MYL	CON CONNECTOR, 2 PIN, VERTICLE HI VOLTAGE	EA		2.000		1	J2	J3			
45	TST-117-01-G-D	CON CONNECTOR,34 PIN, VERTICLE SHROUDED HEAD	EA		1.000		1	J4				
47	TST-125-01-G-D	CON CONNECTOR,50 PIN, VERTICLE SHROUDED HEAD	EA		1.000		1	J1				
50	CHF1/16-1002-F	RES RESISTOR, 10K OHM, 1%, RC0603	EA		7.000		1	R26	R27	R28	R29	R30
								R34	R35			
50	RK73H1J1002F	RES RESISTOR, 10K OHM, 1%, RC0603	EA		5.000	SUB						
50	RMC1/16 10K1%TR	RES RESISTOR, 10K OHM, 1%, RC0603	EA		5.000	SUB						
50	RMC1161002FT	RES RESISTOR, CHIP, 10K 1%, RC0603	EA		5.000	SUB						
52	CHF1/16-1001-F	RES RESISTOR,CHIP, 1K OHM, 1%, RC0603	EA		3.000		1	R23	R24	R25		
52	RK73H1J1001F	RES RESISTOR, CHIP, 1K OHM, 1%, RC0603	EA		3.000	SUB						
52	RMC1/16 1K 1%TR	RES RESISTOR,CHIP, 1K OHM, 1%, RC0603	EA		3.000	SUB						
52	RMC1161001FT	RES RESISTOR,CHIP,1K 1% RC0603	EA		3.000	SUB						
54	CHF1/16-2212-F	RES RESISTOR,CHIP, 22.1K OHM, 1%, RC0603	EA		3.000		1	R31	R32	R33		
54	RK73H1J2212F	RES RESISTOR,CHIP, 22.1K OHM, 1%, RC0603	EA		3.000	SUB						
54	RMC1/16 22.1K1%	RES RESISTOR, CHIP, 22.1K 1%, RC0603 RMC1/16 22.1K1%TR	EA		3.000	SUB						
54	RMC1162212FT	RES RESISTOR,CHIP, 22.1K 1%, RC0603	EA		3.000	SUB						
56	CHF1/16-1500-F	RES RESISTOR, CHIP, 150 OHM, 1%, RC0603	EA		22.000		1	R1	R10	R11	R12	R13
								R14	R15	R16	R17	R18
								R19	R2	R20	R21	R22
								R3	R4	R5	R6	R7
								R8	R9			
56	RK73H131500F	RES RESISTOR, CHIP, 150 OHM, 1%, RC0603	EA		22.000	SUB						
56	RMC1161500FT	RES RESISTOR,CHIP, 150 OHM, 1%, RC0603	EA		22.000	SUB						
56	RMC1/16 150 1%	RES RESISTOR, CHIP, 150 OHM, 1%, RC0603 RMC1/16 150 1%TR	EA		22.000	SUB						
60	DS1669S-10	ICD IC, DIGITAL POT (PACKAGE SIZE: 8SOP200)	EA		1.000		1	U8				
62	NE555D	MISC TIMER, 555	EA		1.000		1	U7				

BMFSAT FILE
ASSEMBLY 65360-1 ASY PWA, PCT II DISPLAY INTERFACE B/M REVISION DATE - 16FEB95
WITH STANDARD YIELD

REVISION - N/R ECN - NOT REL ECN IMPLEMENTATION DATE - 30NOV94

ITEM	PART NUMBER	DESCRIPTION	U/M	REV	QTY	OPT #	REF DESIGNATOR
63	MC10H350P	ICD IC, ECL TO TTL TRANSLATOR 10H350 19-6367	EA		6.000	1	U1 U2 U3 U4 U5 U6
70	ERG1340	XTR TRANSFORMER, BACKLIGHT	EA		1.000	1	PS1

BMFSAT FILE
CAGE NO 54779
PARTS LIST NO PL65360
ASSEMBLY 65360-2 ASY PWA, PCT II DISPLAY INTERFACE B/M REVISION DATE - 16FEB95
WITH STANDARD YIELD

REVISION - N/R ECN - NOT REL ECN IMPLEMENTATION DATE - 16FEB95 IMPLEMENTED SERIAL NUMBER - UNRELEASED

ITEM	QTY	PART NUMBER	DWG/DOC#	DESCRIPTION	CAGE#	NOTE	REF DESIGNATOR
2	0		ART65361	ARTWORK, NEGATIVES AND SOLDER PASTE MAST			
5	AR	M43553-II WHT	MIL-I-43553	INK, MARKING, EPOXY BASE, WHITE			
8	AR	DC-3140-RTV		CONFORMAL COATING, RTV SILICONE	71984		
11	AR	SN63WRMAP3	QQ-S-571	SOLDER, .025 DIA			
14	AR	SN63PRMA	QQ-S-571	SOLDER PASTE, (25 GRAM SYRINGE)			
17	1	65361-2		PROCESSOR PWB			
18	0		65362	SCHEMATIC DIAGRAM, PROCESSOR			
20	1	TSM-117-01-S-DH		CONNECTOR, 34 PIN, RA SHROUDED HEAD			
22	1	DF9B-15S-W(20)		CONNECTOR,15 PIN,SURFACE MOUNT SOCKET	0AG18		J7
24	1	DF9B-21S-W(20)		CONNECTOR,21 PIN,SURFACE MOUNT SOCKET	0AG18		J8

TOTAL NUMBER OF PAGES - 1

Sharp Panel Data Sheet

SHARP

No.	LD-4Z56
DATE	Feb. 2. 1993

TECHNICAL LITERATURE

FOR

TFT-LCD module

MODEL No. LQ10DX01

The technical literature is subject to change without notice. So, please contact Sharp or its representative before designing your product based on this literature.

SHARP CORPORATION

LIQUID CRYSTAL DISPLAY GROUP

TFT LCD Development Center

1. Application

This technical literature applies to color TFT-LCD module, LQ10DX01.

2. Overview

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel,driver ICs,control circuit and power supply circuit and a backlight unit.Graphics and texts can be displayed on a 1024x768 pixel panel in 512 colors by supplying 9 bitx2 parallel data signals, three kinds of timing signals,+5V and +12V DC supply voltages for TFT-LCD panel driving and supply voltage for backlight. Optimum viewing direction is 6 o'clock.

Backlight-driving DC/AC inverter is not built in this module.

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen size	10.4 (Diagonal)	inch
Effective display area	212.0(H) × 159.0(V)	mm
Display pixels	1024(H) × 768(V)	pixel
	(1 pixel = R + G + B dots)	
Pixel pitch	0.207(H) × 0.207(V)	mm
Pixel configuration	R,G,B vertical stripe	
Display mode	Normally white	
Outline dimension *1	283(W) × 215.6(H) × 12.5(D)	mm
Weight	850±20	g
Surface treatment	anti-glare and hard-coating 2H	

*1 NOTE: excluding backlight cables.

Outline dimensions is shown in Fig.1.

4. Input Terminals and function

4-1) TFT-LCD panel driving

CN1 (Data signals)

Used connector:DF9B-21P-1V(Hirose Electoric Co..Ltd)

Corresponding connector:DF9B-21S-1V(Hirose Electoric Co..Ltd)

Pin No.	Symbol	Function
1	GND	
2	R00	Red data signal of the odd pixels (LSB)
3	R01	Red data signal of the odd pixels
4	R02	Red data signal of the odd pixels (MSB)
5	R10	Red data signal of the even pixels (LSB)
6	R11	Red data signal of the even pixels
7	R12	Red data signal of the even pixels (MSB)
8	GND	
9	G00	Green data signal of the odd pixels (LSB)
10	G01	Green data signal of the odd pixels
11	G02	Green data signal of the odd pixels (MSB)
12	G10	Green data signal of the even pixels (LSB)
13	G11	Green data signal of the even pixels
14	G12	Green data signal of the even pixels (MSB)
15	GND	
16	B00	Blue data signal of the odd pixels (LSB)
17	B01	Blue data signal of the odd pixels
18	B02	Blue data signal of the odd pixels (MSB)
19	B10	Blue data signal of the even pixels (LSB)
20	B11	Blue data signal of the even pixels
21	B12	Blue data signal of the even pixels (MSB)

CN2 (Power supply & signals)

Used connector:DF9B-15P-1V(Hirose Electoric Co..Ltd)

Corresponding connector:DF9B-15S-1V(Hirose Electoric Co..Ltd)

Pin No.	Symbol	Function
1	GND	
2	CK	Clock signal for sampling each data signal
3	GND	
4	Hsync	Horizontal sync. signal (negative)
5	GND	
6	Vsync	Vertical sync. signal (negative)
7	TEST1	This shall be electrically opened during operation
8	TEST2	This shall be electrically opened during operation
9	TEST3	This shall be conected to Vcc
10	Vdd	+12V power supply
11	Vdd	+12V power supply
12	Vdd	+12V power supply
13	Vcc	+5V power supply
14	Vcc	+5V power supply
15	Vcc	+5V power supply

※The shielding case is connected with signal GND.

4-2) Backlight

Used connector:QZ-19-3F01(HONDA TSUSHIN KOGYO CO..LTD)

CNA,CNB Corresponding connector:QZ-19-3MYL(HONDA TSUSHIN KOGYO CO..LTD)

Pin NO.	Symbol	Function
1	V_{HIGH}	Power supply for lamp (High voltage side)
2	N C	
3	V_{LOW}	Power supply for lamp (Low voltage side)

*Cable lergth: CNA&CNB 50±$^{1}_{5}$mm

5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage	V_I	Ta=25℃	−0.3 ~ Vcc+0.3	V	【Note1】
+5V supply voltage	Vcc	Ta=25℃	−0.3 ~ +7	V	
+12V supply voltage	Vdd	Ta=25℃	−0.3 ~ +14	V	
Storage temperature	Tstg	−	−25 ~ +60	℃	【Note2】
Operating temperature (Ambient temp.)	Topa	−	0 ~ +50	℃	

【Note1】 CK.Hsync.Vsync.R00~R02.G00~G02.B00~B02.R10~R12.G10~G12.B10~B12

【Note2】 Relative humidity 95%RH Max. (at Ta≤40℃)
Maximum wet-bulb temperature 39℃ or less. (at Ta>40℃)
No condensation.

6. Electrical Characteristics

6-1. Electrical Characteristics & current dissipation

6-1-a) TFT-LCD panel driving

Ta = 25℃

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+5V	Supply voltage	Vcc	+4.5	+5.0	+5.5	V	
	Current dissipation	Icc	−	TBD	TBD	mA	
+12V	Supply voltage	Vdd	+10.8	+12.0	+13.2	V	
	Current dissipation	Idd	−	TBD	TBD	mA	
Input voltage (Low)		V_{IL}	−	−	1.5	V	Vcc=+5V
Input voltage (High)		V_{IH}	+3.5	−	−	V	
Input low current		I_{OL}	−	−	1.0	μA	V_I=0V
Input high current		I_{OH}	−	−	1.0	μA	V_I=Vcc

6-1-b) Backlight

The backlight system is an edge lighting type. (a couple of CCFT)
The characteristics of single lamp are shown in the following table.

Ta = 25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	−	455	−	Vrms	Just for reference
Lamp current	I_L	6.5	7.0	7.5	mArms	
Lamp power consumption	P_L	−	3.2	−	W	【Note 1】
Frequency	F_L	20	−	60	KHz	【Note 2】
Kick-off voltage	V_s	−	−	1000	Vrms	Ta=25℃
		−	−	1200	Vrms	Ta=0℃
Lamp life time	T_L	TBD	10000	−	hour	【Note 3】

【Note 1】 Calculated values for reference.(I_LxV_L)

【Note 2】 Lamp frequency may produce interference with horizontal sync. frequency,and interference may cause beat on the display. Therefore lamp frequency shall be as different as possibile from that of horizontal sync. signal to avoid interference.

【Note 3】 Brightness becomes 50% of the original value under standard condition.(I_L=7.0mArms)

6-2. Timing Characteristics of input signals

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Clock	Frequency	1/Tc	–	–	28.4	MHz	【Note 1】
	High time	Tch	5	–	–	ns	
	Low time	Tcl	10	–	–	ns	
Data	Setup time	Tds	0	–	–	ns	
	Hold time	Tdh	10	–	–	ns	
Horizontal sync. signal	Cycle	TH	19.0	–	–	μs	
			516	–	–	clock	
	Pulse width	THp	4	–	32	clock	
CK-Hsync. phase difference		THC	0	–	Tc-10	ns	
Vertical sync. signal	Cycle	TV	–	–	17.0	ms	
			772	–	–	line	
	Pulse width	TVp	4	–	8	line	
H-Vsync. phase difference		TVH	0		100	ns	

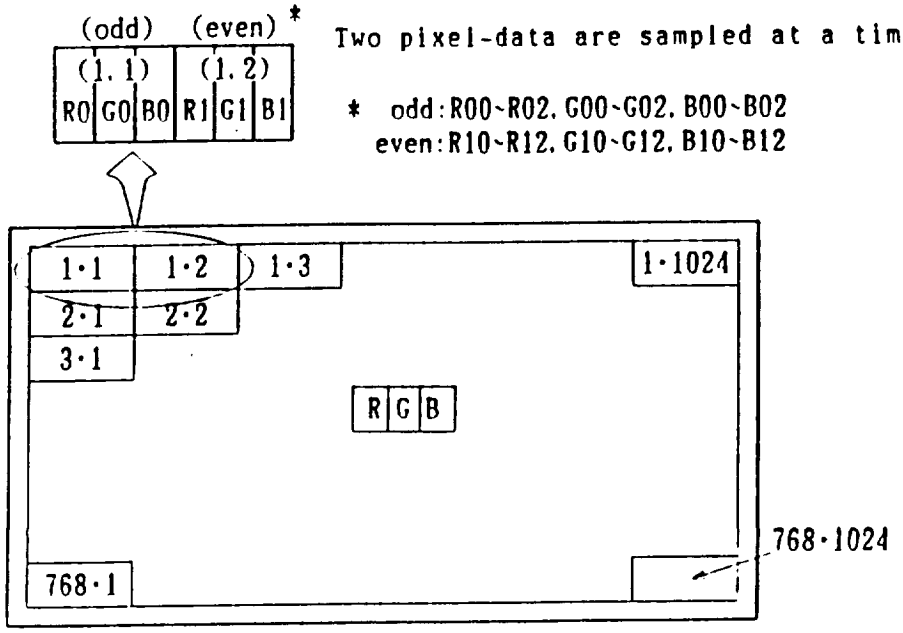
【Note 1】 Two pixel-data are sampled at a time.

Input signal waveforms are shown in Fig.2.

6-3. Display period

Items	Standards	Beginning	Ending	Unit	Remark
Horizontal	falling edge of Hsync.	4	516	clock	
Vertical	falling edge of Vsync.	4	772	line	

6-4. Input Signals and Display on the screen



Display position of input data (V · H)

7. Optical Characteristics

Ta=25℃, Vcc=+5.0V, Vdd=+12.0V

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ 21, 22	CR > 10	45	–	–	Deg.	【Note1】
	Vertical	θ 11		10	–	–	Deg.	
		θ 12		30	–	–	Deg.	
Contrast ratio		C R		60	–	–		【Note2】
Response time	Rise	τ r	θ =0°	–	30	–	ms	【Note3】
	Fall	τ f		–	50	–	ms	
White uniformity		δ w		–	–	1.25		【Note4】
Luminance of white		Y_L		–	70	–	cd/m²	

※ The measurement shall be executed 15~20 minutes after lighting at rating. (I_L=7.0mArms)
The optical characteristics are measured in a darkroom or equivalent state with the method shown in Fig.3. And these characteristics except for White uniformity are measured at the center of the screen.

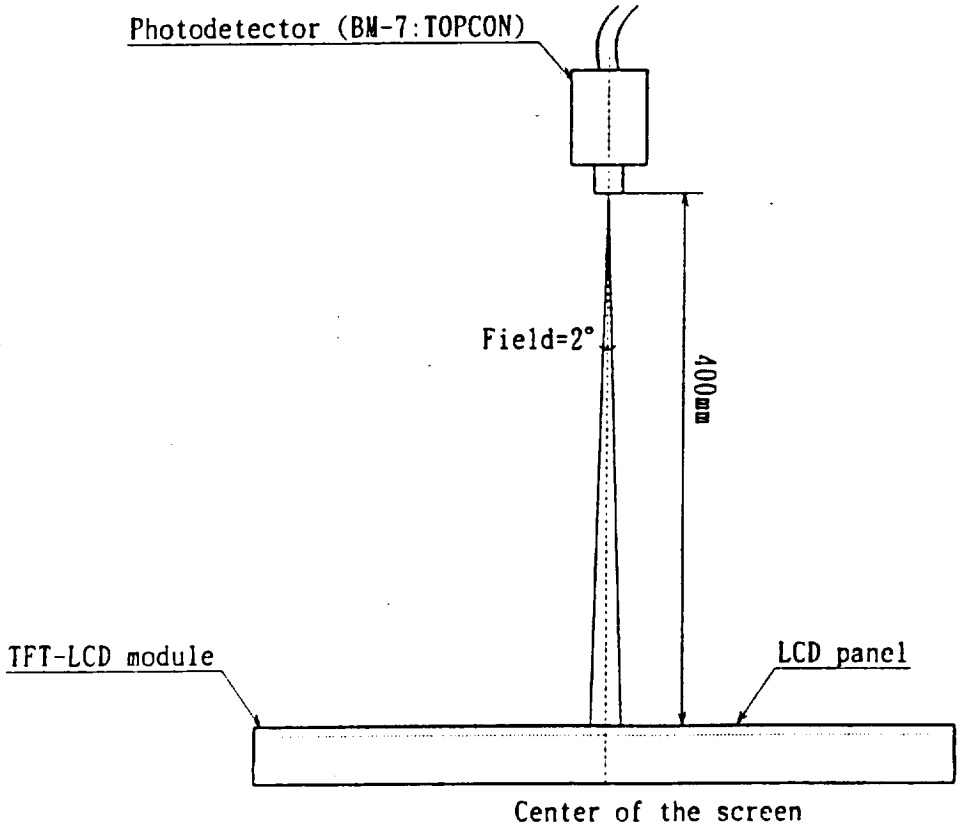


Fig. 3 Optical characteristics measurement method

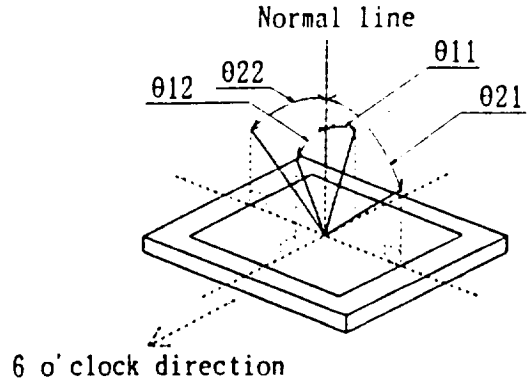
6-4. Input Signals. Basic Display Colors and Gray Scale of Each Color

	color & gray scale		Data signal								
		odd	R00	R01	R02	G00	G01	G02	B00	B01	B02
		even	R10	R11	R12	G10	G11	G12	B10	B11	B12
Basic color	Black		0	0	0	0	0	0	0	0	0
	Blue		0	0	0	0	0	0	1	1	1
	Green		0	0	0	1	1	1	0	0	0
	Light blue		0	0	0	1	1	1	1	1	1
	Red		1	1	1	0	0	0	0	0	0
	Purple		1	1	1	0	0	0	1	1	1
	Yellow		1	1	1	1	1	1	0	0	0
	White		1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black		0	0	0	0	0	0	0	0	0
	⇧		1	0	0	0	0	0	0	0	0
	Darker		0	1	0	0	0	0	0	0	0
	⇧		1	1	0	0	0	0	0	0	0
	⇩		0	0	1	0	0	0	0	0	0
	Brighter		1	0	1	0	0	0	0	0	0
	⇩		0	1	1	0	0	0	0	0	0
	Red		1	1	1	0	0	0	0	0	0
Gray Scale of Green	Black		0	0	0	0	0	0	0	0	0
	⇧		0	0	0	1	0	0	0	0	0
	Darker		0	0	0	0	1	0	0	0	0
	⇧		0	0	0	1	1	0	0	0	0
	⇩		0	0	0	0	0	1	0	0	0
	Brighter		0	0	0	1	0	1	0	0	0
	⇩		0	0	0	0	1	1	0	0	0
	Green		0	0	0	1	1	1	0	0	0
Gray Scale of Blue	Black		0	0	0	0	0	0	0	0	0
	⇧		0	0	0	0	0	0	1	0	0
	Darker		0	0	0	0	0	0	0	1	0
	⇧		0	0	0	0	0	0	1	1	0
	⇩		0	0	0	0	0	0	0	0	1
	Brighter		0	0	0	0	0	0	1	0	1
	⇩		0	0	0	0	0	0	0	1	1
	Blue		0	0	0	0	0	0	1	1	1

0: Low level voltage
1: High level voltage

Each color is displayed in 8 gray scales from 3 bit data signals input. According to the combination of total 9 bit data, 512 colors are displayed.

【Note1】 Definitions of viewing angle:



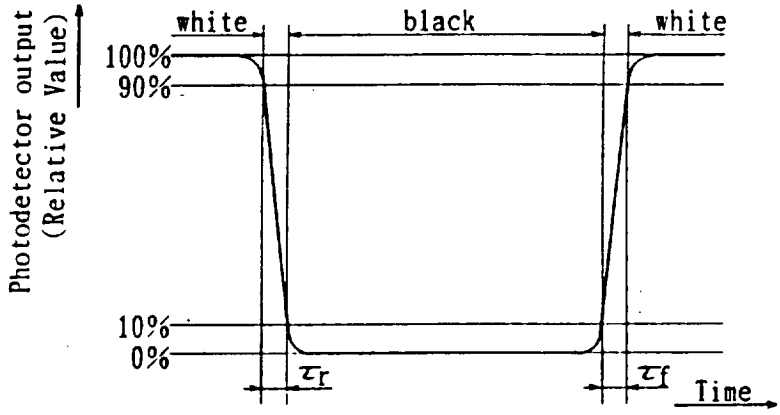
【Note2】 Definitions of Contrast Ratio:

The contrast ratio is defined as follows.

$$\text{Contrast Ratio} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

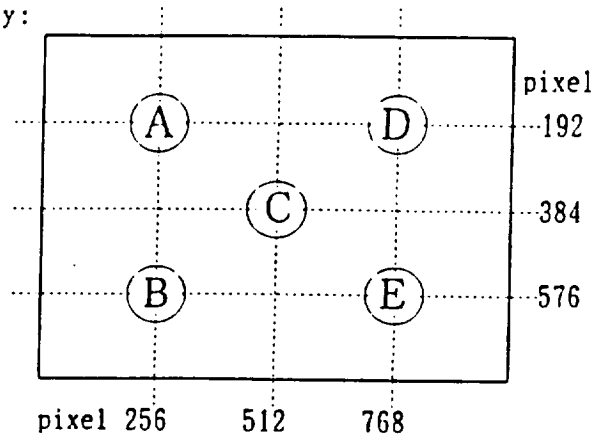
【Note3】 Definitions of Response Time:

The response time shall be measured as the following figure by switching the input signals for "black" ON and OFF.



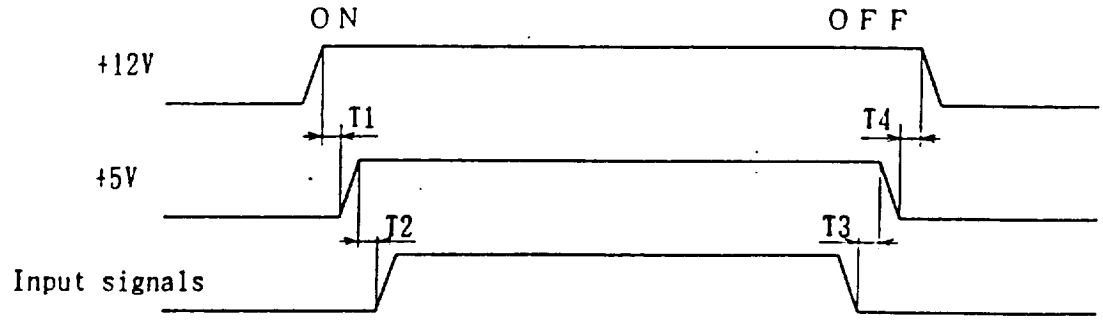
【Note4】 Definition of White uniformity:
The white unifomity is defined as the following equation among the values measured at the 5 spots(A~E).

$$\frac{\text{maximum luminance (brightness)}}{\text{minimum luminance (brightness)}}$$



8. Display quality
The display quality of this module shall be in compliance with the Delivery Inspection Standard.

9. Handling Precautions
9-1) Be sure to insert the cable into the connector or take out of the connector after turning off the power supply on the set side.
9-2) Power ON/OFF sequential timing
To prevent the latch-up of the circuit in the module, keep the sequential timing between the input signals and supply voltage as follows.



$0 \leqq T1 \leqq 1\text{sec}$, $0 \leqq T2 \leqq 1\text{sec}$ $0 \leqq T3 \leqq 1\text{sec}$, $0 \leqq T4 \leqq 1\text{sec}$

9-3) Others
a) When installing the module, be sure to fix the module on the same plane, taking care not to warp or twist the module.
b) Since the front polarizer is easily damaged, pay attention not to scratch it.
c) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
d) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

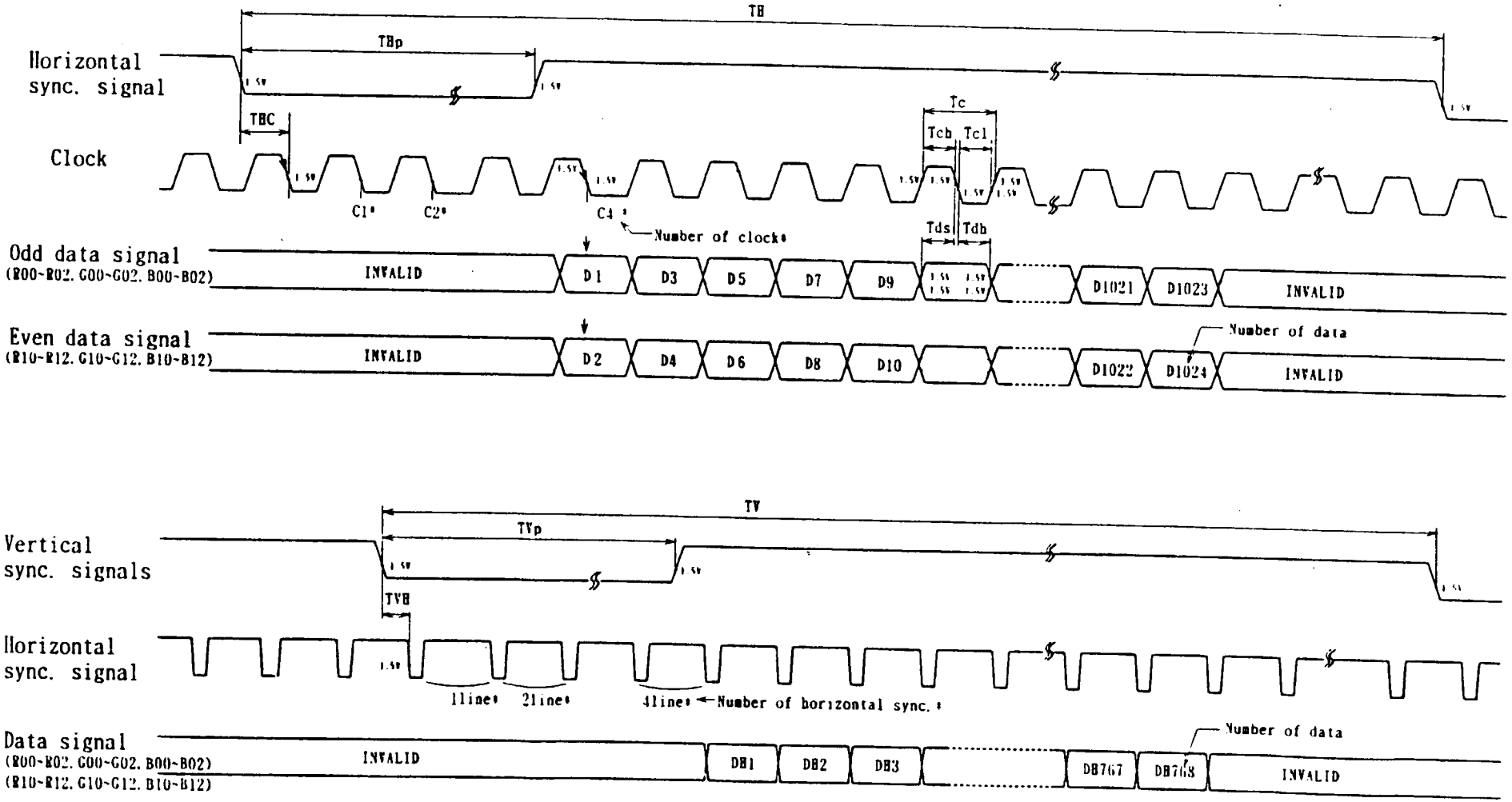


Fig. 2 Input signal waveforms

e) Since the glass is used in the module. it may break or crack if dropped or bumped on hard surface. Handle with care.
f) Since CMOS LSI is used in this module. take care of static electricity and ground your body when handling.
g) Observe all other precautionary requirements in handling components.

10. Packing form
a) Piling number of cartons : MAX. 6
b) Package quantity in one carton : MAX. 10
c) Carton size : 420mm(W)x330mm(H)x400mm(D)
d) Total weight of 1 carton filled with full modules:12000g
Packing form is shown in Fig.4.

11. Reliability test items

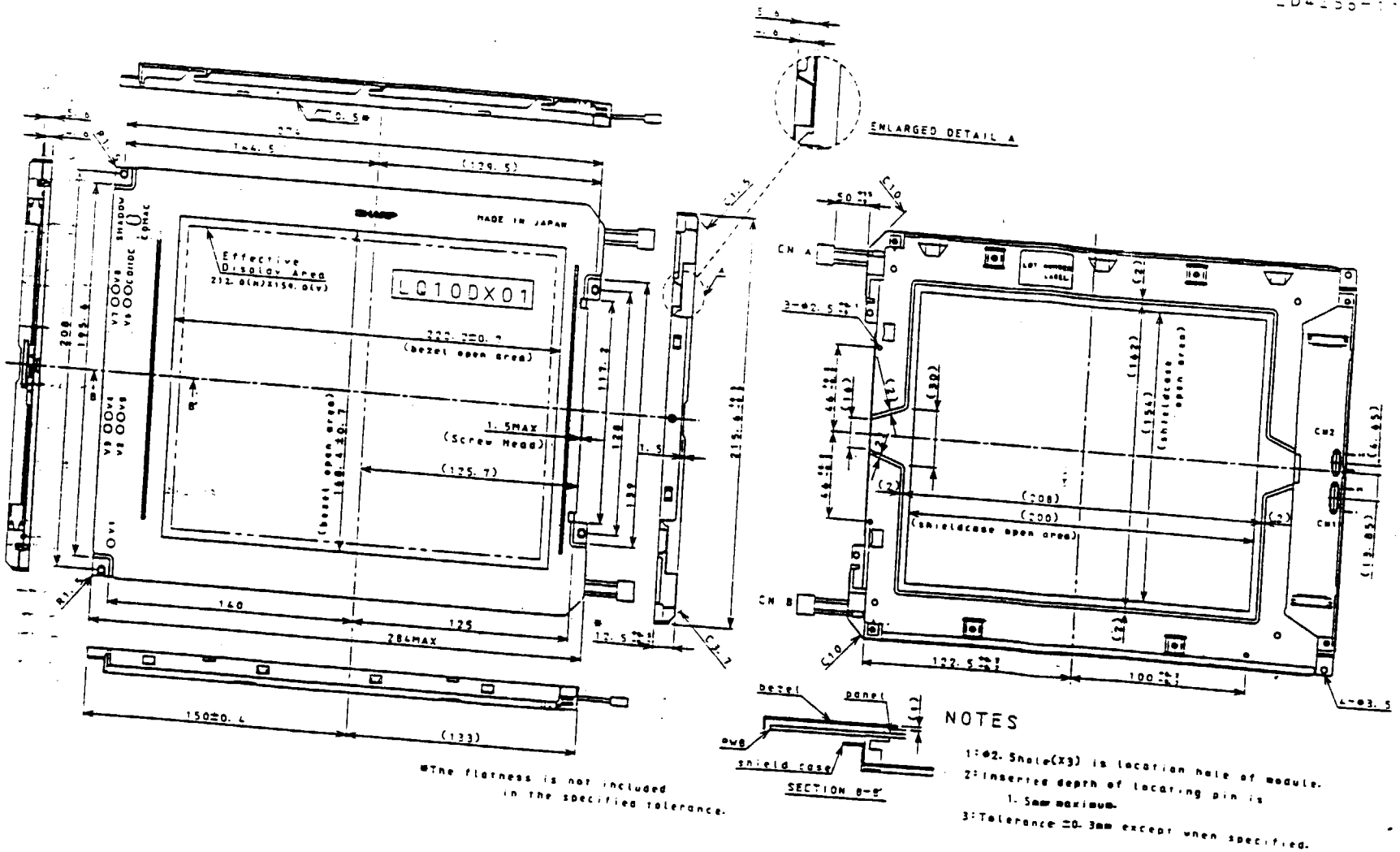
No.	Test item	Conditions
1	High temperature storage test	Ta=60℃ 240h
2	Low temperature storage test	Ta=-25℃ 240h
3	High temperature & high humidity operation test	Ta=40℃;95%RH 240h (No condensation)
4	High temperature operation test	Ta=50℃ 240h (The panel temp must be less than 60℃)
5	Low temperature operation test	Ta=0℃ 240H
6	Vibration test (non-operating)	Frequency:10~57Hz Vibration width(one side):0.075mm Frequency:58~500Hz Gravity:9.8m/s² Sweep time : 11 min. Test period : 3 h (1 hour for each direction of X.Y.Z)
7	Shock test (non-operating)	Max. gravity : 490m/s² Pulse width : 11ms. sine wave Direction : ±X.±Y.±Z once for each direction.

【Result Evaluation Criteria】
Under the display quality test conditions with normal operation state. these shall be no change which may affect practical display function.

12. Others
1) Lot No. Label: TBD
2) Adjusting volumes have been set optimally before shipment. so do not change any adjusted values. If adjusted values are changed. the data mentioned in this technical literature may not be satisfied.
3) Disassembling the module can cause permanent damage and should be strictly avoided.

OUTLINE DIMENSIONS OF TFT-LCD MODULE

Feb 3. 1993



*The flatness is not included in the specified tolerance.

NOTES

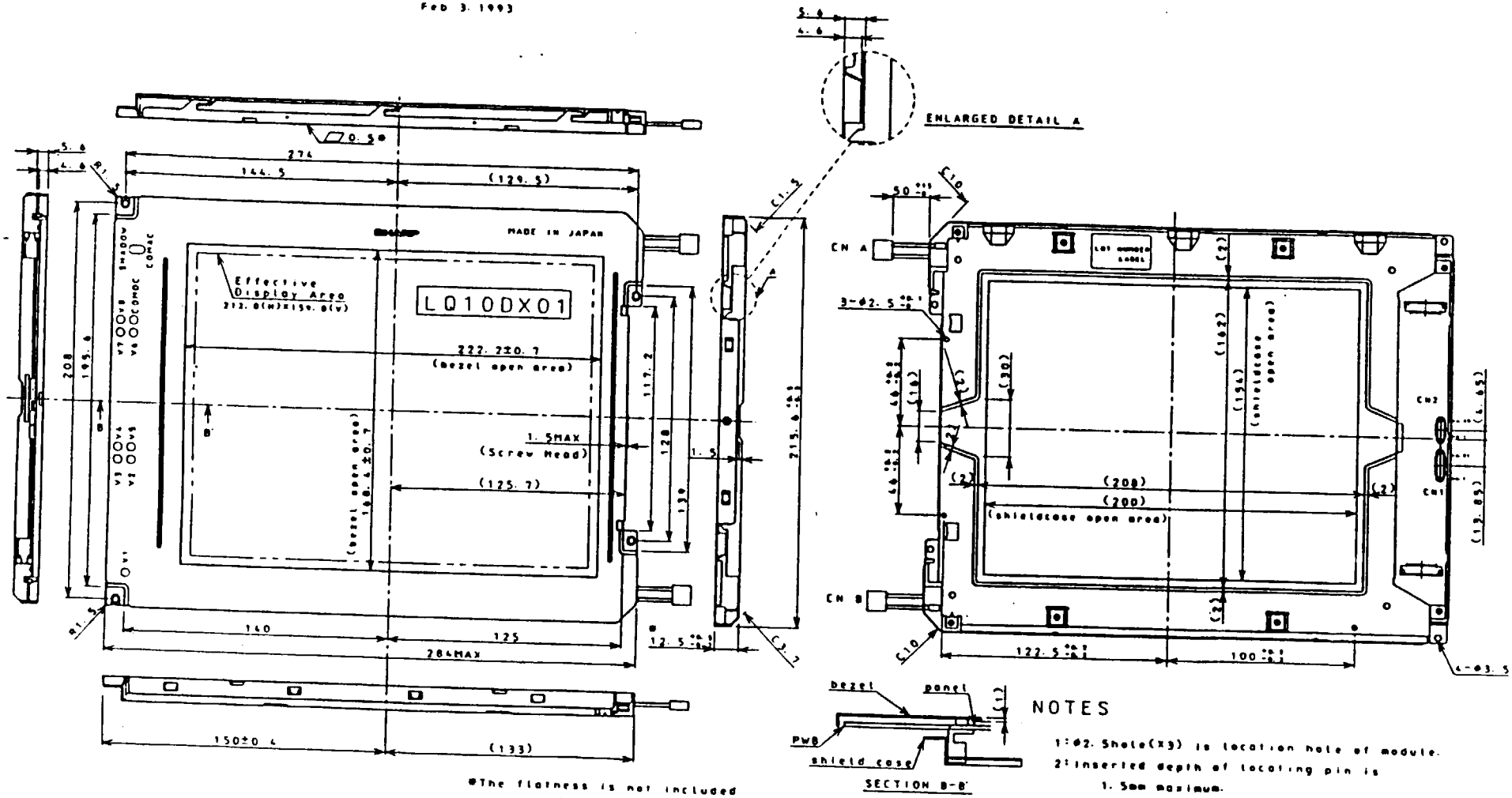
1: φ2.5hole(X3) is location hole of module.
2: Inserted depth of locating pin is 1.5mm maximum.
3: Tolerance ±0.3mm except when specified.

Fig1: Outline Dimensions

OUTLINE DIMENSIONS OF TFT-LCD MODULE

Feb 3. 1993

LD4Z56-11



NOTES

1: φ2.5hole(x3) is location hole of module.
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Fig1: Outline Dimensions

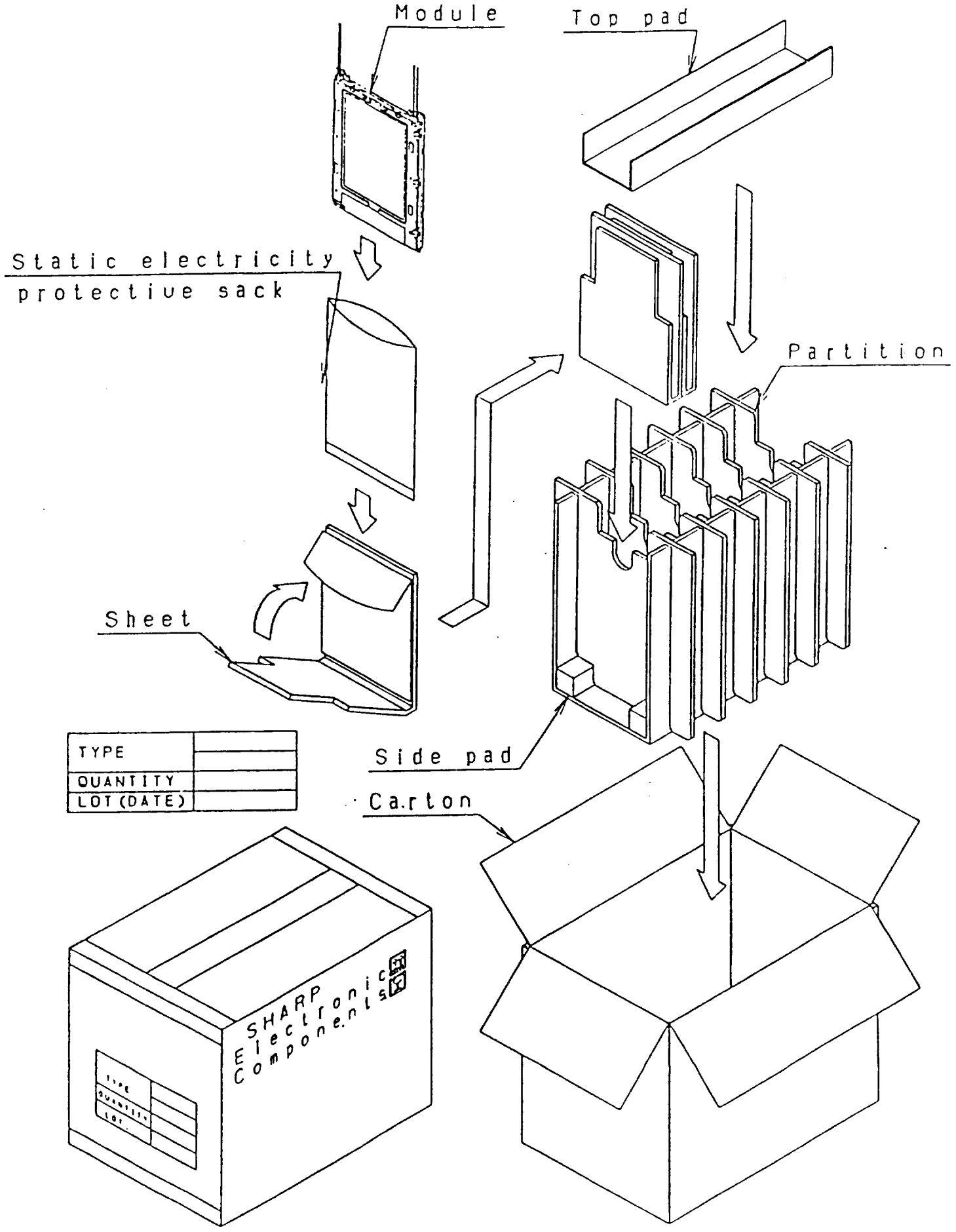


Fig.4 Packing form

Fujitsu Panel Data Sheet

Additional Display Information

Fujitsu 21" Plasma Panel

The Fujitsu 21" Plasma Panel is the world's largest full color plasma display in production. It features 260,000 colors with 64 graduations of RGB with a 640 x 480 pixel format on a 21-inch diagonal screen.

There is tremendous potential in the future of plasma displays. The introduction of a 30" and 42" color plasma panel is expected to be available sometime in 1996 for prototypes, with production units available in 1997. It is expected that these first large panels will be Wide Definition Television (WDTV) compatible. Fujitsu is working on a 25" panel that will be SVGA compatible, however, these panels are not expected to be in production until Quarter 4 in 1998.

NEC 13" LCD Display

The NEC 13" display is an active matrix LCD comprised of amorphous-Silicon thin film transistors placed on each pixel electrode, a driving circuit and a built-in back light. The panel was unavailable for evaluation, in time for this project. Below is a summary of the NEC display characteristics:

- Diagonal screen size — 13 inch
- External WxHxD dimensions (mm) — 310 x 255 x 43
- Effective viewing area (mm) — 211.2 x 158.4
- No. of pixels — 1280 x 1024
- Pixel pitch (mm) — 0.201 (horz) x 0.201 (vert)
- No. of colors — 4,096
- Contrast Ratio — 1:80
- Weight (g) — approx. 2,100

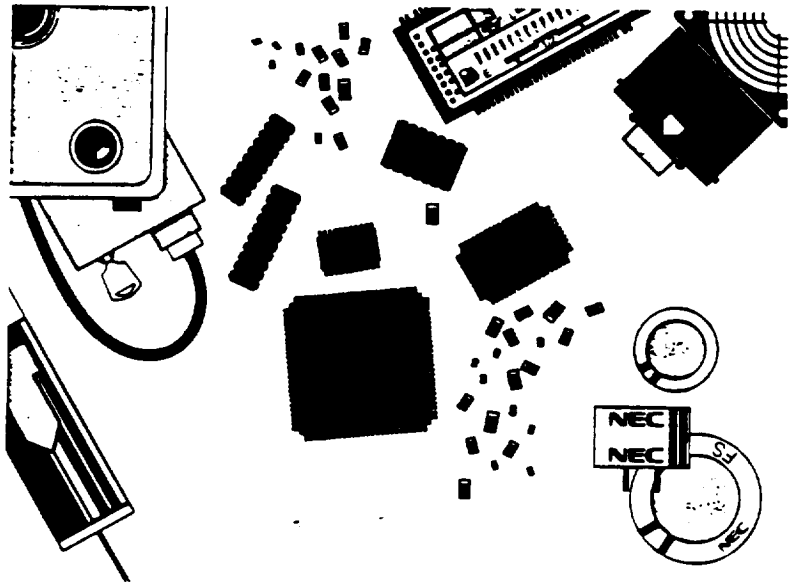
Additional features include:

- High resolution display and wide range of display colors
- Wide viewing angle with high contrast
- High speed response
- Low power consumption (27 W Typical)
- Thin and light weight

NEC Panel Data Sheet

August 1993

Electron Components



13" Color
TFT-LCD Module

Type No. NL128102AC20-03

Preliminary Data Sheet

1250 × 1024

NEC

1. Abstract

The NEC NL128102AC20-03 is an active matrix color-Liquid Crystal Display module comprising amorphous-Silicon thin film transistors (TFTs) placed on each pixel electrode, a driving circuit and a built-in back light.

It has a display area of 257.3(H)×205.8(V)mm (diagonal 13 – inch) 1280×1024 pixels, and 4096-colors display capability.

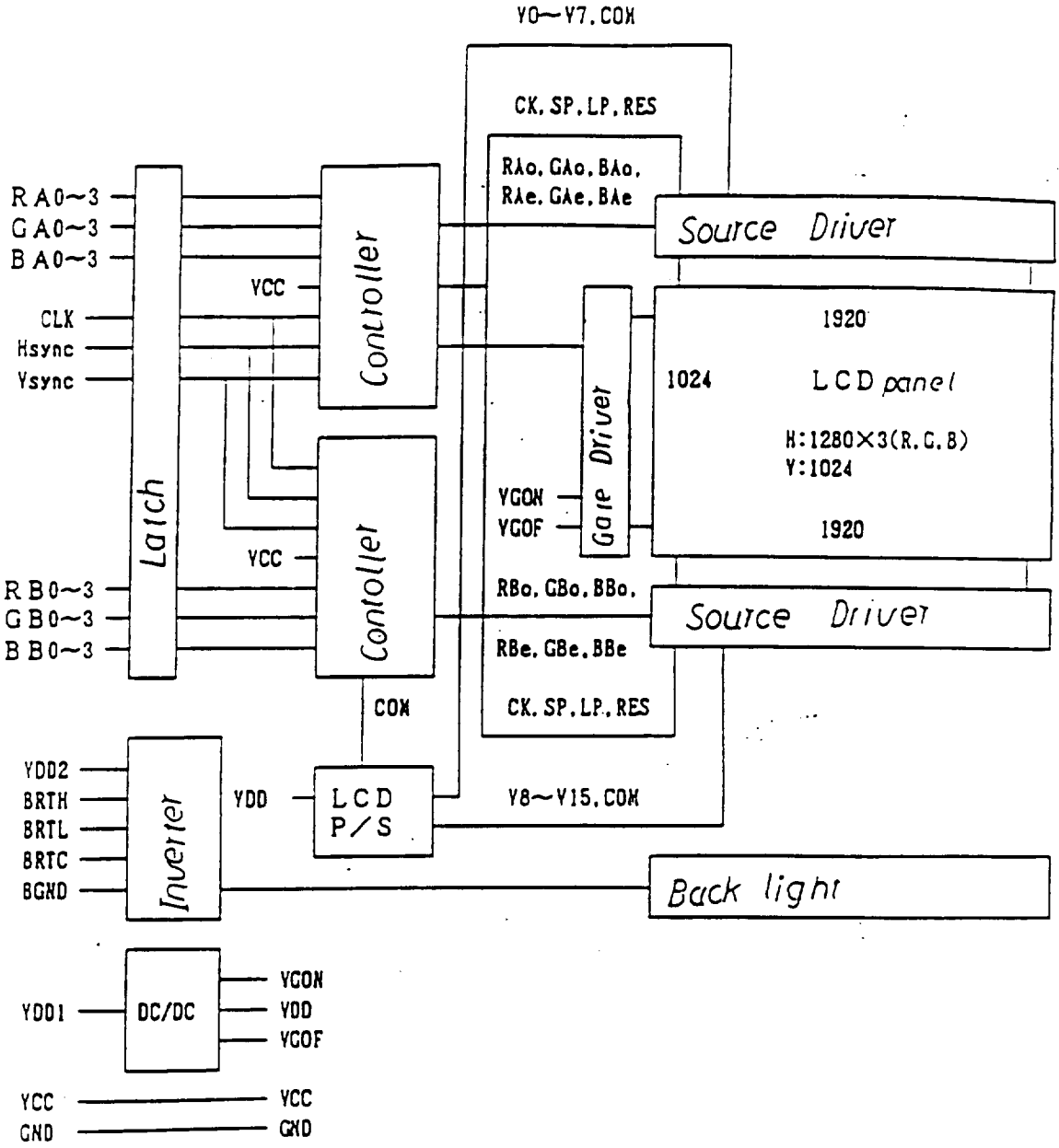
2. Features

- High resolution and wide range of display colors
- Wide viewing angle with high contrast
- High speed response
- Easy interface connection
- Low power consumption
- Thin and light weight

3. Application for example

- Work station moniter display
- Terminal-display for control system
- Operation board of NC-machine
- Monitor of process control system

4. Block diagram of the LCD-module



5. Outline of characteristics (at room temperature)

Item	Specification
Display area	257.3(H) × 205.8(V) mm (diagonal 13 inch)
Drive system	a-Si TFT active matrix system
Display colors	4096 Colors
Number of Pixels	1280 × 1024
Pixel arrangement	RGB Vertical stripe
Pixel pitch	0.201(H) × 0.201(V) mm
Size	310(H) × 255.5(V) × 43 MAX(D) mm
Weight	2100g (Max)
Contrast ratio	80:1
Viewing angle (within contrast ratio of more than 5:1)	Horizontal: 40° (Left side, Right side) Vertical : 10° (up), 30° (down)
Color gamut	40% above (center to NTSC)
Response time	less than 50mm sec.
Luminance	70 cd/m^2
Signal system	RGB 4 bit signals each clock, synchronous signals (H-sync, V-sync)
Supply voltage	24, 12, 5V
Back light	Fluorescent lamps (Cold cathode) with inverter
Power consumption	27W (Typ.)

6. Specification

(1) General specification

Subject	Specification	Unit
Unit size	310±1(H)×255.5±1(V)×43(D) (Max)	mm
Display area	257.3(H) × 205.8(V), (diagonal: 13')	mm
Pixel No.	1280(×3)(H) × 1024(V)	
Dot pitch	0.067(H) × 0.201(V)	mm
Pixel pitch	0.201(H) × 0.201(V)	mm
Pixel arrangement	R.G.B vertical stripe	
Color	4096	Color
Weight	2100 (Max)	g

* The inverter is prepared internal module set.
Dimming potentiometers are extra. (1KΩ)

(2) Absolute rating

Subject		Symble	Rating		Unit	Note
			Min	Max		
Supply voltage		VDD1	-0.3	28	V	Ta=25°C
		VDD2	-0.3	13	V	
		VCC	-0.3	7	V	
Logic input level	L	VIL	-0.3	-	V	
	H	VIH	-	Vcc+0.3	V	
Storage temp.		TST	-20	60	°C	
Operating temp.		TOP	0	50	°C	Surface of LCD-panel
Humidity			-	95	%RH	Ta=40°C
			-	85	%RH	Ta=50°C
				85	%RH	Ta<50°C

(3) Electrical characteristics

- Logic/LCD Operation

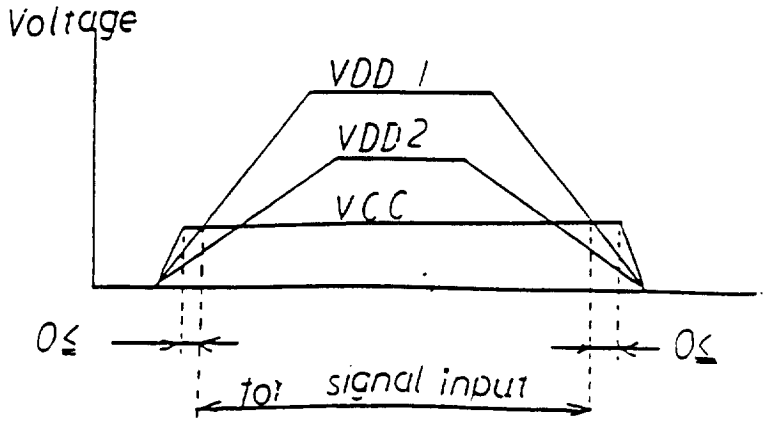
Subject		Symble	Min	Typ	Max	Unit	note
Supply Voltage		VDD1	22.8	24.0	25.2	V	Ta=25°C
		VCC	4.75	5.0	5.25	V	
Logic input level	L	VIL	0	-	0.8	V	Ta=25°C
	H	VIH	2.0	-	Vcc	V	TTL level
Current		IDDI	-	150	170	mA	VDDI=24V for LC-Operation
		ICC	-	1.0	1.2	A	Vcc=5V for Logic

- Back light

Subject	Symble	Min	Typ	Max	Unit	note
Supply Voltage	VDD2	11.4	12.0	12.6	V	
Current	IDD2	—	1.5	1.7	A	VDD2=12V
Power Consumption	WL	—	—	18.0	W	Note 1

Note 1: Total power consumption of unit and inverter must be less than 22W.

Supply voltage sequence



note

*1 The power source for outer driver should be the same as the LCD module power source (VCC).

*2 VDD2 supply voltage should be applied during VDD1.

In case of lighting before LCD-operation or put out lighting after LCD-off, the white color appear momentarily on the screen.

*3 In case of using battery for VDD2, the back light should be controlled by BRTC (back light ON/OFF signal.).

The sequence is the same as above *2.

7. Interface and Connector-pin arrangement

(1) Clock signal, power source-connector

CN1 Connector : 10268-52D2 (Hl0-S68P-L)
MAde by SUMITOMO 3M

View from Parts Side

Pin No.	Signal
117	CLK
116	HOT
115	BB2
114	BB0
113	BA2
112	BA0
111	GB2
110	GB0
109	GA2
108	GA0
107	RB2
106	B0
105	RA2
104	RA0
103	BRTH
102	+12V
101	+5V

Pin No.	Signal
217	SG
216	SG
215	SG
214	SG
213	SG
212	SG
211	SG
210	SG
209	SG
208	SG
207	SG
206	SG
205	SG
204	SG
203	BG
202	BG
201	+5V

Pin No.	Signal
317	SG
316	SG
315	SG
314	SG
313	SG
312	SG
311	SG
310	SG
309	SG
308	SG
307	SG
306	SG
305	SG
304	SG
303	BRTL
302	BG
301	+5V

Pin No.	Signal
417	VOT
416	BB3
415	BB1
414	BA3
413	BA1
412	GB3
411	GB1
410	GA3
409	GA1
408	RB3
407	RB1
406	RA3
405	RA1
404	BRTC
403	+12V
402	+12V
401	+24V

View from cable connector side

Pin No.	Signal
01	CLK
02	SG
03	HOT
04	SG
05	BB2
06	SG
07	BB0
08	SG
09	BA2
10	SG
11	BA0
12	SG
13	GB2
14	SG
15	GB0
16	SG
17	GA2

Pin No.	Signal
18	SG
19	GA0
20	SG
21	RB2
22	SG
23	RB0
24	SG
25	RA2
26	SG
27	RA0
28	SG
29	BRTH
30	BG
31	+12V
32	
33	+5V
34	+5V

Pin No.	Signal
35	SG
36	VOT
37	SG
38	BB3
39	SG
40	BB1
41	SG
42	BA3
43	SG
44	BA1
45	SG
46	GB3
47	SG
48	GB1
49	SG
50	GA3
51	SG

Pin No.	Signal
52	GA1
53	SG
54	RB3
55	SG
56	RB1
57	SG
58	RA3
59	SG
60	RA1
61	SG
62	BRTC
63	BRTL
64	+12V
65	BG
66	+12V
67	+5V
68	+24V

Note: Signal

Signal	Level	Function	frequency
RA(0~3), RB(0~3)	TTL	Data : RED	26.875 MHz
GA(0~3), GB(0~3)	TTL	Data : GREEN	26.875 MHz
BA(0~3), BB(0~3)	TTL	Data : BLUE	26.875 MHz
HOT	TTL	HSYNC	64.60 KHz
VOT	TTL	VSYNC	59.929 KHz
CLK	TTL	CLOCK	53.75 MHz
SG		Signal Ground	
BG		Back Light Ground	
BRTH		Potentiometer	
BRTL		Potentiometer	
BRTC	TTL	Back Light ON/OFF	

(2) POTENTIOMETER

CN2 Connector: S16B-PHDSS

Made by Nippon attchaku tanshi

Pin No.	Signal	Function	Pin No.	Signal	Function
08	BRTC	Resistance	16	SG	GND
07	BRTH	Resistance	15	BRTL	BL ON/OF
06	SG	GND	14	SG	GND
05	VDD1	24V for LC-Operation	13	VDD1	24V for LC-operation
04	BG	GND for BL	12	BG	GND for BL
03	VDD2	12V for BL	11	VDD2	12V for BL
02	SG	GND	10	SG	GND
01	VCC	5V for Logic	09	VCC	5V for Logic

Note 1 Black ligth should be oN at "High-level" or "Open" of BRTC.

Note 2 Potentiometer (Resistance : 1KΩ ±5%),
OΩ-position is minimum brightness.
(Potentiometer should be joint between "BRTH" and "BRTL".)

There is no page 11

8. Input signal, display color and luminance gray scale

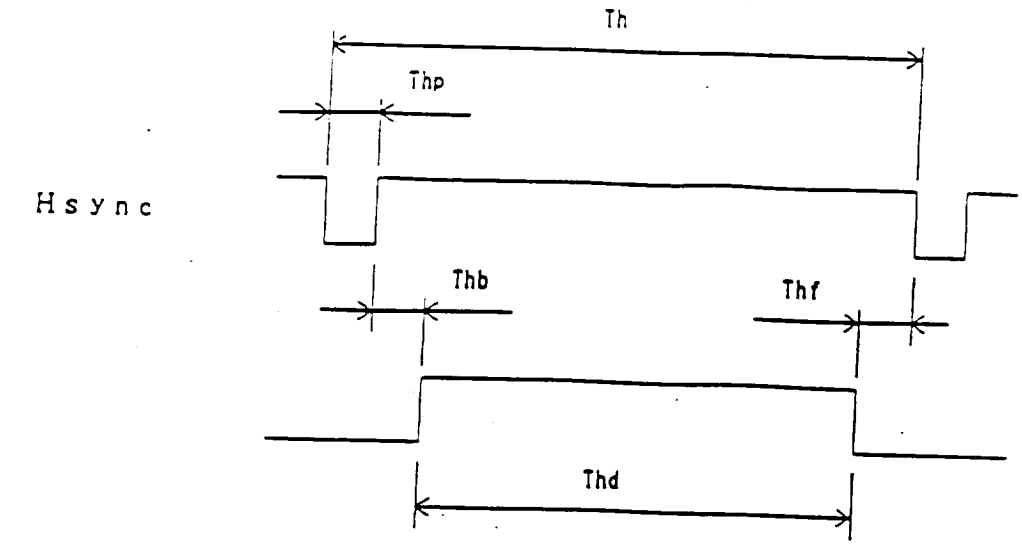
	Display color	Data signal (0: Low level 1: High level)											
		RA3 RB3	RA2 RB2	RA1 RB1	RA0 RB0	GA3 GB3	GA2 GB2	GA1 GB1	GA0 GB0	BA3 BB3	BA2 BB2	BA1 BB1	BA0 BB0
Base	Black	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	1	1	1	1
	Red	1	1	1	1	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	0	0	0	0	1	1	1	1
	Green	0	0	0	0	1	1	1	1	0	0	0	0
	Cyan	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1
Red gray-scal	Black	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	1	0	0	0	0	0	0	0	0	0
	↕			⋮				⋮				⋮	
	bright	1	1	0	1	0	0	0	0	0	0	0	0
		1	1	1	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	0	0	0	0	0	0	0	0
Green gray-scal	Black	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0
	↕			⋮				⋮				⋮	
	bright	0	0	0	0	1	1	0	1	0	0	0	0
		0	0	0	0	1	1	1	0	0	0	0	0
	Green	0	0	0	0	1	1	1	1	0	0	0	0
Blue gray-scal	Black	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	1	0
	↕			⋮				⋮				⋮	
	bright	0	0	0	0	0	0	0	0	1	1	0	1
		0	0	0	0	0	0	0	0	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	1	1	1	1

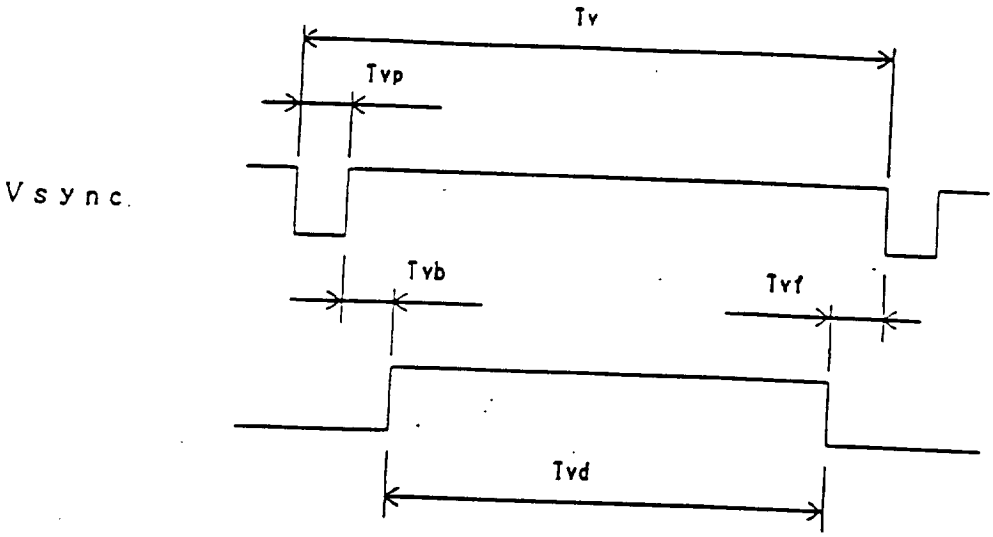
<note> The number of color is 4096 that is according to combination with each 4-bit for three base color (R.G.B) signals. $16^3=4096$.

9. Interface Timing

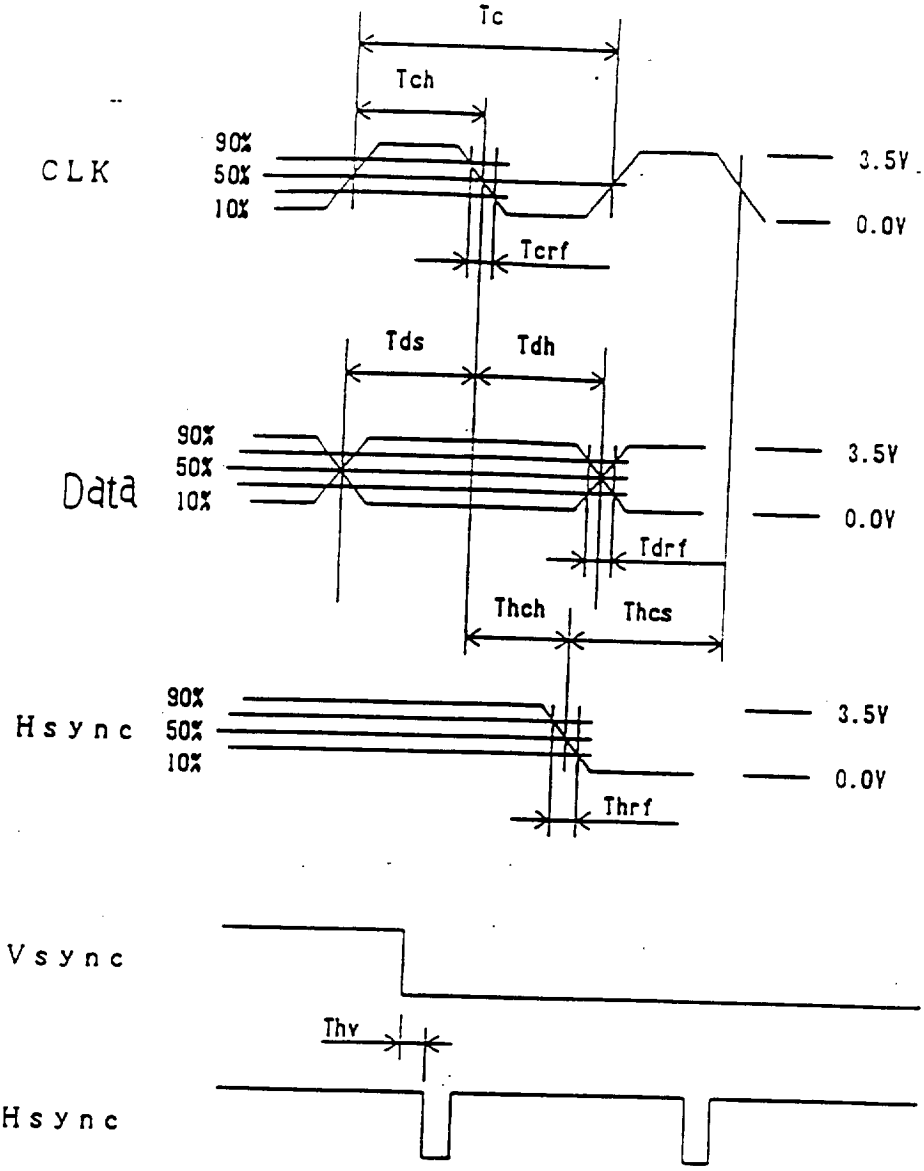
Parameter		Symble	Time	Frequency
Clock	Frequency	1/Tc	18.60ns	53.75MHz
	Duty	Tch/Tc	0.4~0.6	--
	Transient time	Tcrf	2.0ns(MAX)	--
Horizontal sync. Signal		Th	15.479μs	64.60kHz
Video period		Thd	11.907μs	--
Front porch		Thf	0.298μs	--
Pulse width		Thp	1.786μs	--
Back porch		Thb	1.488μs	--
Clock-horizontal Timing	(1)	Thch	7.5ns(MIN)	--
"	(2)	Thcs	2.0ns(MIN)	--
Delay for Vsync		Thv	-6.0~+6.0ns	--
Transient time		Thrf	2.5ns(MAX)	--
Vertical sync. Signal		Tv	16.686ms	59.292Hz
Video period		Tvd	15.850ms	--
Front porch		Tvf	0.108ms	--
Pulse width		Tvp	0.062ms	--
Back porch		Tvb	0.666ms	--
Data	Set up Time	Tds	2.0ns(MIN)	--
	Hold Time	Tdh	7.5ns(MIN)	--
	Transient time	Tdrf	2.5ns(MAX)	--

Timing chart (1)

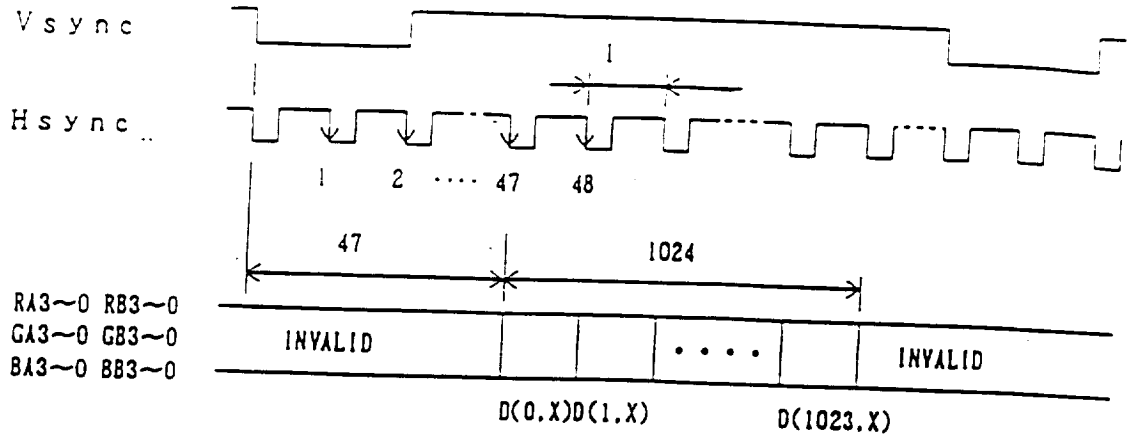


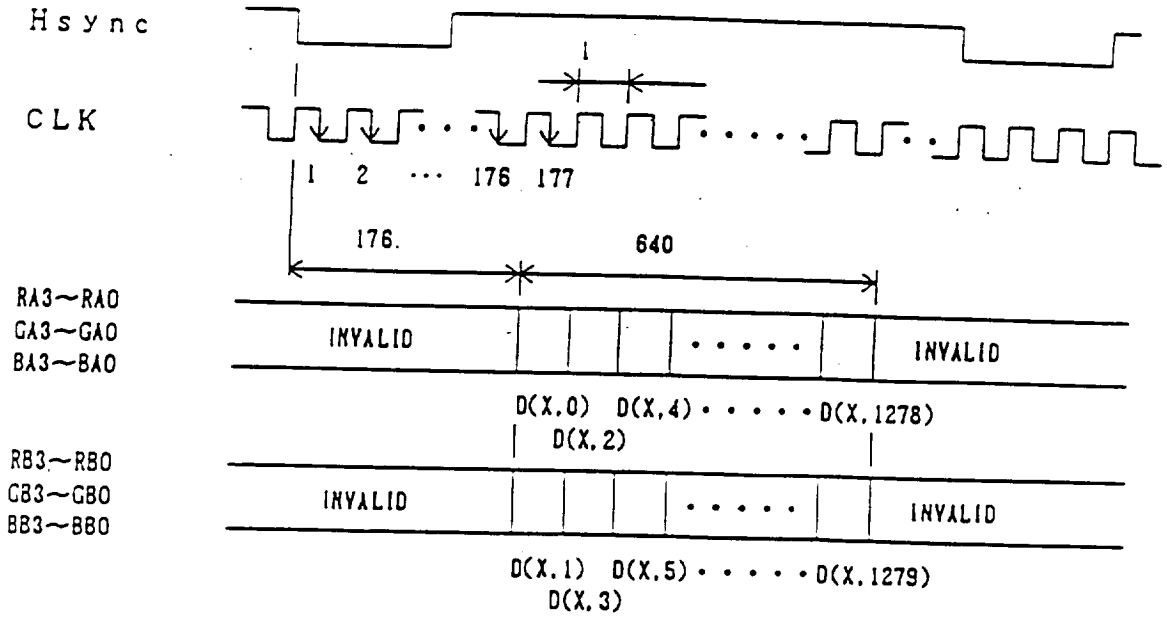


Timing chart (2)



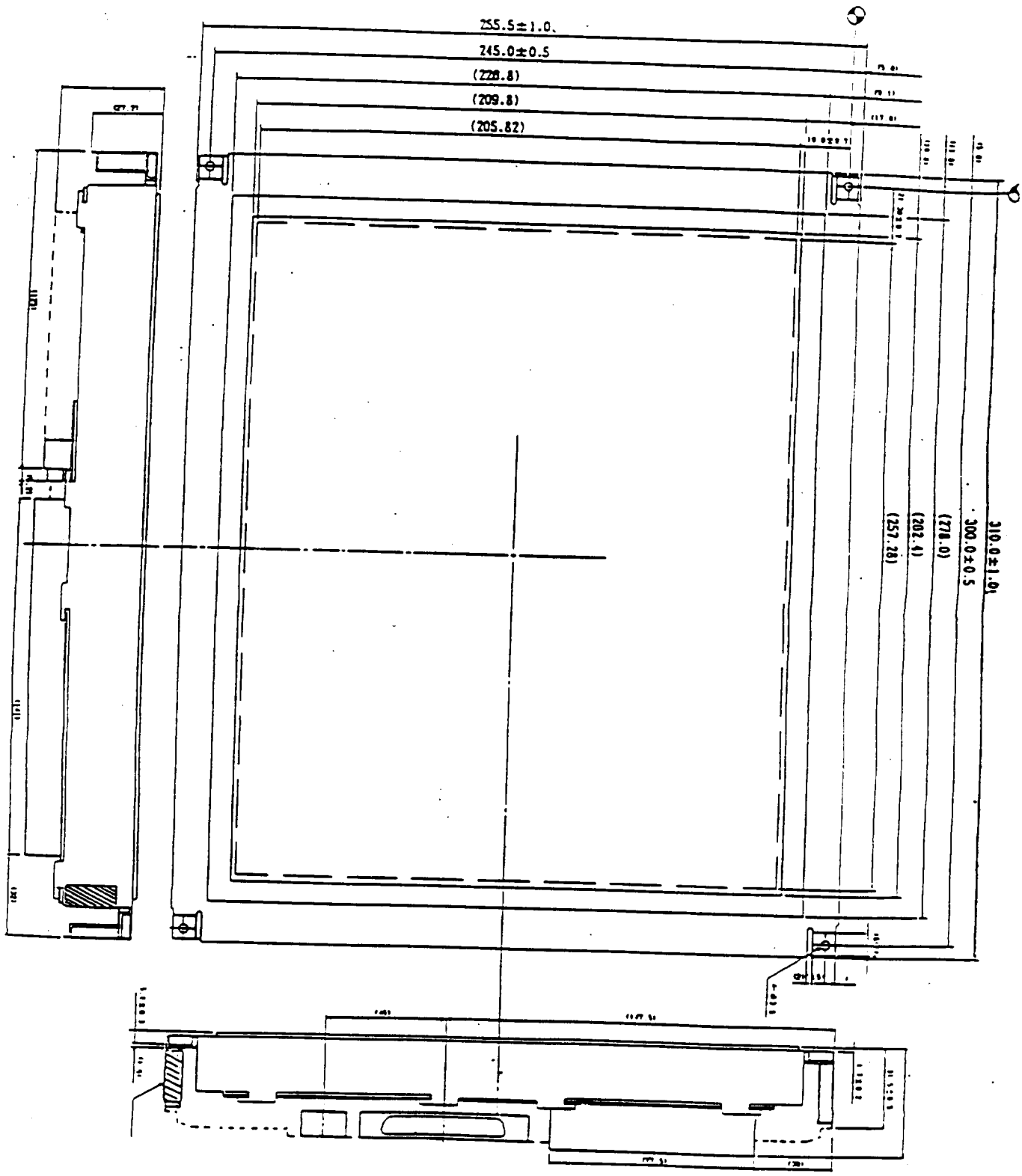
Timing chart (3)





D(0, 0)	D(0, 1)	D(0, 2)	· · · · · ·	D(0,1279)
D(1, 0)	D(1, 1)			
D(2, 0)				
⋮				⋮
D(1023, 0)	D(1023, 1)	D(1023, 2)	· · · · · ·	D(1023,1279)

External drawing (Unit: mm)



General caution for handling

(1) Protector against electrostatic discharge is necessary on handling the LCD-module.
In particular, the protection sheet on the panel should be removed slowly.

(2) The LCD-panel and the back light tube are composed of glass, so handle with care.

Don't push the surface of LCD module. Don't give strong mechanical shock.

(3) The polarizer (the protector) surface is very soft. Use dry soft cloth for cleaning the surface, never use with chemicals.

(4) The interface connector should be handled (insert/pull) during power source OFF.

(5) Don't operate the LCD-module in dew drop atmosphere.

(6) Avoid an atmosphere of high temperature/high humidity when keeping or operating the LCD-module.
For keeping the LCD-module good condition, the electric conductive polyethylene bag should be use.

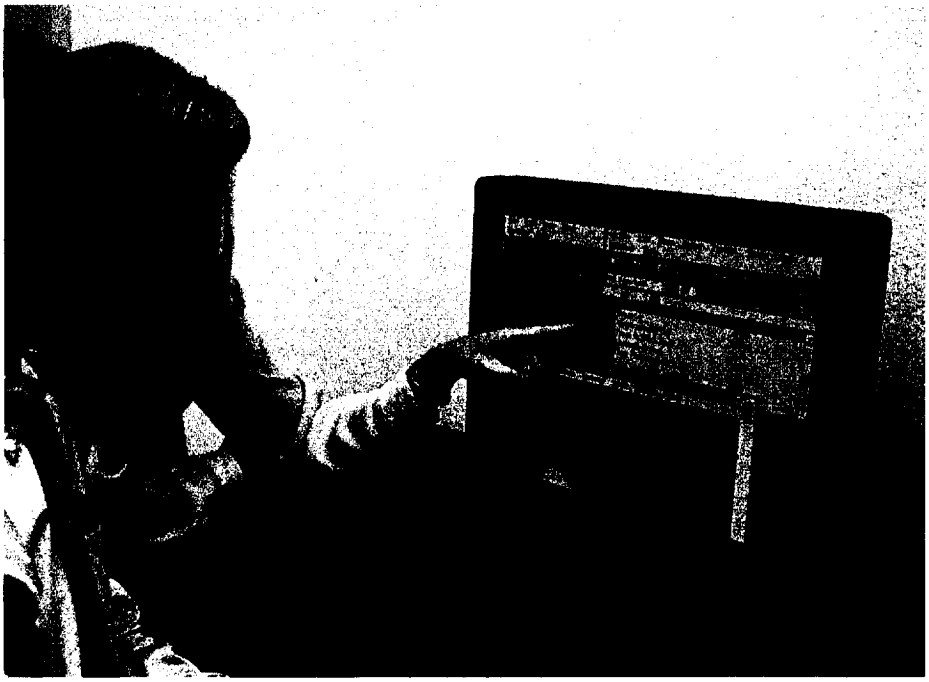
(7) Don't touch the inverter during operation.

(8) The screw to fix the interface cable should be less than 4mm. The long screw occors some display problems.

NEC
NEC Electronics Inc.
CORPORATE HEADQUARTERS
475 Ellis Street
P.O. Box 7241
Mountain View, CA 94039
TEL 415-960-6000

For literature, call toll-free 7 a.m. to 6 p.m. Pacific time: 1-800-366-9782
or FAX your request to: 1-800-729-9288

21 INCH COLOR PLASMA DISPLAY PANEL



Ultra-Thin 21" Display has Viewing Angle of a CRT

Plasma displays have all the advantages of CRTs—high brightness, high contrast ratio, fast response and wide viewing angles—but they are much thinner and lighter than the bulky alternative. The Fujitsu color plasma display panel is sleek and light enough to be hung on a wall, making it ideally suited for limited-space environments. With a viewing angle of more than 140 degrees, groups can watch the screen and see a sharp, clear picture even from the side of the room. The Fujitsu color plasma display panels are ideal as entertainment monitors, teleprompters, public information kiosks and teleconference displays.

- **Winner of two prestigious design awards:**
  - ☛ Voted #1 by EDN Magazine's engineering readers for product innovation
  - ☛ Voted #1 for product development excellence by *Electronic Products*
- **Sleek alternative to the bulky CRT**
  Light and slim enough to hang on a wall
- **World's largest color plasma display panel**
  21 inch diagonal display with 260,000 colors
- **Wide viewing angle — ideal for groups**
  Over 140 degrees, allows off-axis viewing without image distortion
- **Distortion free, flat surface**
  Extremely clear picture from corner-to-corner

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Flat Panel Display Technology - Article

Flat-Panel-Display Technologies in Japan

An update of JTEC's 1991 report reveals a new bullishness toward AMLCDs and a clear understanding that CRTs are here to stay.

by Lawrence E. Tannas, Jr.

In October of 1991 a panel of six experts and five observers visited 33 Japanese sites under the auspices of the Japan Technology Evaluation Center (JTEC).[1] Their mission: to report on the extent to which the Japanese had advanced the state of the art in flat-panel displays (FPDs) in general, and in high-information-content (HIC) liquid-crystal displays (LCDs) in particular.[2-4]

JTEC subsequently asked me, as one of the two co-chairmen of the original JTEC Flat Panel Display Technology Committee (the other was William Glenn of Florida Atlantic University), to do a follow-up study. This is the report of that study.

A recent re-reading of the JTEC Committee's original report leaves me with the conviction that the Committee did a thorough and accurate job of reviewing Japanese FPD technology as it was and seemed to be developing in late 1991. Attendance at the 1992 and 1993 Japan Electronics Shows and recent visits to Japanese FPD manufacturers have convinced me that our predictions of production ramp-up of FPDs in general and active-matrix LCDs (AMLCDs) in particular were, if anything, on the conservative side. In retrospect, this is understandable because the mood in Japan was also conservative at the time. Nonetheless, K. Odawara's recently updated prediction of global display production is essentially the same as was given to the JTEC panel in September of 1991 (Fig. 1).

The figure reflects several fundamental changes in the electronic displays industry:

- In 1989, FPDs became a multibillion-dollar industry, with annual growth rates between 18 and 35%, thanks to the introduction of supertwisted-nematic LCDs (STN-LCDs) for PCs.
- Because of two developments in the 1980s – the STN type of passive-matrix LCD (PMLCD) and the amorphous-silicon (a-Si) thin-film-transistor (TFT) type of AMLCD – LCD flat-panel technology advanced over the last decade to such an extent that it is now orders of magnitude ahead of all other FPD technologies. In addition, AMLCDs with full-color video performance were introduced in the early 1990s.
- The sales of all HIC displays will double in 10 years, corresponding to a compounded annual growth of 7%.
- Because of cost differentials, CRTs will not be replaced by FPDs.
- CRT sales will continue to grow, but at a much slower rate than FPDs.
- By the year 2000, one-half of all HIC display sales will be in FPDs.
- The share of the FPD market captured by AMLCDs and PMLCDs is highly dependent on the technical evolution and cost reduction in these two approaches, as well as on the end-market demand for consumer products. There will be more sales volume in PMLCDs and more sales value in AMLCDs.

What's New?

The present status of the displays industry – exhibited, for example, at JES '93 and the U.S. Consumer Electronics Show – confirms the JTEC study. What is new and was not predictable is the second round of Japan's investment in LCDs: another $2-plus billion over and above the $2-plus-billion figure compiled in the 1990 Nikkei electronic FPD study, updated in late 1991 by Tannas Electronics, and reported by the JTEC Committee.

The new investment is for the second generation of AMLCD production machinery. It comes as a surprise because the JTEC panel was told there would be no second generation of AMLCD machinery until the first generation proved the viability of a-Si TFT-AMLCDs. This viability has now been proved to the satisfaction of Japanese HIC LCD manufacturers.

Price, Price, and Price

The price differential between CRTs and LCDs is immense; 14-in. color CRT televisions are available in Asia at OEM unit prices of $50[5] and 10-in. VGA a-Si TFT-AMLCDs are available at sample prices of about $140 and might be available for $1000 in OEM quantities. Only the highest-tech market segment can afford and use AMLCDs. In a world in which more than half the population still does not have television, the continued production of CRTs is ensured well into the 21st century. (Lower-cost STN-LCDs are still more expensive than CRTs, and offer substantially less performance.)

The price of a-Si TFT-LCDs has been studied extensively in Japan, and the consensus i

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that a price of ¥50,000 ($500) can be achieved by 1996. This consensus arises because the next generation of machinery is expected to provide a productivity of from 3 to 5 times that obtained today. AMLCD factory yields have been significantly improved by many of the Japanese manufacturers, and several of them are now saying they are making a profit.

Profitability and yield have never been an issue with STN-LCDs, which are neither capital intensive nor technically risky. The anticipated price pressure STN-LCDs are expected to exert on AMLCDs will not occur until the production capacity of AMLCDs meets the market demand, which won't occur until more factories come on line with the next generation of manufacturing machinery.

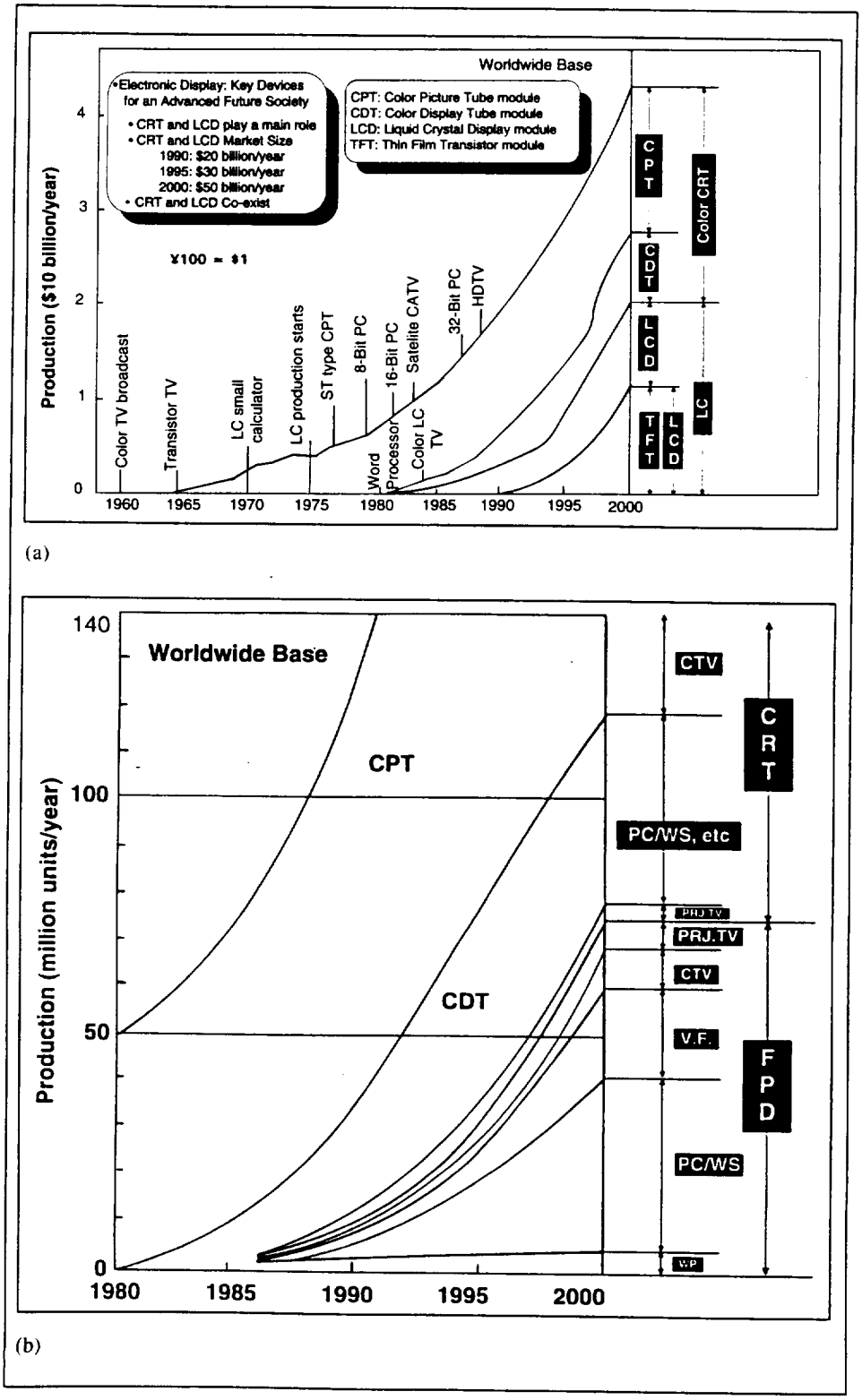
Expanding Applications

There has been a continuing debate whether STN or AMLCD will dominate the HIC FPD market. But rather than converging on one dominant technology, market needs are diverging, which should create long-term application areas for both technologies. If you nsist on an estimate of which technology will have the largest slice of the pie, Nomura Research Institute predicts that a-Si TFTs will have 60% of the HIC FPD market by 1996.

Market applications for all types of LCDs are expanding, and the difference in performance-to-price ratios between a-Si TFTs and STN-LCDs is becoming more sharply defined. Super-MIM, active-addressing, and dual-scan color STNs may find market positions between a-Si TFT and STN-LCDs (Fig. 2).

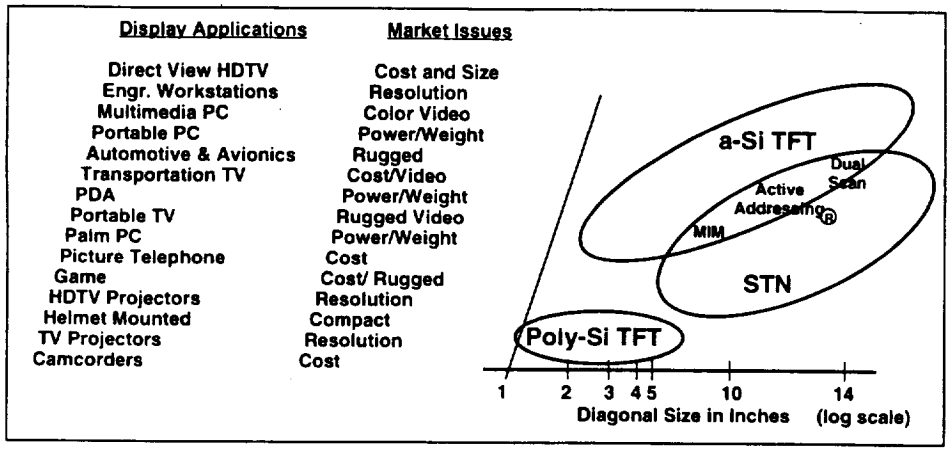
One new product area into which HIC FPDs are expanding is the color camcorder viewfinder. This product was just emerging when the JTEC panel went to Japan in 1991. Now a major component in production by Hitachi and Seiko-Epson, among others, it uses polysilicon (p-Si or poly-Si) TFT-LCDs with integral driver chips made in-situ (Fig. 3). New products, such as virtual-reality goggles and small projectors, are spinning off this component.

A new product made possible by Global Positioning Satellite (GPS) navigation is a moving-map display for automotive, marine, and avionic use. This product – with laser-lisk map storage and player, an LCD displaying maps of Tokyo, a GPS signal antenna, and a processor computing the user's present posi-



Courtesy of K. Odawara, Hitachi, Ltd.

Fig. 1: (a) A September 1993 update of the value of historical and projected display production, along with significant applications developments. (b) Production volume.



Prepared by Tannas Electronics

Fig. 2: Market applications for all types of LCDs are expanding. Super-MIM, active-addressing, and dual-scan color STNs may find market positions between a-Si TFT-LCDs and STN-LCDs.

tion for display on the maps – is now being sold in the Tokyo electronics district of Akihabara for $2000 (Fig. 4).

Thus far, the engineering workstation market has not been penetrated by FPDs because there aren't any FPDs on the market with sufficient size and resolution. But AMLCDs capable of workstation-level performance have been demonstrated (see cover) and could go into production between 1996 and 1999.

An AMLCD of workstation size will present the marketplace with an interesting paradox and will, for the first time, present a direct challenge in a market now dominated and satisfactorily served by the CRT. The AMLCD itself will be much more expensive than the CRT, but for the first time users will have an opportunity to replace the bulky CRT with an FPD and recover valuable desktop space. It will be interesting to see how much of a premium the marketplace will pay for this opportunity.

The price differential between CRTs, AMLCDs, and PMLCDs is a major issue. The different prices buy a different mix of attributes in each technology (Table 1). Whether LCDs can penetrate the workstation market will depend upon a delicate weighing of these metrics.

The FPD industry is going after HDTV in several ways:

- a-Si TFT-LCD projectors – Sharp and Sanyo
- p-Si TFT-LCD projectors – Seiko-Epson and Sharp
- Direct-view AMLCDs in research – GTC (Hitachi)[6]
- Direct-view PDPs in research – NHK and Matsushita

Despite the research activity, there is not yet an obvious solution to the problem of making a consumer-priced display for HDTV.

Another important product is the personal digital assistant (PDA). This product is emphasizing displays with VGA resolution but with smaller dimensions than we usually see in VGA displays. PDAs, along with other portable and pocketable electronic devices, are focusing attention on display ruggedness, as well as on reduced weight and volume. A similar display is used in camcorders (Fig. 5).

At JES '93, Sharp addressed this market by showing a display fabricated on plastic rather than glass. Interestingly, reducing the cost of the display was *not* among the reasons Sharp used plastic. The common conception that a plastic substrate reduces the cost of an FPD is incorrect.

LCD Production in Japan

The increase in the value of LCD production in Japan is a dramatic story, and it coincides with a production volume that is actually decreasing as the production of lower-technology and lower-pixel-count PMLCDs go to other parts of Asia (Fig. 6). The Nomura Research Institute/Sharp has forecast a growth rate in market value of 35%, which produces a dollar value of $15.6 billion by the year 2000 (Fig. 7).

Next-Generation Production Machinery

In 1991 the JTEC Committee visited brand-new Sharp and DTI AMLCD factories incorporating first-generation machinery – machinery that can handle glass substrates measuring approximately 300 × 400 mm using larger PECVD and photolithographical exposure equipment than had ever been used before in production. We were impressed by the expense of the machines and the stipulation that these machines would have to pay for themselves before any further developments could be considered. The first-generation machines were not on line during our visit and the future was uncertain. The yields on "zero-generation" AMLCD pilot lines factories using modified MOS machines were rumored to be less than 10%.

At that time, many people in the displays industry believed that AMLCDs could not be produced profitably because first-generation machines would be unable to process enough glass at sufficient speed and yield. Obviously, Sharp, DTI, NEC, Hosiden, and other companies disagreed, but no one was willing to speculate beyond the first generation.

In 1991 there was clearly a high technical, financial, and market risk. Among the many considerations that tempered commitment to a-Si TFT-AMLCDs were:

- The unresolved question of whether a-Si TFT-AMLCDs could be manufactured economically.
- Technical challenges from MIM and a-Si diodes, p-Si TFTs, and improved lower-cost STN-LCDs.
- Uncertainty over whether the market would accept the most expensive electronic-display product ever offered.
- The absence of a proven consumer market for any high-performance FPD with full color and video speed.
- New technical breakthroughs in other FPD technologies that could mitigate the advantages of a-Si TFTs.

The industry's direction and rate of change were both unclear, and the obvious technical advantages of a-Si TFTs were clouded by market and economic issues.

It is now time to update the appraisal of 1991. The technical, financial, and market risk is over. It is now clear that:

- The technical manufacturability of a-Si TFT-AMLCDs has been proved and the

industry is improving performance.

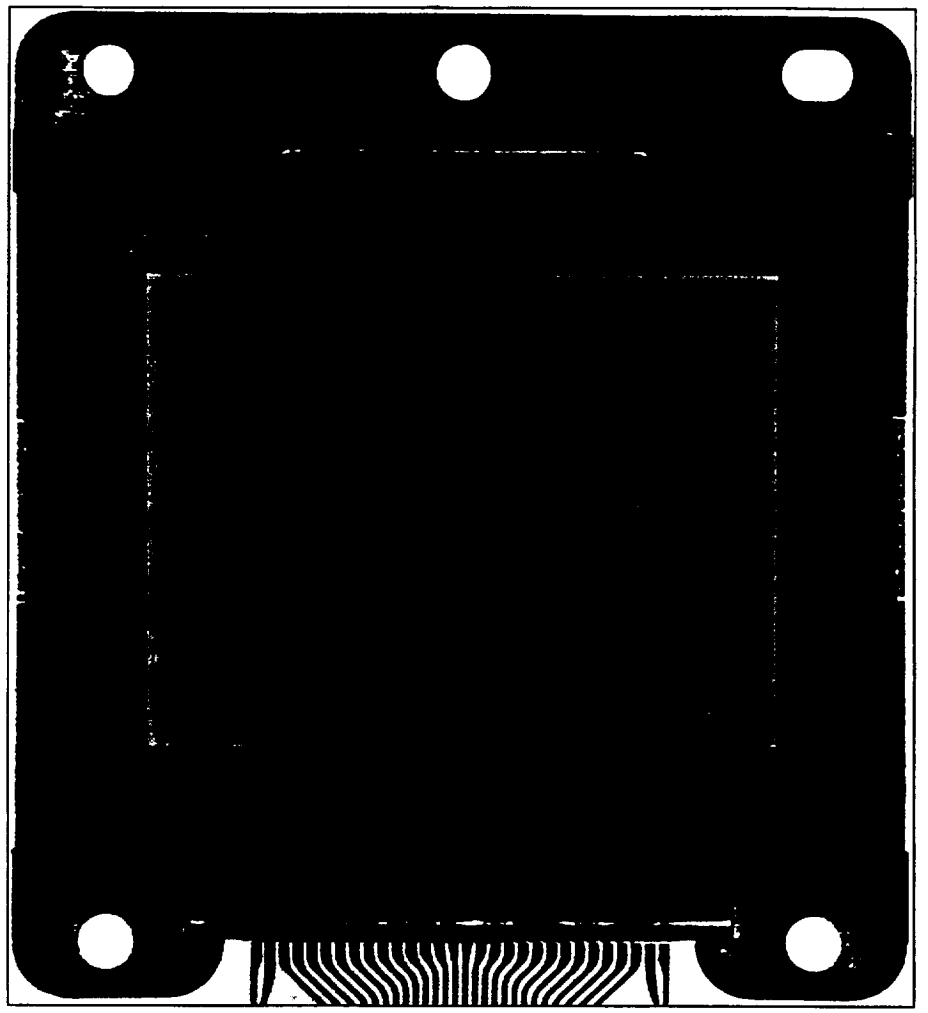
- The financial risk is over. The industry is vigorously working on product cost reduction, and the Japanese AMLCD industry is expanding despite the general slowdown of the global economy. Several AMLCD manufacturers say they are making a profit. The industry is now progressing to the second generation of machinery, which has 3–5 times the productivity of the first generation (Tables 2 and 3).
- Market demand exceeds production capacity. The marketplace has focused on a product size of approximately 10 in. on the diagonal, with VGA resolution and 9–18 bits of color. The focus is on products that use a-Si AMLCDs because of their superior performance and speed of response. The greatest growth is in high-end portable PCs. The PMLCD market is also very strong and growing at a rapid rate.

The new round of investment is the ngest statement the Japanese displays ndustry could possibly make about its commitment to LCDs. The sample of reported investments shown in Table 3 exceeds $2 billion – that's $2 billion above and beyond the more than $2 billion reported in 1991. NEC is leading the charge toward second-generation machinery; installations started in late 1993. In late 1992, Sharp announced its largest single capital investment ever – ¥80 billion – which included new machinery for a new line, machinery upgrades on the first two lines at the 3-year-old Tenri factory, and a new factory in Mie Prefecture.

The new round of investment is causing a shakeout of Japanese AMLCD manufacturers. The cost of entry is now so high that we are not likely to see new manufacturers entering the marketplace. Sharp is now, by far, the world leader in the production of PMLCDs and AMLCDs, and may capture 50% of the world's AMLCD market by 1995.

Second-Generation Production Machinery

The a-Si TFT-AMLCD industry is now fol- wing the same growth pattern we have seen he MOS, DRAM, and microprocessor ndustries (Table 2). Note that the technological life of production machines is expected to be approximately 3 years while production

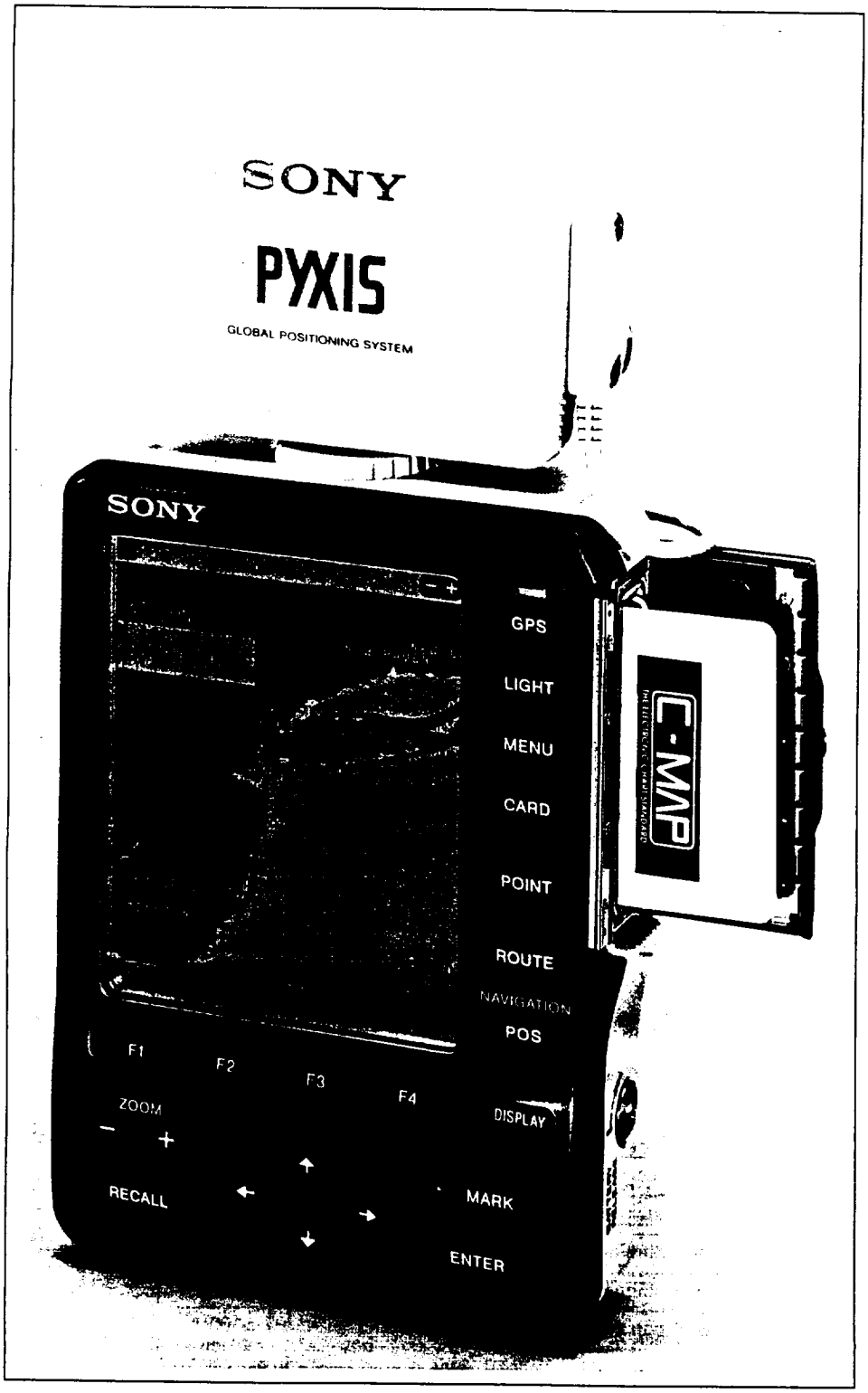


Target Specifications for 1.3-in. Polysilicon Liquid-Crystal Display

Item	Specifications
Module size (mm)	38 (H) × 42 (V)
Display-area dimensions (mm)	26.88 (H) × 20.16 (V) (1.32-in. diagonal)
Number of dots	640 (H) × 480 (V)
Dot pitch (μm)	42 (H) × 42 (V)
Aperture ratio	0.3
Transmittance	0.07
Contrast	>100:1
Response time	50 msec at 25°C

Seiko-Epson

Fig. 3: Seiko-Epson has introduced this new 1.3-in.-diagonal poly-Si AMLCD having 480 × 640 color pixels – 307,200 addressable dots. Seiko-Epson expects to have engineering evaluation units ready for the Japanese market in June.



Sony Corp.

Fig. 4: The newest Sony Portable Global Positioning System (GPS) was released in September. It uses the C-Map Marine Database on a removable Info-Card. For portability, the system uses an STN-LCD.

life may be as long as 7 years. Quantum jumps in size and market are anticipated every 3 years. It is too early to confirm many of the details for generations 3 and 4, but generation 2 has started with NEC.

Extrapolations of when new generations come on line may change with time, but the evolutionary stage is set. Upon that stage, corporate actors will adjust their tactics as shifts in the marketplace demand – and as the electronics industry has often done in the past.

One ramification of the dramatically increased confidence in the FPD industry is that the required broad base of industries has become more supportive. The chemical, glass, printing, electronics, and machinery industries, as well as all of the other industries associated with displays manufacturing, are investing in new plants and capacity.

The JTEC Committee predicted that AMLCD production would not exceed 16 in. by the year 2000, but Sharp demonstrated a 17-in. 1024 × 1280 full-color AMLCD at JES '92 and '93. Samples of sizes over 14 in. on the diagonal may be available from Sharp in the 1995-1996 time frame. Matsushita demonstrated a 15-in. 900 × 1152 full-color AMLCD at JES '92 and '93. Matsushita is sampling the display in Japan but has not announced plans to sample it in the U.S.

Significant Advances

The most significant technical movement within AMLCDs since the original JTEC study has involved the p-Si TFT-AMLCD. The market driving force for this device has been the 0.7-in. 100,000-subpixel color camcorder display. Seiko-Epson has demonstrated a 480 × 640-subpixel color p-Si TFT device that has a 1.3-in. diagonal (Fig. 3).

A second market driver is the p-Si TFT-AMLCD for video projection of TV and HDTV. Perhaps the most significant LCD advance shown at JES '93 was the Sharp HDTV p-Si AMLCD projector (Fig. 8). As exhibited, the display substrate was approximately 1.9 in. on the diagonal with 1.3M pixels (monochrome). Such substrates can be used for color HDTV projectors and, in a truly impressive exhibit, Sharp was using them in that configuration to project an image on a 10-ft. screen. (Two HDTV projectors projected superimposed images for added luminance.)

At SID '93 in Seattle, Washington, Sharp described the device in a technical paper.[7]

p-Si appears to be emerging as the technology for the smaller and larger projectors, viewfinders, goggles, and direct-view displays. Examples of all these applications – including a rear-projection desktop-PC display, virtual-reality goggles, camcorder viewfinders, monocular displays, and direct-view displays – were shown at JES '93. There were no signs of p-Si in devices larger than 2 in. on the diagonal.

In 1991 most projectors used a-Si TFTs. The p-Si TFTs have gained on a-Si for several reasons:

- Lower sensitivity to light, which permits higher luminous flux density.
- Row and column drivers fabricated on the substrate along with the TFTs for pixels, allowing higher-resolution images.
- High-resolution images obtainable from devices with smaller diagonals, which allow the use of smaller optics and smaller projectors.
- Higher-mobility TFTs that can be smaller for a larger pixel aperture.

A second area of dramatic advances is in more-compact displays with highly efficient fluorescent backlights. Two examples, in particular, have established a new level of accomplishment in the use of advanced backlights for FPDs.

The first of these was demonstrated by Sharp at JES '93. It is an a-Si TFT-AMLCD with 480 × 640 × 3 subpixels – 480 rows by 640 columns of full-color pixels, with each pixel containing a red, a green, and a blue subpixel – on a 0.2-mm pitch. It is 6.4 in. on the diagonal, has 2% reflectivity of ambient light for good sunlight readability, weighs 220 grams, and consumes 1.5 W.

The second example was first demonstrated by Hitachi at JES '92. It is an a-Si TFT-AMLCD with 480 × 640 × 3 subpixels. It is 9.4 in. on the diagonal, displays 4096 colors, weighs 590 grams, and consumes 6 W.

A third rapidly advancing area is in STN multiple-row addressing (also known as active addressing, a term that has been registered as a trade name by In Focus Systems). At JES '93, Optrex showed a color STN display with VGA resolution that uses multiple-row addressing in sets of seven rows. The speed response was 50 msec – about the speed of a typical a-Si TFT-AMLCD. Optrex said that the preprocessing required to achieve this increased speed would raise the cost of the STN display by 20%. Seven-row sets were considered optimum for increasing speed while maintaining conventional STN viewing angles and contrast ratio.[8]

Table 1: Metrics for a 10-in. VGA Monitor
A Technology-by-Technology View

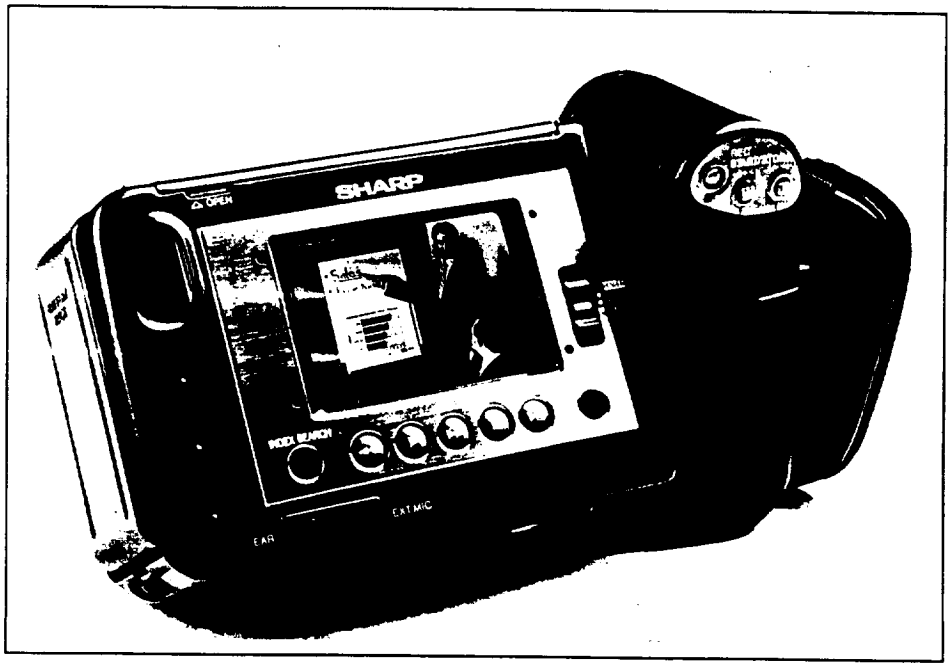
Technology	Price	Speed	Color	Footprint	Weight	Power	Viewing Angle	Sunlight Readability*
CRT	E	E	E	M	M	F	E	M
AMLCD	M	G	E	E	E	G	G	E
PMLCD	G	M	F	E	E	E	F	E

Legend: E = excellent; G = good; F = fair; and M = marginal.
*Sunlight readability refers to a display's ability to be adjustable for and readable in ambient illuminations from full darkness to full direct sunlight.

Reduced Emphasis

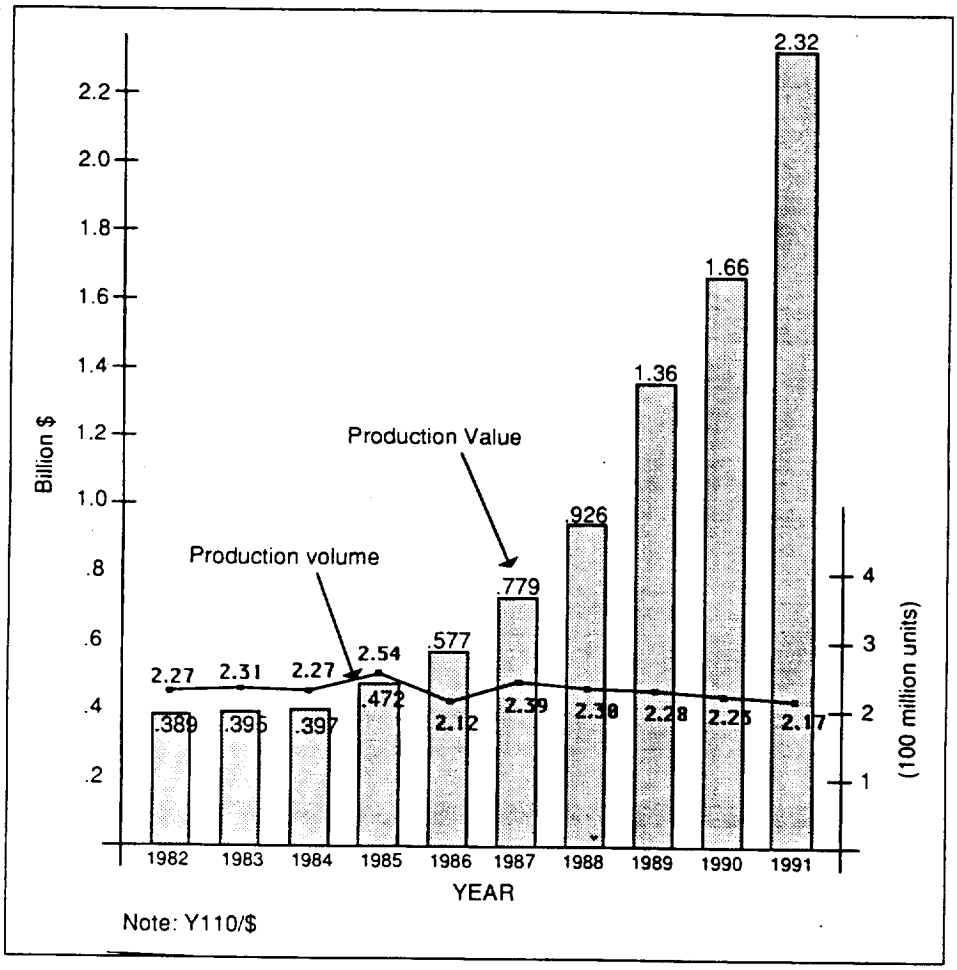
Several areas mentioned by the 1991 JTEC Committee have not materialized to the extent we expected or they are not being renewed.

- The ferroelectric LCD (FLCD) being developed by Canon has not reached production as anticipated. Canon will continue research and development on FLCDs.
- Stanley's electrically controllable birefringent (ECB) PMLCD configuration – also called the vertically aligned configuration – has not reached production as anticipated. This configuration was developed by LETI of France and developed further for production by Stanley in a joint agreement between the French and Japanese Governments.
- The Giant Technology Corporation (GTC) consortium, which has been headed by Hitachi, will come to an end as planned. GTC was initiated as a 5-year research and development effort to make a 1-m HDTV display using p-Si for



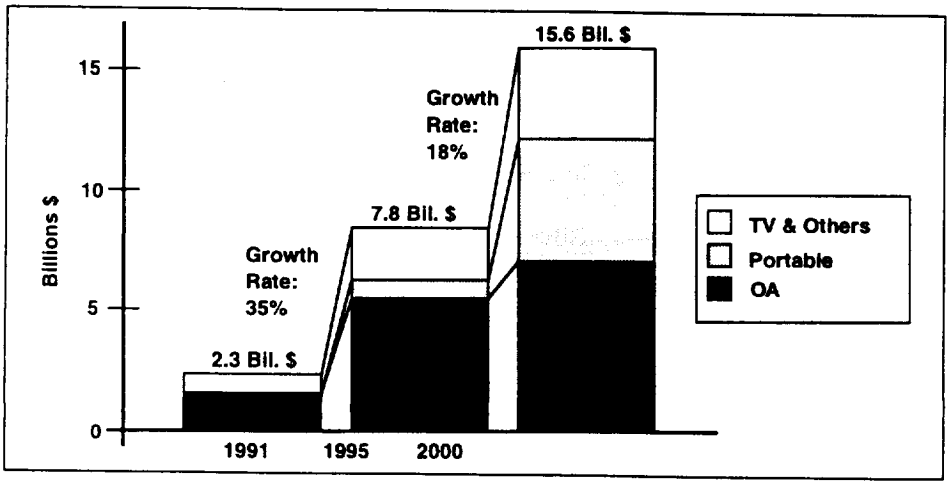
Sharp Corp.

Fig. 5: The new Viewcam™ VL-E3OUP by Sharp Corp. uses a 3-in.-diagonal color a-Si TFT-AMLCD for its innovative viewfinder. This new application of LCDs, which required increased viewing angle and decreased reflectivity, has had a major impact on camcorders.



Source: Japanese Ministry of International Trade and Industry

Fig. 6: The increase in the value of LCD production in Japan is dramatic, and it coincides with a production volume that is actually decreasing as production of the lower-technology and lower-pixel-count PMLCDs go to other parts of Asia.



Source: Nomura Research Institute/Sharp

Fig. 7: A forecast growth rate of 35% in the market value of LCDs produces a dollar value of $15.6 billion by the year 2000.

TFTs and printing in place of the standard photolithography process. The consortium plans to build a 20-in. breadboard demonstrator, which will be a section of the 1-m panel.

- The High Definition Technology Corporation (HDTEC) consortium headed by Seiko-Epson will come to an end as planned. HDTEC was initiated as a 5-year research and development effort to make a p-Si HDTV projector. The consortium has made significant progress.

Other FPDs

The entire FPD industry is dominated by LCD technology, but there are important niche-market activities involving other technologies:

- ***The 21-in. VGA color plasma display developed by Fujitsu.*** Fujitsu is sampling the display and building a factory for modest production. The display was demonstrated at JES '92 and '93 with full multimedia capability. The PDP technology is well-suited to larger sizes because it uses screen printing for pixel definition. It has the disadvantage of low luminous efficiency, which limits its ultimate application unless significant materials improvements are made. At the present time, the PDP is the only direct-view FPD that can (1) be made with a diagonal over 20 in., (2) operate in full color, and (3) operate at video speeds.
- ***The 40-in. PDP with near-HDTV display resolution developed by NHK and Matsushita.*** This is the only existing direct-view display that approaches HDTV resolution and size requirements. The technology currently lacks efficiency, long life, and luminance. Further research and development is necessary before production can be anticipated.
- ***The flat CRT display developed by Matsushita.*** Matsushita continues to develop and demonstrate flat CRTs, and showed a high-quality 14-in. color version at JES '93. But the weight, size, and cost parameters do not hold promise that these displays can compete with AMLCDs. One market application well-suited to the flat CRT, with its wide viewing angle, is "TV on the wall," but this will be a niche market until the price is decreased and the size is increased.

Table 2: AMLCD Machinery Production Generation in Japan
Direct-View a-Si TFT-LCDs

Generation	Zero	1st	2nd	3rd	4th
Year start	1987 LSI	1990 New generation	1993–94 Installation	1996 Planning	1999? Future
Glass sheet size	6 × 6 in. 6 × 8 in.	320 × 400 mm 300 × 350 mm 300 × 400 mm	360 × 465 mm 380 × 480 mm (1994)	500 × 700 mm 500 × 600 mm 450 × 550 mm	TBD
Display size	1 @ 6 in. 1 @ 9 in.	4 @ 8 in. 4 @ 6 in. 2 @ 10 in.	4 @ 10 in. 2 @ 14 in. 6 @ 7 in.	4 @ 14 in. 1 @ 30 in.	
Cycle time	Variable	normalized @ 1	2×		
Productivity		normalized @ 1	3× to 5×		
Yield	<10% initially	>50%	>70%		
Major market	Portable TV	Notebook PC	Desktop PC Subnotebook PC	Engineering workstation	HDTV?

Machine technology life, 3 years.
Machine production life, 7 years.

Source: Tannas Electronics, Orange, California

- ***The Sharp line of EL displays.*** This technology supplied the first HIC FPD manufactured for a consumer product. (PDPs were the first type of FPD manufactured, but they were initially limited to military and industrial markets because of their cost.) Sharp is the only Japanese company manufacturing ELDs – in a product line of approximately a dozen sizes. Sharp claims to have over 50% of the world's market in ELDs.

ELDs have the advantage of wide viewing angle and a fast response speed comparable to a CRT's. They have the disadvantage of limited color capability and limited gray shades. ELDs are several times more expensive than STN displays that are comparable in all respects except speed and viewing angle. Sharp is continuing research to develop a white-color phosphor.

Summary

The Japanese have long recognized that both the computer and television industries will need new display technologies as we enter the "Information Age," and that these new technologies will play a critical role in keeping Japan's electronic products competitive in the international market. Japanese industrialists have thought of FPDs as the last remaining "seed" for new-product innovation. In part, this helps explain Japan's apparent overemphasis on the research and development of FPDs during the last 20 years.

During the 1980s Japan's electronics industry achieved worldwide dominance in FPDs generally and LCDs in particular. FPDs made it practical to produce new products that stimulated the entire Japanese electronics industry.

All the pieces have now been assembled that will allow Japanese laboratories, universities, and companies to dominate the research, development, and production of HIC FPDs. This situation appears more obvious now than in 1991. The dominance is based on phenomenal advances in LCD technology in both the low-cost compensated STN-LCDs and the high-performance a-Si TFT-AMLCDs.

However, one should not assume that these technologies will displace the CRT. They won't because of the CRT's lower cost and high level of performance – except in markets where physical volume, footprint, or sunlight readability are issues. By the year 2000,

Table 3: New Round of Investment for Large AMLCDs
(Partial List, 1993–1995)
Second-Generation Machines

Company	$M	¥B	Plans
Sharp	727	80	Upgrade two Tenri lines Add line at Tenri New plant in Mie Prefecture
NEC	272 273	25 30	Upgrade Kagoshima plant New plant at Akita
DTI (Toshiba/IBM)	273	30	Expand Himeji production line
Hosiden	64	7	Expand Seishin plant ('93 only)
Fijitsu	355	39	Begin mass production
Hitachi Ltd.	273	30	New line at Mobara
Total = >$2 Billion			

Source: Tannas Electronics, Orange, California

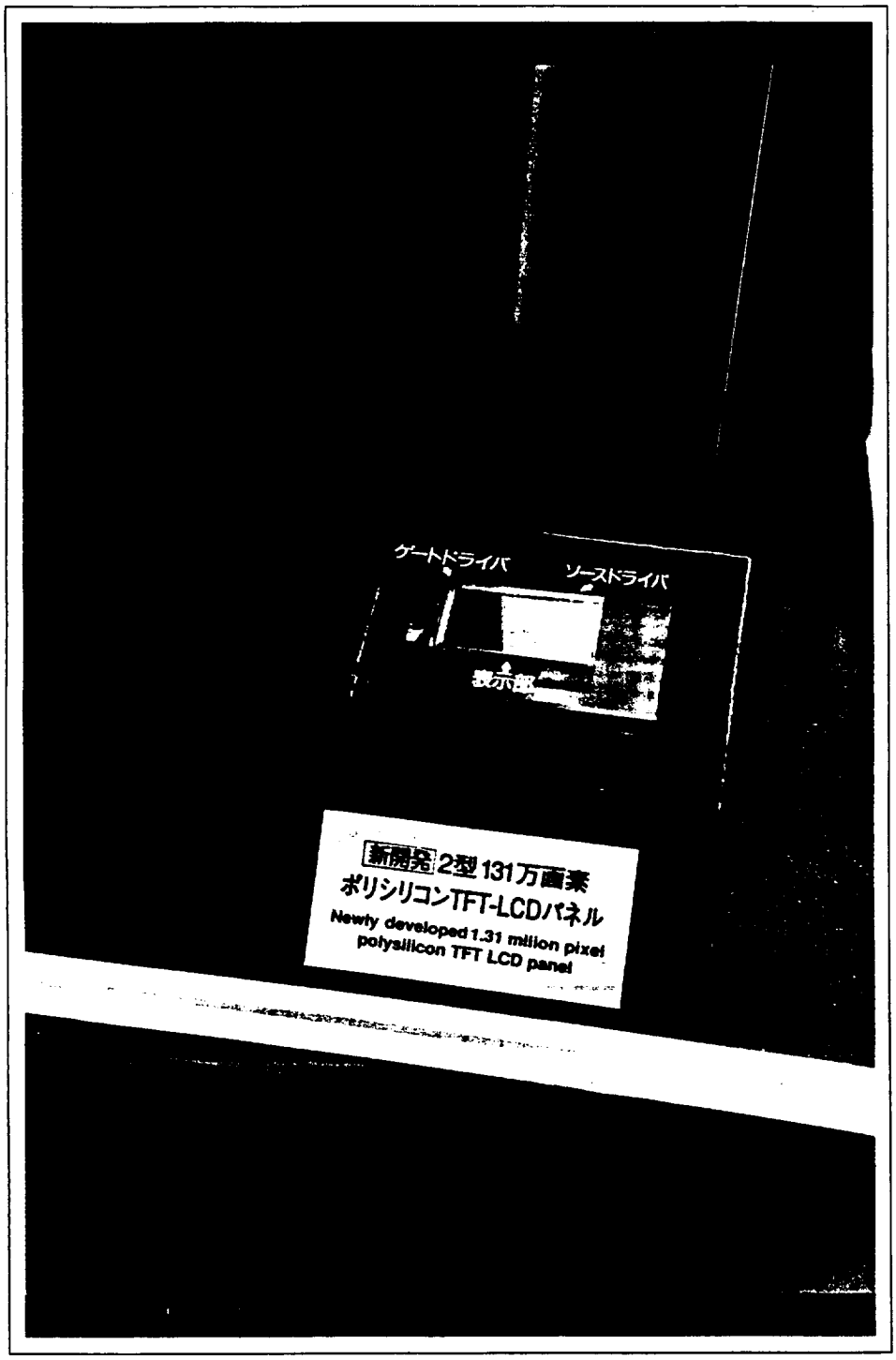


Photo courtesy of L.E. Tannas, Jr.

Fig. 8: *The first showing of a poly-Si active-matrix liquid-crystal display (AMLCD) with high-definition-television (HDTV) resolution and aspect ratio was by Sharp Corp. at the 1993 Japan Electronics Show (JES '93) in an HDTV projector/theater. No technical details were revealed and an availability date was not given.*

worldwide sales of CRTs and LCDs are expected to be about equally divided, with the growth in LCDs occurring primarily in new display-based products.

LCDs now completely overshadow all other flat-panel technologies, another statement that appears more obvious today than it did to the JTEC Committee in 1991. The development during the 1980s of techniques to successfully matrix address high-resolution LCDs is bearing fruit in the 1990s.

Successful production of color AMLCDs and low-cost STN-LCDs in Japan has changed the entire picture in the FPD industry. Of all the FPD technologies, the LCD will dominate through the 1990s and beyond. A new paradigm must be created before this can change.

AMLCD production is maturing rapidly and is starting to follow the evolutionary pattern previously seen in the MOS and DRAM industries. The second round of investments and second generation of machinery for AMLCD production is the ultimate confirmation that LCDs are firmly in place and guaranteed to be with us well into the 21st century.

The achievements in AMLCD technology are the most significant since the invention of the shadow-mask color CRT, and there is no close rival left for high-performance color video displays except the CRT itself. It is even conceivable that by the year 2000 the AMLCD may be superior to the CRT as an HIC electronic display. But regardless of FPD performance, the CRT will remain a potent force because of its absolute price advantage and the worldwide need for low-cost television sets. As yet, no one is predicting that the cost of FPDs will ever be competitive with that of CRTs.

Notes

[1]The Japan Technology Evaluation Center (JTEC) is operated for the U.S. Federal Government to provide assessments of Japanese research and development in key technologies. The lead support agency is The National Science Foundation.

[2]JTEC Flat Panel Display Technology Committee, L. E. Tannas, Jr., and William Glenn, Co-Chairmen, "Display Technologies in Japan," NTIS Report #PB92-100247

(National Technical Information Service, phone 703/487-4650, June 1992).
[3]L. E. Tannas, Jr., "Japanese Flat-Panel Displays: What JTEC Saw," *Information Display*, 18-22 (July/August 1992).
[4]In this article, we define an HIC display as one with 100,000 or more pixels – a pixel count that historically required a CRT.
[5]K. Odawara, private communication.
[6]Giant Technology Corporation (GTC) is a consortium funded by MITI and the Japan Key Technology Center with the single objective of researching and developing a 1-m HDTV display that uses p-Si as the TFT semiconductor and is fabricated with high-resolution printing instead of the more expensive photolithography.
[7]Y. Takafuji *et al.*, "A 1.9-in. 1.5-M Pixel Driver Fully-Integrated Poly-Si TFT-LCD for HDTV Projection," *SID International Symposium Digest of Technical Papers*, 383-386 (1993).
[8]Takeshi Kuwata, Asahi Glass Co., Ltd., R&D Center, Kanagawa, Japan. Private communication. ■

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Flat Panel's Future - Article

The flat panel's future

Notebook PCs and wall-mounted, high-definition TVs define the fast-changing world in which display makers must survive

The Japanese giants of the flat-panel display industry—Sharp, NEC, DTI (a Toshiba-IBM joint venture), Hitachi, and Hosiden—have spent an estimated US $3 billion to commercialize the color, active-matrix liquid-crystal display. Now that heavy investment is starting to pay off.

Less than three years ago, manufacturing yields of color liquid-crystal displays (LCDs) based on active-matrix technology were a dismal 10–20 percent for most manufacturers. Today, the leaders among them are—with evident satisfaction—claiming yields in excess of 50 percent. As a result, prices are down (a little) and, according to industry consultant Larry Tannas, chairman of the Japan Technology Evaluation Committee (JTEC) on display technology, Video Graphics Adapter (VGA) versions of these displays are being delivered this year. With additional manufacturing capacity now going on line, next year an estimated 500 000 displays will be produced each month, Tannas said. But even with this additional output, supply is not expected to catch up with demand until 1996.

The image quality on the best displays is stunning (Fig. 1). Sizes also are inching up. Prices, though, are still too high for color active-matrix LCDs (commonly called AMLCDs) to be a truly mass-market item. After all, how many $4000 laptop computers will people buy?

Prices will drop, but the long-predicted target year of 1995 will not see a color VGA AMLCD priced at ¥50 000 (or US $500 at a projected ¥100 to the dollar). A more realistic estimate is 1996 or 1997, said Hosiden Corp.'s Shinji Morozumi, developer of the AMLCD TV receiver, when he spoke in Seattle last May at SID '93—the annual Society for Information Display's International Symposium and Exhibition.

With all of this, the Japanese giants and their North American marketing groups seem generally optimistic, but new technologies—such as the active-addressing display from Motif Inc., Wilsonville, OR, or the plasma-addressed unit from Tektronix Inc., Beaverton, OR—threaten to cloud at least a portion of active matrix's rising sun.

Kenneth I. Werner Contributing Editor

PASSIVE PROBLEMS. AMLCDs are complex, but the complexity is there for good reason. In the simpler, passive LCDs like the super-twisted nematic (STN) units used in most monochrome notebook computers [Fig. 2], a tradeoff limits display performance. Because the rows in such displays are addressed sequentially, the number of rows of pixels in the display must be traded off against the length of time during a frame period that the driving circuitry can apply voltage to a turned-on pixel.

For instance, if there are 240 rows, any pixel that is turned on during that frame period can only have its on-voltage applied to it for approximately 1/240 of the frame period—which is generally 1/60 second. This time division of voltage is called multiplexing, and the portion of the frame period that each on-pixel experiences the voltage is called the duty cycle.

Thus, any pixel in a 240-row display would have a maximum duty cycle of 1/240. All other things being equal, the smaller the duty cycle, the poorer the contrast ratio, the narrower the viewing angle, and the fewer the gray levels.

Another potential problem with passive display designs is crosstalk. In display technology, crosstalk is the tendency for pixel intensities in a column containing both on- and off-pixels to vary around their intended values. Modern displays exhibit crosstalk to varying degrees. It is particularly noticeable in a windowed environment where, for example, the vertical edges of a dialog box may have a ghostly continuation beyond the box's horizontal edges.

To avoid flicker in passive displays, a relatively viscous and slow-to-respond liquid-crystal material must be used. This solves the flicker problem but prevents the display from responding quickly enough to reproduce video signals or allow a mouse cursor to be moved rapidly across the screen without submarining—temporarily disappearing as it is moved.

A pixel turn-on time, T_{on}, of 125 ms is on the borderline for keeping moving mouse cursors visible and, for video, 50 ms is needed. Some of the latest passive displays appearing in laptop computers exhibit a T_{on} in the vicinity of 125 ms. (T_{on} is commonly referred to as one-way optical response time. Two-way response time, $T_{on} + T_{off}$, is also a frequently cited specification. It is approximately double the one-way response in most displays.)

Active-matrix LCDs were developed to overcome these limitations of passive displays. In the early 1970s Peter Brody and his group at Westinghouse Corp., Pittsburgh, recognized that placing a switch at each pixel location was one way of avoiding crosstalk and optical response tradeoffs forced by time-multiplexing the driving signals. The Westinghouse group employed a transistor fabricated with thin films of semiconducting material.

ACTIVE DEVELOPMENT. Researchers experimented with cadmium selenide and other materials. But since the quality of this thin-film transistor did not have to be very high, by the early 1980s most developers had settled on amorphous silicon as a good compromise between adequate performance and an economical, low-temperature manufacturing processing.

But a color VGA display contains 640-by-480 full-color pixels, and each full-color pixel in most designs contains a red, a green, and a blue subpixel. (Some older designs add a fourth, either white or green; at least one manufacturer stacks three panels and uses subtractive primaries to obtain colors by subtraction.) Since each AMLCD subpixel requires a transistor, a 640-by-480-pixel display that uses three subpixels for each color pixel requires over 920 000 transistors, which must be deposited on one 9- or 10-inch substrate. With a few minor exceptions, all these transistors have to work.

The problem has been likened to making perfect 10-inch ICs with 3-μm design rules at high yield. Its solution has proved far harder and costlier than anyone foresaw. Some analysts say that the $3 billion invested to date will never be recovered using

Defining terms

Liquid-crystal display (LCD): a display in which the opacity of a gelatinous quasi-crystalline material is controlled by an electric field.

Optical response time: the amount of time it takes for an LCD pixel to change opacity.

Pixel duty cycle: the portion of the entire display cycle during which an address signal is applied to a single pixel to turn it on.

Transmittance: the amount of light able to pass through a material, given as a percentage of the light entering it.

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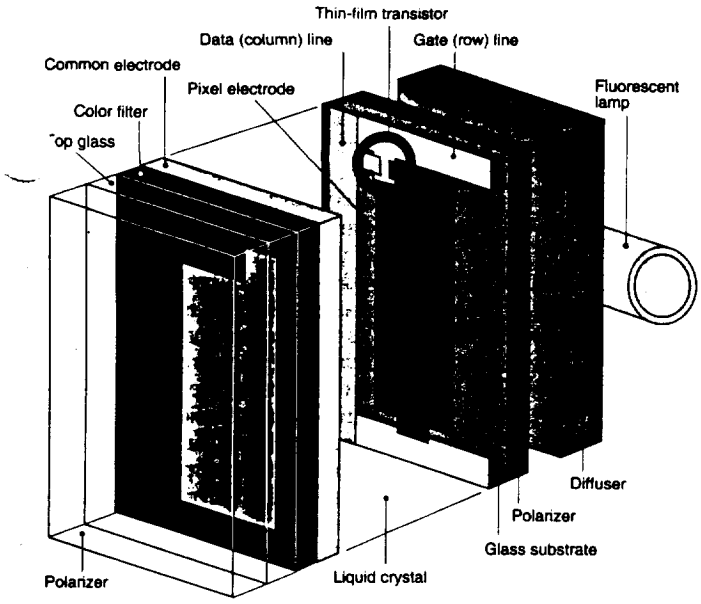
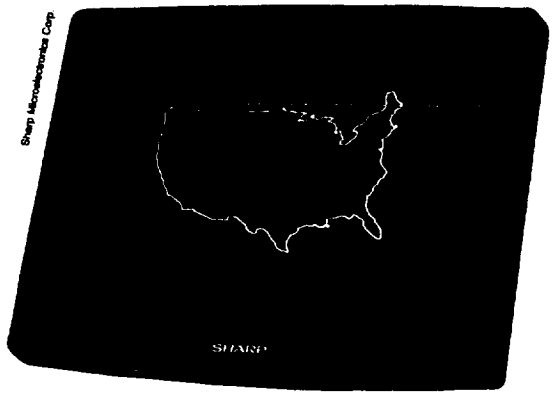
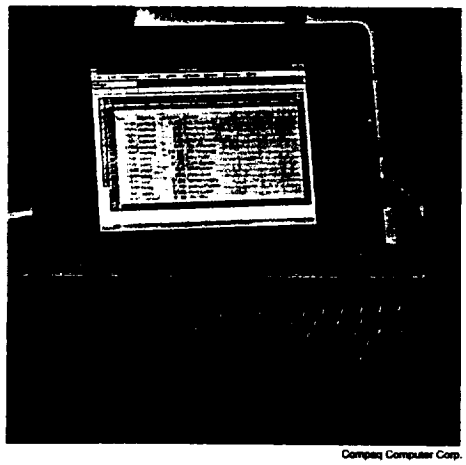
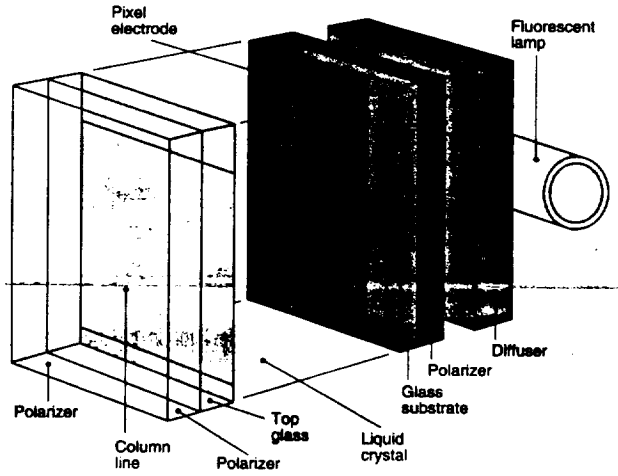




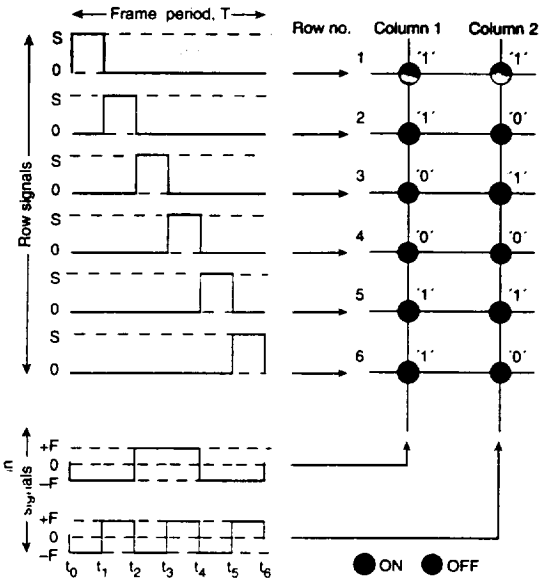
[1] Among the most sophisticated commercial color liquid-crystal displays (LCDs), Sharp Microelectronics Corp.'s 10.4-inch active-matrix LCD display [above] exhibits thousands of colors. Like other top-of-the-line displays, it is based on thin-film transistor technology [left].

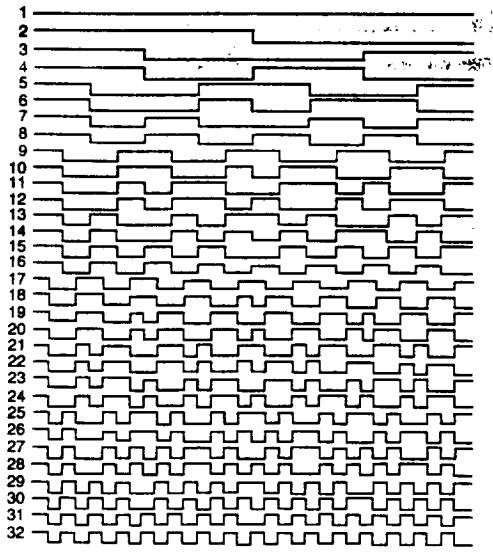
[2] Passive LCD technology [far right] is simpler than active-matrix. The pixel count, contrast ratio, response, and gray scale of top-of-the-line passive LCDs are gradually increasing to provide a crisper, more pleasing display, such as that used in Compaq Computer Corp.'s most recent notebook computer [right].





[3] In a traditional passive-matrix liquid-crystal display, a pixel is turned on by an "on" column signal during the time it is selected by a row pulse [left]. Each pixel experiences a voltage that is the difference between the row and column signals. F is a voltage selected to produce the desired pixel response. The column signal is set to −F to turn a pixel on, +F to turn or keep it off. (The pulse width, t, is equal to the frame period—usually about 1/60 second—divided by the number of multiplexed rows.) The column signals shown are intended to produce a binary display—one whose pixels are entirely on or entirely off—but crosstalk hampers full realization of this intention. In active addressing of a passive display, a much more complicated set of row functions [right] makes it possible to use a faster liquid-crystal material, retain a flicker-free display, and eliminate crosstalk. Any set of orthonormal functions will work, but the approach requires the column voltage to be a function of every pixel in the column. Walsh functions—the set of order 32 is shown—are a set of functions that can sharply reduce the number of computations needed to generate the column signals. (Figures courtesy of Terry Scheffer and Jürgen Nehring at Motif.)





traditional measures of cost recovery. Whether or not these costs really can be recovered, the extremely high manufacturing investment required to make AMLCDs affects both suppliers and consumers.

Only seriously committed suppliers can enter this game, and only successful ones remain in it. The price tag for the equipment in a single, state-of-the-art AMLCD production line exceeds $100 million, said consultant Tannas, and industry leaders are now adding second and third lines.

Several Japanese companies that had been actively involved in AMLCD development have decided to fold their cards. Outside Japan, only two North American companies—Optical Imaging Systems (OIS), Troy, MI, and Litton Canada, Toronto—are making the displays, and only one new player, a consortium led by Philips Electronics NV, Eindhoven, the Netherlands, has summoned the courage to build a full plant for active-matrix LCD manufacturing.

For consumers, the price of color VGA AMLCDs cannot drop sharply before the second half of this decade, even if yields rise to 70 or 80 percent, because manufacturers need to recover the cost of building the plants scheduled to go on line next year.

Given the continuing prospects for high AMLCD prices, therefore, could there be a window of opportunity here for other technologies? In fact, there are at least two, and they are related by their reliance on the innovative use of factory-proven approaches.

The most recent alternative cropped up in 1992, when Terry Scheffer and his colleagues at In Focus Systems announced a new method for driving passive LCDs that would give them most of the benefits of active-matrix displays.

Traditionally, in both active and passive displays, the display signal is applied to the columns of pixels in parallel while the rows are pulsed sequentially. Each pixel is exposed to a potential that is the difference between its row and column signals. When an "on" column signal and a row pulse simultaneously excite a pixel, the resulting potential difference is sufficient to turn it on [Fig. 3, left]. Unfortunately, for passive LCDs, the technique also produces intermediate voltages that engender crosstalk, as previously noted.

In STN displays, gray levels are implemented with two techniques. Frame modulation applies pixel select and nonselect voltages to a pixel in each frame over a cycle of, say, 16 frames. The response time of the LCD (about 150 ms) is usually much longer than the frame period (about 17 ms), so the rms average of the 16 different voltages produces a shade of gray—a gray level—that is between the pixel's fully on- and fully off-state.

Alternatively, simple pulse-width modulation can be used. Here, the column signal is held low for a portion of the select interval and then high for the remainder of the interval. The resulting rms voltage again produces a particular gray level, since the transmittance of each LCD pixel is proportional to the rms value of the voltage applied to it.

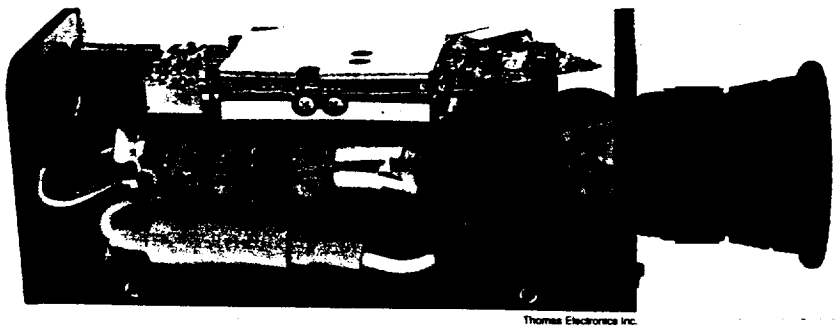
The contrast and viewing angles of STN displays are now quite good, but response times remain much too long for video. The problem is not that liquid-crystal materials are inherently slow. Higher-voltage and lower-viscosity liquid-crystal materials easily accommodate video rates in active-matrix displays.

Using a fast-responding, high-voltage liquid crystal in passive STN displays, however, results in the liquid crystal's state decaying markedly between select pulses. The display is no longer responding to the rms voltage averaged over a frame period, but is responding to voltage changes during the frame period. The result is reduced transmittance (brightness), poor contrast, and a narrower viewing angle.

The In Focus team realized (and have demonstrated) that it is possible to use a faster liquid-crystal material, have a bright flicker-free display, and minimize ghosting effects, all at the same time. They do it by employing a much more complicated set of row functions [Fig. 3, right] to distribute the selection intervals over the frame period, and by combining the row functions with more complex, calculated column functions.

The tradeoff is that the row functions are not only more complicated in themselves,

Return of the color wheel



Thomas Electronics Inc.

The original system proposed for color television in 1940 was an electromechanical color-wheel system. Frames for the red, green, and blue components of the color image followed each other sequentially on a black-and-white TV screen. A motor-driven wheel containing red, green, and blue gels rotated in synchronization with the frame presentation, and the viewer observed the screen through this rapidly rotating color wheel. A full-color image emerged as the viewer's visual system blended these sequential frames. The general term for such systems is frame-sequential color.

Two discouraging problems occurred with these early frame-sequential systems. First, they required a cabinet roughly twice as wide as an otherwise equivalent monochrome receiver. Second, and more seriously, they required three times the frame rate of an otherwise equivalent monochrome system. The electronics of the period could not produce a frame rate of 180 frames per second (60 frames per second times 3 color images per full-color frame), and using a reduced frame rate produced a flickering image.

With the success of RCA Corp.'s shadow-mask system, which distributed the red, green, and blue images on the tube face instead of presenting them sequentially, field-sequential color fell out of fashion. Tektronix Inc., Beaverton, OR, brought it back three years ago with its liquid-crystal color shutter. This system replaced the color wheel with a stationary, solid-state device no larger than the screen of the monochrome cathode-ray tube (CRT) it works with. The shutter is fast, but as its associated polarizers absorb a great deal of light, a fairly bright CRT is required.

What all this buys is a very-high-resolution color display. Stand-alone shutters and tubes with shutters bonded to their faceplates are currently available as off-the-shelf products under the NuColor trade name. A 9-inch NuColor monitor costs US $950.

This year at the Society for Information Display Show in Seattle, two new field-sequential color systems were exhibited—both based on electromechanical color wheels. The first was Dallas-based Texas Instruments Inc.'s projection display based on the company's digital micromirror device [see the following article, "Mirrors on a chip," by Jack M. Younse, p. 27]. The second was a miniature color-wheel CRT from Miyota, Nagano Prefecture, Japan, which is being distributed by Thomas Electronics Inc. of Wayne, NJ [see figure above]. The miniature 0.6-inch-diagonal monochrome CRT is derived from one Miyota makes for camcorder viewfinders and weighs only 5 grams without deflection coils. Complete with deflection coils, motor, and color wheel, the weight is less than 50 grams.

Because the monochrome has no shadow mask, resolution is limited only by the beam spot size and the deflection electronics. Unlike the situation in electronic color shutters, light absorption within each color band is not large, so images are bright. Initially, Miyota and Thomas are marketing the color-wheel tube as a relatively low-cost—less than $1200—alternative to Mil-Spec tubes for applications such as helmet-mounted displays. — *K.I.W.*

but also require a column voltage whose value is a function of every pixel in the column. These more complicated signals have to be calculated by more complex display electronics, but the electronics can be implemented in traditional ICs. This approach—dubbed active addressing by In Focus—allows the display manufacturer to do something very exciting: move the transistors required for active-matrix LCDs off the display glass and into plastic packages, where they can be implemented much less expensively.

What's left on the glass itself? Nothing more than is found in a conventional passive display. A more responsive liquid-crystal material is substituted for the conventional material and the cell thickness is reduced, but the manufacturing process is otherwise identical.

Can the degree of this excitement be quantified? Judging by Motorola Inc.'s August 1992 decision to invest $23 million in a joint venture with In Focus, the answer is yes. Called Motif, the venture is currently building a plant to manufacture the displays in Wilsonville, OR. Motorola, headquartered in Schaumburg, IL, will manufacture the active-addressing chips, which will be available to all display manufacturers—not just Motif—as soon as production levels permit.

Motif's manufacturing line was turned on in September, engineering evaluation units are to be shown later this month at Comdex in Las Vegas, and the company plans to ship production models early next year.

On the all-important matter of price, Scheffer, who is now chief scientist at Motif, said that the new displays, while more expensive than passive color LCDs, will be considerably less expensive than AMLCDs. The difference in price between his new display and a standard passive color display should be about one-quarter the price difference between a color AMLCD and a passive color display.

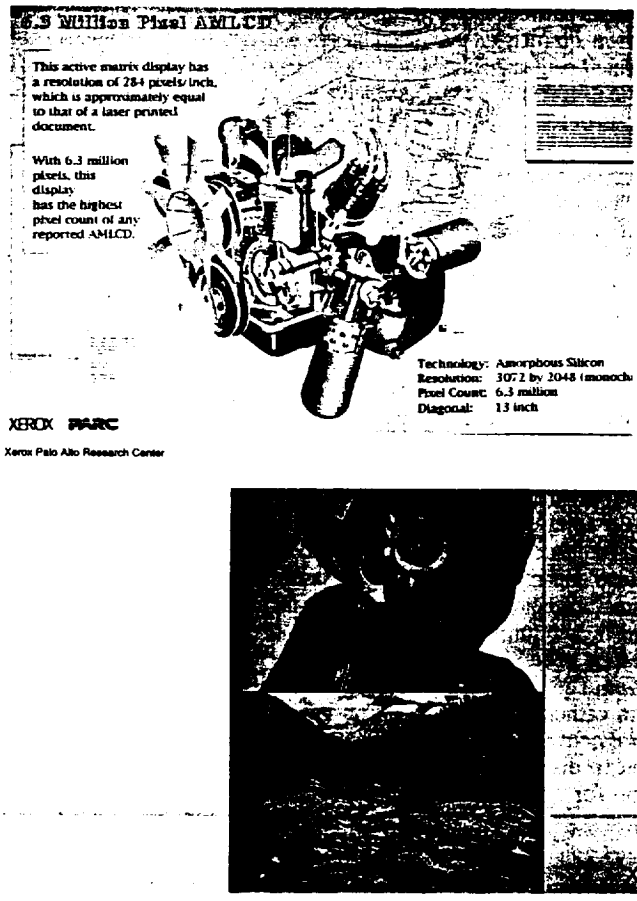
PASSIVE-MATRIX COLOR. The second alternative to color AMLCDs is the existing standard passive-matrix color LCD. Given its limitations, the fact that passive color is any kind of viable alternative to AMLCDs is something of a surprise. Three years ago, Tim Patton, marketing manager at Hitachi America Ltd.'s Electron Tube Division, Norcross, GA, predicted that, while the availability of AMLCDs increased and their prices dropped, there would be a temporary window of opportunity for passive color. Although he expected that window to last only a year or two, he proved more prescient than many of his colleagues, who did not see much of a future for passive-matrix color.

Three factors have broadened the window of opportunity spotted by Patton. Getting AMLCDs into production took longer than anticipated. Then, once display manufacturing began, delays occurred in bringing yields up to the point where original-equipment manufacturers (OEMs) could commit to using the displays in products. And, initially because of low yields, and later because of high plant investment, prices stayed—and continue to stay—high.

Over the last two years Patton's window has also been widened considerably by a surprising improvement in the image quality of passive color displays. Remarkable improvements in color saturation, crosstalk, and viewing angle were seen in displays from such companies as Sharp, Hitachi, and Kyocera at this year's SID. Sharp Microelectronics Corp. and Kyocera Corp. showed displays with a pixel turn-on time of roughly 125 ms, and virtually everyone else is following suit. These faster displays are eminently usable for the vast majority of common computer applications, although they do not have the optical response for animation or video.

Price and availability are the final two variables in the passive-color-display equation. Passive color displays are more expensive than monochrome because, like AMLCDs, every color pixel must contain three subpixels, each of which requires a red, green, or blue filter. The advantage of passive color displays is that they do away with all those thin-film-transistor switches at every subpixel. The result is a display that is much easier to make, so manufacturing plants require one-seventh the in-

Xerox's 6.3-million-pixel LCD



A 10-inch, VGA, liquid-crystal display packs 640 by 480 pixels into an active area of approximately 20 by 15 cm, giving a linear pixel density of 80 pixels per inch (or a pixel pitch of roughly 0.32 mm). Notebook PC users have become accustomed to such a pixel density—and its limitations. They do not, for instance, even try to read the equivalent of 6-point type on such screens. But print that 6-point type on a 300 dot-per-inch (dpi) laser printer, and it is eminently readable.

Without a 300-dpi display, WYSINWYG (what you see is not what you get). There are a few, very expensive, 200- and 300-dpi monochrome cathode-ray tube (CRT) monitors around, but liquid-crystal displays (LCDs) have not come close. For this reason, Xerox Palo Alto Research Center's 13-inch-diagonal active-matrix LCD, with its 6.3 million pixels, is unique [see figure, above left].

Not only does the display have the largest number of pixels ever to appear on a single LCD, but there are 284 of them to the linear inch. The effect is startling: laser-printer quality on an LCD.

A color version has the same number of dots, with quartets of those dots in red-green-blue-green quad patterns serving as the subpixels in each full-color pixel. The result is a 1536-by-1024 full-color display [see figure, above right]. The U.S. Advanced Research Projects Agency, Arlington, VA, helped with the funding.

—*K.I.W.*

vestment of a color AMLCD plant, according to Hitachi's Patton.

Consequently, major display manufacturers are now quoting prices between $550 and $850 for production quantities of passive color displays, which compare with prices in the vicinity of $1400 for color AMLCDs. Furthermore, as of late summer, demand for color AMLCDs has been handily outstripping supply, so manufacturers are trying hard to convert OEM customers to passive color displays, which have been available in quantity.

Because the plant investment required for passive color displays is relatively modest, more players—including Kyocera and Optrex/Satori, Torrance, CA—can afford the ante. That bodes well for price competition and continued availability in the near term.

There is at least a chance that other existing technologies might find ingenious application to color laptop computers and other portable systems, too. For example, Miyota, Nagano Prefecture, Japan, has suggested that its new miniature color-wheel cathode-ray tube could be mounted in a laptop case and used in a projection or virtual-image configuration. The well-known custom and semicustom cathode-ray tube manufacturer, Thomas Electronics Inc. of Wayne, NJ, has agreed to distribute the small, lightweight tube for Miyota [see "Return of the color wheel," p. 20].

The development of color LCDs is a glamorous activity at the moment, but monochrome STN LCDs are the industry's bread and butter. VGA panels of excellent quality are readily available from many sources for around $200.

IN BLACK AND WHITE. Film compensation, which has replaced heavier and more complicated dual-cell compensation techniques, produces true black-and-white displays and all but eliminates color distortion. In the best displays, contrast ratio, viewing angle, and crosstalk are at very acceptable levels, while white backgrounds are admirably free of blotchiness and backlights produce acceptably bright images with reasonably even illumination. Displays routinely offer 16 levels of gray, and 64 levels are no longer unusual. In some, response time is approaching 125 ms.

However, all of these characteristics can vary widely among the displays in current laptop computers and, to a somewhat lesser extent, among those that OEMs may now be purchasing in quantity. Units with similar specifications may engender very different subjective impressions, and thereby give the products that contain them a substantial competitive advantage—or disadvantage.

For battery-powered applications, a display's power consumption (largely a function of the backlight) is a big issue. For monochrome VGA laptop displays, typical luminance-power values are 65 cd/m^2 at 2W.

Recently, some manufacturers of subnotebook computers—such as Hewlett-Packard Co.'s OmniBook 300—have decided to run their LCDs in reflective mode, doing away with the backlight entirely. This design yields a very lightweight computer that operates for hours on a few standard penlight batteries, but it unfortunately compromises image quality in all but bright ambients.

Such problems will not last. All LCD technologies are advancing quickly, with more pixels, finer pixel pitches, more colors or gray levels, and larger screens [see "Xerox's 6.3-million-pixel LCD," p. 21]. The larger screens have diagonals of about 14 inches for commercial "conventional" LCDs and up to 24 inches for Canon's as yet unproved implementation of ferroelectric LCD technology (which has suffered from mechanical instability in previous incarnations).

LARGE-SCREEN LCDs? But they are not considered "really large," and "really large" is an issue. If the high-information-content flat-panel display market is defined at one end by the reality of laptop computers, it is defined at the other by the dream of 60-inch-diagonal, high-definition television (HDTV) screens hanging on the wall.

Currently, only one full-color, video-rate flat-panel technology can be purchased in the worldwide marketplace: color AMLCDs. But, given the problems LCD manufacturers are having with the current 10-inch glass, it is no wonder that they have no immediate plans to process 60-inch glass.

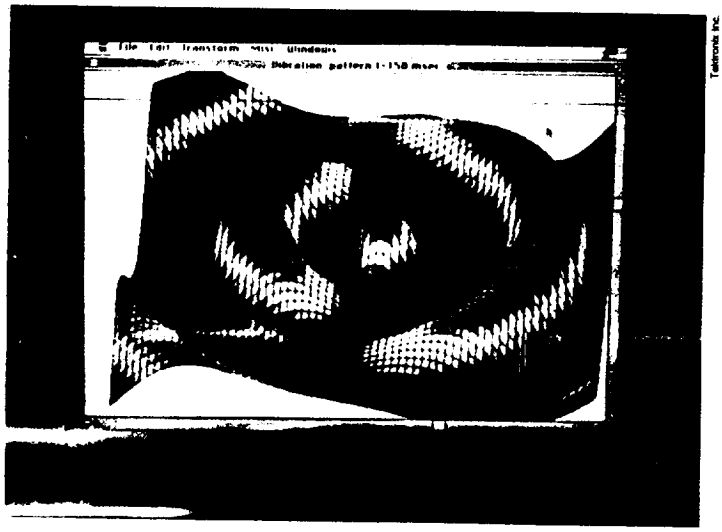
Can LCD technology be a contender in the rich HDTV market that should start developing in 1995? Perhaps eventually. One approach is to assemble small displays into a larger one. The concept is implemented today—crudely—with cathode-ray tubes in "videowalls," but small flat panels would have to be put together seamlessly in a process called tiling. With exquisitely precise control of tile-to-tile alignment, spacing, luminance, and color, researchers think they can make the seams invisible. But making large displays with small-display technology is neither easy nor cheap.

Making a single large LCD could possibly be done with a technology called plasma-addressed liquid crystal, which was first announced three years ago by Tektronix Inc. and shown in a much more refined form at the SID symposium in Seattle [see "Replacing transistors with gas," left].

THE GREAT FLAT HOPE. The most likely candidate for HDTV on a wall in this century is not a variation of LCD technology at all, but a color plasma display panel (PDP). Monochrome (red-orange) PDPs have been built in sizes up to 60 inches diagonal for some time, a size that no other flat-panel technology has ever approached.

Such sizes are possible because PDPs have a fairly simple glass-sandwich structure that scales readily. Monochrome plasma displays use a matrix addressing

Replacing transistors with gas



Three years ago Tom Buzak and his colleagues at Tektronix Inc., Beaverton, OR, raised eyebrows in their suite at the Society for Information Display (SID) in Las Vegas. What Buzak showed was a rough demonstration unit of an active-matrix liquid-crystal display in which the pixels were switched not by thin-film transistors but by a gas plasma contained in channels in the display's glass backplate.

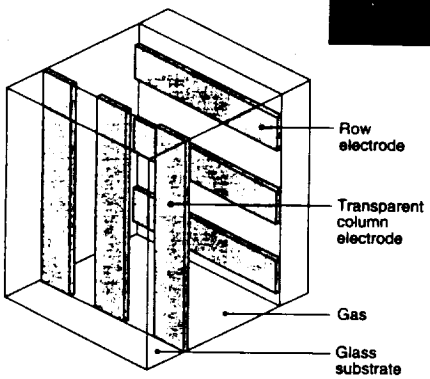
At this year's SID show, Buzak, now director of Tektronix' Display Research Laboratory, was back with a much more polished plasma-addressed liquid-crystal display (PALCD), one having a 16-inch diagonal and 640 by 480 pixels.

The required size and spacing of the plasma channels do not lend themselves to displays with very fine pixel pitches, but the technology is relatively simple, readily scalable, and capable of video speeds. In short, it is a candidate for large-screen, direct-view HDTV.

Tektronix is looking for partners to help convert this well-developed technology into products. Contact Thomas S. Buzak, Display Research Laboratory, Tektronix Inc., Box 500, M/S 46-944, Beaverton, OR 97077.

—*K.I.W.*

[4] Color plasma display technology, which is based on using color phosphors for gas-discharge pixels such as those shown below, is the leading contender for high-definition-television-on-a-wall in this century. Photonics Imaging Inc.'s color panel has a 30-inch diagonal and 1024 by 768 pixels. The photo [right] was taken during the panel's design, and only half of the pixels are lit.



scheme to ionize a gas mixture containing neon, and the neon glows with its characteristic red-orange color. In color PDPs, the gas mixture is changed to one containing xenon, which emits in the ultraviolet (UV) rather than the visible portion of the electromagnetic spectrum. The inner walls of the pixels are coated with red, green, and blue phosphors that are UV-sensitive. This is a well-known and highly efficient mechanism for generating light: it is used in millions of fluorescent lamps. (Fluorescent lamps use ionized mercury to generate UV radiation.)

Japan's NHK Corp. in Tokyo has been developing color PDPs for nearly two decades. Most of this time has been spent on a PDP variant called dc plasma, which is now producing images of high quality but not yet bright enough for commercial products. Recently, the company added a program to develop a variant known as ac plasma.

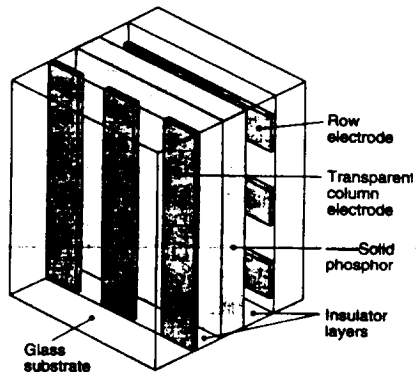
But at the 1992 SID show in Boston, NHK, Oki, and Texas Instruments (Japan) showed a very impressive dc-plasma HDTV set with a 32-inch-diagonal screen. The image quality and color rendition were excellent and, with a luminance estimated at 75 cd/m^2, the image was almost bright enough for a consumer product. This year at SID, NHK described its work on an improved 40-inch-diagonal dc plasma display.

An early exponent of color ac plasma, Peter Friedman is president of Photonics Imaging Inc., Northwood, OH, a long-time maker of military monochrome PDPs. He has been steadily developing color ac plasma for nearly 10 years, most recently with support from the U.S. Advanced Research Projects Agency (ARPA). At SID '93, Photonics displayed a good-looking 19-inch 640-by-480 color display with a luminance of 85 cd/m^2. A brighter, 30-inch display with higher pixel count was completed in August [Fig. 4].

The remaining classical flat-panel technology, electroluminescence [Fig. 5], seems to have peaked. The merger three years ago of Finlux, Espoo, Finland, into Planar Systems Inc., Beaverton, OR, left the world with only two major electroluminescent display suppliers. In addition to Planar, there is Sharp Corp., Osaka, which continues to develop and introduce new products of this type—but in a remarkably understated way.

Planar did create a stir in Seattle by showing the first electroluminescent display that could reasonably be called full-color.

Planar's substantial achievement, accomplished with ARPA support, was the development of the most efficient blue phosphor yet. This phosphor is an impressive R&D development, but it allows a white area luminance of only 15 cd/m^2—too dim for a commercial product by at least a factor of four. The consensus in the display community is that unless Planar makes much progress than most believe possible, its work is fated to be a niche technology.



[5] Electroluminescent technology, once a popular display contender, seems to have been relegated to the niche for bright, red-yellow or monochromatic displays, although full-color work is being done with support from the U.S. Advanced Research Projects Agency.

[6] The direct-view high-definition television sets to be introduced in 1995 will not use flat-panel displays at all, but cathode-ray tubes having a 16:9 aspect ratio and over 1000 horizontal raster lines.

WHAT ABOUT HDTV? Large economical flat-panel displays will not be available for the direct-view HDTV sets to be introduced in 1995. These sets will use conventional cathode-ray tubes having a 16:9 aspect ratio and approximately 1000 raster lines [Fig. 6]. The view of several potential suppliers is that the most common size, at least initially, will have a 32-inch diagonal.

For larger images, consumers will have a choice of projection sets using either projection cathode-ray tubes or an AMLCD of

The best of both worlds?

Conventional color cathode-ray tubes are bright and offer high resolution, fast response, a wide viewing angle, and a broad spectrum of colors—at costs that are modest with respect to display performance.

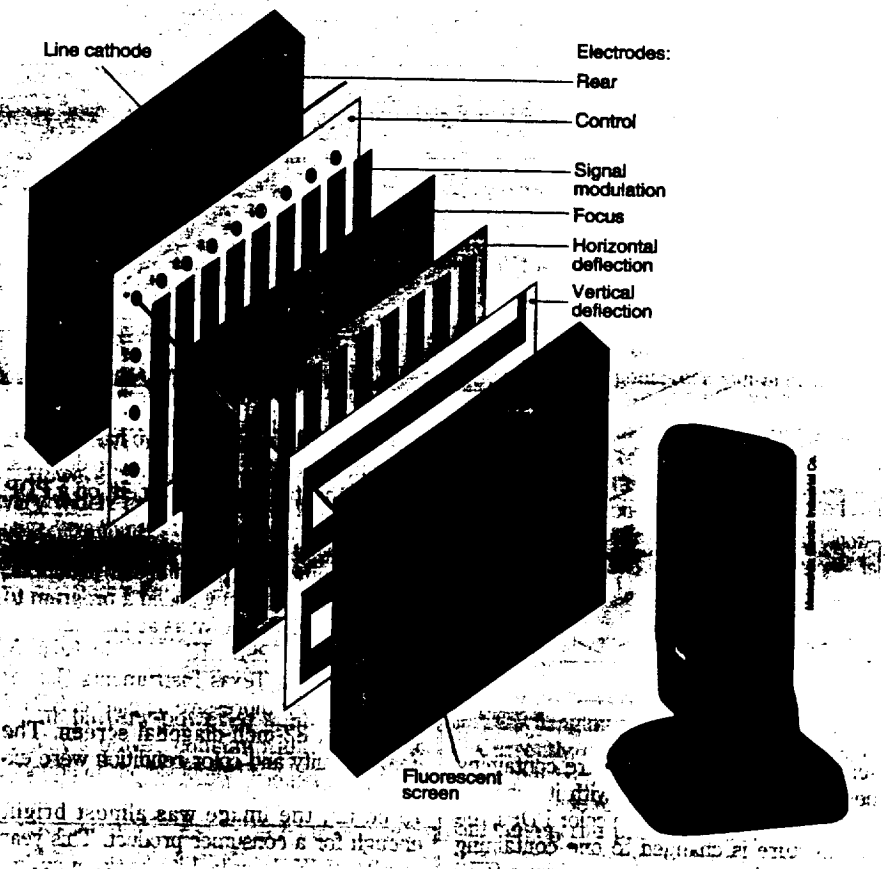
On the other hand, flat panels are, well, flat. It is their flatness, accompanied generally by light weight and sometimes by low power consumption, that is their *raison d'être.*

The designers of most flat panels would be happy to come close to the image quality offered by run-of-the-mill cathode-ray tubes (CRTs). But image quality is not everything. In laptop computers, for instance, users are willing to sacrifice image quality for light weight and long battery life. Starting with W. Ross Alken at the University of California Berkeley, in 1951, periodically designers have tried to come up with flat CRTs that would combine the advantages of both display technologies.

Now, Matsushita Electric Industrial Co., Osaka, has announced the commercial production of a 14-inch-diagonal television receiver based on a cross between CRT and matrix-addressing technologies, which the company calls Flat Vision. Like a conventional CRT, Flat Vision uses a cathode to produce electrons, a deflection system (in this case, electrostatic deflection) to direct the electron beam, and a phosphor screen with red, green, and blue (RGB) stripes, all of which are maintained in a vacuum.

But this is not a single CRT. Contained within one flat, evacuated bulb is an array of many CRTs, built with laminar structures for the sake of relatively economical fabrication. If the system's basic structure were used to make a single, conventional CRT of moderate size, it could not maintain focus and color convergence across the screen. But all of these CRTs are tiny in terms of their pixel dimensions.

The TV set that Matsushita began selling in Japan last month—with 442 pixels horizontally and 440 pixels vertically—has nearly 10 000 CRTs in the array. That comes to 20 pixels per mini-CRT, each of which is turned on at the appropriate time by means of the control electrode [see figure]. Electronically, such a system is very complex, even though switching its matrix of 10 000 elements is much less demanding than switching the nearly one million elements in a full-color LCD.



Matsushita's 14-inch display is 98 mm (3.9 inches) thick. The entire TV set weighs 16.2 kg and consumes 85 W of power. Clearly, substantial weight and power savings are not part of the Flat Vision package. But flatness—in comparison to a conventional CRT—is.

As intriguing as the new technology is, it poses several questions. Is 98 mm thin enough? Can resolution be brought up to the demands of high-definition television and computer monitors? As sizes grow, will the design be susceptible to matrix crosstalk problems? Can the cost be brought down? (The TV's introductory price is ¥288 000, or about US $2700 at the current ¥105 to the dollar.)

Matsushita has clearly answered these questions to its own satisfaction. Sources within the company say that, despite the modest initial production of 1000 units a month, the company's goal is nothing less than head-to-head competition with the world's color LCD manufacturers. It is projecting that Flat Vision will capture 10 percent of the worldwide display market—currently 140 million units annually spread over all technologies—by the year 2000.

Until Flat Vision displays are in wider distribution and subject to independent analysis, it is hard to say whether Matsushita's optimism is justified. But, as the Japanese industrial giant's sole entry in the flat-panel sweepstakes, it certainly gives equipment designers and end users a novel display technology worth considering for future products.

—*K.I.W.*

moderate size employed as a light valve. The only other projection technology that could appear in a consumer product within the next three or four years is Texas Instruments' innovative array of deflectable micro-mirrors [see the article, "Mirrors on a chip," by Jack M. Younse, opposite.]

Color plasma is the most likely candidate for a large direct-view flat-panel display in this century, but Tektronix' plasma-addressed LCD is an interesting possibility. And Matsushita entered a dark horse called Flat Vision in the race this summer [see "The best of both worlds?," above].

TO PROBE FURTHER. While there has been a plethora of papers on LCDs, one tutorial that does justice to the electro-optic effects through which LCDs operate (a topic intentionally avoided in the current article) is Terry Scheffer and Jürgen Nehring's surprisingly readable "Supertwisted Nematic (STN) LCDs." It appears in Volume 1 of the Society for Information Display (SID) '93 Seminar Lecture Notes.

The current article's discussion of display addressing borrows from Sheffer and Nehring, but leaves most of their 60 pages untapped. Contact the Society for Information Display, 8055 W. Manchester Ave., Playa del Rey, CA 90293; 310-305-1502.

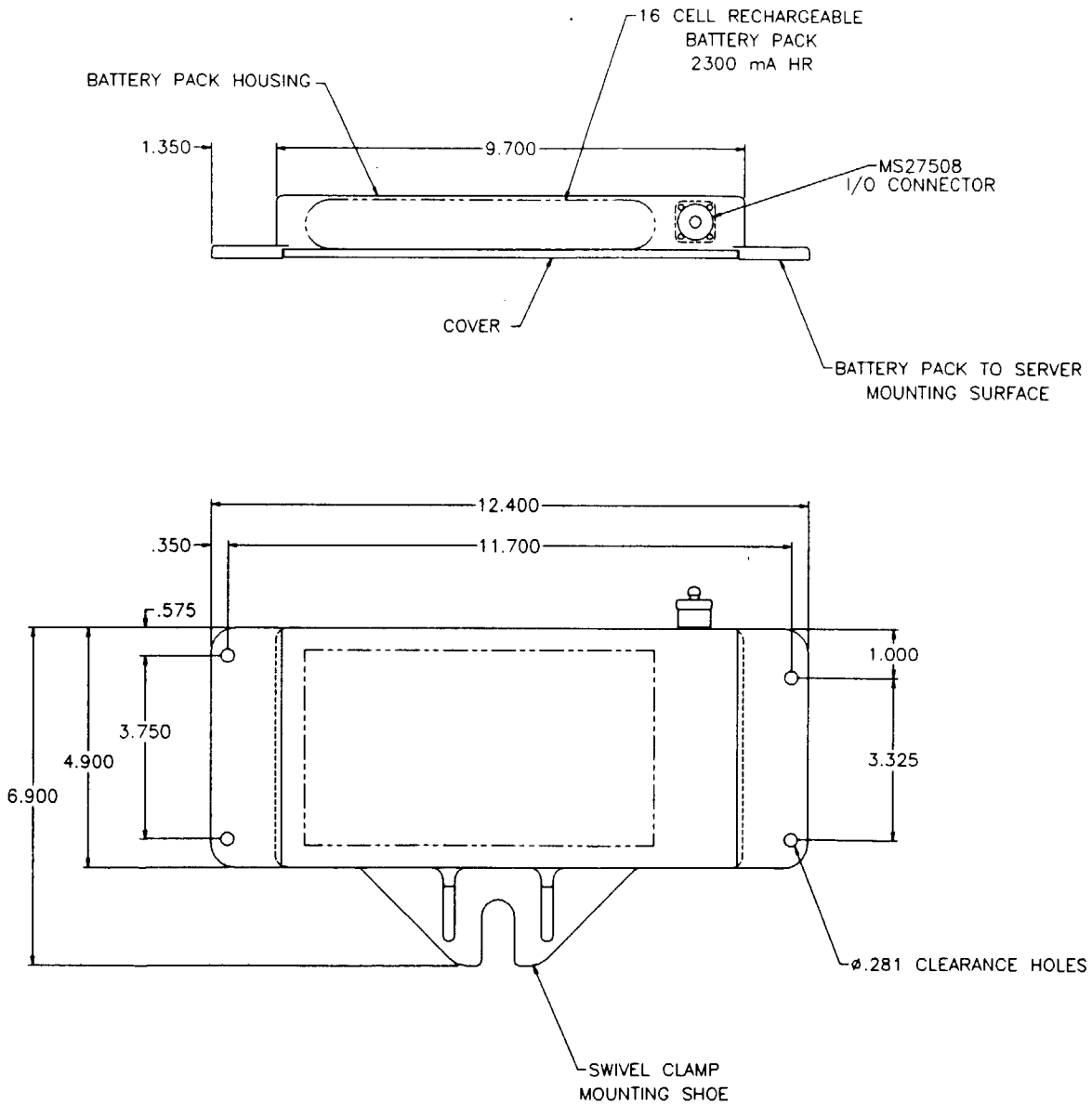
Two books that survey display technologies in general are *Flat-panel Displays and CRTs*, edited and partially written by Larry E. Tannas Jr. (Van Nostrand Reinhold, New York, 1985), and *Handbook of Display Technology* by Joseph A. Castellano (Academic Press, San Diego, CA, 1992.)

The monthly *Information Display Magazine* contains readable articles and columns on display technology, products, applications, and marketing. It is available with membership in SID or on a controlled-circulation basis. (The society's address is listed above.)

A remarkably rich exposure to display issues, R&D, products, and applications is available at SID's annual symposium and show. The 1994 edition will be held in San Jose, CA, during the week of June 13. Call the society for information. ◆

APPENDIX 3

BATTERY MODULE DATA SHEETS



BATTERY PACK ASSEMBLY

REVISED : 950424

SAIC An Employee-Owned Company

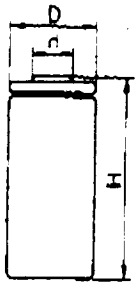
SAI® Technology
A Division of Science Applications
International Corporation

Sanyo NiCad Battery Cell Data Sheet

SANYO

CADNICA

Cell Type KR-2300SCE
Specifications

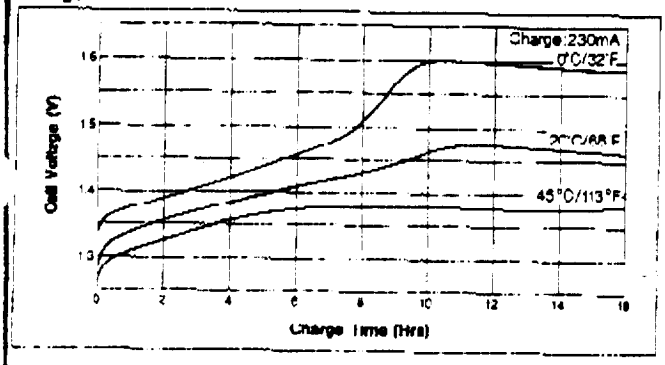


Dimensions of Bare Cell	H	49.0 +0.3	mm
		1.929 ±0.012	inch
	b	22.0 ±0.3	mm
		0.866 ±0.012	inch
	d	10.0	mm
		0.394	inch

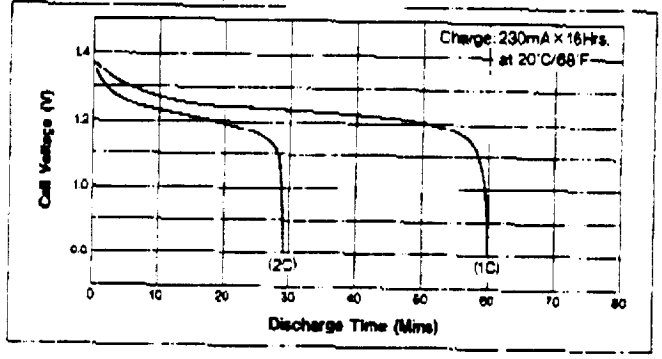
Nominal Capacity			2300mAh
Nominal Voltage			1.2V
Charging Current		Standard	230mA
		Fast	3500mA
Charging Time		Standard	14~16Hrs.
		Fast	about 1Hr.
Ambient Temperature	Charge	Standard	0°C~+45°C (+32°F~113°F)
		Fast	0°C~+45°C (+32°F~113°F)
	Discharge		−20°C~+60°C (−4°F~140°F)
	Storage		−30°C~+60°C (−22°F~122°F)
Internal Impedance (Av.) (at 50% discharge)			5.5mΩ (at 1000Hz)
Weight			58g/2.04oz
Dimensions (D) × (H) (with tube)		23.0 $^{0}_{-1}$	× 50.0 $^{0}_{-2}$ mm
		0.91 $^{0}_{-0.04}$	× 1.97 $^{0}_{-0.08}$ inch

Typical Characteristics

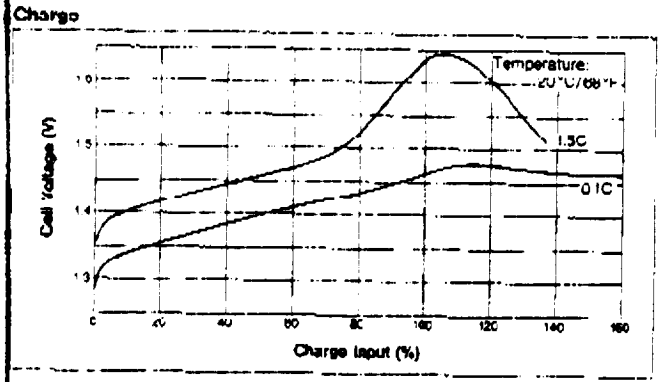
Charge



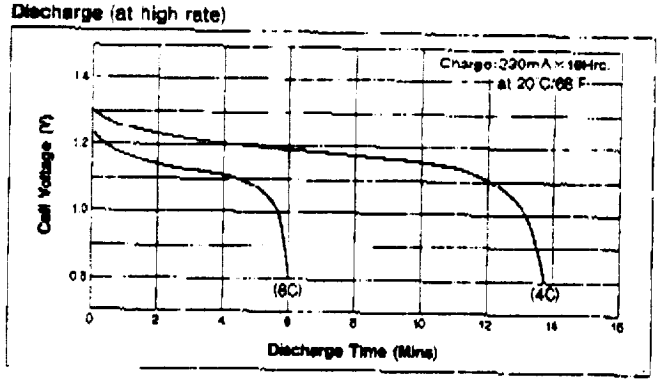
Discharge (at high rate)



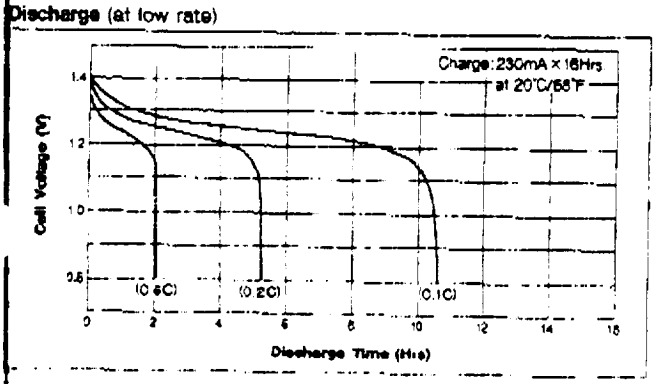
Charge



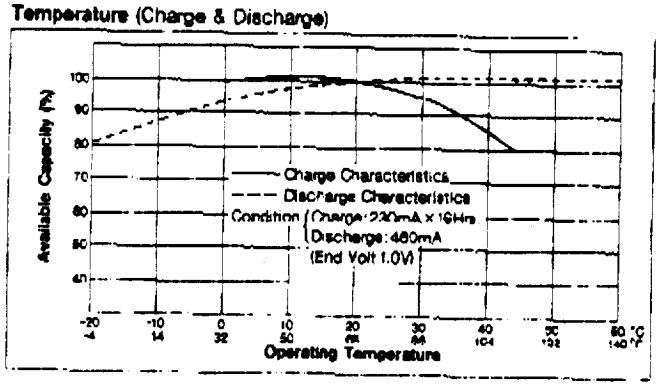
Discharge (at high rate)



Discharge (at low rate)



Temperature (Charge & Discharge)



PIG Mat Material Data Sheet

How to use the

& PIG® Mat with Perforations!

PIG® Mat absorbs petroleums, aqueous solutions, solvents, and most acids and chemicals.

U.S. Gov't

Follow these easy steps to assure maximum effectiveness:

1 Clean up loose absorbents.

No clay on the floor! PIG® Mat works alone! Put PIG® Mat on a clean floor to catch drips or overspray. Cuts easily to any shape with scissors or a knife. With Perforated PIG® Mat just tear off as much as you need without having to use a utility knife!

2 Let it work.

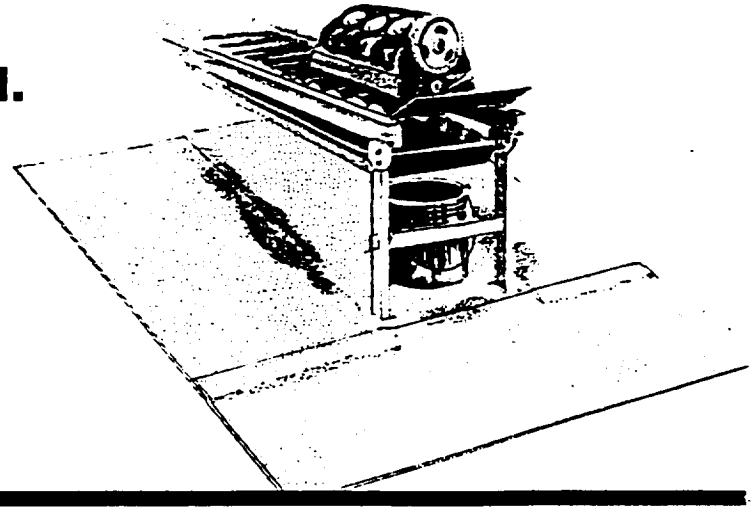
PIG® Mat's dimpled design pulls in liquids fast. The wicking power does the work – not you!

3 Replace when fully saturated.

It's time to replace PIG® Mat when liquid has fully darkened it.

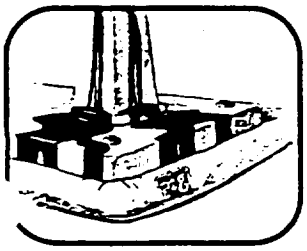
WHERE TO USE:

- Around screw machines
- Under conveyors
- Loading docks
- On tool benches
- Under presses
- On machine beds



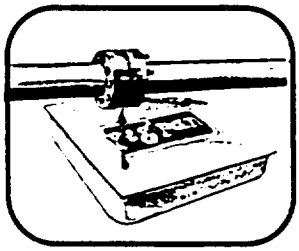
Other PIG® products for you

For Leaks:



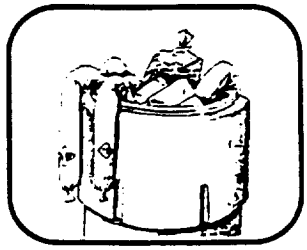
PIG® Absorbent Socks

For Drips:



PIG® Pan

For Contingency Planning:



Spill Response Kit for accidental spills

You want to know more abou these products? GREAT! Jus call our toll-free number and we' send you a FREE Pigalog®, a catalog filled with information on all PIG® products.

***Call* 1-800-HOT-HOGS**(468-46- ***Fax 24 hrs.* 1-800-621-PIGS**(7447)

NEW PIG CORPORATIO
One Pork Avenue
Tipton, PA 16684-0304

Material Safety Data Sheet

U.S. Gov't

Product Identification: *PIG® mats*, Item #MAT201, #MAT202, #MAT203, #MAT204, #MAT208, #MAT216, #MAT217, #MAT220, #MAT221, #MAT225, #MAT226, #MAT229, #MAT230, #MAT231, #MAT237 & #MAT238

Please Note: PIG® absorbent products must be disposed of in compliance with local, state and federal regulations. This product is considered non-hazardous in its purchased or unused state and requires no special disposal procedures.

I. Manufacturer Identification

Manufacturer's Name: New Pig Corporation
Address: One Pork Avenue
Tipton, PA 16684-0304
Emergency Telephone Number: (800) 468-4647
Telephone Number for Information: (800) 468-4647
(Above numbers during hours of 8 a.m. - 5 p.m. ET)
Date Prepared: 12-08-93 (5)

II. Ingredients/Identity Information

Chemical Identity: Polypropylene: 99.7%
(CAS#: 9003-07-0)
Grey Pigment: 0.3%

(Both components considered non-hazardous)

III. Physical/Chemical Characteristics

Boiling Point: N/A
Vapor Pressure: N/A
Vapor Density: N/A
Solubility in Water: Insoluble
Specific Gravity (H_2O = 1): 0.9
Melting Point: 320° F
Evaporation Rate: N/A
Appearance and Odor: Grey sheets or rolls. No odor.

IV. Fire and Explosion Hazard Data

Flash Point: 825° F (Autoignition)
Flammable Limits: N/A LEL: N/A UEL: N/A
Extinguishing Media: In its purchased or unused form; water, chemical foam, dry chemical or CO_2. In its used form; that which is compatible to liquid absorbed.
Special Fire Fighting Procedures: Wear a self-contained breathing apparatus and refer to absorbed liquid(s) MSDS(s), for the *PIG® mats* do not render liquid nonflammable, neutral or less hazardous.
Unusual Fire and Explosion Hazards: Refer to absorbed liquid(s) MSDS(s), for the *PIG® mats* do not render liquids nonflammable, neutral or less hazardous.

V. Reactivity Data

Stability: Unstable _____ Stable X
Conditions to Avoid: N/A
Incompatibility (Materials to avoid): Strong oxidizing agents may degrade product.
Hazardous Decomposition or By products: N/A
Hazardous Polymerization: Will not occur.

VI. Health Hazard Data

Route(s) of Entry: Inhalation: N/A Skin: N/A
Ingestion: Possible
Health Hazards (Acute and Chronic): N/A
Carcinogenicity: NTP: N/A IARC: N/A
OSHA Regulated: N/A
Signs/Symptoms of Exposure: N/A
Medical Conditions Generally Aggravated by Exposure: N/A
Emergency and First Aid Procedures: N/A

VII. Precautions for Safe Handling and Use

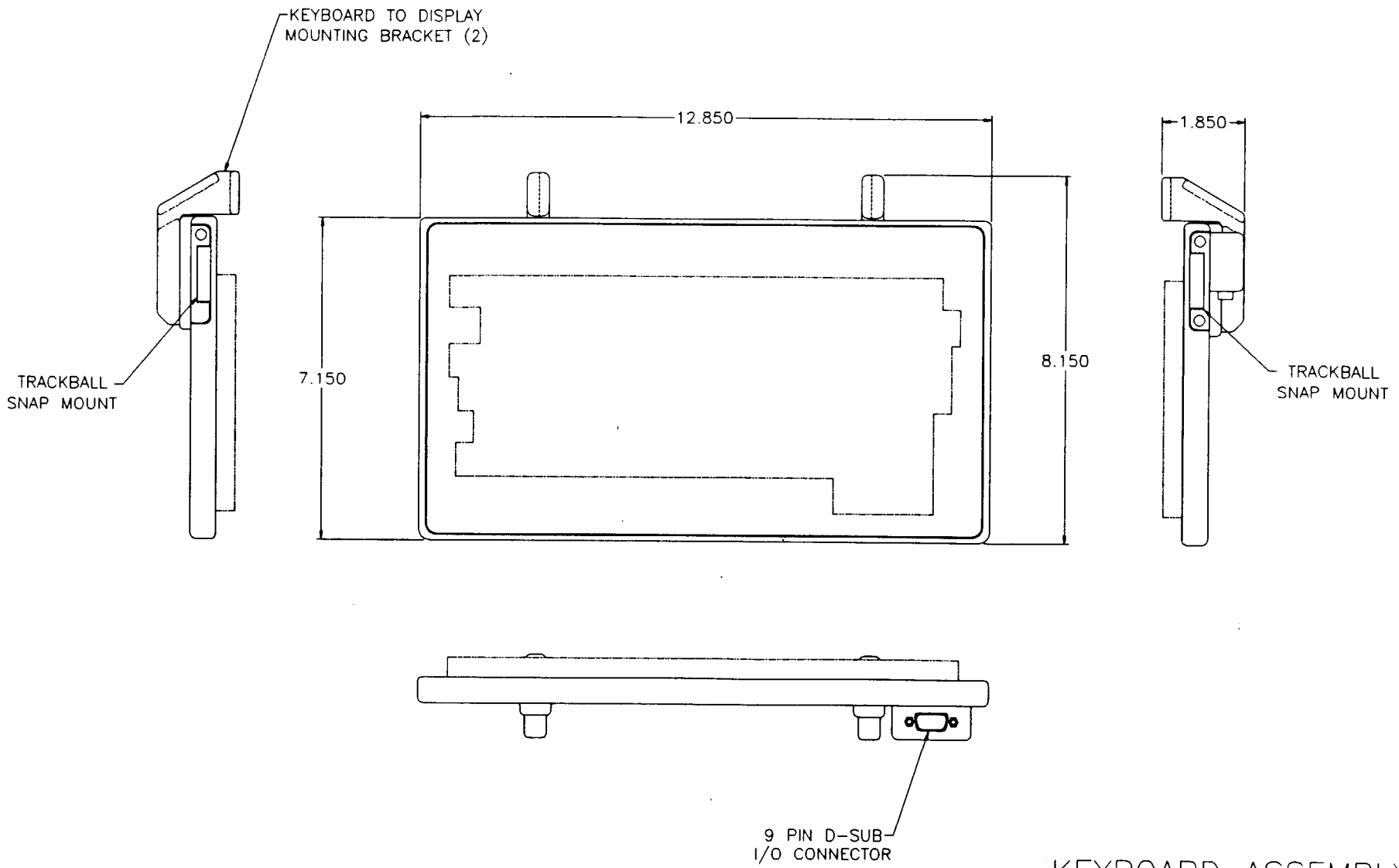
Steps to Be Taken in Case Material is Released or Spilled: In its purchased or unused form: Sweep or vacuum product and dispose of as a non-hazardous material.
Waste Disposal Method: In its purchased or unused form: No special precautions necessary. (Not classified as a hazard). In its used form: Dispose of all waste (based on the components of the liquid absorbed) according to federal, state, and local laws.
Precautions to Be Taken in Handling and Storing: N/A
Other Precautions: N/A (Refer to absorbed liquid(s) MSDS(s), for the *PIG® mats* do not render liquids nonflammable, neutral, or less hazardous.)

VIII. Control Measures

Respiratory Protection: N/A
Ventilation: Local Exhaust: N/A Mechanical: N/A
Special: N/A Other: N/A
Protective Gloves: N/A
Eye Protection: N/A
Other Protective Clothing or Equipment: N/A
Work/Hygienic Practices: N/A

APPENDIX 4

KEYBOARD MODULE DATA SHEETS



KEYBOARD ASSEMBLY

REVISED : 950425

SAIC
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SAI® Technology
A Division of Science Applications
International Corporation

Part No.	APPLICATION		REVISIONS			
	NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
-1	65440	APW II	1	Engineering Release	94/07/15	

SOURCE CONTROL DRAWING

ADVANCED PORTABLE WORKSTATION (APW II) PROGRAM

REV	-	-	-	-	-	-	-	-	-	-	-	-															
SHEET	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
REV STATUS	REV				-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
OF SHEETS	SHEET				1	2	3	4	5	6	7	8	9	10	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCES ARE:

DECIMALS: ANGLES:
X ± ±
XX ± 03°
XXX ± 010°

MATERIAL

FINISH

CONTRACT NUMBER

NAS 213902

		DATE
PREPARED	M Castillo	94/07/15
CHECKED		94/07/18
APPROVED	M A Dawson	7/18/94
APPROVED		
QA		7/18/94
RELEASED		

SAIC An Employee-Owned Company — SAI Technology, A Division of Science Applications International Corporation

TITLE

APW II Keyboard Assembly

SIZE	CODE IDENT NO.	DWG. NO.	REV.
A	54779	65442	1

SCALE: NONE

SHEET 1 OF 36

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1. SCOPE

This source control document establishes the performance, design, manufacture and acceptance requirements for the APW II Keyboard Assembly critical item hardware component, intended for use in the Advanced Portable Workstation (APW II) for the NASA Ames Portable Computer Technology Program. The configuration of the APW II Keyboard Assembly shall be SAI Technology Part Number 65442–1.

2. APPLICABLE DOCUMENTS

The following documents of the exact issue shown form a part of this source control document to the extent specified herein.

2.1. Precedence of Specifications

If any conflict exists between the technical requirements of this source control document and that of any specification, standard, drawing or publication forming a part of this source control document, the requirements of this source control document shall take precedence.

2.2. Government Documents

The following documents are referenced to provide clarification and guidelines in support of meeting the requirements of this document.

2.2.1. Specifications

MIL-C-5541	Military Specification – Chemical Conversion Coatings on Aluminum and Aluminum Alloys
MIL-A-8625	Military Specification – Anodic Coatings, for Aluminum and Aluminum Alloys
MIL-W-16878/4	Military Specification Sheet – Wire, Electrical, Polytetrafluoroethylene (PTFE) Insulated, 200°C, 600 volts, Extruded Insulation
MIL-A-46146	Military Specification – Adhesives-Sealants, Silicone, RTV, Noncorrosive (For Use with Sensitive Metals and Equipment)

2.2.2. Standards

MIL-STD-130G	Identification of U.S. Military Property
MIL-STD-454K	Standard General Requirements for Electronic Equipment, Requirement 4 - Fungus Inert Materials – 14 Feb. 1985.
MIL-STD-810E	Environmental Test Methods and Engineering Guidelines – 14 July 1989

2.2.3. Other Publications

FCC Part 15 Subpart J	FCC Commercial Class A/B Title 47 Code of Federal Regulation (CFR) 1 Oct. 1989 – Radio Frequency Devices.
MIL-HDBK-217E Notice 1	Reliability Prediction of Electronic Equipment

2.3. Non-Government Documents

Not applicable

3. REQUIREMENTS

The APW II Keyboard Assembly shall be a commercially available keyboard assembly. The specific detailed requirements of the APW II Keyboard Assembly are described in Section 3.

3.1. Critical Item Definition

This source control document shall define the APW II Keyboard Assembly's overall requirements and performance including size, weight, operating modes, key groupings, test conditions, and interface.

3.1.1. Item Configuration

3.1.1.1. Part Number 65442-1

The APW II Keyboard Assembly Part Number 65442-1, as shown in Figure 3.1.1.1–1, shall consist of a single assembly which includes the keyboard assembly (printed circuit cards and components) and status indicators.

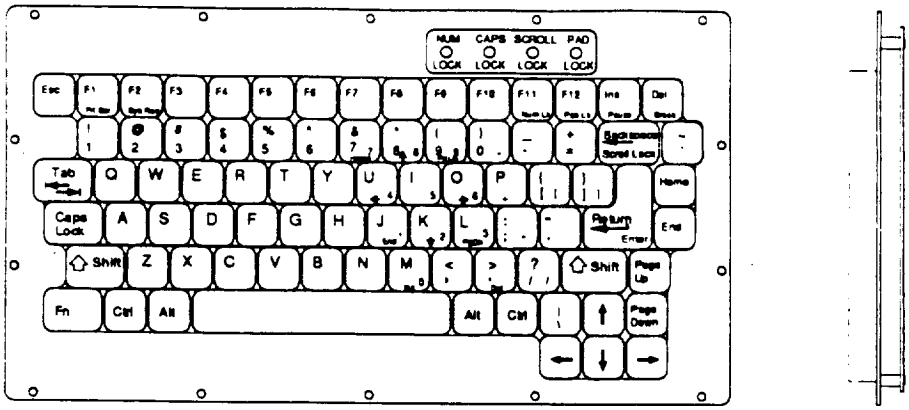


Figure 3.1.1.1–1 APW II Keyboard Assembly (65442-1)

3.1.2. Electrical Interface

3.1.2.1. Power Interface

3.1.2.1.1. Part Number 65442-1

The APW II Keyboard Assembly shall draw DC power from the computer power supply via a header connector mounted on the keyboard assembly printed circuit board.

3.1.2.2. Data Interface

3.1.2.2.1. Part Number 65442-1

The APW II Keyboard Assembly Part Number 65442-1 shall transmit clock pulses and exchange serial data via a header connector mounted on the keyboard assembly printed circuit board.

3.1.3. Mechanical Interface

The APW II Keyboard Assembly shall be designed with the physical dimensions as shown in Figure 3.2.4.1–1.

3.1.4. Operator Interface

3.1.4.1. Part Number 65442-1

The APW II Keyboard Assembly Part Number 65442-1 shall have (1) operator interface: an 82 key keyboard.

3.1.5. Appearance

The APW II Keyboard Assembly shall have no defects that affect the serviceability of the product.

3.1.6. Style and Dimensions

The APW II Keyboard Assembly Part Number 65442-1 shall conform to the style and dimensions shown on Figure 3.2.4.1–1. Variations in key shape, color, size or location are subject to review and approval by SAI Technology.

3.1.7. Documentation

The APW II Keyboard Assembly shall be supplied with existing standard commercial documentation.

3.2. Characteristics

The APW II Keyboard Assembly shall meet the design requirements in this section.

3.2.1. Functional Characteristics

3.2.1.1.4. Keyboard Scan Codes

Each key action, for the keys listed, shall generate a unique scan code from the keyboard. The scan codes shall be sent by the keyboard to the keyboard controller. A break code shall be sent on release of the key. Except as noted in the scan code tables, the break code shall consist of code F0 followed by the key scan code. The keyboard mode, described in Table 3.2.1.1.2, shall determine which scan code is generated and sent to the controller. The scan codes are described in Sections 3.2.1.1.4.1 through 3.2.1.1.4.4.

NOTE: In all cases of scan codes and scan code sequences described throughout this document, the codes are described in hexadecimal notation.

3.2.1.1.4.1. Normal Mode — Pad Lock Off

Table 3.2.1.1.4.1-1 Normal Mode — Pad Lock Off

Key	Scan Code
ESC	76
F1	05
F2	06
F3	04
F4	0C
F5	03
F6	0B
F7	83
F8	0A
F9	01
F10	09
F11	78
F12	07
INSERT	E0, 70
DELETE	E0, 71
1	16
2	1E
3	26
4	25
5	2E
6	36
7	3D
8	3E
9	46

Table 3.2.1.1.4.1–1 Normal Mode — Pad Lock Off (continued)

0	45
-	4E
=	55
Backspace	66
`	0E
TAB	0D
Q	15
W	1D
E	24
R	2D
T	2C
Y	35
U	3C
I	43
O	44
P	4D
[	54
]	5B
HOME	E0, 6C
CAPS LOCK	58
A	1C
S	1B
D	23
F	2B
G	34
H	33
J	3B
K	42
L	4B
;	4C
'	52
RETURN	5A
END	E0, 69
L SHIFT	12
Z	1A
X	22
C	21
V	2A
B	32
N	31
M	3A

Table 3.2.1.1.4.1-1 Normal Mode — Pad Lock Off (continued)

,	41
.	49
/	4A
R SHIFT	59
PAGE UP	E0, 7D
FN	–
L CONTROL	14
L ALT	11
SPACE	29
R ALT	E0, 11
R CONTROL	E0, 14
\	5D
UP ARROW	E0, 75
PAGE DOWN	E0, 7A
LEFT ARROW	E0, 6B
DOWN ARROW	E0, 72
RIGHT ARROW	E0, 74

3.2.1.1.4.2. Normal Mode — Fn Promotion

Table 3.2.1.1.4.2-1 Normal Mode — Fn Promotion

Keys	Scan Code	Notes
F1	Make: E0, 12, E0, 7C Break: E0, F0, 7C, E0, F0, 12	PrtScr
F2	Make: 11, 84 Break: F0, 84, F0, 11	SysReq
F3	17	Optional
F4	1F	Optional
F8	27	Optional
F9	2F	Optional
F10	37	Optional
F11	77	NumLock
F12	–	PadLock
INSERT	E1, 14, 77, E1, F0, 14, F0, 77	Pause — NOTE 1
DELETE	14, E0, 7E, E0, F0, 7E, F0, 14	Break — NOTE 1
7	6C	Keypad 7
8	75	Keypad 8
9	7D	Keypad 9
0	7B	Keypad –
BACKSPACE	7E	Scroll Lock
U	6B	Keypad 4
I	73	Keypad 5
O	74	Keypad 6
P	79	Keypad +
[	59, 46	Shift-R Parenthesis
]	59, 45	Shift-L Parenthesis
J	69	Keypad 1
K	72	Keypad 2
L	7A	Keypad 3
;	7C	Keypad *
RETURN	E0, 5A	Keypad Enter
M	70	Keypad 0
.	71	Keypad .
/	E0, 4A	Keypad /

Note 1. No break code is transmitted on release of this key.

3.2.1.1.4.3. Pad Lock Mode

Table 3.2.1.1.4.3–1 Pad Lock Mode

Keys	Scan Code	Notes
7	6C	Keypad 7
8	75	Keypad 8
9	7D	Keypad 9
0	7B	Keypad –
U	6B	Keypad 4
I	73	Keypad 5
O	74	Keypad 6
P	79	Keypad +
[	59, 46	Shift-R Parenthesis
]	59, 45	Shift-L Parenthesis
J	69	Keypad 1
K	72	Keypad 2
L	7A	Keypad 3
;	7C	Keypad *
RETURN	E0, 5A	Keypad Enter
M	70	Keypad 0
.	71	Keypad .
/	E0, 4A	Keypad /

3.2.1.1.4.4. Pad Lock Mode Fn Promotion (Back to Normal Mode)

Table 3.2.1.1.4.4–1 Pad Lock Mode Fn Promotion (Back to Normal Mode)

Keys	Scan Code
7	3D
8	3E
9	46
0	45
U	3C
I	43
O	44
P	4D
[	54
]	5B
J	3B
K	42
L	4B
;	4C
RETURN	5A
M	3A
.	49
/	4A

3.2.1.1.5. Data Transmission

Data shall be transmitted from the keyboard to the system if transmissions are not inhibited by the system (clock line held low) and if there is some code to be transmitted: i.e. key codes, status codes, or the resend code. If the data transmission was not successful, the system shall transmit the Resend command (FE) to request that the code be retransmitted by the keyboard.

Transmission shall be bi-directional in serial synchronous form, with the data stream consisting of eleven bits: one start bit of logical zero, eight data bits, one even parity bit, and one stop bit of logical one. Clocking of the data stream shall be done by the keyboard, even if the system issues a request to send (data line held low) to transmit a command.

3.2.1.1.6. Data Reception

Commands shall be transmitted from the system to the keyboard by holding the clock line low (inhibit keyboard transmission), setting the data line low (request to send), and then releasing the clock line. The keyboard shall then acknowledge the request by clocking in the eleven bit serial data stream. If transmission was successful, the keyboard shall send the Acknowledge code (FA); if the transmission was not successful, the keyboard shall send the Resend code (FE).

3.2.1.1.7. Commands and Status

3.2.1.1.7.1. System Commands

The keyboard shall accept commands issued from the system and sent through the keyboard controller as described in Table 3.2.1.1.7.1–1.

The system shall issue a two byte command code to the keyboard for the NUM LOCK, CAPS LOCK, and SCROLL LOCK functions. The code shall be interpreted by the keyboard and shall illuminate the corresponding mode status indicators for which the bits in the second byte have been set, as described in Table 3.2.1.1.7.1–1.

Table 3.2.1.1.7.1–1 System Commands to Keyboard

Code	Command	
ED, 01	Set Mode Indicator:	Scroll Lock
ED, 02		Num Lock
ED, 04		Caps Lock
EE	Echo	
F0	Select Scan Code Set	
F2	Read ID	
F3	Set Typematic Rate/Delay — NOTE 1	
F4	Enable	
F5	Default Disable	
F6	Set Default	
F7	Set All Keys:	Typematic
F8		Make/Break
F9		Make
FA		Typematic/Make/Break
FB	Set Key Types:	Typematic
FC		Make/Break
FD		Make
FE	Resend	
FF	Reset	

Note 1. F2 is followed by a byte indicating typematic rate and delay. Bits 5 and 6 select the delay from 250 milliseconds ±20% to 1 second ±20%. Bits 0–4 select the repeat rate from 30.0 ±20% per second (00000) to 2 ±20% per second (11111).

3.2.1.1.7.2. Keyboard Messages

The keyboard shall send messages to the system through the keyboard controller as described in Table 3.2.1.1.7.2–1. The keyboard shall acknowledge system commands by sending the Acknowledge code (FA) to the system and then shall execute the command, except in the case of the Echo command where the keyboard shall send back the Echo code (EE) to the system instead of the Acknowledge code.

Table 3.2.1.1.7.2–1 Keyboard Messages to System

00 or FF	Error
AA	Test OK
EE	Echo Response
F0	Break Prefix
FA	ACK
FC	Diagnostic Failure
FE	Resend

The keyboard shall send status codes to the system under the following conditions:

- At the end of the reset routine the keyboard shall send the Diagnostic OK code (AA) or the Diagnostic Failure code (FD);
- After receiving a command the keyboard shall send an Acknowledge code (FA) or the Resend code (FE);
- If the FIFO becomes full and one or more keycodes are received causing a buffer overrun, the Error code (00 or FF) shall be sent after sending all the 16 codes in the FIFO;
- If conditions in the keyboard make it impossible to identify a switch closure or to identify a key, the Error code shall be sent (00 or FF);
- The two byte keyboard ID (83, AB) shall be sent in response to the READ ID command.

3.2.1.1. Keyboard

The keyboard assembly shall consist of an alphanumeric American Standard 82 key 'QWERTY' style keyboard with function keys, screen/cursor control keys and four keyboard status indicators. The keyboard shall support the IBM-PC AT type 101-key keyboard functions. Figure 3.2.1.1–1 shows the overall view of the keyboard.

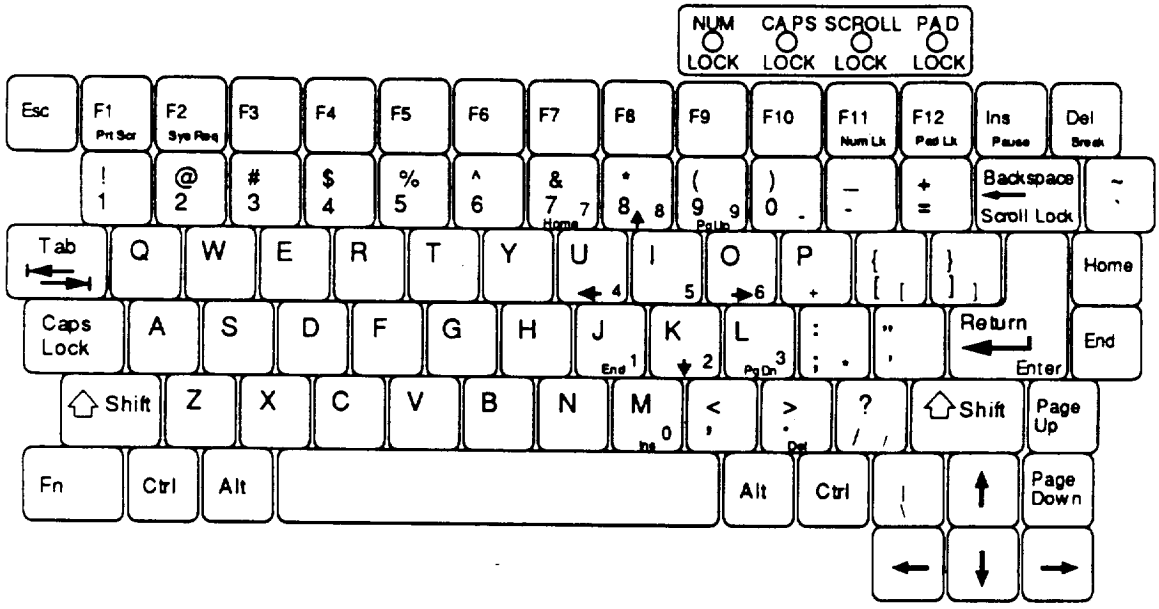


Figure 3.2.1.1–1 Keyboard

The keys shall repeat, after a short delay, when they are pressed and held down.

The keyboard electronics shall be capable of supporting 82 keys with minimum 3-key rollover and shall support, as a minimum, the following functions:

- Reset the keyboard microcontroller and initialize variables upon power up or software reset.
- Scan the keyboard for key status changes.
- Transmit any available data or status (if enabled by the system).
- Receive, acknowledge, and execute commands from the system.

3.2.1.1.1. Keyboard Reset

The keyboard shall execute the reset routine for initial power on, and thereafter upon a software Reset command (FF) from the system. The reset routine shall first initialize the keyboard by initializing the FIFO (First-In-First-Out data buffer), clearing the key status, resetting the counters, and enabling the key click (unless it was disabled and it is a software reset).

The reset routine shall then test the RAM and perform a ROM CHECKSUM. If all tests pass, the reset routine shall then send a Diagnostic OK code (AA) to the system. If one of the tests failed, a Diagnostic Failure code (FC) shall be sent to the system.

3.2.1.1.2. Keyboard Modes

The keyboard shall have four different modes. There shall be two "Normal" modes and two "Pad Lock" modes, each with an associated function key (Fn) promotion. Fn Promotion is achieved by holding down the Fn key while pressing another key. The four modes are described in Table 3.2.1.1.2–1.

Table 3.2.1.1.2–1 Keyboard Modes

Normal Mode — Pad Lock Off
Normal Mode — Fn Promotion
Pad Lock Mode — Pad Lock On
Pad Lock Mode — Fn Promotion (Back to Normal Mode)

3.2.1.1.3. Keyboard Scan

The keyboard shall be continuously scanned to detect key changes, unless keyboard scanning is disabled by a Default Disable (F5) command from the system. If there is a change detected after a rebounding delay, or if the last key pressed is still down after a repeat delay, the code for that key change shall be sent to the keyboard controller in the computer.

3.2.1.1.8. Multipurpose Keys

The 82-key keyboard shall support the entire IBM-PC AT 101-key function set by way of key press combinations and/ or various keyboard modes.

The various functions for each key are indicated by color coded symbols on top or on the front of the key. The character or action that a specific key enters, shall be determined by the combination of the character key and either the FN key, or the SHIFT key, and by the operating mode of the keyboard as described in Section 3.2.1.1.2.

3.2.1.3. Status Indicators

The APW II Keyboard Assembly shall have four status indicators that shall illuminate to show positive functioning of the respective keyboard status. The state of the status indicators shall be unambiguous when viewed in direct sunlight. The indicators and their functions are described in Table 3.2.1.3–1 and in Section 3.2.1.1.7.1. Figure 3.2.1.1–1 shows the approximate location of the status indicators located above the F9, F10, F11, and F12 function keys on the top row of keys.

Table 3.2.1.3–1 Status Indicators

Status Indicator	Function
NUM LOCK	Number Key Function Lock
CAPS LOCK	Caps Key Lock
SCROLL LOCK	Scroll Key Function Lock
PAD LOCK	Pad Key Function Lock

3.2.2. Performance Characteristics

The keyboard shall meet the mechanical performance test conditions described in Table 3.2.2–1.

Table 3.2.2–1 Mechanical Performance Test Conditions

Item	Test Conditions	Requirements
Actuating Force	Placing the key such that the direction is vertical and then gradually increasing the load applied to the center of the stem, the maximum load required for the stem to come to a stop shall be measured.	70 ±25 g
Travel	Placing the key such that the direction is vertical and then applying a static load twice the actuating force to the center of the stem, the travel distance for the stem to come to a stop shall be measured.	2.3 ±.5 mm
Stop Strength	Placing the key such that the direction is vertical, a static load of 5 kg shall be applied in the direction of stem operation for a period of 60 seconds.	There shall be no sign of damage mechanically or electrically
Stem Strength	Placing the key such that the direction is vertical, the maximum force to withstand a pull applied opposite to the direction of stem operation shall be measured.	2.5 kg
Tactility	The center of the stem shall be struck lightly at a rate encountered in normal use (3 to 4 operations per second)	Free of noticeable binding
Peak Load	Placing the key such that the direction is vertical and then gradually increasing the load applied to the center of the stem, the maximum load required for the key to make shall be measured.	55 ±15 g
Crew Applied Loads	The keyboard shall withstand crew loads of 57 kg from any direction distributed over an area of one square foot without failure.	57 kg

3.2.3. Electrical Characteristics

3.2.3.1. Power Requirements

The APW II Keyboard Assembly shall comply with the voltage and current specified in Table 3.2.3.1–1. Decoupling capacitors shall be provided within the keyboard electronics.

Table 3.2.3.1–1 Keyboard Power Requirements

Voltage	Current
+5 VDC ±10%	300 mA Max.

3.2.3.1.1. Part Number 65442-1

Power for APW II Keyboard Assembly Part Number 65442-1 shall be provided through pin contact 4 of the circuit board header connector, with logic ground on pin contact 3. See Section 3.2.3.6.1.

3.2.3.2. Interface Logic Levels

Logic levels at the interface connector shall conform to standard 5V TTL or CMOS voltage levels.

The clock and data lines shall be driven by buffers with 2 kΩ pull-up resistors and 47 pF capacitors to ground.

3.2.3.3. Key Contacts

The key contacts shall conform to the specifications in Table 3.2.3.3-1.

Table 3.2.3.3–1 Key Contact Specifications

Type of actuation	Momentary
Contact Arrangement	Single pole single throw
Contact Minimum Ratings	12 VDC @ 5 mA

3.2.3.4. Interface

The keyboard shall operate with standard IBM-PC type computers and shall communicate using the keyboard serial data interface.

3.2.3.5. Status Indicators

The APW II Keyboard Assembly status indicators shall be driven by the keyboard and shall not require an additional external source of power.

3.2.3.6. Interface Connector

3.2.3.6.1. Part Number 65442-1

The APW II Keyboard Assembly Part Number 65442-1 interface shall be a Molex 5268–NA Series 6-pin right angle fully shrouded header connector, and shall be mounted on the circuit board approximately as shown in Figure 3.2.4.1–1. The contact assignments for the connector shall be as described in Table 3.2.3.6.1–1.

Table 3.2.3.6.1–1 Connector Contact Assignments (65442-1)

Position	Function
1	KEYBOARD CLOCK
2	KEYBOARD DATA
3	KEYBOARD LOGIC GND
4	KEYBOARD +5V DC
5	N/C
6	KEYBOARD CHASSIS GND

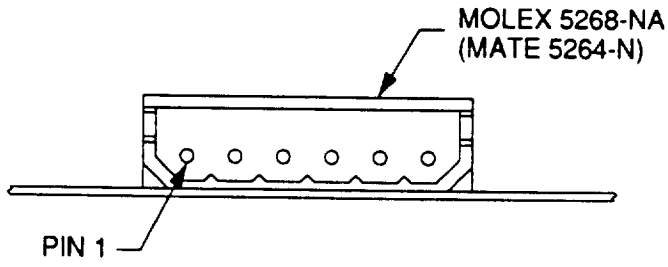
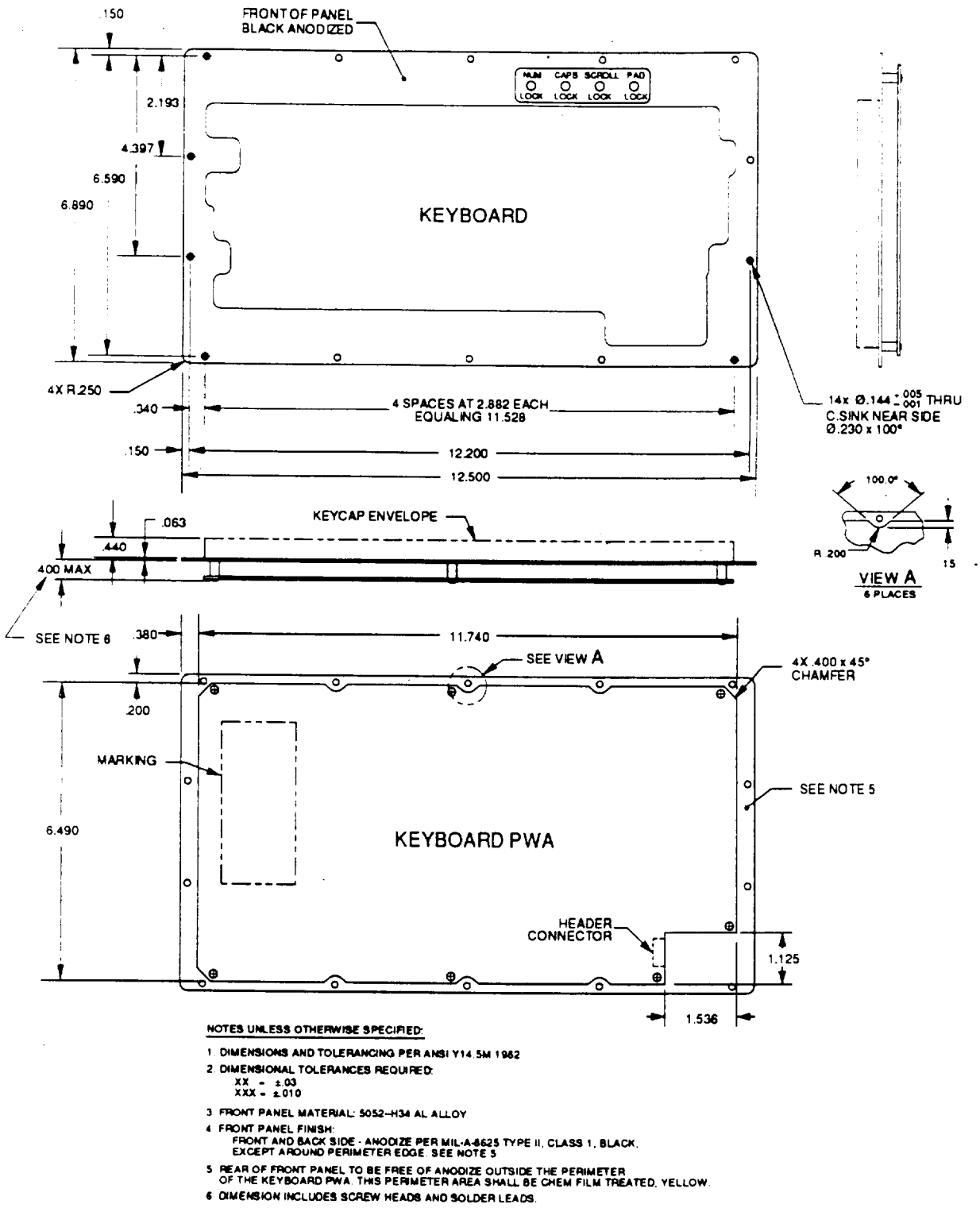


Figure 3.2.3.6.1–1 Connector Configuration (65442-1)

3.2.4. Mechanical Characteristics

3.2.4.1. Dimensions

The APW II Keyboard Assembly shall comply with the dimensions as shown in Figure 3.2.4.1–1 for Part Number 65442-1.



NOTES UNLESS OTHERWISE SPECIFIED:

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M 1982
2. DIMENSIONAL TOLERANCES REQUIRED:
   XX = ±.03
   XXX = ±.010
3. FRONT PANEL MATERIAL: 5052-H34 AL ALLOY
4. FRONT PANEL FINISH:
   FRONT AND BACK SIDE - ANODIZE PER MIL-A-8625 TYPE II, CLASS 1, BLACK.
   EXCEPT AROUND PERIMETER EDGE. SEE NOTE 5
5. REAR OF FRONT PANEL TO BE FREE OF ANODIZE OUTSIDE THE PERIMETER OF THE KEYBOARD PWA. THIS PERIMETER AREA SHALL BE CHEM FILM TREATED, YELLOW.
6. DIMENSION INCLUDES SCREW HEADS AND SOLDER LEADS.

Figure 3.2.4.1–1 Physical Dimensions (65442-1)

3.2.4.2. Weight

The APW II Keyboard Assembly, including cable and connector, shall not exceed 2.0 lb. (907 g).

3.2.4.3. Keytop Legends

The APW II Keyboard Assembly keytop legends shall be double shot molded, sublimation printed, or by other equivalent durable manufacturing technique.

3.2.4.4. Marking

The APW II Keyboard Assembly shall be clearly marked with the information in Table 3.2.4.4-1 in the location shown in Figure 3.2.4.1-1. The vendor's identification and identifying number may also be included.

Table 3.2.4.4–1 Marking

54779 SOCN 65442 (applicable dash number)
Serialization Number

3.2.4.5. Keycap Color

The keycaps of the APW II Keyboard Assembly shall be off white in color. The legends shall be black for the key primary function and blue for secondary functions (such as in padlock mode). The vendor shall submit sample keys with legends of both colors to SAI Technology for approval.

3.2.5. Documentation

Existing standard commercial documentation shall be provided. This documentation shall, as a minimum, describe the hardware, interfaces, capabilities and specifications and provide the user with installation, set-up, interfacing, and diagnostic guidelines.

3.2.6. Reliability

The APW II Keyboard Assembly shall have a predicted mean-time-between-failures (MTBF) of no less than 12,000 hours. These MTBF figures are predicted on the basis of component failure rates per MIL-HDBK-217E Notice 1 assuming the following conditions:

- Ambient (free air) temperature 25°C.
- Ground Fixed Environment.

3.2.7. Maintainability

The APW II Keyboard Assembly shall have no user-maintainable components.

3.2.8. Environmental Conditions

The APW II Keyboard Assembly shall perform within specified limits subsequent to exposure to the environmental conditions specified in the following paragraphs. These environmental conditions shall use MIL-STD-810E procedures, or equivalent, as limited herein.

Table 3.2.8–1 Ambient Temperatures

Operating	Non–Operating
0 to +65 °C (+32 to +149 °F)	–25 to +75 °C (–13 to +167 °F)

3.2.8.1. Operating Temperature

The APW II Keyboard Assembly shall be capable of continuous operation over an ambient air temperature range as shown in Table 3.2.8-1. The APW II Keyboard Assembly shall not require external cooling or heating other than natural convection for continuous operation.

3.2.8.2. Non-Operating Temperature

The APW II Keyboard Assembly shall be designed so that it will not be damaged nor will the operational performance be degraded when restored to the operating temperature range after exposure for a 72 hour period in a non-operating ambient temperature range as shown in Table 3.2.8–1.

3.2.8.3. Temperature Shock

The APW II Keyboard Assembly shall operate without degradation of specified performance after being subjected to variations in temperature in the non-operating mode as shown in table 3.2.8.3–1.

Table 3.2.8.3–1 Temperature Shock

+49 to –25 °C (+120 to –13 °F) in a 10 minute interval

3.2.8.4. Operating Humidity

The APW II Keyboard Assembly shall be designed so that it shall operate during and after exposure to humid conditions, including conditions where condensation occurs, as shown in Table 3.2.8.4–1.

Table 3.2.8.4–1 Relative Humidity

Operating	Non–Operating
10 to 95 %	5 to 95 %

3.2.8.5. Non-Operating Humidity

The APW II Keyboard Assembly shall be designed so that it will survive exposure to humid conditions, including conditions where condensation occurs, as shown in Table 3.2.8.4–1.

3.2.8.6. Altitude

The APW II Keyboard Assembly shall operate without degradation of specified performance at altitudes from sea level to 30,000 feet.

3.2.8.7. Fungus

The APW II Keyboard Assembly shall not contain exposed fungus nutrient materials. Only inherently fungus inert materials shall be used in the APW II Keyboard Assembly. The APW II Keyboard Assembly shall not support fungus growth. Table 3.2.8.7–1 summarizes the susceptibility of materials.

Table 3.2.8.7–1 Fungi Susceptibility of Materials
(from MIL–STD–454K Table 4–I)

GROUP I (Fungus-inert in all modified states and grades)	
Acrylics	Polyamide[1]
Acrylonitrile-styrene	Polycarbonate
Acrylonitrile-vinyl-chloride copolymer	Polyester-glass fiber laminates
Asbestos	Polyethylene, high density (>.94)
Ceramics	Polyethylene terephthalate
Chlorinated polyether	Polyimide
Flourinated ethylenepropylene copolymer (FEP)	Polymonochlorotrifluoroethylene
Glass	Polypropylene
Metals	Polystyrene
Mica	Polysulfone
Plastic laminates:	Polytetrafluoroethylene
Silicone-glass fiber	Polyvinylidene chloride
Phenolic-nylon fiber	Silicone resin
Diallyl phthalate	Siloxane-polyolefin polymer
Polyacrylonitrile	Siloxane-polystyrene
GROUP II (Not fungus-resistant in all grades; fungus resistance shall be established by test)	
ABS	Polydiclorostyrene
Acetal resins	Polyethylene, low and medium density (.94 and below)
Cellulose acetate	Polymethyl methacrylate
Cellulose acetate butyrate	Polyurethane (the ester types are particularly susceptible)
Epoxy glass fiber laminates	Polyricinoleates
Epoxy resin	Polyvinyl chloride
Lubricants	Polyvinyl chloride acetate
Melanine-formaldehyde	Polyvinyl fluoride
Organic polysulphides	Rubbers, natural and synthetic
Phenol-formaldehyde	Urea formaldehyde

[1] Literature shows that under certain conditions polyamides may be attacked by selective micro-organisms. However, for military applications they are considered Group I.

3.2.8.8. Dust Seal

The APW II Keyboard Assembly be sealed against dust and shall operate without degradation of specified performance after being subjected to a dust filled environment.

3.2.8.9. Vibration

Any integrated circuit devices which are installed in sockets on the APW II Keyboard Assembly shall be equipped with a positive-retention mechanism such as a latch, strap, or similar device.

The APW II Keyboard Assembly shall be able to withstand, at a minimum, a random vibrational force over a frequency range of 20 to 2000 Hz in the operating and non-operating modes as described in Table 3.2.8.9-1.

Table 3.2.8.9-1 Vibration

Frequency	Force
20 Hz	.02 G^2/Hz
20–80 Hz	+3 dB/ octave
80–500 Hz	.08 G^2/Hz
500–2000 Hz	–3 dB/ octave

3.2.8.10. Shock

The APW II Keyboard Assembly shall be able to withstand a shock for a period of 11 ms, 1/2 sine-wave pulse, in the operating and non-operating modes as described in Table 3.2.8.10-1.

Table 3.2.8.10-1 Shock

Operating	Non–Operating
40 G	40 G

3.2.8.11. Orientation

The APW II Keyboard Assembly shall be capable of being operated in any orientation.

3.2.8.12. Explosive Atmosphere

The APW II Keyboard Assembly shall not cause ignition of any ambient explosive gaseous mixture with air when operating in such an atmosphere.

3.2.9. Transportability

The APW II Keyboard Assembly shall be shipped in a shock resistant container suitable for standard common-carrier transportation.

3.3. Design and Construction

The detailed design and construction of the APW II Keyboard Assembly shall meet the environmental, electrical and mechanical criteria established in Section 3.2.

3.3.1. Materials, Processes and Parts

Parts, materials, and processes shall be specified as appropriate to obtain the desired electrical, mechanical, environmental and reliability characteristics of this source control document. Materials used in the construction of the APW II Keyboard Assembly which are not covered by applicable specifications shall be of the best commercial quality.

Processes and treatments (welding, soldering, brazing and corrosion-resistance protection) of the APW II Keyboard Assembly shall be in accordance with best commercial practice.

3.3.1.1. Finish

The keyboard mounting panel shall be black anodized per MIL-A-8625, Type II, Class I on the front side and shall be chem film treated per MIL-C-5541 Class 3, yellow on the back side. (See Figures 3.2.4.1-1 and 3.2.4.1-2).

3.3.1.2. Conformal Coating

All printed wiring boards that make up the APW II Keyboard Assembly shall be conformal coated using Dow Corning 3140 RTV silicone rubber coating per MIL-A-46146 Type II. If required, key contact areas may be free of conformal coating.

3.3.2. Electromagnetic Radiation (EMI)

The APW II Keyboard Assembly shall meet the requirements of FCC Part 15, Subpart J, Class B for radiated emissions when properly installed as a component of the LSLE/Microcomputer-2.

3.3.3. Identification and Marking

The APW II Keyboard Assembly shall be marked in accordance with best commercial standard practice, and shall show the information in Section 3.2.4.4, in accordance with MIL–STD–130.

3.3.4. Workmanship

Workmanship in the fabrication and assembly of the APW II Keyboard Assembly shall comply with best commercial standard practice. The fabrication shall be processed in such a manner as to be uniform in quality and shall be free from defects that would affect life, serviceability, and appearance.

3.3.5. Interchangeability

All parts having the same part number shall be functionally and dimensionally interchangeable.

3.3.6. Human Performance and Human Engineering

Human engineering design criteria and principles shall be applied in the design of the APW II Keyboard Assembly so as to achieve safe, reliable and effective performance by operator, maintenance and control personnel and to optimize personnel skill requirements and training time. The APW II Keyboard Assembly shall be designed to insure maximum efficiency, ease of use, operator safety and minimum degradation and variability in system performance.

3.3.7. Product Change

Vendor shall notify SAI Technology in writing prior to the implementation of any change to the product under this source control document which would affect performance, quality, reliability, size, weight, or interchangeability of parts.

SAI Technology must issue written approval prior to the implementation of these changes. A SAI Technology representative's signature must appear on the original change request form and be part of the permanent record.

3.3.8. Standards of Manufacture

The manufacture of the APW II Keyboard Assembly shall comply with best commercial standard practice.

3.4. Acceptance Testing

Each APW II Keyboard Assembly shall be subjected by the vendor to a 24 hour burn-in at a minimum temperature of 20°C. The vendor shall certify compliance to this source control document for all assemblies after this burn-in period.

3.5. Approved Source(s) of Supply

Only the item(s) described by this document when procured from the vendor(s) listed in Table 3.5–1 is approved for use in the application specified hereon. A substitute item shall not be used without prior approval by SAIT.

Identification of the approved source(s) of supply hereon is not to be construed as a guarantee of present or continued availability as a source of supply for the item(s).

Table 3.5–1 Approved Source(s) of Supply

Dash Number	Manufacturer Part Number	Manufacturer
–1	TBD	Flex-Key Corporation Emerson Ave. Gloucester, MA 01930 (508) 281–2040

4. QUALITY ASSURANCE PROVISIONS

4.1. General

All deliverable items shall be inspected and tested according to best commercial practice, and in accordance with the acceptance criteria of paragraph 3.4. herein.

4.2. Responsibility for Inspection

Unless otherwise specified in the contract, purchase order, or this source control document, the manufacturer is responsible for the performance of all inspection requirements to insure compliance with this source control document. Except as otherwise specified, the manufacturer may utilize its own facilities or any commercial laboratory.

4.2.1. Special Tests and Examinations

4.2.1.1. Altitude

The APW II Keyboard Assembly shall be subjected to the altitude test specified in MIL-STD-810E, Method 500.3, Procedure II at 30,000 feet, or an equivalent procedure to demonstrate the required performance. Specific requirements are contained in Section 3.2.8.6.

4.2.1.2. Temperature

The APW II Keyboard Assembly shall be subjected to the temperature test specified in MIL-STD-810E, Method 501.3, Procedures I and II, and Method 502.3, Procedures I and II, or equivalent procedures to demonstrate the required performance. Specific requirements are contained in sections 3.2.8.1 and 3.2.8.2.

4.2.1.3. Temperature Shock

The APW II Keyboard Assembly shall be subjected to the temperature shock test specified in MIL-STD-810E, Method 503.3, Section II-3, or an equivalent procedure to demonstrate the required performance. Specific requirements are contained in Section 3.2.8.3.

4.2.1.4. Fungus

The APW II Keyboard Assembly shall be subjected to analysis to verify the requirements of Section 3.2.8.7. are met.

4.2.1.5. Vibration

The APW II Keyboard Assembly shall be subjected to the vibration test specified in MIL-STD-810E, Method 514.4, Procedure I, or an equivalent procedure to demonstrate the required performance. Specific requirements are contained in section 3.2.8.9.

4.2.1.6. Shock

The APW II Keyboard Assembly shall be subjected to the shock test specified in MIL-STD-810E, Method 516.4, Procedures IV and VI, or an equivalent procedure to demonstrate the required performance. Specific requirements are contained in section 3.2.8.10.

4.2.1.7. Orientation

The APW II Keyboard Assembly shall operate when oriented in any axis. Specific requirements are contained in Section 3.2.8.11.

4.2.1.8. Explosive Atmosphere

The APW II Keyboard Assembly shall be subjected to analysis to verify the requirements of Section 3.2.8.12. are met.

4.3. Analysis

The vendor shall demonstrate by analysis that all requirements of this source control document are met. The analysis must demonstrate, in particular, that the expected service life will be met under the stated parameters and conditions.

4.4. Right of Inspection

SAI Technology shall have access to all test equipment or facilities for performance of acceptance inspections at no cost to SAI Technology. Inspections will be limited to those activities that are specific and required to manufacture and test the APW II Keyboard Assembly.

5. PREPARATION FOR DELIVERY

Packaging shall be to best commercial practice.

6. NOTES

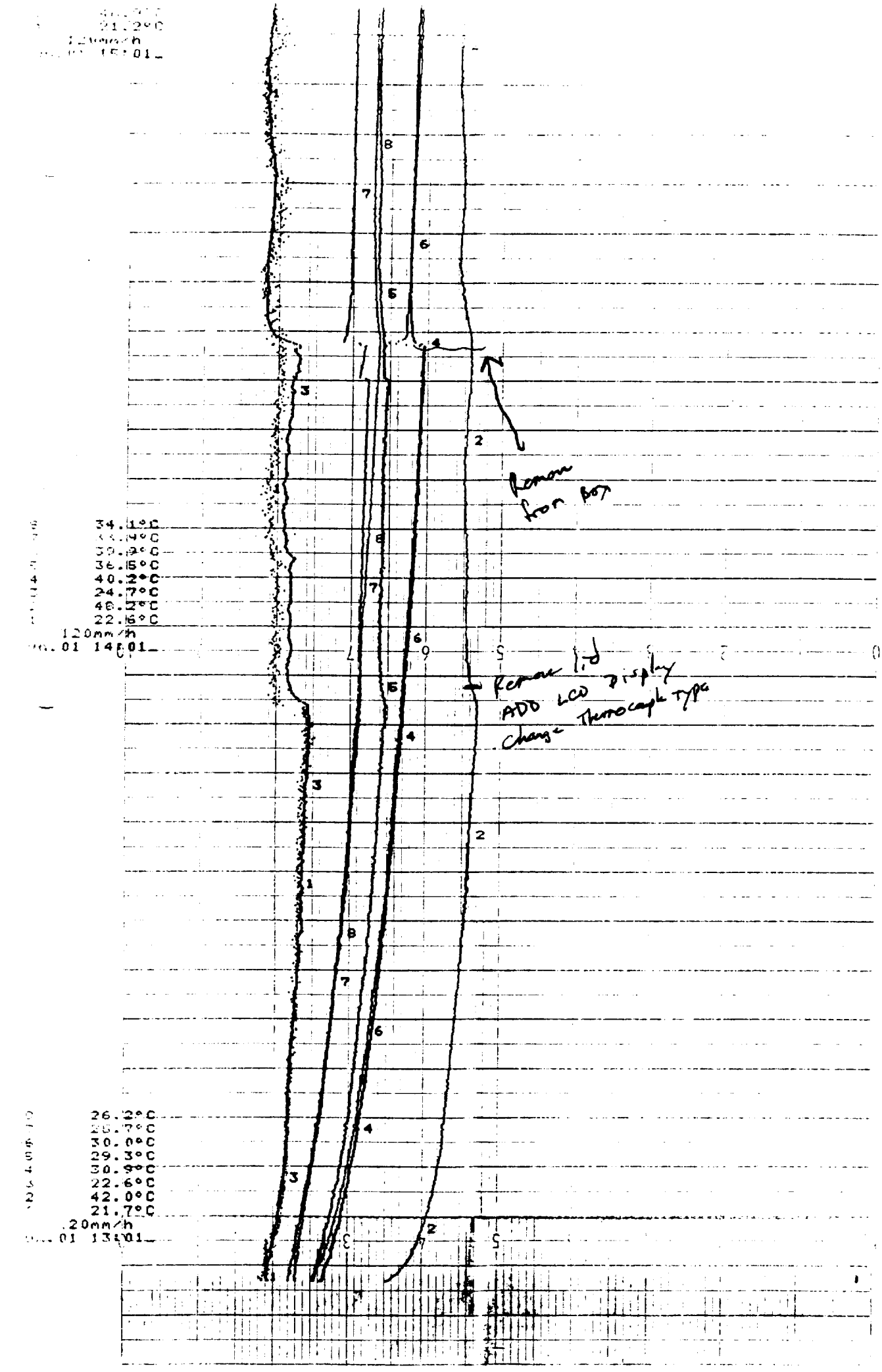
10. APPENDIX A – List of Acronyms and Abbreviations

dB	Decibel
FIFO	First-In-First-Out (data buffer)
g	gram
Hz	Hertz
kg	kilogram
kΩ	kilohm
lb.	pounds
mm	millimeter
ms	millisecond
MTBF	Mean Time Between Failures
MΩ	Megohm
N/C	No Connection
P/N	Part Number
pF	picofarad
PTFE	Polytetrafluoroethylene
°C	Degrees Celsius
°F	Degrees Fahrenheit
Ω	Ohm

APPENDIX 5

THERMAL, EMI TEST RESULTS

Thermal Survey Data Test Results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120mm/h
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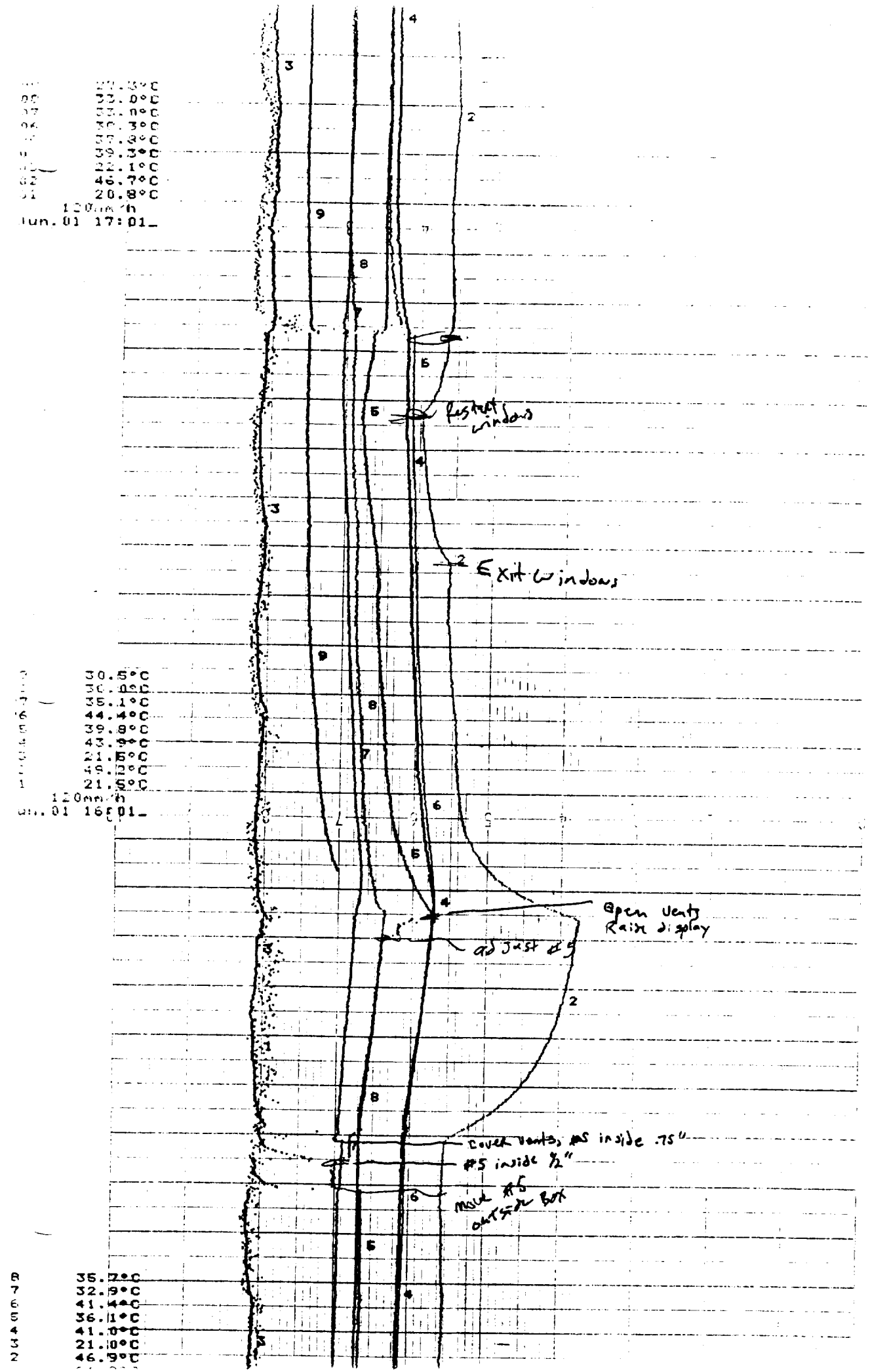
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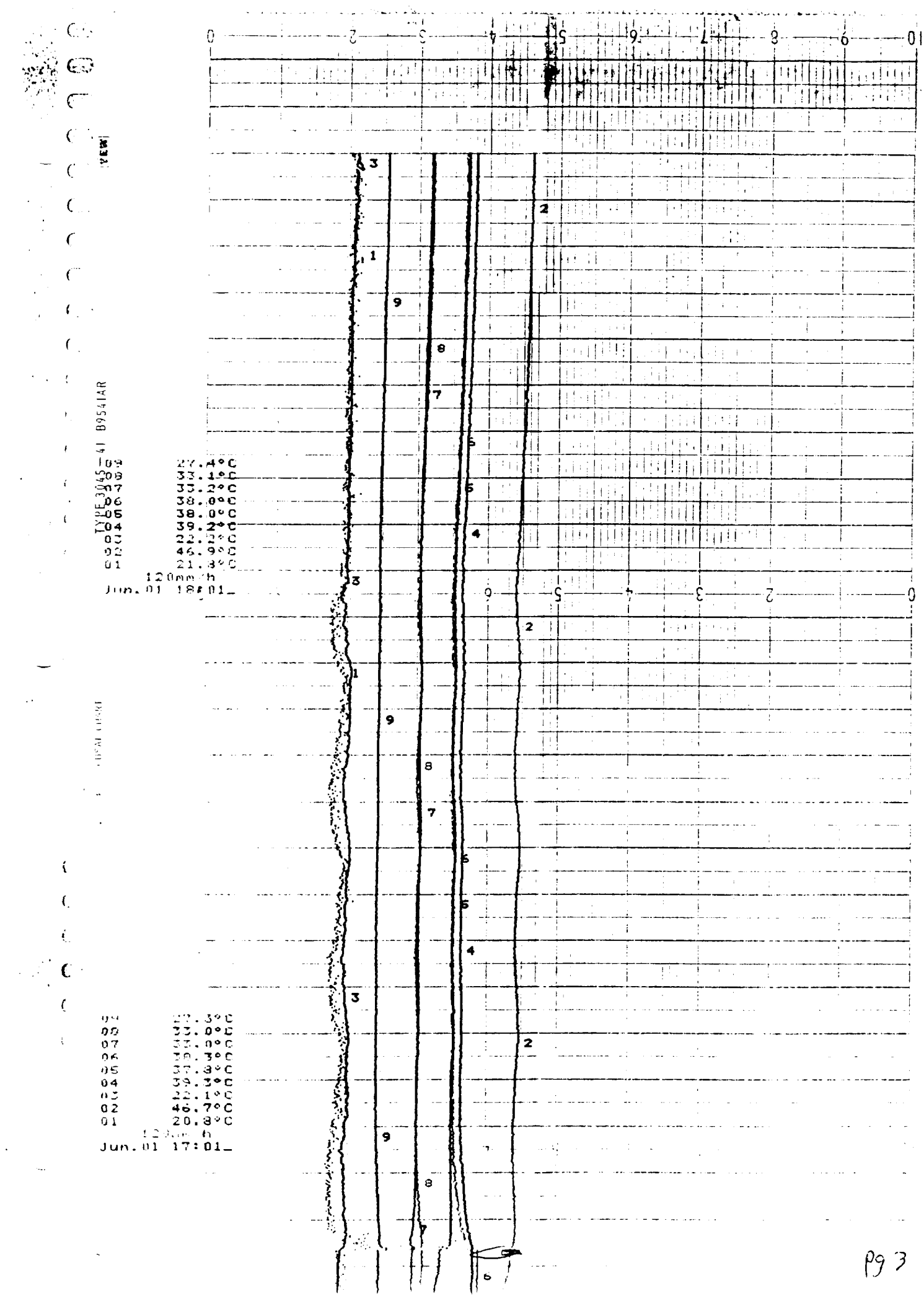
Exit windows
Open vents
Rain display
adjust #9
Cover vents, as inside .75"
#5 inside ½"
mount #5 outside box


TYPE3045-41 B954IAR
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P9 3

EMI Test Results

EMI TESTS - APW II

TEST DATE: 5/23/95

TEST OPERATORS: SAIC: TIM GIORGETTA
TELEDYNE-RYAN: EVERETT

UNIT UNDER TEST (UUT) : WNE WITH BATTERY MODULE, DISPLAY MODULE, AND KEYBOARD MODULE INSTALLED.

RE02 UUT SCAN 1:

The purpose of this scan was to establish a baseline characterization of the UUT. Noticeable outages were between 4MHZ and 400MHZ HORIZONTAL and VERTICAL polarization. NASA specification (MSFC 521B) was penciled in above the MIL-STD-461 limits. Based on scan 1's results it was decided to "SNIFF" the UUT to determine the major radiated emissions sources.

See ATTACHMENTS - PLOT TIME: 09:35 on 05:23:95.

SNIFFER:

2-25MHZ RANGE
- Display - lower left corner
  - 0.59MHZ spikes and 2.07MHZ spikes
- Floppy Disk Drive Opening
  - 0.59MHZ spikes
- Battery Cable - charging from DC
  - 0.59MHZ spikes at end of spectrum
- Battery Cable - UUT power from battery
  - 0.59MHZ spikes

25-100MHZ
- Battery Cable - charging from DC
  - 1MHZ spikes
- Display - lower left corner
  - 6.16MHZ spikes and 2.03 MHz spikes

100MHz - 200MHZ
- Display - lower left corner
  - 6.14MHZ spikes
- Battery Cable - charging from DC
  - little noise

200MHZ - 400 MHz
- Display - lower left corner
  - 24.57MHZ spikes and 6.14MHZ spikes

See ATTACHMENTS FOR VARIOUS RANGES AND LOCATIONS.

RE02 HP OMNI BOOK:

Out in lower frequency ranges (14KHZ to 2MHZ).
See ATTACHMENTS - PLOT TIME: 12:08 on 05:23:95.

RE02 UUT SCAN 2:

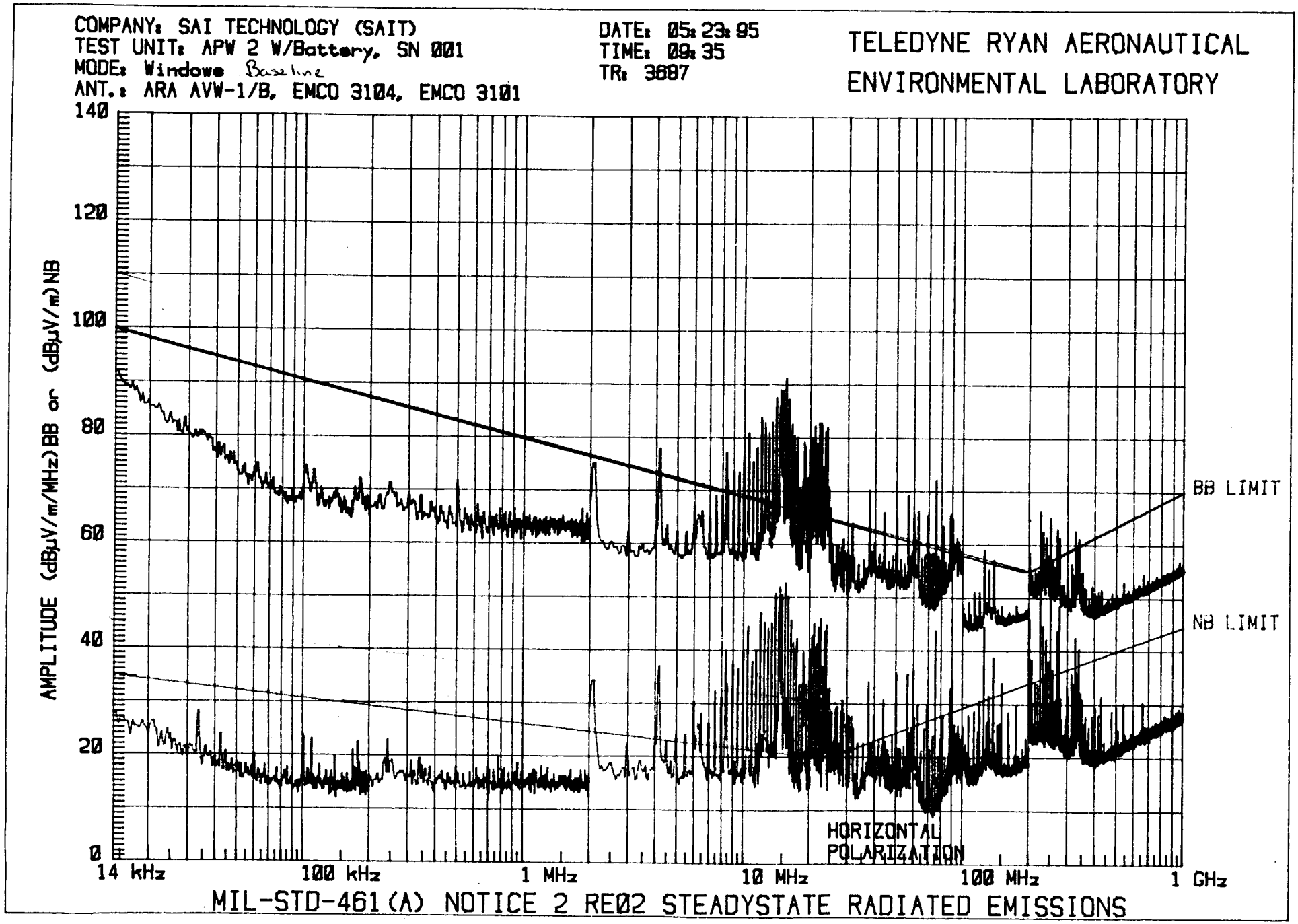
From "SNIFFER" data it was determined the the display opening was the largest contributor of radiated noise. This scan was taken with the display opening sealed off with a grounded sheet of aluminum foil. The results were greatly improved. Improved HORIZONTAL polorization reading except for one signal at approximately 14MHZ. This scan indicates that most of the radiated noise is coming out of the display window frame; lower left corner. A noticable amount of noise was still visible in the VERTICAL polarization.

See ATTACHMENTS - PLOT TIME: 13:21 on 05:23:95

RE02 UUT SCAN 3:

This last scan is the same as scan 2 except the battery has been removed from the system. It appeared from "SNIFFING" the UUT that the second major noise contributor was the battery cable. This plot is slightly better than the previous one, indicating that the battery module/cable is adding a small amount of noise to the system. The only remaining outage in this configuration is a 185MHZ signal in the VERTICAL polarization. It's source to be determined with future testing.

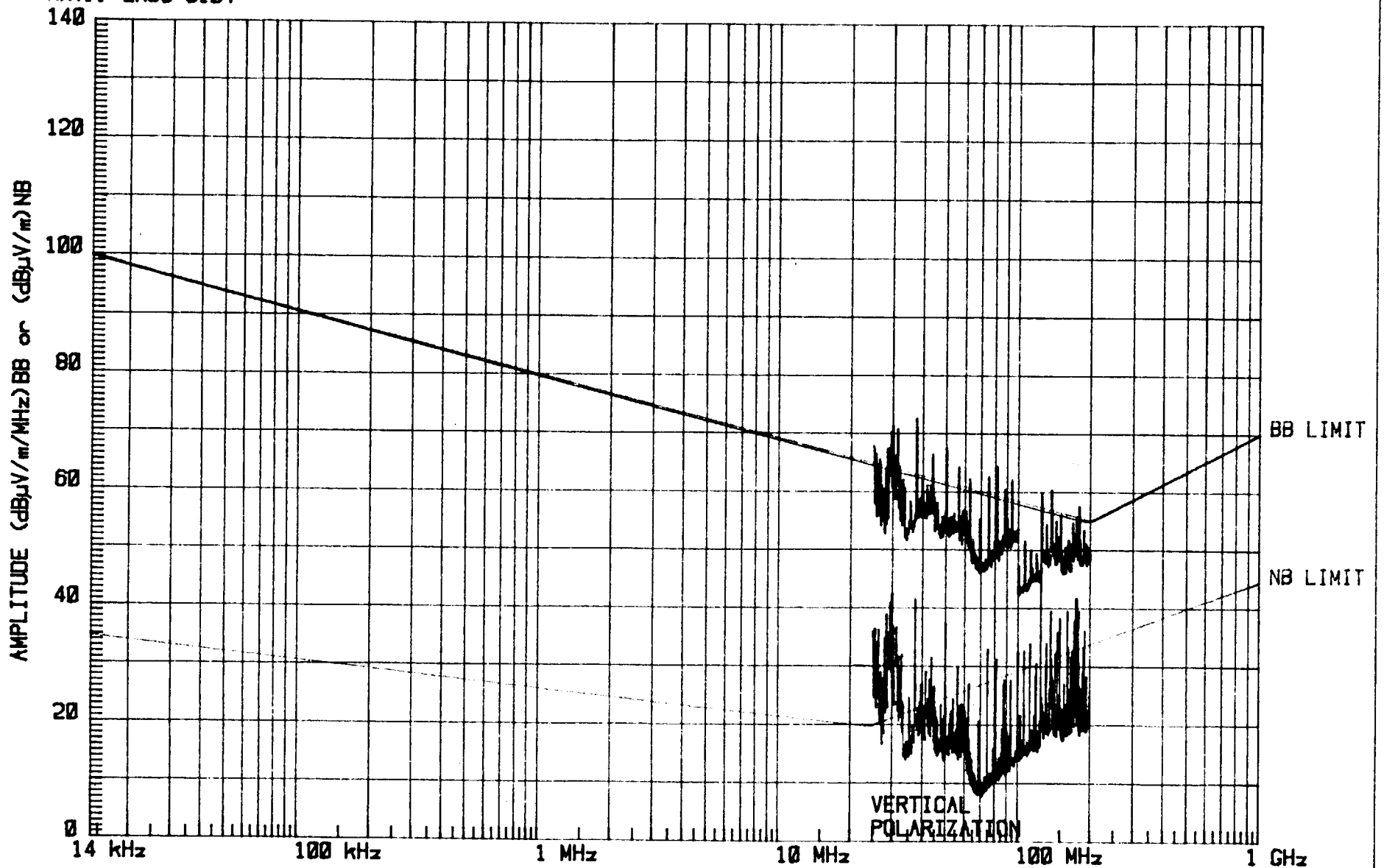
See ATTACHMENTS - PLOT TIME: 14:20 on 05:23:95


COMPANY: SAI TECHNOLOGY (SAIT)
TEST UNIT: APW 2 W/Battery, SN 001
MODE: Windowe Baseline
ANT.: ARA AVW-1/B, EMCO 3104, EMCO 3101
DATE: 05:23:95
TIME: 09:35
TR: 3687
TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY
AMPLITUDE (dBµV/m/MHz)BB or (dBµV/m)NB
140
120
100
80
60
40
20
0
14 kHz
100 kHz
1 MHz
10 MHz
100 MHz
1 GHz
BB LIMIT
NB LIMIT
HORIZONTAL
POLARIZATION
MIL-STD-461(A) NOTICE 2 RE02 STEADYSTATE RADIATED EMISSIONS

COMPANY: SAI TECHNOLOGY (SAIT)
TEST UNIT: APW 2 W/Battery, SN 001
MODE: Windows Baseline
ANT.: EMCO 3104

DATE: 05:23:95
TIME: 09:35
TR: 3687

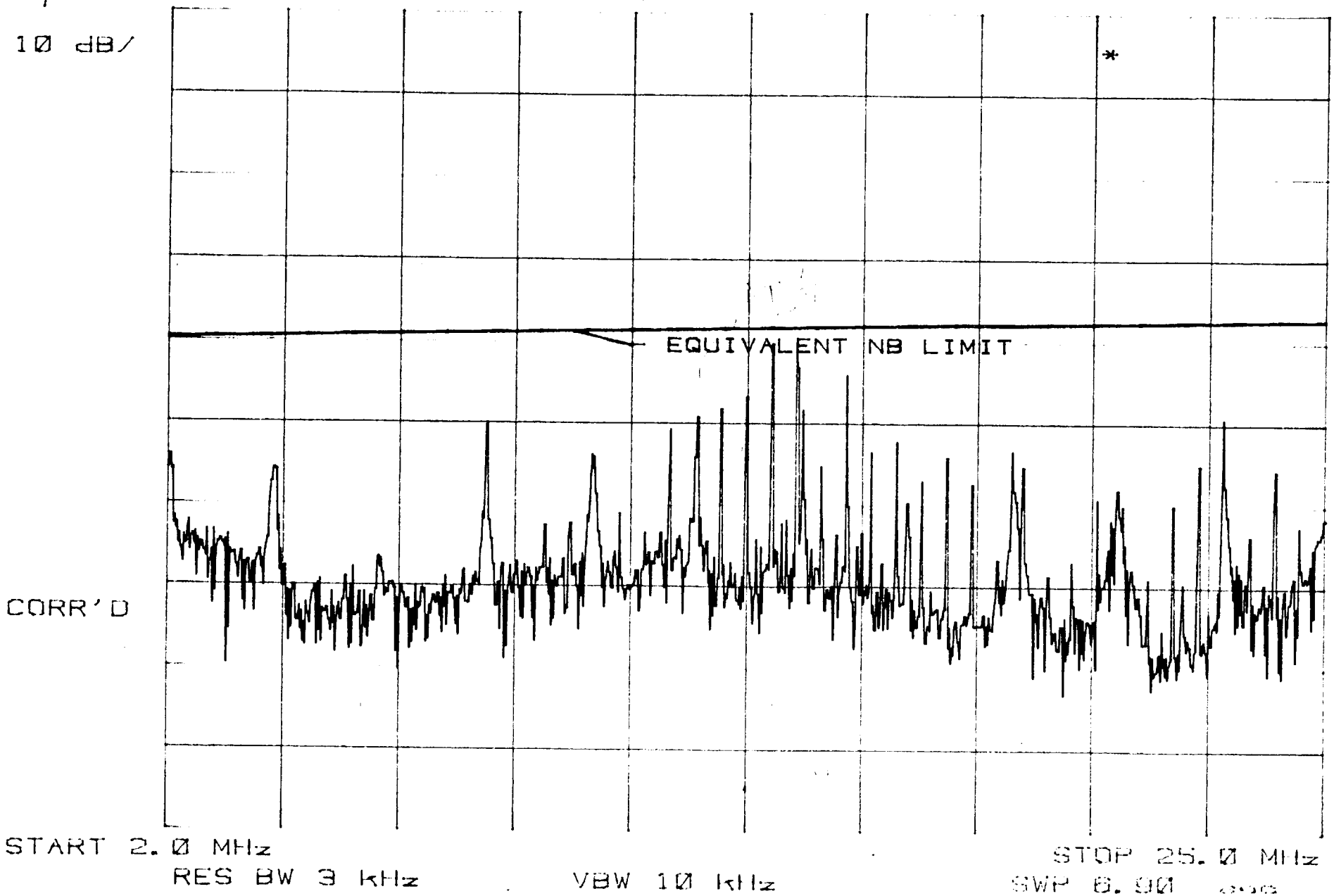
TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY



MIL-STD-461(A) NOTICE 2 RE02 STEADYSTATE RADIATED EMISSIONS

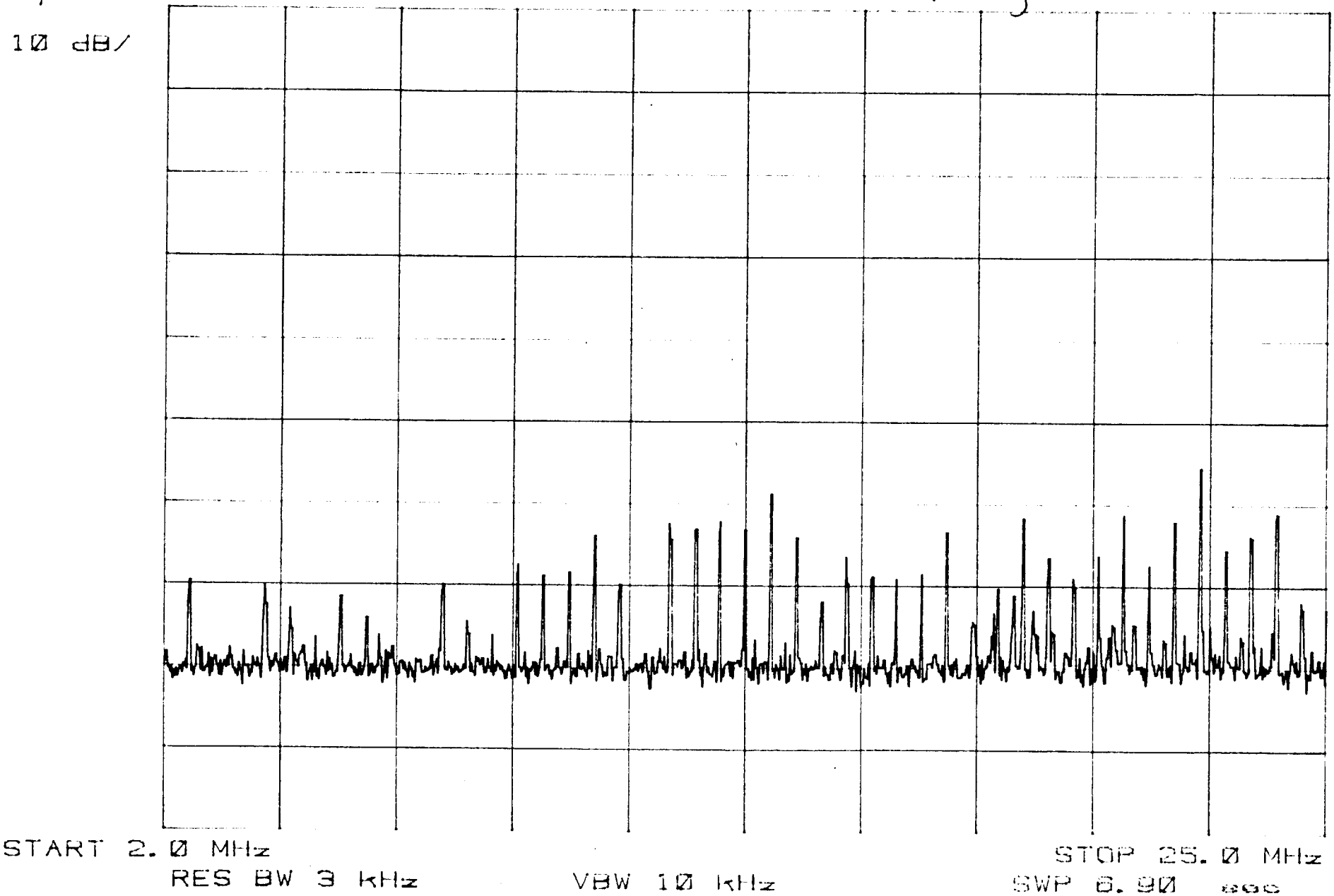
APW2 Baseline

RE02: APW 2 W/Battery. SN 001. Windows Display - lower left corner

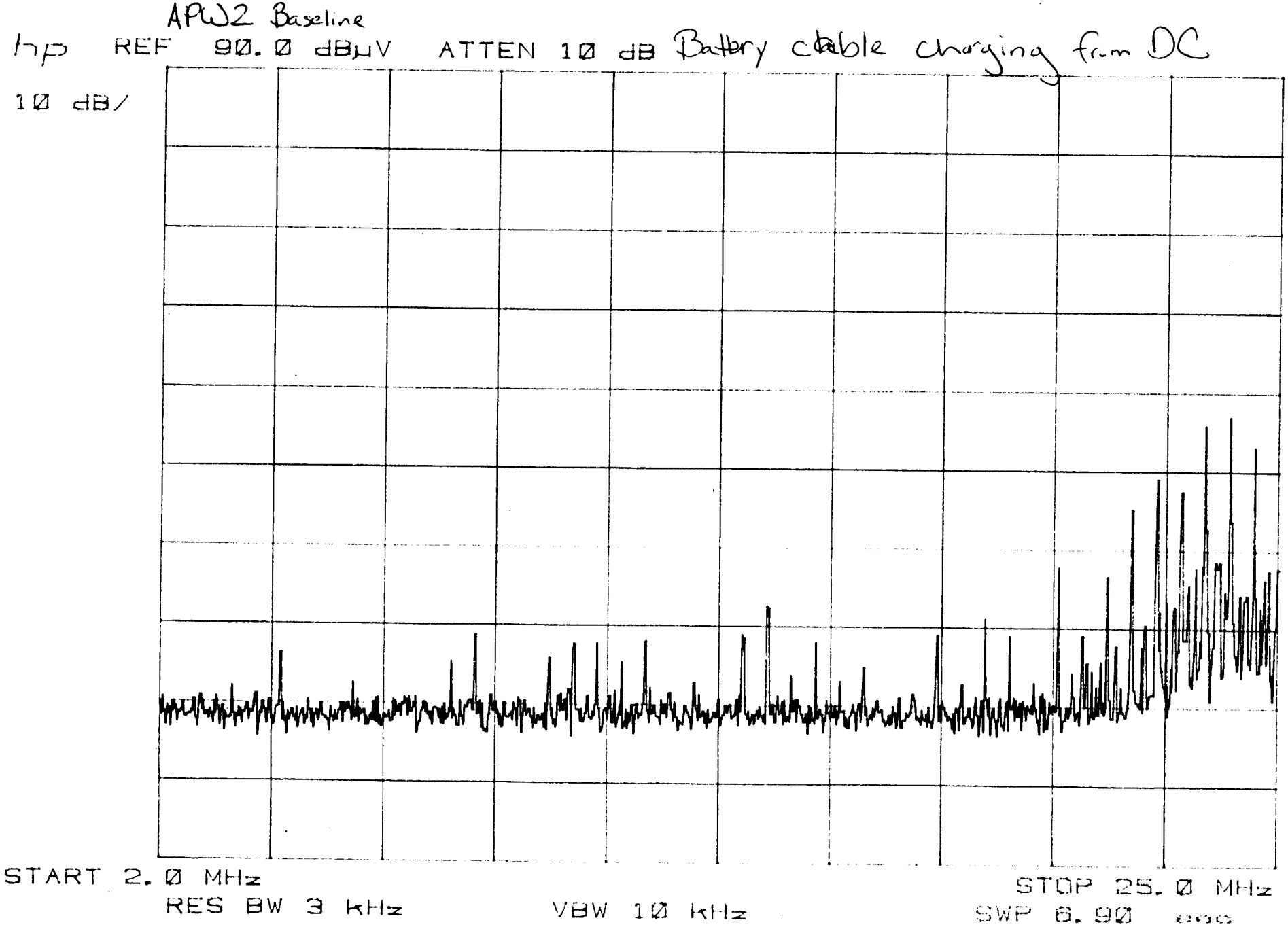


APW2 Baseline

Floppy 0.5K drive opening



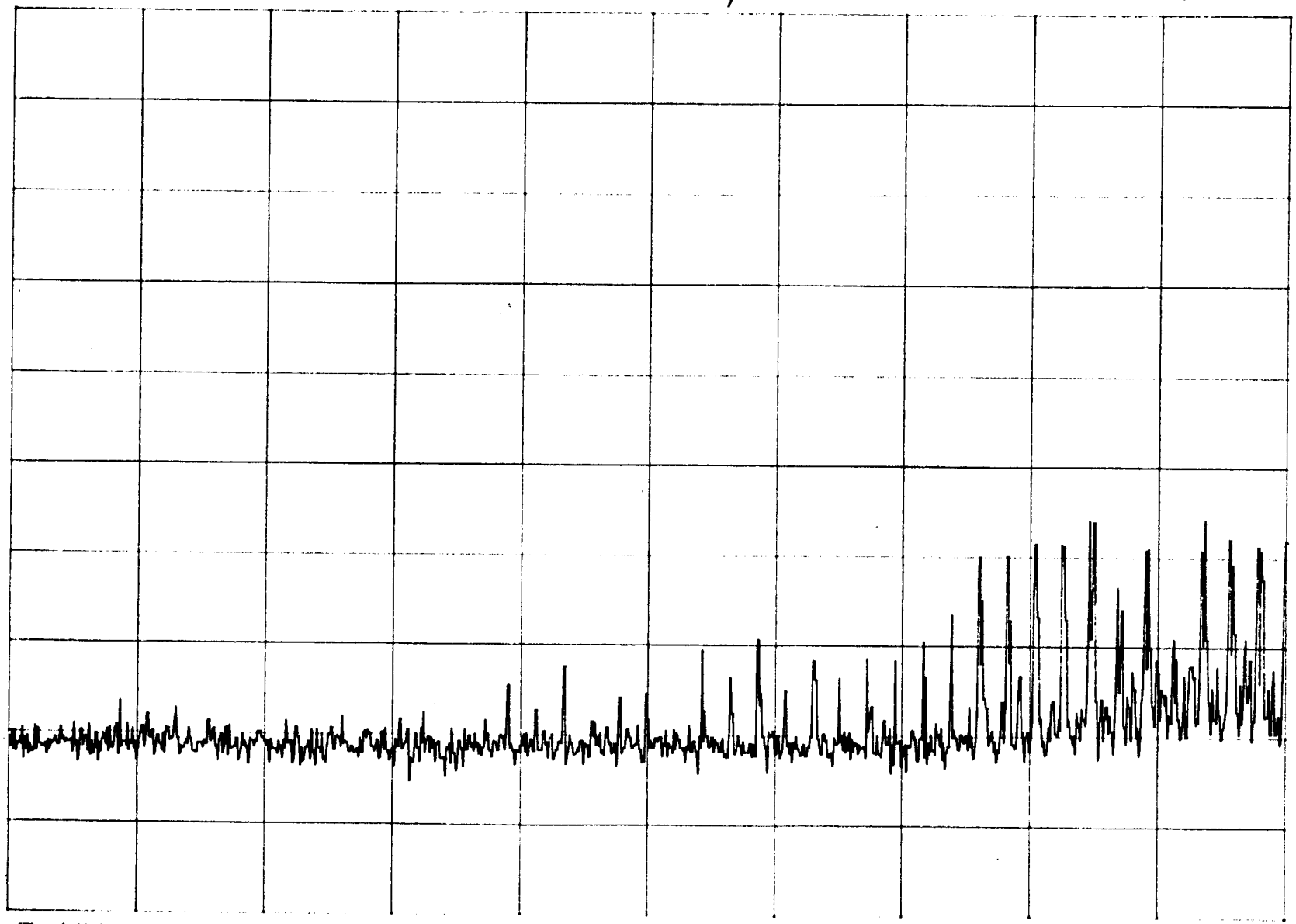
APW2 Baseline



APW2 Baseline

hp REF 90.0 dBµV ATTEN 10 dB Battery Cable powered from battery

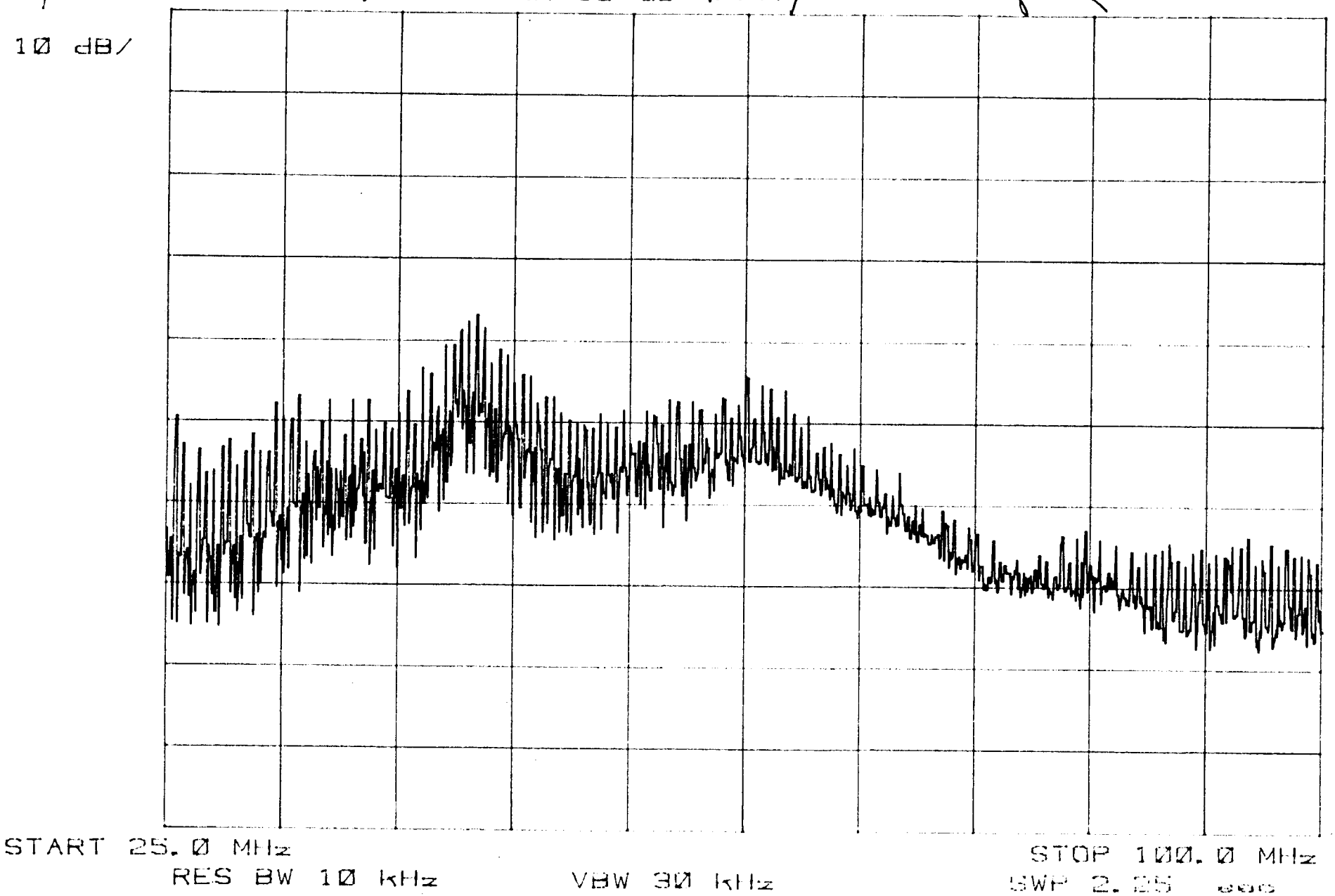
10 dB/



START 2.0 MHz STOP 25.0 MHz

RES BW 3 kHz VBW 10 kHz SWP 8.90

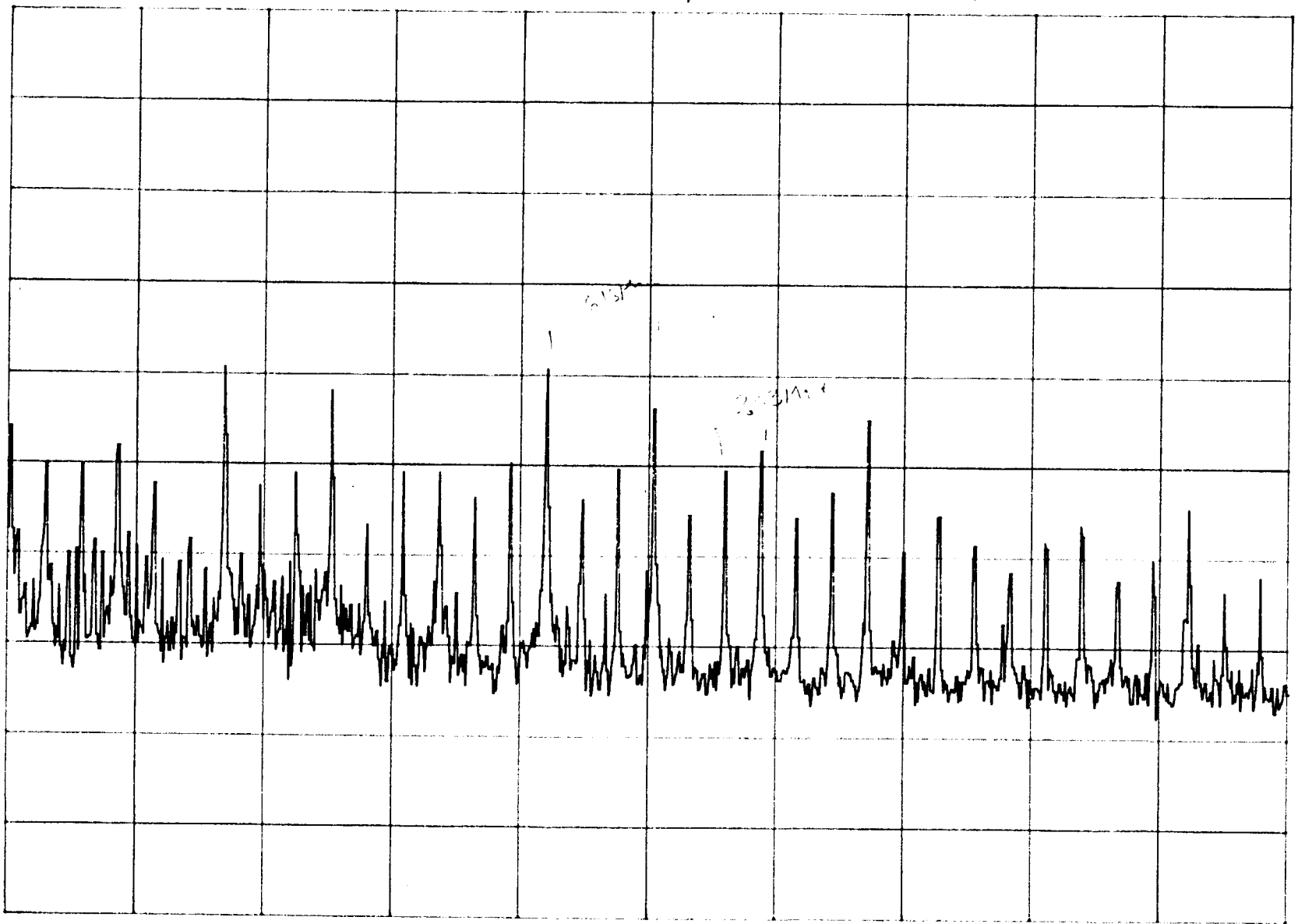
APW2 Baseline



APW2 Baseline

hp REF 90.0 dBµV ATTEN 10 dB Display lower left corner

10 dB/

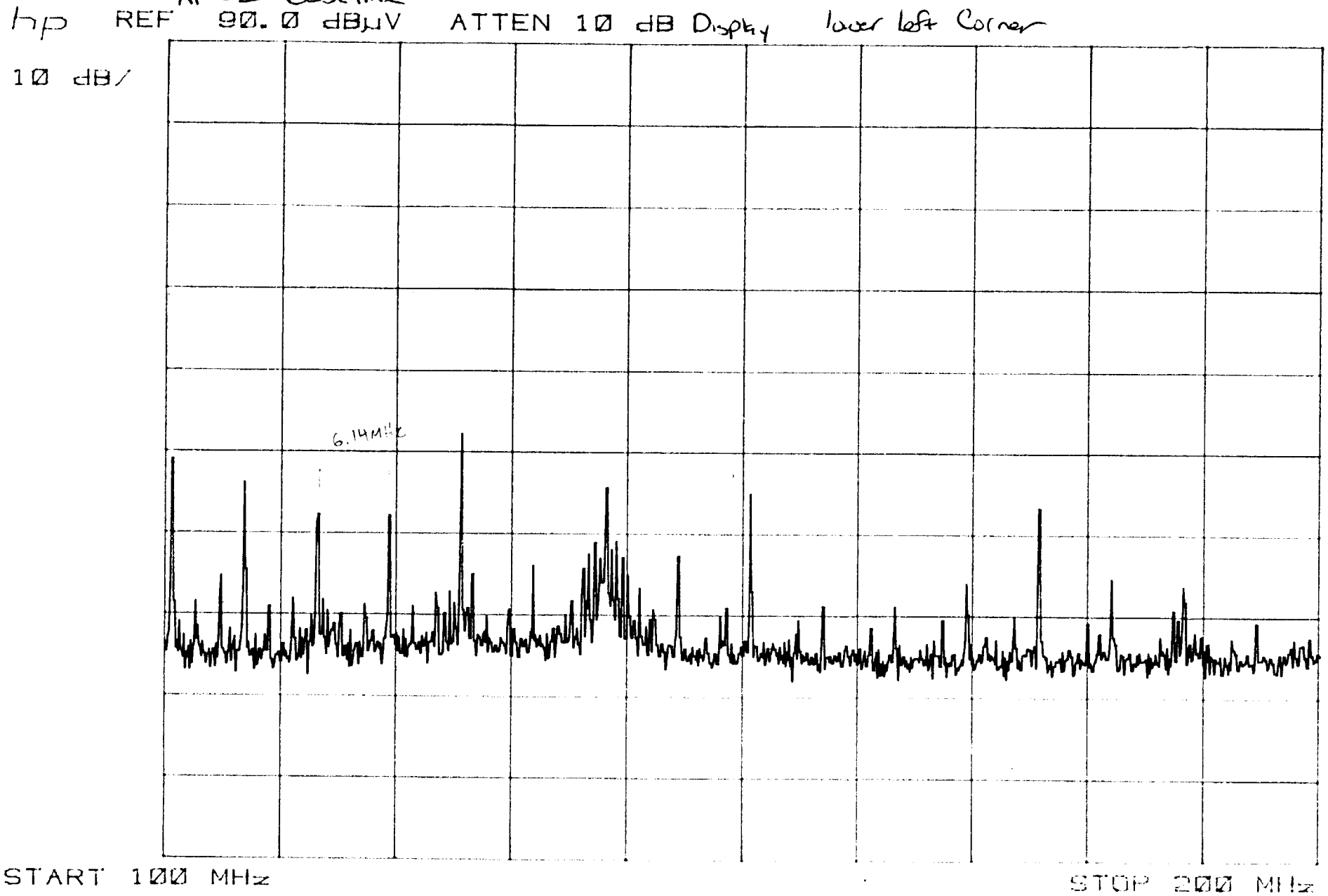


START 25.0 MHz

STOP 100.0 MHz

RES BW 10 kHz VBW 30 kHz SWP 2.25 sec

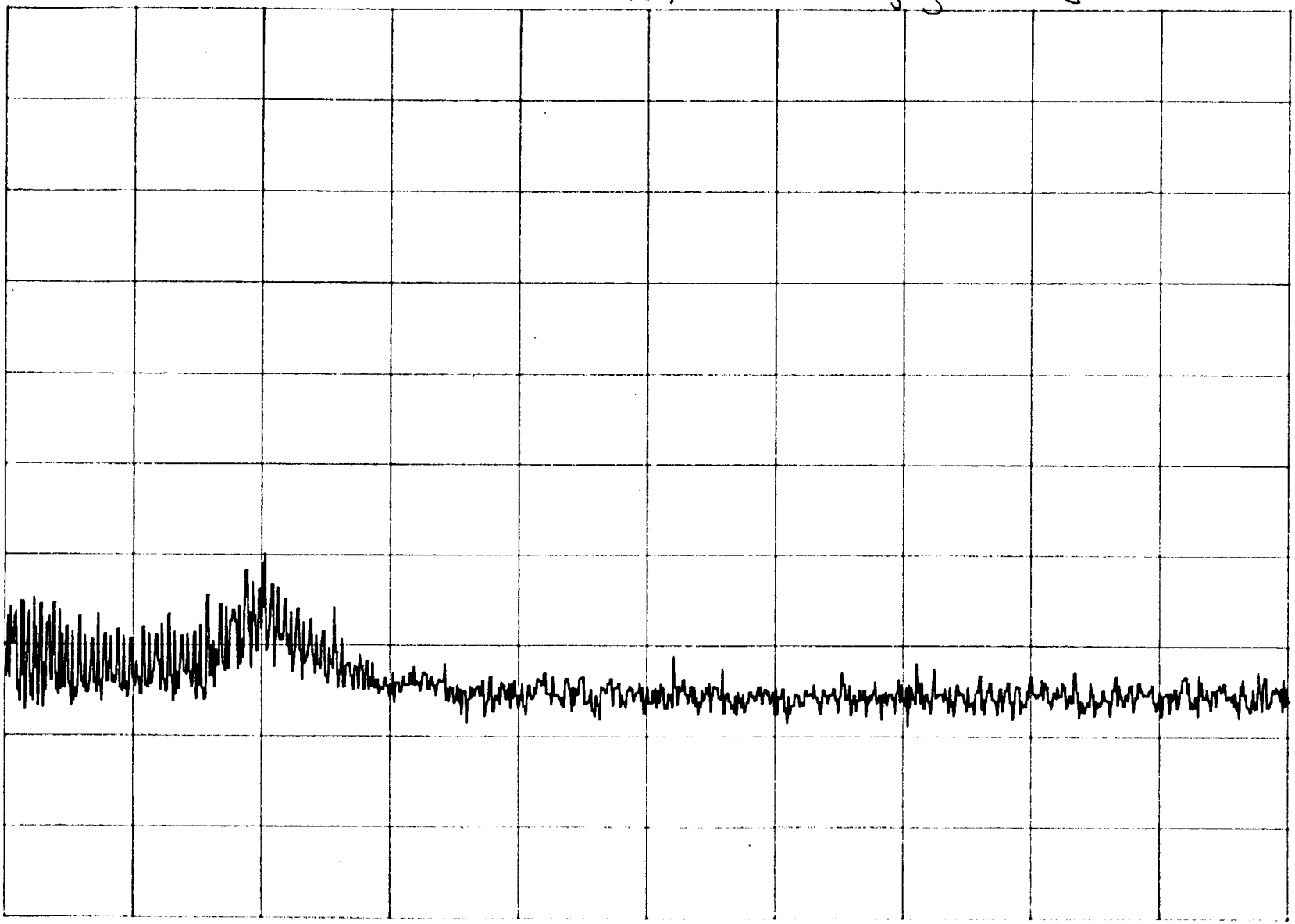
APW2 Baseline



APW2 Baseline

Hp REF 90.0 dBµV ATTEN 10 dB Battery Cable Changing from DC

10 dB/



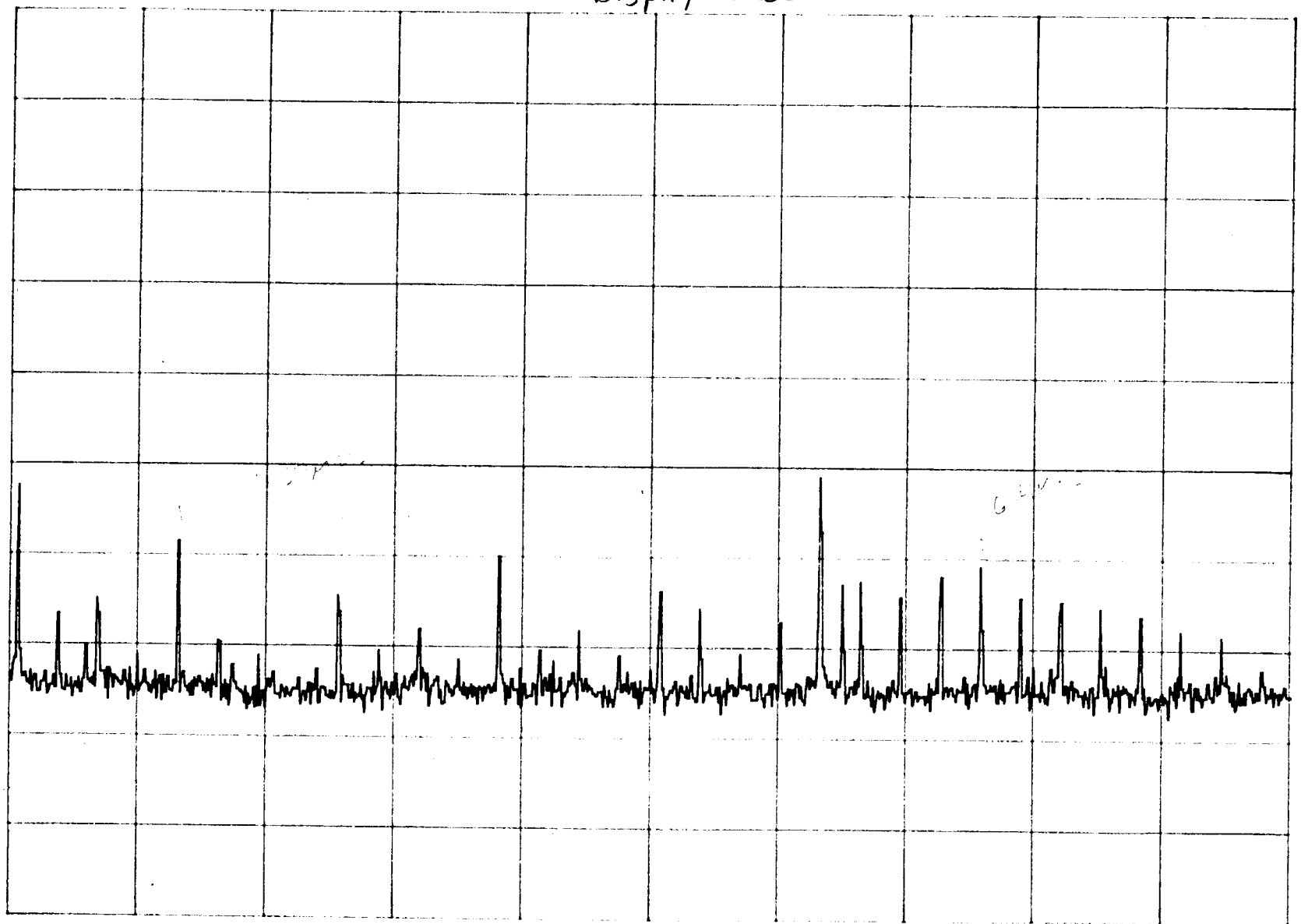
START 100 MHz STOP 200 MHz

RES BW 10 kHz VBW 30 kHz SWP 3.00 sec

APW2 Baseline

hp REF 90.0 dBµV ATTEN 10 dB Display lower left corner

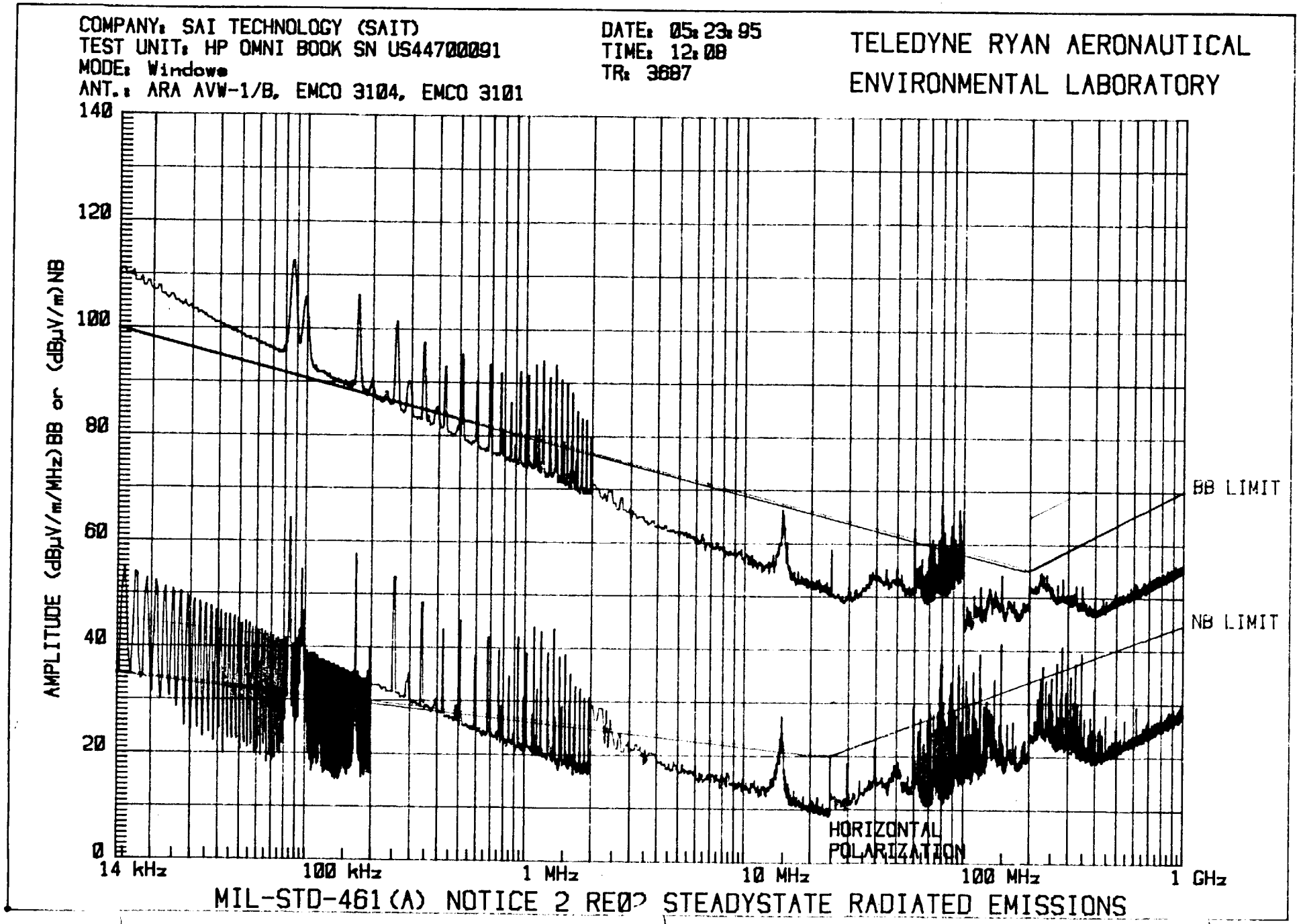
10 dB/



START 200 MHz

STOP 400 MHz

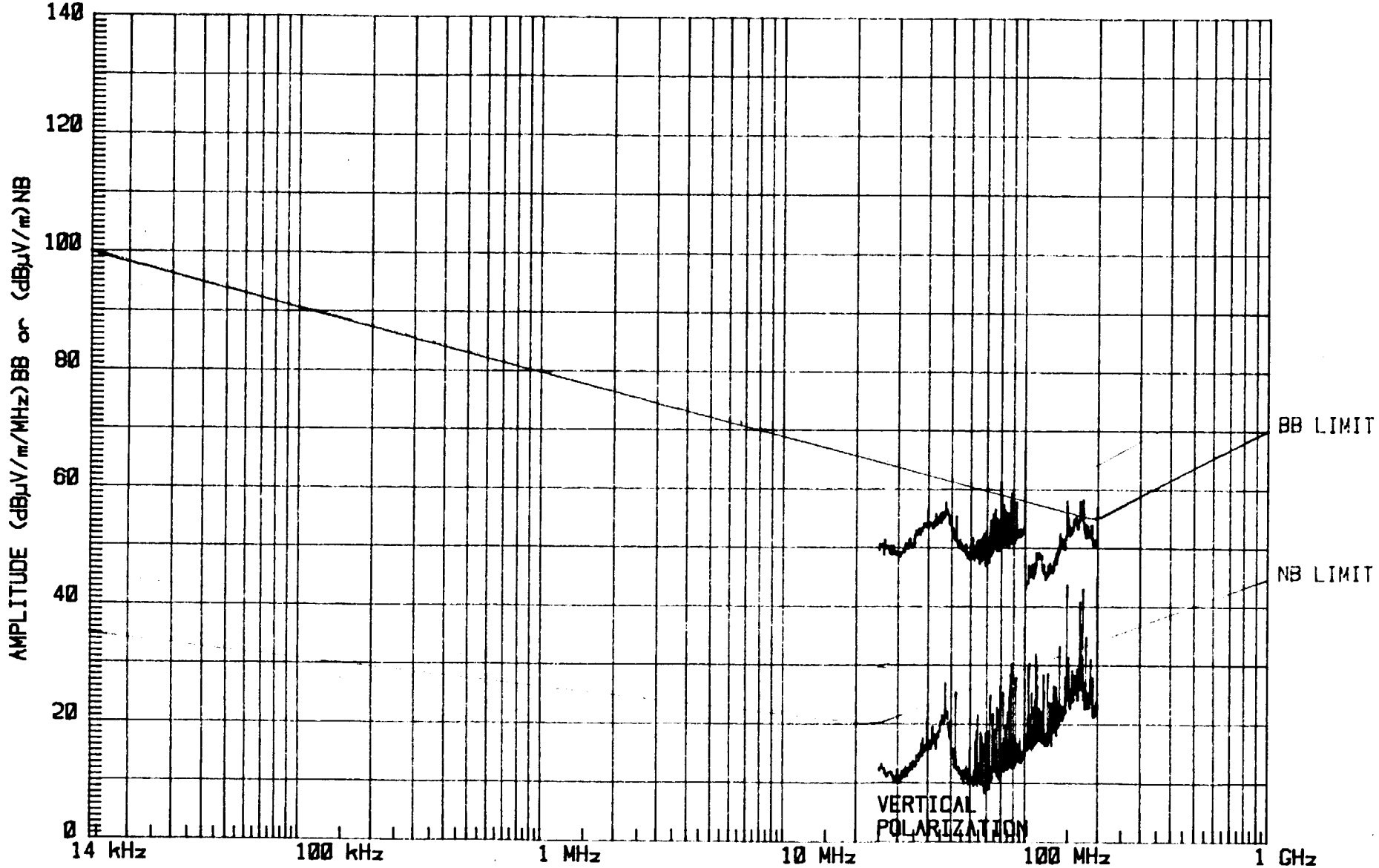
RES BW 10 kHz VBW 30 kHz SWP 6.00 sec


COMPANY: SAI TECHNOLOGY (SAIT)
TEST UNIT: HP OMNI BOOK SN US44700091
MODE: Windows
ANT.: ARA AVW-1/B, EMCO 3104, EMCO 3101
DATE: 05:23:95
TIME: 12:08
TR: 3687
TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY
AMPLITUDE (dBµV/m/MHz)BB or (dBµV/m)NB
140
120
100
80
60
40
20
0
14 kHz
100 kHz
1 MHz
10 MHz
100 MHz
1 GHz
BB LIMIT
NB LIMIT
HORIZONTAL
POLARIZATION
MIL-STD-461(A) NOTICE 2 REQ? STEADYSTATE RADIATED EMISSIONS

COMPANY: SAI TECHNOLOGY (SAIT)
TEST UNIT: HP OMNI BOOK SN US44700091
MODE: Windows
ANT.: EMCO 3104

DATE: 05:23:95
TIME: 12:08
TR: 3687

TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY

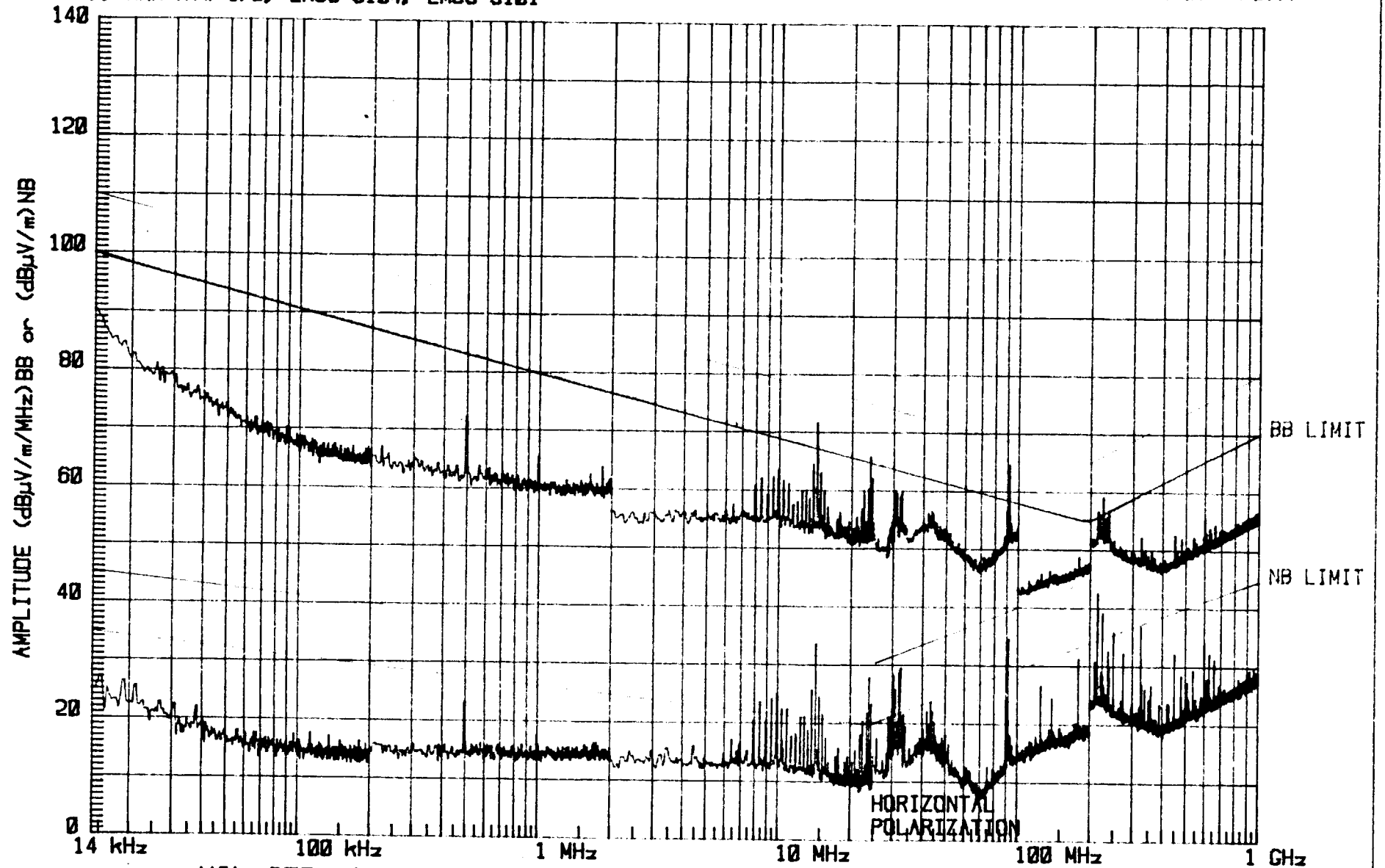


MIL-STD-461(A) NOTICE 2 RE02 STEADYSTATE RADIATED EMISSIONS

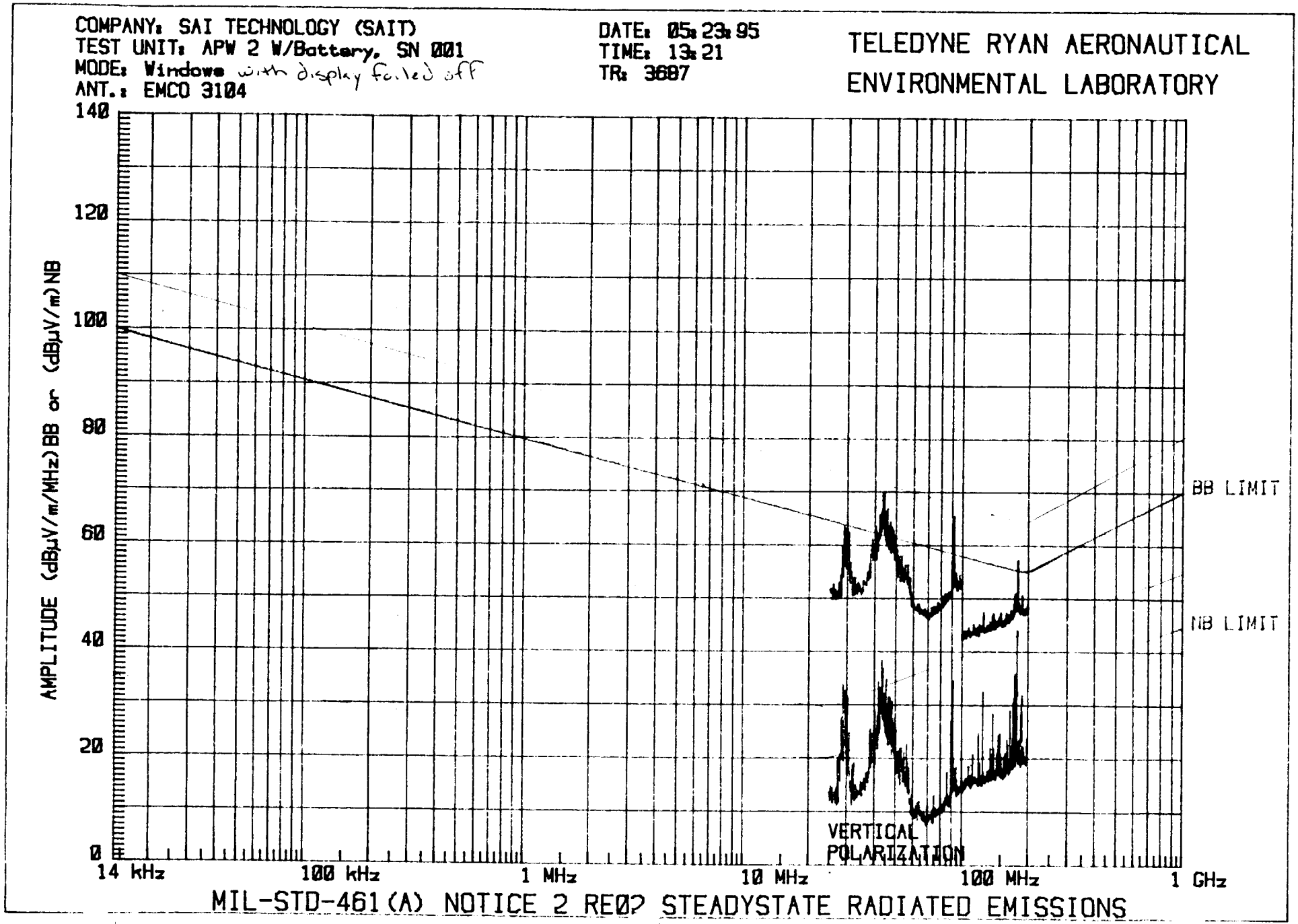
COMPANY: SAI TECHNOLOGY (SAIT)
TEST UNIT: APW 2 W/Battery, SN 001
MODE: Windows with display folded off
ANT.: ARA AVW-1/B, EMCO 3104, EMCO 3101

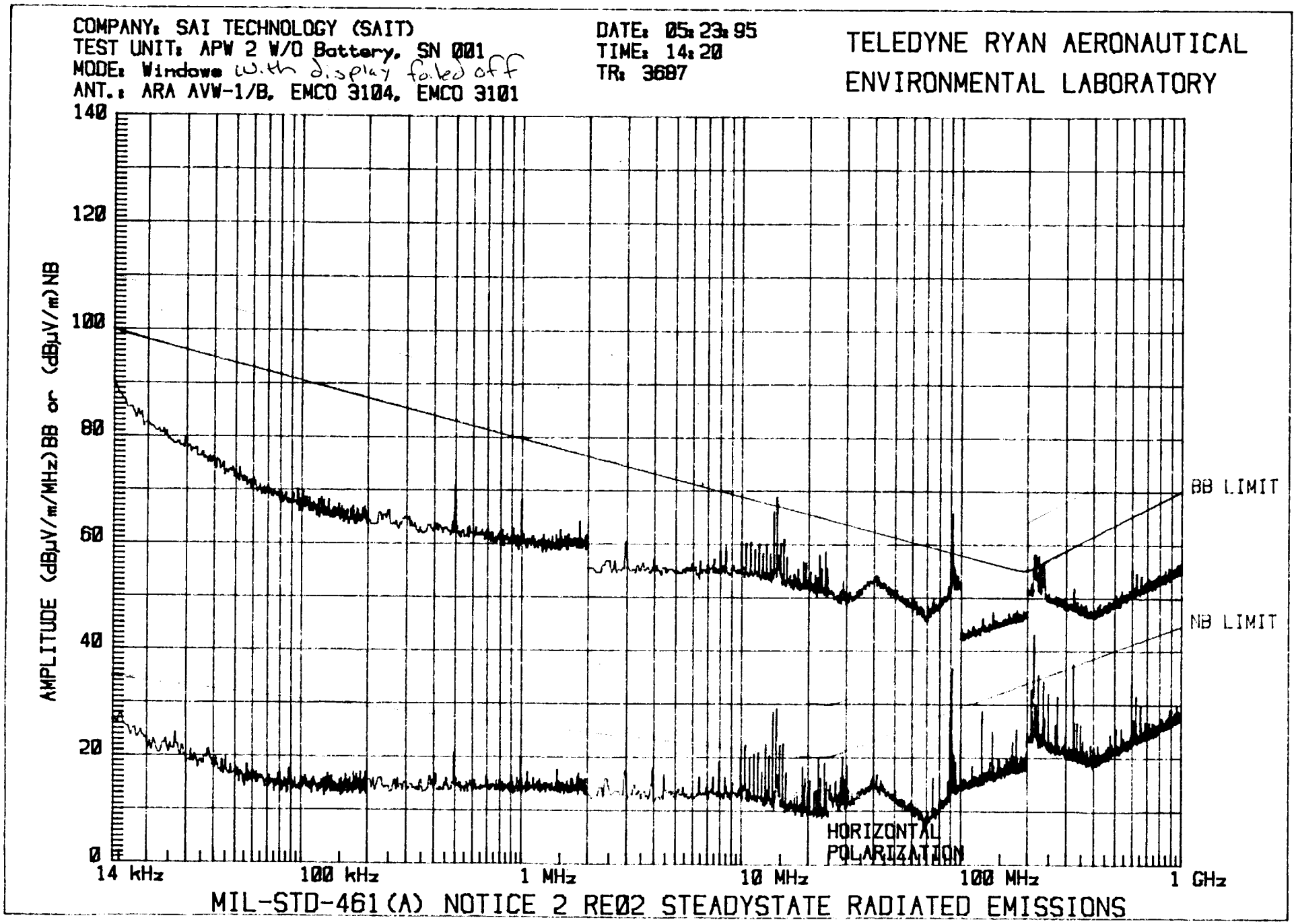
DATE: 05:23:95
TIME: 13:21
TR: 3687

TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY



MIL-STD-461(A) NOTICE 2 RE02 STEADYSTATE RADIATED EMISSIONS

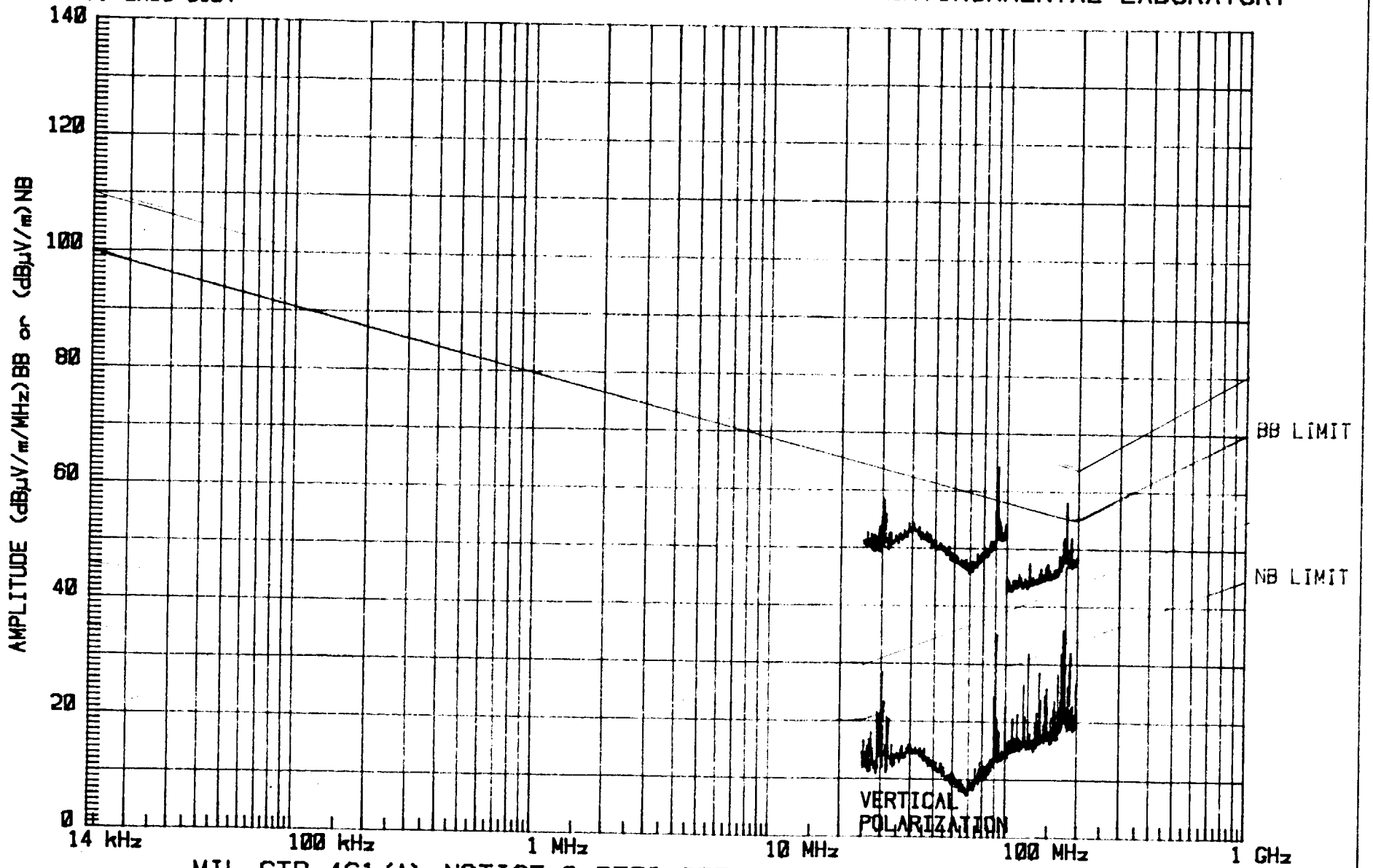

COMPANY: SAI TECHNOLOGY (SAIT)
TEST UNIT: APW 2 W/Battery, SN 001
MODE: Windows with display failed off
ANT.: EMCO 3104
DATE: 05:23:95
TIME: 13:21
TR: 3687
TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY
AMPLITUDE (dBµV/m/MHz)BB or (dBµV/m)NB
140
120
100
80
60
40
20
0
14 kHz
100 kHz
1 MHz
10 MHz
100 MHz
1 GHz
BB LIMIT
NB LIMIT
VERTICAL
POLARIZATION
MIL-STD-461(A) NOTICE 2 RE02 STEADYSTATE RADIATED EMISSIONS


COMPANY: SAI TECHNOLOGY (SAIT)
TEST UNIT: APW 2 W/O Battery, SN 001
MODE: Windowe with display faked off
ANT.: ARA AVW-1/B, EMCO 3104, EMCO 3101
DATE: 05:23:95
TIME: 14:20
TR: 3687
TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY
AMPLITUDE (dBµV/m/MHz)BB or (dBµV/m)NB
140
120
100
80
60
40
20
0
14 kHz
100 kHz
1 MHz
10 MHz
100 MHz
1 GHz
BB LIMIT
NB LIMIT
HORIZONTAL
POLARIZATION
MIL-STD-461(A) NOTICE 2 RE02 STEADYSTATE RADIATED EMISSIONS

COMPANY: SAI TECHNOLOGY (SAIT)
TEST UNIT: APW 2 W/O Battery, SN 001
MODE: Windowe
ANT.: EMCO 3104

DATE: 05:23:95
TIME: 14:20
TR: 3687

TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY



MIL-STD-461(A) NOTICE 2 RE02 STEADYSTATE RADIATED EMISSIONS

5/26/95

8:51

REØ2 on APW2 w/battery charging
running on 28VDC
4G1 (A)

Range 100-200MHz spikes every 5-6MHz } 5.7
25-100MHz spikes every 5.6MHz }

Running Windows with program manager closed.
Music tried Checkit & wanted to run
Memory tests but NO loop back board
& System had a strange anomaly - it would
reboot occasionally while running Memory test

Plotted @ 9:35
NASA Payload Equipment Specs placed
on chart in pencil

NB	BB
45@14KHz	110@14KHz
30@25MHz	65@200MHz
55@1GHz	80@1GHz

Noticeable Problems between 2-25MHz
25-100MHz &
100-400MHz

Sniffer scans were used
to find problems

2-25MHz
Display had a problem
Disk drive opening
Battery cable

1 to 2 order of magnitude

25-100MHz
Battery Cable
Display

100-200MHz
Display
Battery Cable

200-400MHz
Display

5/26/95

11:15

HP Omnibook Scan RE02
AC adapter was removed from chamber but unit was operating on its DC Voltage. Battery was in unit. Power was plugged in as well as the floppy drive

Done Printout @ 12:05

12:20

Sniffing to find out display problem
New foil - didn't help
28B choke on ECL disp input - didn't help
28B choke on TTL to disp - didn't help

Problem thought to be with disp electronics on left side of display.

Front of display sealed w/AL foil to see if the other unit leaks are of significance.

12:45 RE02
Same setup as before except disp opening was foiled off
This test was run to see the effects of the other leaks

Printout @ 13:21

Spike peaks pin out printed
14.466 or 14.512 MHz is the only horizontal non compliant signal

29.2 & 29.65, 43.75, 47.2, 44.35, 180 & 190.2 are failures' — Vertical band

5/26/95

1:37 REQ2 APW2

Scan w/foil & w/o bottom

plot @ 14:20

Scan AC supply in Chamber.
Print pic in control room w/VGA
cable routed to EMI chamber

Print time 1504

TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY

ENVIRONMENTAL TEST DATA SHEET

TEST UNIT SAIT APW 2 Computer T.R. NO. 3687 DATE 5/26/95

TEST REO2 Investigation TEST SPEC. _____ PARA. _____

AMBIENT CONDITIONS: TEMP. _____ °F, HUMIDITY _____ %, PRESSURE _____ IN. HG.

SIGN OFF: TECHNICIAN _____, SUPERVISOR Everett, QC _____

— 1. TEST DATA 2. INSTRUMENT LIST —

DATE	TIME	
5/26/95	0800	Customer arrived with Several test units. We will be doing RE02 work. Setting up in Enclosure.
	0850	Photo taken & Ready to Start 1st RE02 scan 14K to 1GHz Standard Setup 10 ft cable + 2 meters of coax NOT twisted 5 cm off GND plane. Note to pl of computer screen.
	0851	Started 1st RE02 Scan on APW 2 SN001, 14K - 1GHz
	0945	Completed 1st RE02 Scan. Customer wants to use sniffer to check areas of leakage. Setups remote display in the shielded enclosure
	1000	Completed plot from 2m - 25MHz monitor lower left corner of display screen.
	1031	Completed 2nd sniffer plot - disk drive open 2-25MHz
	1035	Completed 3rd sniffer plot - Battery cable while running of the battery. 2-25MHz
	1040	Completed 4th sniffer plot - Same as 3 but on internal power. 2-25MHz
	1045	5th Sniffer plot 25MHz - 100MHz Display screen.
	1051	6th Sniffer plot 25-100MHz PWR Cord / Battery
	1055	7th sniffer plot 100-200 MHz Display

TELEDYNE RYAN AERONAUTICAL
ENVIRONMENTAL LABORATORY

ENVIRONMENTAL TEST DATA SHEET

TEST UNIT SAIT APW 2 + HP OMNI BOOK Computer T.R. NO. 3687 DATE 5/26/05

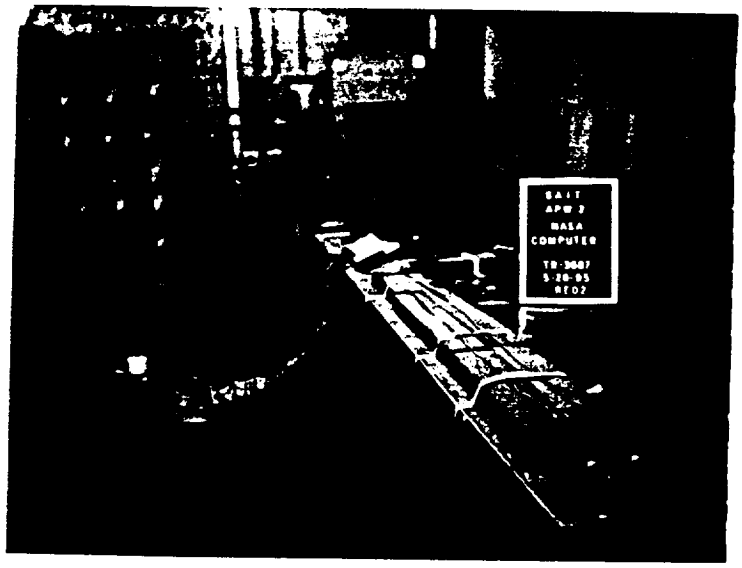
TEST RF02 Investigation TEST SPEC. ______ PARA. ______

AMBIENT CONDITIONS: TEMP. ______ °F, HUMIDITY ______ %, PRESSURE ______ IN. HG

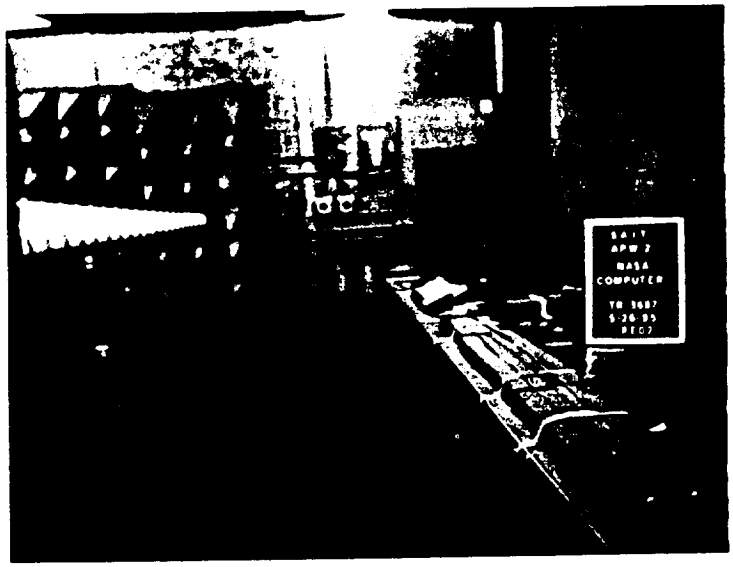
SIGN OFF: TECHNICIAN ______, SUPERVISOR Everett, QC ______

— 1. TEST DATA 2. INSTRUMENT LIST —

DATE	TIME	
5/26/05	1059	8th sniffer plot, 100-200 MHz - PW cable/Battery
	1105	9th sniffer plot 200-400 MHz - Display
	1110	Completed testing APW2, we are switching
		to the HP OMNI BOOK computer.
	1124	Started RF02 scan on HP-OMNI.
	1146	Scan completed, plotting results. We will
		work through lunch since I have an eye
		appointment & must depart at 2 pm today.
	1200	Plotting completed. Will start sniffing
		the APW 2. Customer made some changes to it
	1243	Customer shielded display with Al foil (APW 2
	1244	Started RF02 full scan, APW 2 w/ Al foil
	1300	Scan completed, plotting results.
	1325	Plots completed, printing summary report
	1335	Report completed
	1337	Started RF02 sweep of APW 2 Al w/o Battery.
	1356	Scan completed plotting results.

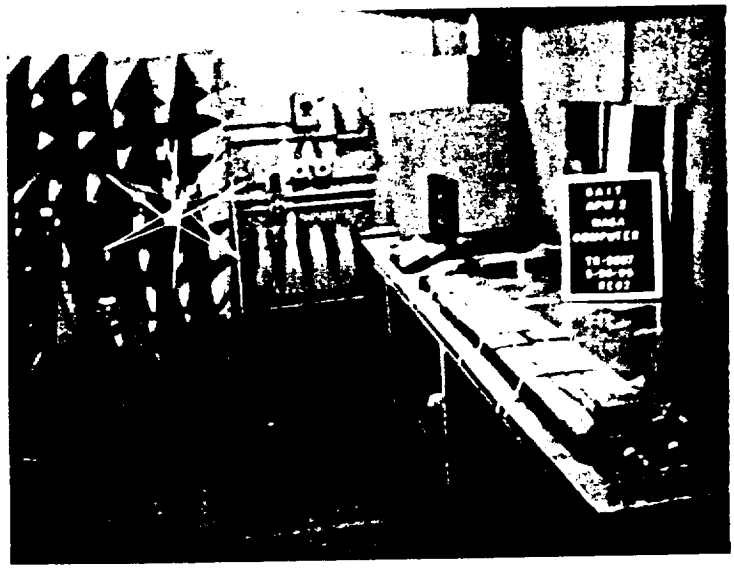


14KHz - 25MHz

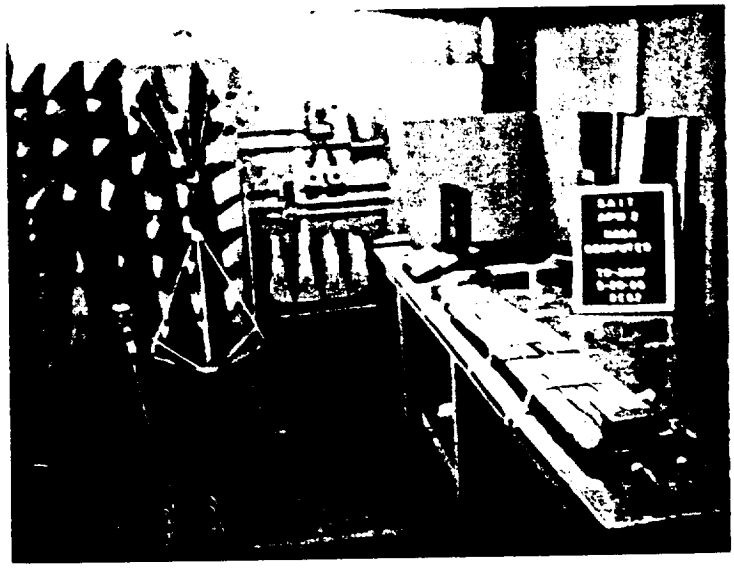


200MHz - 1GHz

UUT EMI REØ2 CONFIG.



25MHz - 100MHz
Horizontal



25MHz - 100MHz
Vertical

UUT EMI REØ2 CONFIG.

14kHz - 25MHz

HP OMNIBOOK RE02 CONFIG

APPENDIX 6

POWER SUPPLY TEST RESULTS

POWER TESTS - WNE

TEST DATE: 6/1/95
TEST OPERATOR: TIM GIORGETTA
UNIT UNDER TEST (UUT) : APW II WITH PROXIM WIRELESS, BATTERY MODULE, DISPLAY MODULE, AND KEYBOARD MODULE.

POWER CONSUMPTION IN WORKING MODE

PURPOSE: To determine the working mode power consumption for the three operating voltages: 23 VDC, 28 VDC, and 32 VDC.

TEST EQUIPMENT:

UUT:
- Serial Number: 001

FLUKE Multimeter:
- Model Number: 87
- Serial Number: 5444058

Hewlett-Packard Power Supply:
- Model Number: 6274B
- Serial Number: 3222A-11185

TEST DESCRIPTION:

Test configuration per attachment 1. Current measured on primary low side. Voltage measured at UUT. Power calculated from voltage and current readings.

RESULTS:

V = 23.00 VDC
I = 2.40 ADC
P = (23.00V * 2.40A) = 55.20 W

V = 28.00 VDC
I = 1.97 ADC
P = (28.00V * 1.97A) = 55.16 W

V = 32.00 VDC
I = 1.72 ADC
P = (32.00V * 1.72A) = 55.04 W

STARTUP CURRENT - AMPLITUDE AND DURATION

PURPOSE: To determine the startup currents maximum amplitude and pulse width for the three operating voltages: 23 VDC, 28 VDC, and 32 VDC.

TEST EQUIPMENT:

UUT:
- Serial Number: 001

FLUKE Multimeter:
- Model Number: 87
- Serial Number: 54440548

Hewlett-Packard Power Supply:
- Model Number: 6274B
- Serial Number: 3222A-11185

Tektronix Current Probe:
- Model Number: TM501A
- Serial Number: B012595

TEKTRONIX Oscilloscope:
- Model Number: TDS 540
- Serial Number: B024348

TEST DESCRIPTION:

Test configuration per attachment 2. Current is measured from primary low side with current probe. Voltage measured at UUT input.

RESULTS: SEE ATTACHMENTS 5-10 FOR PLOTS

V = 23.00 VDC

I_{PEAK} = 13.36 ADC
= (53.20mV) * (1DIV/10mV) * (5A/DIV)

$t_{DURATION}$ = 289 us

V = 28.00 VDC

I_{PEAK} = 23.10 ADC
= (46.20mV) * (1DIV/10mV) * (5A/DIV)

$t_{DURATION}$ = 297 us

V = 32.00 VDC

I_{PEAK} = 26.60 ADC
= (66.80mV) * (1DIV/10mV) * (2A/DIV)

$t_{DURATION}$ = 281 us

ELECTRICAL INSULATION STRENGTH TEST

PURPOSE: To determine the insulation strength between primary high side and chassis ground and also between primary low side and chassis ground.

TEST EQUIPMENT:

UUT:

Serial Number: 001

FLUKE Multimeter:

Model Number: 87

Serial Number: 54440548

TEST DESCRIPTION:

Test configuration per attachment 3. Primary high side measured with DMM_+ to V_A and DMM_{COM} to V_C (chassis GND). Primary low side measured with DMM_{COM} to V_B and DMM_+ to V_C (chassis GND).

RESULTS:

V_A TO V_C > 20 MOHM

V_B TO V_C > 20 MOHM

ELECTRICAL INSULATION RESISTANCE AND BREAKDOWN TEST

PURPOSE: To determine the amount of leakage current when +100 VDC and -100 VDC are applied between the primary high side and chassis ground and between the primary low side and chassis ground.

TEST EQUIPMENT:

UUT:
- Serial Number: 001

FLUKE Multimeter:
- Model Number: 87
- Serial Number: 54440548

Hewlett-Packard Power Supply:
- Model Number: 6274B
- Serial Number: 3222A-11185

Hewlett-Packard Power Supply:
- Model Number: 6274B
- Serial Number: 3035A-11015

TEST DESCRIPTION:

Test configuration per attachment 4. Apply +100 VDC between V_A and V_C and also between V_B and V_C. Apply -100 VDC between V_A and V_C and also between V_B and V_C. Measure leakage current in all four cases.

RESULTS:

+100 VDC APPLIED

V_A TO V_C

$I_{LEAKAGE}$ = 0000mA

V_B TO V_C

$I_{LEAKAGE}$ = 0000mA

-100 VDC APPLIED

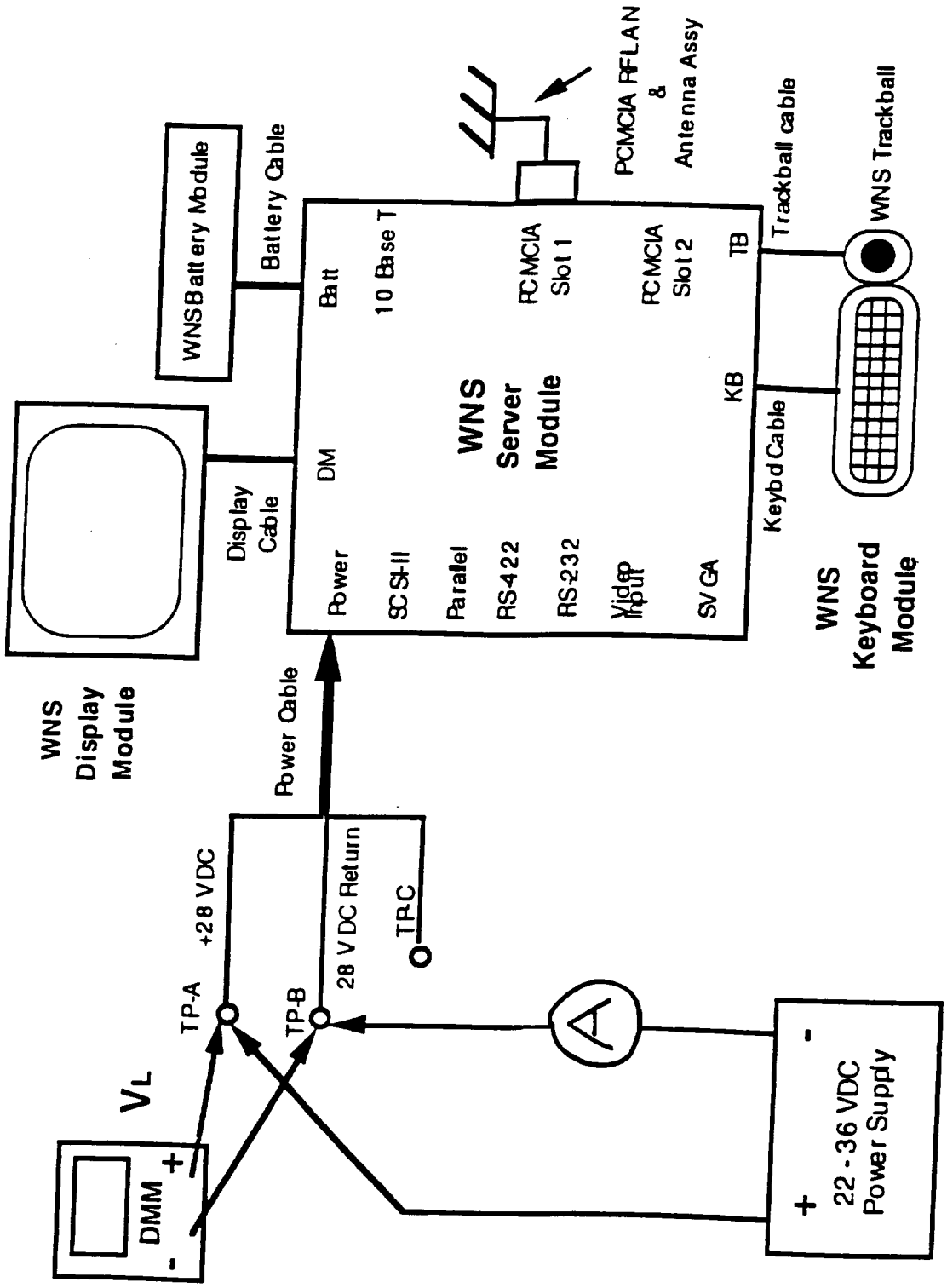
V_A TO V_C

$I_{LEAKAGE}$ = 0000mA

V_B TO V_C

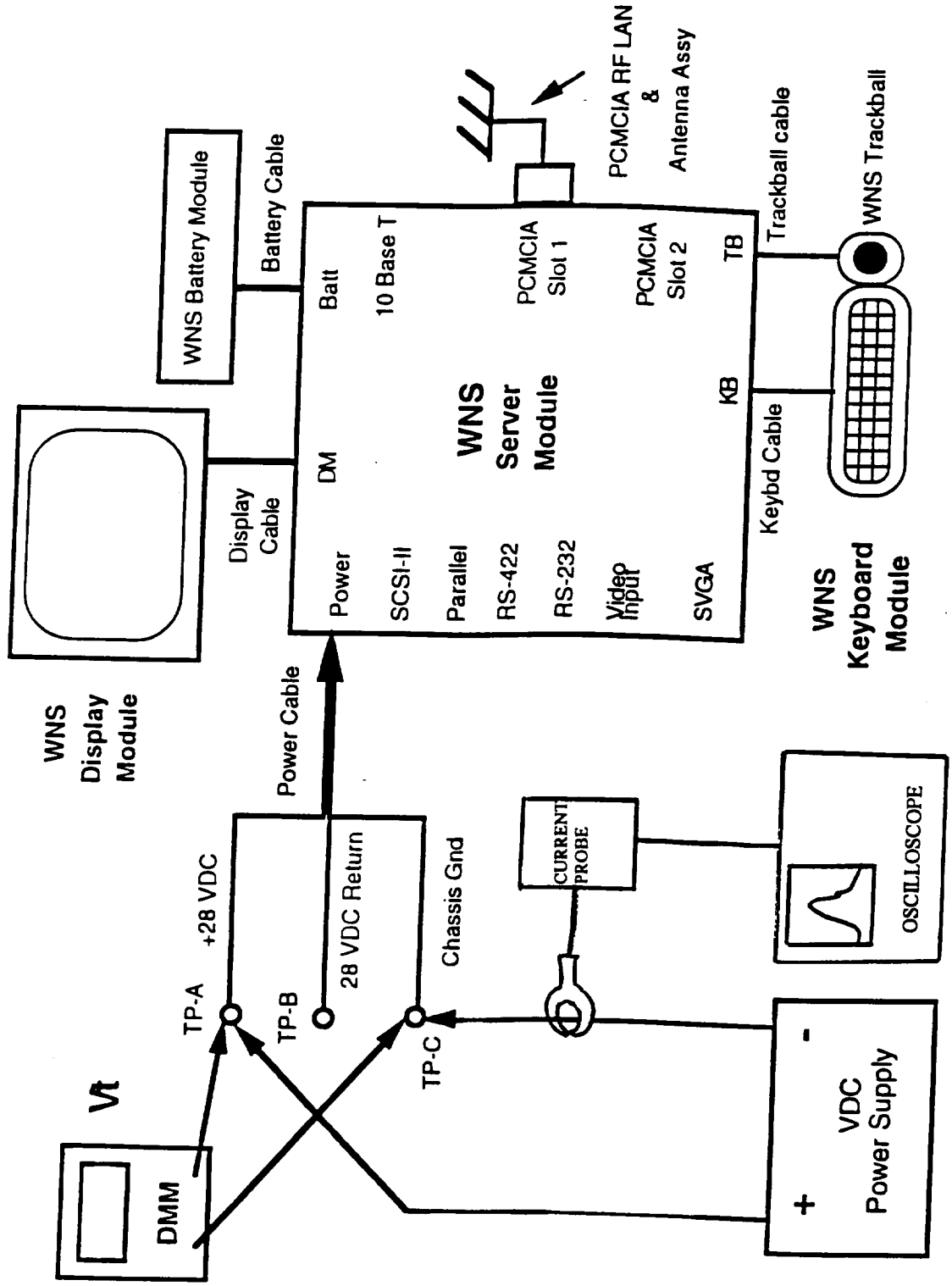
$I_{LEAKAGE}$ = 0000mA

ATTACHMENT 1



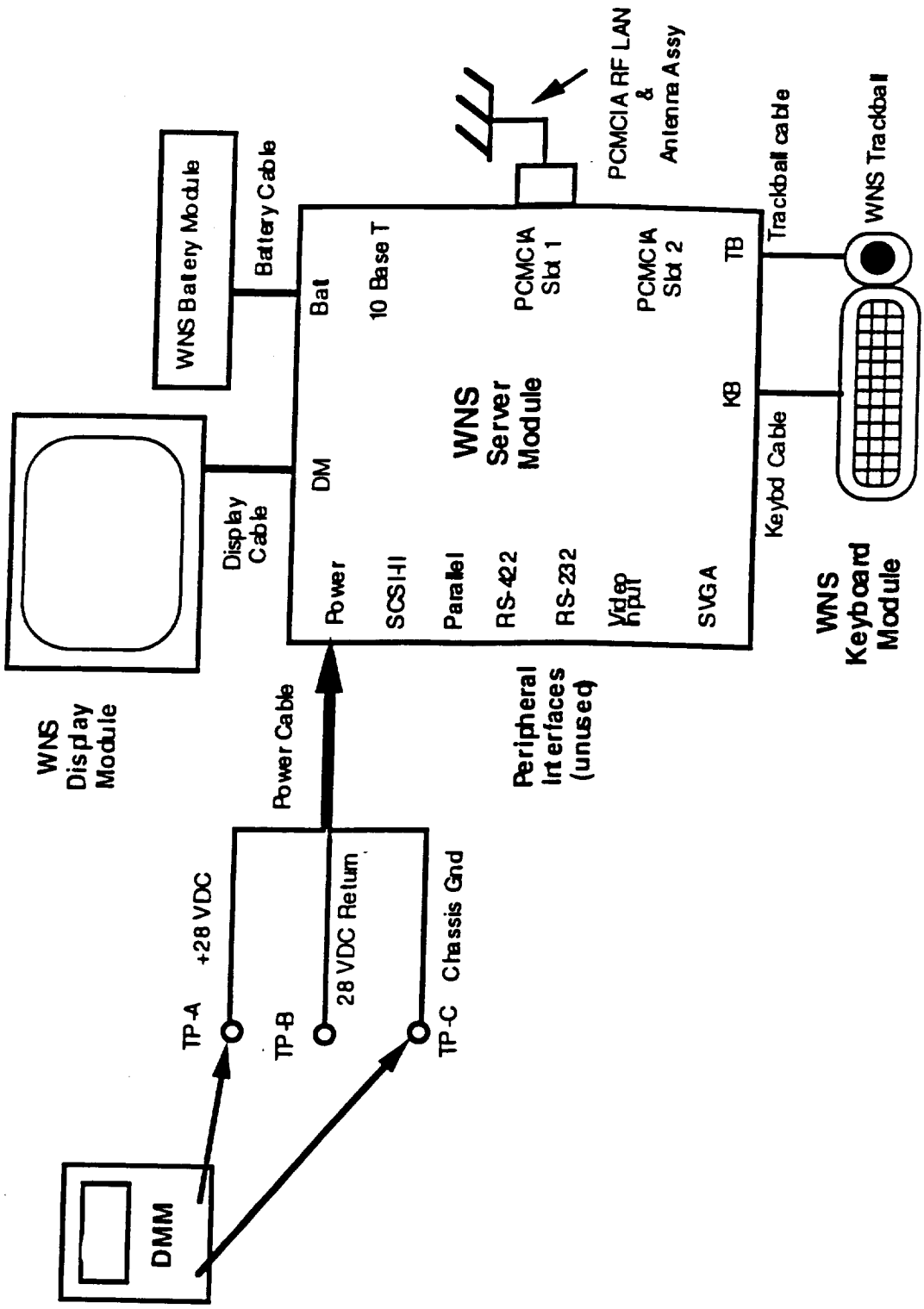
Electrical Power Test Configuration

ATTACHMENT 2



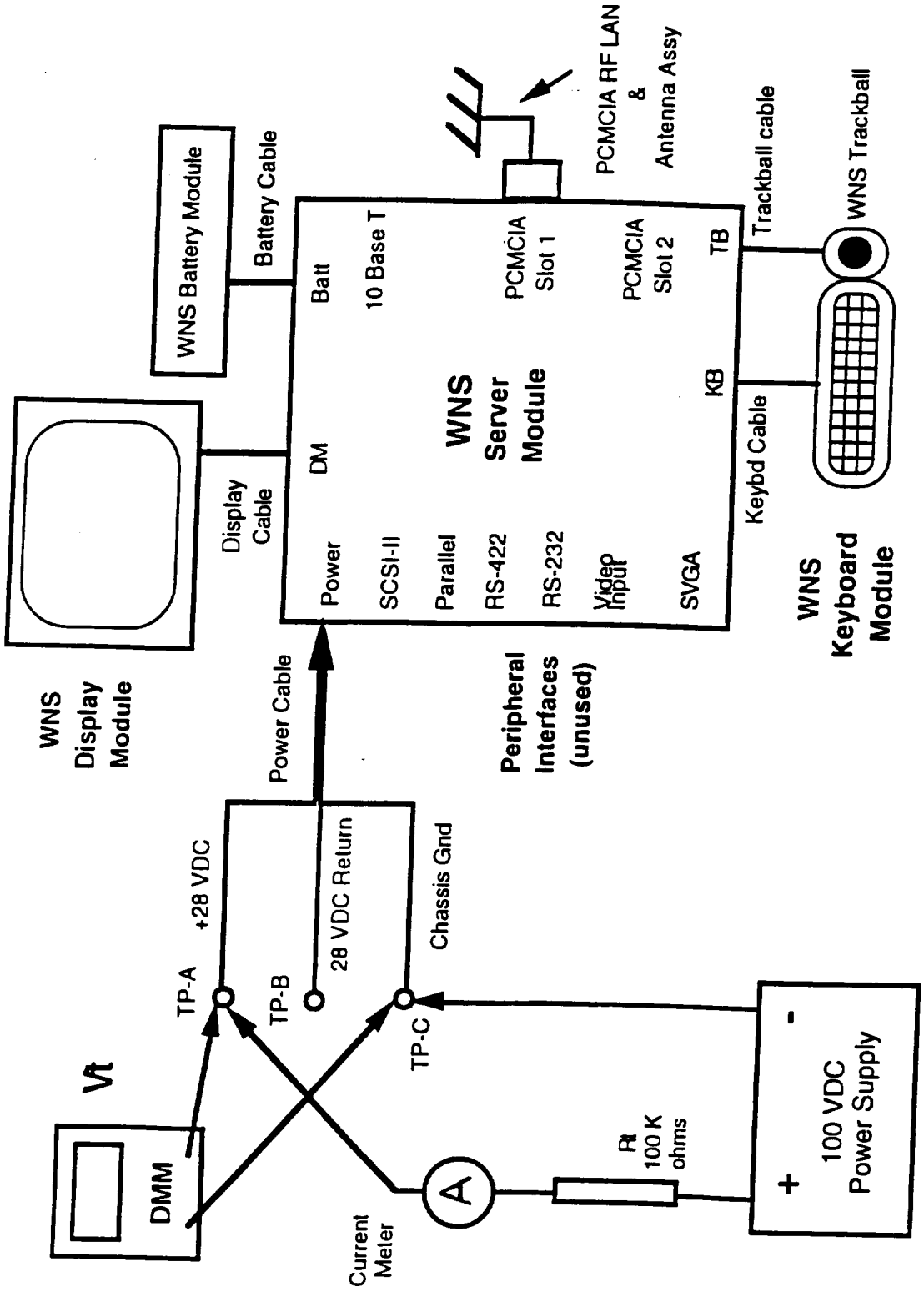
Startup Current Test Configuration

ATTACHMENT 3



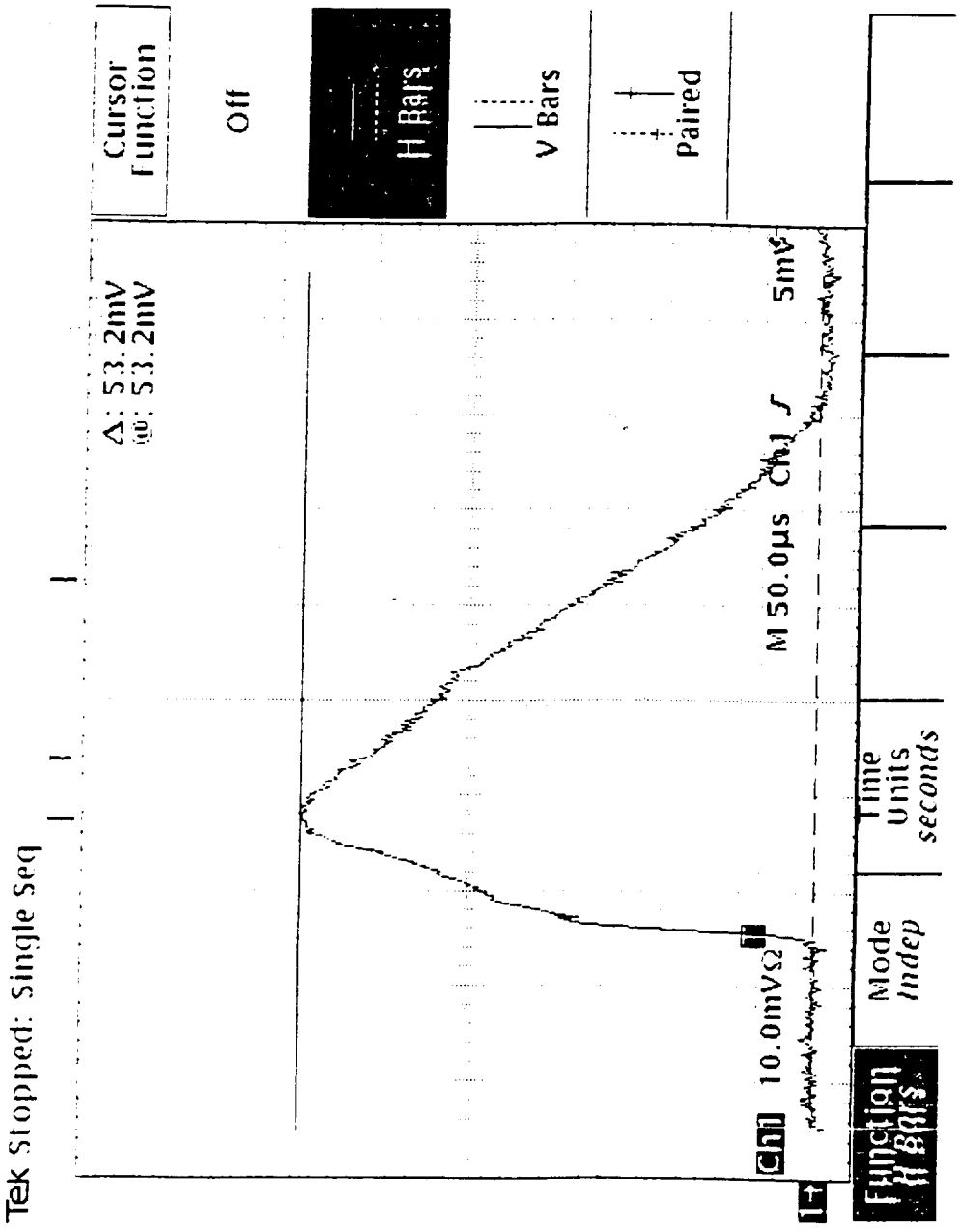
Electrical Isolation Test Configuration

ATTACHMENT 4



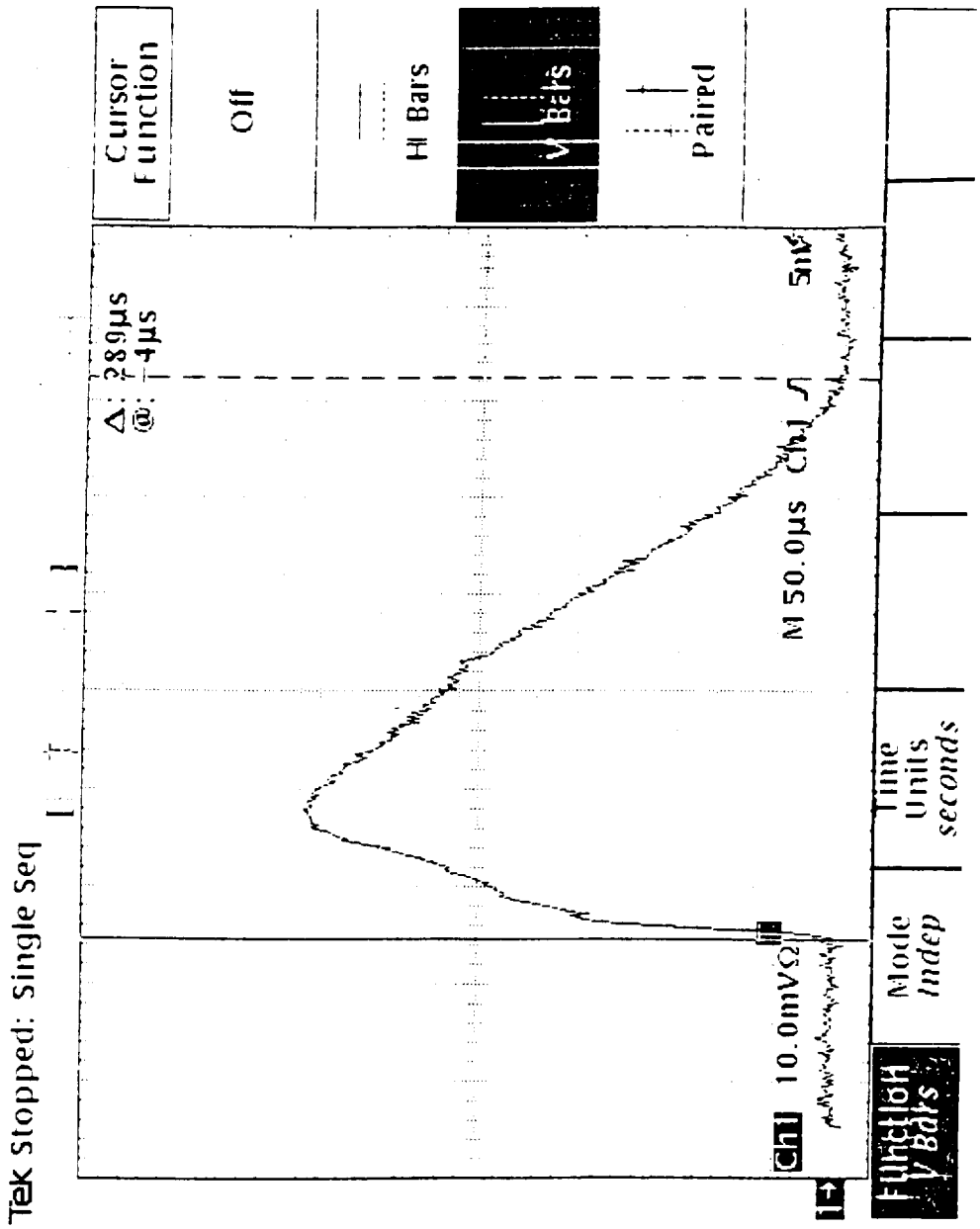
Electrical Breakdown Test Configuration

ATTACHMENT 5



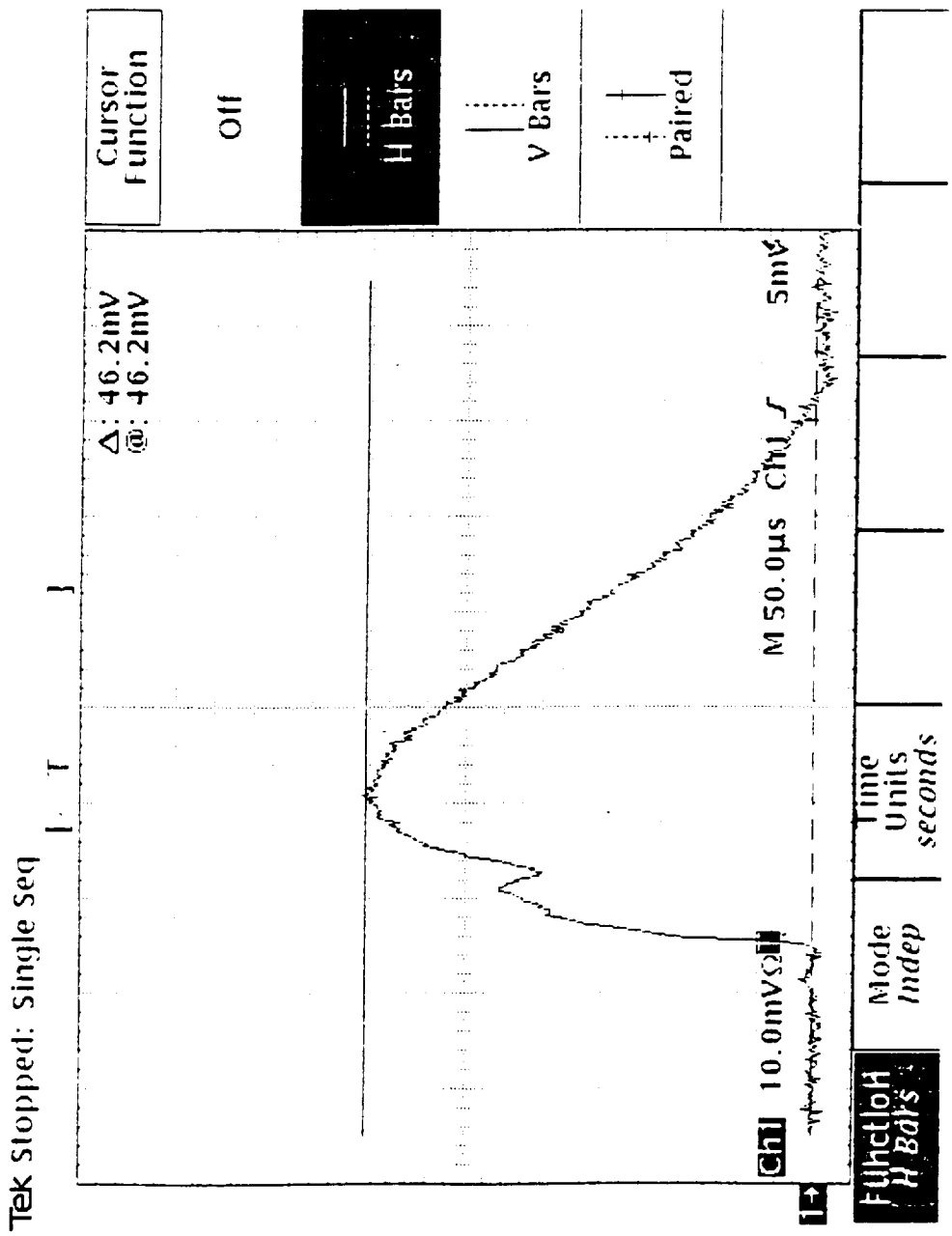
PEAK STARTUP CURRENT @ V=23.00VDC
PROBE SETTINGS: (5A/DIV) * (1DIV/10mV) = 0.5A/DIV

ATTACHMENT 6



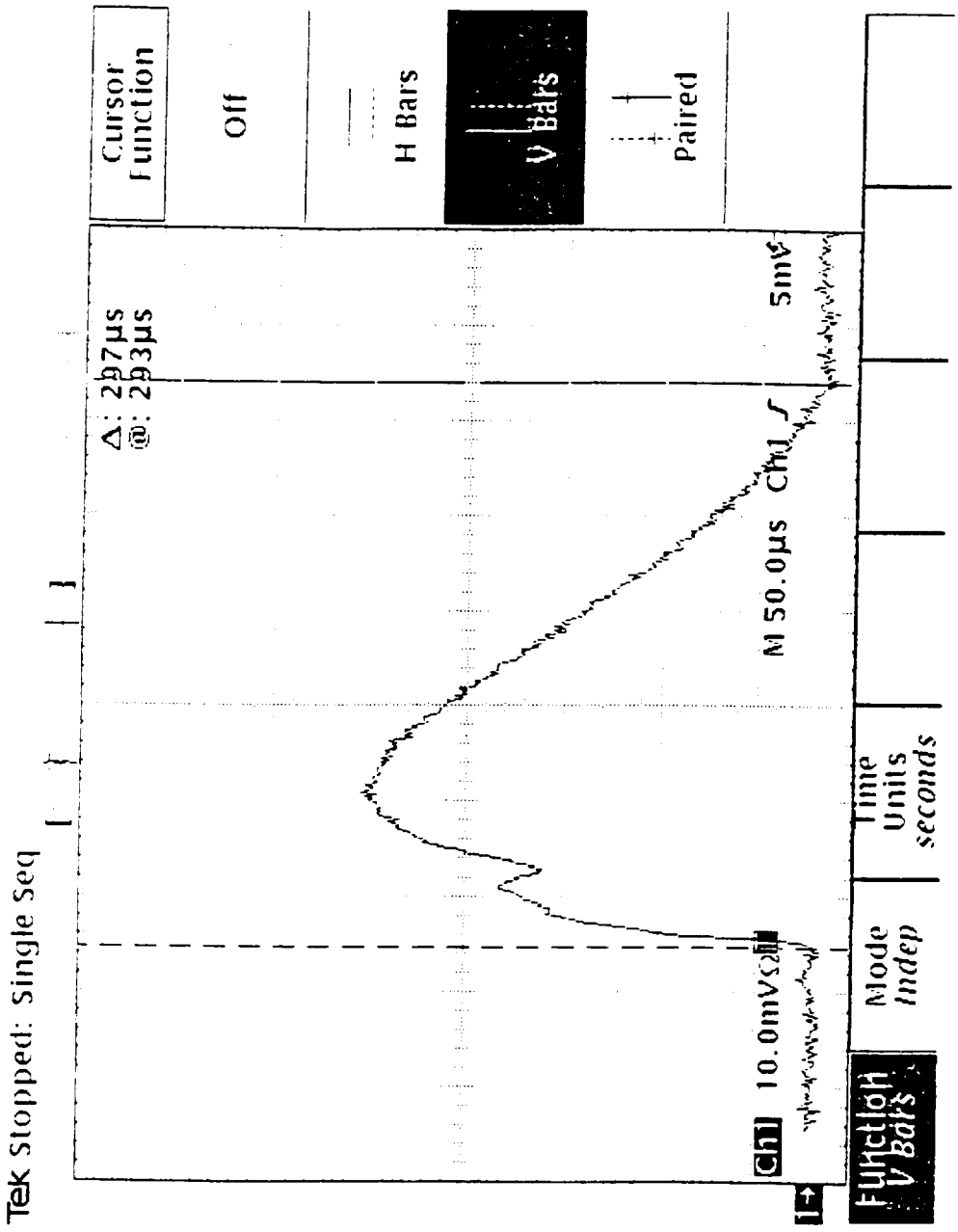
PULSE WIDTH @ V=23.00VDC
PROBE SETTINGS: (5A/DIV) * (1DIV/10mV) = 0.5A/DIV

ATTACHMENT 7



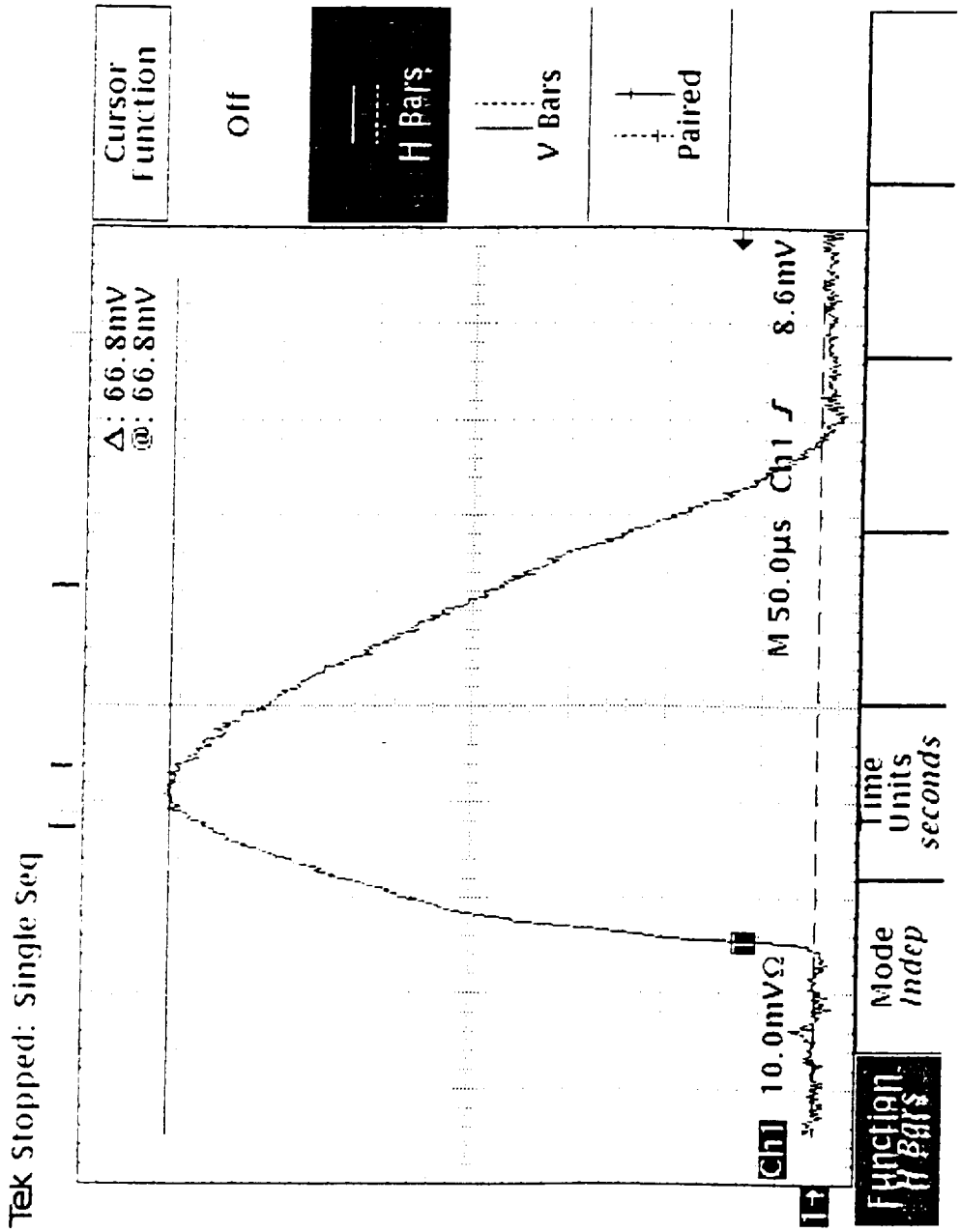
PEAK STARTUP CURRENT @ V=28.00VDC
PROBE SETTINGS: (5A/DIV) * (1DIV/10mV) = 0.5A/DIV

ATTACHMENT 8



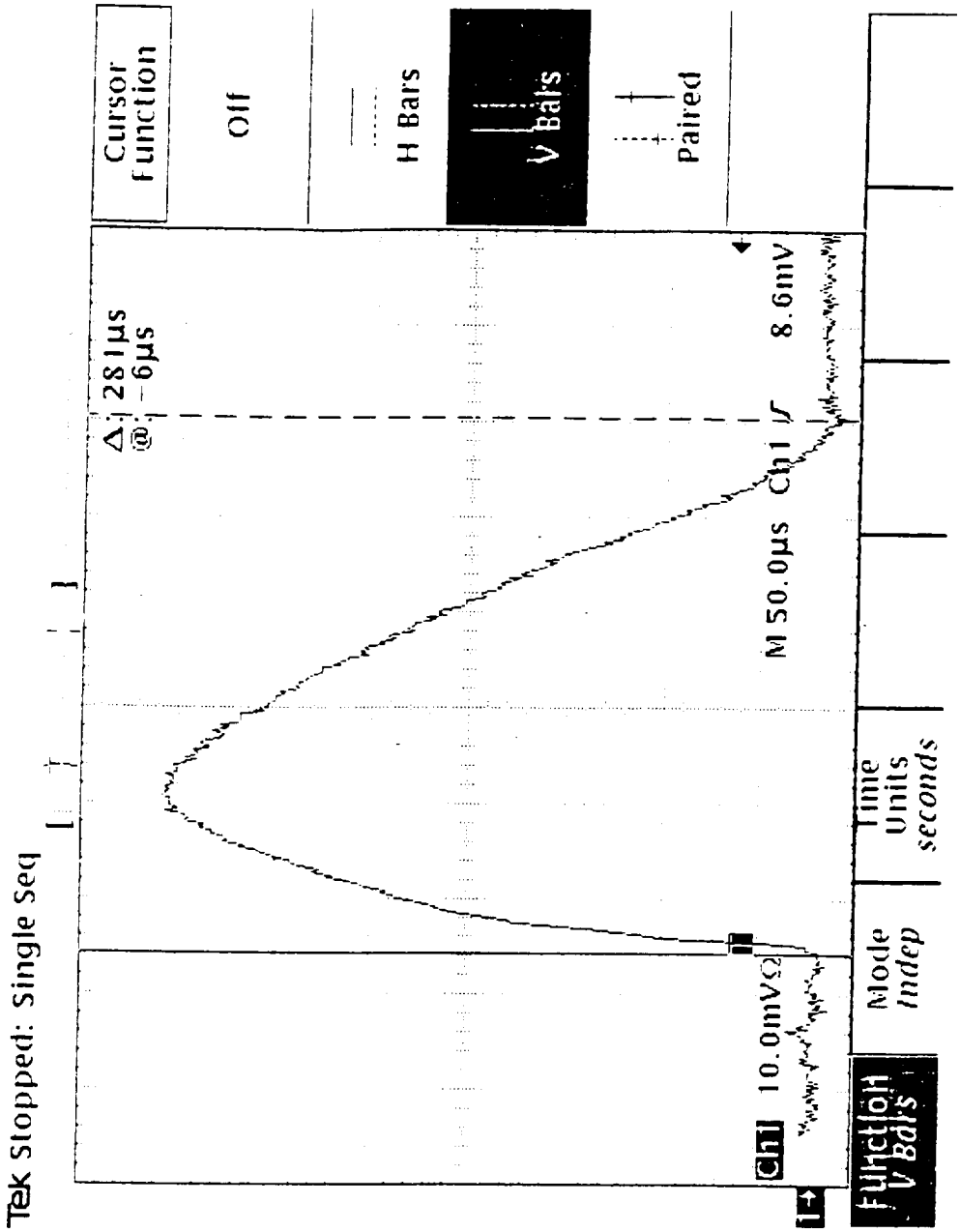
PULSE WIDTH @ V=28.00VDC
PROBE SETTINGS: (5A/DIV) * (1DIV/10mV) = 0.5A/DIV

ATTACHMENT 9



PEAK STARTUP CURRENT @ V=32.00VDC
PROBE SETTINGS: (2A/DIV) * (1DIV/10mV) = 0.2A/DIV

ATTACHMENT 10



PULSE WIDTH @ V=32.00VDC
PROBE SETTINGS: (2A/DIV) * (1DIV/10mV) = 0.2A/DIV

APPENDIX 7

CONFORMAL COAT RESULTS

SUBNOTEBOOK PRODUCT MATRIX

Subnotebook Product	SYSTEM SPEC	MEMORY (RAM)	STORAGE	INTERFACES	POINTING DEVICE	DISPLAY	KEYBOARD	SOFTWARE	PHYSICAL
Compaq Contura Aero/25 MHz	25 MHZ 486SX	4 MB (expandable to 12 MB)	84 or 170 MB Hard Drive	PCMCIA Type II Slot, Enhanced Parallel, Serial	Intergrated Easy Point Trackball	8 " Passive Matrix Mono Backlit, VGA	76 Key	MS-DOS 6, MS-Windows, Winlink File Transfer Utility	1.5 x 7.5 x 10.25 3.5 lbs
Compaq Contura Aero/33 MHz	33 MHZ 486SX	4 MB (expandable to 12 MB)	170 or 250 MB Hard Drive	PCMCIA Type II Slot, Enhanced Parallel, Serial	Intergrated Easy Point Trackball	7.8" Color Backlit, VGA	76 Key	MS-DOS 6, MS-Windows, Winlink File Transfer Utility	1.7 x 7.5 x 10.25 4.2 lbs
Gateway 2000/Handbook DX2-40	40 MHz DX2	8 MB (expandable to 20 MB)	130 MB Hard Drive	PCMCIA Type II Slot, Parallel, Serial, PS/2	Integrated	7.9" Backlit VGA	78 Key	MS-DOS 6, Windows, Interlink, MS works 3.0	1.6 x 5.9 x 9.75 2.9 lbs
Gateway 2000/Handbook DX2-50	50 MHz DX2	8 MB (expandable to 20 MB)	250 MB Hard Drive	PCMCIA Type II Slot, Parallel, Serial, PS/2	Integrated	7.9" Backlit VGA	78 Key	MS-DOS 6, Windows, Interlink, MS works 4.3	1.6 x 5.9 x 9.75 2.9 lbs
Hewlett-Packard/Omnibook 530	33 MHz 486 CPU	4 MB (expandable to 8 MB or 12 MB with opt RAM expansion card)	130 MB Hard Drive	Serial, Parallel, Infrared port	Built-in Popup Mouse	9" 16 Shades of gray, VGA	85 Key	MS-DOS 6.2, Windows 3.3.1, Laplink Remote Access, MS works 3.0	1.4 x 6.4 x 11.1 3 lbs
Prolinear Palmbook 386/PS-3000	386SXLV/25 MHz	2 MB (expandable to 4 MB)	PCMCIA, 2MB ROM	Two PCMCIA Type II Slots, Serial, Parallel	N/A	7.5" 16 Shades of gray, CGA	82 Key	MS-DOS 6, MS-Windows	1 x 4.5 x 9.5 1.5 lbs
Toshiba Protege/3400CT	iSX/33 MHz	4 MB (expandable to 20 MB)	120 MB or 250 MB Hard Drive	PCMCIA Type II Slot, Serial, Parallel	Integrated	7.8" AMLCD	76 Key	MS-DOS 5, MS-Windows	2 x 7.75 x10 4.4 lbs
Zenith Data Systems/Z-Lite 425L	iSL/25 MHz	4 MB (expandable to 8 MB)	80 MB or 120 MB Hard Drive	Two PCMCIA Type II Slots, Serial, Parallel	Optional	8.5"	82 Key	MS-DOS 5, MS-Windows	1.5 x 7.5 x 9.9 3.77 lbs
Kalidor/K2000	Am386SXLV -3.3V/25 MHz	8 MB (expandable to 16 MB)	1.8" 85 MB Hard Drive	Parallel, Serial, Infrared (Note: PCMCIA and Integrated Wireless LAn available as an option)	Pen	7.5" VGA	None	MS-DOS, MS-Windows, PenDOS, PenRight!	1.8 x 6.4 x 9.7 3.5 lbs

SNB CONFORMAL COAT PROCESS

Date: 5/26/95

Subject: Dis-assembly of NASA Ames GFE (Subnotebook: Hewlett Packard Omnibook 600C, S/N US50700339)

The following lists the steps taken to dis-assemble the Subnotebook (SNB).

1. Removed all peripheral devices from the SNB.

- Floppy Drive
- Hard Drive
- PCMCIA Card Bracket
- Battery Pack
- Rear I/O Cover Plate

2. Removed visible screws from bottom of SNB

3. Removed Rubber foot pads and then removed screws which were underneath.

4. Ejected mouse and removed screw located on inside of mouse cavity.

5. At this point the bottom half of SNB can be separated from the display housing (top half of SNB).

Caution: there are several cable connections (3) preventing the bottom half from being completely disconnected from the top half.

6. Disconnected the three connectors (the two near the front end of SNB. The third connector is the display connector near the rear right of SNB). Removed the screw attached to the lug. This is part of the display coonector. The next step should be to remove the hinge plate. If not careful the hinge plate will fall out and re-assembly will be more difficult (see step 7).

7. The hinge plate fell out of the assembly. It was undetermined as to how it was assembled. There was a spring mechanism which also fell out. This made the re-assembly difficult because the assembler was unable to recall how this particular assembly was assembled.

8. Once steps 1 through 7 are complete, the bottom half of the unit can be completely detached from the rest of the unit.

9. The circuit board is mounted in the bottom half and is secured by mounting screws.

10. Removed all the mounting screws holding in the circuit board.

11. Removed all the ribbon cables which were attached to the circuit board.

12. Removed the studs from the I/O connector panel (the three connectors looking at rear of unit left to right)

13. Removed I/O panel from bottom housing.

14. Removed Circuit board from bottom housing.

15. Board was sent to SAIC Conformal Coat process room for conformal coating.

16. In addition to conformal coating the SNB, SAIC was requested to dis-assemble the display housing and evaluate the display and also analyze the SNB circuit board battery design etc.

After examination of the display housing, it was determined that dis-assembly would be destructive to the housing. NASA Ames was notified of this and agreed to not dis-assemble the display housing.

SAIC did attempt to evaluate the battery design. Without schematics, or a parts list, it was difficult to make any conclusions. SAIC was able to identify what appeared to be three batteries rated at 5.5 volts each. Identification of the manufacture name and part number was difficult. The nomenclature located on the batteries was small and indiscernible.

17. The circuit board was returned from conformal coating.

18. Re-assembly consisted of performing the dis-assembly steps in reverse order.

19. After the unit was completely re-assembled it was powered on to verify operation. SAIC confirmed SNB operation to be satifactory.

APPENDIX 8

ACCEPTANCE TEST PROCEDURE

APW II ACCEPTANCE TEST PROCEDURE/RESULTS

1. EQUIPMENT REQUIRED

1.1 This ATP verifies the operation of the four major modules in the APW II computer. Table 1 defines the APW II hardware to be tested.

Table 1

Item	Model/Part Number	Description
Server Module	65460-1	Includes CPU, Power supply, 32 MB RAM, Floppy Drive, Dual PCMCIA Sockets, Removable Hard Drive, SCSI Port, Etehrnet Port, NTSC Port, SVGA Port, Trackball and Keyboard Ports, RS232 and RS422 Ports, and Parallel Port
Display Module	65430-1	
Keyboard Module	65410-1	
Battery Module	65420-1	
Battery Cable	65407-1	
Display Cable	65405-1	
Keyboard Cable	65406-1	
External Power Supply	50362-1	

1.2 TEST SET-UP

1.2.1 Ensure all equipment power switches are OFF.

1.2.2 Enter Part Number and Serial Number of the UUT, and the date on the Acceptance Test Record here. Signature to be added after completion of testing.

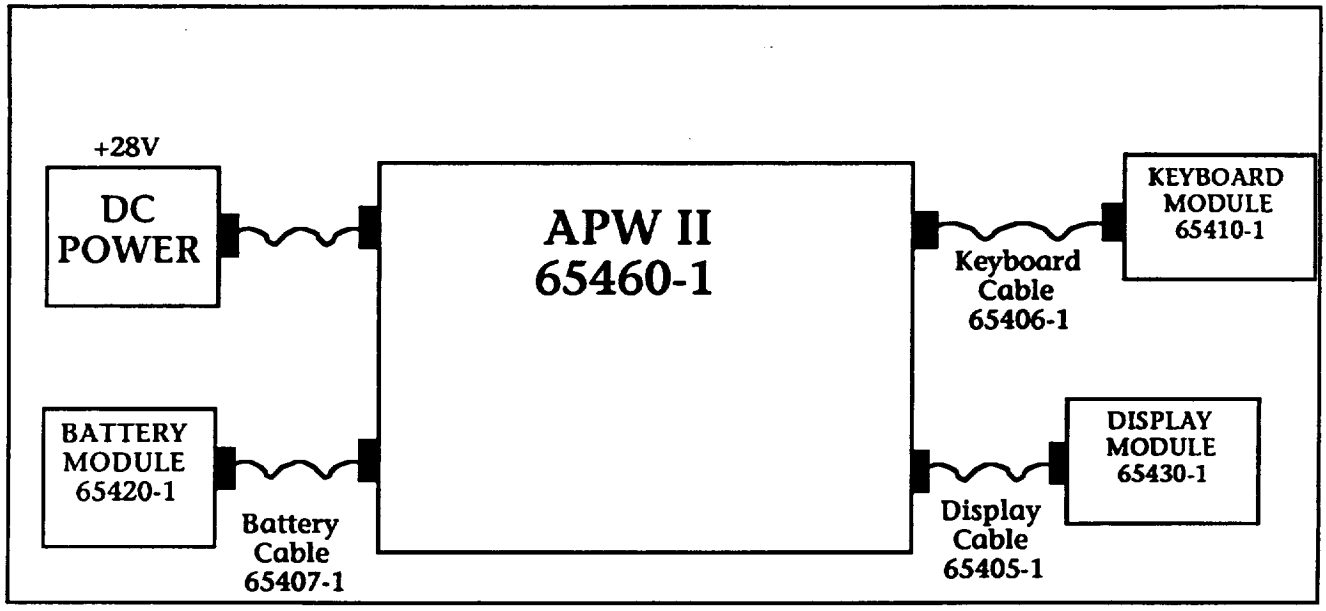
Part Number _____

Serial Number _____

Date:_____

Test Technician: _____/_____
Signature Date

1.2.3 The following diagram illustrates the test setup for the APW II ATP test:



Test Set-Up

1.3 START TEST

1.3.1 Power On APW II

1.3.2 Press F5 key when "starting MS-DOS Prompt." This will bypass system setup and free-up the necessary memory to run CheckIt.

1.3.3 After system completes boot-up, run DIAG out of the CheckIt directory.

2. CPU AND CORE LOGIC TEST

2.1 The following selected tests from Touchstone CheckIt v3.0 diagnostics were used in verifying the functions of the CPU and core logic, real time clock, keyboard, mouse and memory.

Table 2 System Board Test Results

	Pass/Fail
CPU General Functions	
CPU Interrupt Bug	
CPU 32-bit Multiply (80386 and above)	
CPU Protected Mode (80286 and above)	
NPU Arithmetic Functions	
NPU Trigonometric Functions	
NPU Comparison Functions	
DMA Controller(s)	
Interrupt Controller(s)	

Table 3 Real-Time Clock Test Results

	Pass/Fail
Compare Real-Time Clock time to DOS time.	
Compare Real-Time Clock date to DOS date.	
Test Real-Time Clock alarm.	
Compare Elapsed Time.	

Table 4 Keyboard Test Results

	Pass/Fail
Press Each Key	
Typeamatic Repeat Test	
Keyboard Lights Test	

2.2 The mouse test is optional. If decide to run this test, the mouse driver provided with the mouse must be installed prior to conducting this test.

Table 5 Mouse Test Results

	Pass/Fail
Press each mouse button.	
Move mouse to screen top.	
Move mouse to screen bottom.	
Move mouse to screen left.	
Move mouse to screen right.	

2.3 The following Touchstone CheckIt v3.0 diagnostics and functional tests validate the memory. Note: CheckIt will only test the first 16MB.

Table 6 Memory Test Results

	Pass/Fail
Program Buffers.	
Base memory.	
Extended memory.	
Expanded memory.	Not tested
High address lines.	

3. IDE INTERFACE TEST

3.1 The following Touchstone CheckIt v3.0 diagnostics and functional tests validate the IDE interface.

Table 7 IDE Hard Disk Diagnostic Test Results

	Pass/Fail
Controller Diags	
Linear Read	
Butterfly Read	
Random Read	

4. FLOPPY DRIVE INTERFACE TEST

4.1 The following Touchstone CheckIt v3.0 diagnostics and functional tests validate the floppy drive interface.

Table 8 Floppy Diskette Drive Diagnostic Test Results

	Pass/Fail
Insert Disk	
Random Read	
Random Write	

5. SERIAL PORTS (RS232 and RS422) TEST

5.1 The following Touchstone Checkit v3.0 diagnostics validate the serial ports. The results of the modem control and modem status for both COMM ports will be FAILED. This is not considered a failure of the test.

Table 9 RS232 Serial Port Diagnostic Test Results

	Pass/Fail
Describe serial port.	
Test data register.	
Test interrupt enable.	
Test interrupt id.	
Test line control.	
Test modem control.	
Test line status.	
Test modem status.	
Test different baud rates.	

Table 10 RS422 Serial Port Diagnostic Test Results

	Pass/Fail
Describe serial port.	
Test data register.	
Test interrupt enable.	
Test interrupt id.	
Test line control.	
Test modem control.	
Test line status.	
Test modem status.	
Test different baud rates.	

6. PARALLEL PORT TEST

6.1 The following Touchstone Checkit v3.0 diagnostics validate the parallel port. Must connect a printer or use a parallel loopback connector.

Table 11 Parallel Port Diagnostic Test Results

	Pass/Fail
Describe serial port.	
Test data register.	
Test interrupt enable.	
Test interrupt id.	

7. SVGA CRT INTERFACE TEST

7.1 The following Touchstone Checkit v3.0 diagnostics and functional ports validate the SVGA interface. Note: This test is optional.

Table 12 RAM Video Diagnostic Test Results

	Pass/Fail
Video Memory	
Video Page Test (8 Pages)	

7.2 VIDEO TEXT TESTS

Table 13 Character Set Video Diagnostic Test Results

	Pass/Fail
Mode 00h (CGA)	
Mode 01h (CGA)	
Mode 07h (MDA)	
Mode 02h (CGA)	
Mode 03h (CGA)	

Table 14 Character Attribute Video Diagnostic Test Results

	Pass/Fail
Mode 00h (CGA)	
Mode 01h (CGA)	
Mode 07h (MDA)	
Mode 02h (CGA)	
Mode 03h (CGA)	

Table 15 Character Color Video Diagnostic Test Results

	Pass/Fail
Mode 03h (CGA)	

7.3 VIDEO GRAPHICS TEST

Table 16 Graphics Grid Video Diagnostic Test Results

	Pass/Fail
Mode 04h (CGA)	
Mode 05h (CGA)	
Mode 0Dh (EGA COLOR)	
Mode 13h (MCGA)	
Mode 06h (CGA)	
Mode 0Eh (EGA COLOR)	
Mode 0Fh (EGA MONO)	
Mode 10h (EGA HIRES)	
Mode 11h (MCGA)	
Mode 12h (VGA)	

Table 17 Color Palette Video Diagnostic Test Results

	Pass/Fail
Mode 04h (CGA)	
Mode 0Dh (EGA COLOR)	
Mode 13h (MCGA)	
Mode 0Eh (EGA COLOR)	
Mode 10h (EGA HIRES)	
Mode 12h (VGA)	

Table 18 Color Purity Video Diagnostic Test Results

	Pass/Fail
Red	
Green	
Blue	

8. FLAT PANEL DISPLAY TEST

8.1 The following functional tests validate the the flat panel display interface.

Table 19 RAM Video Diagnostic Test Results

	Pass/Fail
Video Memory	
Video Page Test (8 Pages)	

8.2 VIDEO TEXT TEST

Table 20 Character Set Video Diagnostic Test Results

	Pass/Fail
Mode 00h (CGA)	
Mode 01h (CGA)	
Mode 07h (MDA)	
Mode 02h (CGA)	
Mode 03h (CGA)	

Table 21 Character Attribute Video Diagnostic Test Results

	Pass/Fail
Mode 00h (CGA)	
Mode 01h (CGA)	
Mode 07h (MDA)	
Mode 02h (CGA)	
Mode 03h (CGA)	

Table 22 Character Color Video Diagnostic Test Results

	Pass/Fail
Mode 03h (CGA)	

8.3 VIDEO GRAPHICS TEST

Table 23 Graphics Grid Video Diagnostic Test Results

	Pass/Fail
Mode 04h (CGA)	
Mode 05h (CGA)	
Mode 0Dh (EGA COLOR)	
Mode 13h (MCGA)	
Mode 06h (CGA)	
Mode 0Eh (EGA COLOR)	
Mode 0Fh (EGA MONO)	
Mode 10h (EGA HIRES)	
Mode 11h (MCGA)	
Mode 12h (VGA)	

Table 24 Color Palette Video Diagnostic Test Results

	Pass/Fail
Mode 04h (CGA)	
Mode 0Dh (EGA COLOR)	
Mode 13h (MCGA)	
Mode 0Eh (EGA COLOR)	
Mode 10h (EGA HIRES)	
Mode 12h (VGA)	

Table 25 Color Purity Video Diagnostic Test Results

	Pass/Fail
Red	
Green	
Blue	

9. ETHERNET NETWORK INTERFACE TEST

9.1 The following functional tests validate the the Ethernet network interface.

Table 26 Ethernet Network Interface Custom Diagnostics Results

	Pass/Fail
Base address register read/write	
Ethernet ID test	
I/O register base address	
I/O Register read/write test	
Chip ID Register (low)	
Internal loopback (no MENDEC) 64 byte test	
Internal loopback (no MENDEC)2 byte RUNT test	
Internal loopback (MENDEC) 12 byte RUNT test	

10. SCSI INTERFACE TEST

10.1 The following custom diagnostics and functional tests validate the SCSI interface.

Table 27 SCSI Controller Custom Diagnostic Test Results

	Pass/Fail
Base address register read/write	
SCSI ID test	
I/O Register base address	
I/O Register read/write test	
IRQ 11 test	

11. PCMCIA INTERFACE TEST

11.1 The following custom diagnostics and functional tests validate the PCMCIA interface.

Table 28 PCMCIA Controller Custom Diagnostic Test Results

	Pass/Fail
Base address register read/write	
PCMCIA ID test	
I/O Index base address	
I/O Index register read/write	

12. NTSC VIDEO INPUT TEST

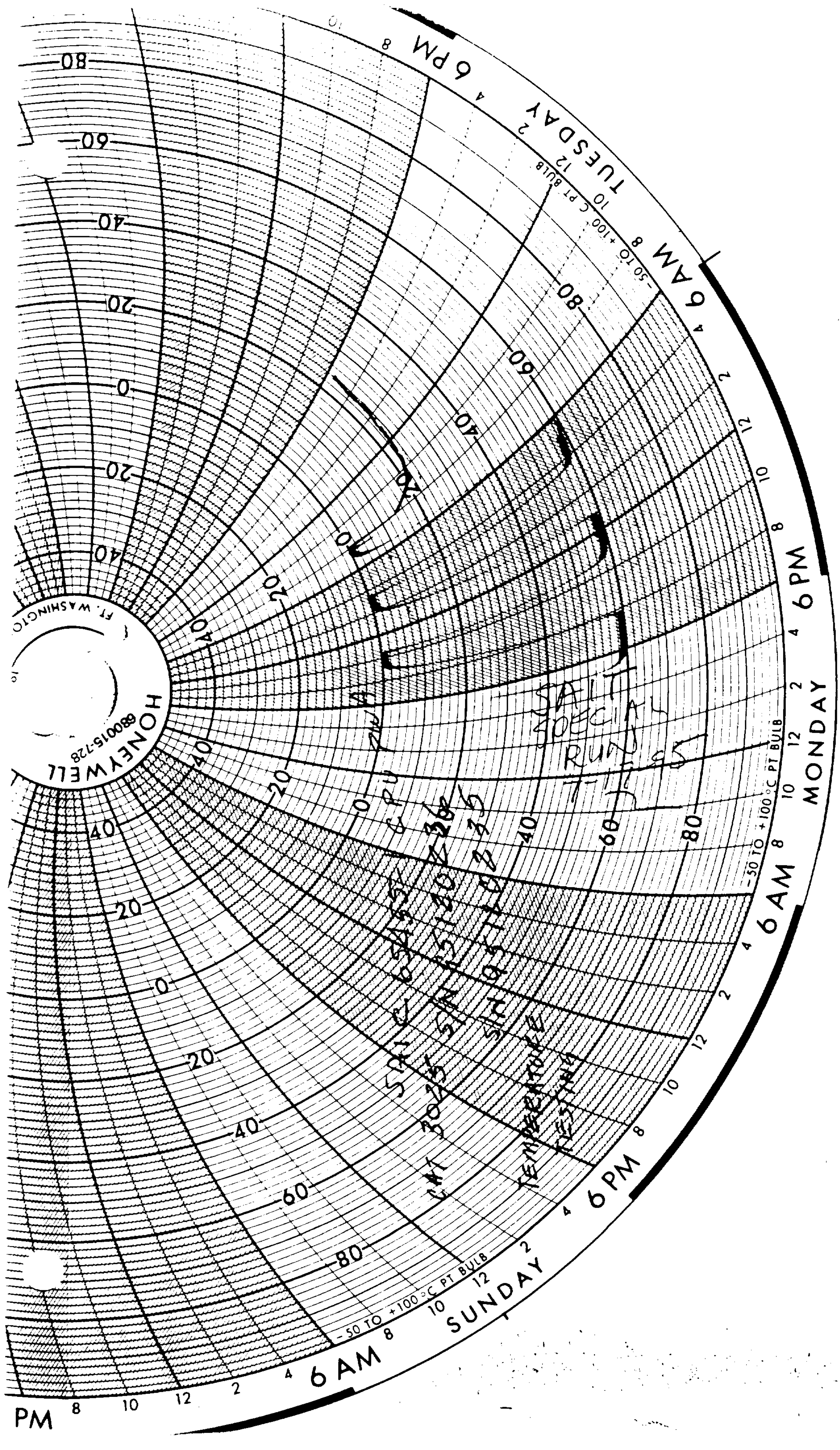
12.1 The following functional tests validate the the NTSC video input.

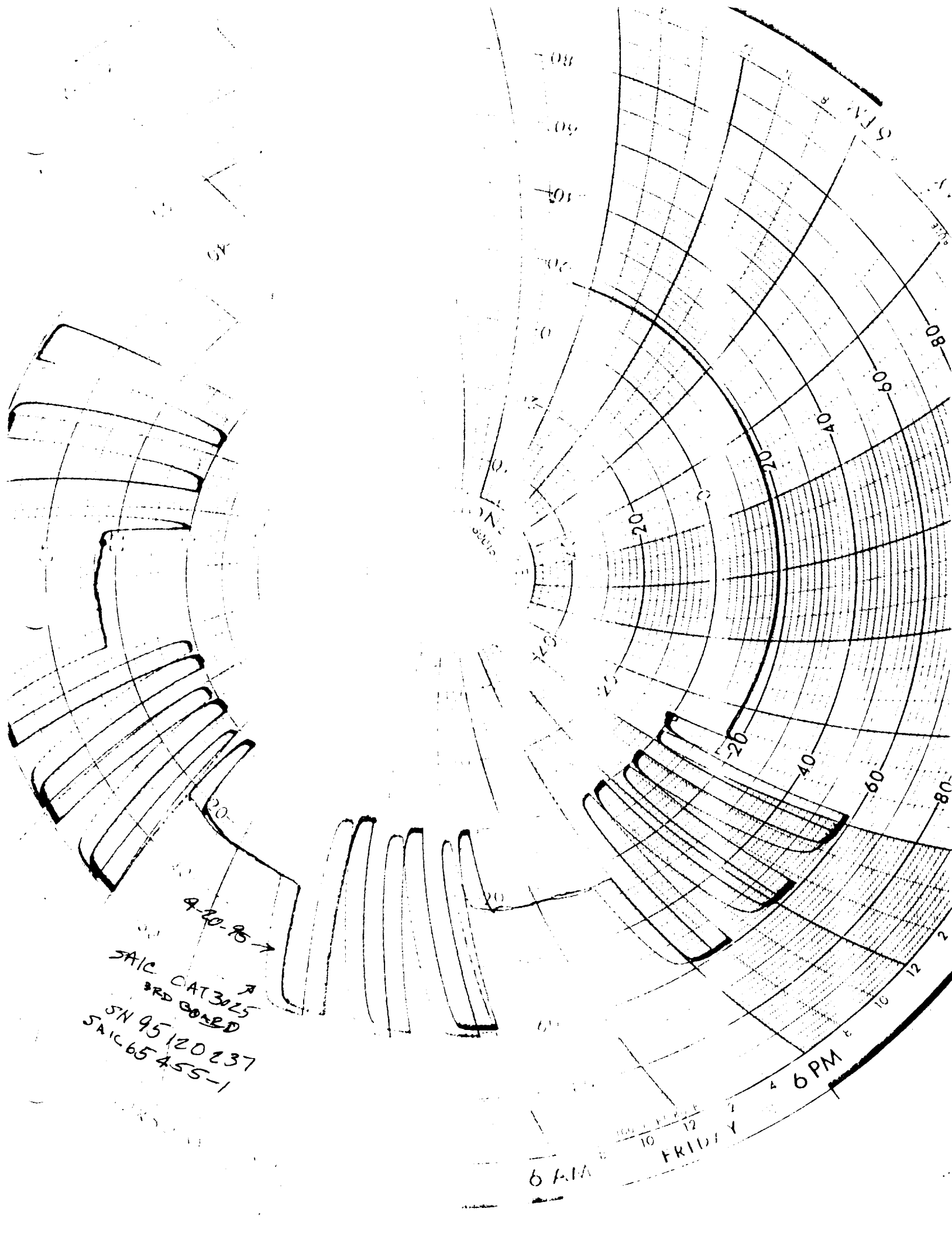
Table 29 NTSC Video Input Custom Diagnostic Test Results

	Pass/Fail
Testing PC Video analog input interface message displayed	
Phillips 7191 does not detect a video source message displayed	
Video RAM test	

APPENDIX 9

ENVIRONMENTAL STRESS SCREENING RESULTS


HONEYWELL
680015-728
FT. WASHINGTON
SUNDAY
MONDAY
TUESDAY
6 AM
6 PM
-50 TO +100°C PT BULB


9-20-95
SAIC CAT3025
3RD BOARD
SN 95120237
SAIC 65455-1
6 PM
6 AM
FRIDAY

APPENDIX 10

SOFTWARE VALIDATION RESULTS

CAT3025 DVT/ACCEPTANCE TEST RESULTS

1. EQUIPMENT

1.1 Table 1.1 defines the hardware setup used in performing the acceptance testing.

Item	Make	Model	Description
CPU	DTI	CAT3025	Pentium laptop motherboard
Main memory	IBM	1104480BA-	(2) 4MB x 36-70 SIMMs
IDE hard disk drive	DiscTec	A260	262 MB removable hard disk
SCSI hard disk drive	Seagate	ST3550N	435 MB SCSI hard disk
SCSI CDROM drive	NEC	CDR501	Quad-speed SCSI
PCMCIA hard disk drive	Maxtor	C1001YBU	105 MB ATA
PCMCIA flash	Intel	IMC010FLSA-20	10 MB flash card
Ethernet hub	Gateway Communications, Inc.	62000125	G/Ethertwist hub null
Floppy diskette drive	NEC	FD1139H	Small form factor
3.5" floppy drive			
Mouse	Microsoft	37967	Serial - mouse port compatible mouse
Keyboard	BTC	BTC-53	101-key keyboard
CRT monitor	NEC	Multisync 3D	14 inch SVGA monitor
Power supply	Yahata	PSK-D247B-3	5 output power with 24 V @ 60 W output
Printer	Citizen	120D	9-pin dot matrix parallel port printer

Table 1.1

2. CPU AND CORE LOGIC

2.1 The following selected tests from Touchstone CheckIt v3.0 diagnostics were used in verifying several functions of the CPU and core logic.

Touchstone CheckIt v3.0 System Board Test Results	
CPU General Functions	Passed
CPU Interrupt Bug	Passed
CPU 32-bit Multiply (80386 and above)	Passed
CPU Protected Mode (80286 and above)	Passed
NPU Arithmetic Functions	Passed
NPU Trigonometric Functions	Passed
NPU Comparison Functions	Passed
DMA Controller(s)	Passed
Interrupt Controller(s)	Passed

Table 2.1

Touchstone CheckIt v3.0 Real-Time Clock Test Results	
Compare Real-Time Clock time to DOS time.	Passed
Compare Real-Time Clock date to DOS date.	Passed
Test Real-Time Clock alarm.	Passed
Compare Elapsed Time.	Passed

Table 2.2

Touchstone CheckIt v3.0 Keyboard Test Results	
Press Each Key	Passed
Typeamatic Repeat Test	Passed
Keyboard Lights Test	Passed

Table 2.3

Touchstone CheckIt v3.0 Mouse Test Results	
Press each mouse button.	Passed
Move mouse to screen top.	Passed
Move mouse to screen bottom.	Passed
Move mouse to screen left.	Passed
Move mouse to screen right.	Passed

Table 2.4

2.2 Selected tests from Symantec Norton Diagnostics v7.0 diagnostics were used in verifying the following functions of the CPU and core logic.

Symantec Norton Diagnostics v7.0 Base Memory Test Results	
Bit stuck @ 0	Passed
Bit stuck @ 1	Passed
Walking 1's	Passed
Walking 0's	Passed
Checkerboard	Passed
Inverted checkerboard	Passed

Table 2.5

Symantec Norton Diagnostics v7.0 Extended Memory Test Results	
Bit stuck @ 0	Passed
Bit stuck @ 1	Passed
Walking 1's	Passed
Walking 0's	Passed
Checkerboard	Passed
Inverted checkerboard	Passed

Table 2.6

Symantec Norton Diagnostics v7.0 Other Test Results	
Speaker	Passed

Table 2.7

2.3 Benchmark measurements were obtained in order to verify optimal CPU / core logic performance.

HLFloat Benchmark Results	
Total floating point (s)	0.32
Forward FFT, 2048 pts. (s)	0.16
Reverse FFT, 2048 pts. (s)	0.16
Total time, include. graphics (s)	0.49

Table 2.8

Core International Coretest v2.92 Benchmark Results	
Data transfer rate (KB/s) (DiscTec A260)	1062.7
Average seek time (ms) (DiscTec A260)	14.2
Track to track seek time (ms) (DiscTec A260)	4.7
Performance index	122.0

Table 2.9

Symantec Norton SI v6.0 Benchmark Results	
Computing index	286.1
Disk index (DiscTec A260)	8.6
Performance index	193.5

Table 2.10

Landmark System Speed Test v2.0 Benchmark Results	
CPU (Mhz)	520.65
FPU (Mhz)	1525.14
Video (char./s)	3437.0

Table 2.11

Landmark System Speed Test v6.0 Benchmark Results	
CPU (Mhz)	940.91
FPU (Mhz)	1497.99
Video (char./s)	3449.26

Table 2.12

Database Group Power Meter v1.2 enchmark Results	
MIPS	58.171
Whetstones (K whet/s)	937.510
NOPs (ns/NOP)	5.813

Table 2.13

Diagsoft Power Meter v1.8 Benchmark Results	
MIPS	41.8
Whetstones (K whet/s)	17,531.8

Table 2.14

PC Magazine Winbench v2.50 Benchmark Results	
Winmarks (x106)	4.098

Table 2.15

DiscTec Hard Disk Utility v1.15 Benchmark Results	
Track to track seek time (ms)	2.71
Average seek time (ms)	13.55
16 KB block read (KB/s)	1366.70
32 KB block read (KB/s)	1391.90
64 KB block read (KB/s)	1090.05

Table 2.16

3. IDE INTERFACE

3.1 The following Touchstone CheckIt v3.0 diagnostics and functional tests were performed in order to validate the IDE interface.

Touchstone Checkit v3.0 IDE Hard Disk Diagnostic Test Results	
Controller Diags	Passed
Linear Read	Passed
Butterfly Read	Passed
Random Read	Passed

Table 3.1

IDE Hard Disk Drive Functional Test Results	
DiscTec Removable Hard Disk driver v1.34	Passed
Hard disk file write / read test	Passed
Software and operating system installation	Passed

Table 3.2

4. FLOPPY DRIVE INTERFACE

4.1 The following Touchstone CheckIt v3.0 diagnostics and functional tests were performed in order to validate the floppy drive interface.

Touchstone CheckIt v3.0 Floppy Diskette Drive Diagnostic Test Results	
Insert Disk	Passed
Random Read	Passed
Random Write	Passed

Table 4.1

Floppy Diskette Drive Functional Test Results	
Software installation	Passed
File write / read test	Passed

Table 4.2

5. SCSI INTERFACE

5.1 The following custom diagnostics and functional tests were performed in order to validate the SCSI interface.

SCSI Hard Disk Drive Functional Test Results	
Driver installation and verification	Passed
Hard disk file write / read test	Passed
Still camera connection and diagnostics	Passed

Table 5.1

SCSI Controller Custom Diagnostic Test Results	
Base address register read/write	Passed
SCSI ID test	Passed
I/O Register base address	3400
I/O Register read/write test	Passed
IRQ 11 test	Passed

Table 5.2

6. PCMCIA INTERFACE

6.1 The following custom diagnostics and functional tests were performed in order to validate the PCMCIA interface.

PCMCIA Device Functional Test Results	
Driver installation and verification	Passed
Card installation, detection, and verification	Passed
ATA hard disk boot source	Passed
ATA hard disk file write / read test	Passed
Flash card file write / read test	Passed

Table 6.1

PCMCIA Controller Custom Diagnostic Test Results	
Base address register read/write	Passed
PCMCIA ID test	Passed
I/O Index base address	34a0
I/O Index register read/write	Passed

Table 6.2

7. SERIAL PORTS

7.1 The following Touchstone Checkit v3.0 diagnostics were performed in order to validate the serial ports.

Touchstone CheckIt v3.0 Serial Port Diagnostic Test Results	
Describe serial port.	Has Loopback
Test data register.	Passed
Test interrupt enable.	Passed
Test interrupt id.	Passed
Test line control.	Passed
Test modem control.	Passed
Test line status.	Passed
Test modem status.	Passed
Test different baud rates.	Passed

Table 7.1

8. PARALLEL PORT

8.1 The following Touchstone Checkit v3.0 diagnostics were performed in order to validate the parallel ports.

Touchstone CheckIt v3.0 Parallel Port Diagnostic Test Results	
Describe parallel port.	Has Loopback
Test parallel data register.	Passed
Test with external loopback.	Passed
Printer interface test	Passed

Table 8.1

9. SVGA CRT INTERFACE

9.1 The following Touchstone Checkit v3.0 diagnostics and functional ports were performed in order to validate the SVGA interface.

Touchstone CheckIt v3.0 RAM Video Diagnostic Test Results	
Video Memory	Passed
Video Page Test (8 Pages)	Passed

Table 9.1

9.2 VIDEO TEXT TESTS

Touchstone CheckIt v3.0 Character Set Video Diagnostic Test Results	
Mode 00h (CGA)	Passed
Mode 01h (CGA)	Passed
Mode 07h (MDA)	Passed
Mode 02h (CGA)	Passed
Mode 03h (CGA)	Passed

Table 9.2

Touchstone CheckIt v3.0 Character Attribute Video Diagnostic Test Results	
Mode 00h (CGA)	Passed
Mode 01h (CGA)	Passed
Mode 07h (MDA)	Passed
Mode 02h (CGA)	Passed
Mode 03h (CGA)	Passed

Table 9.3

Touchstone CheckIt v3.0 Character Color Video Diagnostic Test Results	
Mode 03h (CGA)	Passed

Table 9.4

9.3 VIDEO GRAPHICS TESTS

Touchstone CheckIt v3.0 Graphics Grid Video Diagnostic Test Results	
Mode 04h (CGA)	Passed
Mode 05h (CGA)	Passed
Mode 0Dh (EGA COLOR)	Passed
Mode 13h (MCGA)	Passed
Mode 06h (CGA)	Passed
Mode 0Eh (EGA COLOR)	Passed
Mode 0Fh (EGA MONO)	Passed
Mode 10h (EGA HIRES)	Passed
Mode 11h (MCGA)	Passed
Mode 12h (VGA)	Passed

Table 9.5

Touchstone CheckIt v3.0 Color Palette Video Diagnostic Test Results	
Mode 04h (CGA)	Passed
Mode 0Dh (EGA COLOR)	Passed
Mode 13h (MCGA)	Passed
Mode 0Eh (EGA COLOR)	Passed
Mode 10h (EGA HIRES)	Passed
Mode 12h (VGA)	Passed

Table 9.6

Touchstone CheckIt v3.0 Color Purity Video Diagnostic Test Results	
Red	Passed
Green	Passed
Blue	Passed

Table 9.7

Windows v3.x Video Driver Installation and Verification (All Resolutions)	
1024 x 768 x 16 color	Passed
1024 x 768 x 256 color	Passed
1280 x 1024 x 16 color	Not supported
640 x 480 x 16 color	Passed
640 x 480 x 16 M color	Passed
640 x 480 x 256 color	Passed
640 x 480 x 32K color	Not supported
640 x 480 x 64K color	Not supported
800 x 600 x 16 color	Passed
800 x 600 x 256 color	Passed

Table 9.8

10. FLAT PANEL DISPLAY INTERFACE

10.1 The following functional tests were performed in order to validate the the flat panel display interface.

FPD Interface Functional Test Results	
CheckIt v3.0 diagnostics (see section 9)	Passed
Flat panel centering and alignment verfication	Passed
Driver verification (all resolutions) (see section 9)	Passed

Table 10.1

11. NTSC VIDEO INPUT

11.1 The following functional tests were performed in order to validate the the NTSC video input.

NTSC Video Input Functional Test Results	
Driver installation and verification	Passed
Microsoft Video for Windows compatibility	Passed
Image capture	Passed
Image sizing and scrolling	Passed

Table 11.1

NTSC Video Input Custom Diagnostic Test Results	
Testing PC Video analog input interface	Passed
Phillips 7191 does not detect a video source	Passed
Video RAM test	Passed

Table 11.2

12. ETHERNET NETWORK INTERFACE

12.1 The following functional tests were performed in order to validate the the Ethernet network interface.

Ethernet Network Interface Functional Test Results	
Driver installation and verification	Passed
Network connection to host	Passed
File write / read via network	Passed

Table 12.1

Ethernet Network Interface Custom Diagnostics Results	
Base address register read/write	Passed
Ethernet ID test	Passed
I/O register base address	3480
I/O Register read/write test	Passed
Chip ID Register (low)	12430003
Internal loopback (no MENDEC) 64 byte test	Passed
Internal loopback (no MENDEC) 12 byte RUNT test	Passed
Internal loopback (MENDEC) 12 byte RUNT test	Passed

Table 12.2

13. SYSTEM LEVEL VALIDATION

13.1 The following functional tests were performed in order to validate operating system comatibility.

Operating System Installation	
Microsoft MSDOS v6.22	Passed
Microsoft Windows for Workgroups v3.11	Passed
Microsoft Windows NT Workstation v3.5	*Passed
Novell Netware v4.0	Passed
OS/2 v3.0	Passed

Table 13.1

* Conner CFS210A IDE hard disk drive was used

13.2 ROM utility verification

The following functional tests were performed in order to validate ROM utility functionality.

System Summary	
Processor revision	Verified
Clock speed	Verified
Secondary cache	Verified

Table 13.2

System Setup	
System Time	Passed
System Date	Passed
Video System	Passed
System Memory	Verified
Extended memory	Verified
Diskette Drive A:	Passed
Diskette Drive B:	Not tested

Table 13.3

Hard Disk Setup	
Hard Disk 0	Passed
Hard Disk 1	Passed

Table 13.4

BIOS Options	
Disk drive boot sequence	Passed
System summary screen at boot	Passed
Display SETUP prompt during POST	Passed
Pause on POST errors	Passed
Floppy seek	Passed
Gate A20 at boot	Not tested
Key click	Passed
Keyboard typematic rate	Passed
Keyboard typematic delay	Passed
Numlock	Passed

Table 13.5

Peripherals	
COM Port 1 At	Passed
COM Port 2 AT	Passed
LPT Port At	Passed
Diskette Interace	Passed
IDE interface	Passed
PCMCIA PCI device	Passed
SCSI PCMCIA device	Passed
Ethernet PCI device	Passed

Table 13.6

Security / Virus	
Superviser Password is	Passed
User Password is	Passed
Set Superviser Password	Passed
Set User Password	Passed
Password on boot	Passed
Diskette access	Passed
Fixed disk boot sector	Passed
System backup reminder	Passed

Table 13.7

Power Manager	
Power Savings	Passed
Standby Timeout	Passed
Standby CPU Speed	Passed
Fixed Disk Timeout	Passed
CRT (in Standby)	Passed
Timer Reset and Wake Events	Passed

Table 13.8

System Monitor	
System Temp Lo	Passed
System Temp Hi	Passed
+5 V Tolerance	Passed
+12 V Tolerance	Passed
CPU Tolerance	Passed
Battery minimum voltage	Passed
Fan RPS (min.)	Passed
IRQ 10 Alarm Enables	Passed

Table 13.9

Thermal Manager	
Thermal Management	Passed
CPU Throttle Control	Passed
Thermal IRQ 10 Alarm	Passed

Table 13.10

CMOS Load / Save Functions	
Load From ROM	Passed
Load From CMOS	Passed
Save to CMOS	Passed

Table 13.11

APPENDIX 11

SAFETY DATA INFORMATION

NASA RTV Spray Application Procedure

National Aeronautics and
Space Administration

Lyndon B. Johnson Space Center
Houston, Texas 77058

JSC 18222

PROCEDURE

Procedure for Spray Application of Thin (1-7 mils) RTV Silicone Conformal Coatings for Electronic Assemblies

JULY 1982

This procedure has been established and approved by the JSC Engineering and Development Directorate to provide a standard process for the spray application of thin (1 to 7 mils thick) RTV (room temperature vulcanized) silicone conformal coatings to electronic assemblies.

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TABLE OF CONTENTS

1.0 SCOPE. This procedure specifies the materials, equipment, application procedure, and quality requirements to be used in the spray application of thin conformal coatings to printed circuit boards, wire-wrapped boards, and other electronic assemblies.

2.0 APPLICABLE DOCUMENTS. The following documents form a part of this procedure to the extent specified herein:

a. MIL-A-46146, Adhesive-Sealants, RTV, Silicone, Non-Corrosive (for use with sensitive metals and equipment).

b. JSCM 5312, QOP No. 3.1B, "Raw Material Specification Compliance."

c. JSCM 5312, QOP No. 3.10C, "Control of Limited Life Items."

d. NHB 5300.4(3A-1), "Requirements for Soldered Electrical Connections."

3.0 DEFINITIONS. For the purpose of this procedure, the following definitions shall apply:

a. RTV. Room temperature vulcanizing.

b. Conformal coating. A coating that conforms to the configuration of the object coated.

c. Room temperature. Room temperature is defined as $75\pm4^{o}F/24\pm2^{o}C$.

d. Staking compound. A material used for bonding or mechanical attachment of parts.

e. Room humidity. Relative humidity 20-55 percent.

4.0 REQUIREMENTS.

a. E&D (Engineering and Development) activity. The E&D Directorate shall be responsible for authorizing the use of this procedure.

b. Contractor/user activity. The contractor/user shall be responsible for the following:

(1) Proper implementation of the requirements presented herein.

(2) Providing necessary training of personnel in the use of equipment and techniques used in applying conformal coatings of thin coating materials.

(3) Assuring that all personnel who perform or inspect conformal coatings have demonstrated proficiency in producing high quality end items.

4.1 APPROVED MATERIALS. The following materials have been approved by JSC E&D and shall be used in conjunction with this procedure. Contractors shall use approved materials from approved suppliers only.

Material Name	Approved Source
3140 RTV Silicone Rubber Coating as specified in MIL-A-46146, Type II	Dow Corning Corp. Midland, MI
Primer 1204 as specified in MIL-A-46146	Dow Corning Corp. Midland, MI
Xylene	Commercial grade
Acetone - Technical grade	Federal specification O-A-15F
Other cleaning solvents	Ethyl alcohol, ASC grade, 95 or 99.5 percent by volume.
	Isopropyl alcohol, best commercial grade, 99 percent pure.
	Trichlorotrifluoroethane, clear, 99.8 percent pure.
	Any mixture of the above solvents.
Naptha	VM&P (varnish makers & painters) grade

4.2 PROCESSING EQUIPMENT.

4.2.1 Facility.

a. Size and location. Facility dimensions shall be governed by work volume. The area shall contain sufficient equipment and supplies to prevent the need for an overlap of operations and shall be isolated from all other activities that could result in contamination such as dust, metallic particles, water, oil, and/or grease. Smoking or open flames shall not be allowed within 25 feet of an area where coating materials or solvents are being used.

b. Ventilation. The conformal coating area shall be provided with forced draft ventilation such that vapors are away from the operator and vented to the outside.

c. Environmental conditions. Facility temperature shall be maintained at $75 \pm 4^{\circ}F / 24 \pm 2^{\circ}C$ and the relative humidity shall not exceed 55 percent. A hygrometer and thermometer of sufficient quality to record an accuracy of ± 5 percent relative humidity and $\pm 4^{\circ}F / \pm 2^{\circ}C$ temperature shall be installed within the conformal coating area. The hygrometer and thermometer records shall be maintained for a period of 6 months and shall be made available to the procuring activity upon request.

d. The work table shall be conductive and have an earth-ground connection for grounding items being coated.

4.2.2 Cleaning. Equipment and materials applicable to cleaning of electronic boards shall be as follows:

a. Ethyl alcohol, ASC grade, 95 or 99.5 percent by volume.

b. Isopropyl alcohol, best commercial grade, 99 percent pure.

c. Trichlorotrifluoroethane, clear, 99.8 percent pure.

NOTE: Any mixture of a., b., and c. above is acceptable.

d. Nonmetallic brushes, sizes and stiffness as applicable.

e. Air supply, dry, filtered and pressure regulated.

4.2.3 Assembly Preparation. Equipment and materials applicable to preparation and assembly of printed circuit boards shall be as follows:

a. Masking tape or masking materials (if applicable).

b. Handling clips or blocks.

c. Lint-free gloves or dust-free finger cots.

4.2.4 Coating Material Preparation. Equipment and materials for preparation of conformal coatings shall be as follows:

a. Mixing container (metal, glass, or ceramic).

b. Spatula (metal, glass, plastic, or ceramic).

c. Coating material conforming to MIL-A-46146, type II.

4.2.5 Application, Draining, and Curing. Equipment and materials for applying, draining, and curing of conformal coatings shall be as follows:

a. Brushes (natural bristle) suitable for the configuration of the object to be coated.

b. Curing rack.

c. Hot-air circulating oven capable of maintaining recommended cure temperature within $\pm 4^{\circ}F/\pm 2^{\circ}C$.

d. Spray equipment, capable of producing a uniform spray pattern.

e. Grounding wires capable of grounding the workpiece(s) and the spray applicator.

4.3 OPERATIONS. The sequence of processing shall be as follows:

a. Preparation.

b. Cleaning.

c. Masking.

d. Priming.

e. Preparation of coating.

f. Applying coating.

g. Curing coating.

h. Cleaning.

4.4 PROCEDURE.

CAUTION: THESE ASSEMBLIES CONTAIN PARTS SENSITIVE TO DAMAGE BY ESD (ELECTROSTATIC DISCHARGE). USE ESD PRECAUTIONARY PROCEDURES WHEN TOUCHING, HANDLING, AND PROCESSING ELECTRONIC ASSEMBLIES. ASSURE THAT ALL EQUIPMENT, PERSONNEL, AND ASSEMBLIES ARE FULLY GROUNDED DURING ALL PHASES OF MANUFACTURING TO AVOID INADVERTENT ELECTROSTATIC DAMAGE TO ASSEMBLIES.

4.4.1 Preparation. All printed wiring board/wire wrap assemblies to be conformal coated shall be received prepacked in conductive bagging material. Prior to removal of assemblies from conductive bagging, assure that all personnel, fixtures, and associated tooling are fully grounded. The workpiece shall be grounded by connecting a ground wire to the conductive foam connector shorting strip, etc., as soon as it is removed from its protective packaging. Upon completion of conformal coating activities, all assemblies will be repackaged in the conductive packaging material.

4.4.2 Cleaning. Clean the areas to be coated until they are free of flux residues, grease, oil, and other contaminants by brushing and rinsing in a clean suitable solvent (see note). The use of agitated counter current rinsing is suggested for efficient removal of most organic residues. Remove excess solvent by air blast or by heating at 167±9°F/75±5°C for 15 minutes. During and after cleaning, handle the boards carefully with lint-free gloves to prevent contamination.

NOTE: The selection of a suitable solvent for cleaning a particular assembly will depend upon safety, cleaning power, and effect on the parts and finishes in the assembly. Cleaning solvents shall be in accordance with NHB 53004(3A-1). Special attention should be directed to insuring that the solvent does not harm the workpiece, its markings, or its component.

CAUTION: CONTAMINATION OR DIRTY SOLVENT WILL LEAVE A RESIDUE ON THE SURFACE.

4.4.3 Masking. Mask all areas in accordance with the drawing requirements. Tapes, silicone compounds, fixtures, and equivalent items may be used for masking. Before using tape, the effect of the coating material on the tape adhesive shall be checked by the cognizant laboratory in order to avoid contamination of the coating material or solvent action on the tape adhesive. The assemblies shall be premasked and all connectors shall be guarded with conductive foams. Under no circumstances will these maskants or connector guards be removed during processing activities after cleaning.

4.4.4 Priming. A single coat of approved primer listed in paragraph 4.1 shall be applied. Use only fresh primer which shows no signs of precipitated matter. Keep the primer container covered when not in use. Allow the applied primer to dry for 1 to 2 hours at room temperature before applying coating.

To eliminate occasional traces of a white crystalline substance in the 1204 primer, it is permissible to thin the primer by adding 1 part by volume of V.M.&P. naptha to 4 parts by volume of primer. This mixture may be reused provided it is capped securely between uses and is re-strained before each use. It shall be discarded at the first sign of white residue on the primed surface.

4.4.5 Preparation of Coating Material. Dilute the approved silicone coating material in the ratio of 1 part by volume of compound to 2 parts by volume of xylene. Mix thoroughly to a uniform consistency with minimum entrapment of air. Allow mixture to stand until most of the entrapped air bubbles have disappeared.

4.4.6 Application of Coating. After primer has air dried, and immediately prior to coating, place the board to be coated in an air circulating oven at $140 \pm 4^{\circ}F/60 \pm 2^{\circ}C$ for a minimum of 15 minutes. Allow the boards to return to room temperature before coating.

Spray method. Spray coating of printed circuit assemblies shall be accomplished as follows:

a. Prepare coating material according to instructions of paragraph 4.4.5.

b. Apply a thin coat of coating material with a minimum of overlap. The assembly shall be sprayed from four directions to insure complete coverage of mounted components.

c. Inspect the coated assembly and remove all bubbles using the tip of a sharp instrument such as a needle or sharpened soldering aid.

d. Cure the coated assembly in accordance with paragraph 4.4.7.

4.4.7 Cure Coating. The coating shall be cured in accordance with either the room temperature schedule or humidified elevated temperature schedule given below.

CAUTION: HANDLING BEFORE FULL CURE MUST BE DONE WITH CARE TO AVOID CONTAMINATION OR RUPTURE OF THE COATING.

a. Room temperature. Air dry a minimum of 20 hours at room temperature and room humidity before handling. Full cure is obtained in 7 days.

b. Elevated temperature. Air dry at room temperature for 1 hour minimum, followed by curing in a humidifier circulating air oven at $167 \pm 9^{\circ}F/75 \pm 5^{\circ}C$ and 20 to 40 percent relative humidity for 16 hours minimum. Water used for humidifying the oven shall be deionized or distilled water.

4.4.8 Cleaning. Masking materials shall be removed as follows: Remove all masking materials and clean the board fingers with a sharpened wooden or similar nonscratching tool, if required, to remove traces of coating material. To prevent lifting of the coating adjacent to masked areas, a scalpel or razer blade

may be used to cut the coating before removing the masking material. Extreme care must be exercised so as not to cut the circuitry, score the board material or thermal planes, or otherwise damage the workpiece. Replace the unit in its anitistatic packaging envelope.

NOTE: Brushes, holding fixtures, and other implements subjected to the coating material must be cleaned promptly after use. Place a tray of xylene in the vented coating station and brush clean nonmetallic items. Metal items may be soaked in xylene, but do not allow brushes to remain in xylene more than a few minutes. Discard contaminated xylene. When cleaning tools and containers associated with primer, use acetone as the preferred cleaner or xylene as an alternate.

5.0 QUALITY ASSURANCE PROVISIONS.

5.1 WORKMANSHIP. Parts or assemblies shall be coated as defined herein. The coating shall conform to the contour of the parts. Occasional small well-scattered bubbles or blisters up to .015 inch in the greatest dimension, and not bridging conducting lines, leads, or surfaces, nor penetrating from the outer surface to the substrate are acceptable. Complete coverage will be determined by visual examination of completed assemblies using ultraviolet light.

5.1.1 Inspection. Each coated assembly shall be inspected for conformance to the following inspection criteria. The criteria below do not apply to insulated wire portions of the assembly.

5.1.2 Acceptance Criteria. An acceptable coated assembly must meet the following requirements:

a. Coating shall be uniform in color.

b. Coating surface shall be tack-free.

c. Coating shall be continuous and present a smooth, ripple-free surface.

d. Coating shall adhere to the printed circuit board.

e. Coating shall be uniform in thickness and in the range of .001 to .007 inch (as determined by measurements on a test sample), with no excessive buildup around components.

f. On units using wire-wrapped pins, coating buildup (ripple) of conformal coating on the end of pins is expected and acceptable.

5.1.3 Rejection Criteria. The following characteristics of coated assemblies are not acceptable:

a. Entrapped air bubbles which exceed 0.015 inch in the greatest dimension.

b. Groups of two or more bubbles less than 0.015 inch in diameter within any 1 square-inch area.

c. Bubbles contacting conductive materials, or any void which exposes the surface of conductive material.

Dow Corning 3140 RTV Data Sheet

Information About High Technology Silicone Materials

DOW CORNING

Now Contains Ultraviolet Indicator

DESCRIPTION

DOW CORNING® 3140 RTV coating is a self-leveling, ready-to-use, room-temperature-vulcanizing silicone rubber. No corrosive by-products are generated during its cure. As a result, DOW CORNING 3140 RTV coating can be used in corrosion-sensitive electrical/electronic equipment with no adverse effect.

DOW CORNING 3140 RTV coating is a clear material and allows easy visual component identification, inspection and repair. Its good tear strength and toughness make it well-suited for applications requiring ruggedness and high durability. Other important features include:

- Ease of processing – no mixing; no heating; no exothermic heat during cure; no solvent hazard
- Noncorrosive to copper and other sensitive metals
- Good dielectric properties over a wide temperature range
- Remains rubbery from -55 to 200 C (-67 to 392 F)
- Easy to repair by cutting away old material and replacing with new material
- Resistant to harsh environments such as ozone, corona, moisture and weathering
- Meets requirements of MIL-I-46058C and MIL-A-46146
- Recognized by Underwriter Laboratories for service to 180 C (365 F) when used in minimum thicknesses of 0.075 inch
- Recognized by Underwriters Laboratories as a conformal coating on PC boards

DOW CORNING® 3140 RTV COATING

Type	One-part solventless silicone rubber
Physical Form	Ready-to-use viscous liquid
Cure	24 to 72 hours at 25 C (77 F) and 20 percent relative humidity
Special Properties	Noncorrosive; self-leveling
Primary Uses	Dielectric coating for electrical and electronic equipment

TYPICAL PROPERTIES

These values are not intended for use in preparing specifications.

As Supplied		
CTM[1] 0050	Viscosity, poise	350
	Coating Thickness, mils per dip	15
CTM 0098	Skin-Over Time, minutes	25
CTM 0095	Tack-Free Time, hours	1.5
CTM 0084	Cure Time, 25 mils, hours	24
	Cure Time, 0.125-inch thickness, hours	72
	Full Cure, 0.125-inch thickness, days	7
CTM 0010	Nonvolatile Content, percent	97
	Thick Section Cure	Good
As Cured[2] – Physical		
CTM 0176	Appearance	Clear
CTM 0022	Specific Gravity, at 25 C (77 F)	1.05
CTM 0099	Durometer Hardness, Shore A, points	22
CTM 0137A	Tensile Strength, psi	300
CTM 0137A	Elongation, percent	350
CTM 0159A	Tear Strength, Die B, ppi	20
CTM 0293	Peel Strength, primed aluminum, ppiw	24
CTM 0562	Volume Expansion, 25 to 100 C (77 to 212 F), cc/cc-C	8.8×10^{-4}
As Cured[2] – Electrical		
CTM 0114	Dielectric Strength, volts/mil	500
CTM 0249	Volume Resistivity, ohm-cm	5×10^{14}
CTM 0112	Dielectric Constant, at 25 C (77 F)	
	100 Hz	2.64
	100 kHz	2.63
CTM 0112	Dissipation Factor, at 25 C (77 F)	
	100 Hz	0.0016
	100 kHz	0.0004

[1]In most cases, CTMs (Corporate Test Methods) correspond to standard ASTM tests. Copies of CTMs are available upon request.

[2]After 5 days at 25 C (77 F) and 50 percent relative humidity.

Specification Writers: Please contact Dow Corning Corporation, Midland, Michigan, before writing specifications on this product.

• Contains ultraviolet indicator for ease in inspection under a black light

USES

DOW CORNING 3140 RTV coating is primarily used as a conformal coating on printed circuit assemblies and electronic components. It is also ideal for encapsulating small circuits or connectors.

HOW TO USE

DOW CORNING 3140 RTV coating should be applied to clean, dry surfaces. A satisfactory bond will usually result on clean surfaces without using a primer. For maximum adhesion, however, use DOW CORNING® 1204 primer or DOW CORNING® 1205 prime coat.

Surface Preparation

Clean and degrease all metal and plastic surfaces. Then wipe or rinse all surfaces, except acetate plastics, with acetone. Rubber surfaces should be roughened with sandpaper and wiped with acetone.

Apply recommended primer to areas where maximum adhesion is desired, and allow the prime coat to dry as directed on the prime coat technical bulletin. Silicone rubber substrates need not be primed, but should be cleaned and roughened.

Application

DOW CORNING 3140 RTV coating may be applied by dipping, brushing, spraying or flow coating. To apply a conformal coating by dipping, immerse the circuit board or assembly into the silicone rubber slowly to avoid entrapment of air bubbles. Withdraw the assembly and allow excess rubber to drain back into dip tank. Position assemblies with sharp points down during curing for best point coverage.

To apply DOW CORNING 3140 RTV coating by spraying, it may be necessary to lower the viscosity by adding solvent. Any solvent of suitable volatility, such as xylene, can be used if it is free of moisture.

CAUTION: When using solvents, provide adequate ventilation. Follow all precautions given on solvent containers.

The coating can be cut away with a sharp knife for repair or modification. To aid the removal of coating, soak the coated unit in toluene or similar aromatic solvents. This will cause swelling and deterioration of the coating.

Localized areas on circuit boards or components can be coated by applying DOW CORNING 3140 RTV coating directly from its collapsible container. The material will flow out and level to a neat, uniform coating.

Curing

Let the unit stand undisturbed at room temperature and 20 percent or higher relative humidity. The time required for proper cure will vary with the thickness of the RTV coating, the thickness of the parts being joined, and the permeability of the materials. Usually, 24 to 72 hours will suffice for thin coatings or units having one permeable member. Full bond strength will be established after approximately 7 days at room temperature.

When bonding two impermeable surfaces together, as in the case of two metal plates, cure time will depend on the thickness of the silicone rubber and the area under the joint. The larger the unexposed bond area, the longer the cure time and maximum bond strength. Keep the area enclosed by the joint to a minimum. A metal-to-metal bond, for example, should not overlap more than one inch for best results.

DOW CORNING 3140 RTV coating cures at room temperature by exposure to existing humidity in the

air. Dow Corning recommends a minimum of 20 percent relative humidity for proper cure. Less humidity will extend the curing time, and higher humidity will form a tack-free "skin" after approximately 2 hours at room temperature.

In thicknesses up to 0.125 inch, it will cure to a solid rubbery mass in 72 hours. Optimum physical and electrical properties are reached after a cure of approximately 7 days at room temperature.

DOW CORNING 3140 RTV coating will release small amounts of methanol during curing. Provide adequate ventilation in the working environment to prevent excessive methanol vapor accumulation.

SHIPPING LIMITATIONS

None.

STORAGE AND SHELF LIFE

When stored in original, unopened containers at or below 32 C (90 F), DOW CORNING 3140 RTV coating has a shelf life of 6 months from date of shipment. While refrigeration is not necessary, it may extend the useful life of this product.

Since DOW CORNING 3140 RTV coating cures upon exposure to moisture in the air, keep container sealed when not in use. A plug of cured material may form in the tip of the tube during storage. This is easily removed and does not affect the remaining contents.

PACKAGING

DOW CORNING 3140 RTV coating is supplied in 3-fl oz (89-mL), 1-pt (473-mL) and 4.5-gal (17-L) containers.

MSDS INFORMATION

ATTENTION: PRODUCT SAFETY INFORMATION REQUIRED FOR SAFE USE IS NOT INCLUDED. BEFORE HANDLING, READ PRODUCT AND MATERIAL SAFETY DATA SHEETS AND CONTAINER LABELS FOR SAFE USE, PHYSICAL AND HEALTH HAZARD INFORMATION. THE MATERIAL SAFETY DATA SHEET IS AVAILABLE FROM YOUR DOW CORNING REPRESENTATIVE, OR DISTRIBUTOR, OR BY WRITING TO DOW CORNING CUSTOMER SERVICE, OR BY CALLING 1-517-496-6000.

WARRANTY INFORMATION - PLEASE READ CAREFULLY

Dow Corning believes that the information in this publication is an accurate description of the typical characteristics and or uses of the product or products, but it is your responsibility to thoroughly test the product in your specific application to determine its performance, efficacy and safety.

Unless Dow Corning provides you with a specific written warranty of fitness for a particular use, Dow Corning's sole warranty is that the product or products will meet Dow Corning's then current sales specifications. **DOW CORNING SPECIFICALLY DISCLAIMS ANY OTHER EXPRESS OR IMPLIED WARRANTY, INCLUDING THE WARRANTIES OF MERCHANTABILITY AND OF FITNESS FOR USE.** Your exclusive remedy and Dow Corning's sole liability for breach of warranty is limited to refund of the purchase price or replacement of any product shown to be other than as warranted, and Dow Corning expressly disclaims any liability for incidental or consequential damages.

BL38854

DOW CORNING CORPORATION
MIDLAND, MICHIGAN 48686-0994

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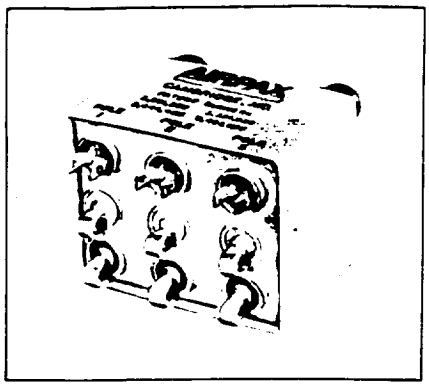
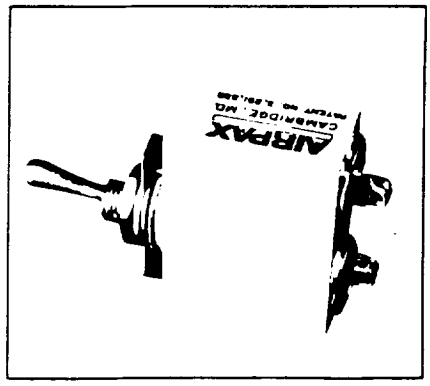
DOW CORNING

Circuit Breaker Data Sheet





Airpax AP/UP, AP-MIL Multi-Pole Circuit Breakers

Circuit demands and design ingenuity suggest a limitless number of special combinations, ranging from a two pole unit with one series breaker and a simple ON-OFF switch, to a more complex 3 pole unit having one series, one shunt and one relay configuration with auxiliary indicator circuit contacts.

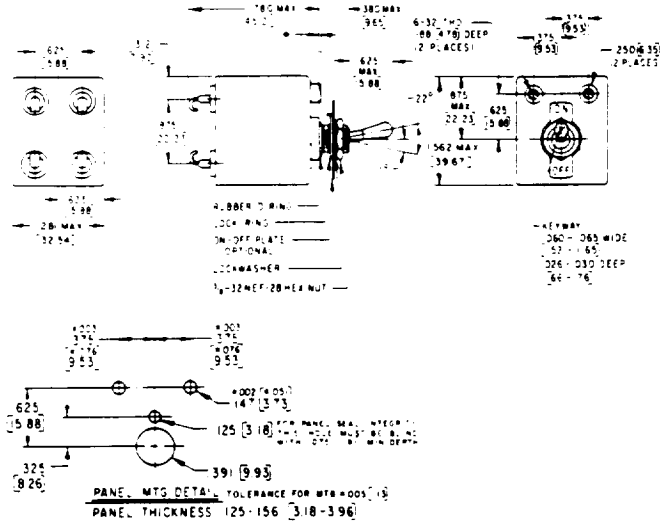
Two Pole
AP-12
Two of the basic units are combined in a hermetically sealed case to provide protection for dual circuits. A single toggle handle actuates both internal trip mechanisms. Conversely, an overload in either circuit trips both simultaneously.

The AP-12 consists of two independent series trip breakers, each available with its own rating and delay characteristics. This two pole unit can therefore have an unlimited number of combinations, which makes ordering by a code system impractical. Thus, if the poles differ, a descriptive drawing is recommended.

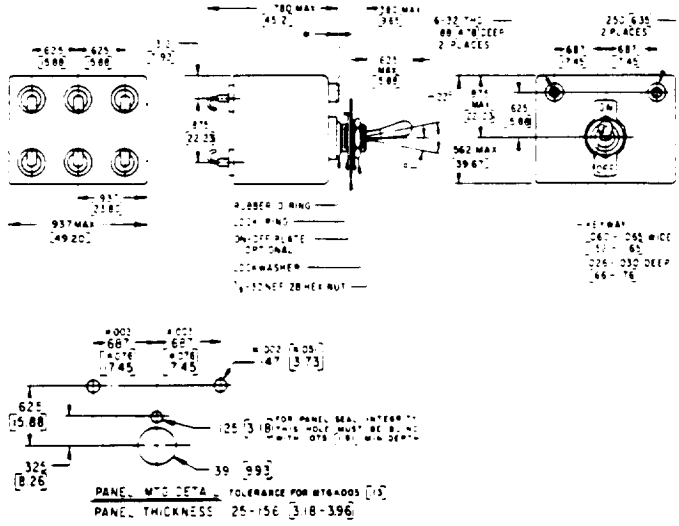
All multi-pole units have provision for a rugged three point panel mount. When the 6-32 panel seal screws are used together with the bushing mount, a level of shock and vibration in excess of the specification values can be tolerated. When the screws are not used and the bushing is secured, the bosses contact the back of the panel insuring performance to specification.

Three Pole
AP-112
Three circuits may be simultaneously protected. One actuating toggle handle closes all circuits and all poles trip in the presence of an overload on any circuit. Some typical combinations could be: 3 series poles; 2 series and one shunt; 2 series and one relay; or 3 series with a set of auxiliary contacts. Like the two pole breakers, each pole may have different ratings and delays.

Two Pole
AP-12



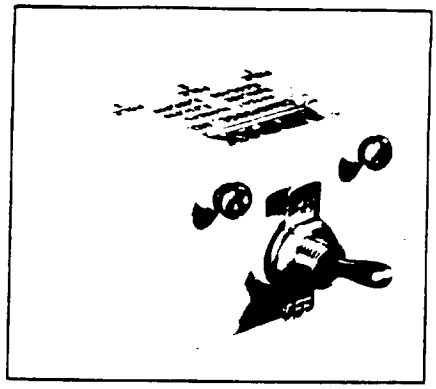
Three Pole
AP-112

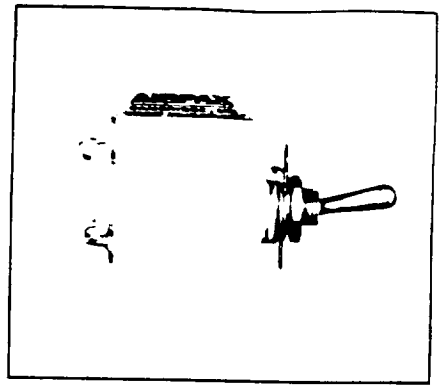


*Threaded inserts exceed seated height of bushing by .005-.015 [.13-.38]

TOLERANCE ±.031 [.79] ANGLES: ±5° UNLESS NOTED DIMENSIONS IN BRACKETS [ ] ARE MILLIMETERS

Airpax AP/UP, AP-MIL Operating Characteristics And Delay Curves





The following table provides a comparison of inrush pulse tolerance with and without the inertial delay feature for each of the 50/60Hz delays. Pulse tolerance is defined as a single pulse of half sine wave peak current amplitude of 8 milliseconds duration that will not trip the circuit breaker.

Delay	Pulse Tolerance
41, 51, 61	4 × Rated Current
41F, 51F, 61F	8 × Rated Current
64, 65	10 × Rated Current
64F, 65F	15 × Rated Current

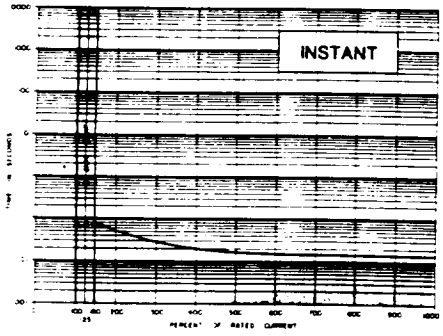
The delay curves below illustrate the improved inrush tolerance provided by delays 64 and 65 compared to standard delays, and a decision guide regarding the need for the inertial delay feature. Consult factory for further assistance.

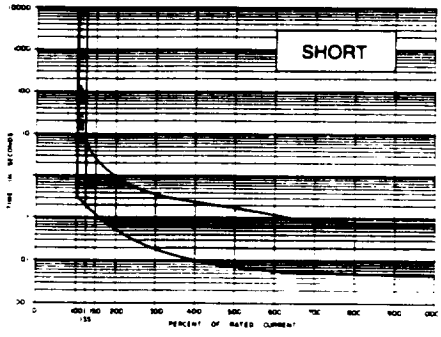
Nominal Values of Series Resistance at +25°C

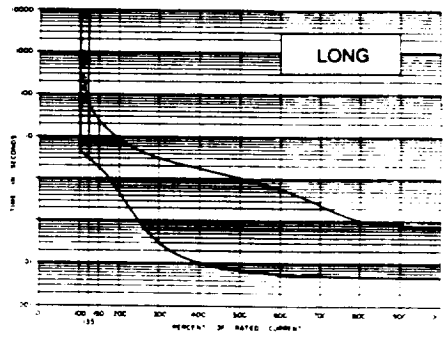
Current Ratings DC, 50/60, 400Hz	DC Series Resist. All delays except 40, 50, 60	DC Series Resist. Delays 40, 50, 60
50 ma	470 ohms	105 ohms
100	145	27 ohms
250	18	3 8 ohms
500	4 3	1 0 ohms
750	1 6	4 ohms
1 0 amps	1 15	23 ohms
2.0	2 98	06 ohms
3.0	130	033 ohms
5.0	052	012 ohms
7.5	025	007 ohms
10.0	016	006 ohms
15.0	006	005 ohms
20.0	005	004 ohms

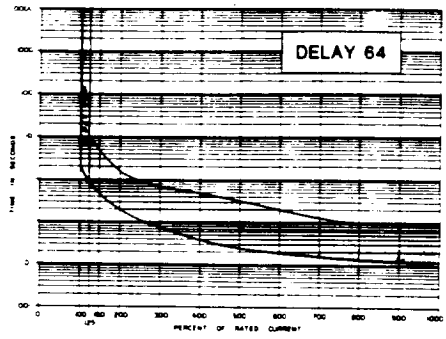
Tolerance at ±25°₀ values based on V-A method after 1 hour stabilization at 100°₀ rated current Consult factory for other limits.

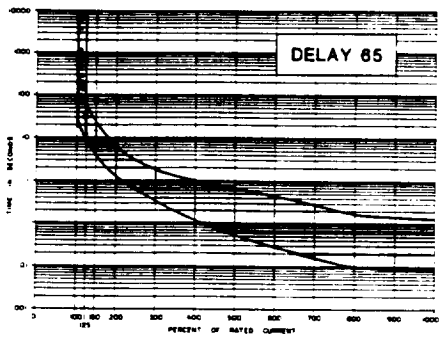
Typical Delay Curves

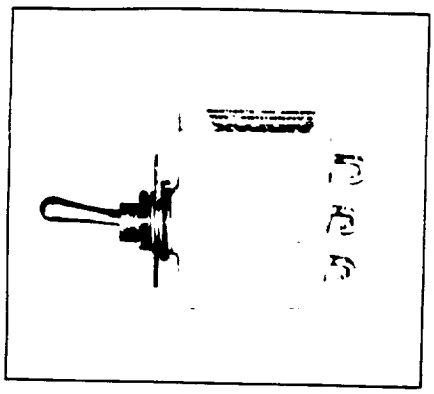


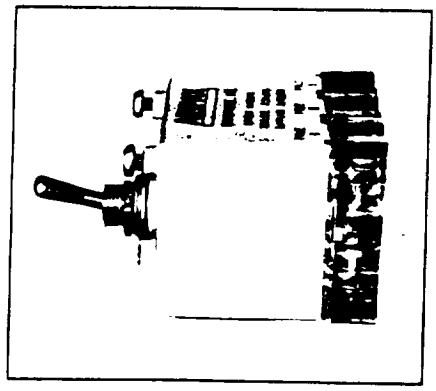












Airpax AP/UP, AP-MIL Specifications

Trip Free: AP circuit breakers will trip open on overload, even when forcibly held on. This prevents the operator from damaging the circuit by holding in the breaker.

Trip Indication: The operating handle of the breaker moves forcibly and positively to the OFF position on overload. It is not necessary to manually "reset" to full "OFF" in order to turn it on again.

Shock: All breakers withstand 100G without tripping, even while carrying full rated current, with shock applied in any plane, of 6 ms duration. Test is made according to Method 213, Test Condition 1 of MIL-Std-202 as outlined in Paragraph 4.6.14 of MIL-C-39019. Delay 40, 50, 60 breakers are tested at 90% of rated current.

Vibration: All breakers withstand vibration from 10 to 55 cycles at .06 double amplitude and 55 to 2000 cycles at 10G, applied in any plane, without damage and without tripping even while operated at full rated current. Test is made in accordance with Method 204A, Test Condition C, of MIL-Std-202 as outlined in Paragraph 4.6.12 of MIL-C-39019. Delay 40, 50, 60 breakers are tested at 90% of rated current.

Ambient Operation: The breaker will operate at any ambient between −40°C and +100°C.

Endurance: With the circuit breaker operated as an ON-OFF switch at rated current, operating life exceeds 10,000 operations at a rate of 6 per minute.

Dielectric Strength: The breaker will withstand 1250 volts RMS, 60Hz from terminals to case and between the terminals when open.

Insulation Resistance: Exceeds 100 megohms at a potential of 500Vdc.

Panel Seal: The "O" ring provided with the other illustrated hardware provides a seal against a pressure differential of 15 psi applied for an hour.

Multiple Poles: One frequent use of 2 pole breakers is to interrupt either or both sides of a power line. Likewise, 3 pole breakers often use 3 identical coils. However, any 2 or 3 pole breaker may have any coil of any delay in any desired combination. (Unless otherwise specified, we assume the 2 or 3 poles to be all alike.)

Case Seal: The breaker is fully hermetically sealed, and will not show evidence of leakage under total immersion.

Lever Strength: The operating lever or its seal will not be damaged by a 10 lb. force applied in any direction.

Short Circuit Capacity: When tested in accordance with the procedures of UL1077, AP breakers have a short circuit capacity of 1000 amperes at 32Vdc, 120Vac, 240Vac, 60 or 400Hz. Parts are not recognized to UL1077 for type UPI.

The rated Rupture Capacity per MIL-C-39019 is 500 amperes, 50 volts DC, 500 amperes, 120 volts AC and 300 amperes, 240 volts AC, 60 or 400Hz.

Ratings: AP breakers are available in current ratings from 50 milliamperes to 20 amperes, 50 volts DC or 240 volts AC maximum, 60 or 400Hz.

Contact the factory for detailed test specifications, delay curves and other current or Hz requirements.

Auxiliary Switch Ratings: 0.5 amps 50Vdc or 120Vac.

Percent of Rated Current vs Trip Time in Seconds At 25°C in Vertical Mtg. Position

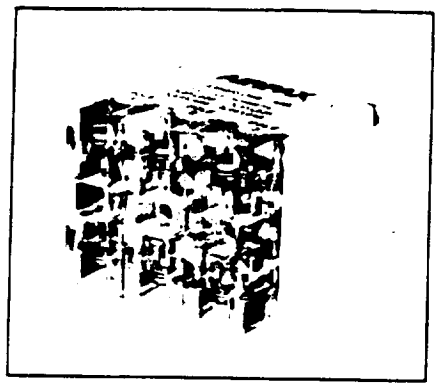
Delay	100%	125%*	200%	400%	800%
40	No Trip	.010-.035	.007-.025	.004-.015	.003-.015
41	No Trip	.2-7.0	.055-.95	.01-.24	.005-.08
42	No Trip	3-60	.5-9.0	.01-1.75	.005-.1
49	No Trip	.100 Max.	.050 Max.	.020 Max.	.015 Max.
50	No trip	.010-.035	.007-.025	.004-.015	.003-.015
51	No trip	4-4.0	.06-.6	.01-.2	.005-.035
52	No trip	4.0-40.0	.6-6.0	.01-1.5	.005-.05
59	No trip	.100 Max.	.050 Max.	.020 Max.	.015 Max.
60	No trip	.010-.035	.007-.025	.004-.015	.003-.015
61	No trip	.5-5	.07-.7	.02-.2	.008-.08
62	No trip	4.0-40.0	.8-8.0	.01-.3	.005-.08
64	No trip	.90-10.0	.20-1.7	.04-.5	.012-.100
65	No trip	9.0-60.0	1.15-7.0	.11-1.0	.010-.190
69	No trip	.100 Max.	.050 Max.	.020 Max.	.015 Max.
71	No trip	.2-7.0	.055-.95	.01-.24	.005-.08
72	No trip	3-60	.5-9.0	.010-1.75	.005-.1
79	No trip	.100 Max.	.050 Max.	.020 Max.	.015 Max.

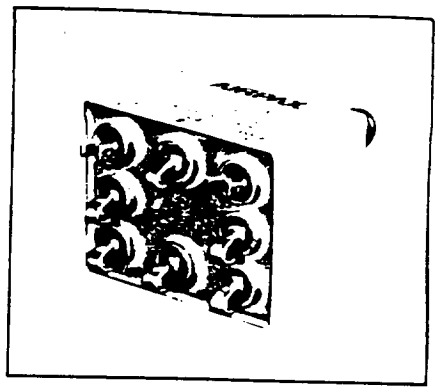
*150% for delays 40,50, & 60.
*135% minimum trip for delays 41, 42, 49, 71, 72, & 79

Approximate Weights Per Pole

oz.	grams
1.8	49

Decision Tables For Ordering Airpax AP/UP, AP-MIL Circuit Breakers





The ordering code for AP magnetic circuit breakers may be determined by following the decision steps in the tables shown here.

For example, the following is the code for a two pole AP, hook terminal, series unit, designed for operation in a DC circuit. It has a short time delay and a rating of 20 amperes. The coding given permits a descriptive part number, but with definite limitations. In the illustrated double pole example (AP-12-1-51-203), it is automatically assumed that both poles are identical. One great virtue of magnetic circuit breakers is their adaptability to complex circuits, thus variations from pole to pole become the rule rather than the exception. Descriptive drawings are recommended to avoid confusion.

Now it's your turn. To determine the ordering number for your particular AP unit, simply follow the steps shown. You may use this number to place an order or as a reference for further questions you may have.

First Decision	
Type	
AP	Hermetically sealed magnetic circuit breaker
UP (Note 1)	Underwriters' Laboratories recognized circuit breaker
AP-MIL (Note 2)	/1D through /6D QPL per MIL-C-39019B

Fourth Decision	
Hz and Delay	
40	400Hz 150% instant trip
41	400Hz short time delay
42	400Hz long time delay
49	400Hz 135% instant trip
50	DC 150% instant trip
51	DC short time delay
52	DC long time delay
59	DC 125% instant trip
60	50/60Hz 150% instant trip
61	50/60Hz short time delay
62	50/60Hz long time delay
64	50/60Hz high pulse, short time delay (50/60Hz only)
65	50/60Hz high pulse, long time delay (50/60Hz only)
69	50/60Hz 125% instant trip
74	DC, 50/60, 400Hz short time delay 135% trip
75	DC, 50/60, 400Hz long time delay 135% trip
79	DC, 50/60, 400Hz instant time delay 135% trip
For addition of inertial delay, add an "F" to any delay number.	

Notes:

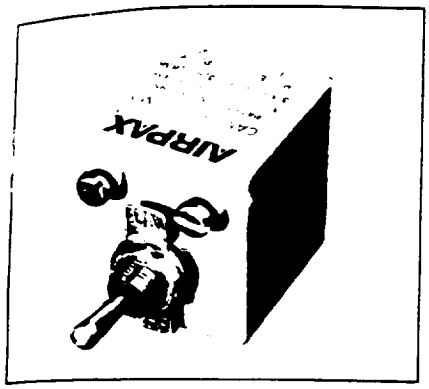
1. The UP has a wide glass terminal to meet UL and CSA creepage specifications. Except as completely non-standard, there is no space for more than two terminals and the UP is therefore limited to only the single pole series circuit configuration (Third Decision Table, — 1). Delays available in the UP are:
   40, 50 and 60
   41, 51 and 61
   42, 52 and 62

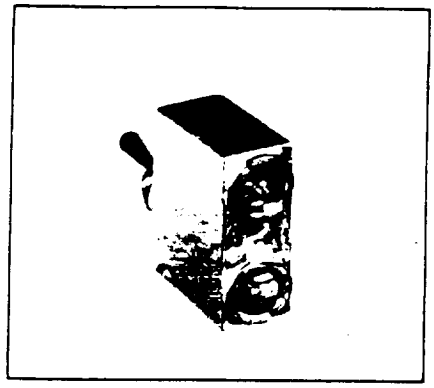
2. Users should refer to the applicable drawings of MIL-C-39019. The 6-32 threaded mounted bushings, useful for added strength, are approved under this specification.

Parts ordered to MIL-C-39019/1B through 6B are covered by main specification MIL-C 39019A, and carry dash numbers 1 through 123.

Parts ordered to MIL-C-39019/1C through 6C are covered by main specification MIL-C-39019B, and carry dash numbers 200 through 259.

Parts ordered to MIL-C-39019/1D through 6D are covered by main specification MIL-C-39019B, amendment 2, and cover dash numbers 200 through 259 as well as the new 300 series dash numbers. There are some impor-





Decision Tables For Ordering Airpax AP/UP AP-MIL Circuit Breakers

Second Decision (Note 3)		
Poles		
Hook Terminals	Screw Terminals	
−1	−7	Single pole unit mounted with ⅜ threaded bushing
−12	−17	Two pole unit, bushing plus (2) 6-32 threaded inserts
−112	−117	Three pole unit, bushing plus (2) 6-32 threaded inserts

Third Decision	
Internal Configurations	
−0	Switch Only (Omit 4th and 5th Decisions)
−1	Series
−1R (Note 4)	Series with Auxiliary Switch with pierced pin terminals
−1RC (Note 4)	Series with Auxiliary Switch with cane hook terminals
−3	Shunt
−4	Relay (5 amps max coil rating)

Multipole units with mixed construction, poles numbered left to right when viewed from terminal end. (Note 6)

AP-12-1-51-203

Fifth Decision (Note 5)			
Nominal Amperage Rating			
Code	Amperes	Code	Amperes
−051	.050	−252	2.500
−101	.100	−302	3.000
−201	.200	−502	5.000
−251	.250	−702	7.000
−401	.400	−802	8.000
−601	.600	−103	10.000
−751	.750	−123	12.000
−102	1.000	−153	15.000
−1251	1.250	−1752	17.500
−1751	1.750	−203	20.000
−202	2.000		

See page 57 for maximum voltage ratings.

Mil II P/N #:
AP-12-1-52-502

tant differences within these three revisions. To assure that proper parts are received, consult the factory for application assistance if there is any doubt about which version is correct for the application concerned.

3. Screw terminals are available. Space permits their use only in the series configuration (Third Decision Table). Standard terminals are heavy copper hooks.

4. The SPDT auxiliary switch, available only with the series circuit, may have "R" soldering terminals, flattened and pierced, or "RC" soldering terminals which are cane hooks.

5. The nominal current values for 100% of rated current (see delay curves) are those listed. Other values can be readily supplied, in general, without delayed delivery. For values above or below the listed range, please consult an Airpax sales office or sales representative. For UP maximum ratings see page 57.

6. Consult factory for assigned part numbers.

PTC Fuse Data Sheet

Raychem

RDE FAMILY

PTC Resistance Devices for Circuit Protection

Overcurrent and overtemperature protection
The PolySwitch circuit protector is a positive temperature coefficient (PTC) resistor that undergoes a large, abrupt change in resistance when an overcurrent or high temperature heats it above a specific point.

Normally just tens of milliohms, the resistance of the PolySwitch protector increases orders of magnitude when switched. This increase limits current to several milliamps.

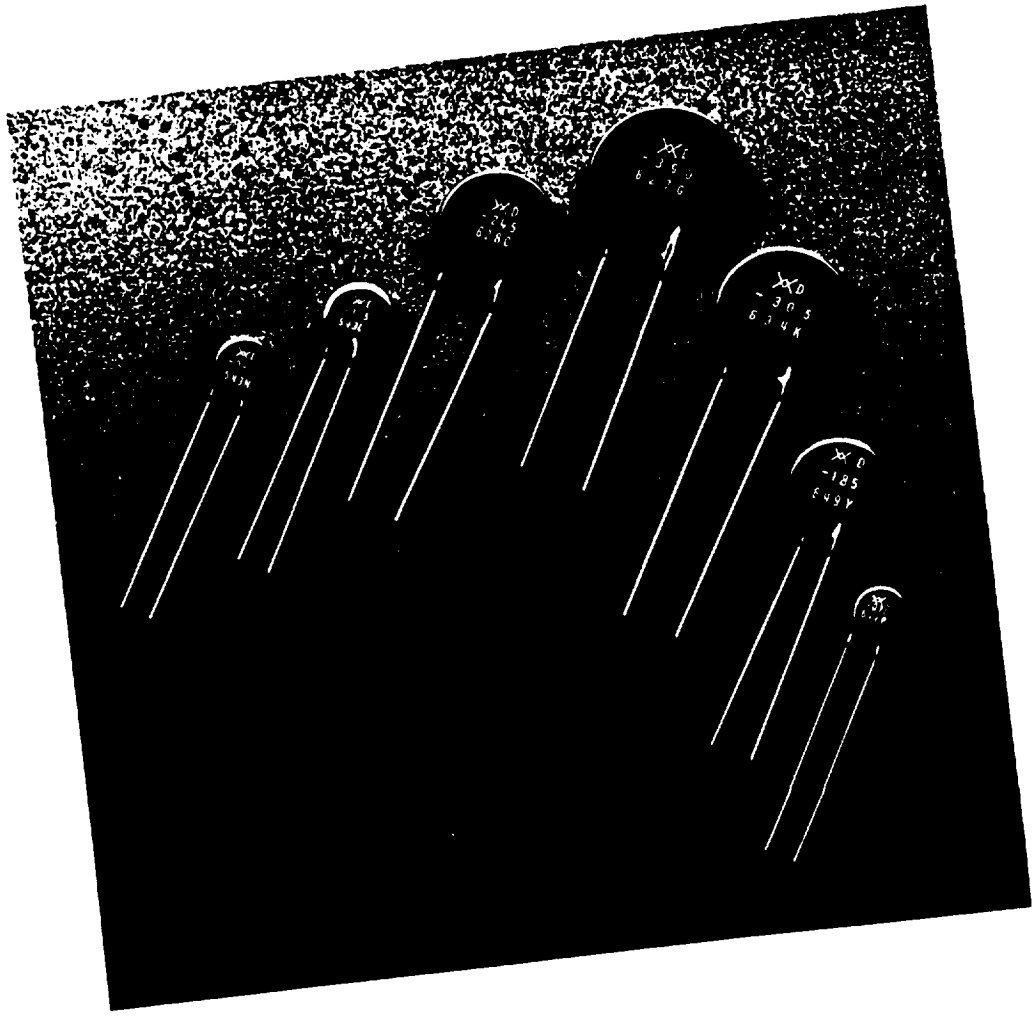
Remotely resettable
When the current or temperature fault that caused the device to switch has been substantially reduced, the PolySwitch device resets, allowing normal circuit operation to resume. The protector requires no manual resetting or replacement.

Latching (noncycling) operation
After switching, the PolySwitch device is latched into its high-resistance, protective state by the small, sustained self-heating current. The protector will reset only after it has cooled and the fault condition has been corrected, thus avoiding continuous cycling that could cause circuit damage.

Rugged monolithic construction
Since they are made from solid-state material, PolySwitch devices have no moving parts that can be damaged.

Versatile, UL-recognized components
PolySwitch protectors can be mounted on PC boards for easy use in many circuits. The devices are FR-encapsulated (UL 94V-0) for electrical insulation. They are recognized under UL file number E74889.

Wide variety of applications
Possible applications for PolySwitch devices include:
- *audio speakers*
- *batteries*
- *motors*
- *power supplies*
- *transformers*
- *solenoids*



. Distributor ≈ ACACA (617) 547-0577
Insulation supplies 452-8580

Maximum operating characteristics

Maximum operating voltage	50V (RMS)
Maximum interrupt current	40 amperes
Maximum interrupt cycles	500
Temperature range: operating	0° to 70°C
storage	−40° to 70°C

Maximum surface temperature in tripped state	125°C
Nominal reset time* (after power removed)	< 20 seconds (at 20°C)
Device resistance in tripped state*	V^2/P_d

*Note: Device will automatically reset when $V^2/4R_L < P_d$, where R_L is load resistance, V is circuit voltage, P_d is power dissipation in tripped state.

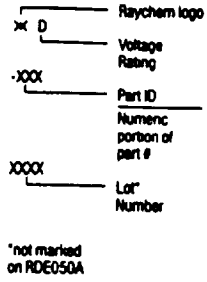
Electrical characteristics (20°C)

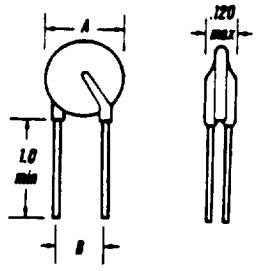
Part number	I_H (amps)	R nom. (Ω)	P_d typ. (watts)	R min. (Ω)	R max. (Ω)
RDE050A	.50	.423	1.4	.360	1.13
RDE070A	.70	.259	1.6	.220	.649
RDE090A	.90	.177	1.8	.150	.412
RDE115A	1.15	.123	1.9	.105	.275
RDE135A	1.35	.093	2.1	.079	.209
RDE185A	1.85	.059	2.4	.050	.122
RDE245A	2.45	.039	2.8	.033	.083
RDE305A	3.05	.030	3.2	.025	.062
RDE390A	3.90	.021	3.7	.018	.044

Dimensions

A max. (in.)	B nom. (in.)
.300	.2
.380	.2
.445	.2
.510	.2
.570	.2
.695	.2
.835	.4
.975	.4
1.120	.4

Part Marking





I_H = Hold Current Typical Trip Current (I_T) = 2 x I_H P_d = Typical Power Dissipated in Tripped State Tripped State = High Resistance Equilibrium R(max) = 1 Hour After Trip

1.93 2 weeks

Insulating material: cured, flame-retarded epoxy polymer meets UL 94V-0 requirements

Lead material: 20 AWG, Sn plated Cu 0.032 ± 0.002 inches

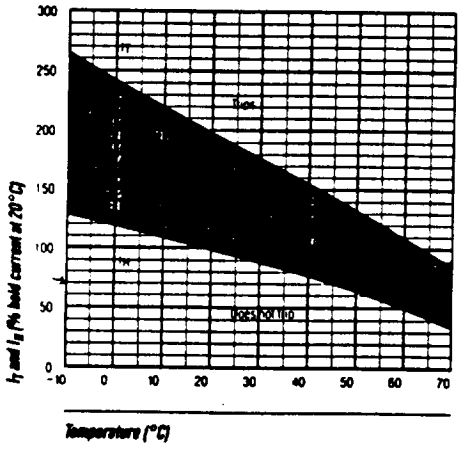
Solderability per MIL-STD-202, Method 208D

Solder heat withstand per MIL-STD-202, Method 210, Condition B

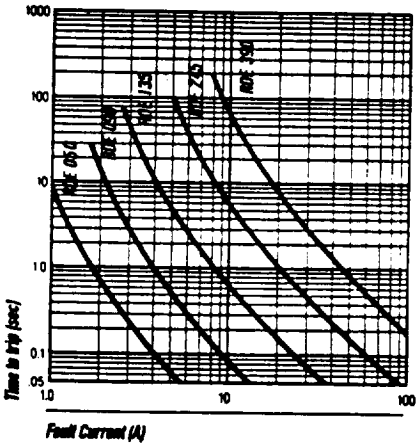
Solvent resistance per MIL-STD-202, Method 215B

Caution:
Operation beyond maximum ratings may result in rupture of the device and possible electrical arcing and flame.

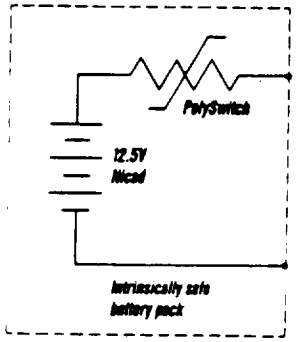
Typical thermal derating

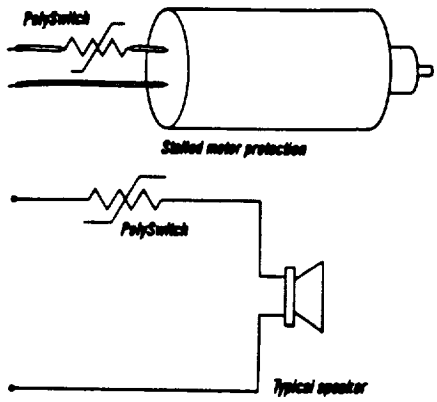


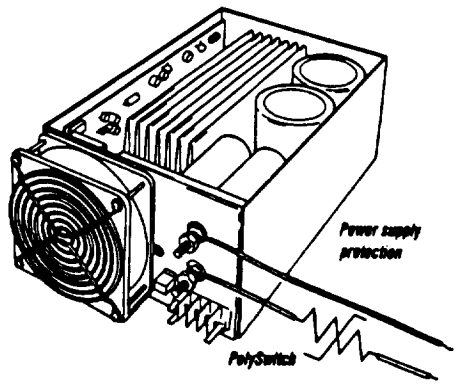
Typical trip time (20°C)



Application examples







Raychem Corporation
PolySwitch Products
300 Constitution Drive
Menlo Park, California 94025-1164
415) 361 6900 TWX 910 373 1728

Raychem

PolySwitch® Products

Standard Product List

PART #	MAXIMUM VOLTAGE	—RATED CURRENT— (amps) HOLD	TRIP	MAX	NOMINAL R (ohms)	RECOGNIZED BY	PACKAGE NUMBER	W (in)	H (in)
20901S	9	1.640	2.700	100.0	0.05		1	0.94	0.42
21412	15	2.000	3.500	100.0	0.04		1	0.83	0.41
21413	15	3.500	5.500	100.0	0.02		1	1.10	0.51
20547	15	0.550	1.100	40.0	0.31	UL	3	.31	.30
RBE085A	15	0.850	1.660	40.0	0.21	UL	3	.29	.31
RBE110A	15	1.100	2.130	40.0	0.13	UL	3	.37	.39
RBE130A	15	1.300	2.540	40.0	0.09	UL	3	.43	.45
RBE165A	15	1.650	3.040	40.0	0.06	UL	3	.50	.52
RBE205A	15	2.050	3.770	40.0	0.05	UL	3	.56	.56
RBE270A	15	2.700	4.960	40.0	0.03	UL	3	.69	.71
RBE360A	15	3.600	6.480	40.0	0.02	UL	3	.83	.85
RBE460A	15	4.600	8.160	40.0	0.02	UL	3	.97	.99
RBE570A	15	5.700	10.000	40.0	0.01	UL	3	1.10	1.12
RBE885A	15	8.850	15.600	40.0	0.01	UL	3	1.40	1.42
RDE050A	50	0.500	1.100	40.0	0.42	UL	3	.29	.31
RDE070A	50	0.700	1.400	40.0	0.26	UL	3	.37	.39
RDE090A	50	0.900	1.780	40.0	0.18	UL	3	.43	.45
RDE115	50	1.150	2.200	40.0	0.12	UL	3	.50	.52
RDE135A	50	1.350	2.600	40.0	0.09	UL	3	.56	.56
RDE185A	50	1.850	3.430	40.0	0.06	UL	3	.69	.71
RDE245A	50	2.450	4.620	40.0	0.04	UL	3	.83	.85
RDE305A	50	3.050	5.690	40.0	0.03	UL	3	.97	.99
RDE390A	50	3.900	7.350	40.0	0.02	UL	3	1.10	1.12
RXE017	60	0.170	0.260	40.0	4.85	UL	4	.21	.48
RXE020	60	0.200	0.300	40.0	2.67	UL	4	.18	.46
RXE025	60	0.250	0.380	40.0	1.83	UL	4	.19	.48
RXE030	60	0.300	0.450	40.0	1.27	UL	4	.22	.49
RXE040	60	0.400	0.600	40.0	0.81	UL	4	.27	.52
RXE050	60	0.500	0.750	40.0	0.75	UL	4	.28	.54
RXE065	60	0.650	0.980	40.0	0.46	UL	4	.33	.55
RXE075	60	0.750	1.130	40.0	0.39	UL	4	.37	.58
RXE090	60	0.900	1.350	40.0	0.34	UL	4	.40	.60
RXE110	50	1.100	1.650	40.0	0.21	UL	3	.46	.48
RXE135	50	1.350	2.050	40.0	0.18	UL	3	.53	.55
RXE160	50	1.600	2.400	40.0	0.14	UL	3	.60	.62
RXE185	50	1.850	2.800	40.0	0.12	UL	3	.65	.67
RXE250	50	2.500	3.750	40.0	0.08	UL	3	.78	.80
RXE300	50	3.000	4.500	40.0	0.06	UL	3	.90	.92
RXE375	50	3.750	5.630	40.0	0.04	UL	3	1.03	1.23
21160	120	0.280	0.470	3.0	4.60	UL	4	.32	.81
20963	250	0.110	0.165	3.0	16.50	UL	4	.42	.48
21104A	250	0.145	0.220	3.0	8.50	UL	4	.42	.48
21017	300	0.069	0.104	0.50	33.50	UL	4	.44	.41
21091	600	0.069	0.104	0.66	33.50		2	.41	.49
21072	600	0.100	0.160	0.86	17.00		2	.41	.49
21214B	600	0.145	0.220	1.0	8.50		2	.41	.49

Lithium Battery Data Sheet

Diversified Technology
An Ergon Co.

COMPONENT SPECIFICATION

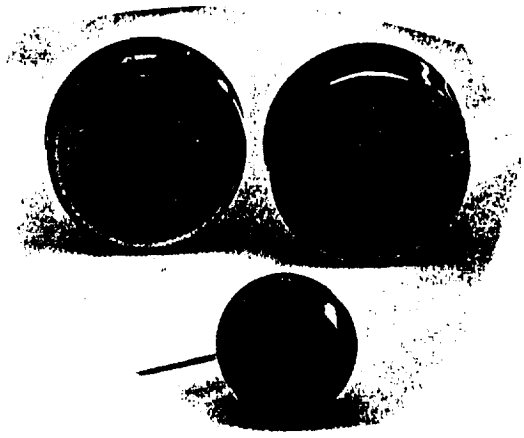
COMPONENT SPECIFICATION NO. 600000405

DESCRIPTION 3.6 V Battery

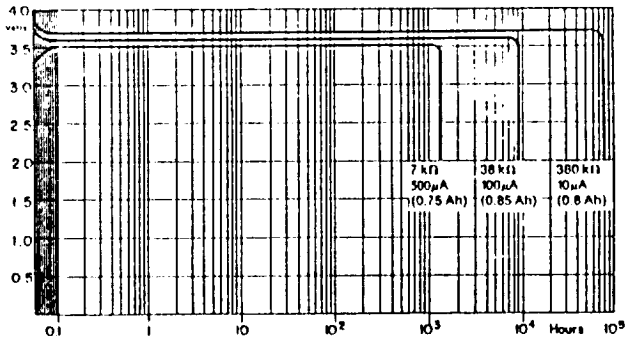
Manufacturer Data

Tadiran - TL5186

DO NOT accept Batteries with a date code older than one (1) year!!



Typical Discharge Characteristics (at 25°C)
Memory Back-up Cell



Cell Features

- [ ] **Stable voltage:** 3.6 V
- [ ] **Leakproof:** hermetic sealing
- [ ] **Long Life:** Less than 1% self discharge/year
- [ ] **Wide temperature range:** –55°C to +85°C
- [ ] **UL recognized:** File No. MH 12193
- [ ] **Concentrated energy:** up to 420 Wh/kg

Diversified Technology
An Ergon Co.

COMPONENT SPECIFICATION

COMPONENT SPECIFICATION NO. 600000405

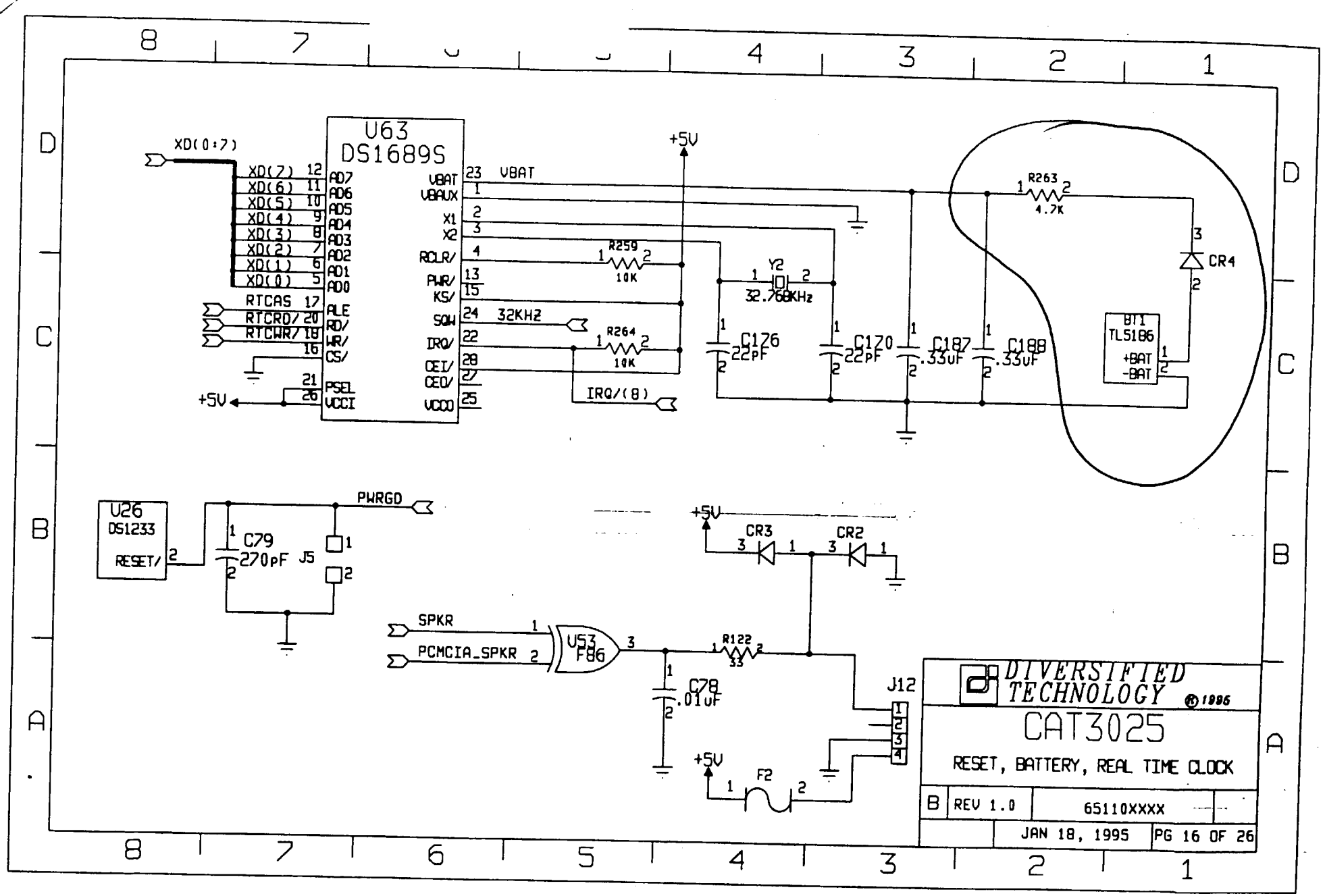
DESCRIPTION 3.6 V Battery

Recognized under the Component Program of Underwriters Laboratories Inc. File #MH 12193

PRODUCT LIST

Designation Model No.	Type	Catalog No.	Max. Capacity mAh	Dimensions mm(inch)	UL Component Recognition MH 12193	Terminals
Xtra Cells						
TL-2150	1/2AA/S	15-51-02-215-000	750	ø14.7×25.2(ø0.57×1.0)	Yes	Pressure Contact
	1/2AA/T	15-51-02-315-000				Flat Tab
	1/2AA/P	15-51-02-415-000				Axial Pin
TL-2100	AA/S	15-51-03-215-000	1800	ø14.7×50.5(ø0.57×2.0)	Yes	Pressure Contact
	AA/T	15-51-03-315-000				Flat Tab
	AA/P	15-51-03-415-000				Axial Pin
TL-2200	C/S	15-51-20-215-000	5200	ø26.0×50.5(ø1.0×2.0)	Yes	Pressure Contact
	C/T	15-51-20-315-000				Flat Tab
TL-2300	D/S	15-51-30-215-000	13500	ø32.9×61.3(ø1.3×2.4)	Yes	Pressure Contact
	D/T	15-51-30-315-000				Flat Tab
TL-5137	DD/S	15-51-37-215-000	27000	ø32.9×122(ø1.3×4.8)	No	Pressure Contact
	DD/T	15-51-37-315-000				Flat Tab
Medium Power Cells						
TP-5830	D/T	15-58-30-310-000	14000	ø33.8×61.3(ø1.3×2.4)	Yes	Flat Tab
TP-5820	C/T	15-58-20-310-000	5500	ø26.0×50.5(ø1.0×2.0)	Yes	Flat Tab
Memory Back-up Cells						
TL-5101	1/2AA/S	15-51-01-210-000	850	ø14.7×25.2(ø0.57×1.0)	Yes	Pressure Contact
	1/2AA/T	15-51-01-310-000				Flat Tab
	1/2AA/P	15-51-01-410-000				Axial Pin
TL-5104	AA/S	15-51-04-210-000	1900	ø14.7×50.5(ø0.57×2.0)	Yes	Pressure Contact
	AA/T	15-51-04-310-000				Flat Tab
	AA/P	15-51-04-410-000				Axial Pin
TL-5135	1/6D/P	15-51-35-420-000	1500	ø32.9×10.0(ø1.3×0.4)	Yes	Plug In
TL-5134	1/10D/P	15-51-34-420-000	1000	ø32.9×7.0(ø1.3×0.28)	Yes	Plug In
TL-5186	BEL/P	15-51-86-420-000	370	ø22.5×7.0(ø0.9×0.28)	Yes	Plug In
	BEL/B	15-51-86-200-000		ø24.0×24.0(ø0.94×0.94)	Yes	Plug In
	BEL/SM	15-51-86-300-000		ø24.0×24.0(ø0.94×0.94)	Yes	SMT
High Temperature Cells (150 C)						
TL-5526	C/T	15-55-26-31-000	4500	ø26×50.5(ø1.0×2.0)	No	Flat Tab
TL-5551	D/T	15-55-55-31-000	10000	ø33×61.5(ø1.3×2.4)	No	Flat Tab
TL-5576	DD/T	15-55-76-31-000	22000	ø33×125(ø1.3×4.9)	No	Flat Tab
***Battery Assemblies*						
TL-5242/W		15-52-42-40-000	3.6V	0.7×0.6×2.4	Yes	
TL-5253/C		15-52-53-30-000	6.8V	0.8×1.5×2.3	Yes	
TL-5280		15-52-80-20-000	7.2V	0.8×1.5×2.3	Yes	
TL-5293/W		15-52-93-30-000	6.0V	0.8×1.5×2.3	Yes	

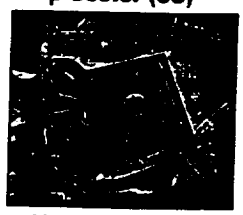
**Additional types of battery assemblies are available.


U63
DS1689S
XD(0:7)
XD(7) 12 AD7
XD(6) 11 AD6
XD(5) 10 AD5
XD(4) 9 AD4
XD(3) 8 AD3
XD(2) 7 AD2
XD(1) 6 AD1
XD(0) 5 AD0
RTCAS 17 ALE
RTCRD/ 20 RD/
RTCWR/ 18 WR/
16 CS/
21 PSEL
26 VCCI
23 VBAT
1 VBAUX
2 X1
3 X2
4 RCLR/
13 PWR/
15 KS/
24 SQW 32KHZ
22 IRQ/
28 CEI/
27 CEO/
25 VCCO
+5V
R259 10K
R264 10K
IRQ/(8)
Y2 32.768KHz
C176 22pF
C170 22pF
C187 .33uF
C188 .33uF
R263 4.7K
CR4
BT1 TL5186 +BAT -BAT
U26 DS1233 RESET/
C79 270pF J5
PWRGD
CR3
CR2
SPKR
PCMCIA_SPKR
U53 F86
R122 33
C78 .01uF
J12
F2
DIVERSIFIED TECHNOLOGY ®1996
CAT3025
RESET, BATTERY, REAL TIME CLOCK
B REV 1.0
65110XXXX
JAN 18, 1995
PG 16 OF 26

Cooling Fan Data Sheet

SOLUTION #2

Chip Cooler (CC)

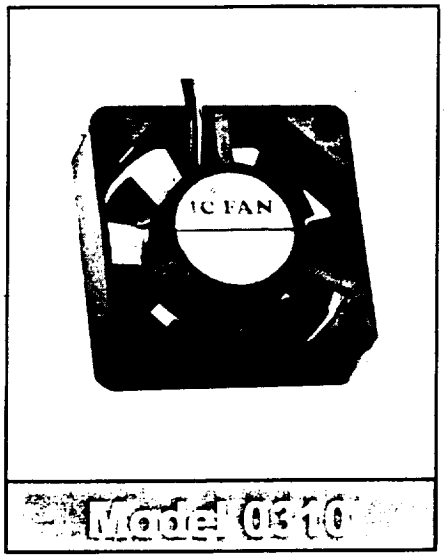


- Thinnest Chip Cooler at 10mm
- With or without Alarm
- Ball Bearing Fan
- Patented single-coil DC Brushless motor design
- Life expectancy 50,000 hours at 80 deg C
- Heat resistance 3.9 C/W
- Thermoplastic UL 94V-0
- Die cast aluminum
- 45x45x10
- Catalogs, call 714-583-9802

- Controlled flatness to insure maximum contact.
- This should be used with a thermal compound.
- To be used with 486 and Pentium processors
- Custom Designs available

SHICOH 30 x 30 x 10mm Subminiature Fan for Spot Cooling

New Product



Model 0310

A new approach to cooling:

- Locate cooling where you need it.
- Unique design provides high airflow with less power and noise.
- Integrate cooling in the initial design phase.

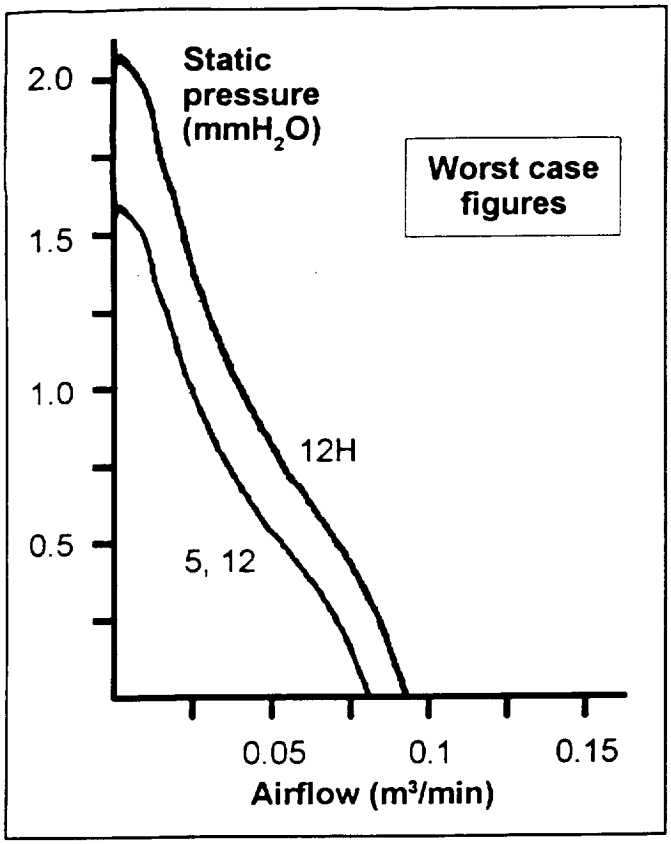
Applications: Wherever spot cooling of devices or enclosures is required.

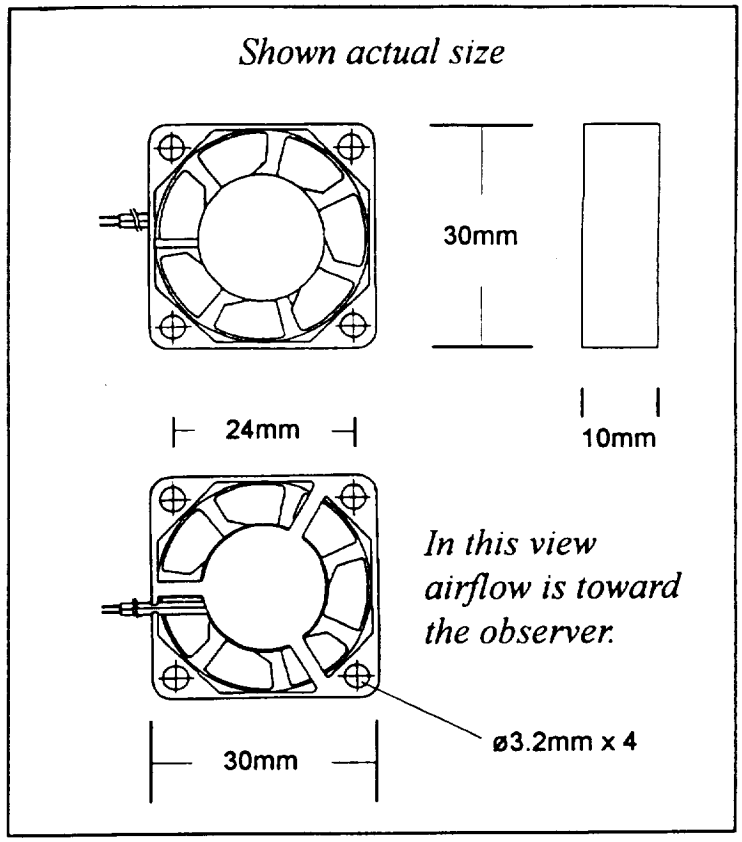
- High speed microprocessors
- Data processing equipment
- Medical electronics
- Instrumentation

Preliminary Specifications

Part number	0310–	5	12	12H						
Rated voltage	(VDC)	5	12	12						
Operating voltage range	(VDC)	4.5–5.5	10.2–13.8	10.2–13.8						
Current (worst case)	(mA)	240	120	160						
Air volume (worst case) at zero pressure	(m^3/min) (CFM)	0.08 2.82	0.08 2.82	0.09 3.18						
Static pressure (worst case) at zero airflow	(mmH_2O) (inH_2O)	1.6 0.063	1.6 0.063	2.1 0.083						
Noise (worst case)	(dB @ 1m)	26	26	28						
Initial RPM (nominal)	(RPM)	6500	6500	7500						
Operating temperature range	(°C)	–10 to +60	–10 to +60	–10 to +60						
Storage temp. range	(°C)	–40 to +70								
Weight	(grams)	Approximately 8.3								
Bearing (load bearing)		Precision sealed ball								

Specifications subject to change without notice.





Additional Specifications										
Part number	0310–	5	12	12H						
Alarm signal available										
Thermistor speed control available			Yes							
UL recognized	E131310	Pend	Pend	Pend						
CSA certified	LR92346	Pend	Pend	Pend						
Wire colors (positive / negative)		red/ green	red/ black	red/ black						
Standard wire length	(mm/inch)	122/4.8 (±10mm)								
Wire type		AWG 28, UL rated								
Voltage withstand		500 VAC for 1 minute, from leads to frame								
Specified life	(Hrs @ 25°C)	50,000 *minimum*. Data at high temperatures is available.								

Specifications subject to change without notice.

PW Fins With Fan-〈High performance Heat Sinks for LSI〉

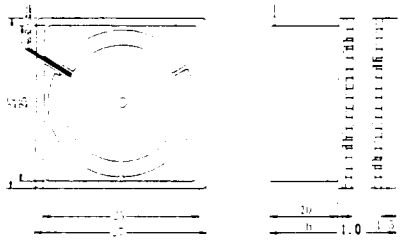
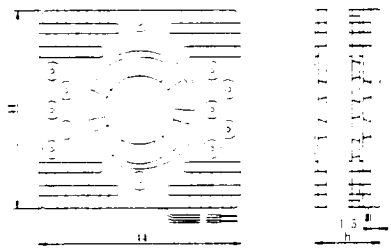
Features

Heat Sinks of Micro PW Fins and Micro Fans combined together.
Cooling unit to be mounted to LSI directly.

Attaching Method

Thermal double faced adhesive tape.
Specially designed Clamp (for PGA only).
Utilization of thermal compound between PWFins and LSI is recomended.

■Standard Products

Dimensions	Numbers for□□	Height (mm)	Weight (gram)	Fan Motor Specifiations voltage(current)	Applications
H-632-□□ Unit mm 	05	16.6	12.2	12V(80mA) 5V(90mA)	QFP, TCP (e.g. Intel i486DX4, Pentium P54C etc.)
	09	20.6	13.0		
	12	23.6	13.6		
	14	25.6	14.0		
H-617-□□ Unit mm 	31	10.0	19.5	12V(120mA)	PGA (e.g. Intel i486DX2, Pentium etc.)
	32	11.7	21.5	12V(80mA) 5V(90mA)	

Diamond Electric Mfg. Co., Ltd.
MHP Division

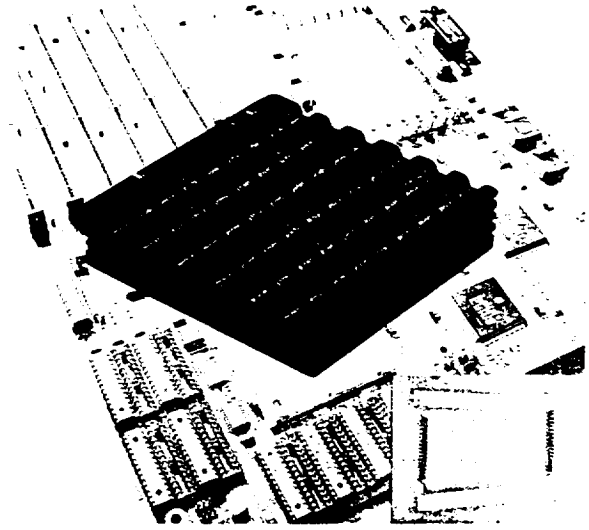
Head Office : 5-13-12 Nishinakajima, Yodogawa-ku, Osaka 532. Japan
Tel : 81-6-308 8420 Fax : 81-6-303-0832

U.S.A. Office : 110 Research Parkway Dundee, Michigan 48131 U.S.A.
Tel : (313) 529 5525 Fax : (313) 529-5359
: 160 West Santa Clara Street, Suite 800, SanJose California 95113 U.S.A.
Tel : (408) 283 0255 Fax : (408) 283-0344

PW Fins 〈High Performance Heat Sinks for LSI〉

■Features

- Design flexibility is excellent due to its manufacturing method of Pressing and Brazing Technique.
- Larger surface area due to its structure of No Thermal Conduction Post for Annular fins.
- No restriction for Cooling flow direction.
- Lightweight and very small due to the very high Heat Transfer Efficiency.
- Very useful even under hot temperature due To No soldering process.
- Thermal Resistance can be reduced by several tens percent in comparison with Pin Fins.



■Standard Products

Thickness of the pressed Fin

H-□□□-□□

Model Numbers Number of Fins including Heat Receiving Plate (e.g. −05 means 5 fins)

(Unit. mm)

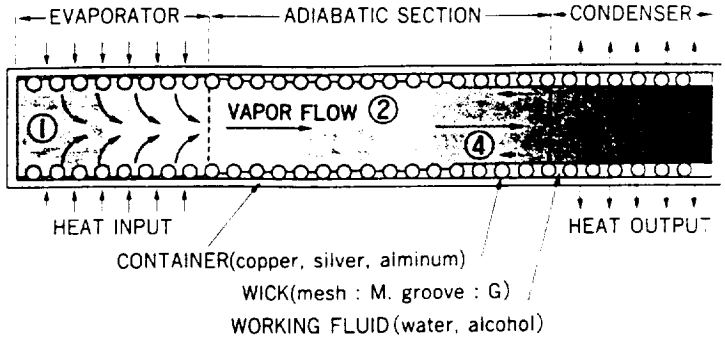
Model Numbers	Dimensions of Heat Receiving Plate	Thickness of Fin Plate	Thickness of the pressed Fin	Fin structure	Applications
H-628	20□ × 1.6 (Thick)	0.16	1.0	Staggered	
H-634	25.4□ × 1.6	0.16	1.0	Staggered	
H-635	25.4□ × 1.6	0.5	2.1	In-line	
H-624	27□ × 1.6	0.16	1.0	Staggered	Intel i486DX4
H-623	44□ × 1.6	0.5	2.1	Staggered	Intel i486DX2 Natural covection
H-621	44□ × 1.6	0.5	2.1	In-line	Intel i486DX2 Forced convection parallel to Fins
H-619	44□ × 1.6	0.5	2.1	Staggered	Intel i486DX2 Forced convection perpendicular to Fins
H-629	50□ × 3.0	0.5	2.1	staggered	Intel Pentium
H-616	54□ × 3.0	0.5	2.1	staggered	Intel Pentium
H-625	57□ × 3.0	0.5	2.1	In-line	DEC Alpha
H-633	75□ × 3.0	0.5	2.1	In-line	DEC Alpha

The electronic cooling device for your heat dissipation troubles.

What's the Micro Heat Pipes (MHP)?

Micro Hreat Pipes (MHP) are very **small** package, and **Diamond** has developed MHP for the purpose of **cooling** of semi-conductors and other electronic systems.

The principle of the operation of MHP is as follows.



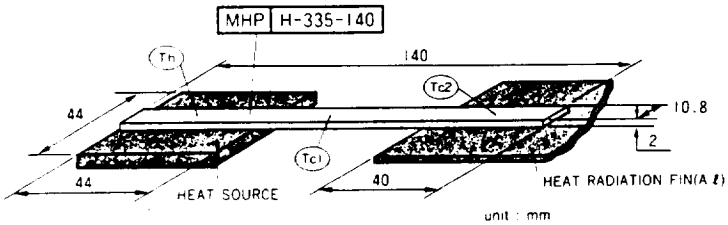
① Evaporation : absorb heat
② Vapor : high speed
③ Condensation : radiate heat
④ Return of Fluid : inside of the wall

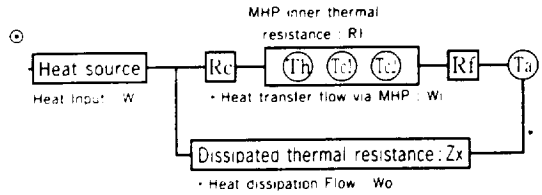
Features of MHP

- ●Thermal conductor with **great thermal conductivity**.
- ●**Better thermal response** compared with the metals.
- ●**Equaliy** on thermal distribution.
- ●**Small** size and **light** weight.
- ●No electrical or mechanical power supply required, and maintenance free.
- ●Flat series ; **Easy to fit** to any heat sources.
- ●Flat series ; It can be **mounted in a several different ways** without changing the characteristics, which is applicable to the portable electronic equipment.
- ●**Large variety of shapes** could be obtained based on the heat transfer.
- ●Combination with **PW Fins** creates many options in many usage.

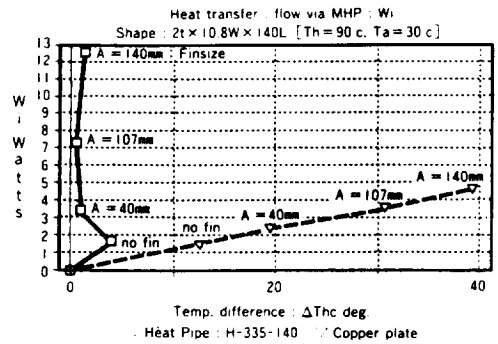
Typical characteristics of products

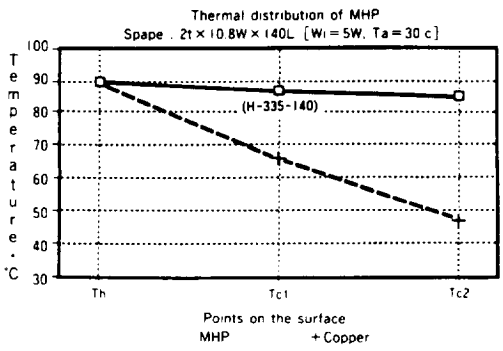
●Method of measurement.

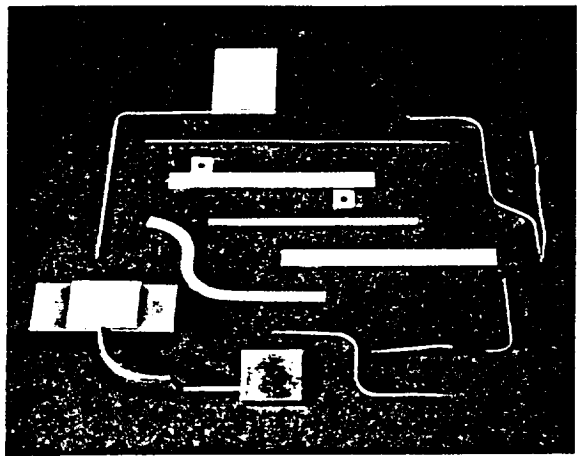




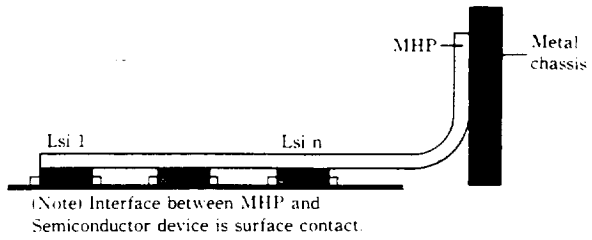
Th,Tc1,Tc2 Temperature of MHP (surface) [°C]
Ta Temperature of ambient [°C]
Rc Thermal resistance at the interface between heat source and mounting surface of MHP [°C/W]
Rf Thermal resistance between heat radiation fin and ambient [°C/W]
Wi = W-Wo [watts]
ΔThc2 = Th-Tc2 [degree]
Ri = ΔThc2/Wi [°C/W]





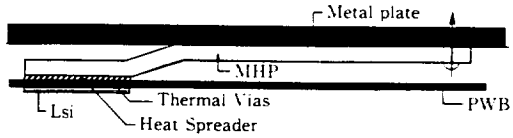


<Example 1>



(Note) Interface between MHP and Semiconductor device is surface contact.

<Example 2>



■ Standard products list

Series	Type	Dimensions(mm)			Active Length:L (mm)								
		t	W	Φd	60	80	100	120	140	150	160	180	200
Flat M	H-331-L	2	5.2	—		○	○	○					
	H-332-L	2	6.8	—		○	○	○					
	H-333-L	2	8.5	—		○	○	○	○				
	H-334-L	2	10.0	—		○	○	○	○				
	H-335-L	2	10.8	—	○	○	○	○	○				
Tube M	H-002-L	—	—	2	○	○	○	○	○	○			
	H-003-L	—	—	3	○	○	○	○	○	○	○	○	○
	H-004-L	—	—	4	○	○	○	○	○	○	○	○	○
	H-005-L	—	—	5	○	○	○	○	○	○	○		
	H-006-L	—	—	6	○	○	○	○	○	○	○		
	H-007-L	—	—	7		○	○	○					
	H-008-L	—	—	8		○	○	○					

Diamond Electric Mfg. Co., Ltd.

MHP Division

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Tel : (408) 283 0255 Fax : (408) 283 0344

Heat Shrink Data Sheet

MIL-I-23053/5B
01 May 1986
SUPERSEDING
MIL-I-23053/5A
20 May 1976

MILITARY SPECIFICATION SHEET

INSULATION SLEEVING, ELECTRICAL, HEAT SHRINKABLE, POLYOLEFIN, FLEXIBLE, CROSSLINKED

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The complete requirements for acquiring the sleeving described herein shall consist of this document and the latest issue of MIL-I-23053.

REQUIREMENTS:

Continuous operating temperature range: Classes 1 and 2: -55°C (-67°F) to +135°C (+275°F); Class 3: -25°C (-13°F) to +125°C (+257°F).

Classification: The heat shrinkable sleeving shall be furnished in the following classes, as specified (see 6.2.1):

Class 1 - Flame resistant
Class 2 - Flammable (clear only)
Class 3 - Highly flame resistant

Color: Class 2 shall be furnished in clear. Classes 1 and 3 shall be furnished in colors only. Colors shall conform to the requirements of Class 1 of MIL-STD-104.

Longitudinal change: Classes 1 and 2: ± 5 percent, overexpanded sleeving +5, -50 percent; Class 3: +1, -10 percent.

Military part number: The Military part number shall consist of the basic number of this specification sheet and dash numbers as follows:

M23053/5 - XXX - X

- X — Color designator (see 1.2.2)
- XX — Size identifier (see Table I)
- X — Class (Where no classes are specified, the numeric "0" shall be used)
- M23053/5 — Specification sheet

NOTE: Entire specifiction sheet revised.

AMSC N/A FSC 5970

DISTRIBUTION STATEMENT A, Approved for public release; distribution is unlimited.

THIS DOCUMENT CONTAINS 10 PAGES.

Example: Class 1, gray (slate), 0.250 inch (6.35 mm) as supplied ID sleeving shall be identified as M23053/5-106-8.

TABLE I. Construction details, inches (mm). 1/

Military part number 3/	As supplied ID minimum	After unrestricted shrinkage	
		ID maximum	Wall thickness 2/
Class 1			
M23053/5-101-*	.046(1.17)	.023 (.58)	.016 ± .003 (.406 ± .076)
M23053/5-102-*	.063(1.60)	.031 (.79)	.017 ± .003 (.432 ± .076)
M23053/5-103-*	.093(2.36)	.046 (1.17)	.020 ± .003 (.508 ± .076)
M23053/5-104-*	.125(3.18)	.062 (1.58)	.020 ± .003 (.508 ± .076)
M23053/5-105-*	.187(4.75)	.093 (2.36)	.020 ± .003 (.508 ± .076)
M23053/5-106-*	.250(6.35)	.125 (3.18)	.025 ± .003 (.635 ± .076)
M23053/5-107-*	.375(9.53)	.187 (4.75)	.025 ± .003 (.635 ± .076)
M23053/5-108-*	.500(12.7)	.250 (6.35)	.025 ± .003 (.635 ± .076)
M23053/5-109-*	.750(19.1)	.375 (9.53)	.030 ± .003 (.762 ± .076)
M23053/5-110-*	1.000(25.4)	.500 (12.7)	.035 ± .005 (.889 ± .127)
M23053/5-111-*	1.500(38.1)	.750 (19.1)	.040 ± .006 (1.016 ± .152)
M23053/5-112-*	2.000(50.8)	1.000 (25.4)	.045 ± .007 (1.143 ± .178)
M23053/5-113-*	3.000(76.2)	1.500 (38.1)	.050 ± .008 (1.270 ± .203)
M23053/5-114-*	4.000(101.6)	2.000 (50.8)	.055 ± .009 (1.397 ± .229)
OVEREXPANDED			
M23053/5-115-*	1.000(25.4)	.275 (6.99)	.045 ± .007 (1.143 ± .178)
M23053/5-116-*	2.000(50.8)	.550 (14.0)	.045 ± .007 (1.143 ± .178)
M23053/5-117-*	3.000(76.2)	.810 (20.6)	.045 ± .007 (1.143 ± .178)
M23053/5-118-*	4.000(101.6)	1.050 (26.7)	.045 ± .007 (1.143 ± .178)
M23053/5-119-*	1.000(25.4)	.462 (11.7)	.045 ± .007 (1.143 ± .178)
M23053/5-120-*	2.375(60.3)	.680 (17.3)	.045 ± .007 (1.143 ± .178)
M23053/5-121-*	3.000(76.2)	.840 (21.3)	.045 ± .007 (1.143 ± .178)
M23053/5-122-*	3.750(95.3)	.930 (23.62)	.045 ± .007 (1.143 ± .178)
M23053/5-123-*	4.500(114.3)	1.450 (36.83)	.045 ± .007 (1.143 ± .178)
Class 2			
M23053/5-201-C	.046(1.17)	.023 (.58)	.016 ± .003 (.406 ± .076)
M23053/5-202-C	.063(1.60)	.031 (.79)	.017 ± .003 (.432 ± .076)
M23053/5-203-C	.093(2.36)	.046 (1.17)	.020 ± .003 (.508 ± .076)
M23053/5-204-C	.125(3.18)	.062 (1.58)	.020 ± .003 (.508 ± .076)
M23053/5-205-C	.187(4.75)	.093 (2.36)	.020 ± .003 (.508 ± .076)
M23053/5-206-C	.250(6.35)	.125 (3.18)	.025 ± .003 (.635 ± .076)
M23053/5-207-C	.375(9.53)	.187 (4.75)	.025 ± .003 (.635 ± .076)
M23053/5-208-C	.500(12.7)	.250 (6.35)	.025 ± .003 (.635 ± .076)
M23053/5-209-C	.750(19.1)	.375 (9.53)	.030 ± .003 (.762 ± .076)
M23053/5-210-C	1.000(25.4)	.500 (12.7)	.035 ± .005 (.889 ± .127)
M23053/5-211-C	1.500(38.1)	.750 (19.1)	.040 ± .006 (1.016 ± .152)
M23053/5-212-C	2.000(50.8)	1.000 (25.4)	.045 ± .007 (1.143 ± .178)
M23053/5-213-C	3.000(76.2)	1.500 (38.1)	.050 ± .008 (1.270 ± .203)
M23053/5-214-C	4.000(101.6)	2.000 (50.8)	.055 ± .009 (1.397 ± .229)

TABLE I. Construction details, inches (mm). 1/ - Continued

Military part number 3/	As supplied ID minimum	After unrestricted shrinkage	
		ID maximum	Wall thickness 2/
Class 3			
M23053/5-301-*	.046(1.17)	.023 (.58)	.016 ± .003 (.406 ± .076)
M23053/5-302-*	.063(1.60)	.031 (.79)	.017 ± .003 (.432 ± .076)
M23053/5-303-*	.093(2.36)	.046 (1.17)	.020 ± .003 (.508 ± .076)
M23053/5-304-*	.125(3.18)	.062 (1.58)	.020 ± .003 (.508 ± .076)
M23053/5-305-*	.187(4.75)	.093 (2.36)	.020 ± .003 (.508 ± .076)
M23053/5-306-*	.250(6.35)	.125 (3.18)	.025 ± .003 (.635 ± .076)
M23053/5-307-*	.375(9.53)	.187 (4.75)	.025 ± .003 (.635 ± .076)
M23053/5-308-*	.500(12.7)	.250 (6.35)	.025 ± .003 (.635 ± .076)
M23053/5-309-*	.750(19.1)	.375 (9.53)	.030 ± .003 (.762 ± .076)
M23053/5-310-*	1.000(25.4)	.500 (12.7)	.035 ± .005 (.889 ± .127)
M23053/5-311-*	1.500(38.1)	.750 (19.1)	.040 ± .006 (1.016 ± .152)

1/ Diameter limits for object to be enclosed shall be as recommended in technical data.

2/ Wall thickness values are less when shrinkage is restricted.

3/ The asterisk in the part number shall be replaced by color code designations (see 1.2.2).

Unrestricted shrinkage: Test method 4.6.5: 200° ± 2°C (392° ± 4°F) for 3 minutes.

TABLE II. Physical properties. 1/

Characteristic	Requirement	Test procedure and conditions
As supplied:		
ID, minimum	Table I	4.6.3
Heat shock	No cracks, flowing or dripping	4.6.8 Classes 1 and 2: 250° ± 3°C (482° ± 6°F); Class 3: 225° ± 3°C (437° ± 6°F)
Secant modulus, psi (MPa), maximum	25,000 (172.4)	4.6.13.1, 2 percent strain, ASTM D 882
Concentricity	70% minimum (50% minimum for over expanded sizes)	4.6.3.3

TABLE II. Physical properties. 1/

Characteristic	Requirement	Test procedure and conditions
Color stability	Pass	4.6.16 175° ± 2°C (347° ± 4°F), 24 hours
Clarity stability Clear	Pass	4.6.17 175° ± 2°C (347° ± 4°F), 24 hours
Restricted shrinkage	No cracks	4.6.6.1.1 175° ± 2°C (347° ± 4°F)
Voltage withstand	Pass	4.6.6.2
After unrestricted shrinkage:		
ID, maximum	Table I	4.6.3
Wall thickness	Table I	4.6.3
Tensile strength, psi (MPa), minimum	1,500 (10.3)	4.6.14 ASTM D 638, 20 inches/minute
Ultimate elongation, percent, minimum	200	4.6.14 ASTM D 638, 20 inches/minute
Dielectric strength, volts/mil (Kv/mm), minimum	500 (19.7)	4.6.2 ASTM D 2671
Volume resistivity, Ohm-cm, minimum	Classes 1 & 3 - 10^{14}; Class 2 - 10^{16}	4.6.2 ASTM D 876
Dielectric constant, maximum 3/	Classes 1 and 3 - 3.1 Class 2 - 2.7	4.6.2 ASTM D 150
Specific gravity, maximum	Class 1 - 1.35 Class 2 - 1.00 Class 3 - 1.50	4.6.2 ASTM D 792
Water absorption, percent, maximum	Classes 1 and 3 - 0.5 Class 2 - 0.2	4.6.2 ASTM D 570, 24 hrs.at 23°C
Corrosion	No corrosion	4.6.10.1 and 4.6.10.2 175° ± 2°C (347° ± 4°F), 16 hours

TABLE II. Physical properties. 1/ - Continued

Characteristic	Requirement	Test procedure and conditions
Low temperature flexibility	No cracking	4.6.7.1 Classes 1 & 2: -55° ± 1°C (-67° ± 2°F); Class 3: -25° ± 1°C (-13° ± 2°F)
Flammability	Class 1 - self-extinguishing within one minute and no more than 25 percent of indicator flag burned or charred. No dripping, flowing of large sizes;	4.6.15.1
	Class 2 - N/A;	
	Class 3 - Pass	4.6.15.3
Heat resistance, property after:		4.6.9 for 168 hours, Classes 1 and 2: 175° ± 2°C (347° ± 4°F); Class 3: 150° ± 2°C (302° ± 4°F)
Ultimate elongation, percent, minimum	100	
Fluid resistance, property after:		4.6.11 (Use 23°C, not 35°C).
Tensile strength, psi (MPa), minimum	1,000 (6.9)	
Dielectric strength, volt/mil (Kv/mm), minimum	400 (15.8)	
Fungus resistance 2/	No growth	4.6.2 ASTM G 21

1/ Unless otherwise specified, the stated requirements, test conditions and procedures are for all classes.

2/ MIL-I-23053/5 materials do not normally support fungus growth. Performance of this requirement is at the option of the acquisition activity (see 6.2.1).

3/ Dielectric constant is a requirement only when specified in acquisition document.

Shelf life conditions: Supplier shall certify to storage at 40°C (104°F) for 4 years. Conformance to 3.5. See 3.5.2 for shelf life extension.

Intended use: Heat shrinkable flexible polyolefin sleeving is used for light duty harness jackets, wire color coding, marking or identification.

NOTE:

a. Flammability - Class 2 heat shrinkable sleevings described in this specification sheet have not been flame retarded and will burn readily. These sleevings (Class 2) shall not be considered for acquisition when flame resistance is required.

Custodians
Army - ER
Navy - AS
Air Force - 85

Review activities:
Army - AR, ER, MI
Navy - EC
Air Force - 99
DLA - GS

User activities:
Army - ME
Navy - MC

Preparing activity:
Navy - AS

(Project 5970-0577-05)

Capacitor Data Sheet

Diversified Technology®
An Ergon Co.

COMPONENT SPECIFICATION

COMPONENT SPECIFICATION NO.: 170001100

DESCRIPTION: Surface Mount Capacitor, 100uF @ 10V, 20% Tolerance, E Case Size, OS-CON

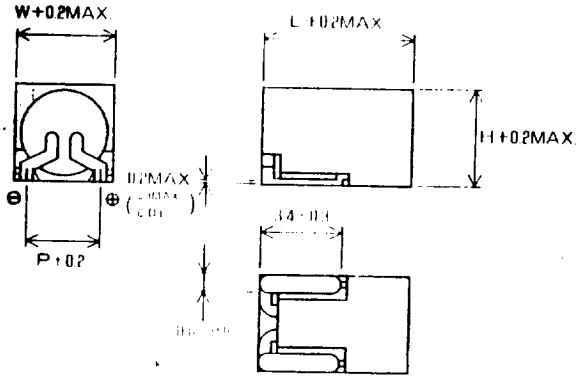
MANUFACTURER

OS-CON (SANYO) 10SM100M

Table 8—1 SM Series Characteristics List

Size Code	Part Number ※1	Rated voltage (V)	Nominal capacitance (μF)	Tangent of loss angle (less than)	Leakage ※2 current (μA) (less than)	E.S.R. ※3 (100~300KHz) (mΩ) (less than)
E	20SM47M	20	47	0.07	47.0	80
	20SM68M	20	68	0.07	68.0	80
	10SM100M	10	100	0.08	50.0	80
	6SM150M	6.3	150	0.09	47.2	80

Dimensions (unit: mm)



Explanation of Code Number

16 SL 4R7 M + TS
(1) (2) (3) (4) (5)

(5) Taping or forming code (1 or 2 figures)
(4) Capacitance tolerance (1 figure)
(3) Capacitance (1 ~ 3 figures)
(2) Series name (2 figures)
(1) Rated voltage (1 or 2 figures)

Molex Connector Data Sheet

Pin and Socket Connectors

Current Rating (Current Density)

Current rating is key to selecting the right connector. It is stated in amperes per circuit with each circuit of the connector carrying the rated current. The rating is based on the current level passing through the terminal resulting in a 30 degree Centigrade (maximum) temperature rise. The current level is then de-rated due to adjacent terminal heating, based on the number of circuits in the housing (insulator).

Connector Size (Circuit Density)

Circuit density, expressed in circuits per square inch, is a relative measure of the size of a connector as reflected in the number of circuits that can be accommodated in one square inch of real estate. The higher the circuit density, the smaller the connector. Connector size is a major design consideration in printed circuit board applications and where equipment downsizing is required. When a connector is mounted in a panel or bulkhead, size may also be a factor.

Engagement Force

Engagement force, measured in pounds per circuit, is the effort required to mate the plug to the receptacle. Total connector engagement force is approximated by multiplying the number of circuits in the housing by the per circuit engagement force. (Due to other factors, actual force may be somewhat higher.) Engagement force can be a major concern in higher circuit count housings due to potentially high total mating forces, and in printed circuit board applications where high mating forces could damage the printed circuit board. In these cases a connector family with a lower engagement force or a terminal having a lower engagement force within a family should be chosen.

Wire Size

The size of wire to which terminals are crimped is not generally a critical consideration. The Molex connectors listed on this chart will typically accommodate the range of 16-28 AWG. Should your application require a heavier wire gauge (a smaller AWG number) for mechanical strength or current carrying capability, choose a compatible connector family.

Configuration and Circuit Size

Molex power connector families are all available in free-hanging or panel mounted wire-to-wire configurations. Most are also offered in vertical printed circuit board header assembly configurations. PC tail terminals can be used to customize the standard plug with any combination of male and female pc (solder) tail terminals. Right angle header assemblies are also available in some connector families.

Choose the circuit size that meets your specifications based on:

1. current rating
2. number of module-to-module interconnects needed
3. total connector engagement force
4. size of the connector

Operating Voltage

The voltage rating is established by U.L. standards at either 250 or 600 volts. These voltage ratings are RMS values (Root Mean Square) and therefore apply to both AC and DC voltages. Generally the higher voltage ratings are obtained by fully enclosing both the male and female terminals in the housing (insulator). Shrouded housings, or fully isolated contacts also offer protection of the contacts during assembly and handling of your products.

Materials and Plating

Housings are available in nylon with a flammability ratings of UL 94V-2 and, in some families, a 94V-0 rating. The higher 94V-0 rating indicates that the material will extinguish itself (in case of fire) more rapidly than the 94V-2 material. A 94V-0 rating does not infer a higher operating temperature rating, but rather a higher resistance to flame continuance.

The standard terminal plating options available for Molex power connectors are tin, tin/lead, and overall or select gold. Tin plating is appropriate for most applications where per circuit currents are above 0.5 amperes. Gold plating should generally be specified in applications where signal or low current lines are used, high mating cycles (>30 cycles) are likely, or within harsh environments. Terminal base materials offered are brass and phosphor bronze. Brass is the standard material and affords an excellent combination of strength and current carrying capability. Phosphor bronze is recommended where:

1. a thinner base material is used to obtain a lower engagement force
2. high engagement/disengagement cycles are likely.
3. prolonged exposure to high ambient temperatures are likely.

Mini-Fit Family High Current/High Density Power Connector System

The Mini-Fit Family of High Current/High Density Power Connectors is designed to meet your requirements for a interconnection system with the broadest possible configurations and options. The Mini-Fit Family allows you the greatest design flexibility in your product's interconnection system, allowing you to interconnect:

Mini-Fit, Jr.
- Wire to Wire
- Wire to Board (vertical header)
- Wire to Board (right angle header)

Mini-Fit, BMI
- Blind Mating Wire to Wire
- Blind Mating Wire to Board (parallel mounting)
- Blind Mating Wire to Board (right angle mounting)
- Blind Mating Board to Board (parallel boards)
- Blind Mating Board to Board (right angle boards)

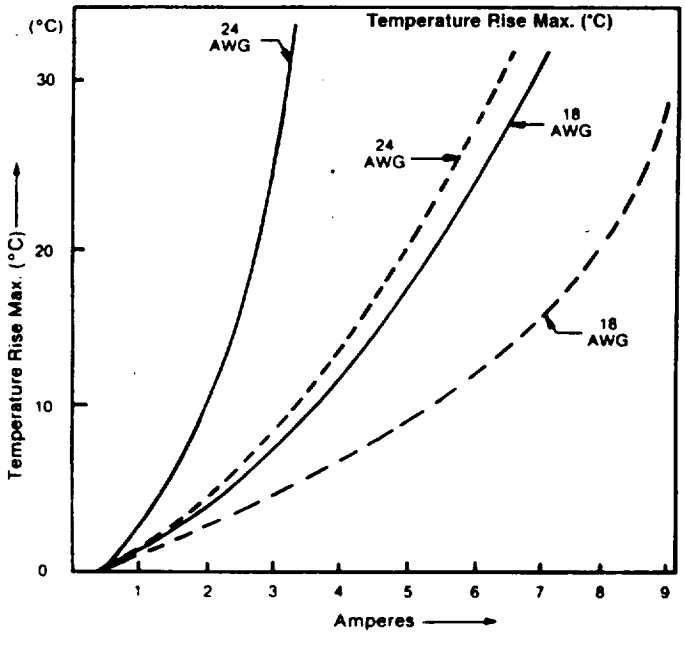
Mini-Fit, TPA
- Wire to Wire with Secondary Terminal Retention (TPA)
- Wire to Board (vertical header) with TPA
- Wire to Board (right angle header) with TPA

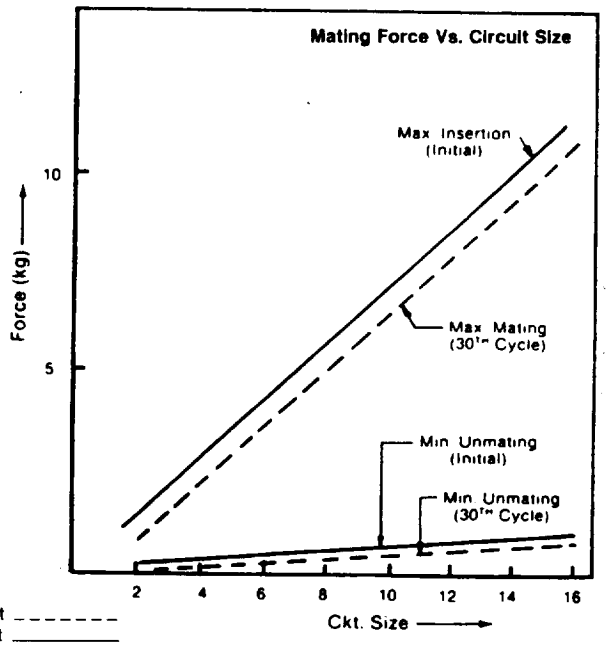
The Mini-Fit, Jr., Mini-Fit, BMI, and Mini-Fit, TPA accept the same terminals and application tooling further reducing your design and qualification effort.

The Mini-Fit Family also features:

- Current rating up to 9 amperes per circuit
- 600 volt rating
- Positive housing locks
- Fully isolated terminals
- Low engagement force terminals
- Available in 94V-2 and 94V-0 materials
- UL recognized, CSA certified, TUV licensed
- 10 milliohm contact resistance

UL Recognized, CSA Certified and T.U.V. Licensed





Specifications

Material:
Terminal — Brass or Phosphor Bronze
Plating — Tin or Select Gold
Housing — UL 94V-0 nylon 6/6 or UL 94V-2 nylon 6/6

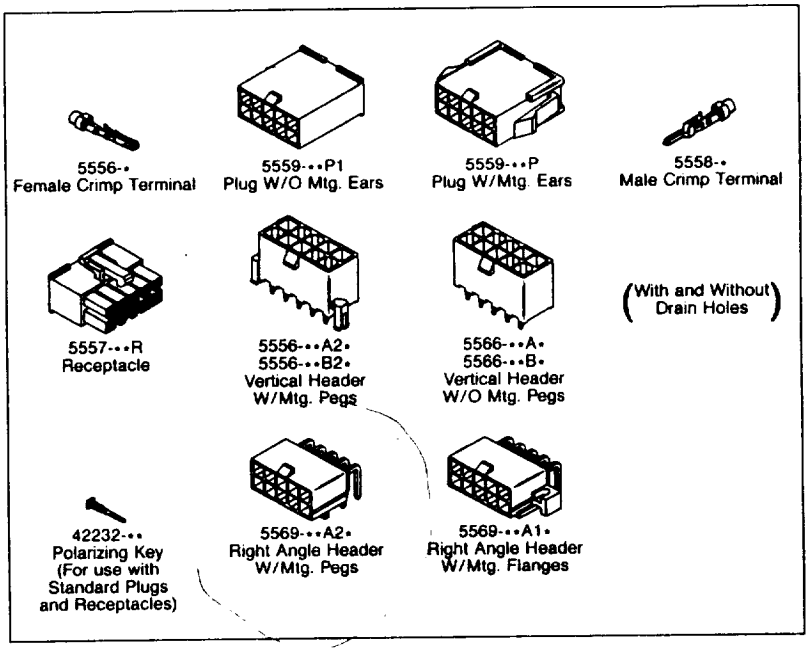
Mechanical:
Temperature Rise — (Carrying rated current load) 30°C max.
Mating Force — **0.7 kg.**/1.54 lbs. per circuit max.
Unmating Force — **.05 kg.**/.11 lbs. per circuit min. initial
.04 kg./.09 lbs. per circuit min. after 30 cycles

Electrical:
Voltage Rating — 600 (RMS)
Current Rating — 9 amps - 2, 3 circuits
8 amps - 4, 5 and 6 circuits
7 amps - 8 and 10 circuits
6 amps - 12, 14, 16, 18, 20, 22 and 24 circuits
Contact Resistance — 10mΩ max.
Insulation Resistance — 1,000 MΩ min.
Dielectric Strength — 1,500V ac

Mini-Fit, Jr.

The Mini-Fit, Jr. Series is designed for high current/high density applications which require the design flexiblity of wire to wire and wire to board configurations in the interconnection system. The Mini-Fit, Jr. is appropriate for both power and signal applications as it can carry currents of up to 9 amperes/circuit and has a 10 milliohm contact resistance.

- Current rating up to 9 amperes per circuit
- 600 volt rating
- 10 milliohm contact resistance
- Positive housing locks
- Fully isolated terminals
- Low engagement force terminals
- Available in 94V-2 and 94V-0 materials
- Available in 2 thru 24 circuit housings
- UL File No. E-29179, CSA File No. 19980 TUV licensed
- Uses standard Mini-Fit series terminals



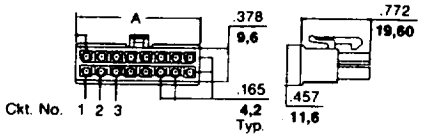
Ordering Information (Order Terminals From Page 11K) Vertical Shading Indicates Single Row Version

CIRCUIT SIZE	Dual Row	Single Row	02	03	04	05	06	08	10	12	14	16	18	20	22	24
Amperes/Circuit (Max)* Voltage Rating (Max)* Dim A inch mm			9 600 .213 5,4	9 600 .543 13,8	8 600 .378 9,6	8 600 .874 22,2	8 600 .543 13,8	7 600 .709 18,0	7 600 .874 22,2	6 600 1.039 26,4	6 600 1.205 30,6	6 600 1.370 34,8	6 600 1.535 39,0	6 600 1.700 43,2	6 600 1.865 47,4	6 600 2.030 51,6
RECEPTACLE (5557-NR)** Uses Female Terminal 5556																
94V-2	39-01-XXXX	39-01-XXXX	• -2020	• -4030	• -2040	• -4050	• -2060	• 2080	• 2100	• -2120	• -2140	• -2160	• -2180	• -2200	• -2220	• -2240
94V-0	39-01-XXXX	39-01-XXXX	• -2025	• -4031	• -2045	• -4051	• -2065	• -2085	• -2105	• -2125	• -2145	• -2165	• -2185	• -2205	• -2225	• -2245
PLUG (5559-NP)** Uses Male Terminal 5558																
Panel Mount 94V-2	39-01-XXXX	39-01-XXXX	• -2021	• -4032	• -2041	• -4052	• -2061	• -2081	• -2101	• -2121	• -2141	• -2161	• -2181	C/F	C/F	C/F
94V-0	39-01-XXXX	39-01-XXXX	• -2026	• -4033	• -2046	• -4053	• -2066	• -2086	• -2106	• -2126	• -2146	• -2166	• -2186	C/F	C/F	C/F
Free Hanging 94V-2	39-01-XXXX	39-01-XXXX	• -3023	• -4036	• -3043	• -4056	• -3063	• -3083	• -3103	• -3123	• -3143	• -3163	C/F	C/F	C/F	C/F
94V-0	39-01-XXXX	39-01-XXXX	• -3029	• -4037	• -3049	• -4057	• -3069	• -3089	• -3109	• -3129	• -3149	• -3169	C/F	C/F	C/F	C/F
Panel Cutout "E" inch mm			.425 10,8	.756 19,2	.591 15,0	1.087 27,6	.756 19,2	.921 23,4	1.087 27,6	1.252 31,8	1.417 36,0	1.583 40,2				
STRAIN RELIEF (41995)**	15-04-XXXX	C/F	• -0340	C/F	• -0294	C/F	• -0296	• -0343	C/F	• -0345	C/F	C/F	C/F	C/F	C/F	C/F
POLARIZING KEY (42232)	• 15-04-0211	• 15-04-0211	Use with Receptacle Housing (5557)													
RIGHT ANGLE HEADER (5569-N) Tin Plated																
PCB Mounting Flanges 94V-2	39-29-XXXX	39-30-XXXX	• -1028	• -3031	• -1048	• -3051	• -1068	• -1088	• -1108	• -1128	• -1148	• -1168	• -1188	• -1208	• -1228	• -1248
94V-0	39-29-XXXX	39-30-XXXX	• -1027	• -3032	• -1047	• -3052	• -1067	• -1087	• -1107	• -1127	• -1147	• -1167	• -1187	• -1207	• -1227	• -1247
PCB Mounting Pegs 94V-2	39-30-XXXX	39-30-XXXX	• -1020	• -3035	• -1040	• -3055	• -1060	• -1080	• -1100	• -1120	• -1140	• -1160	C/F	C/F	C/F	C/F
94V-0	39-30-XXXX	39-30-XXXX	• -0020	• -3036	• -0040	• -3056	• -0060	• -0080	• -0100	• -0120	• -0140	• -0160	C/F	C/F	C/F	C/F
RIGHT ANGLE HEADER (5569-N) Gold Plated (30 Microinch)																
PCB Mounting Flanges 94V-2	39-29-XXXX	39-30-XXXX	• -5023	• -3033	• -5043	• -3053	• -5063	• -5083	• -5103	• -5123	• -5143	• -5163	• -5183	• -5203	• -5223	• -5243
94V-0	39-29-XXXX	39-30-XXXX	• -4029	• -3034	• -4049	• -3054	• -4069	• -4089	• -4109	• -4129	• -4149	• -4169	• -4189	• -4209	• -4229	• -4249
PCB Mounting Pegs 94V-2	39-30-XXXX	39-30-XXXX	• -1021	• -3037	• -1041	• -3057	• -1061	• -1081	• -1101	• -1121	• -1141	• -1161	C/F	C/F	C/F	C/F
94V-0	39-30-XXXX	39-30-XXXX	• -1022	• -3038	• -1042	• -3058	• -1062	• -1082	• -1102	• -1122	• -1142	• -1162	C/F	C/F	C/F	C/F

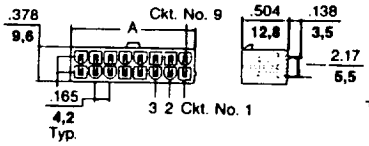
**Strain relief accepts both plug and receptacle. Requires use of "Free Hanging" Plug (w/o ears).
Accepts standard receptacle in sizes 6-24. For 2 or 4 circuit, strain relief uses receptacle Order No. 39-01-3042 (94V-2) or 39-01-3048 (94V-0).
•U.S. Standard Product, available through Molex franchised distributors.
C/F = Consult factory, part designed or in tooling after publication date.
*Rating based on fully loaded housings.

Mini-Fit Jr.

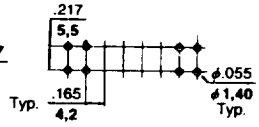
5557-NR Housing
Uses 5556 Terminal



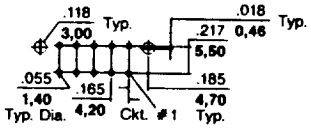
5566-NA Header Assembly
Peg Mounted Version Available



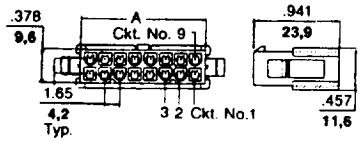
Vertical Header w/o Pegs
P.C. Board Layout



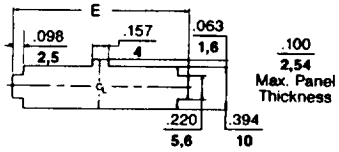
Vertical Header w/Pegs
P.C. Board Layout



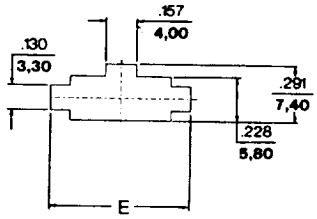
5559-NP Housing
Shown with Optional Panel Mounting Ears
Uses 5558 Terminal



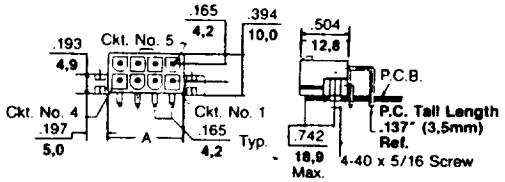
Mounting Hole Details for
5559-NP Housing
Dual Row



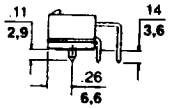
Single Row



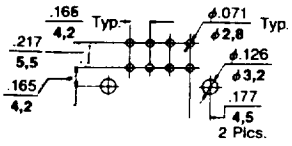
5569-NA Right Angle Header
Flange Mounted Version



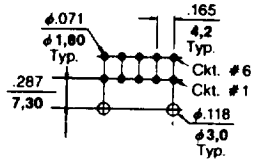
Peg Mounted Version



Right Angle Header w/
Flanges P.C. Board Layout



Right Angle w/Pegs P.C.
Board Layout 6-24 Ckts.



Ordering Information Vertical Shading Indicates Single Row Version

CIRCUIT SIZE	Dual Row	Single Row	02	03†	04	05	06	08	10	12	14	16	18	20	22	24
Amperes/Circuit (Max)* Voltage Rating (Max)* Dim A inch / mm			9 600 .213 5,4	9 600 .543 13,8	8 600 .378 9,6	8 600 .874 22,2	8 600 .543 13,8	7 600 .709 18,0	7 600 .874 22,2	6 600 1.039 26,4	6 600 1.205 30,6	6 600 1.370 34,8	6 600 1.535 39,0	6 600 1.700 43,2	6 600 1.865 47,4	6 600 2.030 51,6
VERTICAL HEADER (5566-N)	**Tin Plated**															
Low Profile Mounting 94V-2	39-28-XXXX	N/A	• -1023	N/A	• -1043	N/A	• -1063	• -1083	• -1103	• 1123	• 1143	• -1163	• -1183	• -1203	• -1223	• -1243
94V-0	39-28-XXXX	N/A	• -8020	N/A	• -8040	N/A	• -8060	• -8080	• -8100	• -8120	• -8140	• -8160	• -8180	• -8200	• -8220	• -8240
Drain Holes 94V-2	39-29-XXXX	N/A	• -3066	N/A	• -3066	N/A	• -3066	• -3086	• -3106	• -3126	• -3146	• -3166	C/F	C/F	C/F	C/F
94V-0	39-31-XXXX	N/A	• -0020	N/A	• -0040	N/A	• -0060	• -0080	• -0100	• -0120	• -0140	• -0160	C/F	C/F	C/F	C/F
PCB Mounting Pegs 94V-2	39-29-XXXX	39-30-XXXX	• -9023	• -1039	• -9043	C/F	• -9063	• -9083	• -9103	• -9123	• -9143	• -9163	C/F	C/F	C/F	C/F
94V-0	39-29-XXXX	39-30-XXXX	• -9027	• -2030	• -9047	C/F	• -9067	• -9087	• -9107	• -9127	• -9147	• -9167	C/F	C/F	C/F	C/F
Drain Holes 94V-2	39-29-XXXX	39-30-XXXX	• -9022	• -2035	• -9042	C/F	• -9062	• -9082	• -9102	• -9122	• -9142	• -9162	C/F	C/F	C/F	C/F
94V-0	39-29-XXXX	39-30-XXXX	• -9026	• -2036	• -9046	C/F	• -9066	• -9086	• -9106	• -9126	• -9146	• -9166	C/F	C/F	C/F	C/F
VERTICAL HEADER (5566-N)	**Gold Plated (30 Microinch)**															
Low Profile Mounting 94V-2	39-29-XXXX	N/A	• -0023	N/A	• -0043	N/A	• -0063	• -0083	• -0103	• -0123	• -0143	• -0163	C/F	C/F	C/F	C/F
94V-0	39-29-XXXX	N/A	• -6028	N/A	• -6048	N/A	• -6068	• -6088	• -6108	• -6128	• -6148	• -6168	C/F	C/F	C/F	C/F
Drain Holes 94V-2	39-31-XXXX	N/A	• -0027	N/A	• -0047	N/A	• -0067	• -0087	• -0107	• -0127	• -0147	• -0167	C/F	C/F	C/F	C/F
94V-0	39-31-XXXX	N/A	• -0028	N/A	• -0048	N/A	• -0068	• -0088	• -0108	• -0128	• -0148	• -0168	C/F	C/F	C/F	C/F
PCB Mounting Pegs 94V-2	39-29-XXXX	39-30-XXXX	• -9025	• -2031	• -9045	C/F	• -9065	• -9085	• -9105	• -9125	• -9145	• -9165	C/F	C/F	C/F	C/F
94V-0	39-29-XXXX	39-30-XXXX	• -9029	• -2032	• -9049	C/F	• -9069	• -9089	• -9109	• -9129	• -9149	• -9169	C/F	C/F	C/F	C/F
Drain Holes 94V-2	39-29-XXXX	39-30-XXXX	• -9024	• -5039	• -9044	C/F	• -9064	• -9084	• -9104	• -9124	• -9144	• -9164	C/F	C/F	C/F	C/F
94V-0	39-28-XXXX	39-30-XXXX	• -9028	• -6030	• -9048	C/F	• -9068	• -9088	• -9108	• -9128	• -9148	• -9168	C/F	C/F	C/F	C/F

train relief accepts both plug and receptacle. Requires use of "Free Hanging" Plug (w/o ears).
.ccepts standard receptacle in sizes 6-24. For 4 circuit, strain relief uses receptacle Order No. 39-01-3042 (94V-2) or 39-01-3048 (94V-0).
•U.S. Standard Product, available through Molex franchised distributor.
C/F = Consult factory, part designed or in tooling after publication date
*Rating based on fully loaded housings

APPENDIX 12

ABBREVIATIONS AND ACRONYMS

List of Abbreviations and Acronyms

A	Amps
AHr	Amp Hours
ANSI	American National Standards Institute
APM	Advanced Power Management
APW II	Advanced Portable Workstation II
ARPA	Advanced Research Projects Agency
BIOS	Basic Input Output System
BITF	Built-in Test Facilities
BM	Battery Module
℃	Degrees Celsius
C	Charge
CPU	Central Processing Unit
CRT	Cathode Ray Tube
DM	Display Module
DRAM	Dynamic Random Access Memory
DMA	Direct Memory Access
ECC	Error Correction Code
EDAC	Error Detection and Correction
ECL	Emitter Coupled Logic
℉	Degrees Fahrenheit
GUI	Graphical User Interface
HDDS	High Definition Display Systems
HDTV	High Definition Television
Hz	Hertz
IDE	Integrated Drive Electronics
IEEE	Institute of Electrical and Electronic Engineers
ISA	International System Architecture
KB	Kilo Bytes
KM	Keyboard Module

LAN	Local Area Network
lbs	pounds
LCD	Liquid Crystal Display
mAh	Milli Amp Hour
MHz	Megahertz (1,000,000 Hz)
NASA	National Aeronautics and Space Administration
NTSC	National Television Standards Committee
PC	Personal Computer (Apple, DOS, UNIX, *etc.*)
PCI	Peripheral Component Interconnect
PCMCIA	Personal Computer Memory Card International Association
PCT	Portable Computer Technology
PDA	Personal Digital Assistant
PWA	Printed Wiring Assembly
RTC	Real Time Clock
SAIC	Science Applications International Corporation
SCSI	Small Computer System Interface
SIMM	Single Inline Memory Modules
SNB	Subnotebook
SRAM	Static Random Access Memory
SVGA	Super Video Graphics Accelerator
TFT	Thin-Film-Transistor
V	Volts
VESA	
VGA	Video Graphics Accelerator
WSM	Wireless Server Module