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16. Abstract The Students for the Exploration and Development of Space Satellite (SEDSAT-1) is an ambitious project to design, build, and fly a generally-accessible low-cost satellite which will 1) act as a technology demonstration to verify the suitability of novel optical, battery, microprocessor, and memory hardware for space flight environments, 2) to advance the understanding of tether dynamics and environmental science through the development of advanced imaging experiments, 3) to act as a communication link for radio amateurs and 4) to provide graduate and undergraduate students with a unique multi-disciplinary experience in designing complex real-world hardware/software. This report highlights the progress made on this project during the time period from January 2, 1996 to June 1, 1996 at the end of which time the SEASIS 0.7 version software was completed and integrated on the SEASIS breadboard, a functional prototype of the PAL Camera was developed, the preferred image compression technique was selected, the layout of the SEASIS board was begun, porting of the SCOS operating system to the CDS board was begun, a new design for a tether release mechanism was developed, safety circuitry to inhibit tether cutting was developed and prototyped, material was prepared to support a comprehensive safety review of the project which was held at JSC (which was personally attended by one of the Principal Investigators), and prototype ground software was developed.

17. Key Words (Suggested by Author (s))
SEASIS -- SEDS (Students for the Exploration and Development of Space) Earth, Atmosphere, and Space Imaging System
CDS -- Command Data System
PAL -- Panoramic Annual Lens
technology demonstration, environmental science, tether dynamics, compression techniques, image processing, software engineering

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SEDSAT-1 Technology Development

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Development Schedule and Progress

During the period of this contract the UAH SEDSAT team has continued development of the SEDSAT. One of the responsibilities of the investigators has been to oversee the teams progress and report to NASA. A detailed schedule, that begins just after the contract began and runs until present, is included as attachment 1. This plan has undergone many revisions over the course of the contract. It current form reflects the up-to-date status of the project and its current planned configuration. Several major SEDSAT development milestones have been accomplished during the course of this contract.

1. The SEASIS 0.7 software release completed coding March 6.
2. The SEASIS 0.7 software completed integration and test on the SEASIS processor bread-board June 16. The test showed the systems ability to capture imagery on a predefined schedule and transmit (on command) to another transputer board.
3. A functional protoype of the PAL camera was completed in aluminum April 1. Since the departure of Amy Houts further optical development has been delayed. However, optical tests were done with the camera by Rachel Flynn during May.
4. Lossless GIF compression was compared with JPEG for PAL images and GIF was selected February 21.
5. A design package for the SEASIS processor board was delivered to SCI in early February, and completed to their satisfaction February 29. Photo plots of the processor board layout were received by us June 20.
6. The first protoflight Command and Data System (CDS) board was received and stuffed with components on March 5. It completed hardware checkout on May 3.
7. The SCOS kernel was brought up on the CDS board May 13.
8. On March 15 Marshall indicated to UAH that safety requirements would demand onboard timers and a new Tether Release Mechanism Design.
9. UAH designed, prototyped, and demonstrated the safety timers on April 24.
10. UAH delivered a set of drawings for a new TRM design May 27.
11. UAH supported the safety panel review of SEDS/SEDSAT.
12. A prototype of the ground communications task and the ground telemetry console was completed in early May. It has not been tested for lack of a CDS link.

A flow chart of the plan for SEDSAT completion extending from this point is provided as a Attachment 1.

Image Quality Comparison

One trade-off examined during the program was what image compression algorithm to use in the SEASIS processor. Compressing SEASIS images serves two purposes. First, it allows more images to be stored in mass memory. Second, it improves the transmission speed to the ground over the very limited 9.6 kbits/sec link. The current design stores images in mass memory uncompressed and only compresses for transmission. This choice is based on our using the full 128 Mbytes of mass memory, the continuing error rate in mass memory, and the time it takes to compress images on the transputer.

The choice of compression algorithm was between Graphics Interchange Format (GIF) and the JPEG standard. GIF is a lossless algorithm, that is the uncompressed image exactly replicates the original image. JPEG is lossy. The uncompressed image is an approximation to the original image, with the algorithm designed to cause distortion in a way that minimizes visual impact. JPEG can, in general, achieve much more compression than GIF. The JPEG quantization matrices allow a trade-off between compressed size and uncompressed image quality.

The planned purpose of SEASIS image collection, during the contract period, was to allow SEDSAT attitude estimation during tether deployment. This was to be achieved by taking images in blocks, with each block set up to over sample the highest expected attitude oscillation frequency. The blocks were spaced throughout the tether deployment. In addition, a special imaging block was scheduled for the first indication of tether cut to attempt to capture images of tether recoil. Through experiment, we determined that the time line could be achieved only by storing images uncompressed because of the time required to compress. It is possible software optimization could have reduced the compression time significantly, but in view of the difficulty of programming the SCC-100 this did not seem a fruitful course. With GIF compression the SEASIS processor is capable to storing roughly 1200 images, more than were required for any planned tether mission collection schedule.

Since the tether mission will no longer be conducted, this requirement is now moot. However, the choice of compression algorithm need not be reconsidered. A lossless algorithm is the robust choice since we can be assured no possibly valuable scientific information is lost. As examples of how the images appear under different compression regimes, the following figures show a set of comparative images. These images were generated using a PAL image simulator written by Mr. Ahmed Siddique. This simulator uses a 3-D graphics model of the earth-sun-moon system. The model contains a sphere to represent the earth, and texture maps an image of the earth onto the sphere. The simulator then calculates the field of view of the PAL at a given attitude and extracts a cylindrical cut from the full scene. The cut is then warped onto a rectangular field using the PAL angular mapping function.

Figure 1 shows the earth and moon in a typical configuration as would be seen by the PAL imaging system. The image is presented as it would be recorded, with the lens image field appearing as an annulus within the rectangular image plane. Another capability of the simulator is dewarping simulated PAL images. An example is given in where the annular image of the PAL is dewarped back into a rectangular panorama.

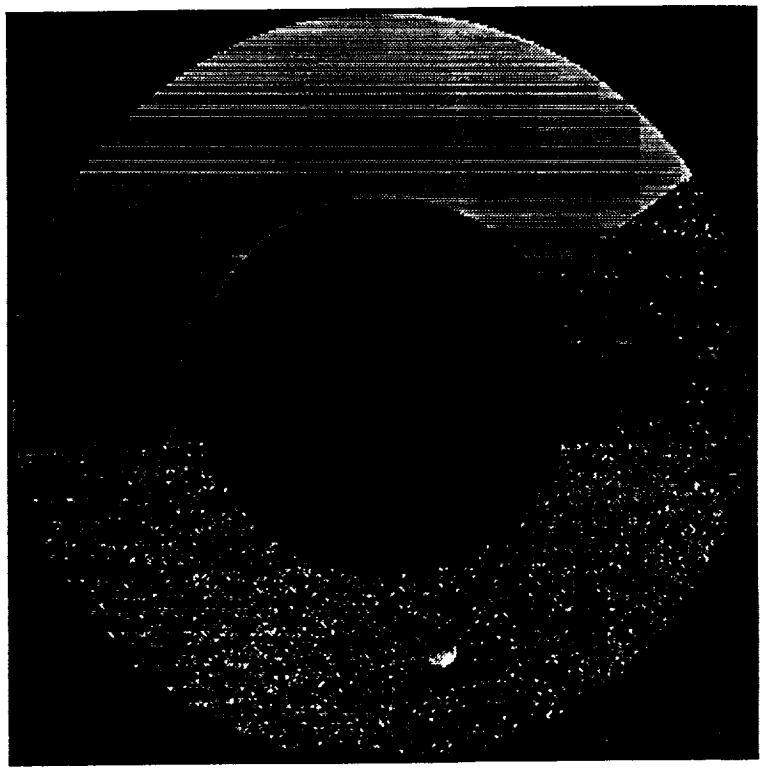


Figure 1: Simulated PAL image (1:2 scale)

Figure 2: Dewarped simmulated PAL image (not to scale)

For the tether mission, the primary measure of quality for imaging is the ability to determine attitude. To determine attitude accurately we must be able to accurately determine the angular location of the crossing of the optical equator and the limb of the earth, or the angular location of the center of the moon or sun. Taking the earth edge as an example, a illustrates the impact of compression on edge sharpness. As the JPEG quality control goes down, the sharpness of the edge visibly degrades. Based on our ability to store all the needed images with lossless compression, the processor impact of more complex compression, and the desire to maintain full image quality, there was no reason to select any algorithm other than lossless.

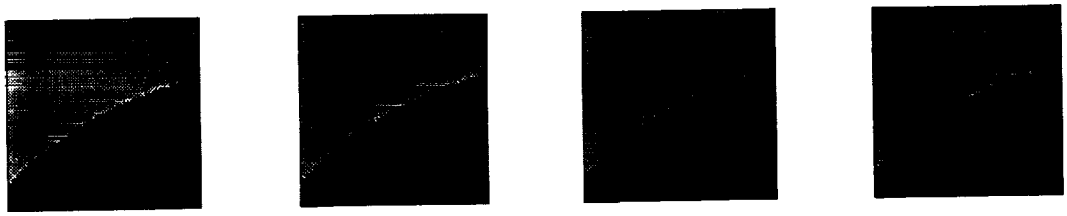


Figure 3: Pixel cutouts, no compression, JPEG high quality, medium quality, and low quality

Even though the tether mission is no longer an issue, we do not plan to revisit the algorithm choice. For all planned operations, lossless compression maintains full image quality. Because a

change of a factor of two in transmission time could be of considerable value in remote sensing applications, we will consider a lossy compression algorithm as an adjunct. The desired solution is a lossy/lossless algorithm that sends a lossy ÒthumbnailÓ of an image, then transmits the full, lossless image is desired by users. If possible, we will incorporate this more advanced version in the flight SEASIS software. While it would not have been necessary if the tether mission where the primary SEASIS objective, it will be higher priority with the tether mission cancelled.

Ground Communications Architecture

One area of SEDSAT design that is still being worked out is the ground communications architecture. shows the basic hardware architecture for SEDSAT-ground communications. The hardware aspects are emphasized, though the schematic breakdown of the software is also shown. illustrates the architecture from a software perspective.

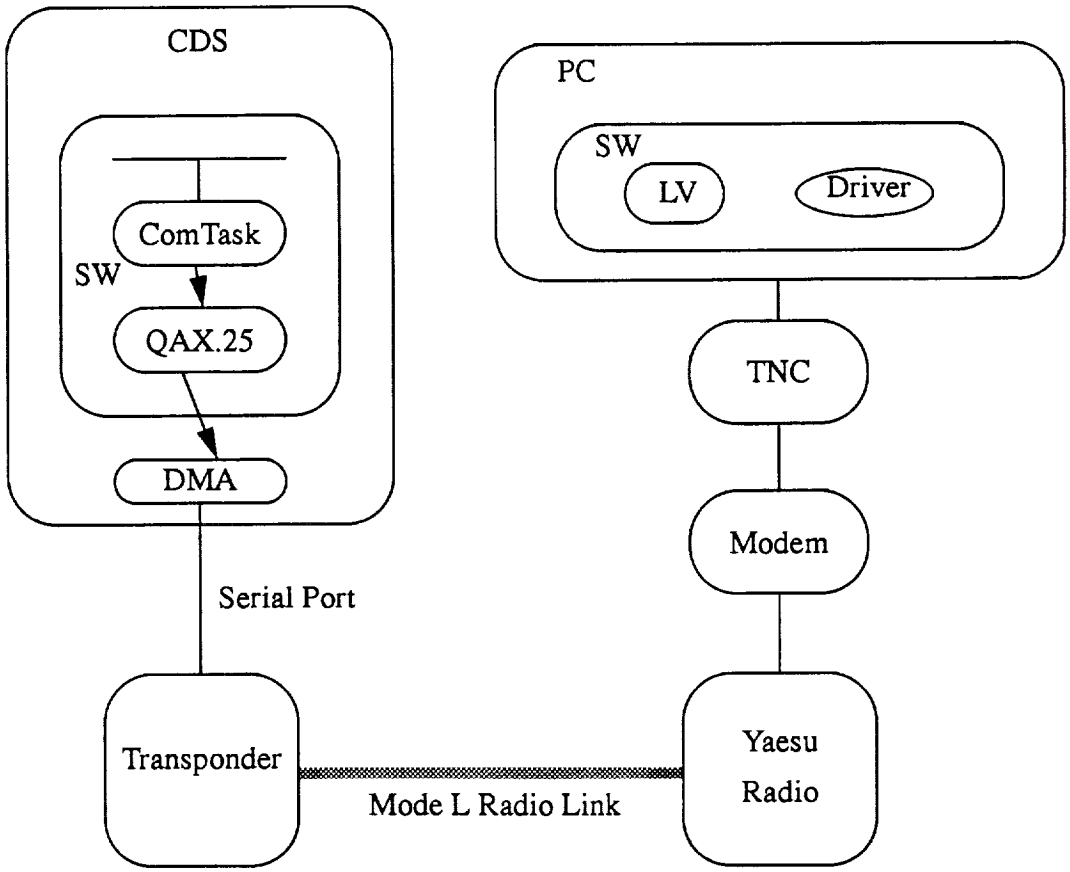


Figure 4: Hardware architecture diagram for SEDSAT ground communications

The communications link between the SEDSAT and the ground is a digital radio link. The basic rate is 9.6 Kbits/sec, though experiments at 56 kbits/sec are also planned. The link carries AX.25 frames, which encapsulate application data specific packets. Software routines, provided as part of SCOS, carry out the encapsulation and pass byte blocks to the hardware. The byte blocks go out over the serial port to the tranponder which transmits them. On the ground side a Yaesu radio picks up the link and passes a lowpass signal to a modem The modem demodulates the bit stream and passes it to the TNC, which interprets the AX.25 packets internally. The data sections are re-encapsulated onto the PC serial port. The serial port is read by PC software drivers,

which pass application level data to the labview front end. The labview front end interprets the packets and displays or archives the received data.

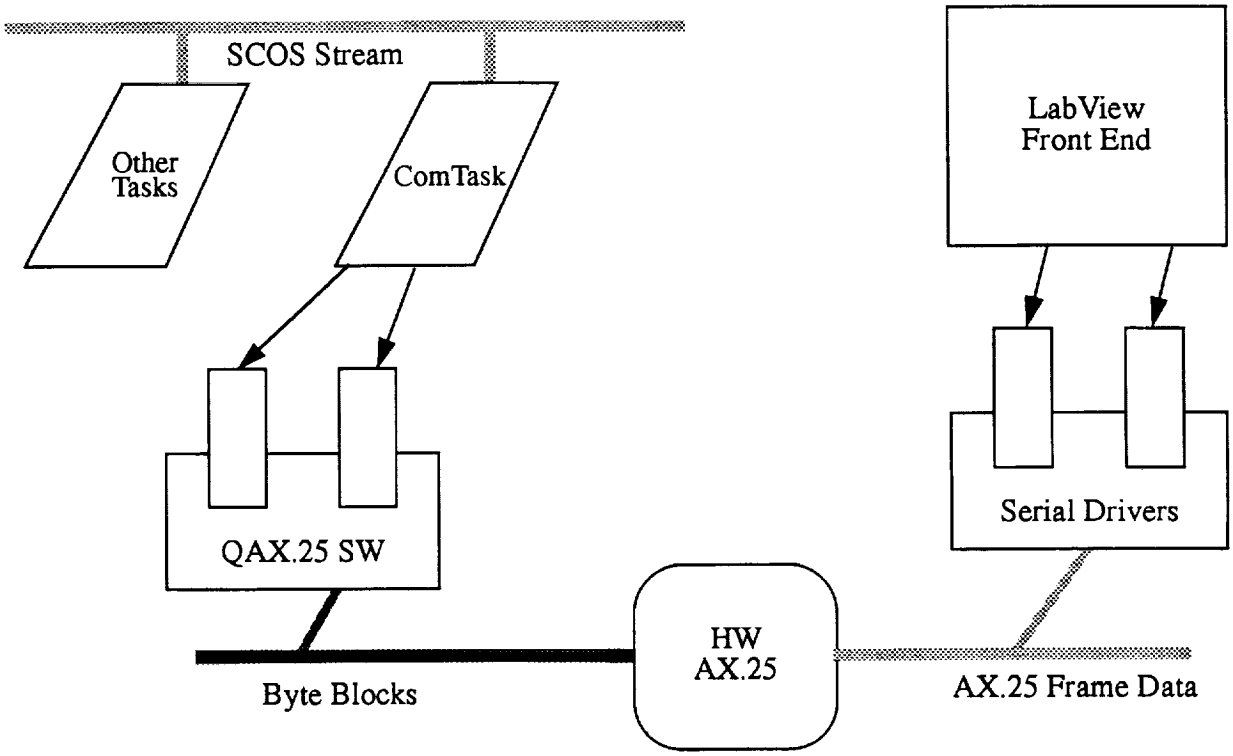


Figure 5: Software architecture diagram for SEDSAT ground communications

From the software perspective, the SEDSAT software tasks read a communications data stream managed through ComTask. ComTask sends and receives data through calls to QAX.25 routines. On the ground end, a front end written in LabView sends and receives application level data packets through a set of serial drivers. The AX.25 protocol encapsulation and decoding is all done in the TNC.

Safety Timer Design

A major concern of the safety panel was the premature cutting of the tether from the SEDSAT-1 end while the tether was still connected to the Orbiter. Such a scenario could lead to a recoil of the tether into the cargo bay and around the shuttle thereby inhibiting the closing of the cargo bay doors and requiring an emergency EVA in order to return to earth. Several alternatives were suggested to solve this problem which included a tension sensitive inhibit and an inhibit mechanism based upon three separate and independent timers. The timer option was chosen because it was unclear if the tension sensitive tether release mechanism could be designed, developed, and tested in time for the mission.

The timer circuit was designed to inhibit the cutting of the tether by interrupting the power being transferred to the tether release mechanism at three points in the circuit which included 1) the +28 volt source from the motherboard, 2) the +15 source from the DC-DC, and 3) the ground return leg. The timer was to begin operation when the satellite was powered up at separation and the to count up to a predetermined time which would be derived from the mission profile (believed to be less than 3 hours). To be conveniently integrated into the satellite, the timers were to be physically located on the CDS board with each timer being designed to be completely inde-

pendent of one another and the CDS electronics. Programming of the timers was to occur by soldering jumpers at the system was to be integrated at which point the tether mission duration would be known. The timers themselves were isolated from the tether release mechanism control circuit by C60-10 opto-relays which respond to standard TTL voltage levels. Figure 6 shows a basic block diagram of a timer module and figure 7 shows the full schematic.

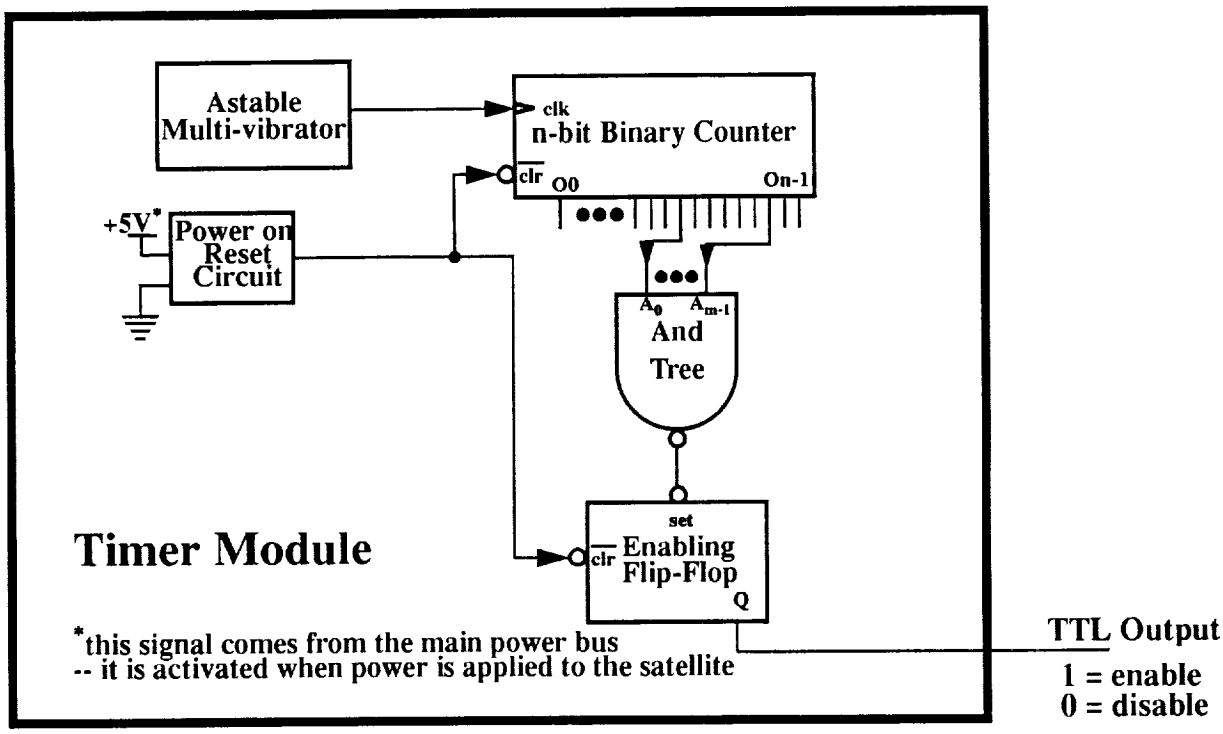


Figure 6: basic block diagram of a timer module

The timer circuit was designed not to be affected significantly by power up transient conditions since the resistor capacitor combination of the power on reset circuit had a time constant of 100ms which is large enough to allow transients to dissipate. Also the Interpoint DC-DC converter which supplies the voltage to the CDS computer and the timer circuits has filtering components which will tend to smooth out the input waveforms.

This operation of the timer was to be verified by a set of tests where the separation switches were repetitively activated and the operation verified. Design constraints on the CDS board required that the full maximum duration of the mission expire to verify timer operation (because it was impossible to read the current time values of the timer via the CDS board due to hardware limitations -- only the output of the final flip-flops could be verified).

The operation of the timers was to be verified by observing their behavior during the environmental testing phase. It was expected that during this phase the behavior of each timer would be individually monitored by the CDS computer by interrogating the output of each of the timer inhibit lines using the analog multiplexer/AtoD decoders which are currently present on the board. (Analog signals are being used here since the necessary circuitry was already present on the board thus minimizing the scope of the redesign effort.)

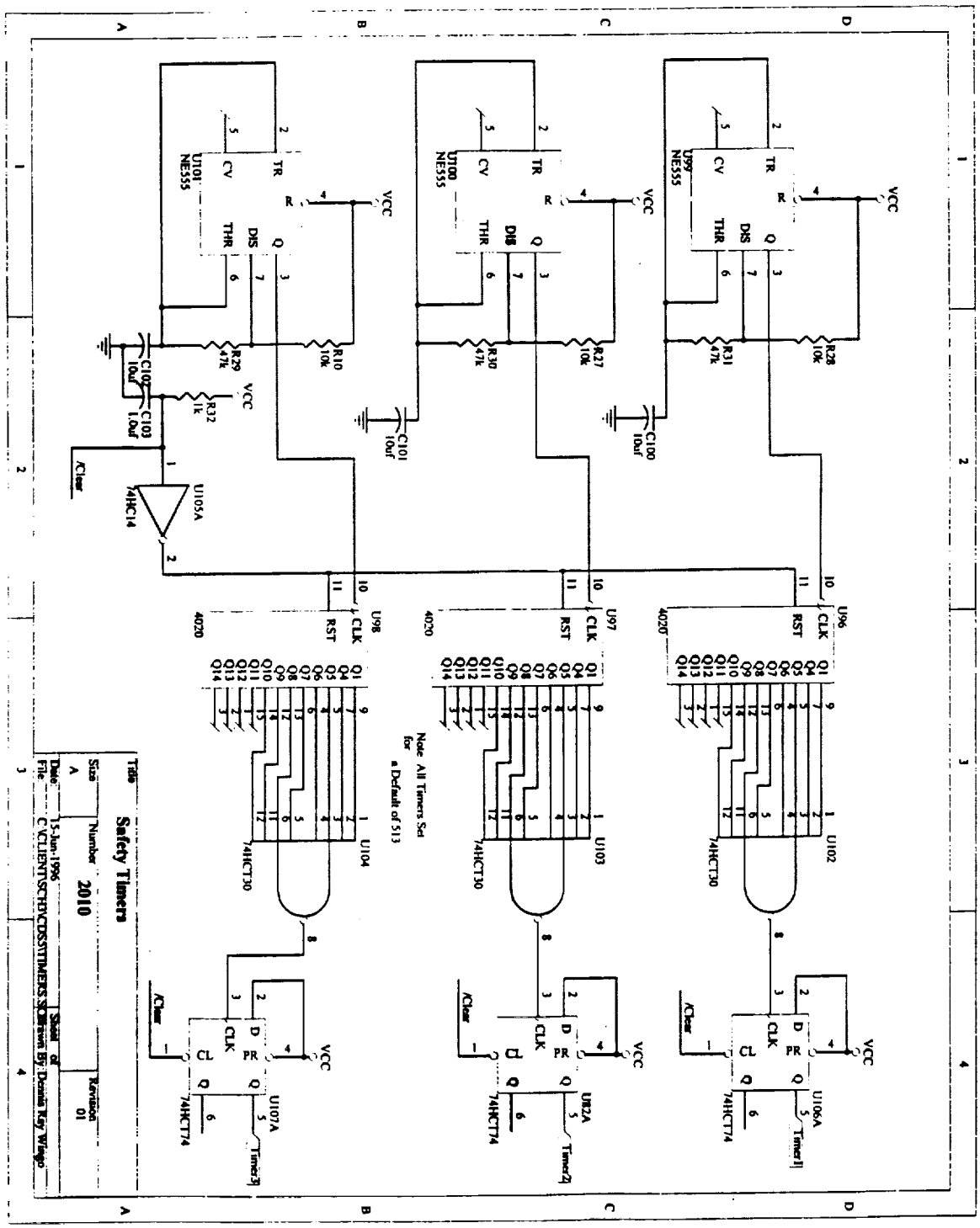


Figure 7: timer schematic

Timer Thermal Considerations

To be effective the timers had to inhibit the cutting of the tether for a period of time which represents the maximum expected tether mission duration (which is equivalent to the minimum amount of time which is allowed to elapse before the tether can be cut at the shuttle's end). The worst-case time associated with the timers, from a mission safety point of view, is the fastest time possible that the timers could complete their count under the worst-case environmental conditions. If it is assumed that there is a given amount of error in selecting the external resister/capacitor combination on the NE 555 ICs shown in figure 7 then the following analysis is a valid means of calculating the lower bound on the cycle time of the circuit for all three timers.

The basic timing formula of the NE 555 chip is

$$T = -ln(0.5)\,(R_A + 2R_B)\,C \approx 0.693\,(R_A + 2R_B)\,C \tag{1}$$

where,
T = timer period (cycle time),
R_A = R28, R27, and R10 on timer schematic,
R_B = R31, R30, and R29 on timer schematic,
C = C100, C101, and C102 on timer schematic.

Accounting for initial timing accuracy, timer drift due to temperature, initial external components accuracy and, external component drift due to temperature leads to the following formula.

$$T \approx 0.693\,(R_A + 2R_B)\,C\,[1 - \varepsilon_{timer}]\,[1 - \delta_{timer}(t - 25)]\,[1 - \varepsilon_{resisters}]\,[1 - \delta_{resisters}(25 - t)]\,[1 - \varepsilon_{capacitor}]\,[1 - \delta_{capacitor}(25 - t)] \tag{2}$$

where,

t = temperature $^{\circ}$C,
ε_{timer} = initial timer accuracy $(\% / 100)$,
δ_{timer} = timer drift $((\% /100)/^{\circ}\mathrm{C})$,
$\varepsilon_{resisters}$ = initial accuracy of resistors $(\% / 100)$,
$\delta_{resisters}$ = worst case temperature cooeficient for resistors $((\% /100)/^{\circ}\mathrm{C})$,
$\varepsilon_{capacitor}$ = initial accuracy of capacitor $(\% / 100)$,
$\delta_{capacitor}$ = worst case temperature cooeficient for capacitor $((\% /100)/^{\circ}\mathrm{C})$.

The following table lists the time critical components which have been selected for this design and their associated parameter values. It should be noted that in the cases of the resisters and capacitor the accuracies are considered to be better than the reported manufacturing tolerances since components can be selected from a sample of components and individually measured to determine how close they are to the specified nominal values. It is believed that a capacitor can be chosen which are within 5% of its desired value and both resistors can be chosen which are within 1/2% of their desired value.

Table 1: values of critical components for timer circuit

Critical Devices	Type	Manufactured Tolerance	Value	Accuracy Parameters
R_A MEPCO/ CENTALAB Inc.	Metal Film Resistor -- RN55D type	1% Temp. Coeff. ±100 PPM/°C	10 K Ω	$\varepsilon_{resisters} = \pm 0.005$
R_B MEPCO/ CENTALAB Inc.	Metal Film Resistor -- RN55D type	1% Temp. Coeff. ±100 PPM/°C	47K Ω	$\delta_{resisters} = 0.0001$
C MEPCO/ CENTALAB Inc.	Commercial Grade Dipped-Radial Lead Tantalum Capacitor	20% Effective Temp. Coeff. ±2000 PPM/°C	10 μF	$\varepsilon_{capacitor} = \pm 0.05$ $\delta_{capacitor} = 0.002$
NE 555 Timer Signetics Inc.	Monolithic Timing Integrated Circuit	1% Temp. Coeff. ±50 PPM/°C	--	$\varepsilon_{timer} = \pm 0.01$ $\delta_{timer} = 5$

The effect of substituting the accuracy parameters shown in Table 1 into Equation 2 and varying the temperature over the desired range of operation is shown in Figure 1. It should be noted that for any given timer it would be possible to remove the base error coefficient (i.e. $\varepsilon_{resistors}$ and $\varepsilon_{capacitor}$) if the actual measured value for C, R_A, and R_B were used instead of the nominal desired value. In this way, each timer could be individual tuned and only the terms associated with temperature variation would effect overall system performance. The reason why this analysis includes the sample error coefficients is to allow for a unified analysis to be performed across all timers in a very conservative manner.

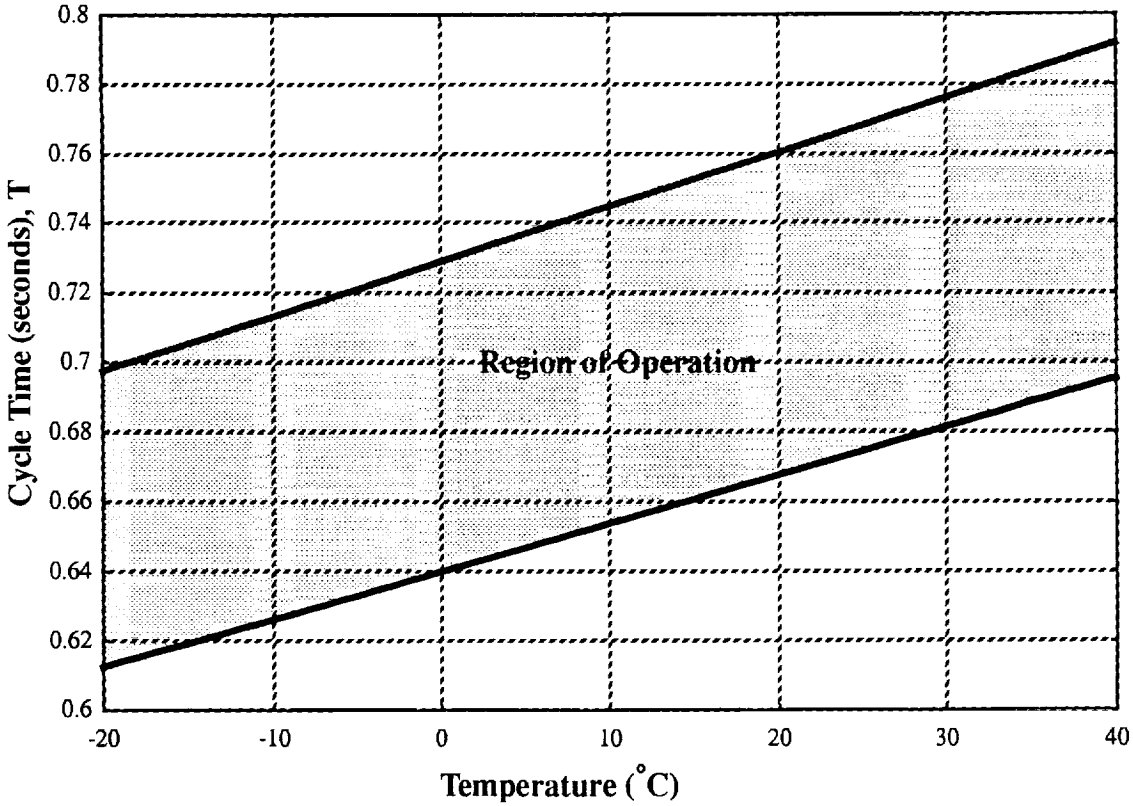


Figure 8: timer base cycle time for specified temperature range

Using the minimum cycle time shown in Figure 8 as the worst-case timer execution time, the number of cycles needed to insure that the tether is not cut prematurely can be easily computed. To accomplish this in hardware the count selection circuitry (the AND gate) will be connected using soldered jumpers (before the system is put into final flight configuration) to the output lines of the counter. The number of counts (i.e. number of timer cycles) will be selected to allow for the maximum tether deployment time scenario as described in Equation 3.

$$\text{Maximum Tether Deployment Time for Mission} \leq T_{min}N = 0.61N \quad (3)$$

where,

N = Number of Timer Cycles.

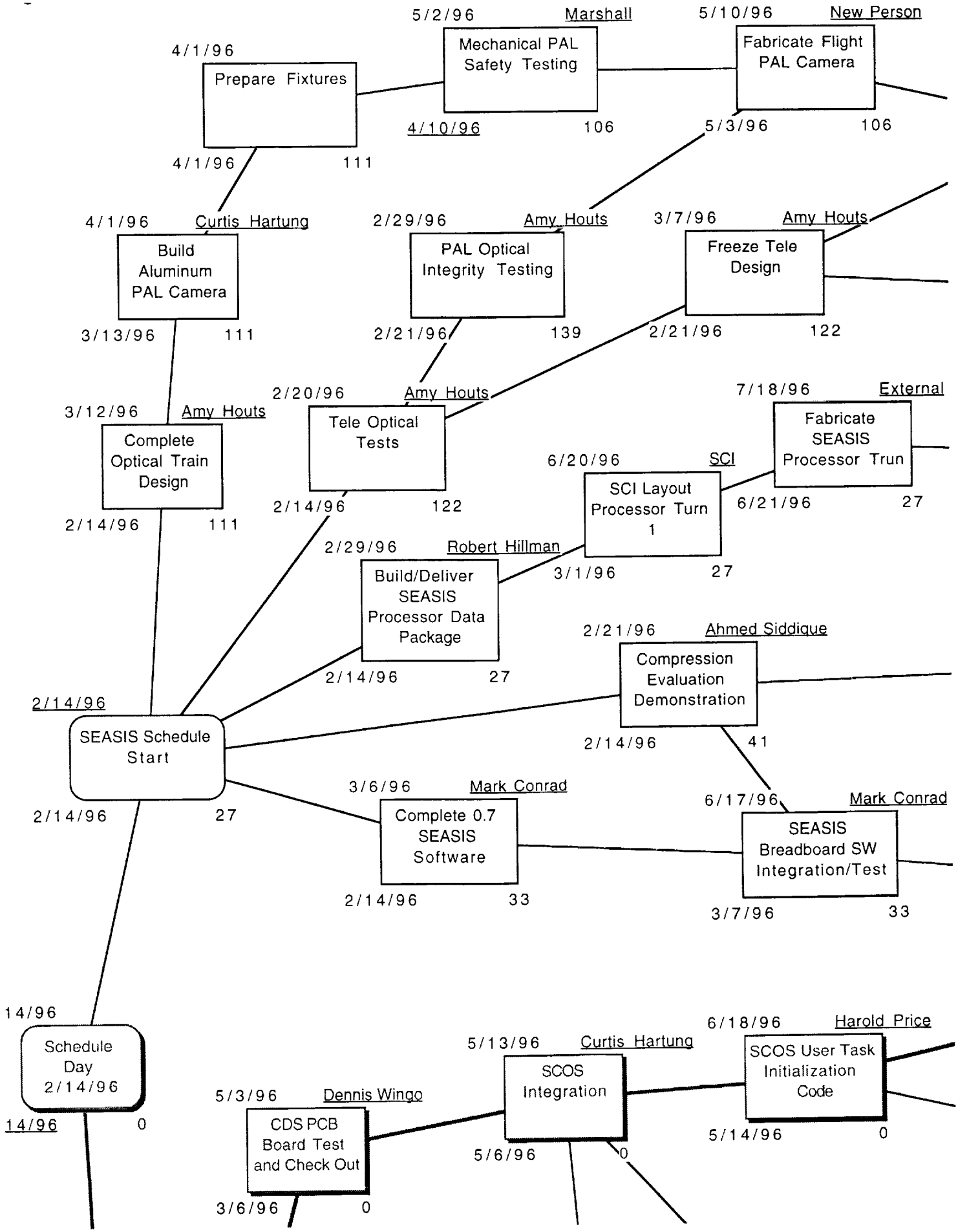
Switches

It is assumed that the separation switches and the optical isolated relay switches will be required to survive a number of vibration tests where the SEDSAT-1 is placed on the shaking apparatus at MSFC in full flight configuration. Verification of such survival will be evaluated after the test have been completed by testing that the power is inhibited when any one of the switches is disabled, in the case of the separation switches and, in the case of the optical-relay switches a test will be performed after the vibration tests which will monitor via the CDS computer the tether

cutting voltage level to insure that the 28 volts is not available until the maximum tether deployment time has expired.

Chattering in the separation switches is another concern. If chattering is defined as the momentary non-destructive activation of the switch during the launch sequence then it is very unlikely that such activity will have any credible effect on system safety. This is supported by the following observations: (1) Although the switches have not been tested on the SEDSAT-1 configuration they are robust as evidence by the manufactures specification and have been specifically designed for such applications. (2) The switches are double pole switches and in order to initiate power from the battery each switch would have to make contact with the other pole not just break contact with the original pole. (3) All three switches must make contact with the other pole simultaneously to initiate power. (4) Short periodic pulses in the power supply would not be long enough to activate the transponders or initialize the computer(s). After launch the satellite will be dead for many days giving adequate time to dissipate any transitive effects on the electronics.

Attachment 1:
SEDSAT-1 Completion Schedule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5/2/96
Marshall
Mechanical PAL Safety Testing
4/10/96
106
5/10/96
New Person
Fabricate Flight PAL Camera
5/3/96
106
4/1/96
Curtis Hartung
Build Aluminum PAL Camera
3/13/96
111
2/29/96
Amy Houts
PAL Optical Integrity Testing
2/21/96
139
3/7/96
Amy Houts
Freeze Tele Design
2/21/96
122
3/12/96
Amy Houts
Complete Optical Train Design
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111
2/20/96
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Tele Optical Tests
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2/29/96
Robert Hillman
Build/Deliver SEASIS Processor Data Package
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2/21/96
Ahmed Siddique
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Mark Conrad
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33
6/17/96
Mark Conrad
SEASIS Breadboard SW Integration/Test
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14/96
Schedule Day 2/14/96
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CDS PCB Board Test and Check Out
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SCOS Integration
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Harold Price
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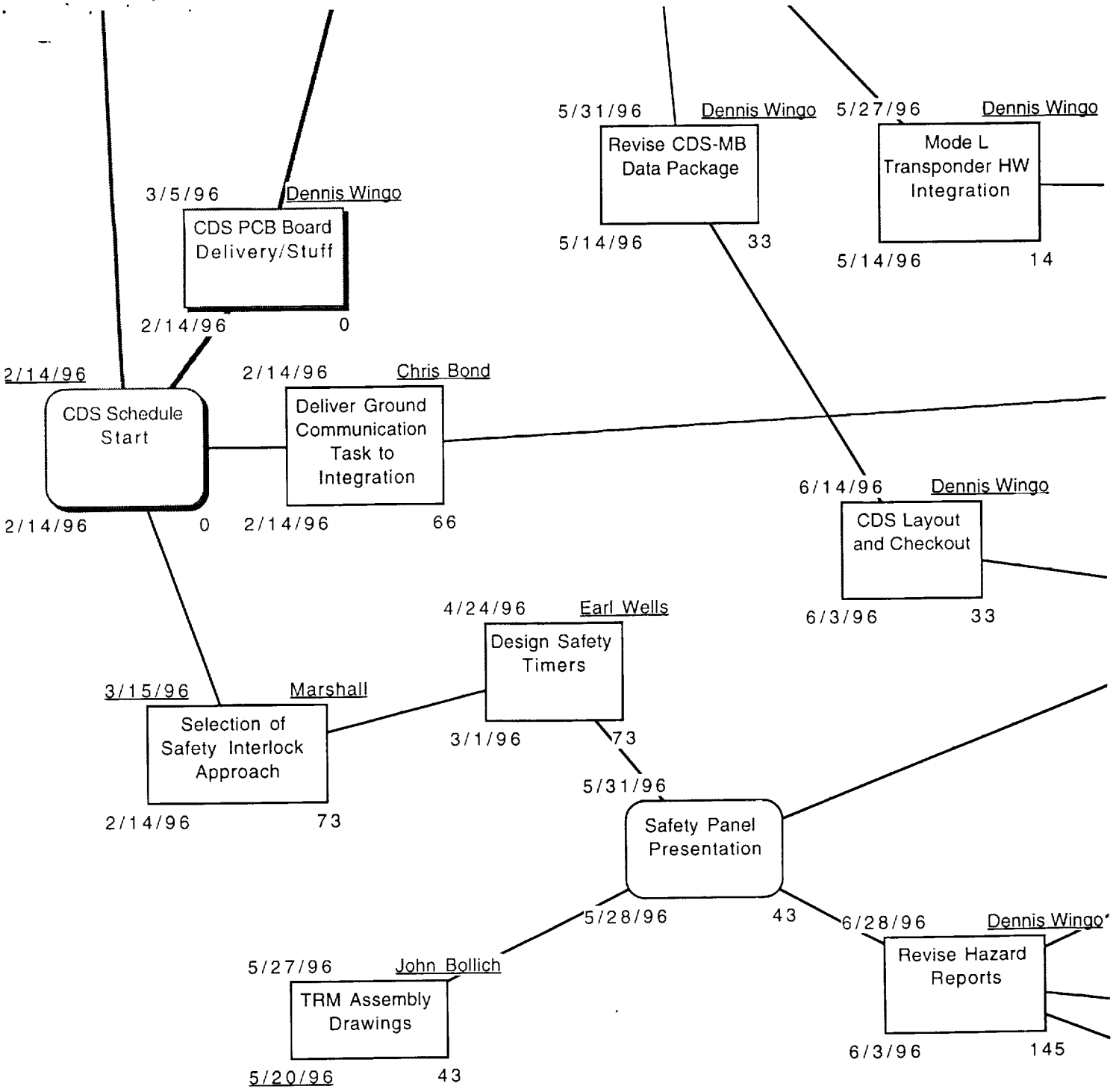
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2/14/96
CDS Schedule Start
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Chris Bond
Deliver Ground Communication Task to Integration
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66
6/14/96
Dennis Wingo
CDS Layout and Checkout
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33
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Earl Wells
Design Safety Timers
3/1/96
73
3/15/96
Marshall
Selection of Safety Interlock Approach
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73
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John Bollich
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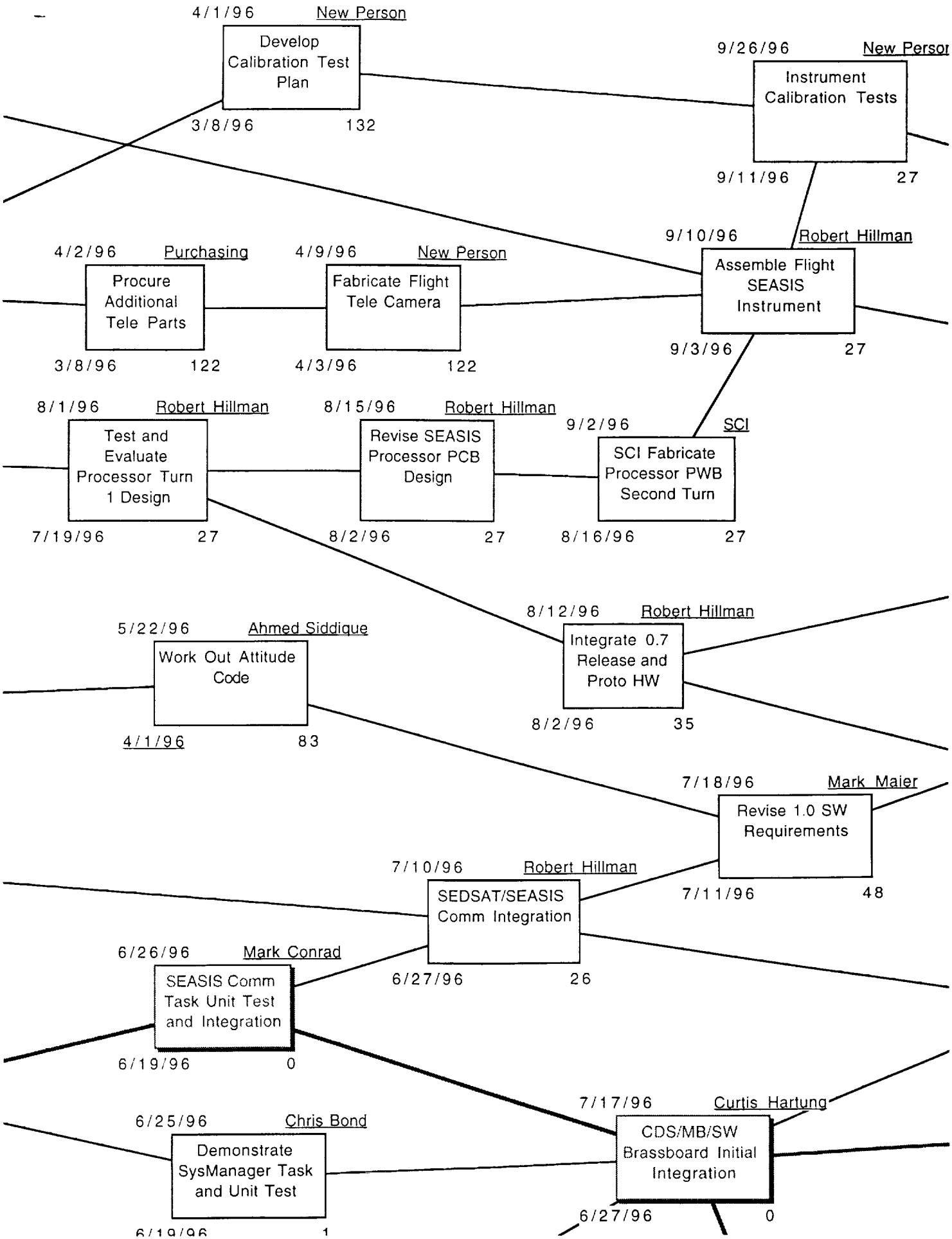
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New Person
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Robert Hillman
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8/1/96
Robert Hillman
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Robert Hillman
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9/2/96
SCI
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8/12/96
Robert Hillman
Integrate 0.7 Release and Proto HW
8/2/96
35
5/22/96
Ahmed Siddique
Work Out Attitude Code
4/1/96
83
7/18/96
Mark Maier
Revise 1.0 SW Requirements
7/11/96
48
7/10/96
Robert Hillman
SEDSAT/SEASIS Comm Integration
6/27/96
26
6/26/96
Mark Conrad
SEASIS Comm Task Unit Test and Integration
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7/17/96
Curtis Hartung
CDS/MB/SW Brassboard Initial Integration
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6/25/96
Chris Bond
Demonstrate SysManager Task and Unit Test
6/19/96
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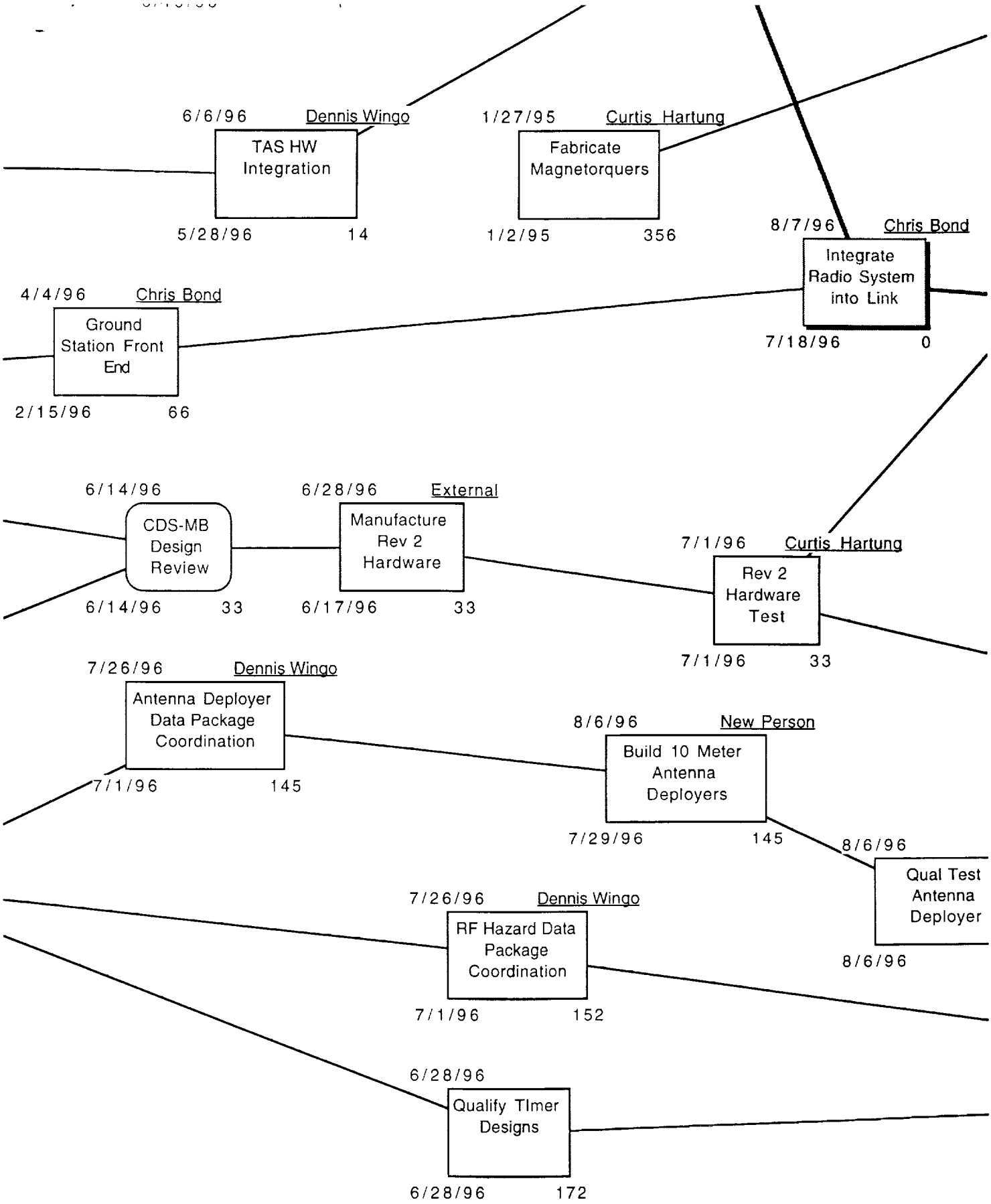
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Chris Bond
Integrate Radio System into Link
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Chris Bond
Ground Station Front End
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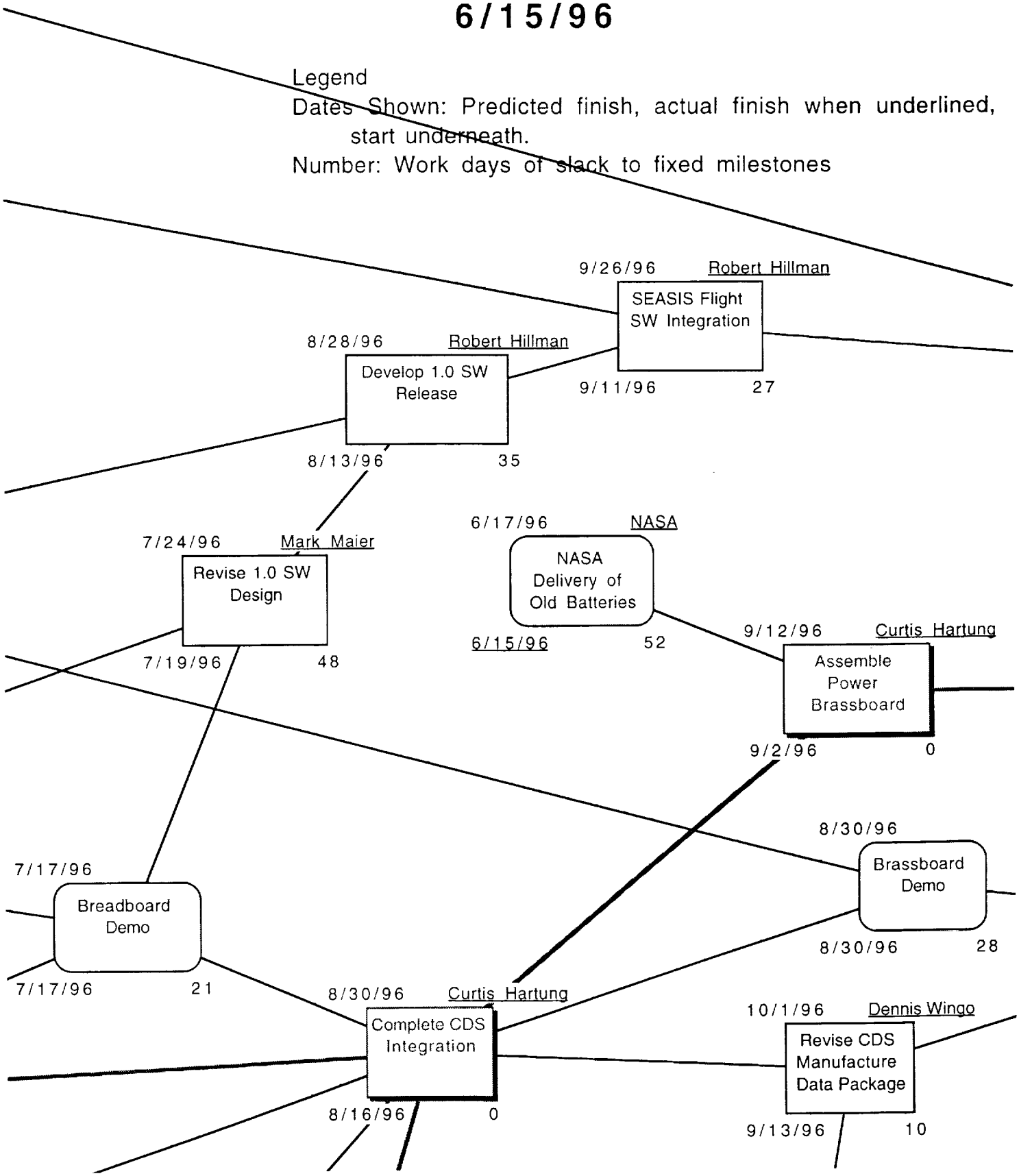
6/14/96
CDS-MB Design Review
6/14/96
33
6/28/96
External
Manufacture Rev 2 Hardware
6/17/96
33
7/1/96
Curtis Hartung
Rev 2 Hardware Test
7/1/96
33
7/26/96
Dennis Wingo
Antenna Deployer Data Package Coordination
7/1/96
145
8/6/96
New Person
Build 10 Meter Antenna Deployers
7/29/96
145
8/6/96
Qual Test Antenna Deployer
8/6/96
7/26/96
Dennis Wingo
RF Hazard Data Package Coordination
7/1/96
152
6/28/96
Qualify TImer Designs
6/28/96
172

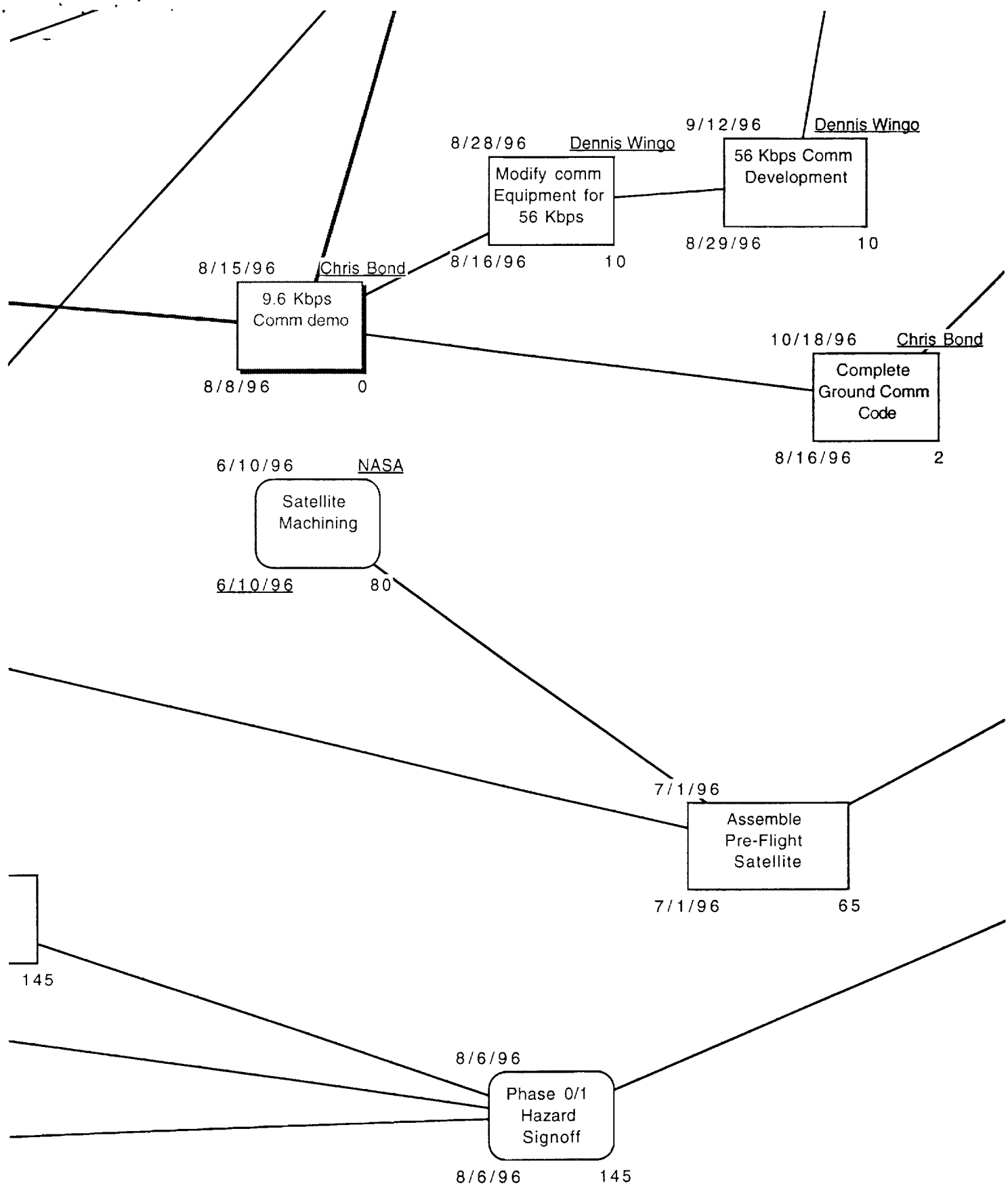
Baseline SEDSAT Task Plan
6/15/96

Legend

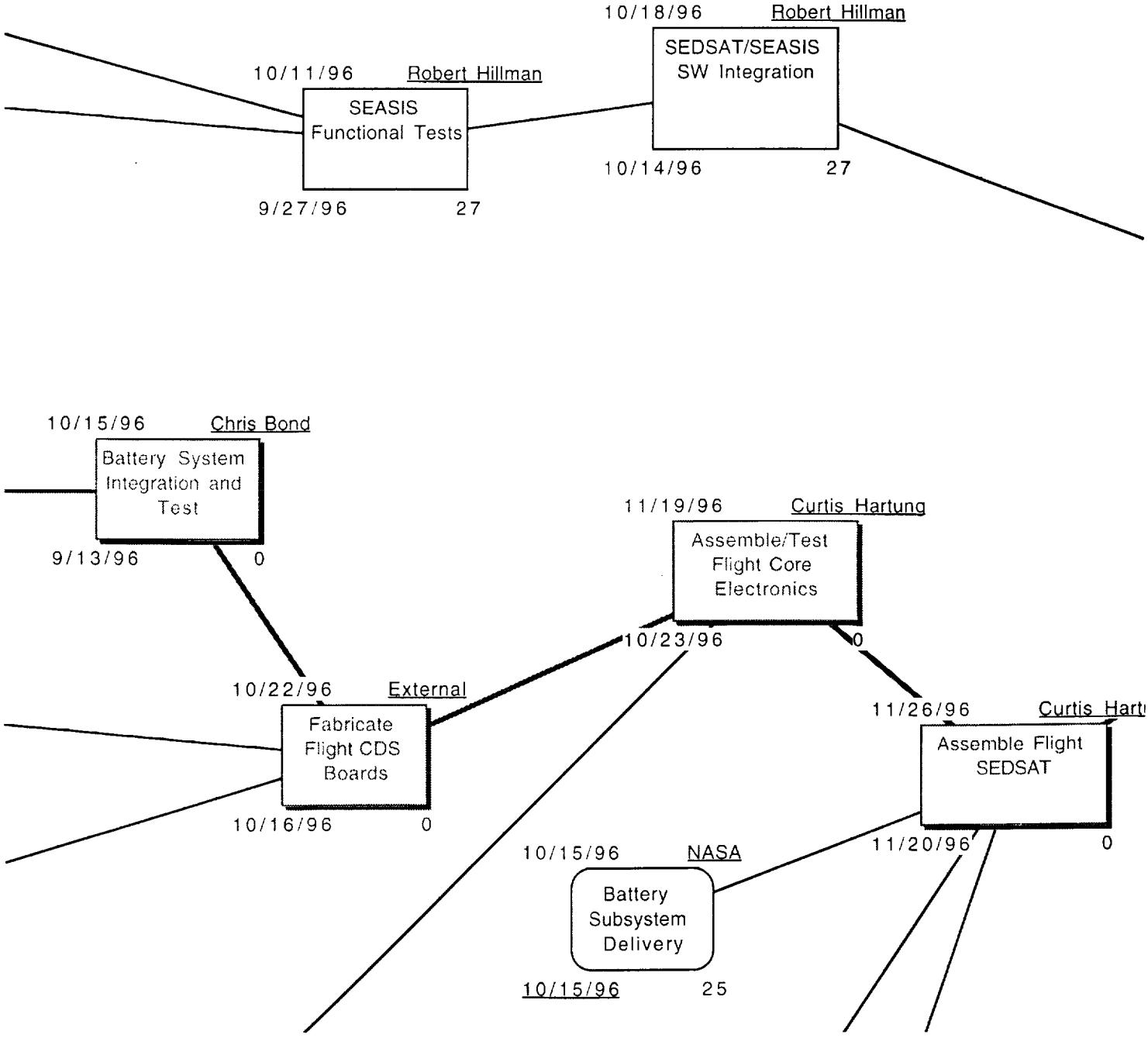
Dates Shown: Predicted finish, actual finish when underlined, start underneath.

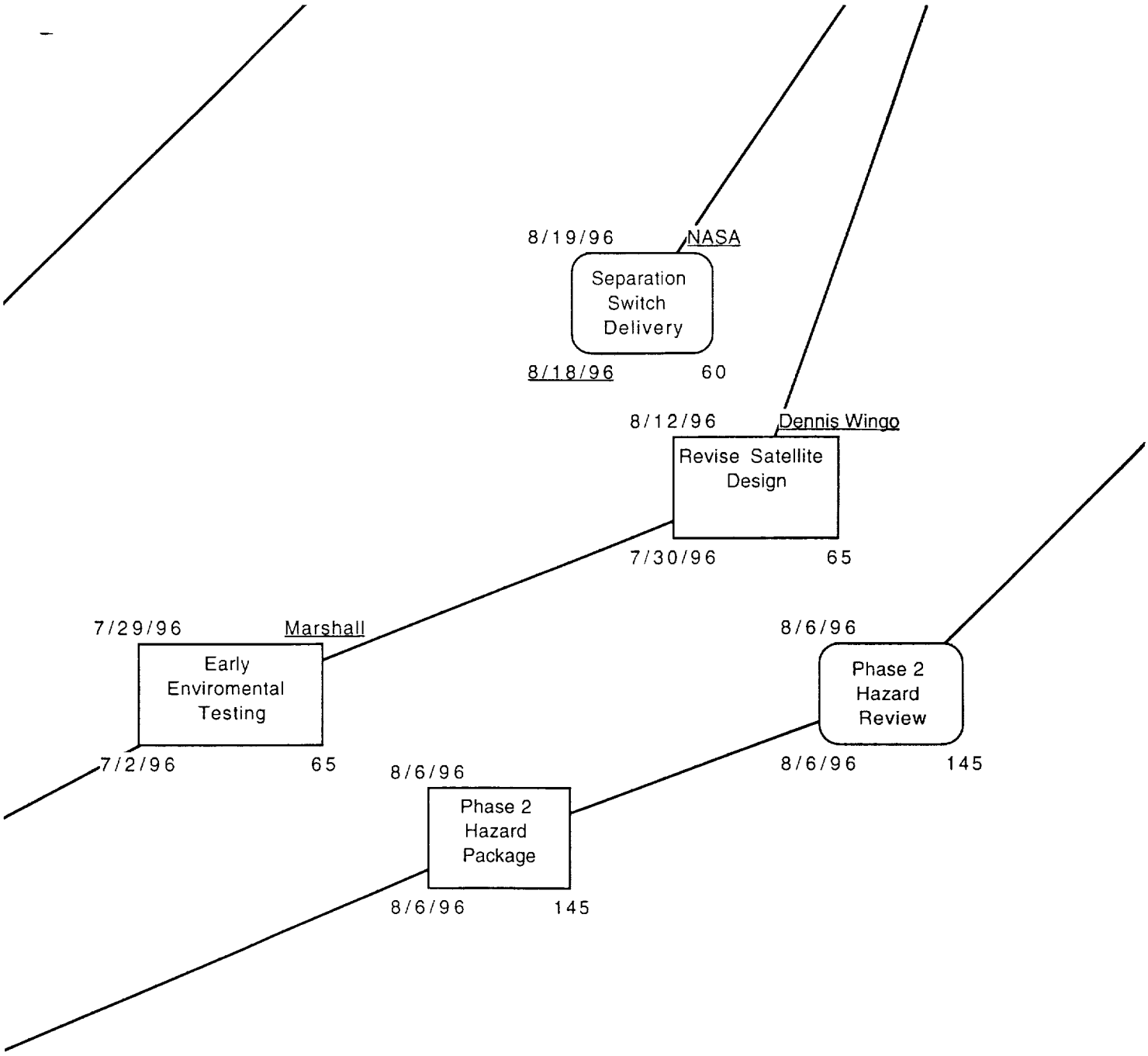
Number: Work days of slack to fixed milestones

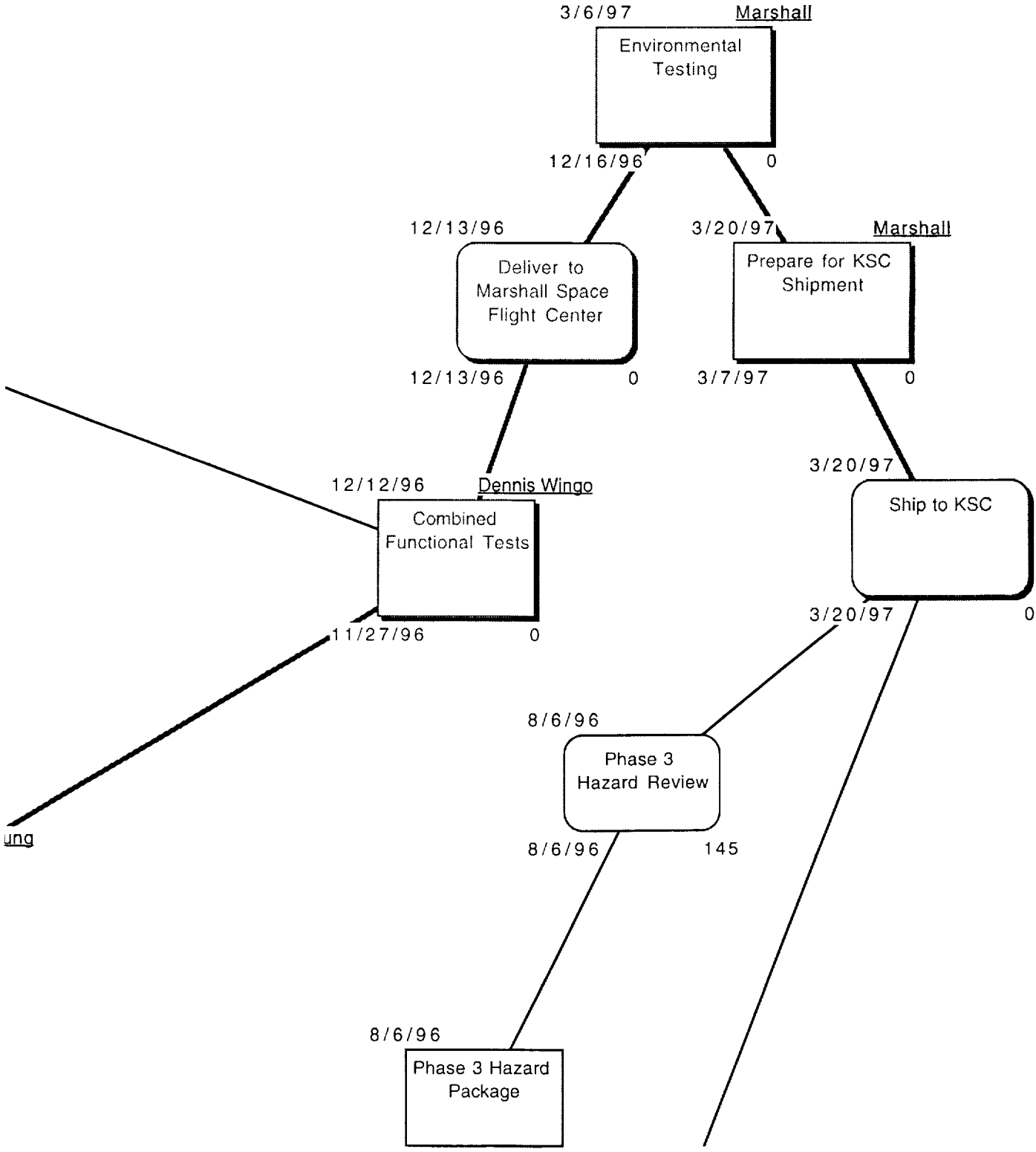


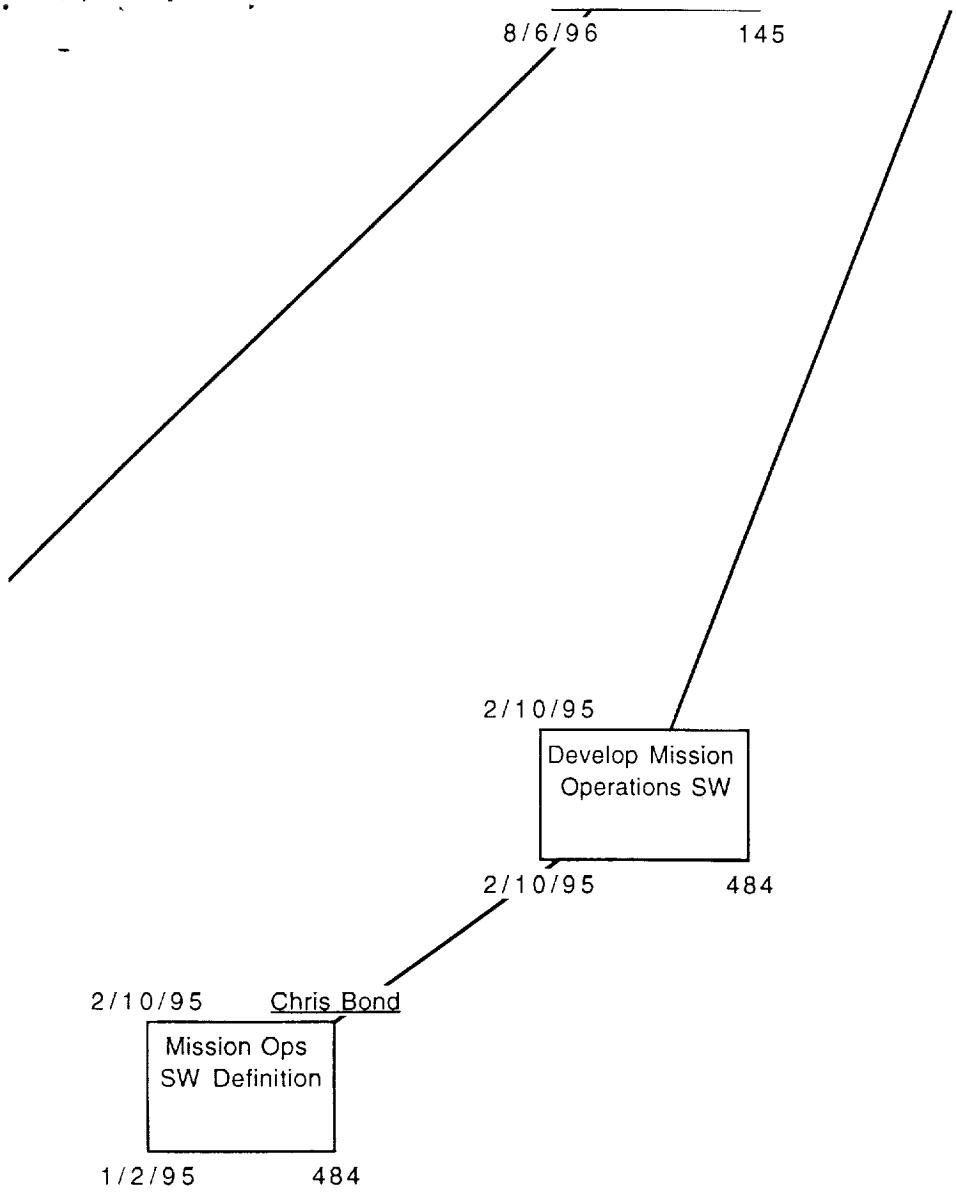

9/12/96
Dennis Wingo
8/28/96
Dennis Wingo
56 Kbps Comm Development
Modify comm Equipment for 56 Kbps
8/29/96
10
8/16/96
10
8/15/96
Chris Bond
9.6 Kbps Comm demo
8/8/96
0
10/18/96
Chris Bond
Complete Ground Comm Code
8/16/96
2
6/10/96
NASA
Satellite Machining
6/10/96
80
7/1/96
Assemble Pre-Flight Satellite
7/1/96
65
145
8/6/96
Phase 0/1 Hazard Signoff
8/6/96
145

Earliest


10/18/96
Robert Hillman
SEDSAT/SEASIS
SW Integration
10/14/96
27
10/11/96
Robert Hillman
SEASIS
Functional Tests
9/27/96
27
10/15/96
Chris Bond
Battery System
Integration and
Test
9/13/96
0
11/19/96
Curtis Hartung
Assemble/Test
Flight Core
Electronics
10/23/96
0
10/22/96
External
Fabricate
Flight CDS
Boards
10/16/96
0
11/26/96
Curtis Hart
Assemble Flight
SEDSAT
11/20/96
0
10/15/96
NASA
Battery
Subsystem
Delivery
10/15/96
25


8/19/96
NASA
Separation Switch Delivery
8/18/96
60
8/12/96
Dennis Wingo
Revise Satellite Design
7/30/96
65
7/29/96
Marshall
Early Enviromental Testing
7/2/96
65
8/6/96
Phase 2 Hazard Review
8/6/96
145
8/6/96
Phase 2 Hazard Package
8/6/96
145


3/6/97
Marshall
Environmental Testing
12/16/96
0
12/13/96
Deliver to Marshall Space Flight Center
12/13/96
0
3/20/97
Marshall
Prepare for KSC Shipment
3/7/97
0
12/12/96
Dennis Wingo
Combined Functional Tests
11/27/96
0
3/20/97
Ship to KSC
3/20/97
0
8/6/96
Phase 3 Hazard Review
8/6/96
145
8/6/96
Phase 3 Hazard Package


8/6/96
145
2/10/95
Develop Mission Operations SW
2/10/95
484
2/10/95
Chris Bond
Mission Ops SW Definition
1/2/95
484